Lab 1 Report
Digital-Analog Converter

By Ogbonnaya Okorie

Goal

Design a 5-bit R-2R ladder digital-to-analog converter (DAC).

Procedure

Drew up a schematic of a R-2R divider circuit that will be used as a base for our DAC.

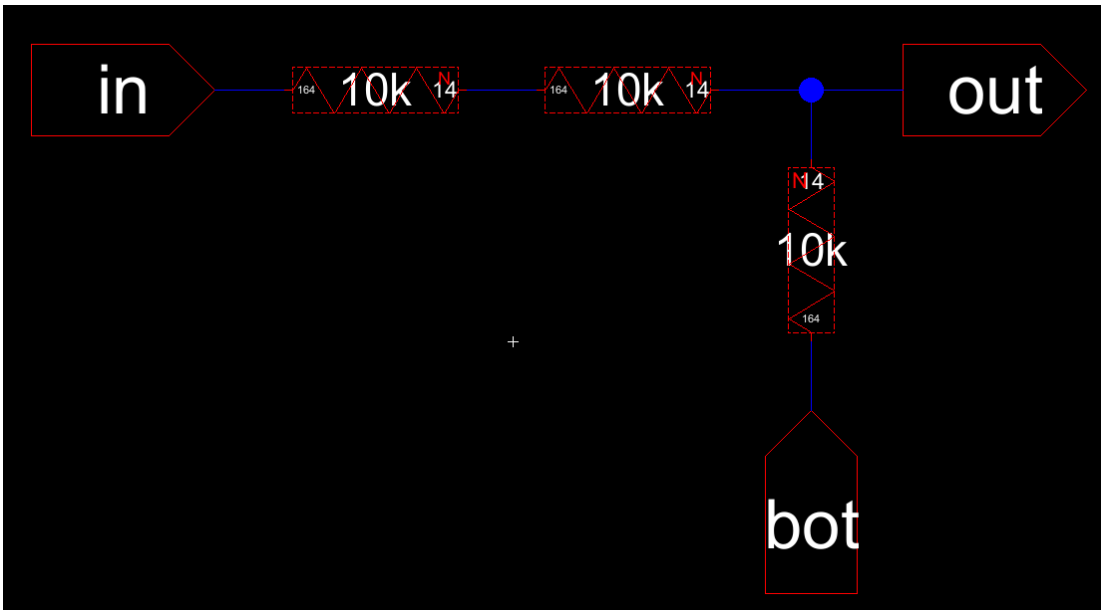

Figure 1.1: R-2R Divider

- Figure 1.2 displays the icon view of the R-2R divider, and the icon view that will be simulated

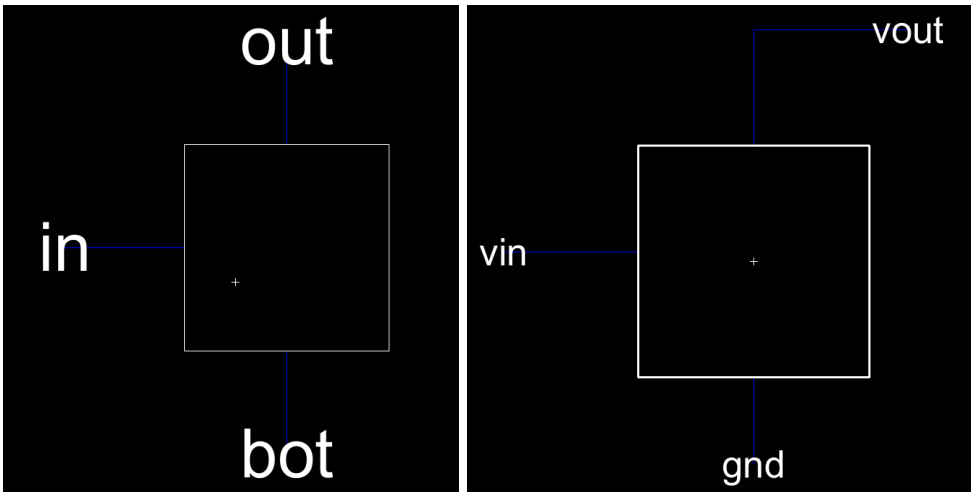

Figure 1.2: R-2R Divider Base & Sim Icon View

- Figure 1.3 displays the operating point of the R-2R divider with a voltage source of 5V.

*** SPICE deck for cell r_divider_sim{sch} from library lab_1_dac

```
        --- Operating Point ---

V(vin):         1               voltage
V(vout):        0.333333        voltage
I(Vin):         -3.33333e-005   device_current
Ix(r_divide@0:BOT):             -3.33333e-005   subckt_current
Ix(r_divide@0:IN):              3.33333e-005    subckt_current
Ix(r_divide@0:OUT):             0               subckt_current
```

Figure 1.3: R-2R Operating Point Schematic Results

- Figure 1.4 is the layout of the 10k n-well resistors in its serpentine shape to replicate the R-2R divider.
    - The 10k n-well resistor has a width of 14 and a length of 164. These values were picked based on the rough estimate of R_{square} = 855 ohms/square.
        - 10,000 ohms divided by 855 ohms/square was roughly 11.7.
        - The minimum n-well width must be 12 - I picked 14. Multiplying 14 by 11.7 gave me 163.7; I rounded up to 164.
- Figure 1.5 is the operating point results of the layout.

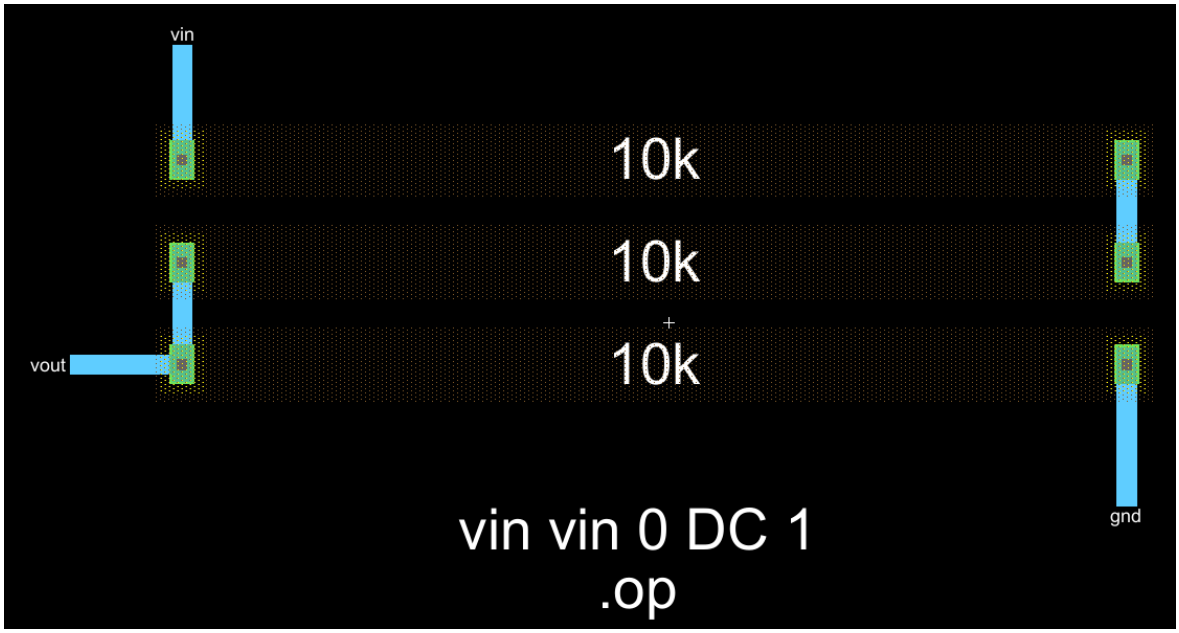

Figure 1.4: Layout of R-2R Divider

```
*** SPICE deck for cell r_divider_sim{lay} from library lab_1_dac

        --- Operating Point ---

V(vin):         1               voltage
V(vout):        0.333333        voltage
I(Vin):         -3.33333e-005   device_current
Ix(r_divide@0:BOT):             -3.33333e-005   subckt_current
Ix(r_divide@0:IN):              3.33333e-005    subckt_current
Ix(r_divide@0:OUT):             0               subckt_current
```

Figure 1.5: R-2R Operating Point Layout Results

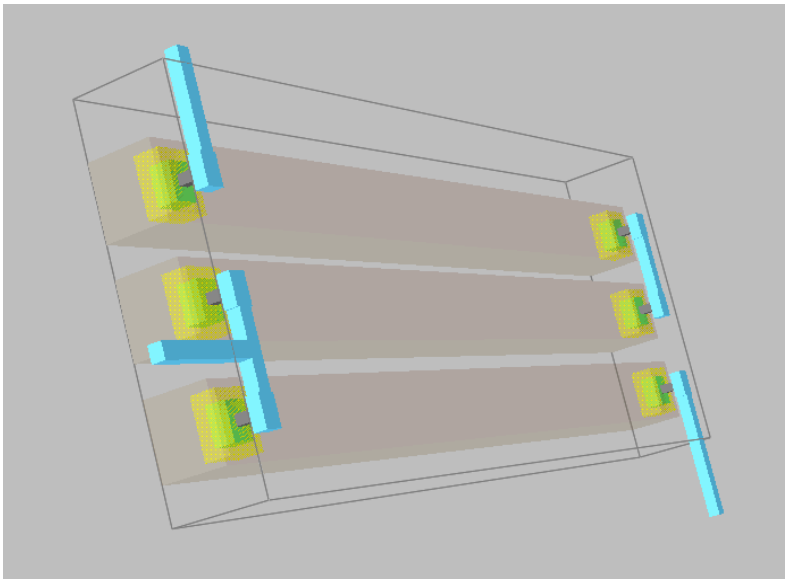

Figure 1.6: 3D Layout View of R-2R Divider

To construct the DAC, I cascade the R-2R divider in a 5-bit ladder, also adding another 10k ohm resistor in series at the ground.

- For an ideal R-2R ladder, if all resistances are the same, the output resistance of the DAC is R. In this case R is 10k ohms; so the output resistance of the DAC is 10k ohms.

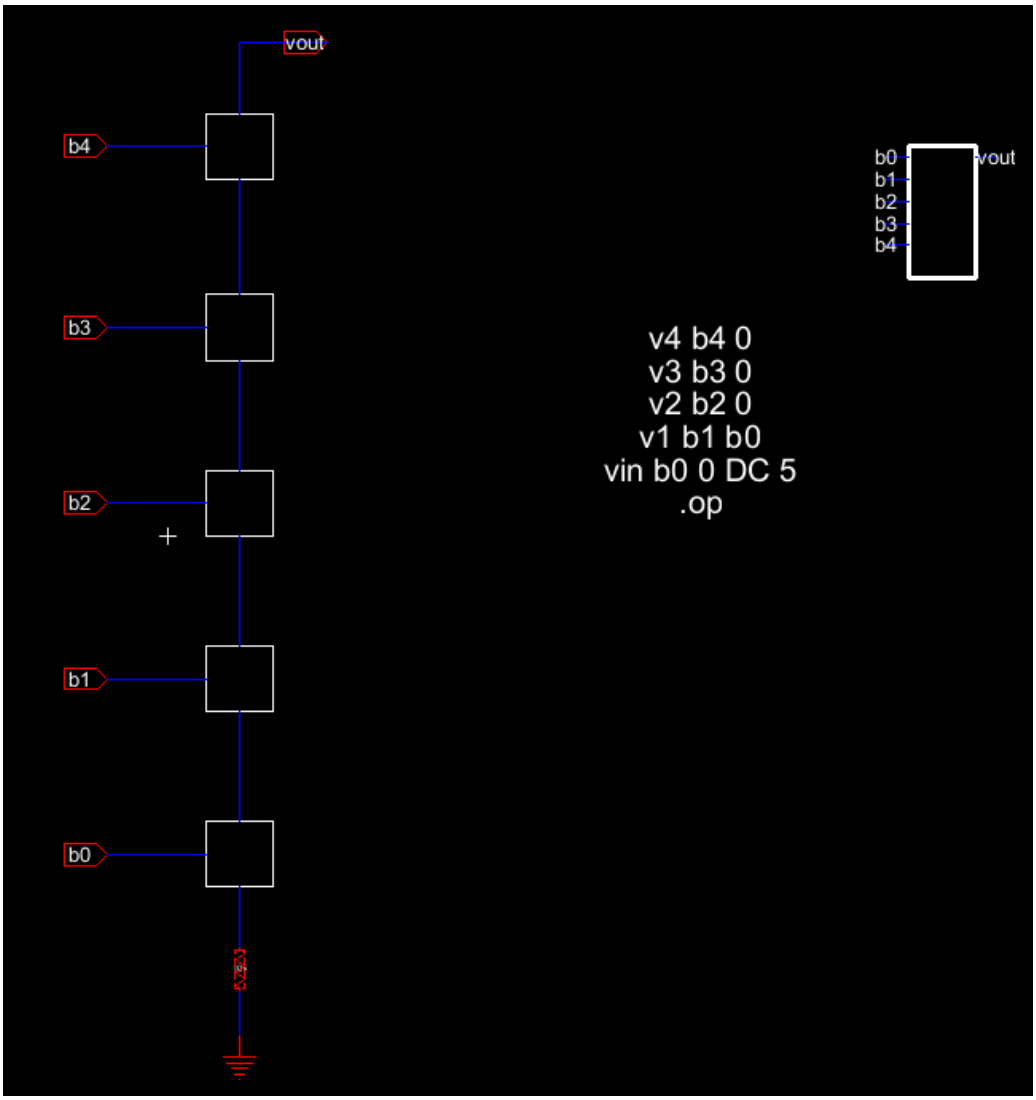

Figure 2.1: DAC Schematic

- Figure 2.2 displays the icon view of the DAC.

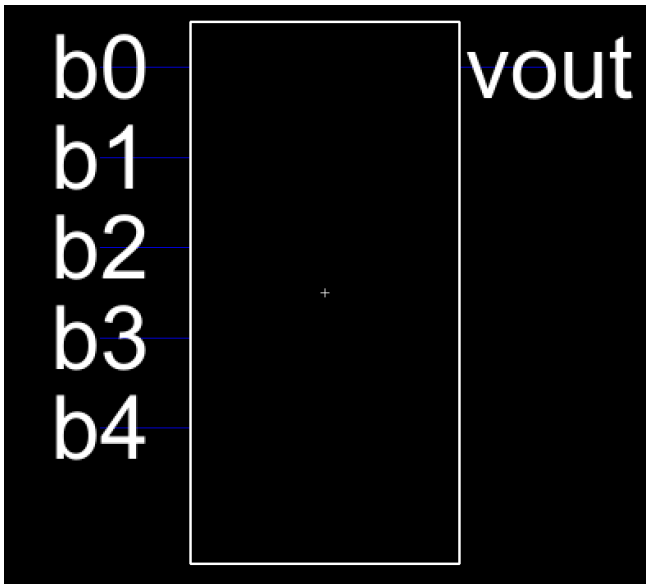

Figure 2.2: DAC Icon View

- Figure 2.3 displays the operating point of the DAC with a voltage source of 5V.

```
*** SPICE deck for cell dac_sim{sch} from library lab_1_dac

        --- Operating Point ---

V(b2):          0               voltage
V(b3):          0               voltage
V(b0):          5               voltage
V(b4):          0               voltage
V(vout):        0.46875         voltage
V(b1):          5               voltage
I(Vin):         -0.000248535    device_current
I(V1):          -0.000124023    device_current
I(V2):          6.44531e-005    device_current
I(V3):          3.51562e-005    device_current
I(V4):          2.34375e-005    device_current
Ix(dac@0:B0):   0.000124512     subckt_current
Ix(dac@0:B1):   0.000124023     subckt_current
Ix(dac@0:B2):   -6.44531e-005   subckt_current
Ix(dac@0:B3):   -3.51562e-005   subckt_current
Ix(dac@0:B4):   -2.34375e-005   subckt_current
Ix(dac@0:GND):  -0.000125488    subckt_current
Ix(dac@0:VOUT):                 0               subckt_current
```

Figure 2.3: DAC Operating Point Schematic Results

- Figure 2.4 is the layout of the DAC in its serpentine pattern. Figure 2.5 is the operating point results of the layout.

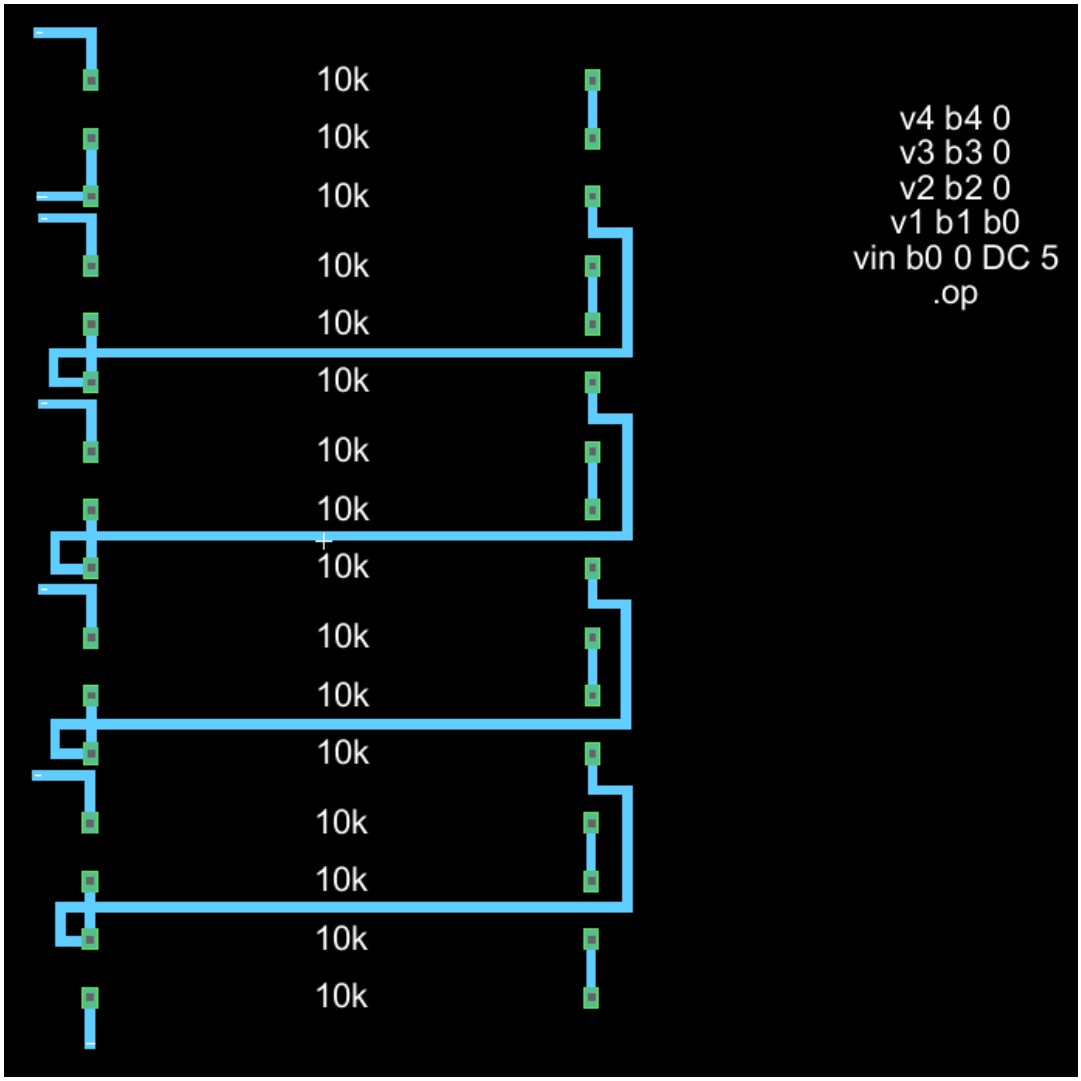

Figure 2.4: Layout of DAC

*** SPICE deck for cell dac_sim{lay} from library lab_1_dac

```
        --- Operating Point ---

V(b4):          0               voltage
V(vout):        0.46875         voltage
V(b3):          0               voltage
V(b2):          0               voltage
V(b1):          5               voltage
V(b0):          5               voltage
I(Vin):         -0.000248535    device_current
I(V1):          -0.000124023    device_current
I(V2):          6.44531e-005    device_current
I(V3):          3.51562e-005    device_current
I(V4):          2.34375e-005    device_current
Ix(dac@2:B0):   0.000124512     subckt_current
Ix(dac@2:B1):   0.000124023     subckt_current
Ix(dac@2:B2):   -6.44531e-005   subckt_current
Ix(dac@2:B3):   -3.51562e-005   subckt_current
Ix(dac@2:B4):   -2.34375e-005   subckt_current
Ix(dac@2:GND):  -0.000125488    subckt_current
Ix(dac@2:VOUT):                 0               subckt_current
```

Figure 2.5: DAC Operating Point Layout Results

- Figure 2.6 is the 3D layout of the DAC.

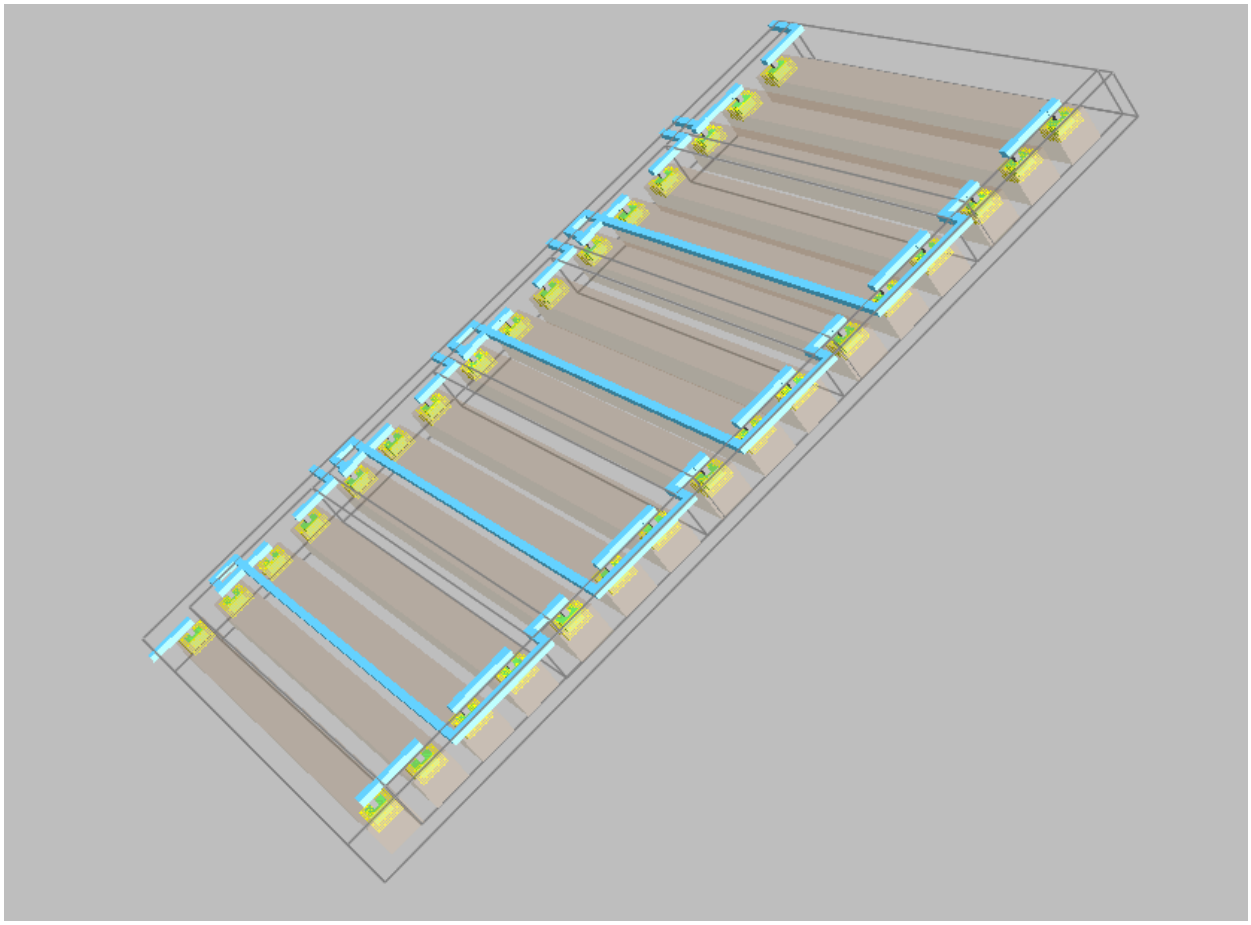

Figure 2.6: 3D Layout View of DAC

- Figure 3.1 displays the DAC schematic and icon where all of bits 0-3 are grounded, but bit 4 has an input voltage of 5V.
    - Figure 3.2 is the operating point of the grounded DAC schematic.

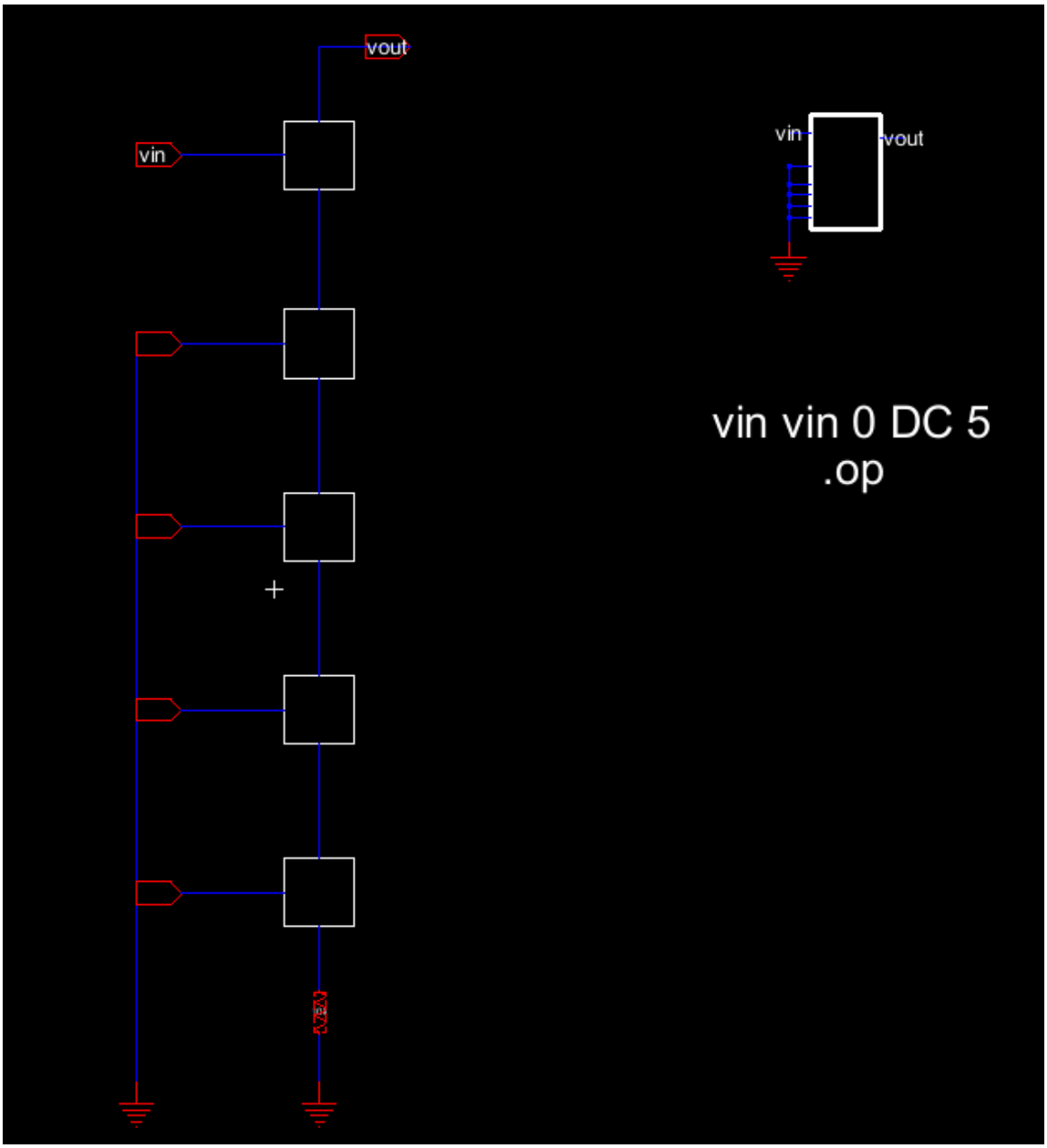

Figure 3.1: Grounded DAC Schematic & Icon

*** SPICE deck for cell dac_gnd_sim{sch} from library lab_1_dac

```
      --- Operating Point ---

V(vin):          5              voltage
V(vout):         2.5            voltage
I(Vin):          -0.000125      device_current
Ix(dac_gnd@0:VIN):              0.000125       subckt_current
Ix(dac_gnd@0:VOUT):             -8.13152e-020  subckt_current
```

Figure 3.2: Grounded DAC Operating Points

- Figure 4.1 shows the grounded DAC schematic and icon with a 10 pF capacitor load.

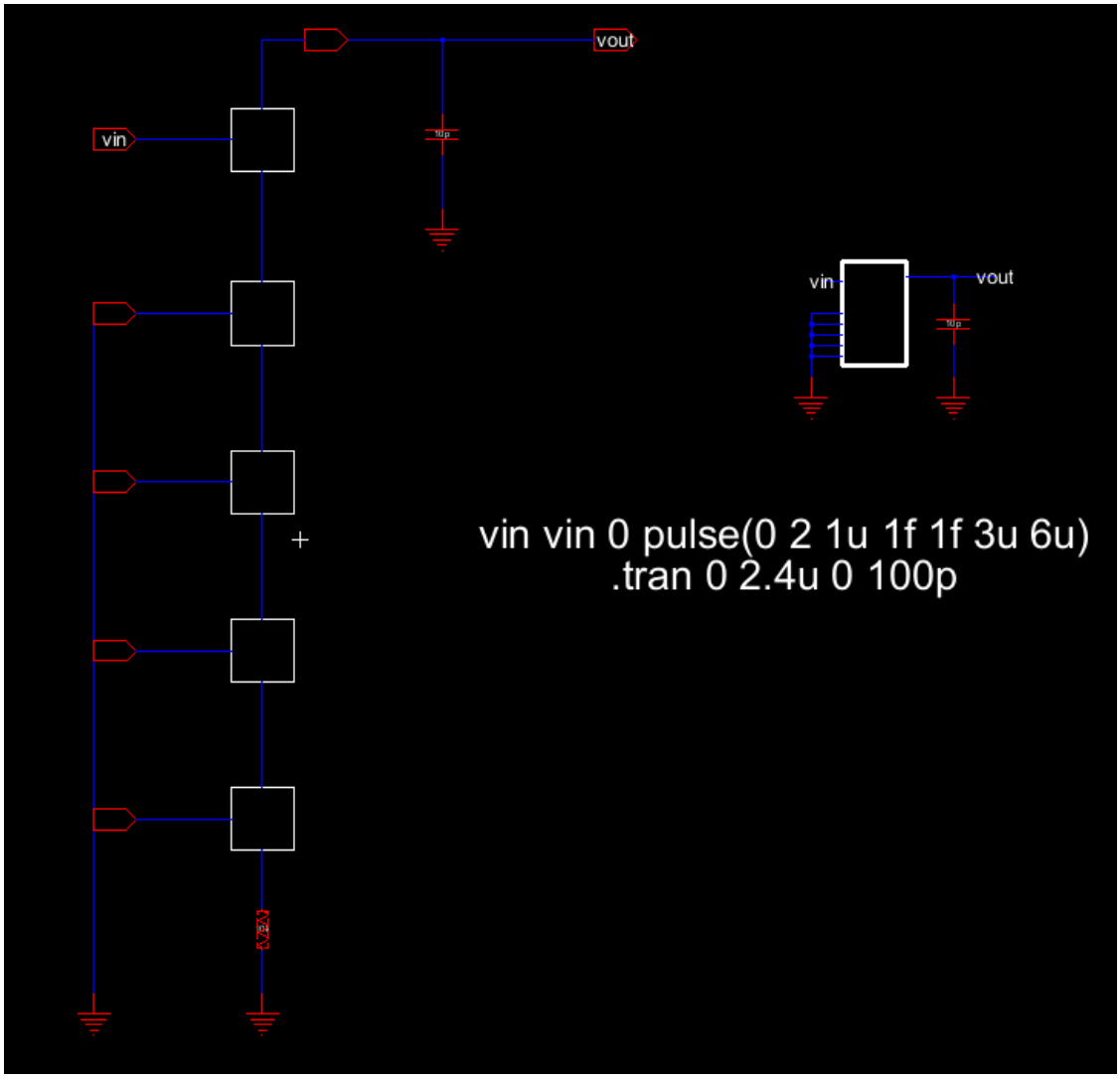

Figure 4.1: DAC with 10 pF Capacitor Load Schematic & Icon

- Figure 4.2 is a simulation of the capacitor at V_{out} being charged over time.
  - Hand calculations of the delay of the DAC is 0.7RC = (0.7)(10kohms)(10pf) = 70ns
  - Simulation observation agrees with hand calculations.

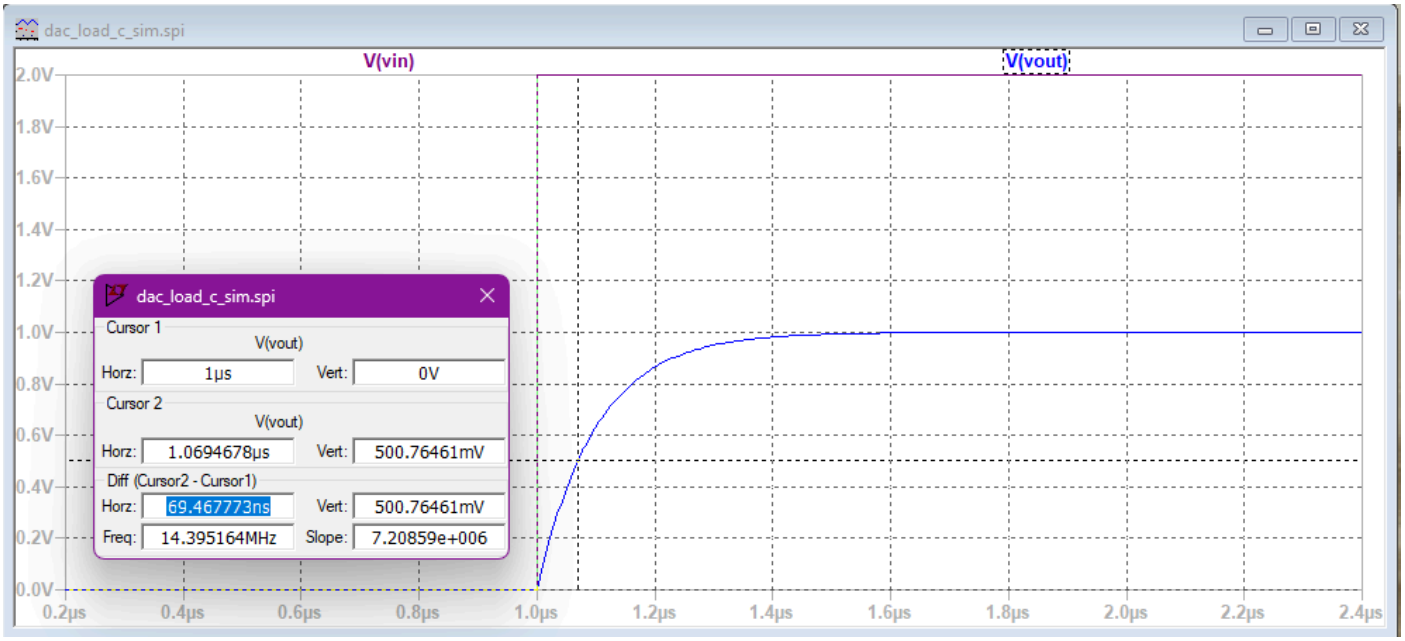

Figure 4.1: Simulation of DAC with 10 pF Capacitor Load

- Figure 5.1 shows the grounded DAC schematic and icon with a 10 pF capacitor and a 10k ohm load.
    - Adding a 10k ohm load changes the overall resistance of the DAC; the 10k ohm load is parallel to the 5-bit DAC, so the resistance changes as follows:
        - $R = R_{DAC} \parallel R_{load} = (R_{DAC} * R_{load}) / (R_{DAC} + R_{load}) = (10k * 10\ k) / (10k + 10k) = 5k$ ohms

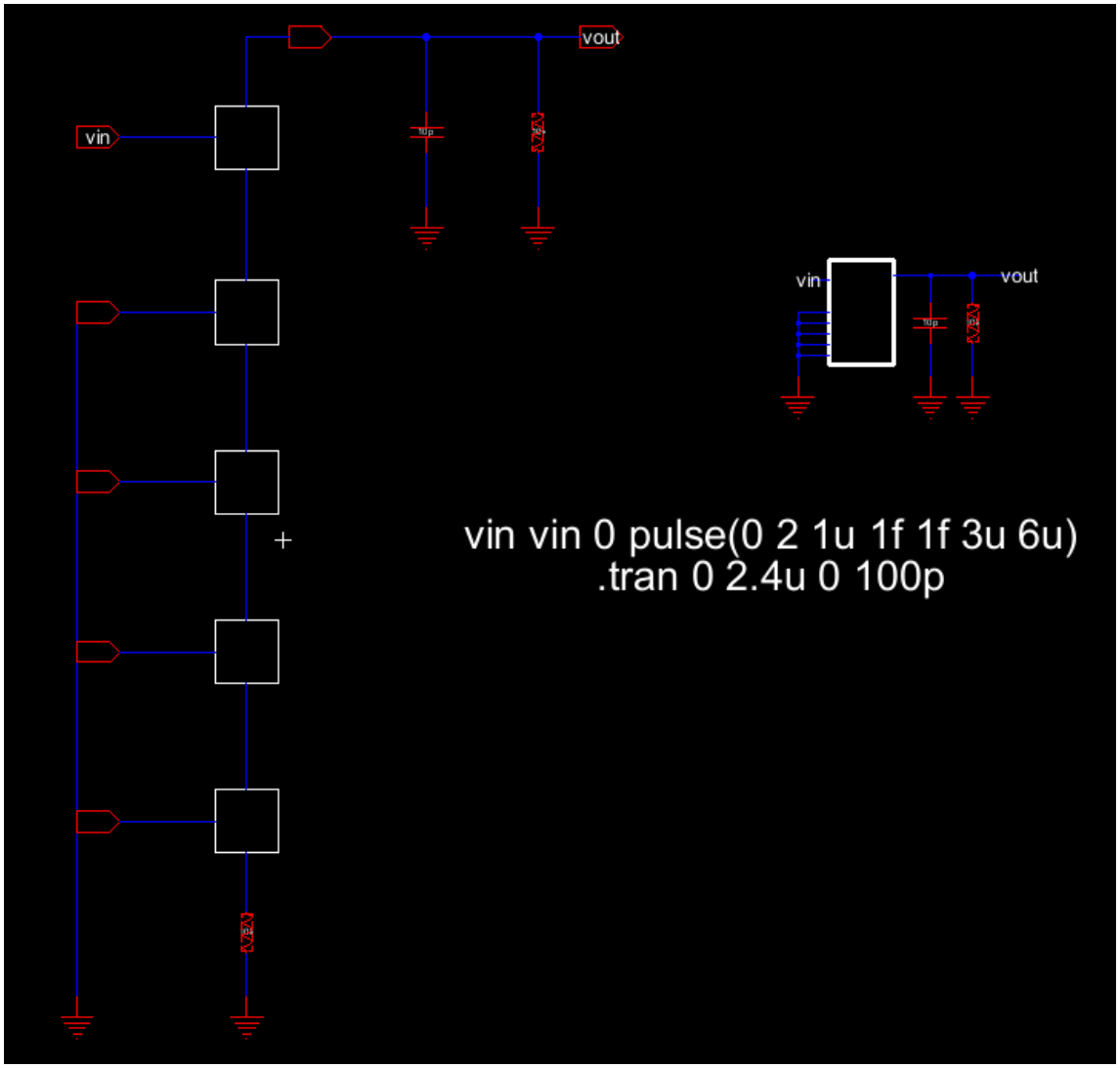

Figure 5.1: DAC with 10 pF Capacitor and 10k ohm Load Schematic & Icon

- Figure 5.2 is a simulation of the V_{out} being charged over time; the delay is halved from the previous schematic.
    - Hand calculations of the delay of the DAC is 0.7RC = (0.7)(5kohms)(10pf) = 35ns
    - Simulation observation agrees with hand calculations.

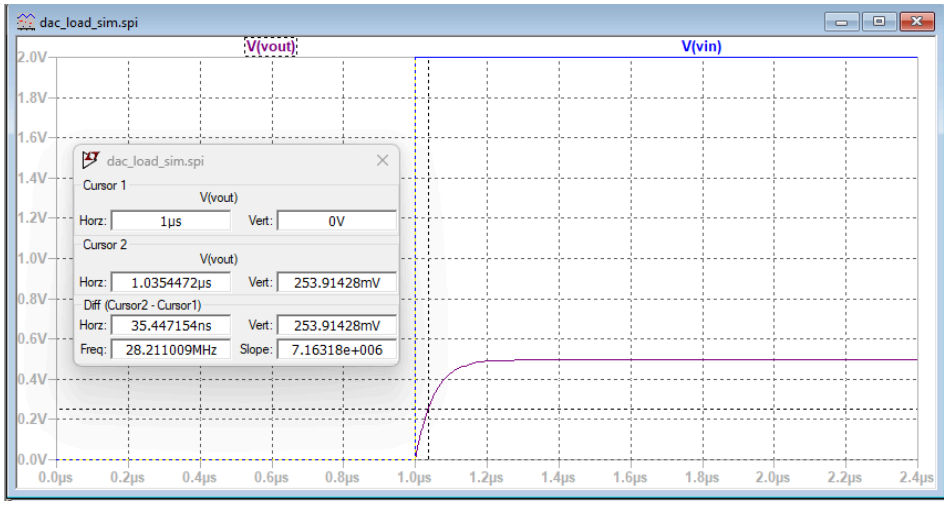

Figure 5.1: Simulation of DAC with 10 pF Capacitor and 10k ohm Load

DRC and LVS Check

```
Checking schematic cell 'r_divider{sch}'
   No errors found
Checking schematic cell 'dac{sch}'
   No errors found
Checking schematic cell 'dac_gnd{sch}'
   No errors found
Checking schematic cell 'dac_load{sch}'
   No errors found
Checking icon cell 'r_divider{ic}'
   No errors found
0 errors and 0 warnings found (took 0.001 secs)
```

Figure 6.1: DRC Check on DAC with Load

```
                                  ---
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 13 networks
0 errors and 0 warnings found (took 0.003 secs)
```

Figure 6.2: LVS Check on DAC