Lab 4 Report
Inverters

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Goal

Understand how to lay out an inverter and its functionality based on different PMOS & NMOS lengths and widths. We will also attach loads to the inverters and also understand their functionality with the loads.

Procedure

An inverter is created with a PMOS and NMOS connected together at the drain. V_{dd} is connected to the source of the PMOS and ground is connected to the source of the NMOS.

The “in” connection is connected to the gates of the MOSFETs, and the “out” connection is connected to the drains of the MOSFETs.

- Below are the schematic, icon, and layout views of an inverter. This inverter has a 12x6 PMOS and a 6x6 NMOS.

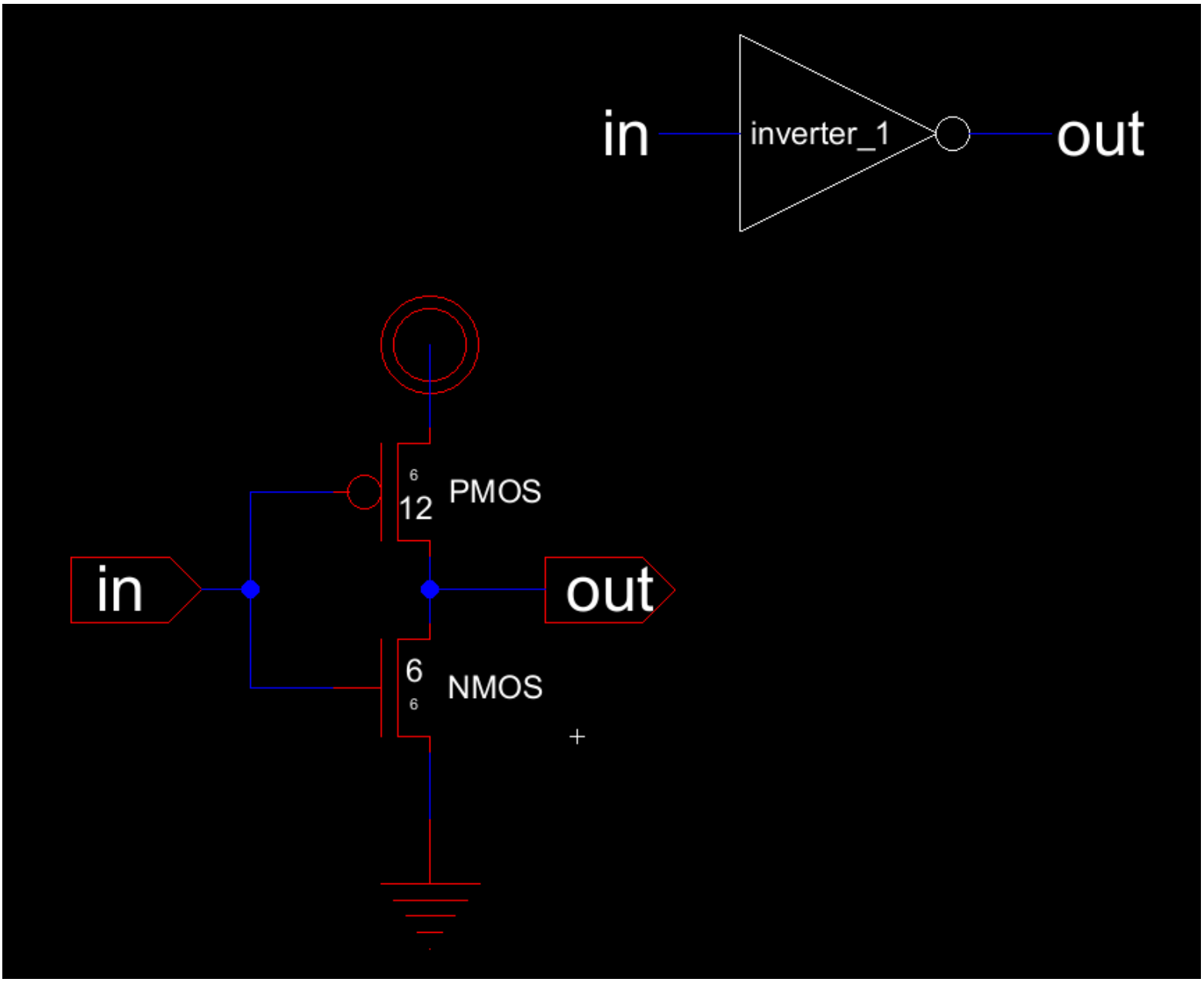

Figure 1.1: Inverter Schematic and Icon

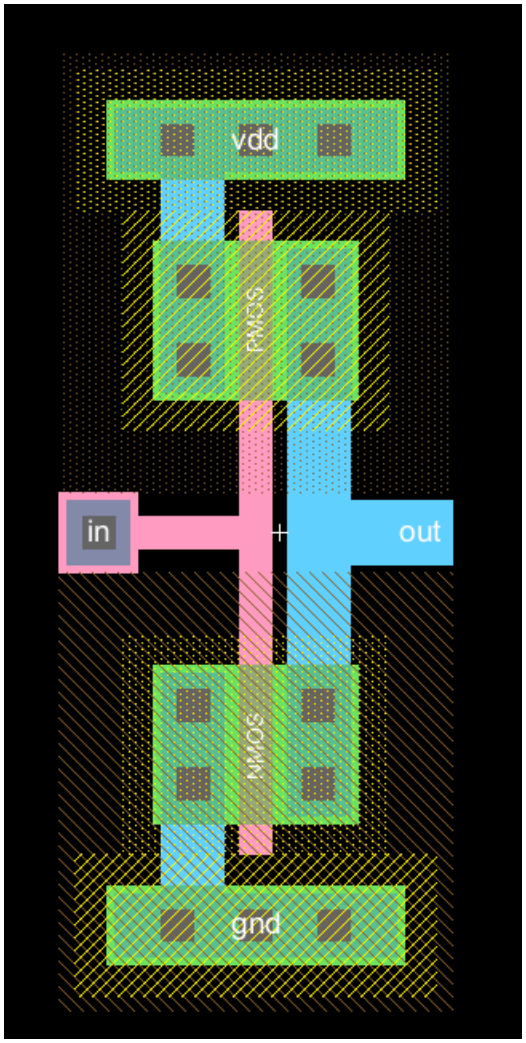

Figure 1.2: Inverter Layout

NOTE: The number of NMOS and PMOS devices on the layout is based on the division of the NMOS…
In this case, 6/6 = 1, so 1 NMOS & PMOS.

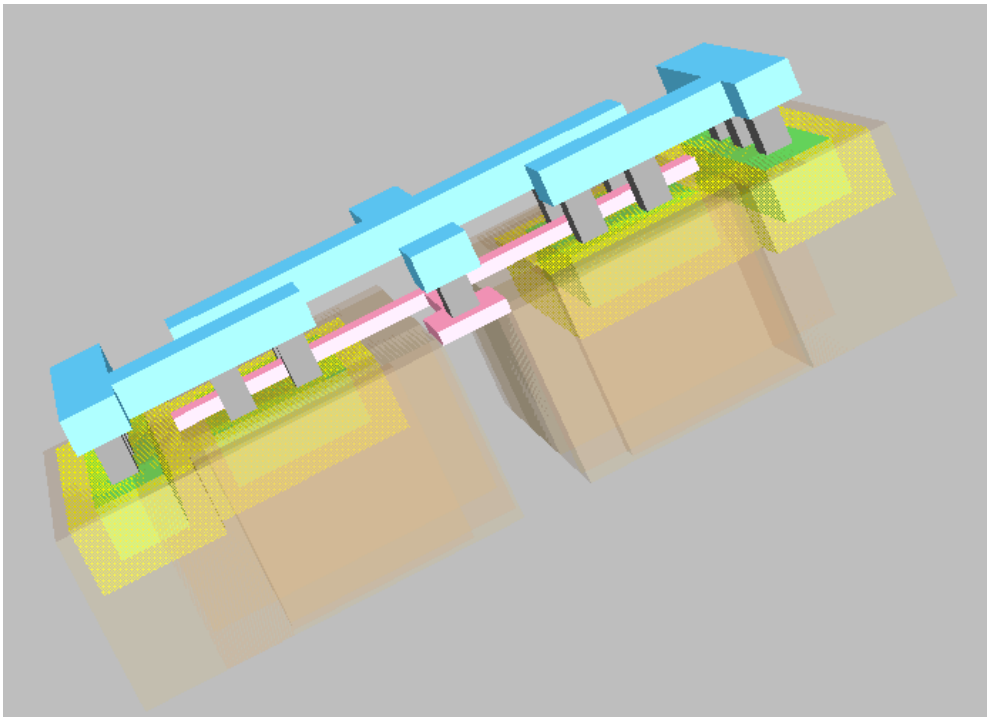

Figure 1.3: 3D View of Inverter Layout

- Below are the schematic, icon, and layout views of an inverter. This inverter has a 12x6 PMOS and a 6x6 NMOS.

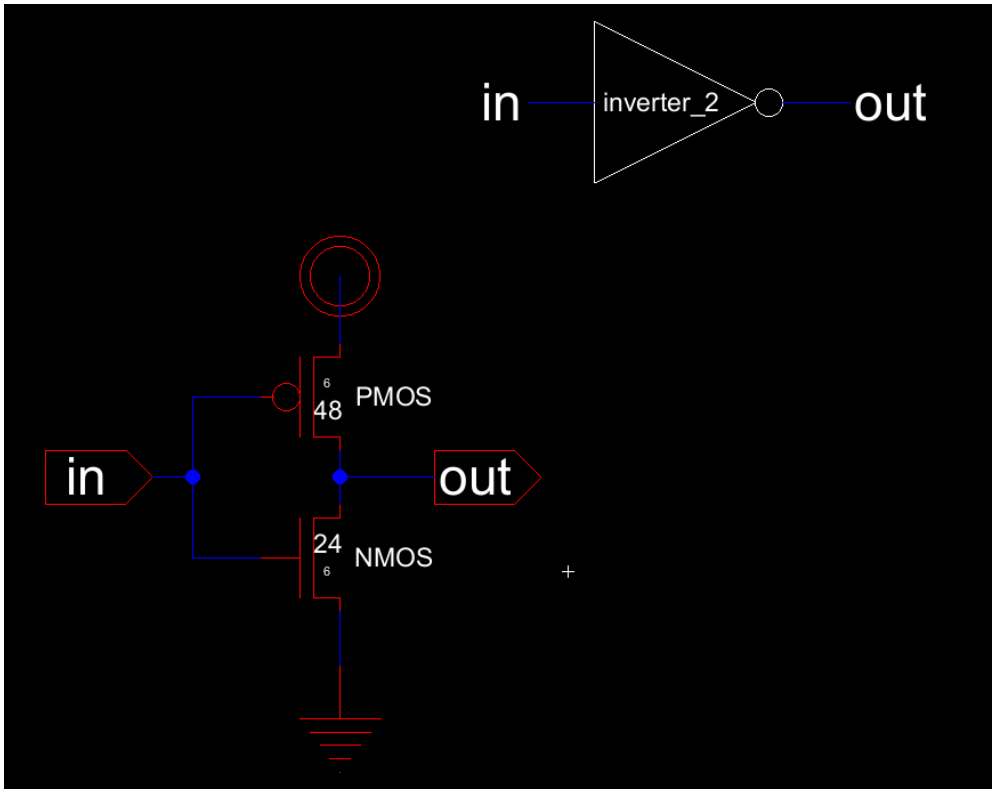

Figure 2.1: 4-MOSFET-Cascaded Inverter Schematic and Icon

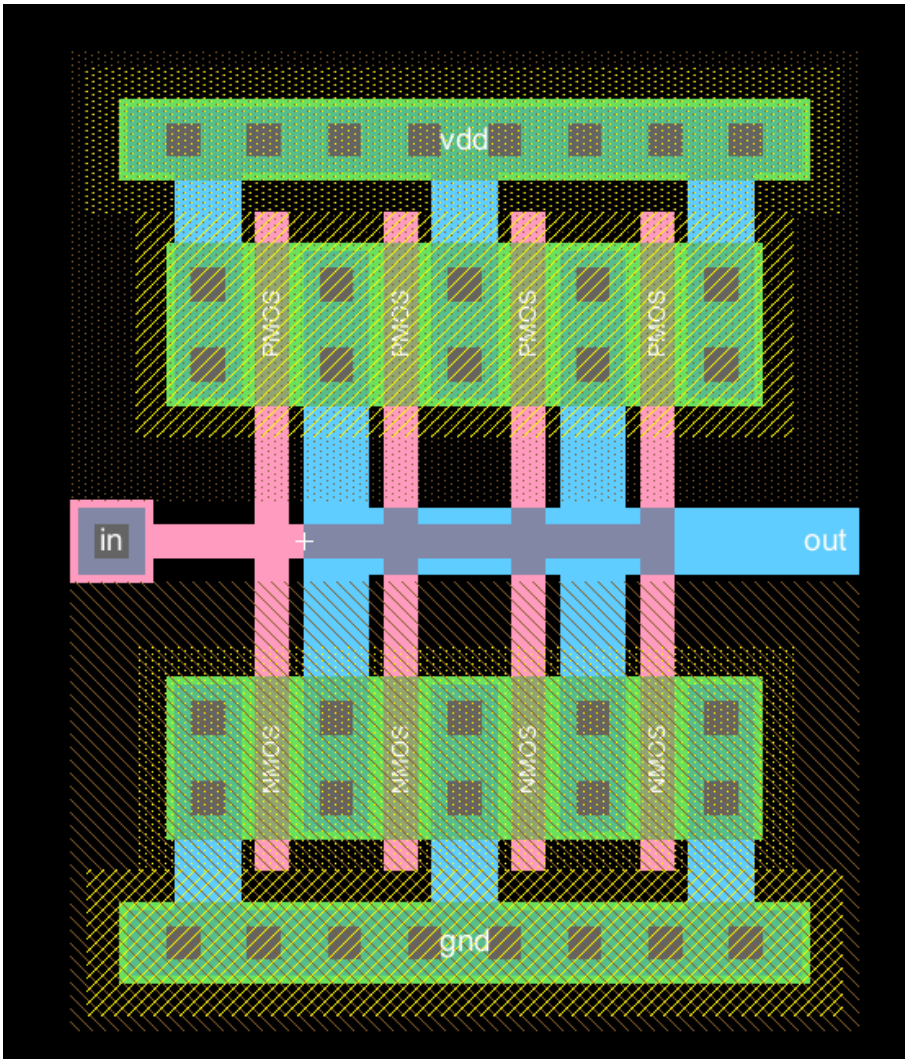

Figure 2.2: 4-MOSFET-Cascaded Inverter Layout

NOTE: The number of NMOS and PMOS devices on the layout is based on the division of the NMOS…
In this case, 24/6 = 1, so 4 NMOS & PMOS.

The MOSFETs are laid out as such for convenient spacing and placement of drains and sources:

- The two NMOS in the middle are connected with their sources; with that in mind, the "out" is connected to the drains of the NMOS.
- The two PMOS in the middle are also connected with their sources; the "out" is connected to the drains of the PMOS.
- V_{dd} is connected to the sources of the PMOS, and ground is connected to the sources of the NMOS, so everything passes in terms of MOSFET configuration

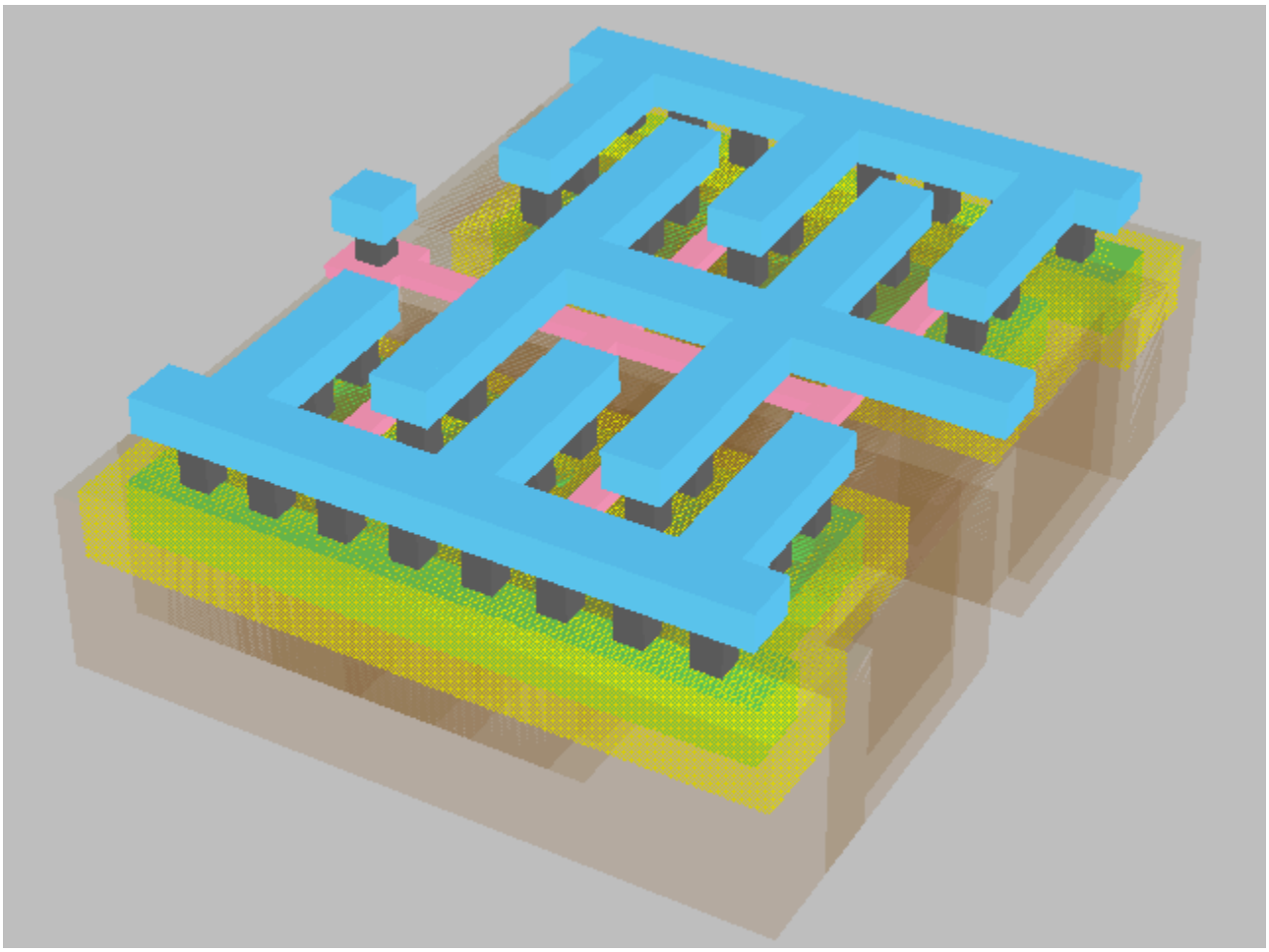

Figure 2.3: 3D View of 4-MOSFET-Cascaded Inverter Layout

We will now connect an input voltage to the inverters and analyze the output voltage of the inverters.

- Below is the schematic of the two inverters that we previously built (refer back to the schematics for which one is inverter 1 and inverter 2).

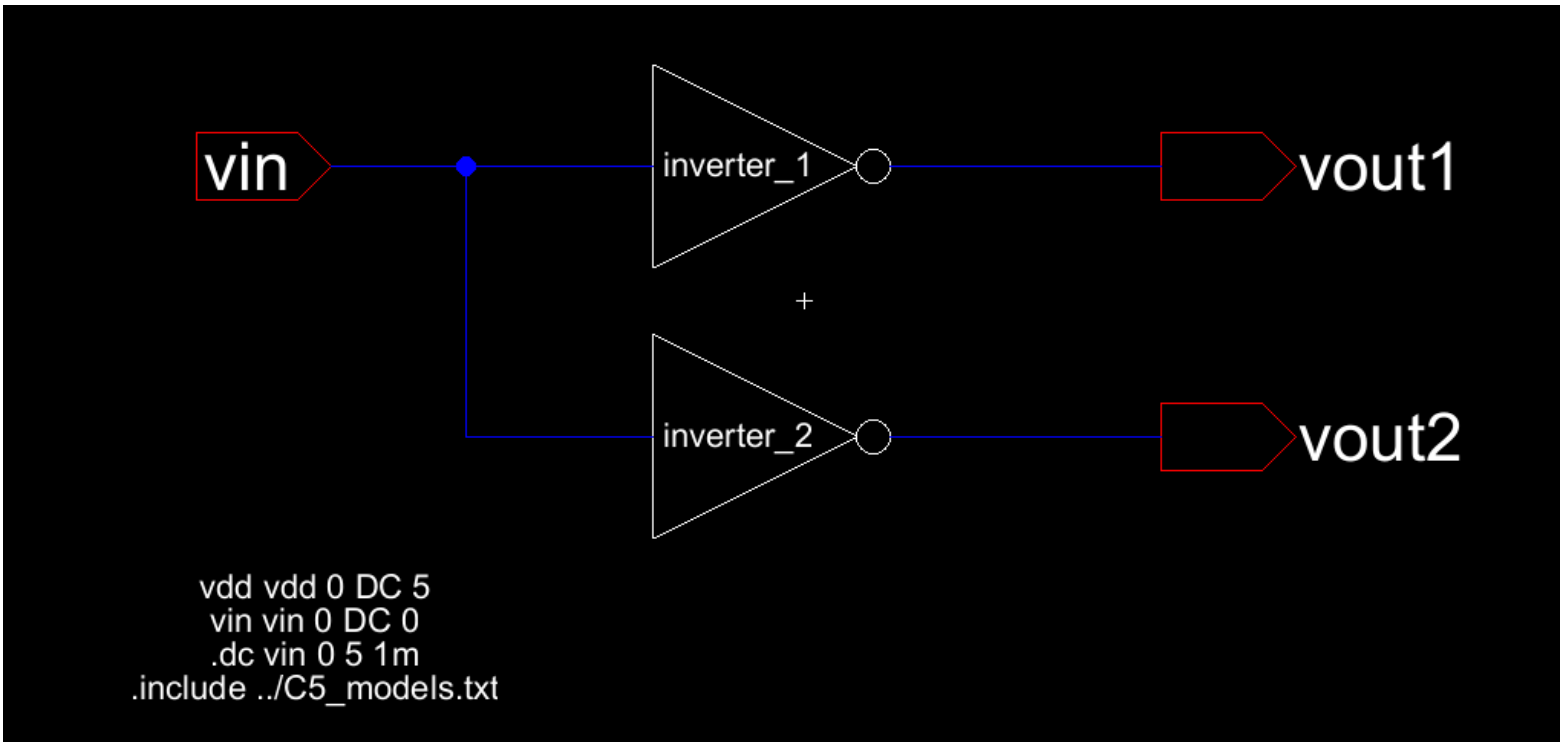

Figure 3.1: Schematic of Inverter 1 and Inverter 2

- Below is the simulation of the two inverters, displaying V_{in}, V_{out1}, and V_{out2}.

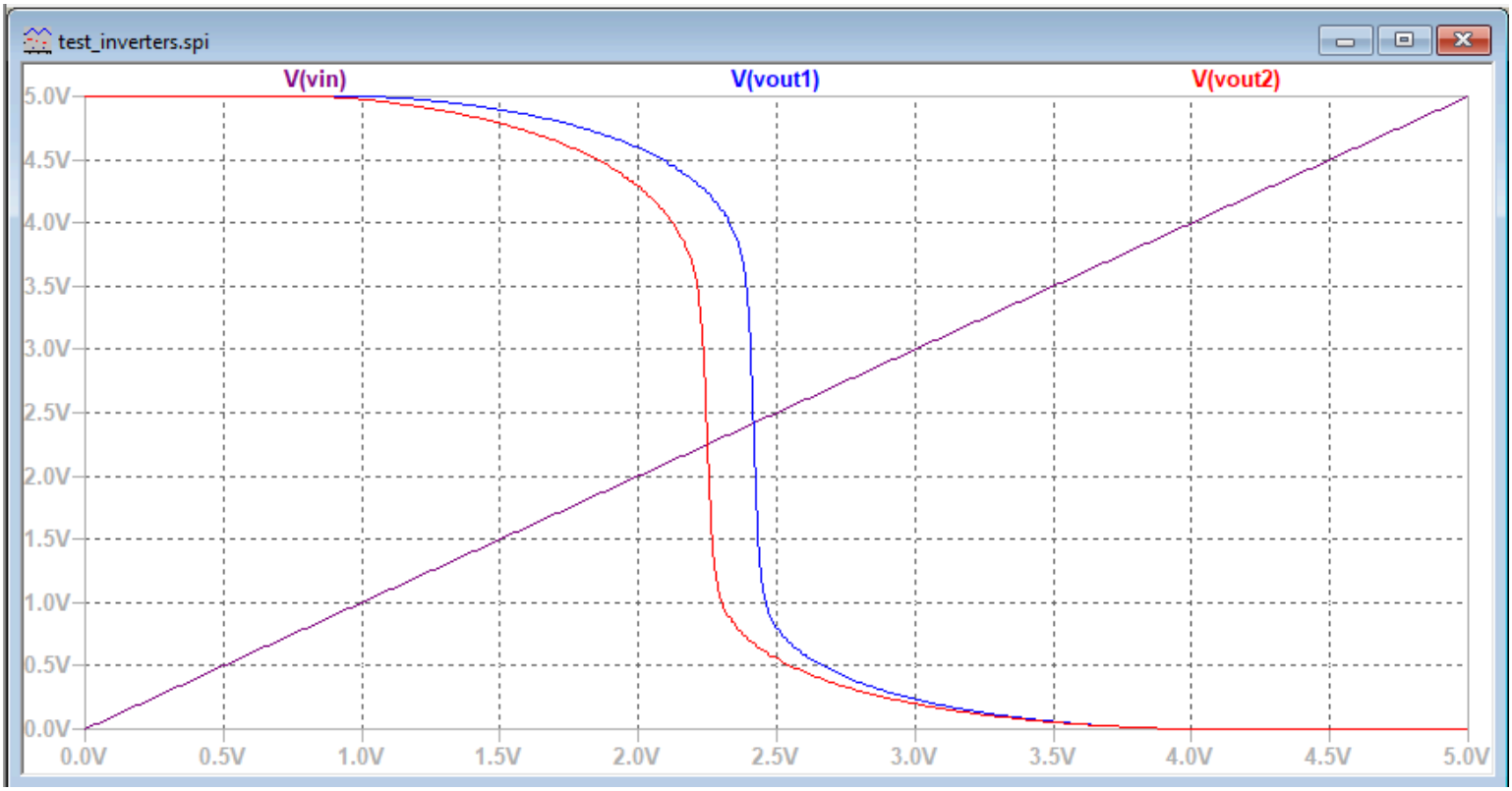

Figure 3.2: Simulation of Inverter 1 and Inverter 2

Let’s add capacitive loads and analyze the inverter’s behavior over various step responses.

- Below is a schematic of the Inverter 1 and Inverter 2 with capacitive loads over a step response of 100 fF, 1 pF, 10 pF, and 100 pF.
    - The following figures are the simulations of V_{in} vs. V_{out} for inverter 1 and inverter 2.

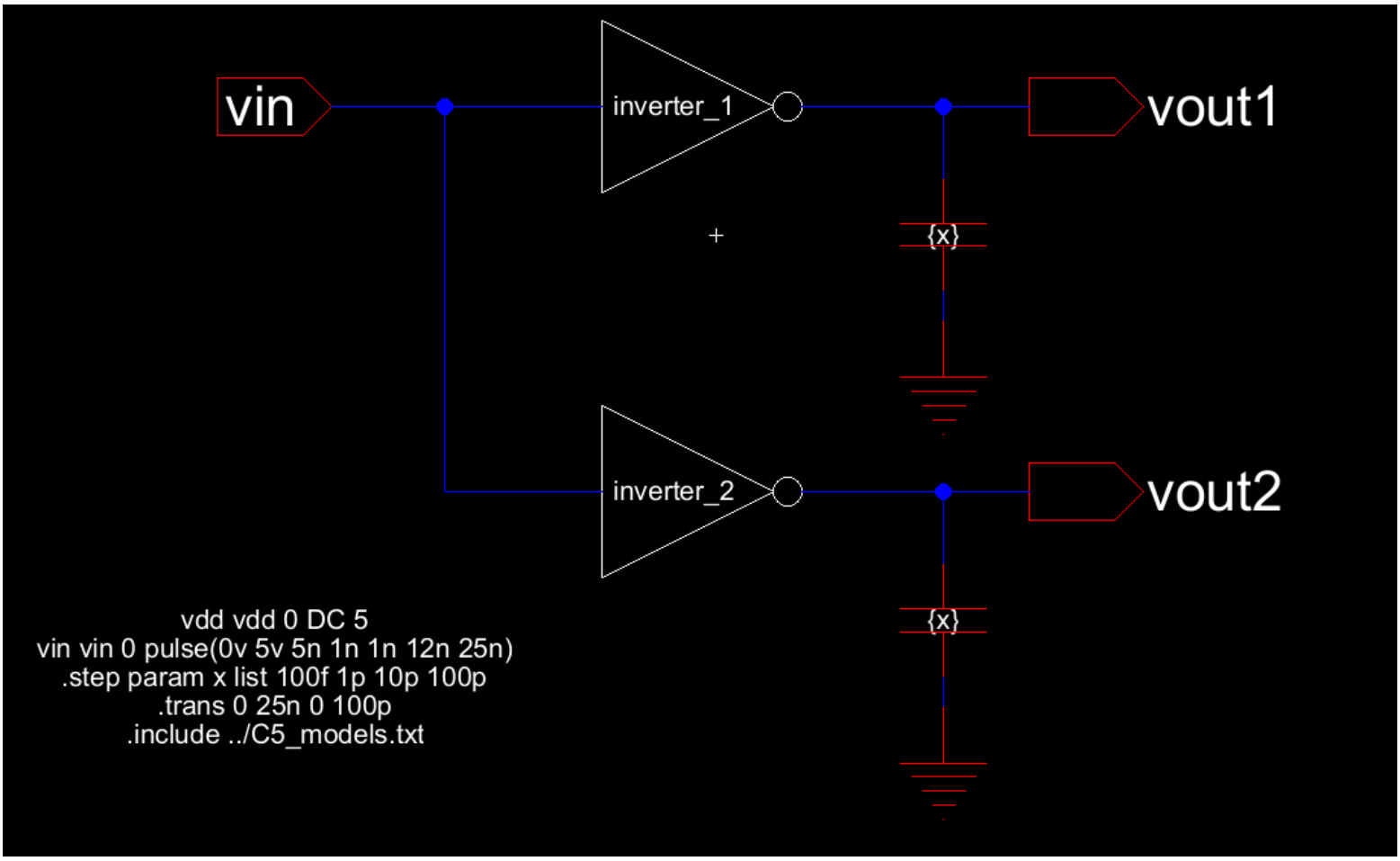

Figure 4.1: Schematic of Inverter 1 and 2 with Capacitive Load Step Response 1

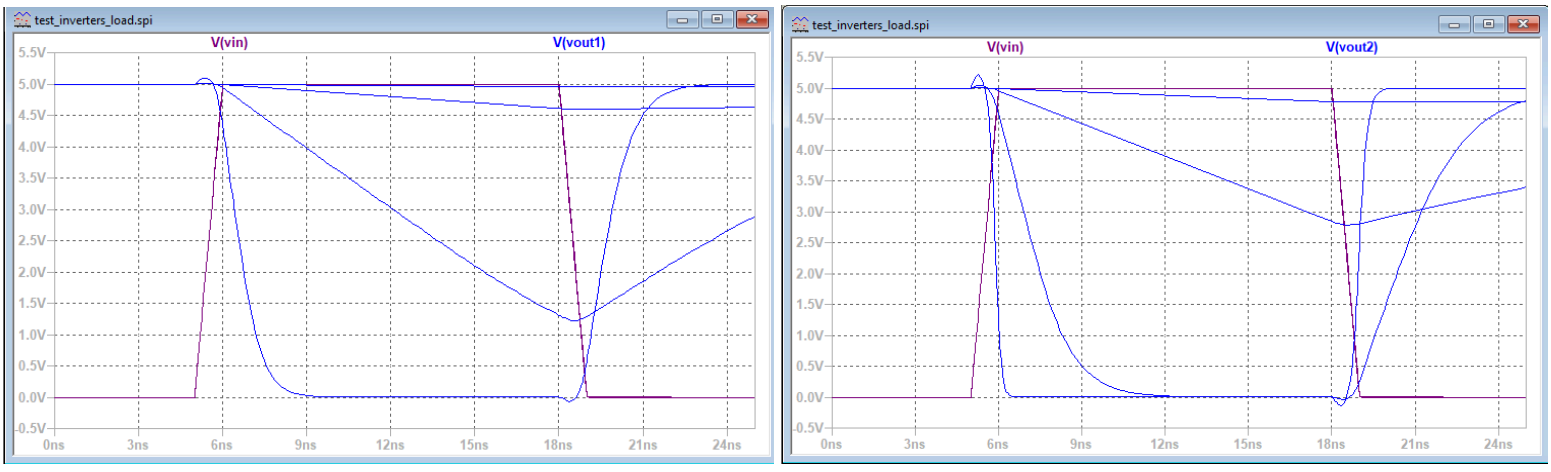

Figure 4.2: Simulation of Inverter 1 and 2 with Step Response 1

- Below is a schematic of the Inverter 1 and Inverter 2 with capacitive loads over a step response of 1 fF, 10 fF, 100 fF.
    - The following figures are the simulations of V_{in} vs. V_{out} for inverter 1 and inverter 2.

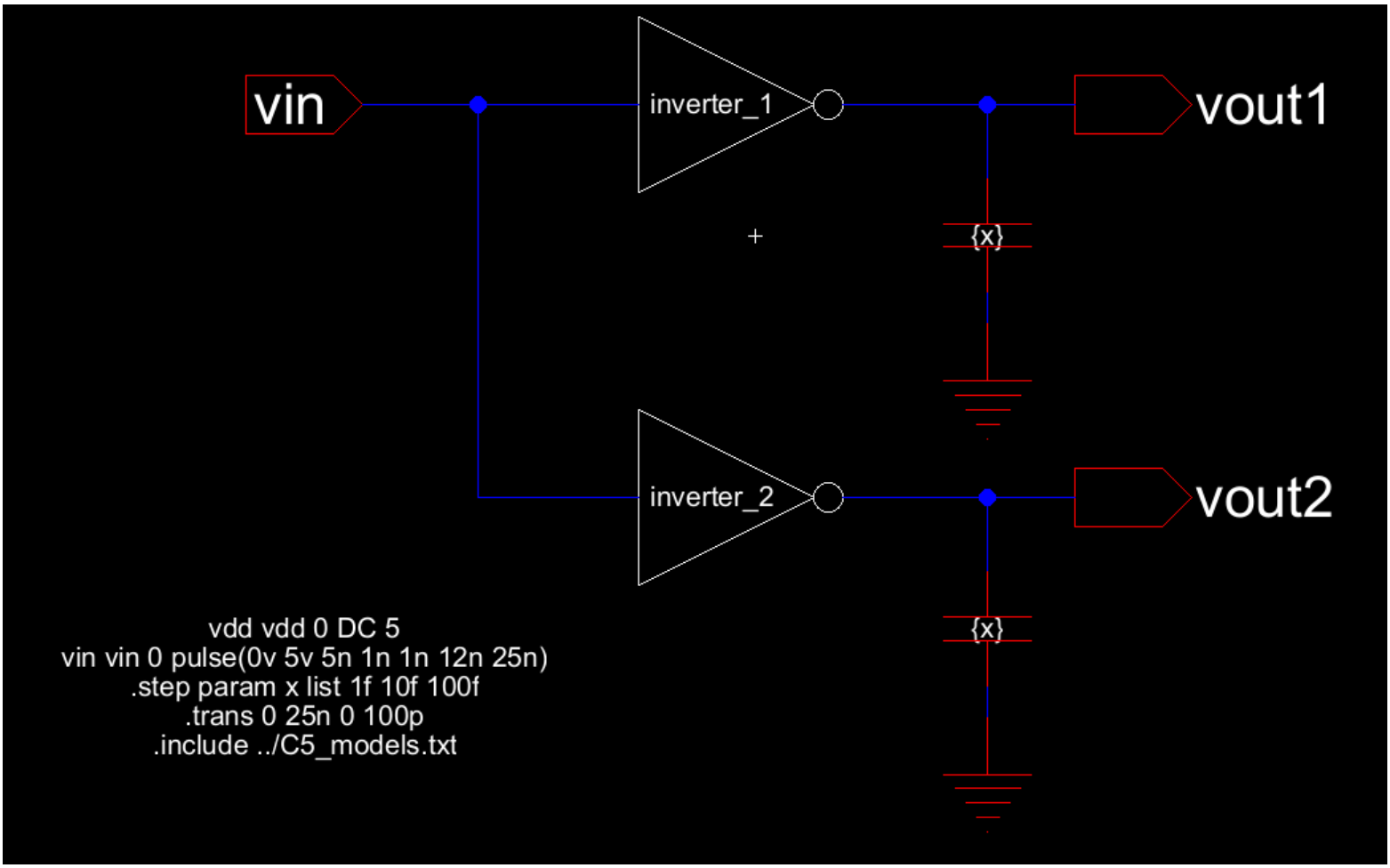

Figure 5.1: Schematic of Inverter 1 and 2 with Capacitive Load Step Response 2

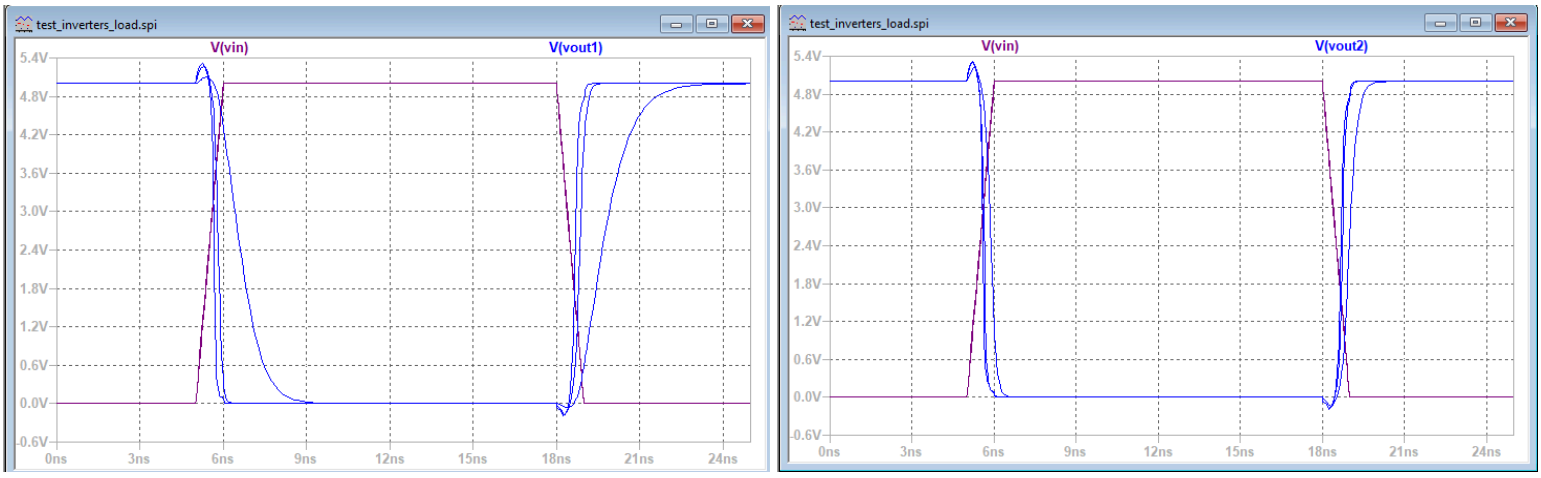

Figure 5.2: Simulation of Inverter 1 and 2 with Step Response 2

DRC and LVS Check

```
Checking schematic cell 'inverter_1{sch}'
   No errors found
Checking schematic cell 'inverter_2{sch}'
   No errors found
Checking schematic cell 'test_inverters{sch}'
   No errors found
Checking icon cell 'inverter_1{ic}'
   No errors found
Checking icon cell 'inverter_2{ic}'
   No errors found
0 errors and 0 warnings found (took 0.014 secs)
```

Figure 6.1: Error Check on Test-Inverters Schematic

```
Checking schematic cell 'inverter_1{sch}'
   No errors found
Checking schematic cell 'inverter_2{sch}'
   No errors found
Checking schematic cell 'test_inverters_load{sch}'
   No errors found
Checking icon cell 'inverter_1{ic}'
   No errors found
Checking icon cell 'inverter_2{ic}'
   No errors found
0 errors and 0 warnings found (took 0.005 secs)
```

Figure 6.2: Error Check on Test-Inverters with Load Schematic

```
Hierarchical NCC every cell in the design: cell 'inverter_1{sch}'  cell 'inverter_1{lay}'
Comparing: lab_4_inverters:inverter_1{sch} with: lab_4_inverters:inverter_1{lay}
  exports match, topologies match, sizes not checked in 0.097 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.13 seconds.
================================237================================
Hierarchical NCC every cell in the design: cell 'inverter_2{sch}'  cell 'inverter_2{lay}'
Comparing: lab_4_inverters:inverter_2{sch} with: lab_4_inverters:inverter_2{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.005 seconds.
```

Figure 6.3: NCC Check on Inverter 1 and Inverter 2 Layout