Lab 3 Report
NMOS with ESD Protection

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Goal

Laying a 4-pin NMOS onto a padframe with ESD protection.

Procedure

These are cells that we will be baselining the NMOS IC with ESD protection.

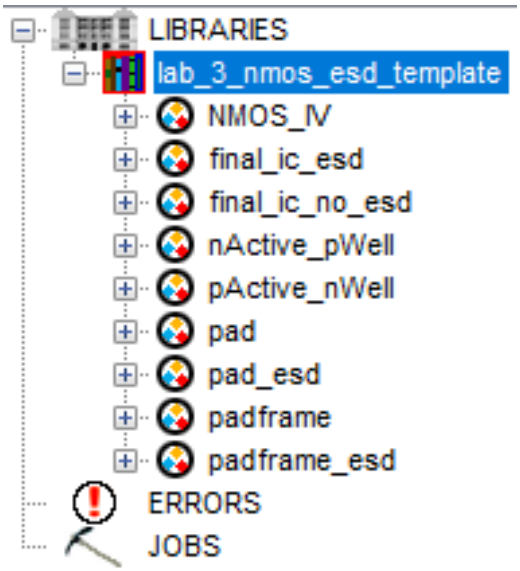

Figure 1.1: NMOS IC w/ ESD Protection Library Baseline

- Below are the schematic icon, and layout views of an NMOS with drain, gate, source, and bulk.

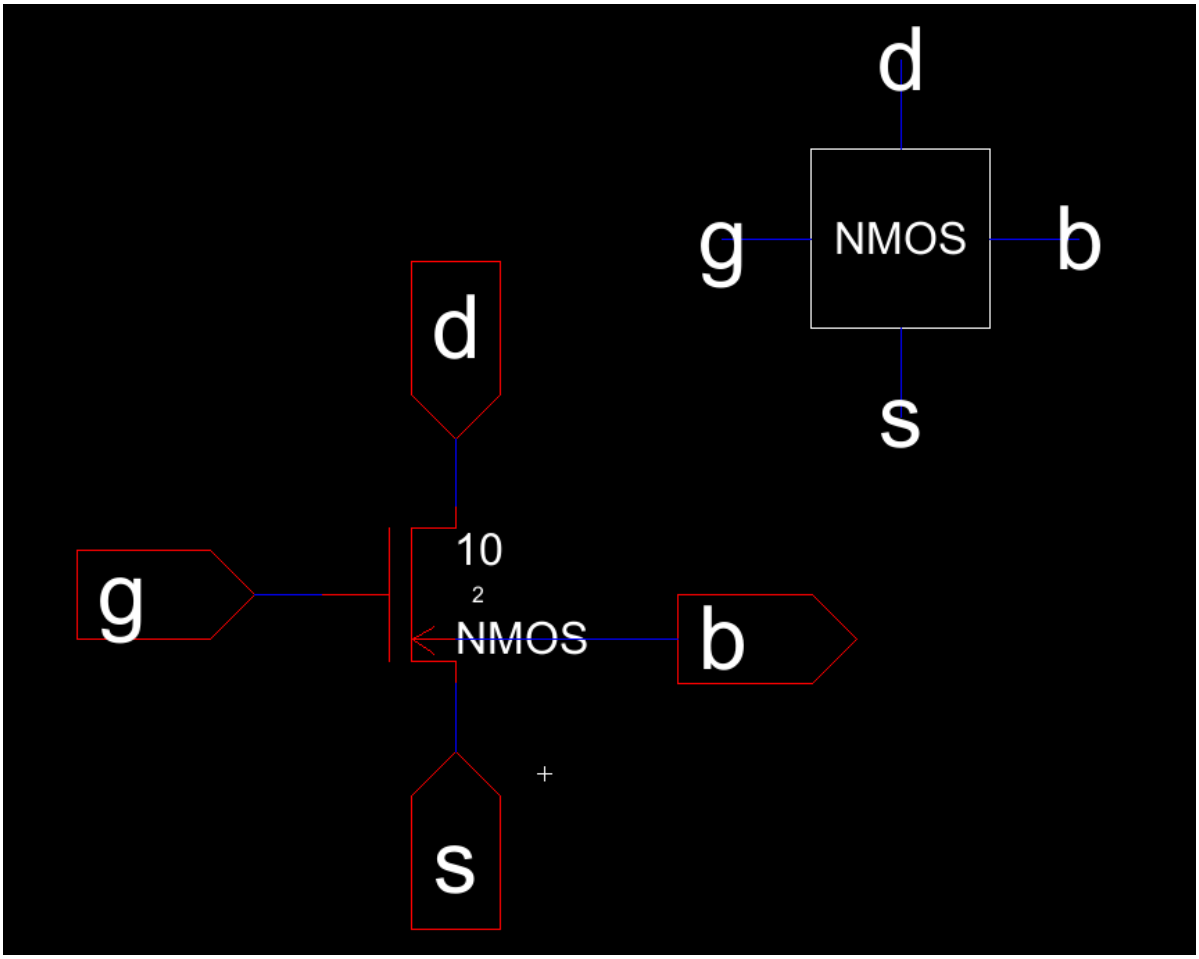

Figure 2.1: 4-pin NMOS Schematic and Icon

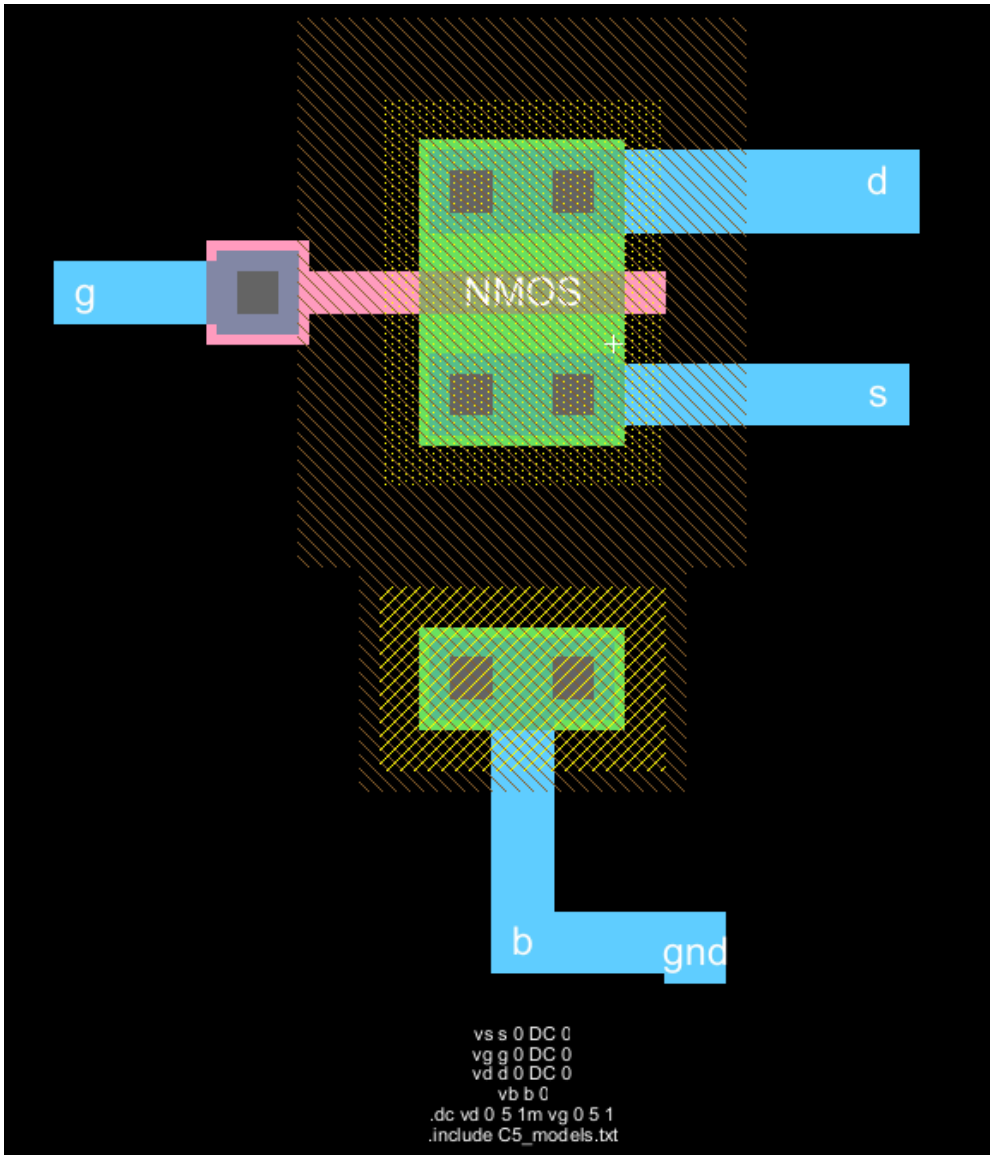

Figure 2.2: 4-pin NMOS Layout

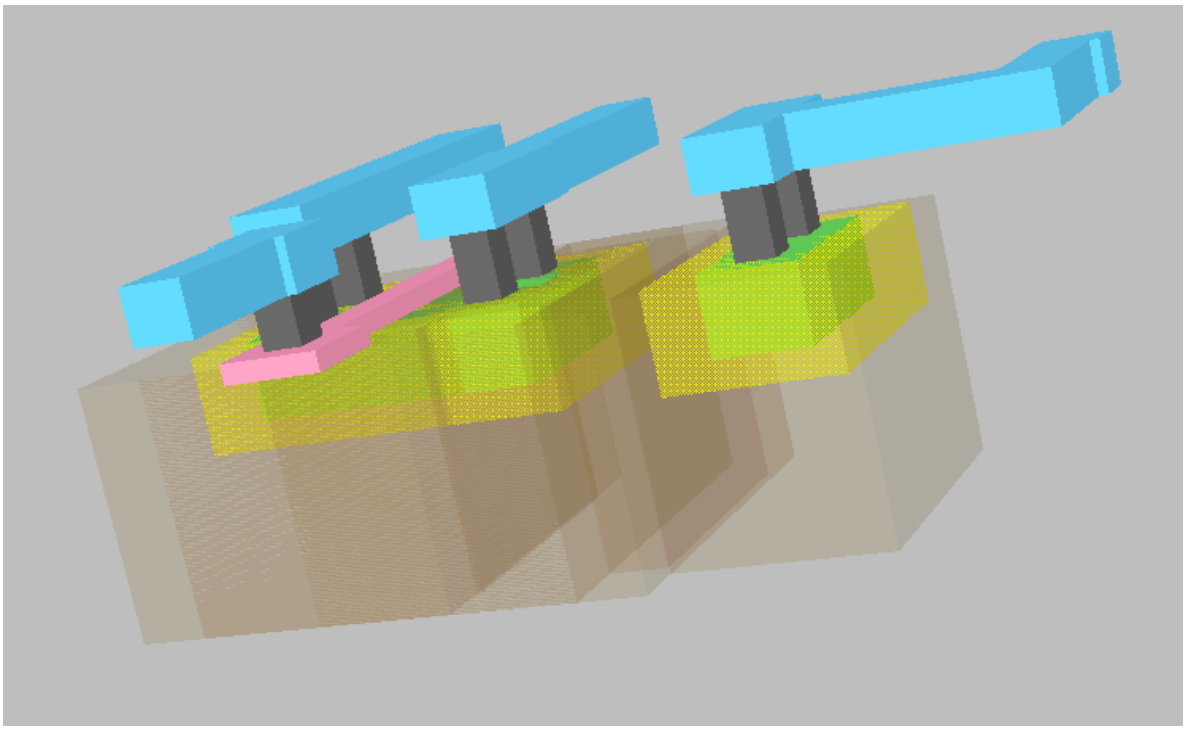

Figure 2.3: 3D View of 4-pin NMOS Layout

- Below are the schematic icon, and layout views of a pad cell.

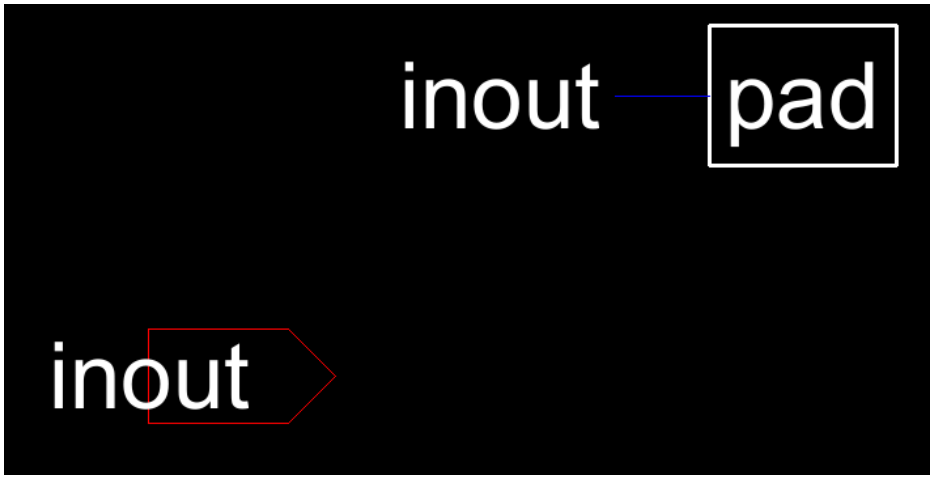

Figure 3.1: Pad Cell Schematic and Icon

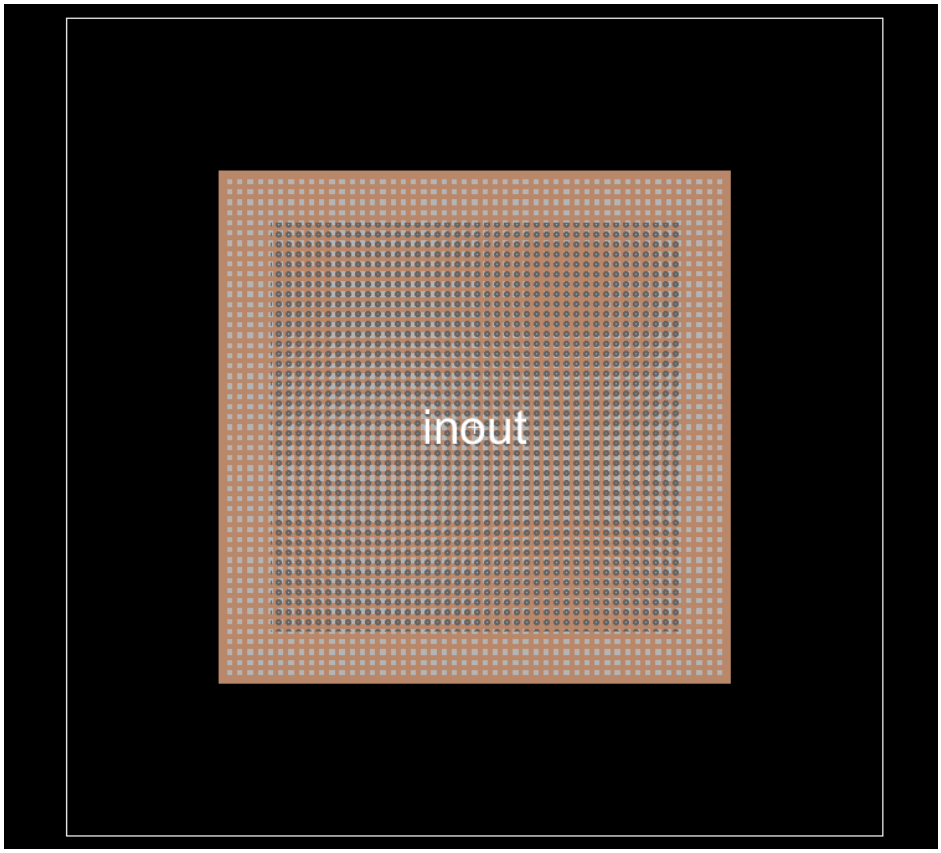

Figure 3.2: Pad Cell Layout

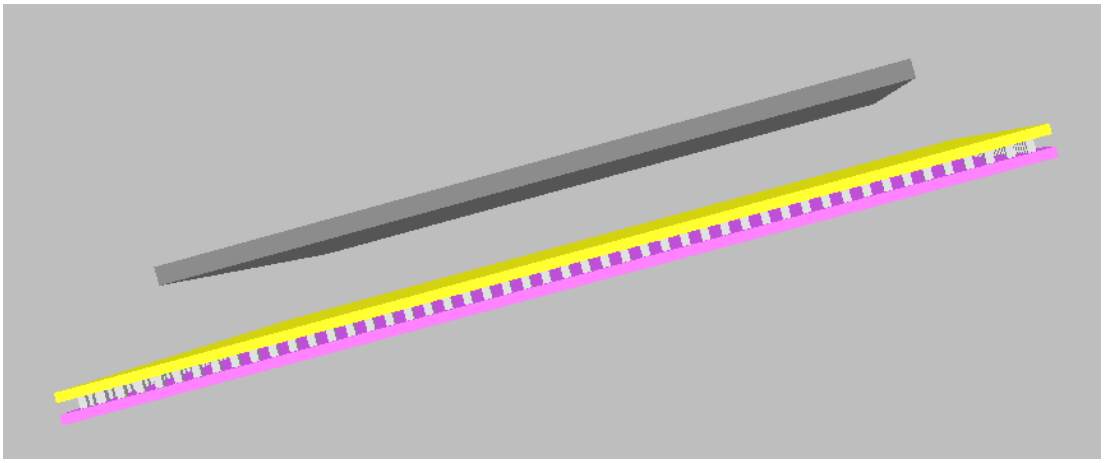

Figure 3.3: 3D View of a Pad Cell Layout

- Below are the schematic icon, and layout views of a padframe.

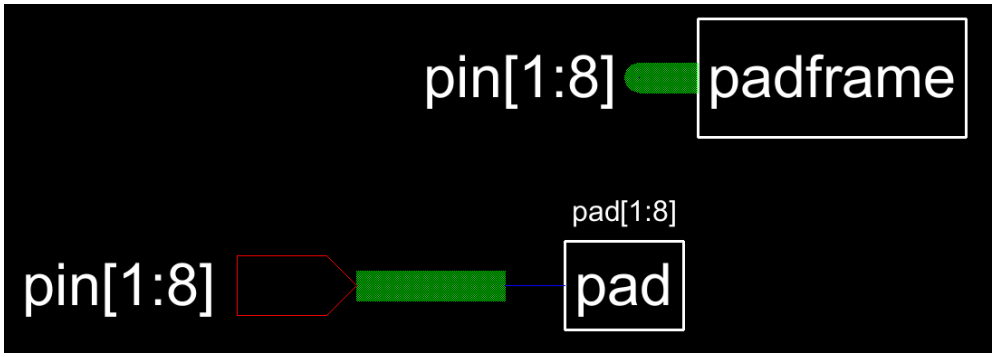

Figure 4.1: Padframe Schematic and Icon

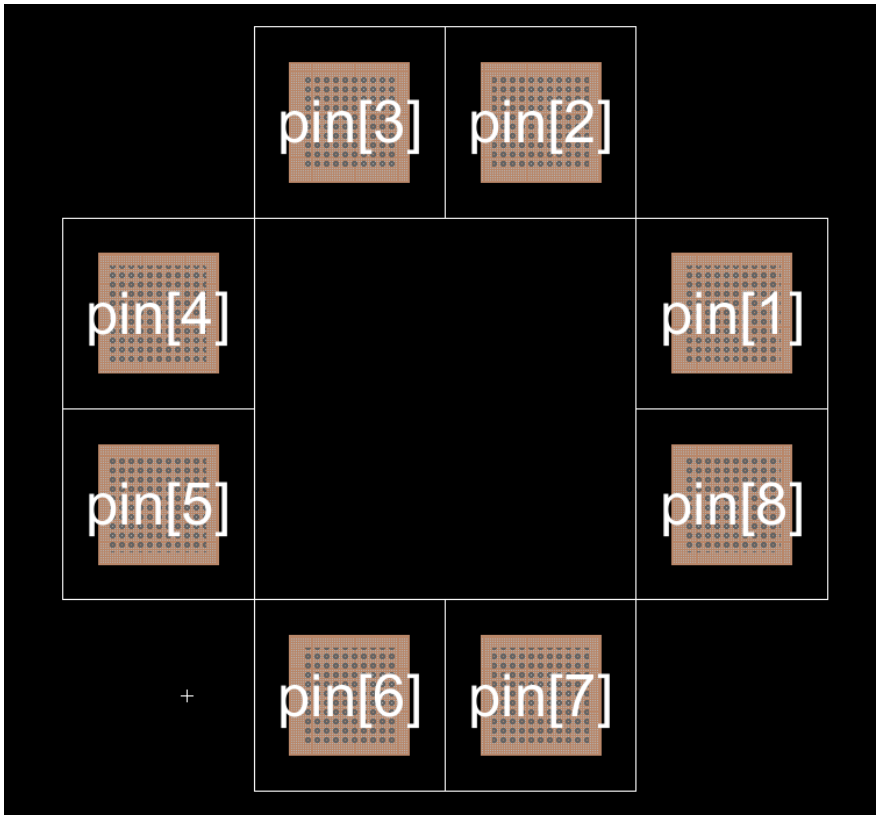

Figure 4.2: Padframe Layout

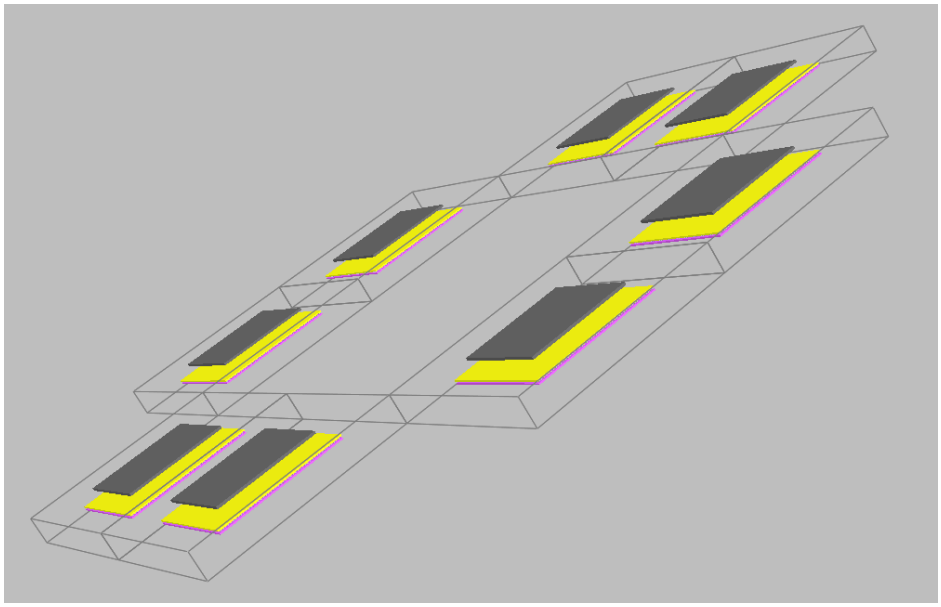

Figure 4.3: 3D View of Padframe Layout

- Below are the schematic icon, and layout views of a padframe.

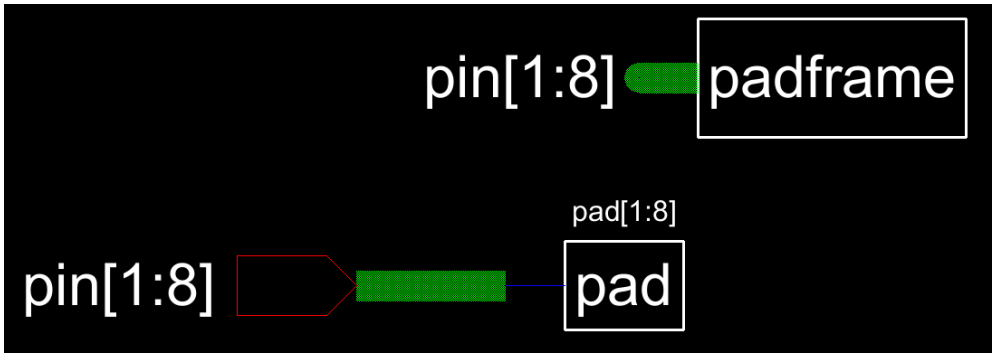

Figure 4.1: Padframe Schematic and Icon

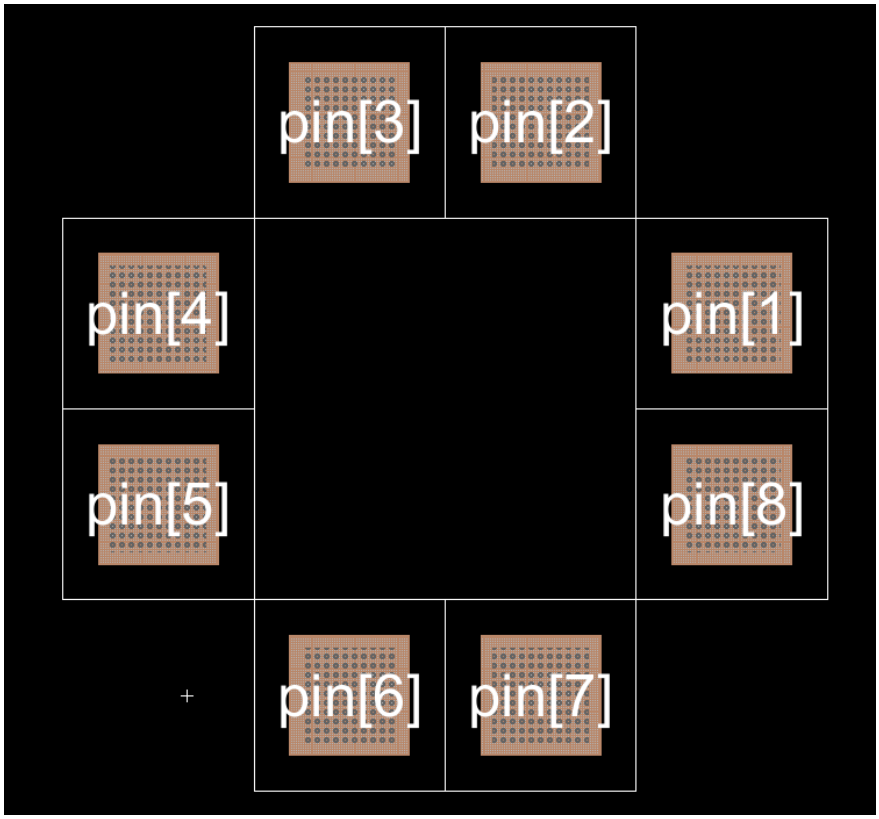

Figure 4.2: Padframe Layout

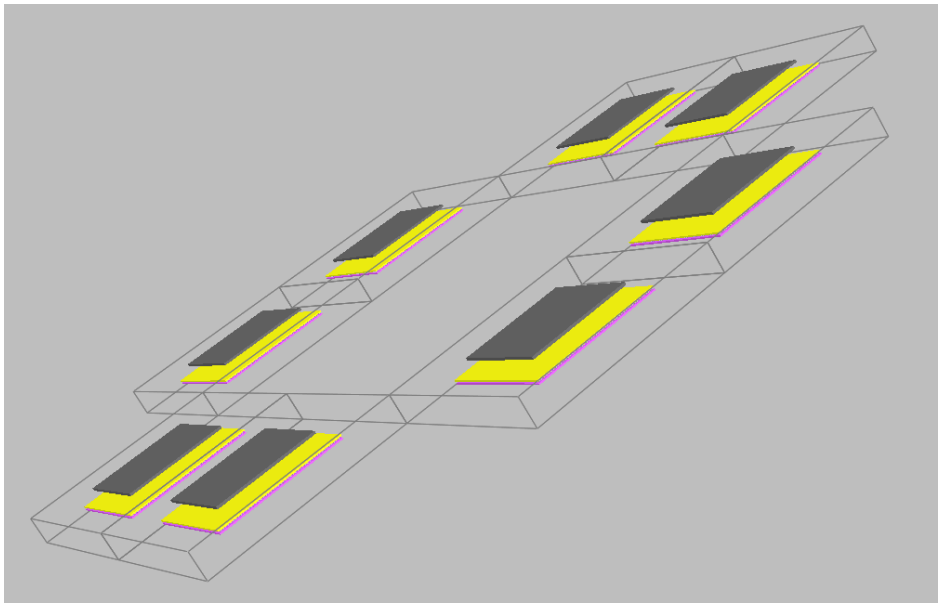

Figure 4.3: 3D View of Padframe Layout

Using these previous library cells, we can create a 4 pin NMOS IC, where we layout the NMOS on the padframe.

- Below are the schematic icon, and layout views of an NMOS IC.

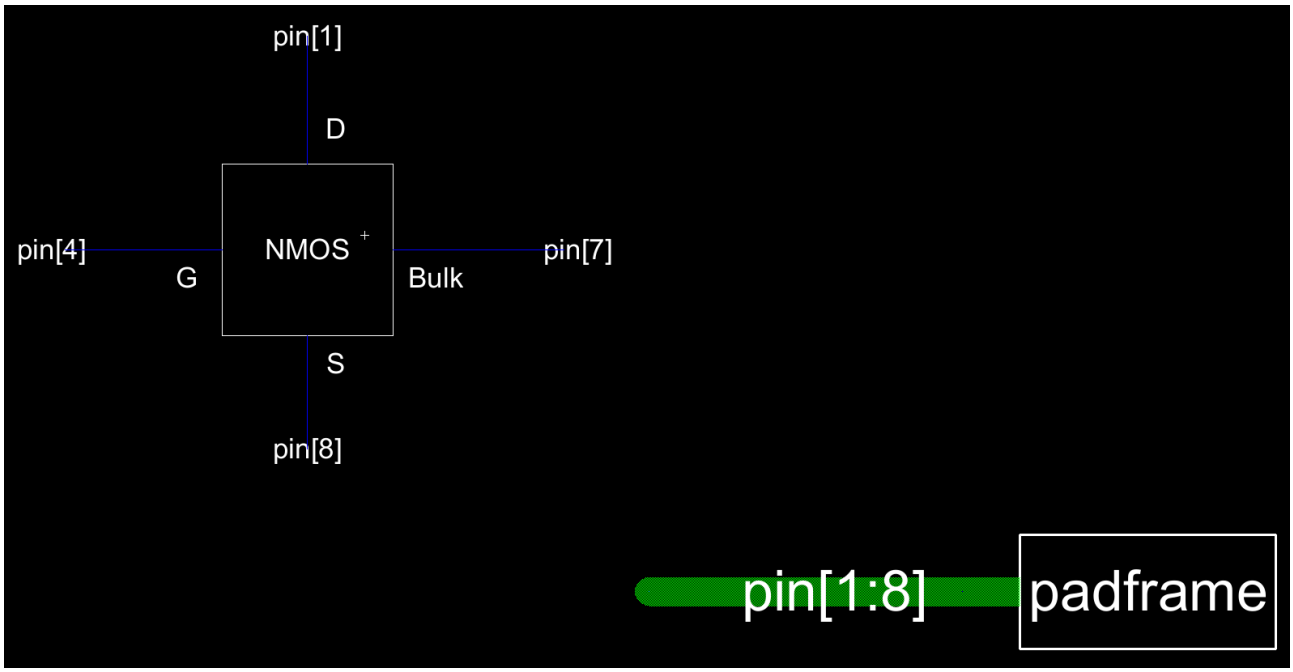

Figure 5.1: 4-pin NMOS IC Schematic and Icon

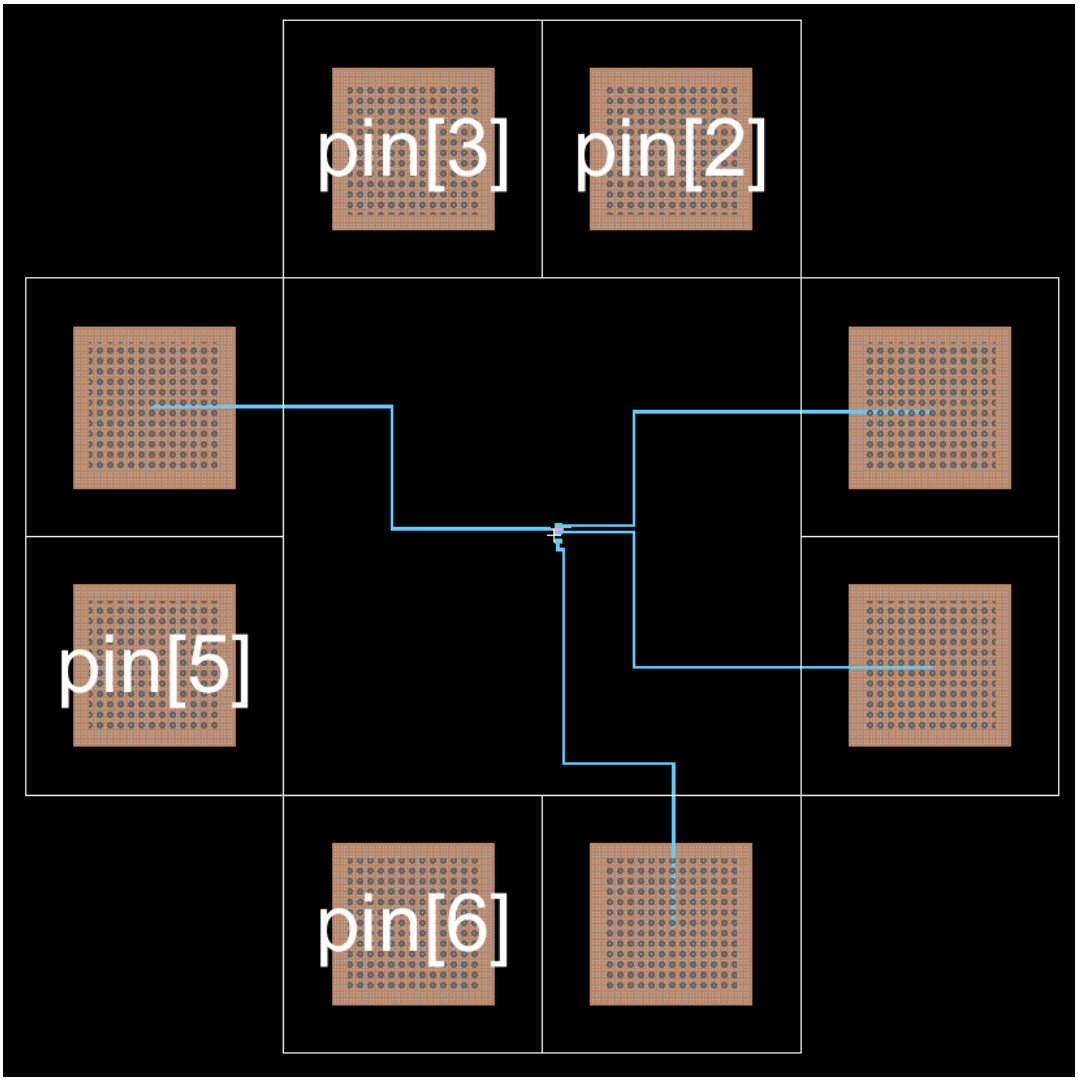

Figure 5.2: 4-pin NMOS IC Layout

- Below is the table of the connections of the 4-pin NMOS relative to the padframe

4-pin NMOS I/O	**Padframe Pins**
gate	pin[4]
bulk	pin[7]
source	pin[8]
drain	pin[1]

Note: pin[2], pin[3], pin[5], and pin[6] in the padframe is unused

Table 5.1: 4-pin NMOS IC Pin Connections

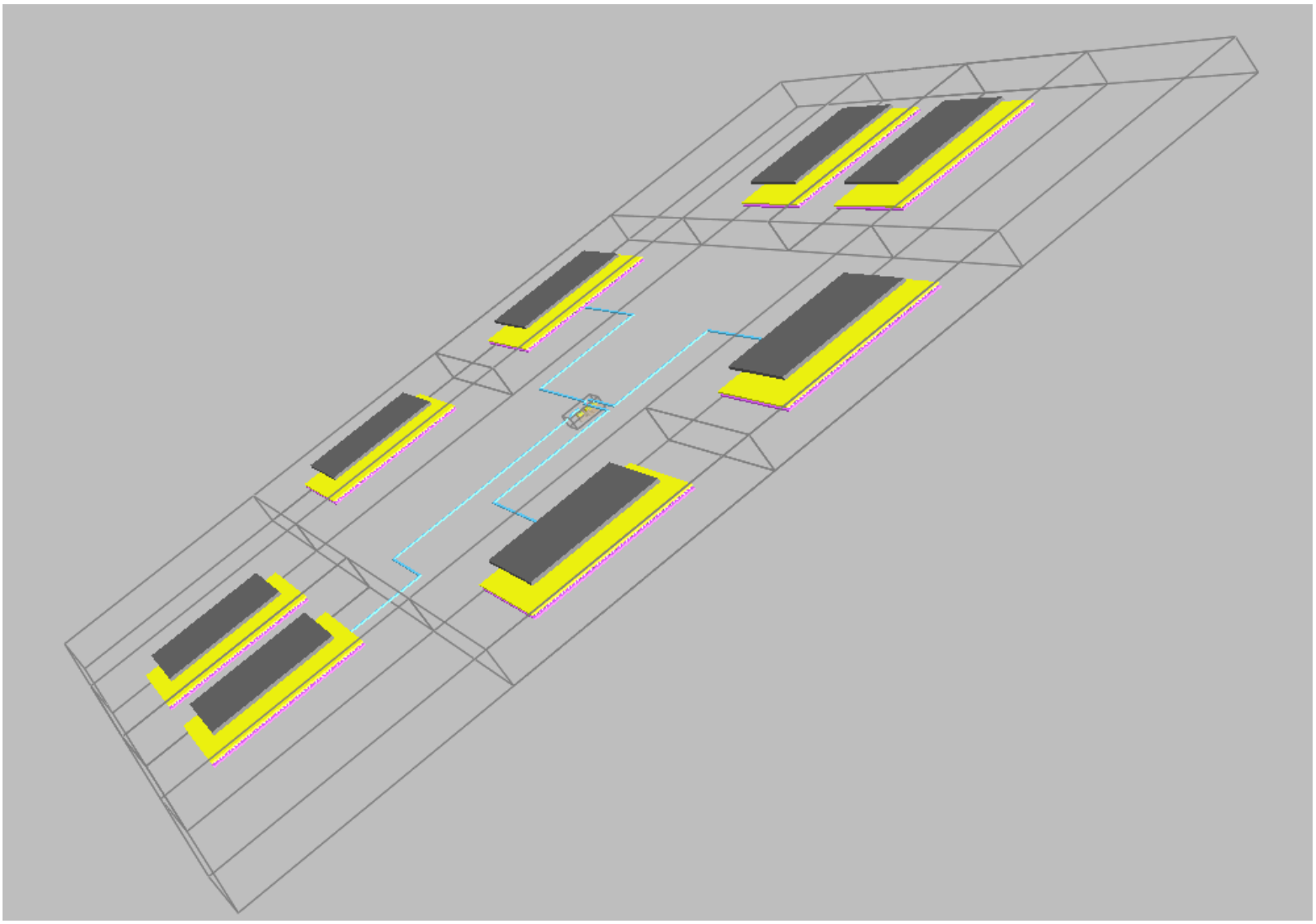

Figure 5.3: 3D View of 4-pin NMOS Layout

The next procedure is to design an NMOS IC with ESD protection. Let's start off with designing the ESD protection part for the padframe.

- Below are the schematic icon, and layout views of an n-active p-well.

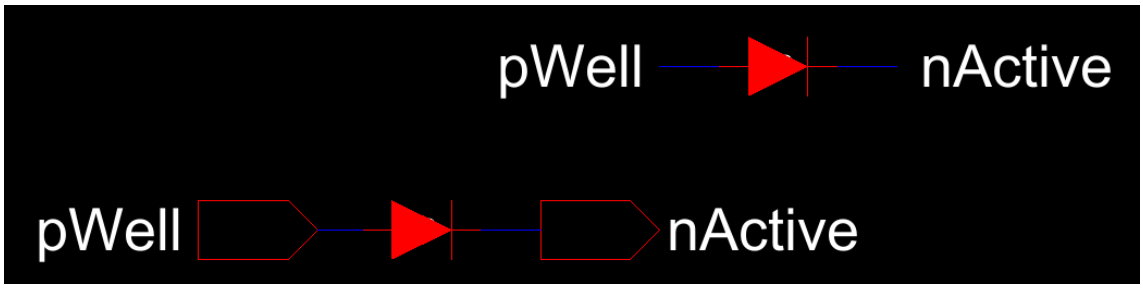

Figure 6.1: N-active P-Well Schematic and Icon

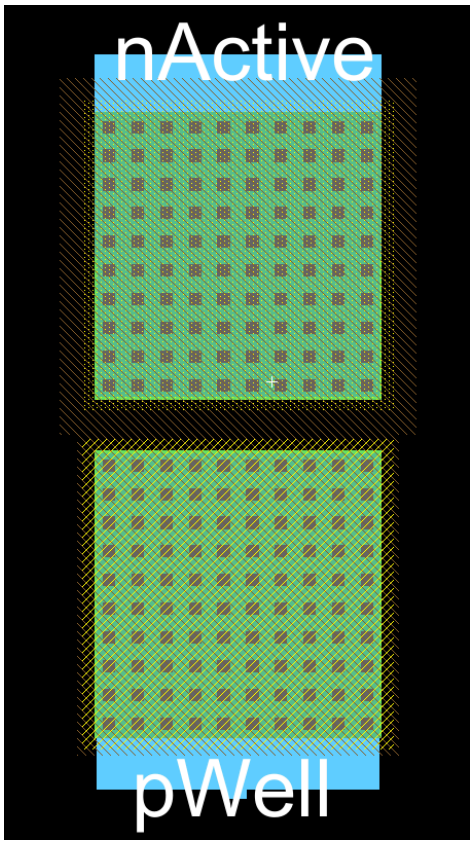

Figure 6.2: N-active P-Well Layout

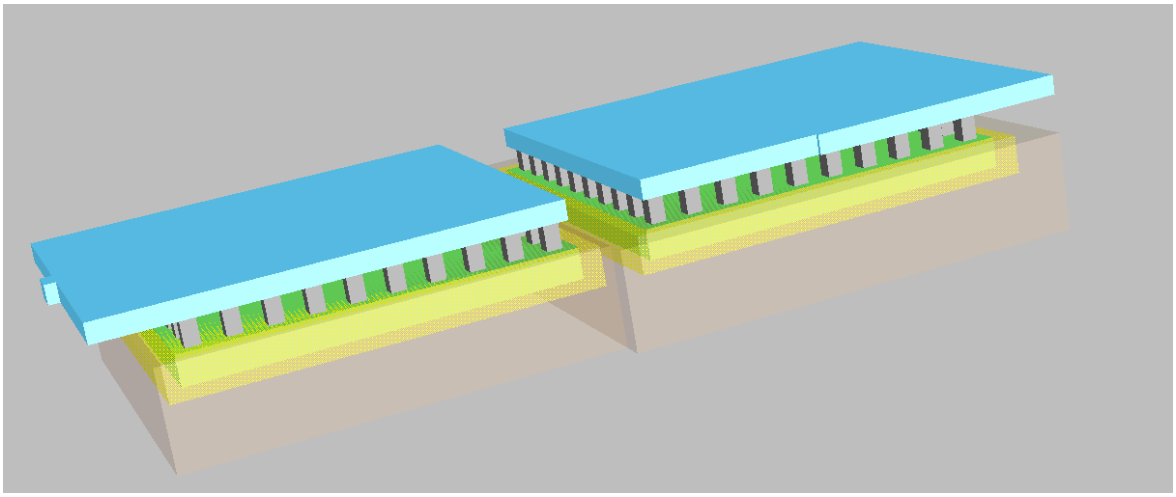

Figure 6.3: 3D View of N-active P-Well Layout

- Below are the schematic icon, and layout views of an p-active n-well.

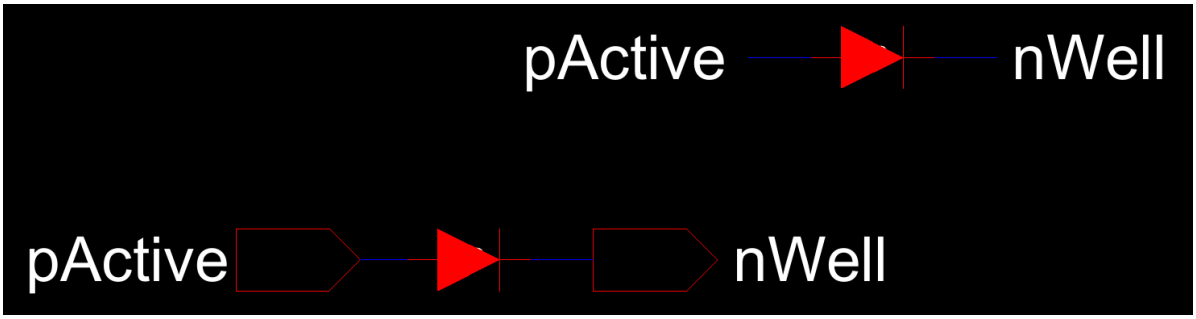

Figure 7.1: P-active N-Well Schematic and Icon

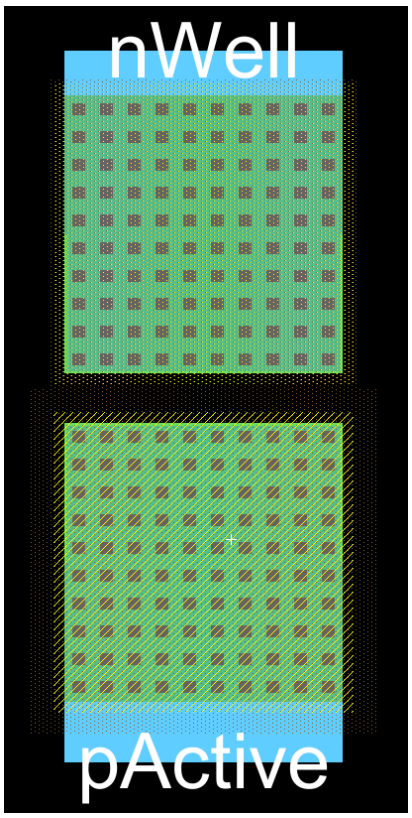

Figure 7.2: P-active N-Well Layout

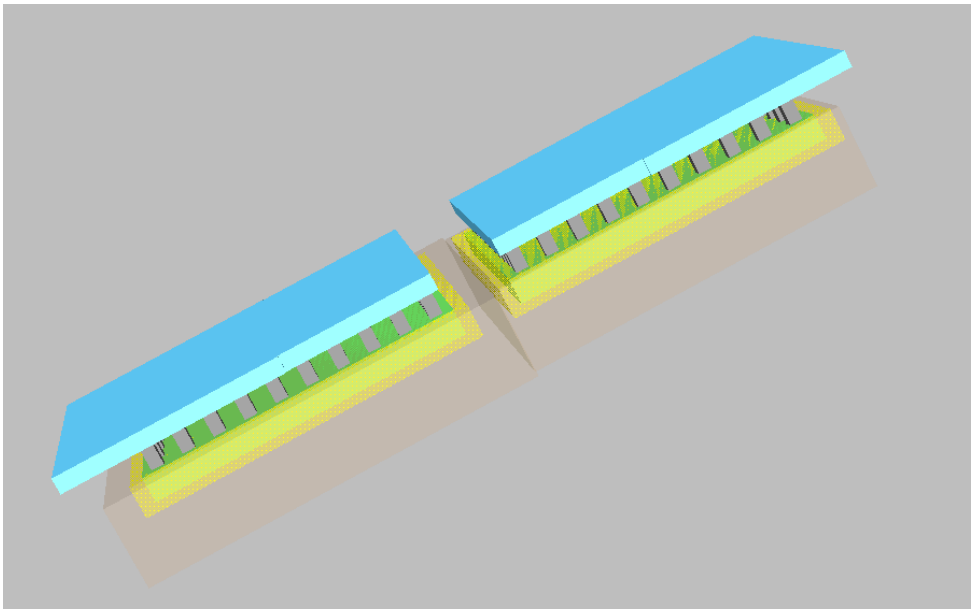

Figure 7.3: 3D View of P-active N-Well Layout

Now that we have an n-active p-well and p-active n-well, we can arrange a connection to the pad that will make it ESD protected.

- Below are the schematic icon, and layout views of an ESD protected pad cell.

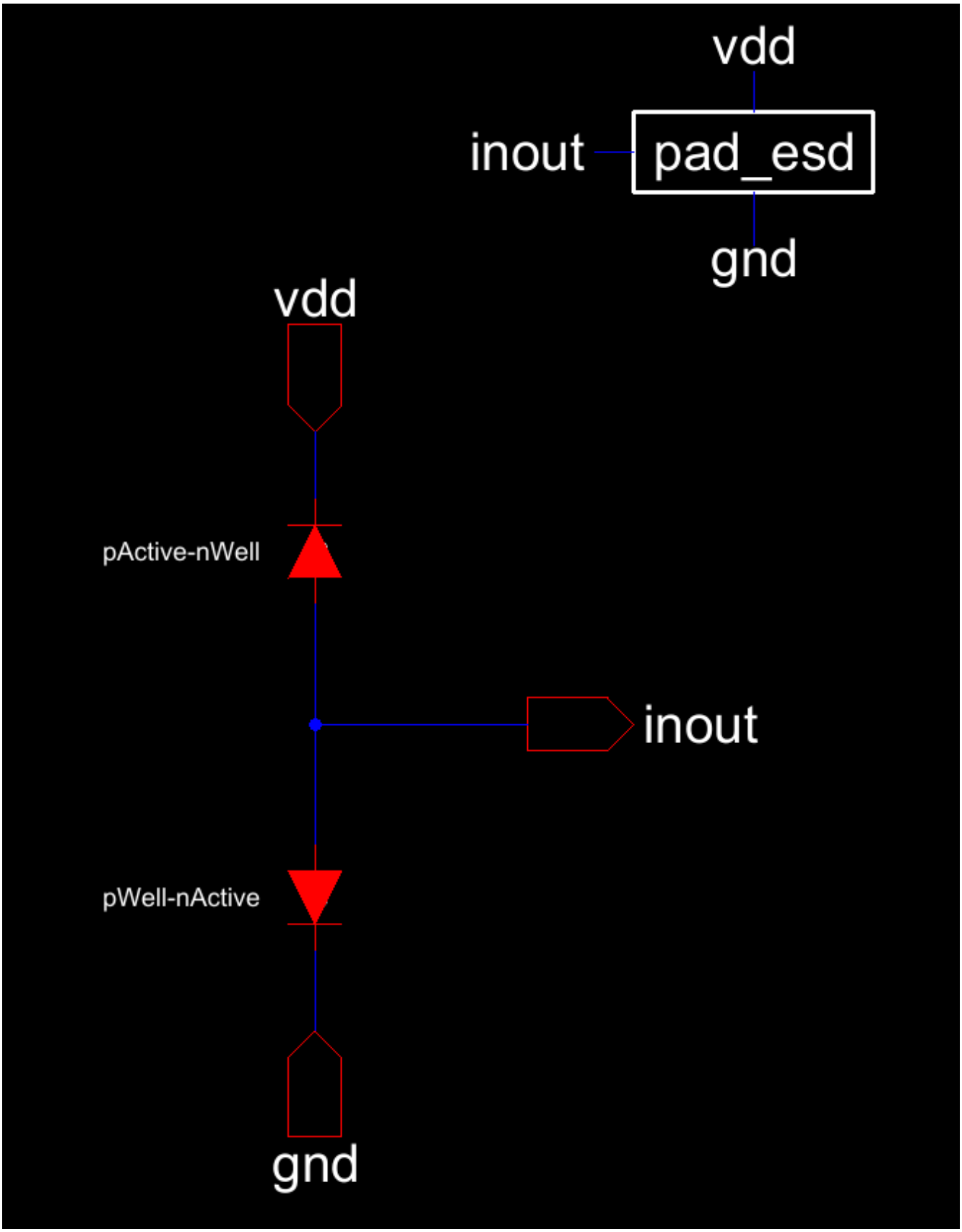

Figure 8.1: ESD Pad Schematic and Icon

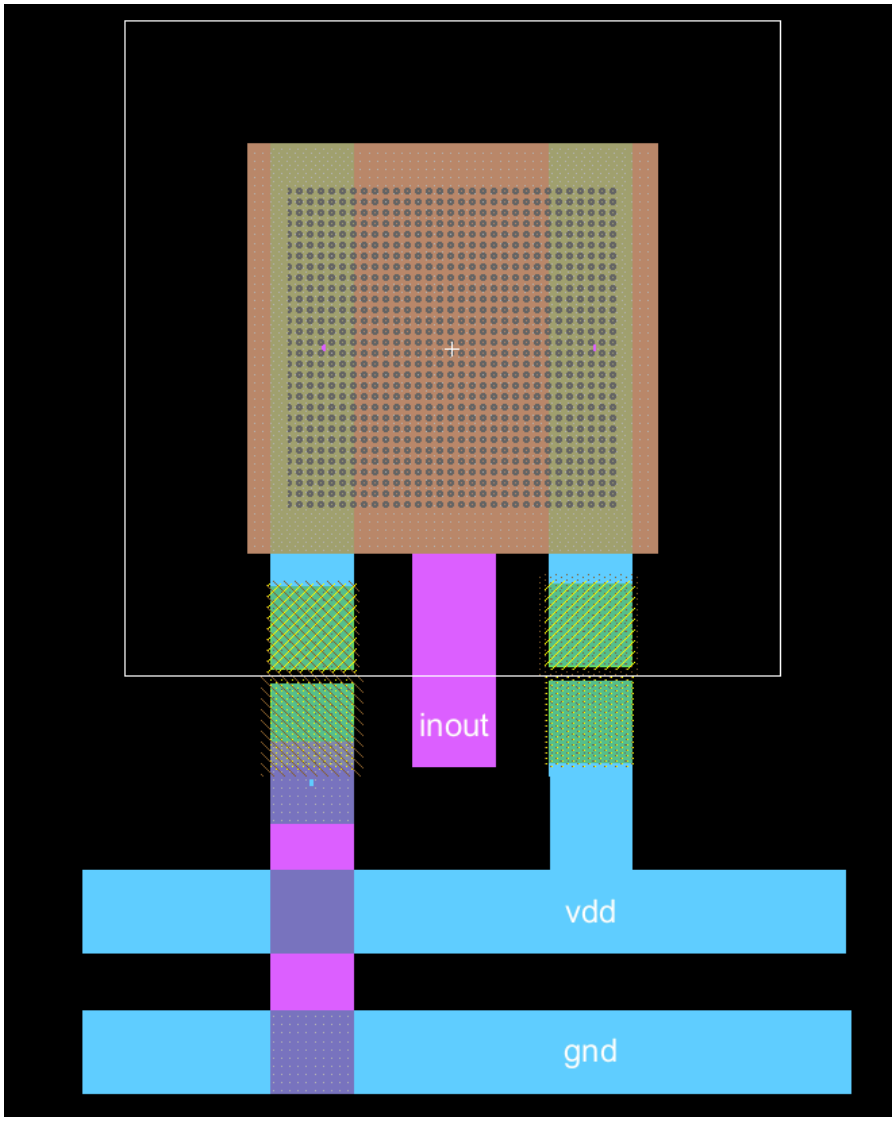

Figure 8.2: ESD Pad Layout

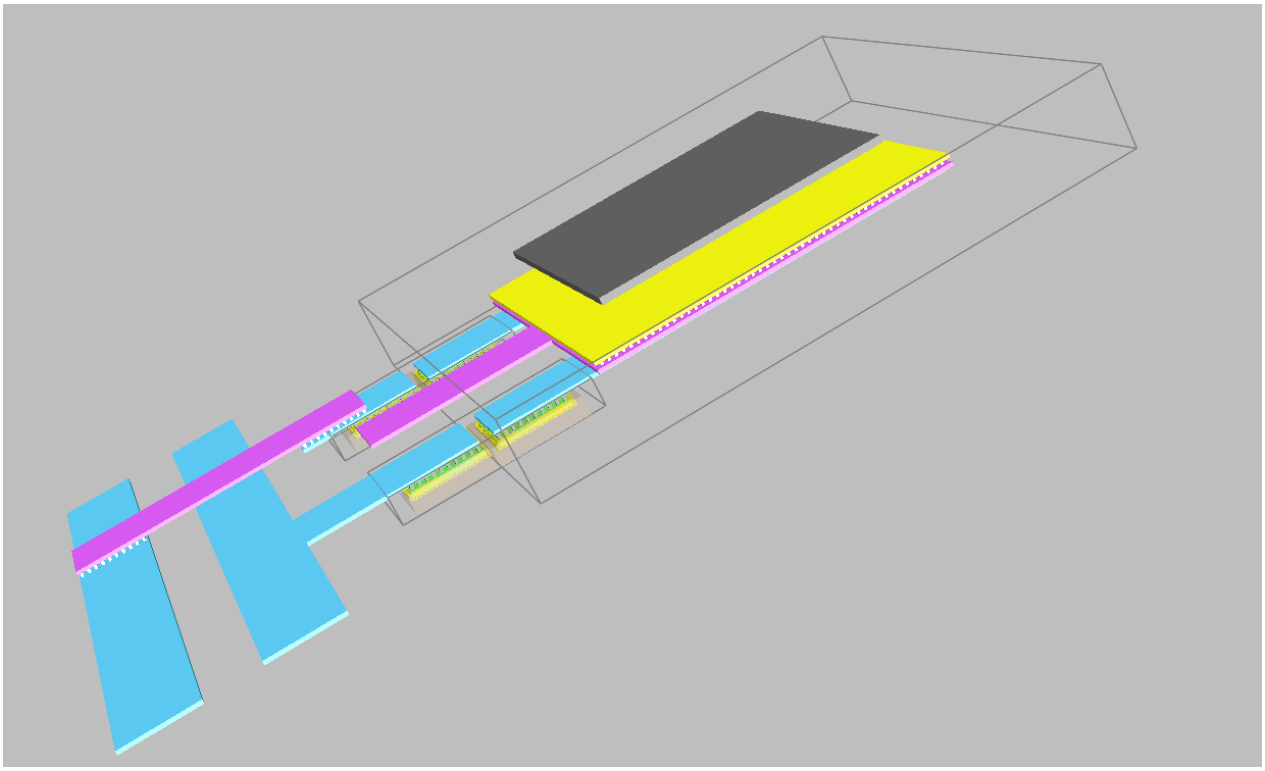

Figure 8.3: 3D View of ESD Pad Layout

- Below are the schematic icon, and layout views of an ESD-protected padframe.

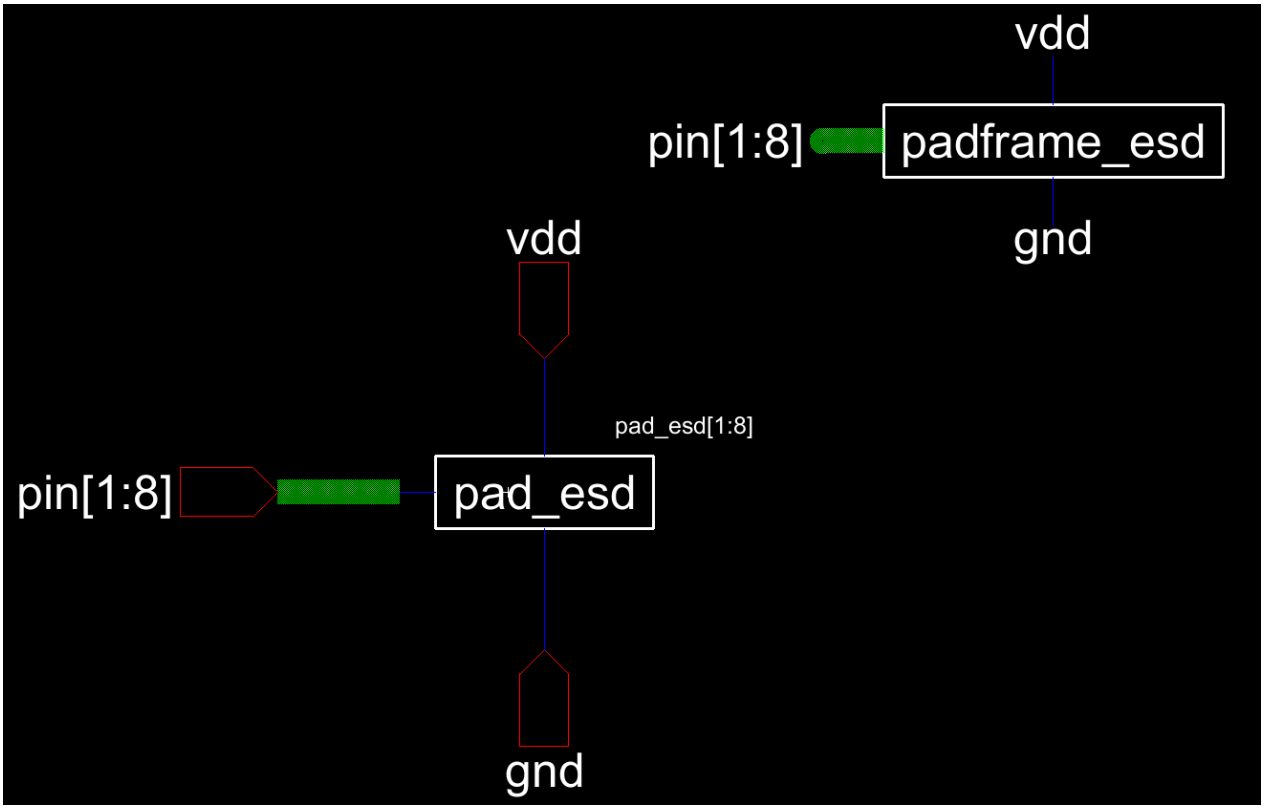

Figure 9.1: ESD Padframe Schematic and Icon

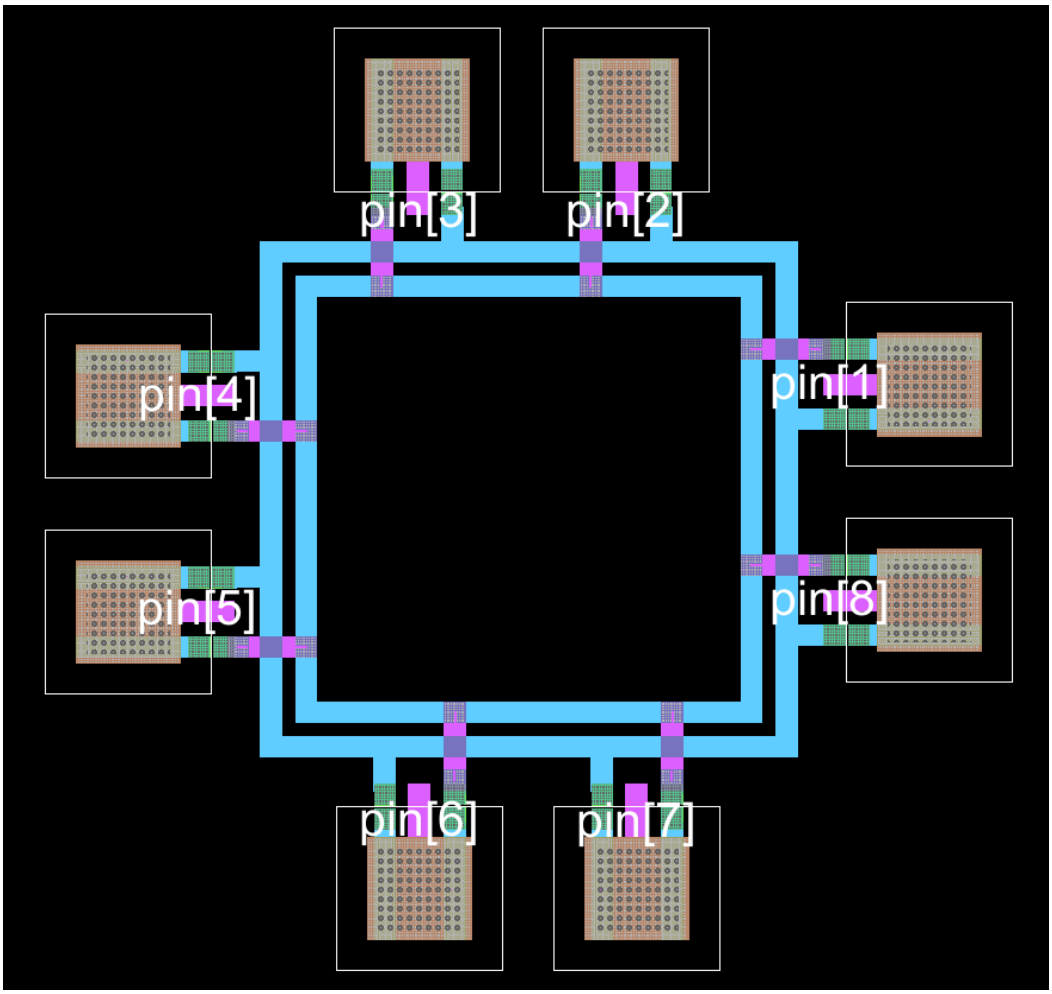

Figure 9.2: ESD Padframe Layout

Now that we have an ESD protected padframe we can connect our NMOS to the padframe, and then we will have an NMOS IC that is ESD protected.

- Below are the schematic icon, and layout views of an ESD-protected NMOS IC

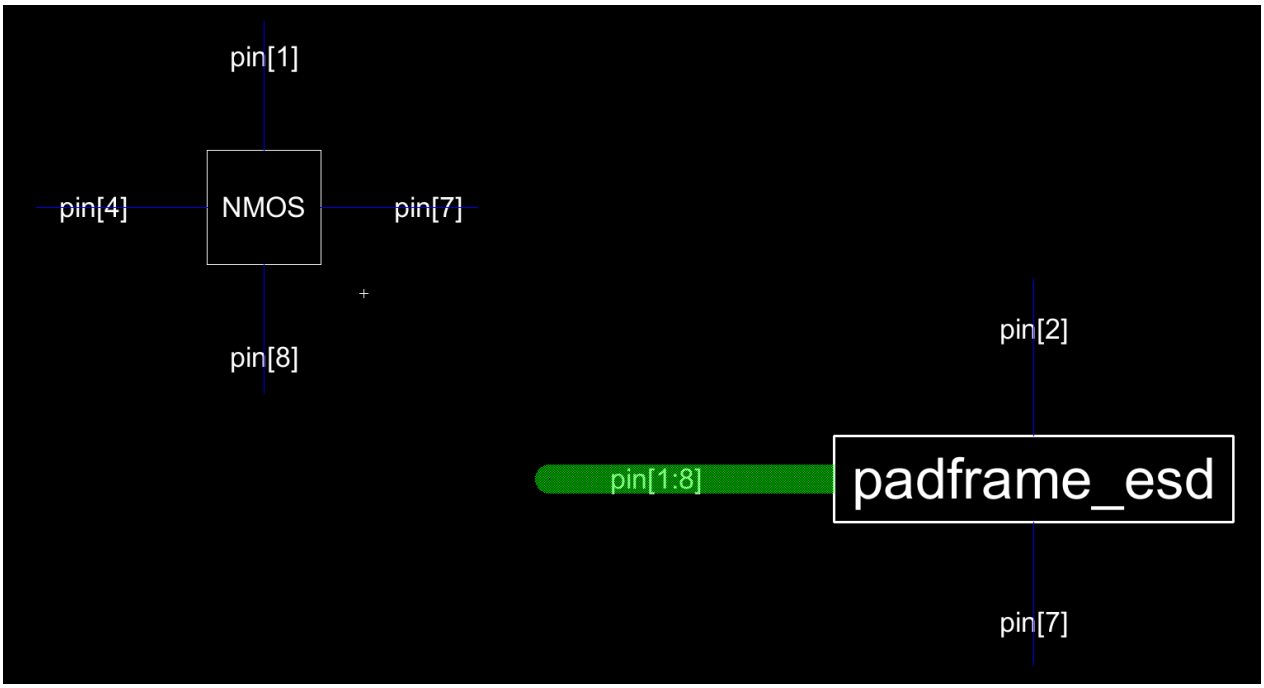

Figure 10.1: ESD-Protected NMOS IC Schematic and Icon

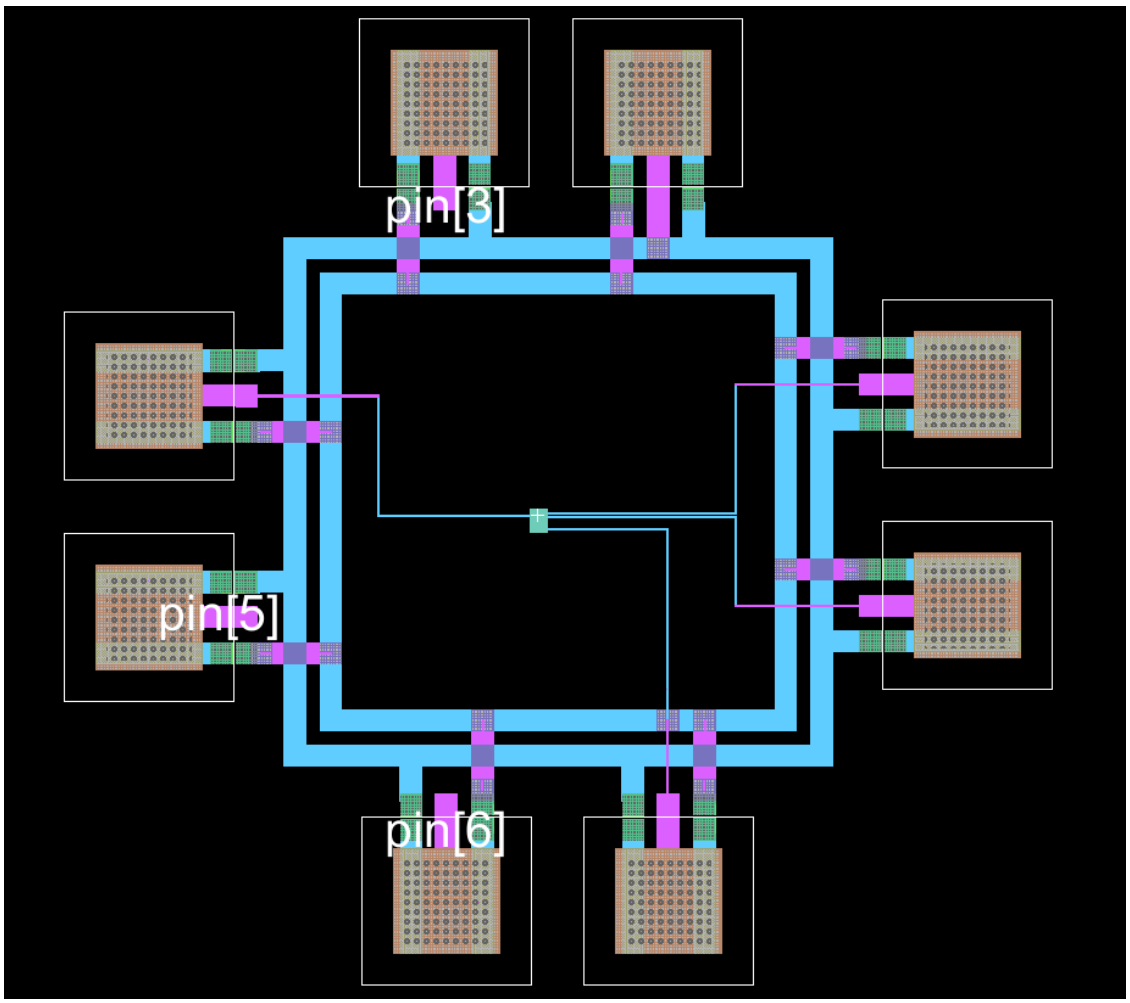

Figure 10.2: ESD-Protected NMOS IC Layout

- Below is the table of the connections of the 4-pin NMOS relative to the padframe

4-pin NMOS I/O	**Padframe Pins**
gate	pin[4]
bulk	pin[7]
source	pin[8]
drain	pin[1]
vdd	pin[2]

Note: pin[3], pin[5], and pin[6] in the padframe is unused

Table 10.1: 4-pin ESD-Protected NMOS IC Pin Connections

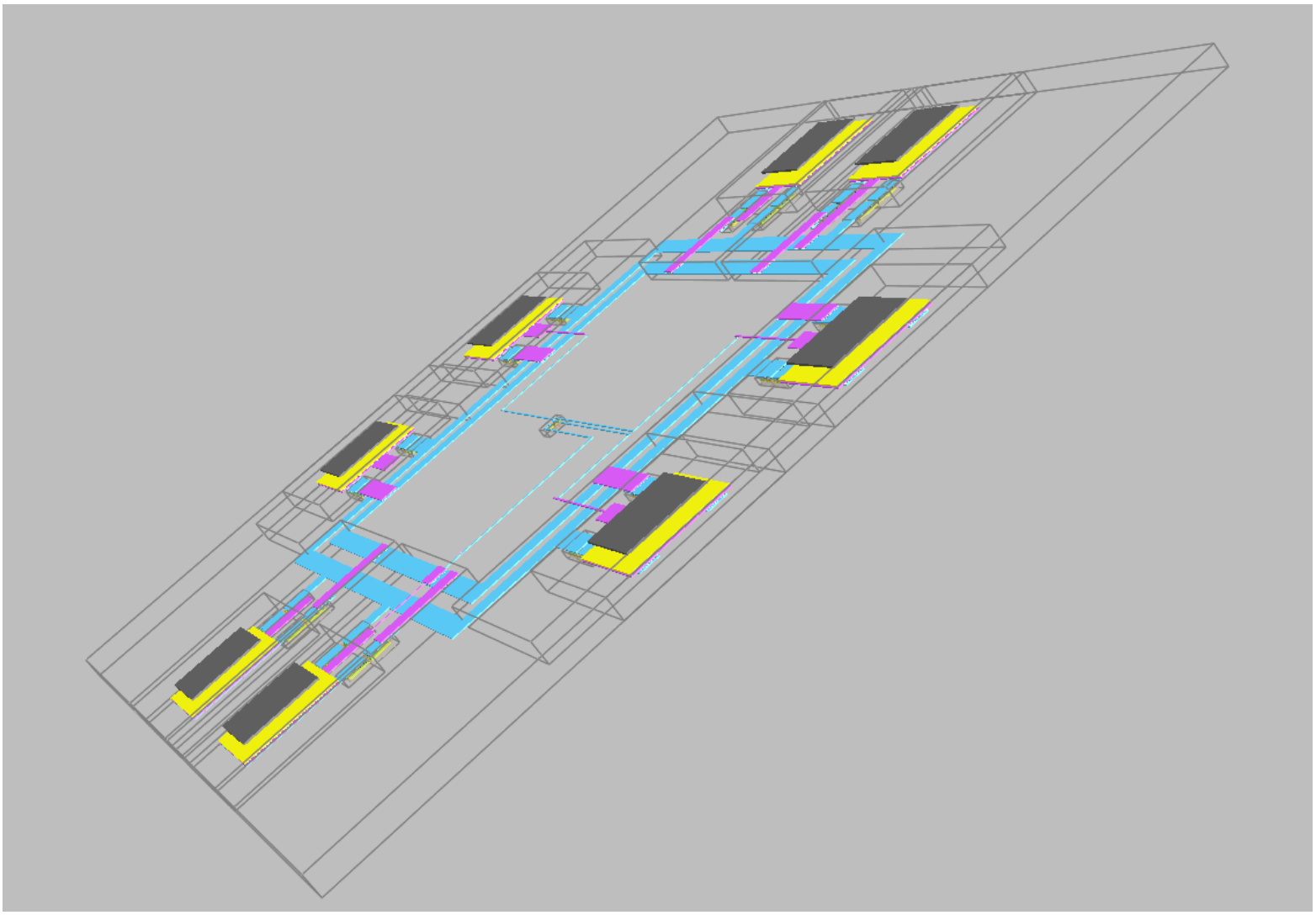

Figure 10.3: 3D View of ESD-Protected NMOS IC Layout

DRC and LVS Check

```
Checking schematic cell 'NMOS_IV{sch}'
   No errors found
Checking schematic cell 'pActive_nWell{sch}'
   No errors found
Checking schematic cell 'nActive_pWell{sch}'
   No errors found
Checking schematic cell 'pad_esd{sch}'
   No errors found
Checking schematic cell 'padframe_esd{sch}'
   No errors found
Checking schematic cell 'final_ic_esd{sch}'
   No errors found
Checking icon cell 'pActive_nWell{ic}'
   No errors found
Checking icon cell 'padframe_esd{ic}'
   No errors found
Checking icon cell 'pad_esd{ic}'
   No errors found
Checking icon cell 'nActive_pWell{ic}'
   No errors found
Checking icon cell 'NMOS_IV{ic}'
   No errors found
0 errors and 0 warnings found (took 0.01 secs)
```

Figure 11.1: Error Check on ESD-Protected NMOS IC Schematic

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 9 networks
0 errors and 0 warnings found (took 0.015 secs)
```

Figure 11.2: DRC Check on ESD-Protected NMOS IC Layout

```
Hierarchical NCC every cell in the design: cell 'final_ic_esd{sch}'  cell 'final_ic_esd{lay}'
Comparing: lab_3_nmos_esd_template:NMOS_IV{sch} with: lab_3_nmos_esd_template:NMOS_IV{lay}
  exports match, topologies match, sizes not checked in 0.09 seconds.
Comparing: lab_3_nmos_esd_template:pActive_nWell{sch} with: lab_3_nmos_esd_template:pActive_nWell{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: lab_3_nmos_esd_template:nActive_pWell{sch} with: lab_3_nmos_esd_template:nActive_pWell{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: lab_3_nmos_esd_template:pad_esd{sch} with: lab_3_nmos_esd_template:pad_esd{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Comparing: lab_3_nmos_esd_template:padframe_esd{sch} with: lab_3_nmos_esd_template:padframe_esd{lay}
  exports match, topologies match, sizes not checked in 0.005 seconds.
Comparing: lab_3_nmos_esd_template:final_ic_esd{sch} with: lab_3_nmos_esd_template:final_ic_esd{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.131 seconds.
```

Figure 11.3: NCC Check on ESD-Protected NMOS IC Layout