Lab 6 Report
Charge Pump

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Goal

Understand how to design the schematic and layout of a DC-to-DC charge pump regulator and analyze its functionality. The charge pump should output 2V and drive a 2 MΩ resistor.

Procedure

To design a charge pump, we would need to cascade capacitors and diodes together – the idea with cascading them together is to pump each capacitor through the cascaded line continuously. Instead of using a diode, we will be using a transistor in its place.

Let's start with designing a 3-stage charge pump.

- Below are the schematic, icon, and layout views of the 3-stage charge pump. Notice how the number of stages coincides with the number of transistor and capacitor cascades.

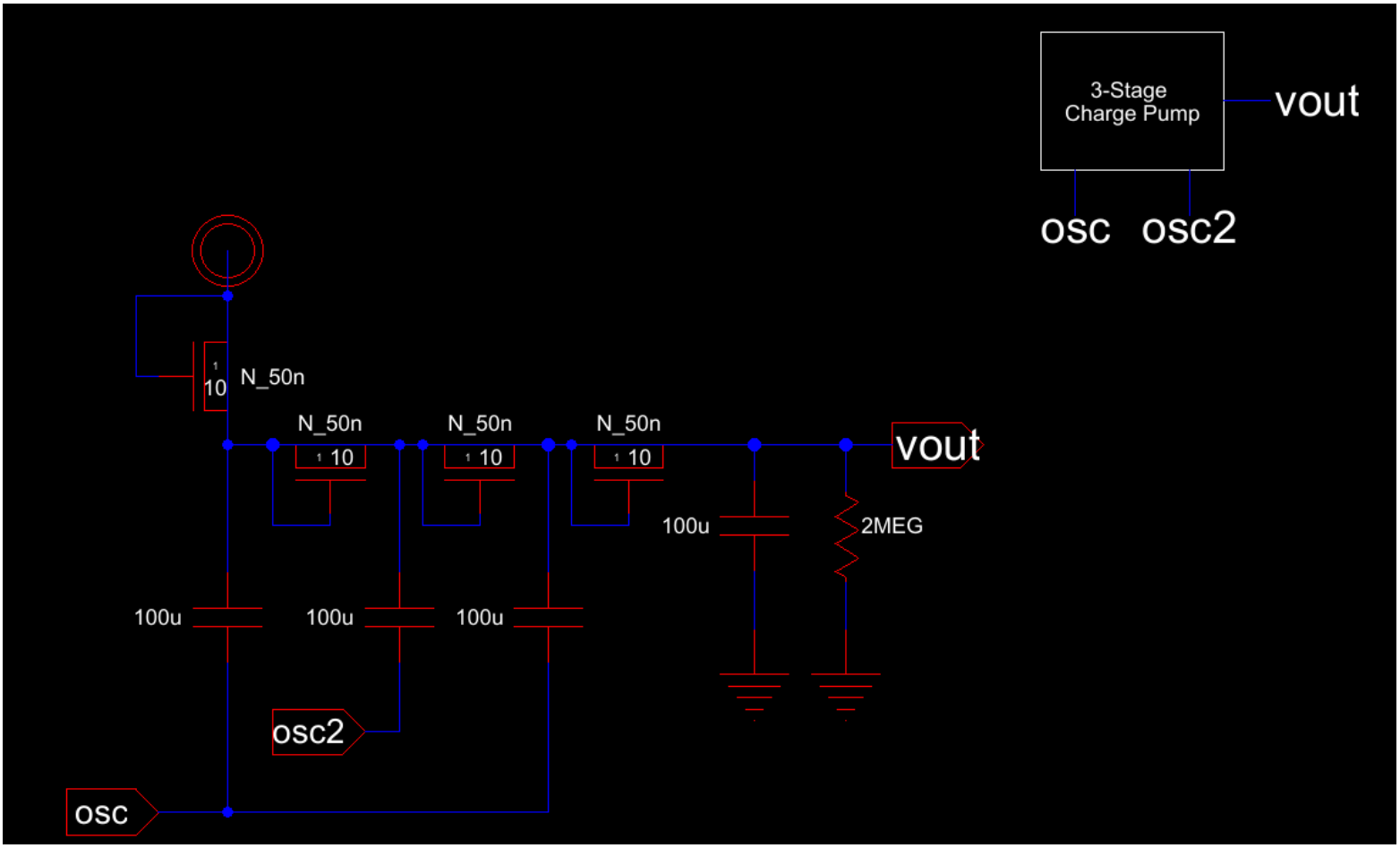

Figure 1.1: Schematic and Icon of 3-Stage Charge Pump

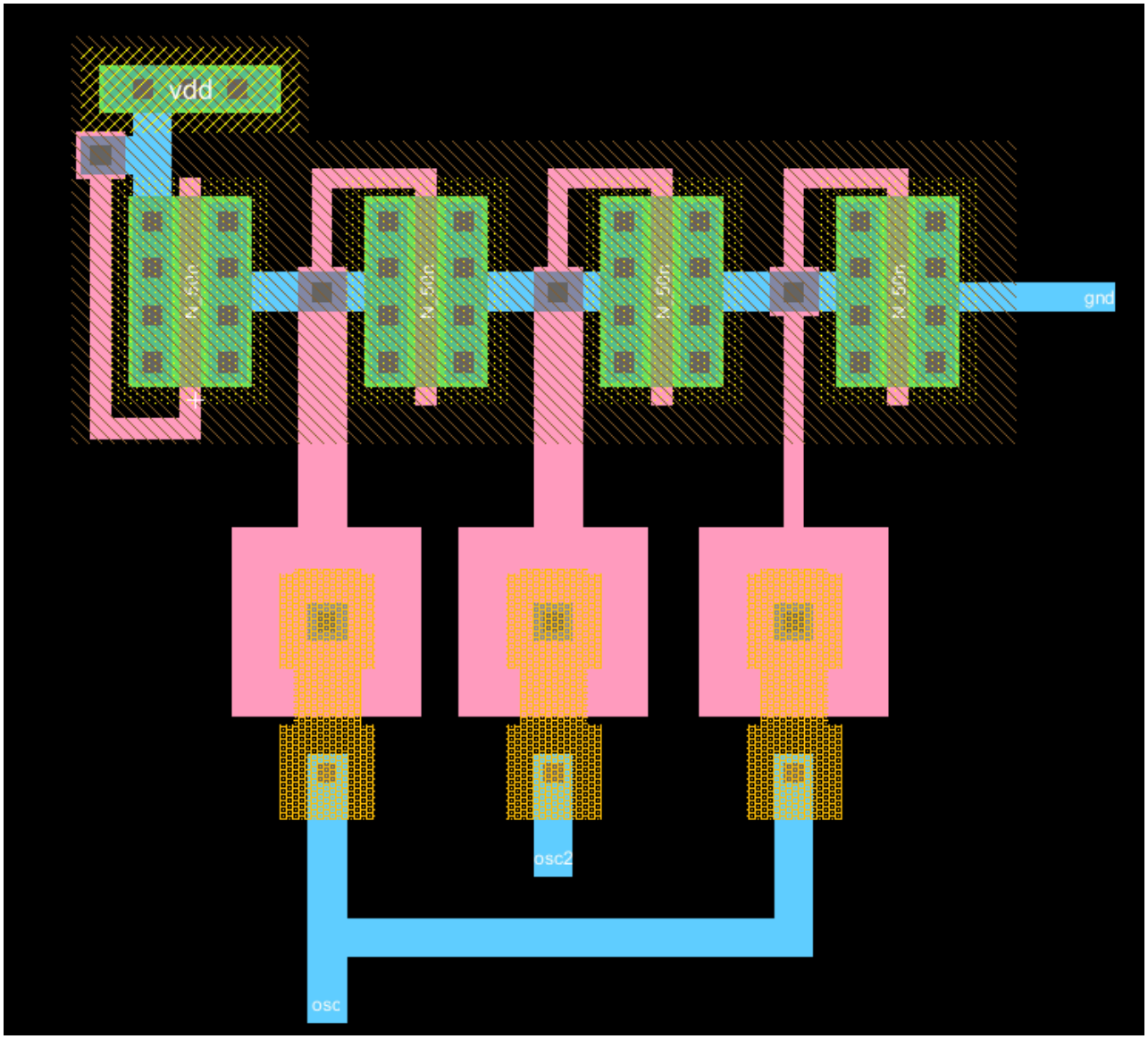

Figure 1.2: Layout of 3-Stage Charge Pump

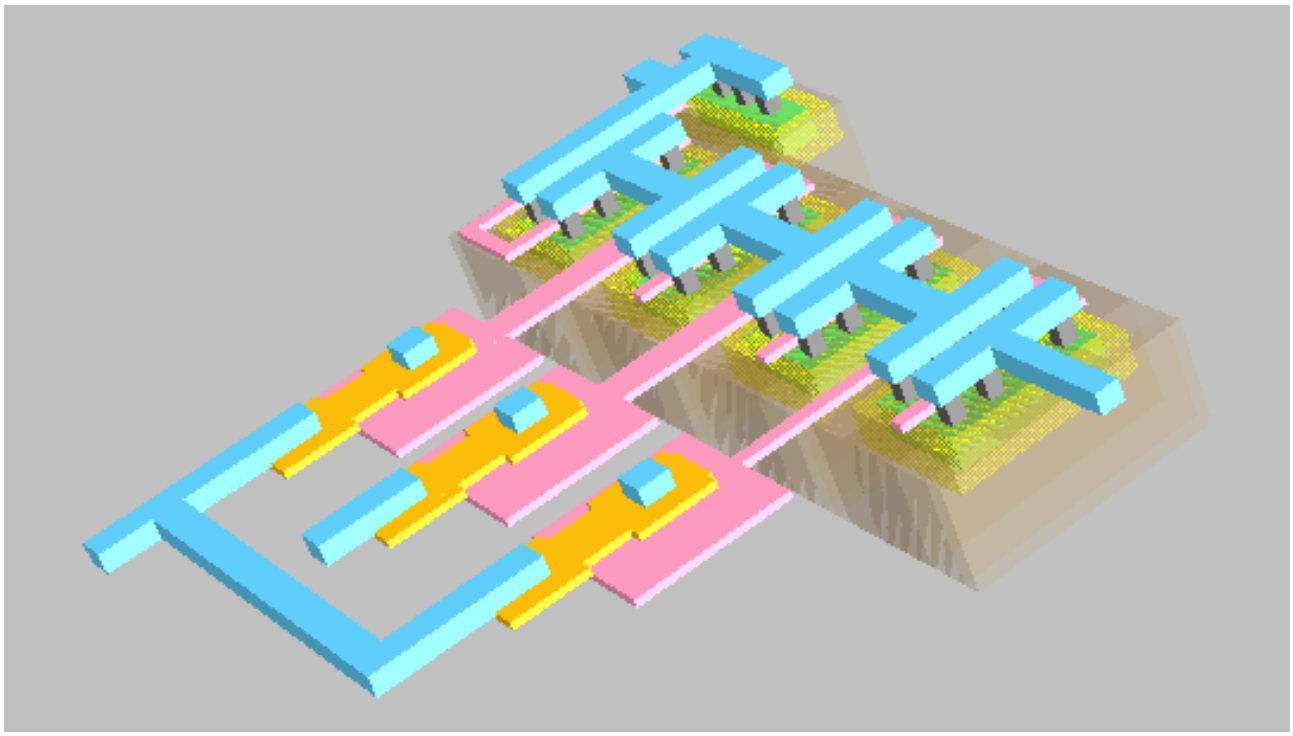

Figure 1.3: 3D View of 3-Stage Charge Pump

- Below is the simulation of the 3-stage charge pump. The input to V_{dd} is 1V DC, and V_{osc} & V_{osc2} oscillate between 0V and 1V. It takes roughly 270s for the design to flatline at a consistent 1.905 V

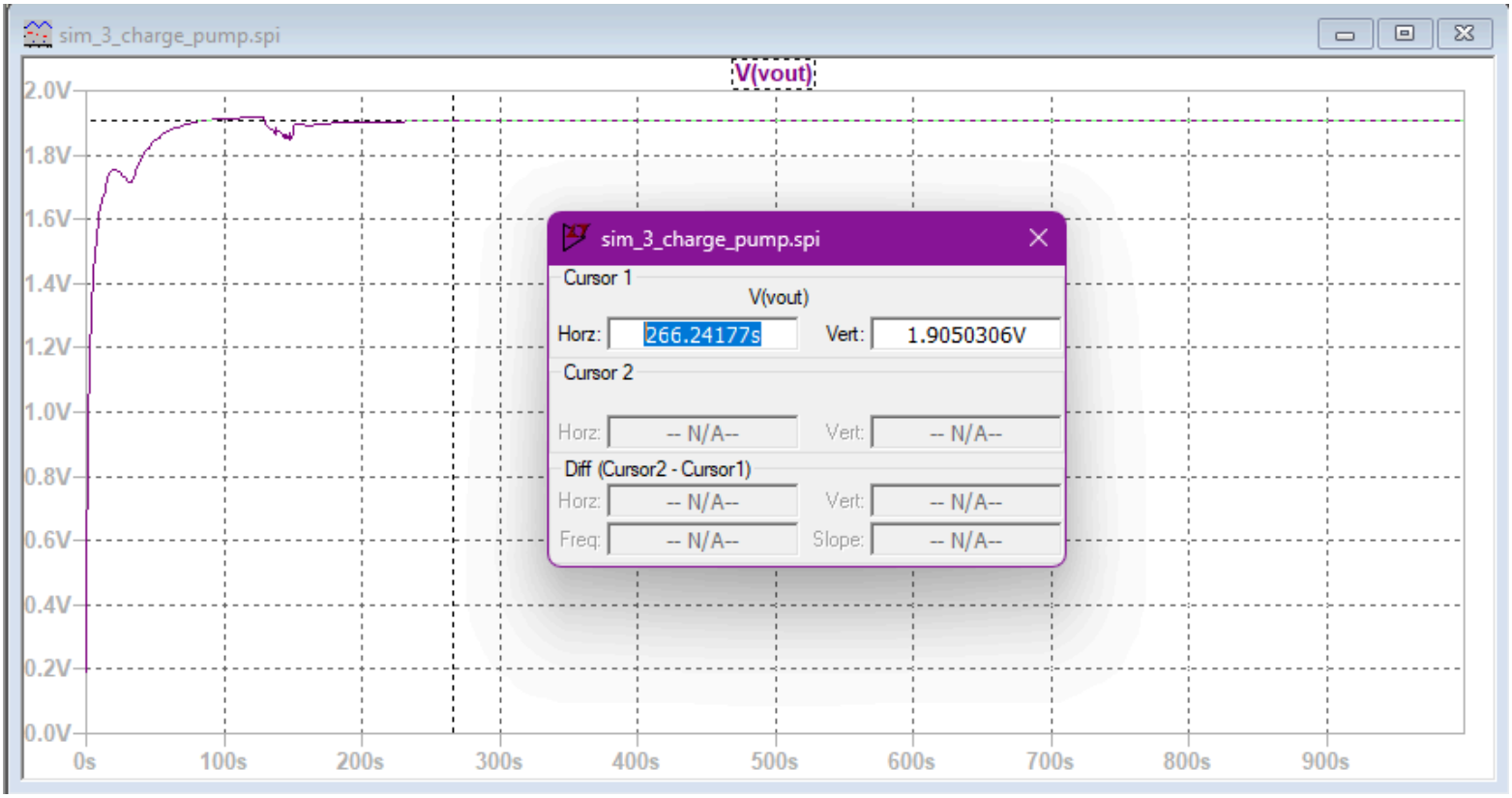

Figure 1.4: Simulation of 3-Stage Charge Pump

DRC & LVS NCC Check for 3-Stage Charge Pump

```
================================2455================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 12 networks
0 errors and 0 warnings found (took 0.027 secs)
================================2456================================
Checking schematic cell '3_charge_pump{sch}'
   No errors found
Checking icon cell '3_charge_pump{ic}'
   No errors found
0 errors and 0 warnings found (took 0.002 secs)
================================2457================================
Hierarchical NCC every cell in the design: cell '3_charge_pump{sch}'  cell '3_charge_pump{lay}'
Comparing: lab_6_charge_pump:3_charge_pump{sch} with: lab_6_charge_pump:3_charge_pump{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
```

Let’s increase the voltage by designing a 5-stage charge pump.

- Below are the schematic, icon, and layout views of the 5-stage charge pump. Same as the 3-stage charge pump the number of stages coincides with the number of transistors and capacitor cascades.

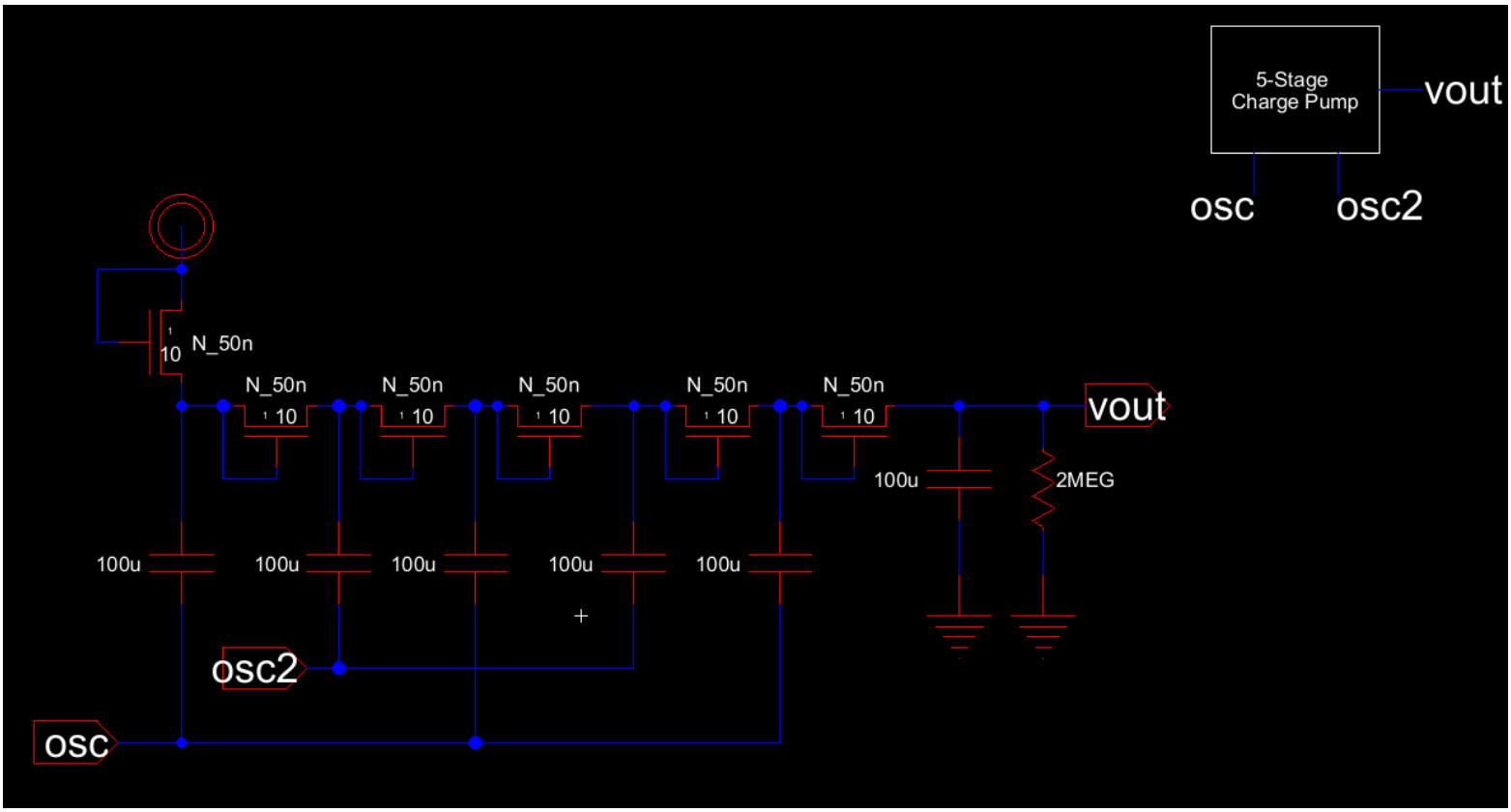

Figure 2.1: Schematic and Icon of 5-Stage Charge Pump

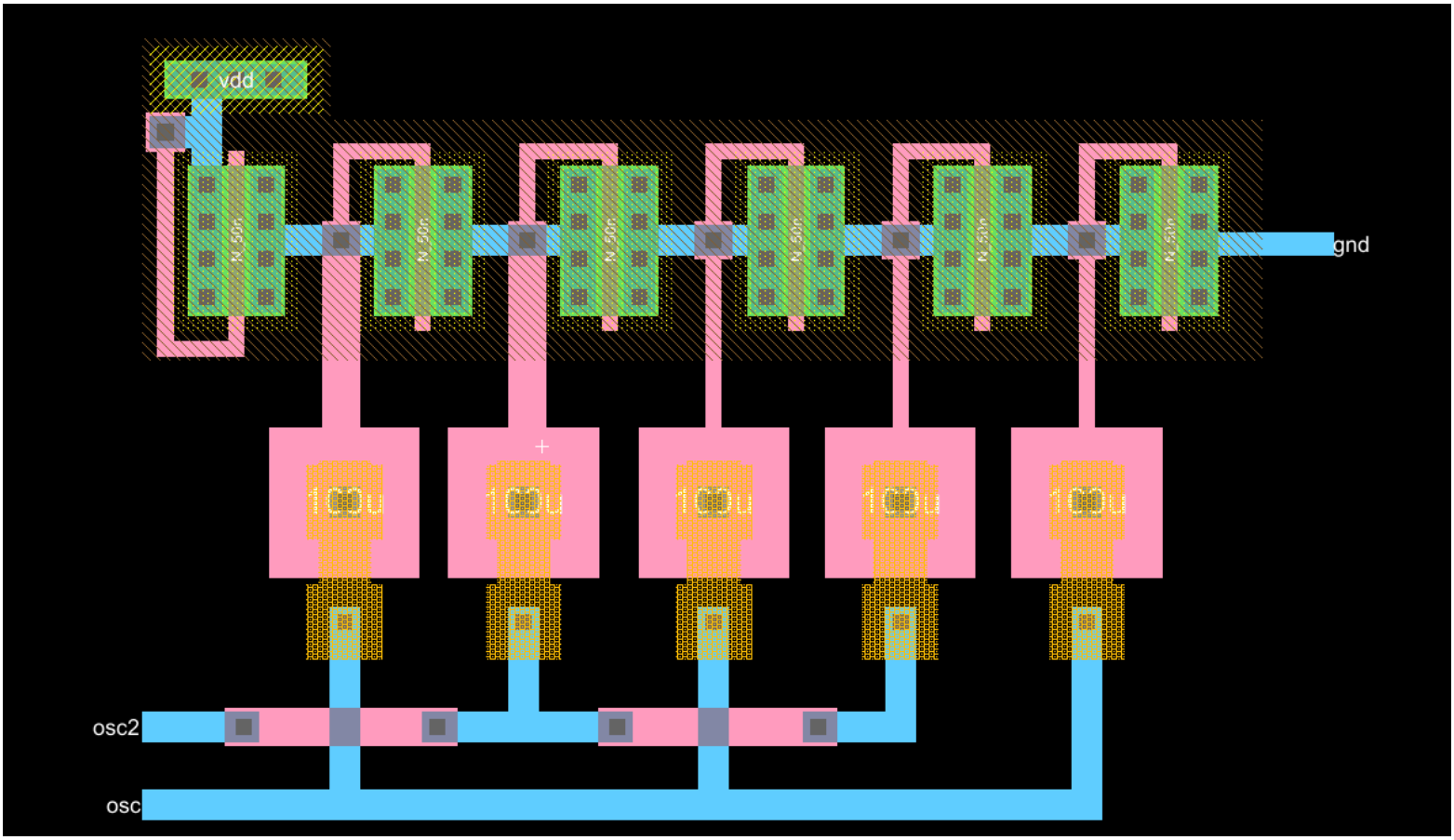

Figure 2.2: Layout of 5-Stage Charge Pump

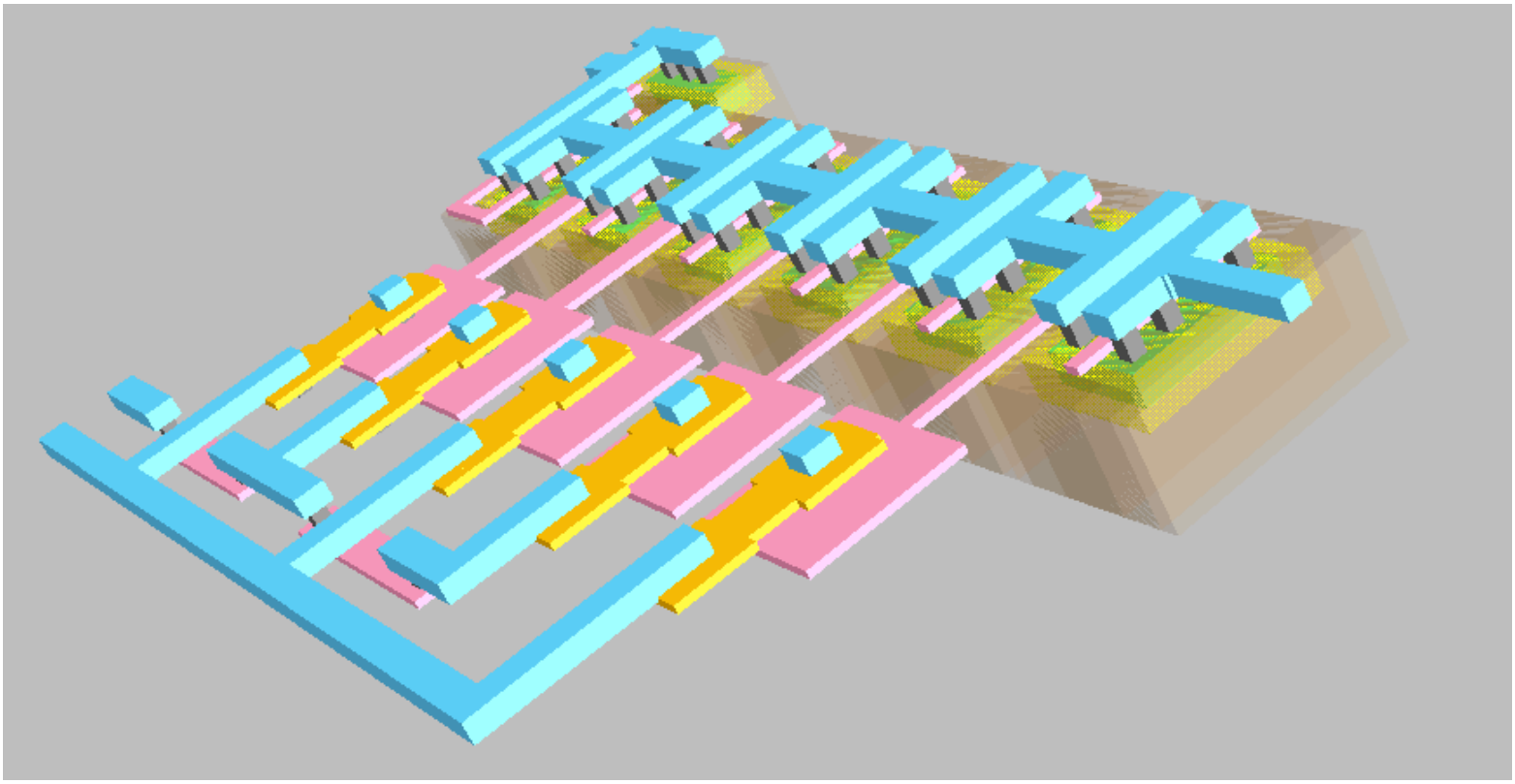

Figure 2.3: 3D View of 5-Stage Charge Pump

- Below is the simulation of the 3-stage charge pump. The input to V_{dd} is 1V DC, and V_{osc} & V_{osc2} oscillate between 0V and 1V. It takes roughly 570s for the design to flatline at a consistent 2.44 V

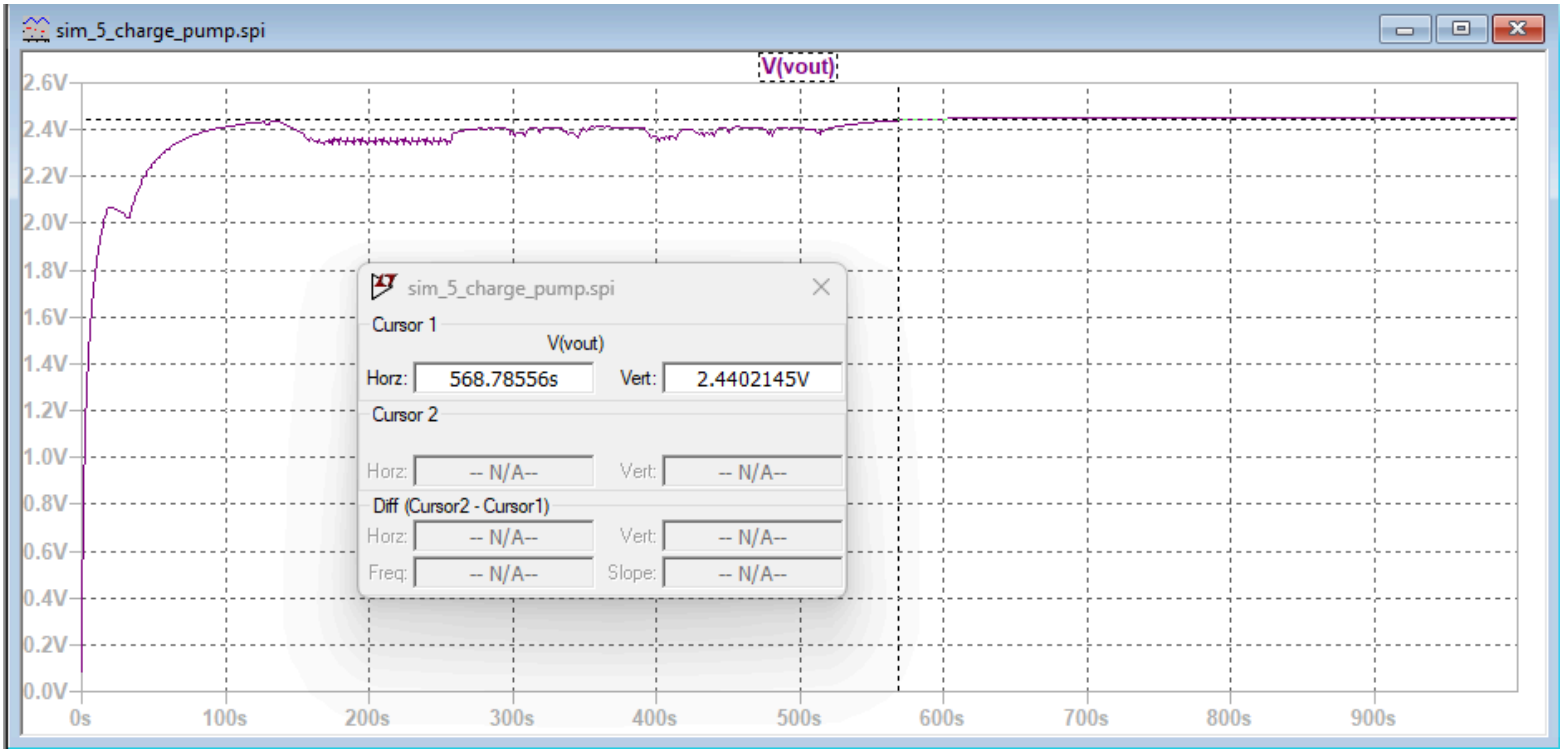

Figure 2.4: Simulation of 5-Stage Charge Pump

DRC & LVS NCC Check for 5-Stage Charge Pump

```
================================7043================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 16 networks
0 errors and 0 warnings found (took 0.001 secs)
================================7044================================
Hierarchical NCC every cell in the design: cell '5_charge_pump{sch}'  cell '5_charge_pump{lay}'
Comparing: lab_6_charge_pump:5_charge_pump{sch} with: lab_6_charge_pump:5_charge_pump{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
```

Our next design is the ring oscillator with an enable.

- Below are the schematic, icon, and layout views of the ring oscillator. There are 6 PMOS in the pull-up network and 6 NMOS in the pull-down network; the design is 4 inverters cascaded, with an enable.

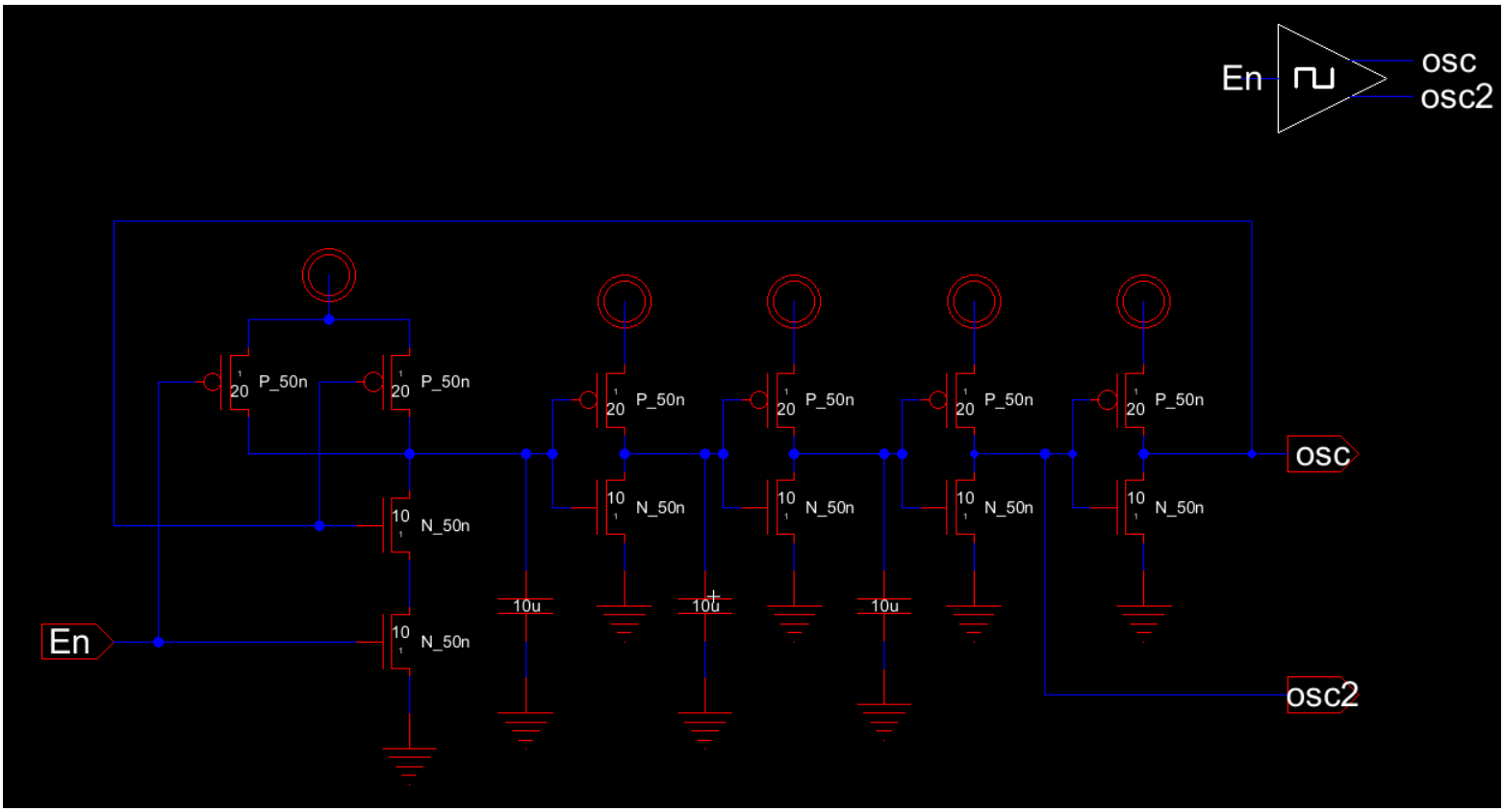

Figure 3.1: Schematic and Icon of Ring Oscillator w/ Enable

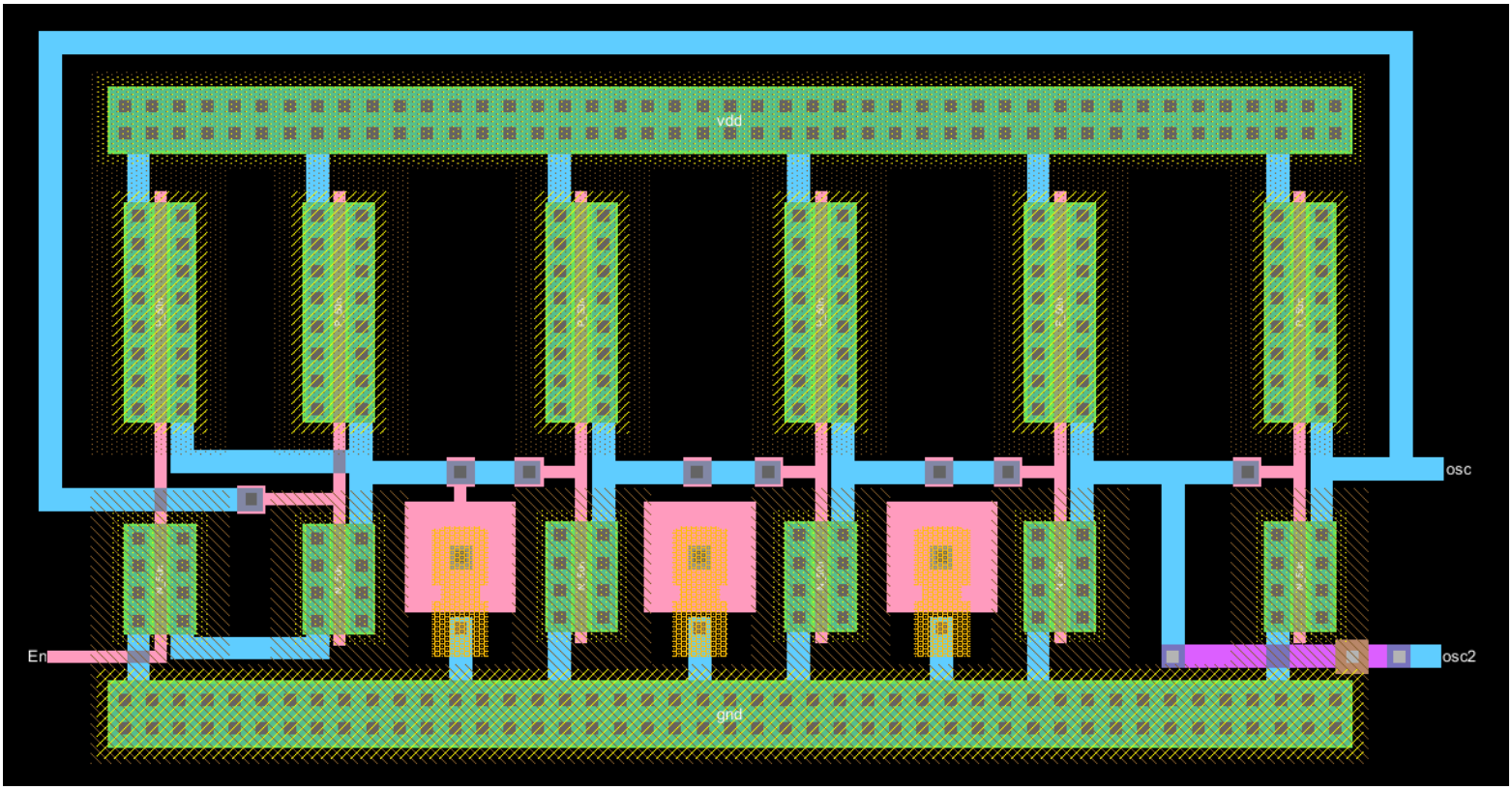

Figure 3.2: Layout of Ring Oscillator w/ Enable

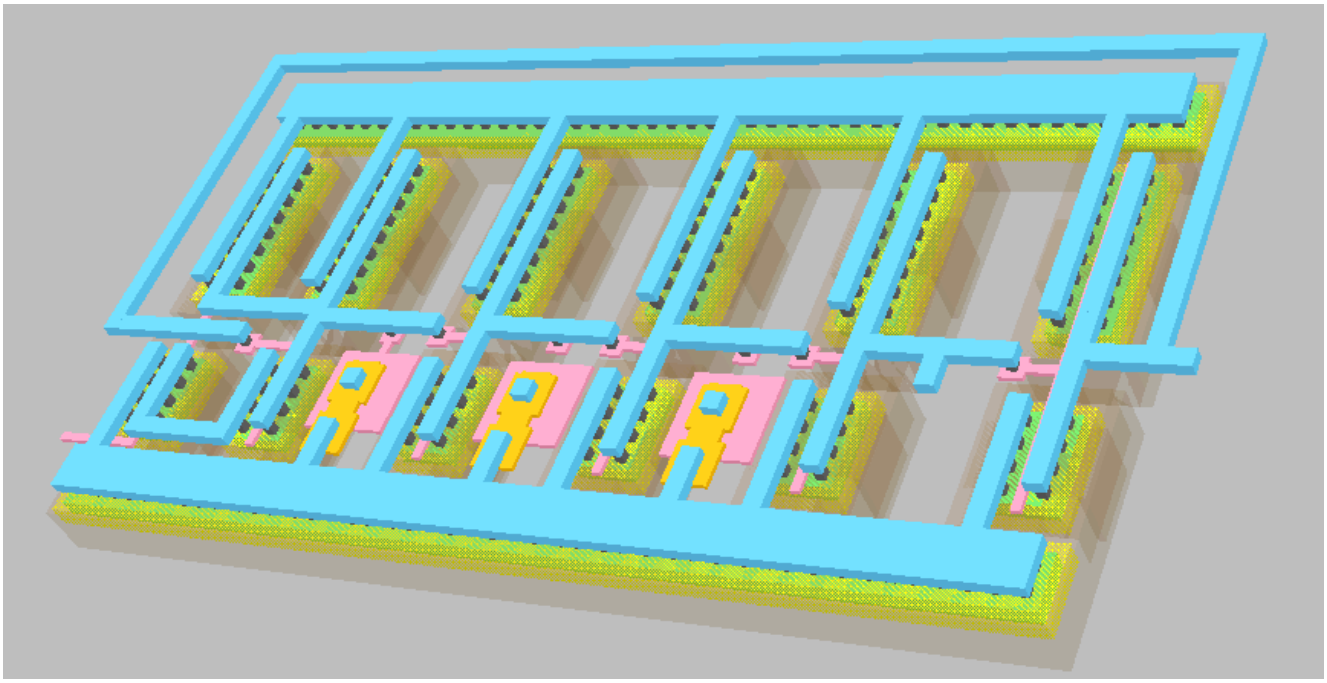

Figure 3.3: 3D View of Ring Oscillator w/ Enable

- Below is the simulation of a ring oscillator. The input enable is set high with 1V, and V_{dd} is tied to 1V. As we see in the simulation, the two output signals are oscillating between 0V and 1V.

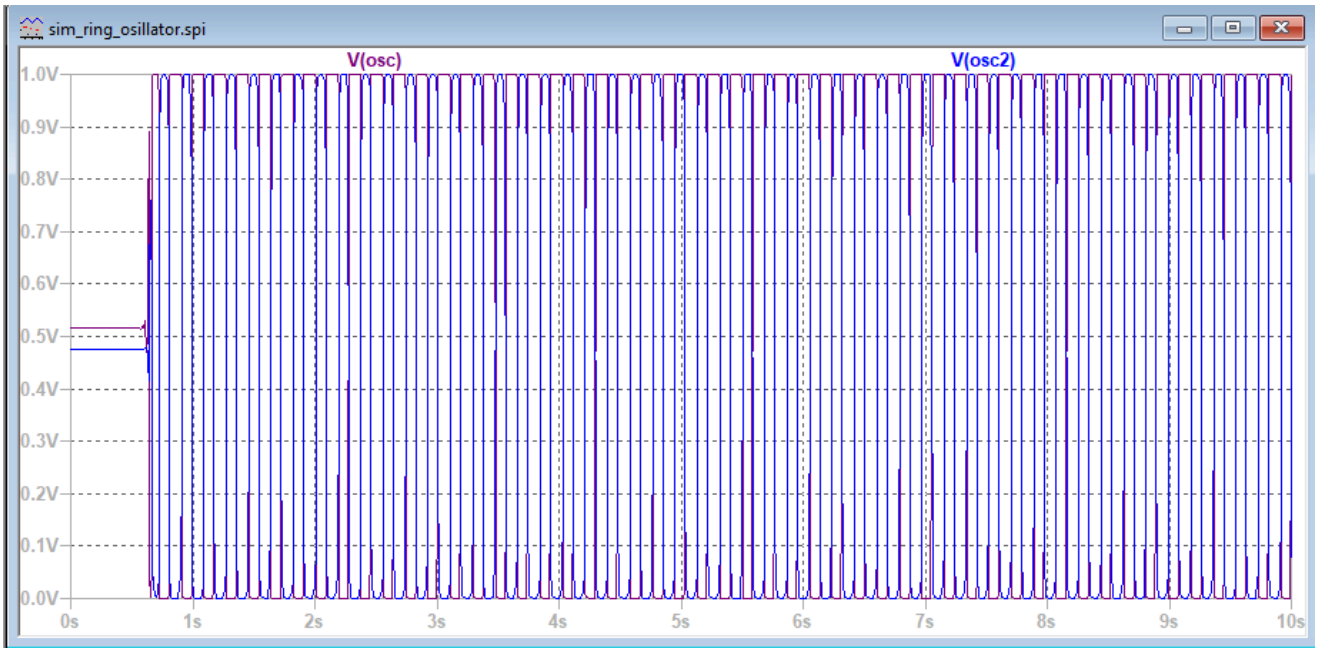

Figure 3.4: Simulation of Ring Oscillator w/ Enable

DRC & LVS NCC Check for Ring Oscillator w/ Enable

```
================================3910================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 24 networks
0 errors and 0 warnings found (took 0.001 secs)
================================3911================================
Hierarchical NCC every cell in the design: cell 'ring_osillator{sch}'  cell 'ring_osillator{lay}'
Comparing: lab_6_charge_pump:ring_osillator{sch} with: lab_6_charge_pump:ring_osillator{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.005 seconds.
```

The next design is a ring voltage regulator, which will be used to maintain a constant voltage.

- Below are the schematic, icon, and layout views of the voltage regulator. This circuit contains 3 PMOS in the pull-up network and 3 NMOS in the pull-down network.

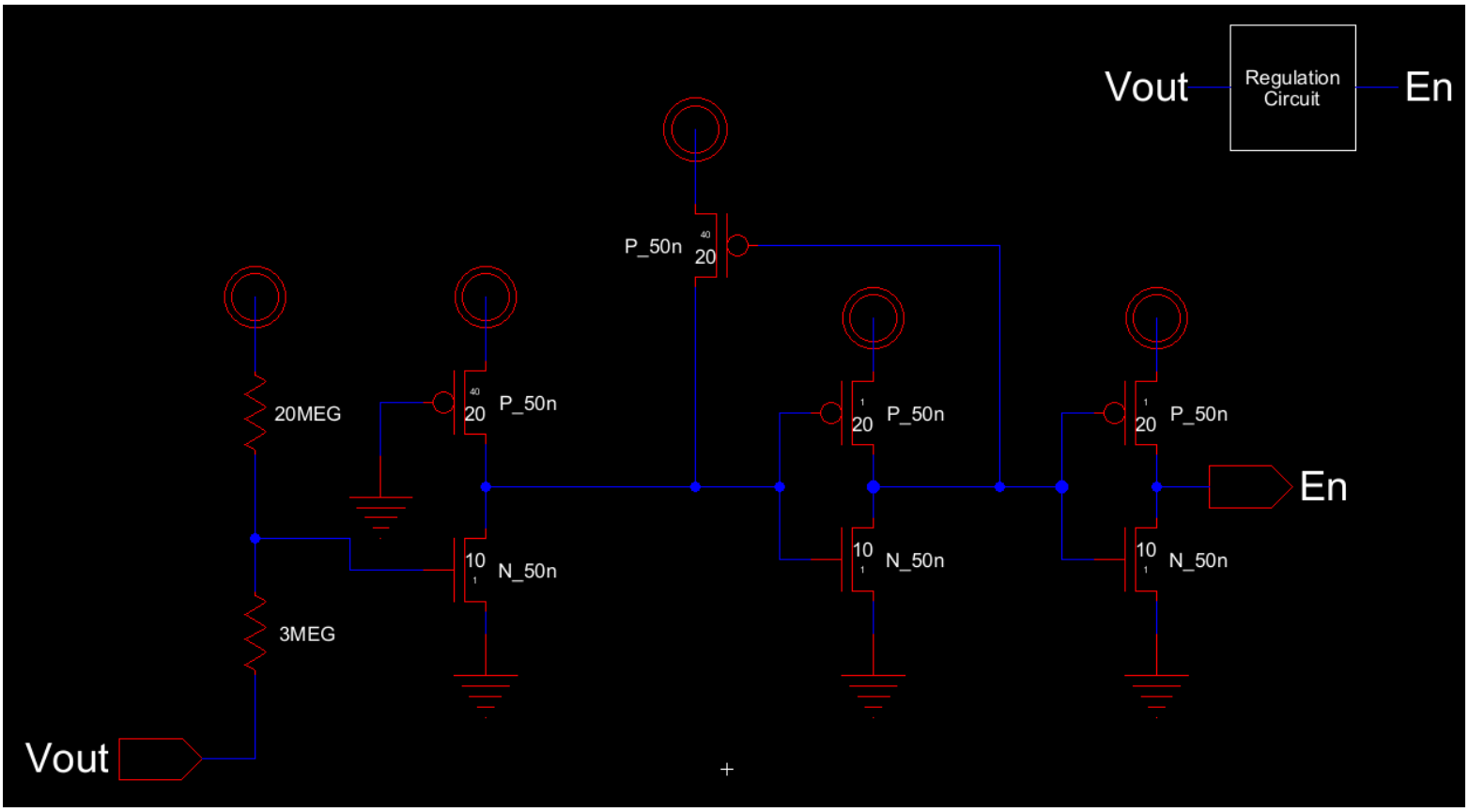

Figure 4.1: Schematic and Icon of Voltage Regulator

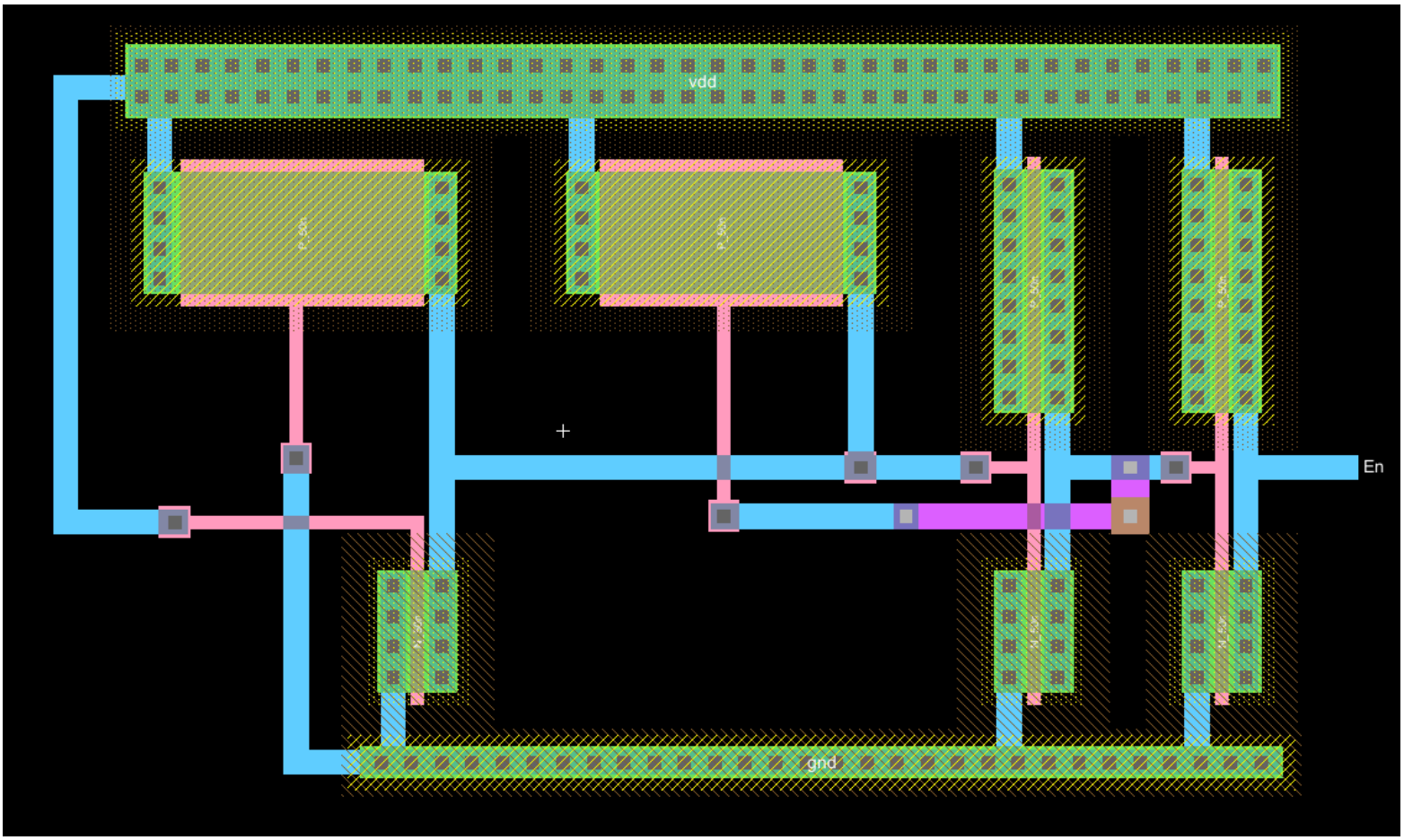

Figure 4.2: Layout of Voltage Regulator

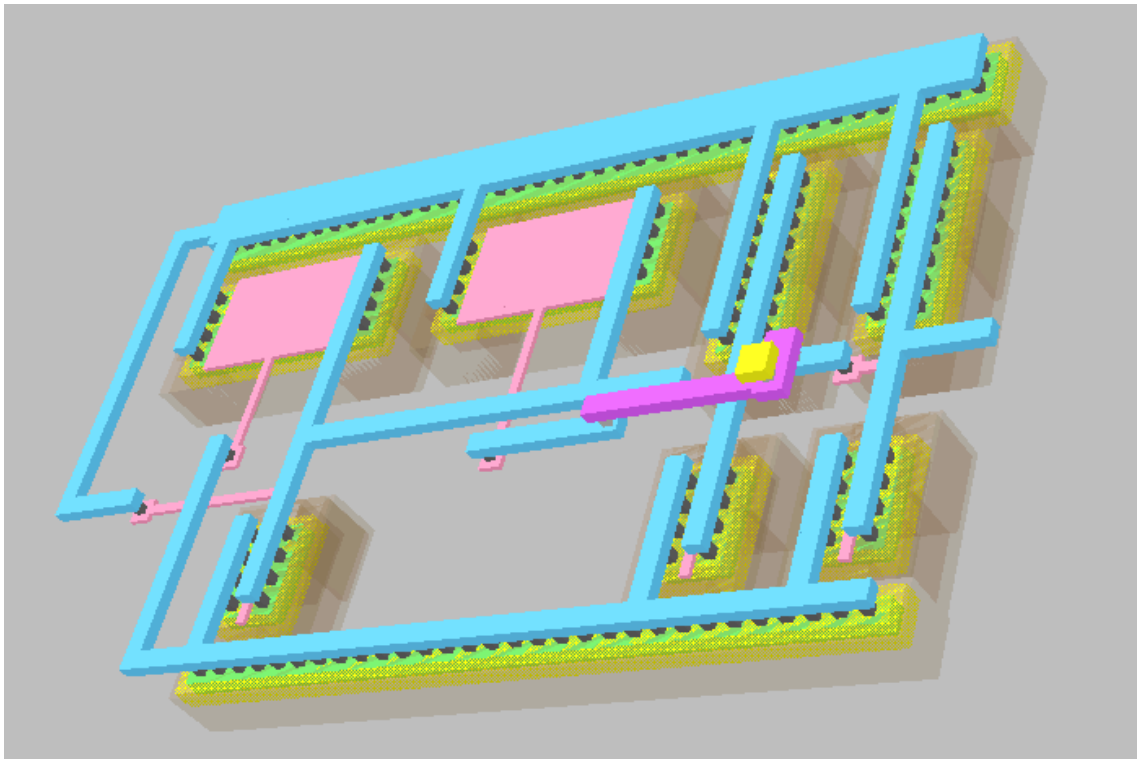

Figure 4.3: 3D View of Voltage Regulator

- Below is the simulation of a voltage regulator. In this simulation, we notice that whenever the sinusoidal wave goes to zero, the enable goes high. This will be useful to keep our circuit active and properly regulated.

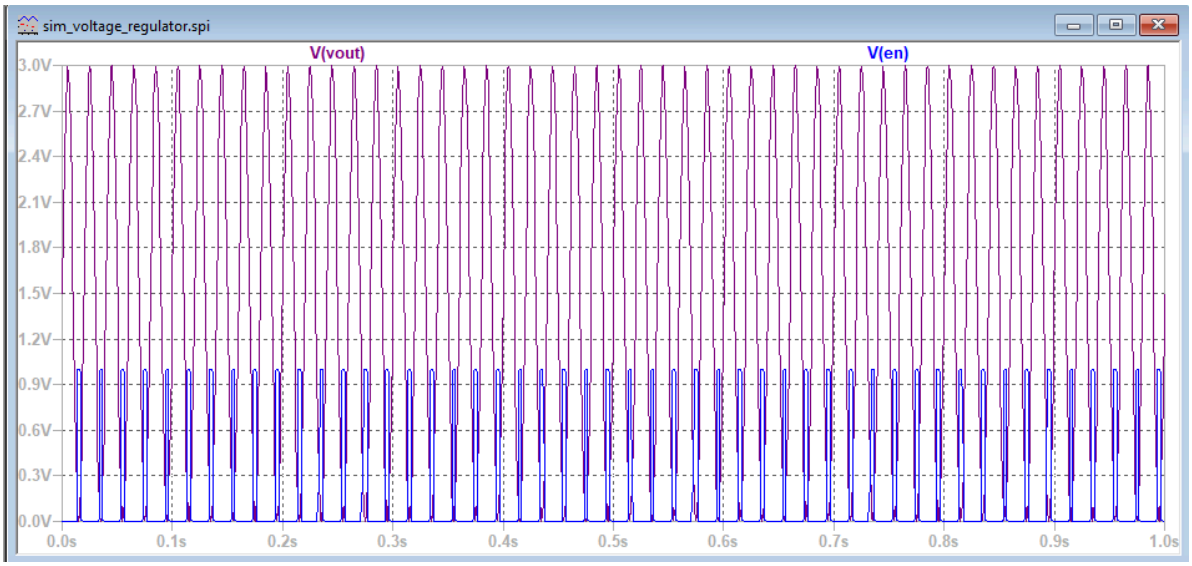

Figure 4.4: Simulation of Voltage Regulator

DRC & LVS NCC Check for Voltage Regulator

```
==================================6600==================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 13 networks
0 errors and 0 warnings found (took 0.001 secs)
==================================6601==================================
Hierarchical NCC every cell in the design: cell 'voltage_regulator{sch}'  cell 'voltage_regulator{lay}'
Comparing: lab_6_charge_pump:voltage_regulator{sch} with: lab_6_charge_pump:voltage_regulator{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
```

Finally, we will connect our 5-stage charge pump, ring oscillator, and voltage regulator together to create our DC-to-DC charge pump regulator.

- Below are the schematic and icon views of the DC-DC Charge Pump Regulator.

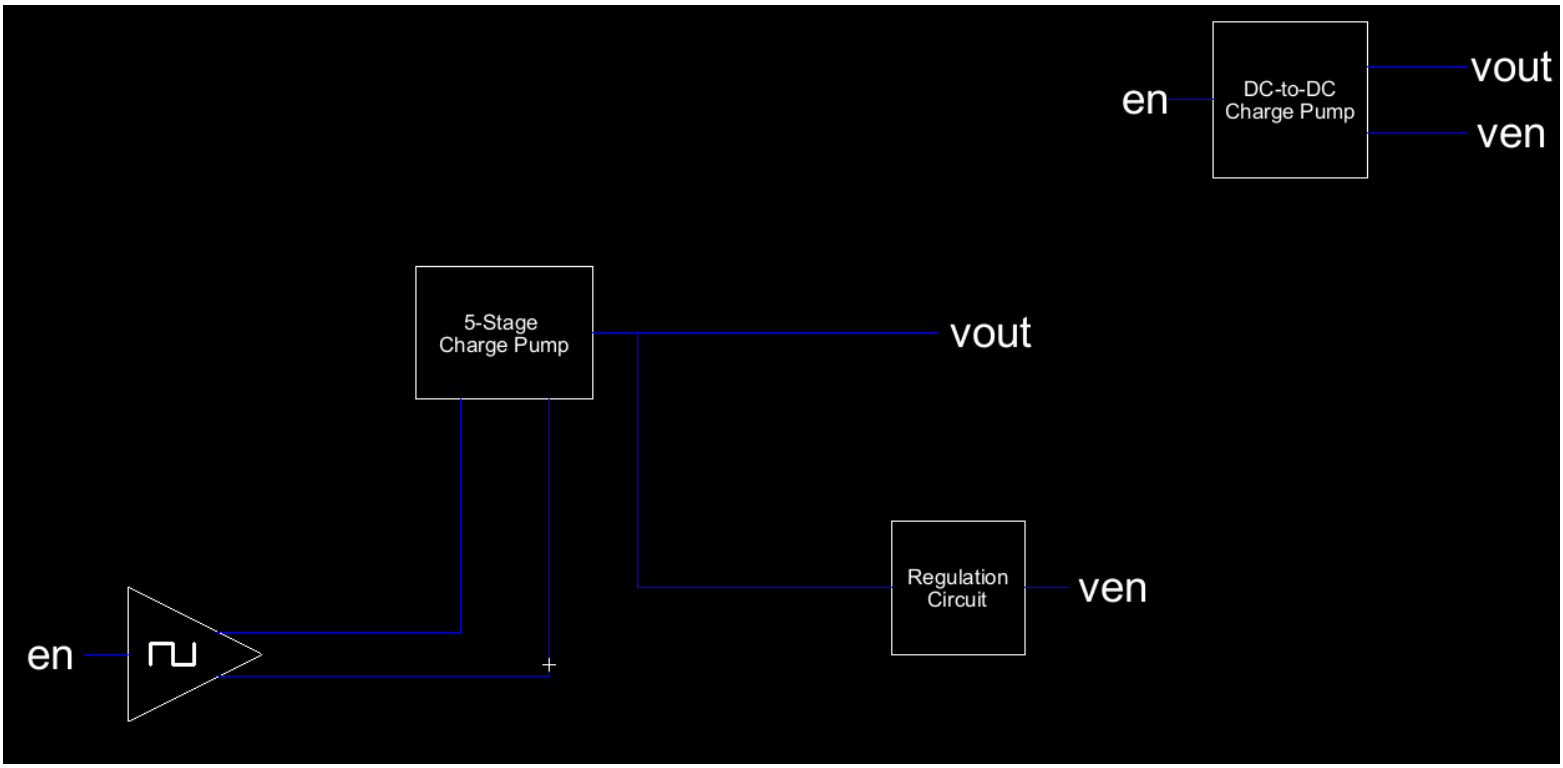

Figure 5.1: Schematic and Icon of DC-DC Charge Pump Regulator

- Below is the simulation of the DC-DC Charge Pump Regulator. As soon as the enable goes low, V_{out} starts to gradually increase.

Figure 5.2: Simulation of DC-DC Charge Pump Regulator