Lab 5 Report
Full Adders

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Goal

Understand how to design the schematic and layout of a full adder and its functionality.

Procedure

To design a full adder, we will need to design gates that consist of the full adder; we will need to design a two-input NAND, a two-input XOR, and a NOT gate.

The first gate I will design is the 2-input NAND gate, and I will simulate to validate functionality.

- Below are the schematic, icon, and layout views of the 2-input NAND gate.

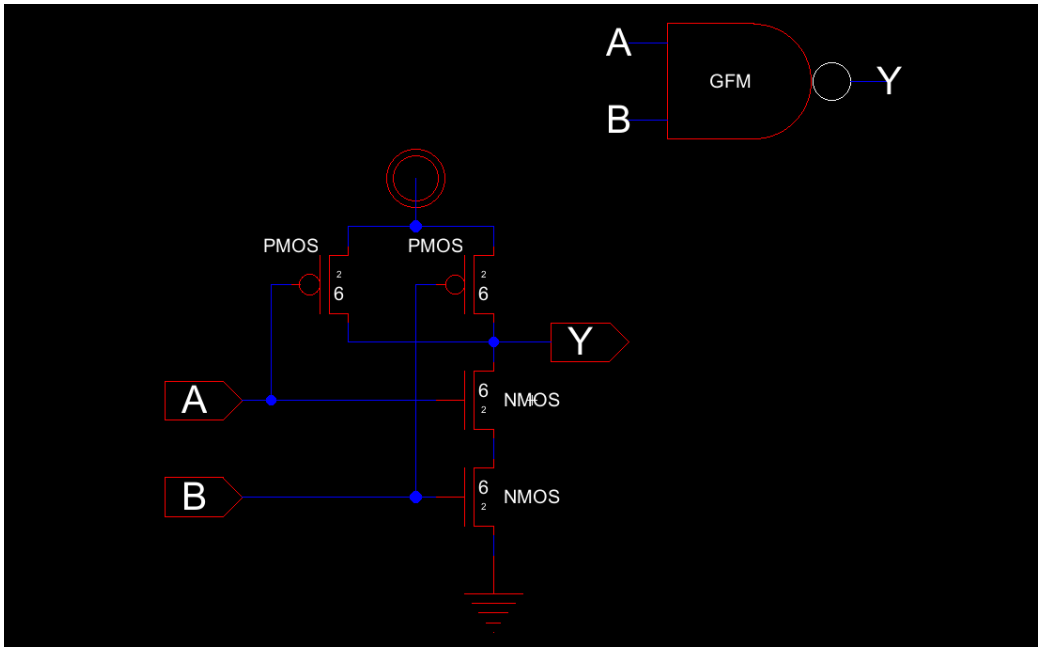

Figure 1.1: Schematic and Icon of 2-Input NAND Gate

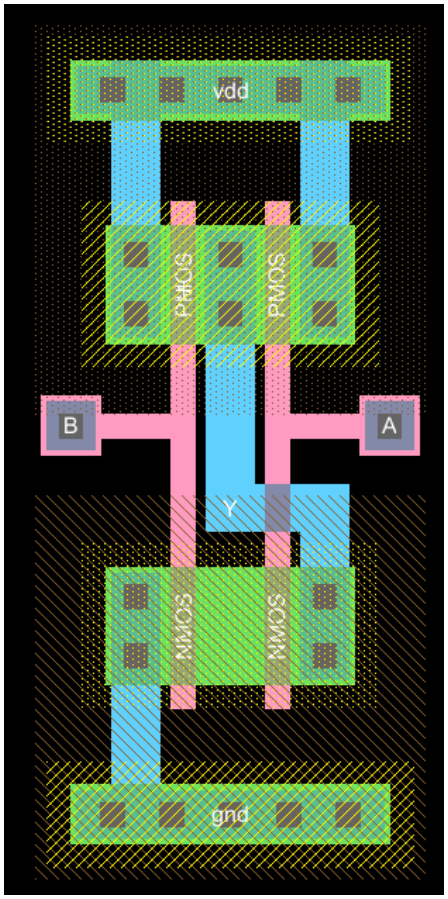

Figure 1.2: Layout of 2-Input NAND Gate

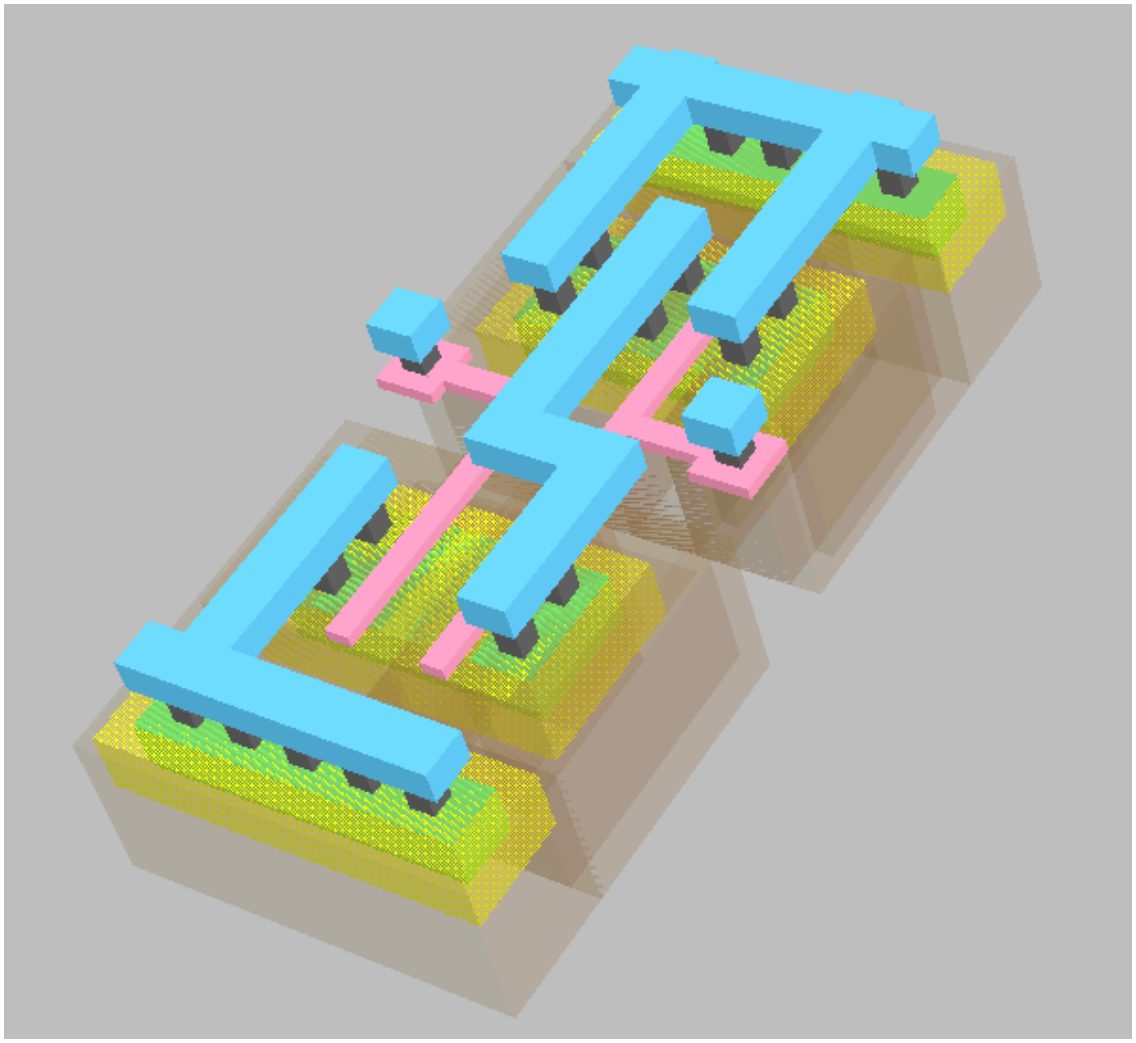

Figure 1.3: 3D View of Layout

- Below is the transition delay simulation of the 2-input NAND gate. We are driving 5V DC to one of the input terminals, which is not shown here.
    - We see that the moment ‘d_in’ starts to rise from 0V to 5V, ‘d_out’ starts to drop from 5V to 0V, as expected. The transition time of ‘d_out’ to drop from 5V to 0V for our design is roughly 1 ns.

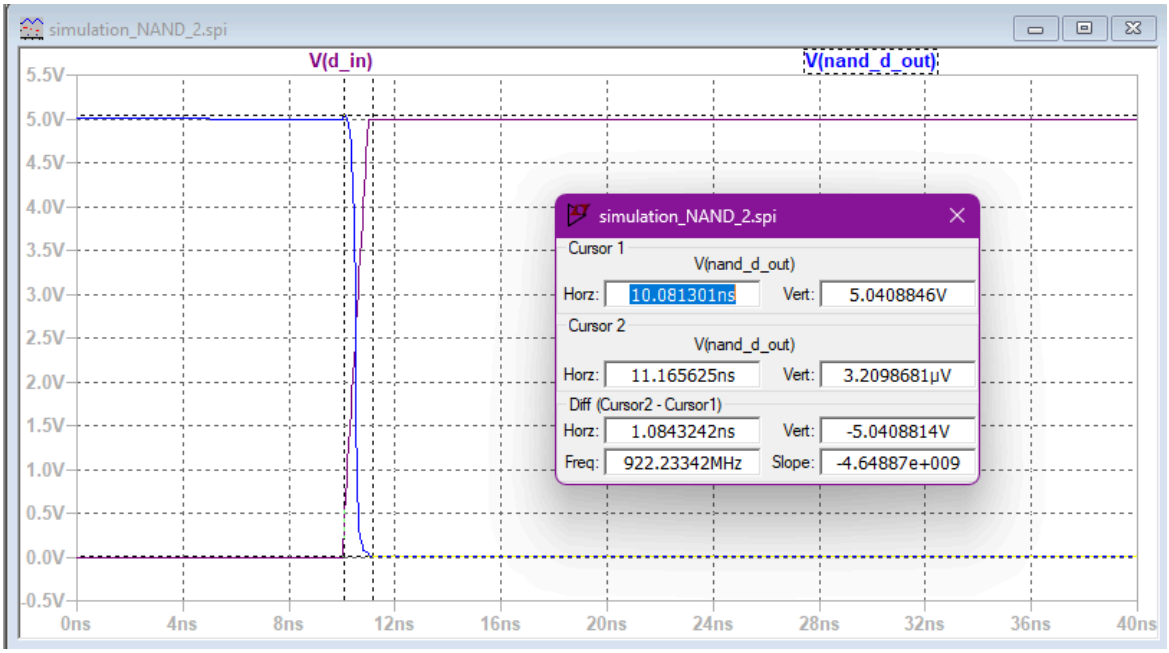

Figure 1.4: Transition Delay Simulation of 2-Input NAND Gate

Table 1.1 displays the truth table of a 2-input NAND gate. Since this is a NAND gate, the output value is the opposite of an AND gate.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 1.1: NAND Gate Truth Table

- Figure 1.5 validates our NAND gate functionality through simulation. The simulation of the NAND gate matches the truth table above.

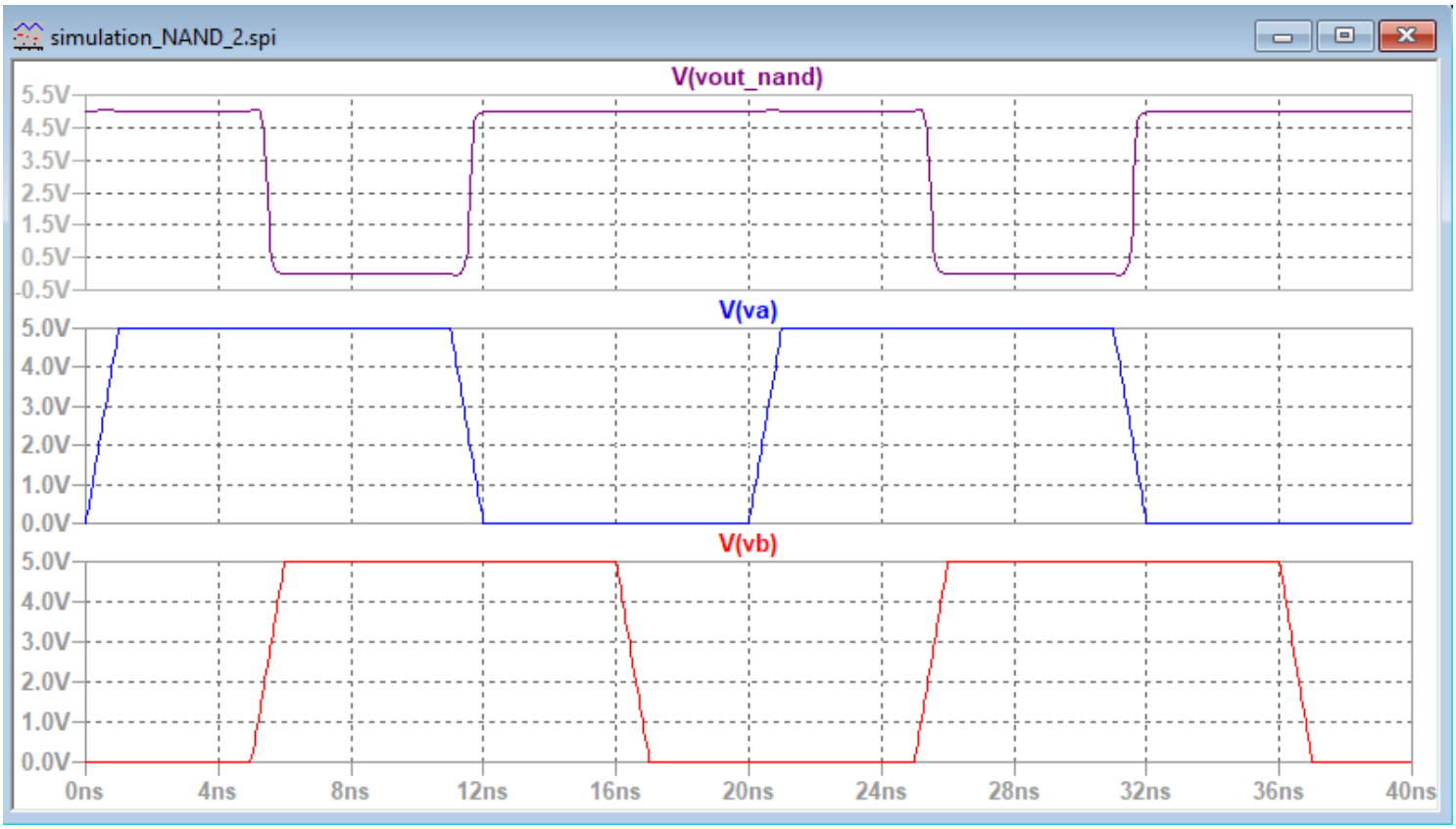

Figure 1.5: 2-Input NAND Gate Truth Table Simulation

DRC & LVS NCC Check for 2-Input NAND Gate

```
================================25================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 6 networks
0 errors and 0 warnings found (took 0.003 secs)
================================26================================
Hierarchical NCC every cell in the design: cell 'simulation_NAND_2{sch}'  cell 'simulation_NAND_2{lay}'
Comparing: lab_5_full_adder:NAND_2{sch} with: lab_5_full_adder:NAND_2{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Comparing: lab_5_full_adder:simulation_NAND_2{sch} with: lab_5_full_adder:simulation_NAND_2{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.007 seconds.
```

The next gate I will design is the NOT gate, and I will simulate to validate functionality.

- Below are the schematic, icon, and layout views of the NOT gate.

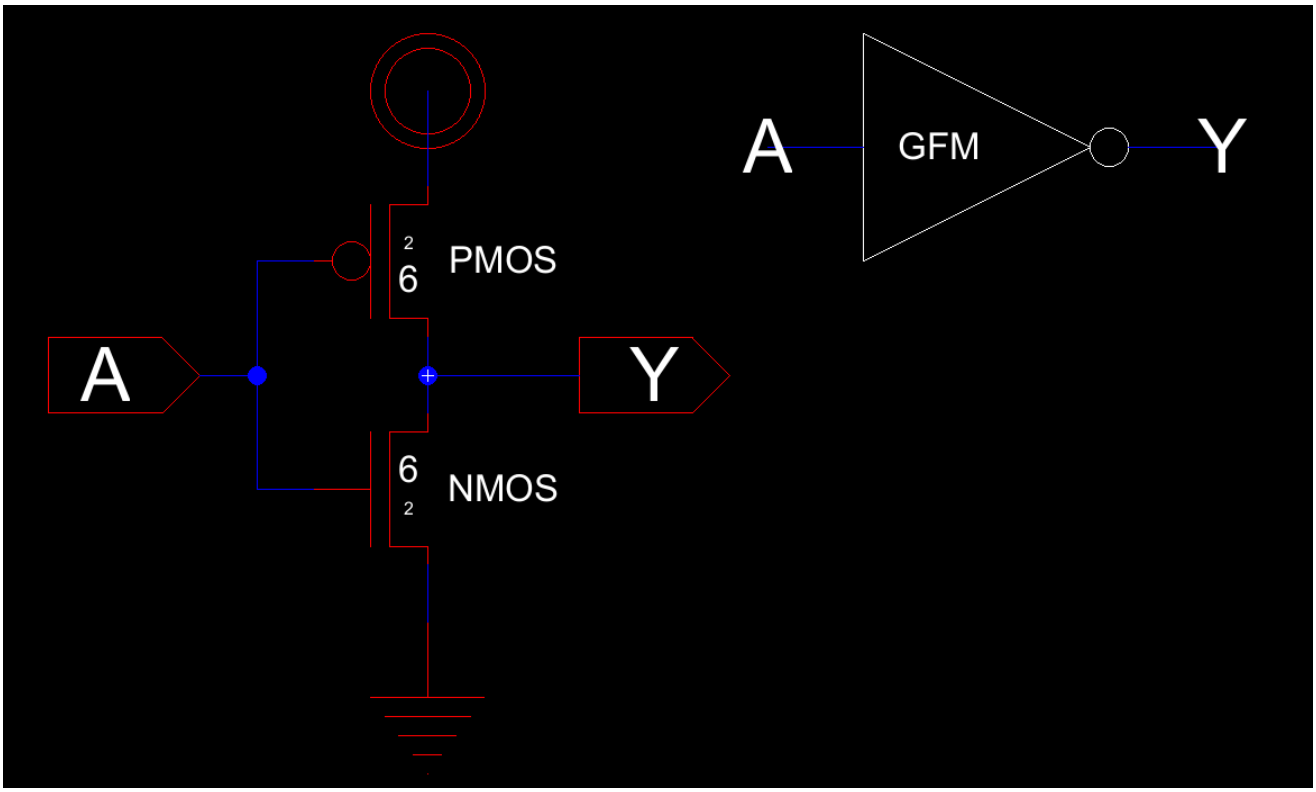

Figure 2.1: Schematic and Icon of NOT Gate

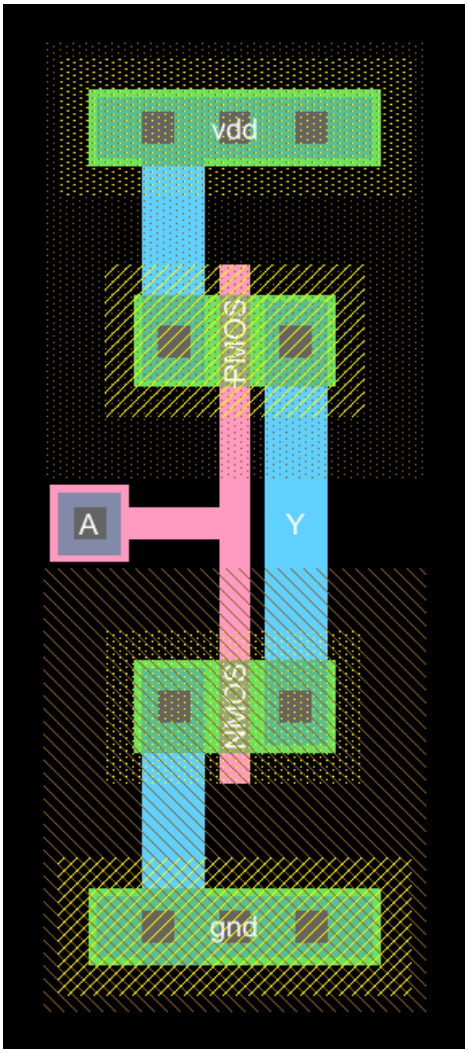

Figure 2.2: Layout of NOT Gate

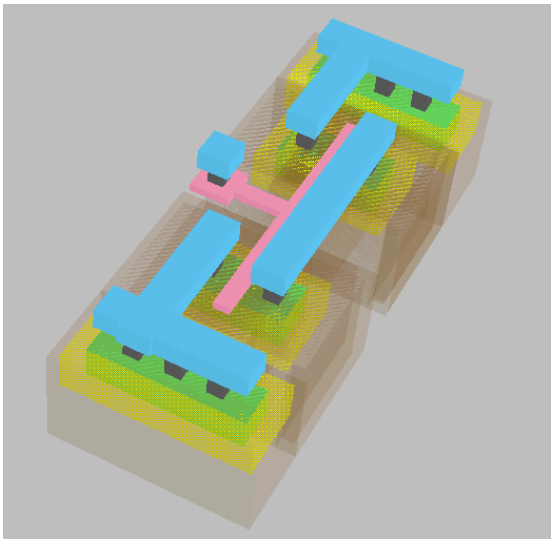

Figure 2.3: 3D View of NOT Gate Layout

- Below is the simulation of a NOT gate; we can analyze the functionality of the NOT gate with the simulation.
    - As the input goes from 0V to 5V, the output goes from 5V to 0V, indicating that the input and output are inverted, as expected.
    - The transition delay is roughly 1 ns for the output to go from high to low based on the input logic of going from low to high.

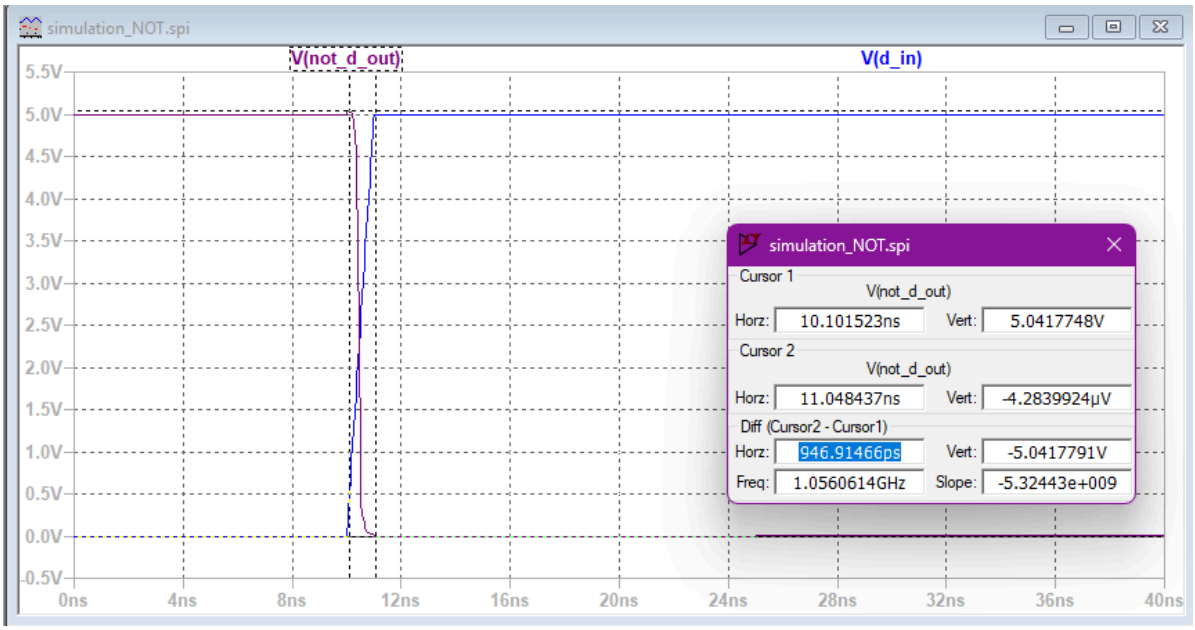

Figure 2.4: Simulation of NOT Gate

DRC & LVS NCC Check for NOT Gate

```
================================834================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 5 networks
Checking cell 'simulation_NOT{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.008 secs)
================================835================================
Hierarchical NCC every cell in the design: cell 'simulation_NOT{sch}'  cell 'simulation_NOT{lay}'
Comparing: lab_5_full_adder:NOT{sch} with: lab_5_full_adder:NOT{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: lab_5_full_adder:simulation_NOT{sch} with: lab_5_full_adder:simulation_NOT{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.004 seconds.
```

The next gate I will design is the 2-input XOR gate, and I will simulate to validate functionality.
To decrease the number of transistors needed to design the XOR gate, I will use two NOT gates in my design.

- Below are the schematic, icon, and layout views of the 2-input XOR gate.

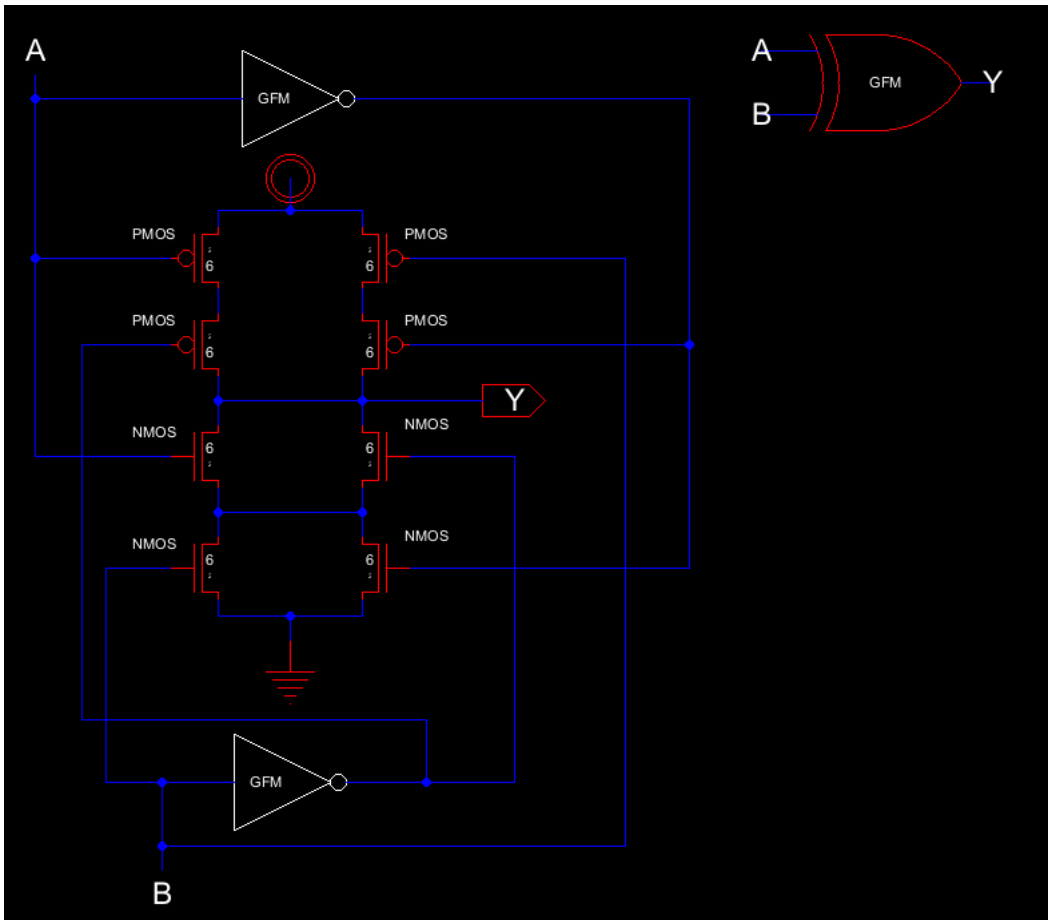

Figure 3.1: Schematic and Icon of XOR Gate

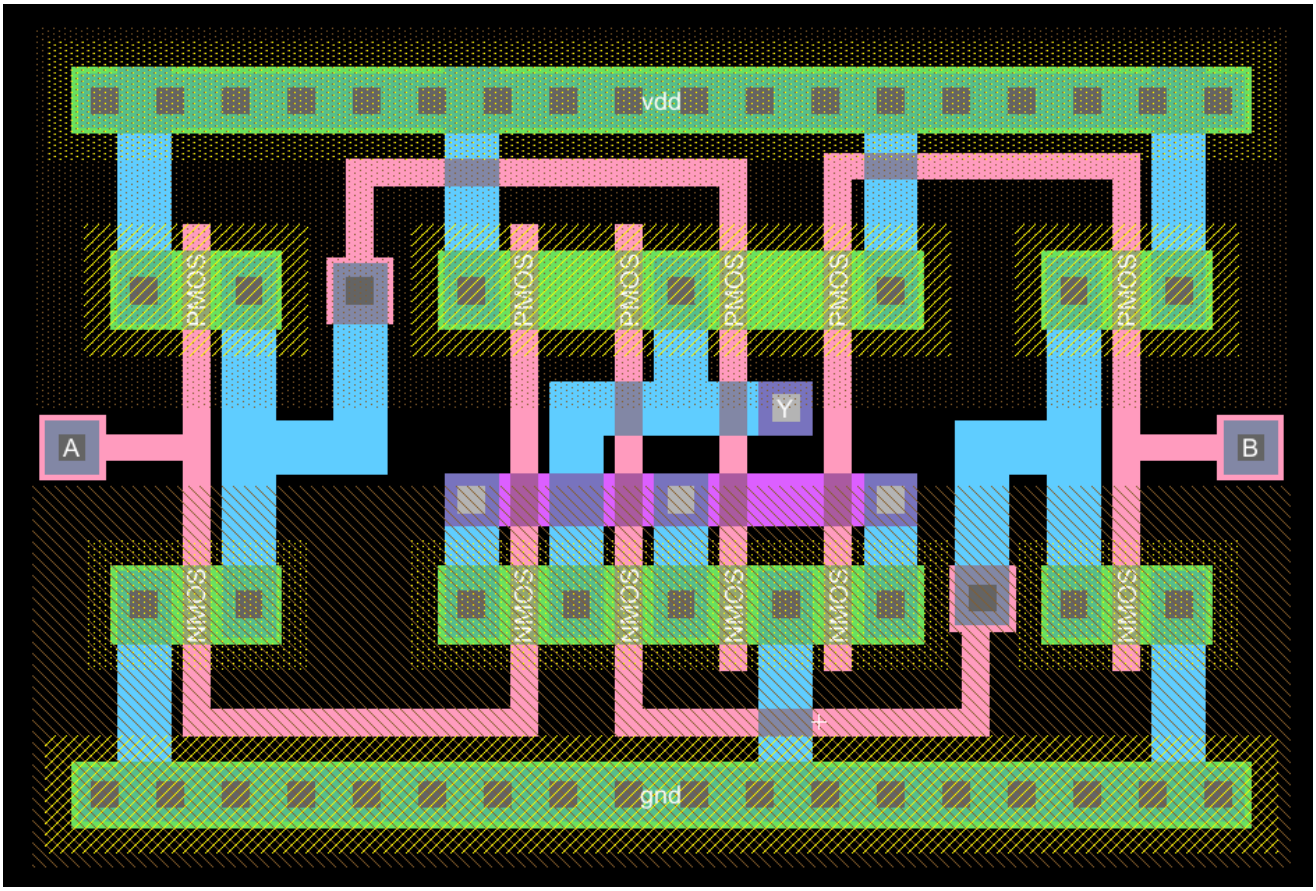

Figure 3.2: Layout of XOR Gate

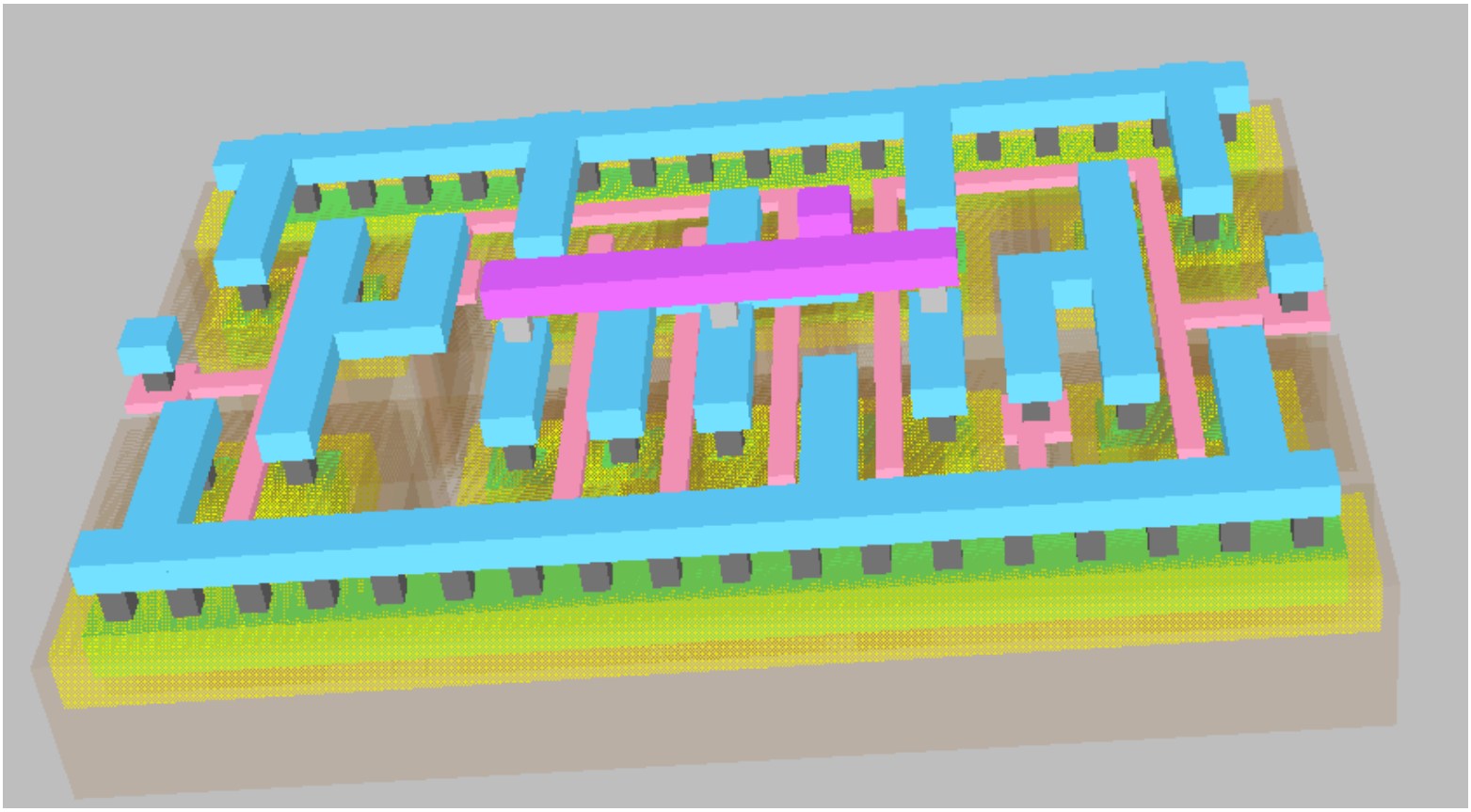

Figure 3.3: 3D View of XOR Gate Layout

- Below is the transition delay simulation of the 2-input XOR gate. We are driving 5V DC to one of the input terminals, which is not shown here.
    - We see that the moment ‘d_in’ starts to rise from 0V to 5V, ‘xor_d_out’ starts to drop from 5V to 0V, as expected. The transition time of ‘d_out’ to drop from 5V to 0V for our design is roughly 1 ns.

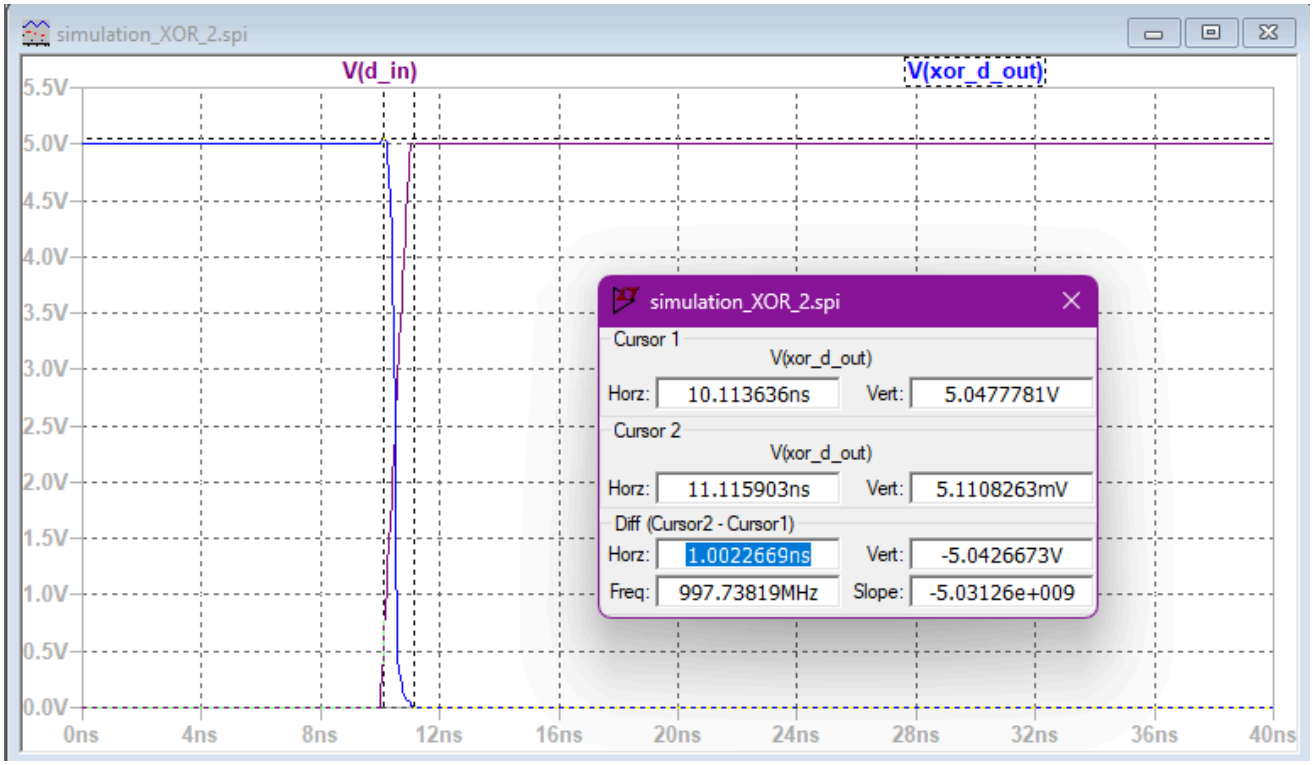

Figure 3.4: Simulation of XOR Gate

Table 3.1 displays the truth table of a 2-input XOR gate. The XOR gate functionality is where the output is dependent exclusively on one input being high.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 3.1: XOR Gate Truth Table

- Figure 3.5 validates the functionality of our XOR gate through simulation. The simulation of the XOR gate matches the truth table above.

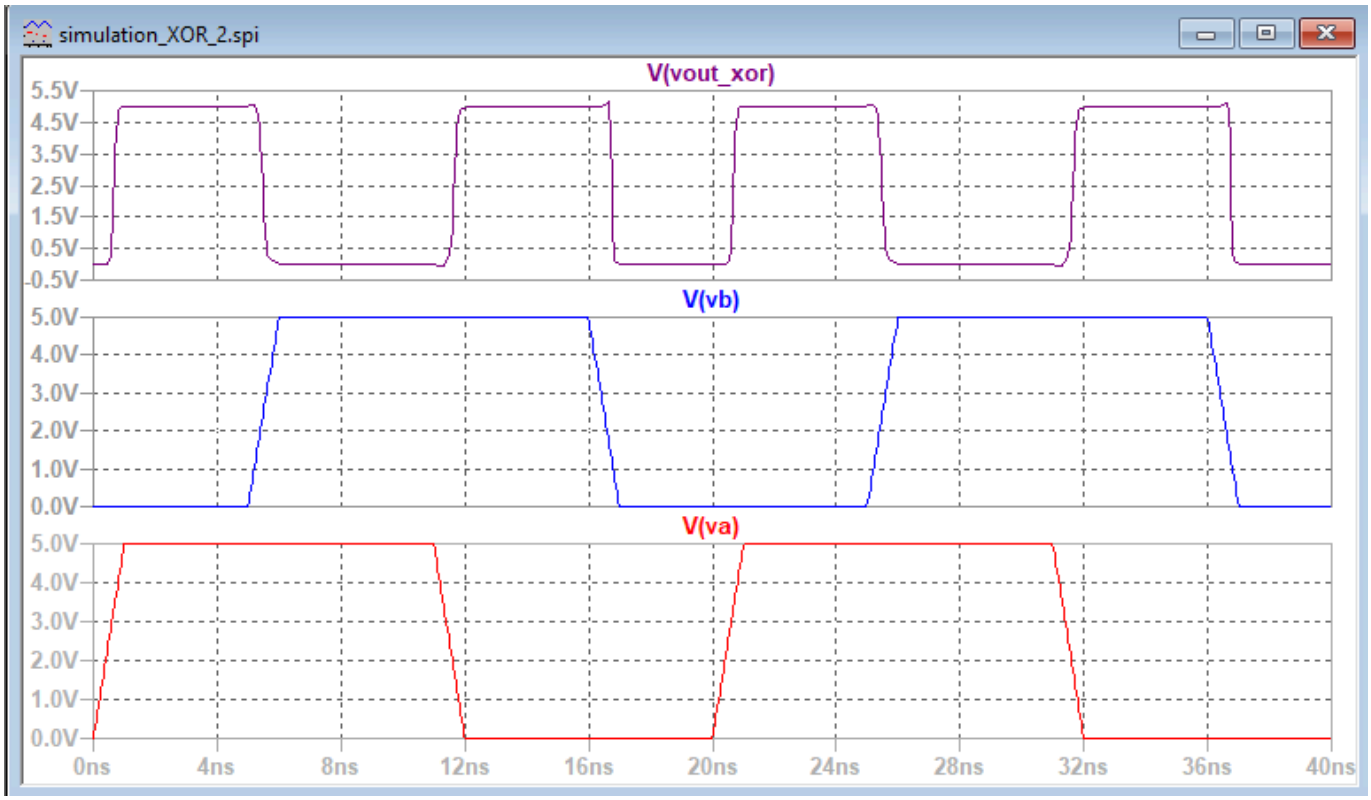

Figure 3.5: 2-Input XOR Gate Truth Table Simulation

DRC & LVS NCC Check for XOR Gate

```
================================1716================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 6 networks
Checking cell 'simulation_XOR_2{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.017 secs)
================================1717================================
Hierarchical NCC every cell in the design: cell 'simulation_XOR_2{sch}'  cell 'simulation_XOR_2{lay}'
Comparing: lab_5_full_adder:XOR_2{sch} with: lab_5_full_adder:XOR_2{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Comparing: lab_5_full_adder:simulation_XOR_2{sch} with: lab_5_full_adder:simulation_XOR_2{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.006 seconds.
```

Now it's time to create our full-adder using the gates we just made.
To reduce the number of gates, I will use two half-adders, cascading the output of one half-adder to the input of the other, to create a full-adder. A half-adder is designed with an XOR and a NAND gate.

- Below are the schematic, icon, and layout views of the full adder.

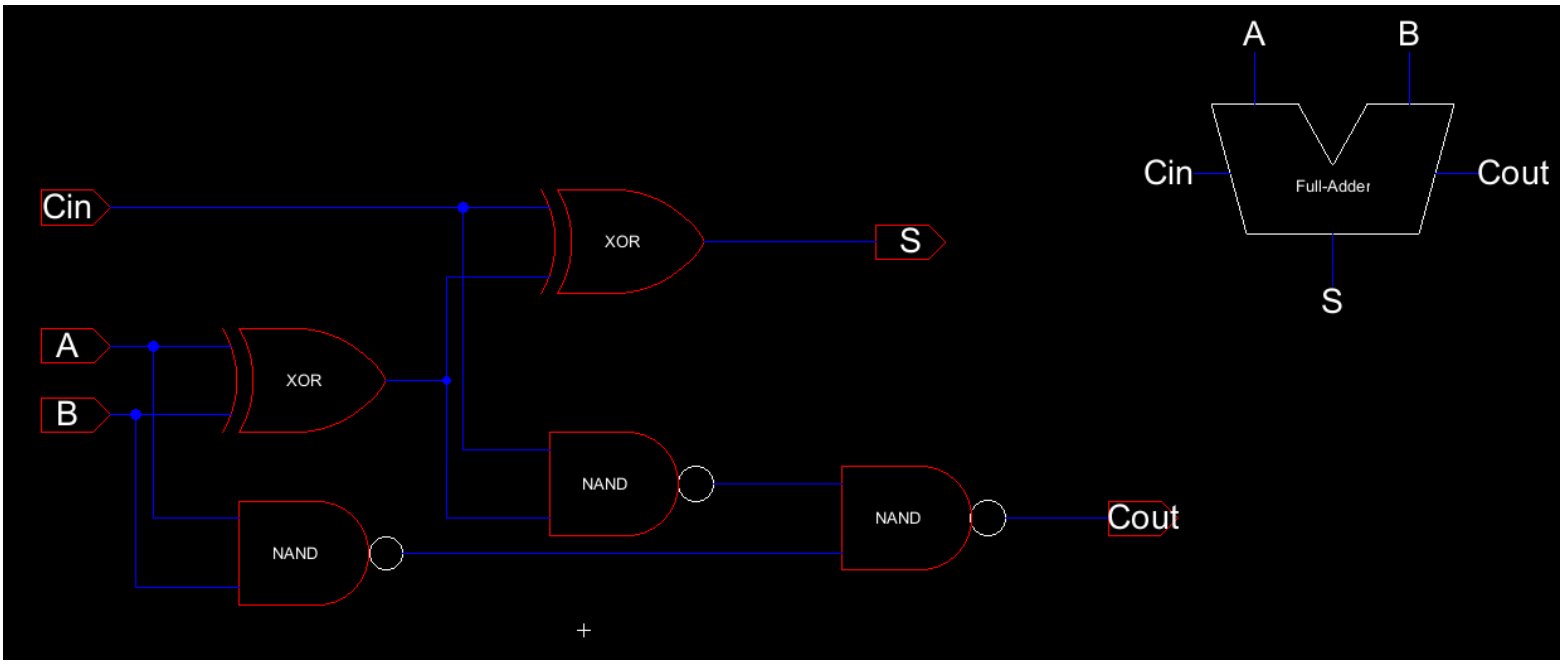

Figure 4.1: Schematic and Icon of Full-Adder

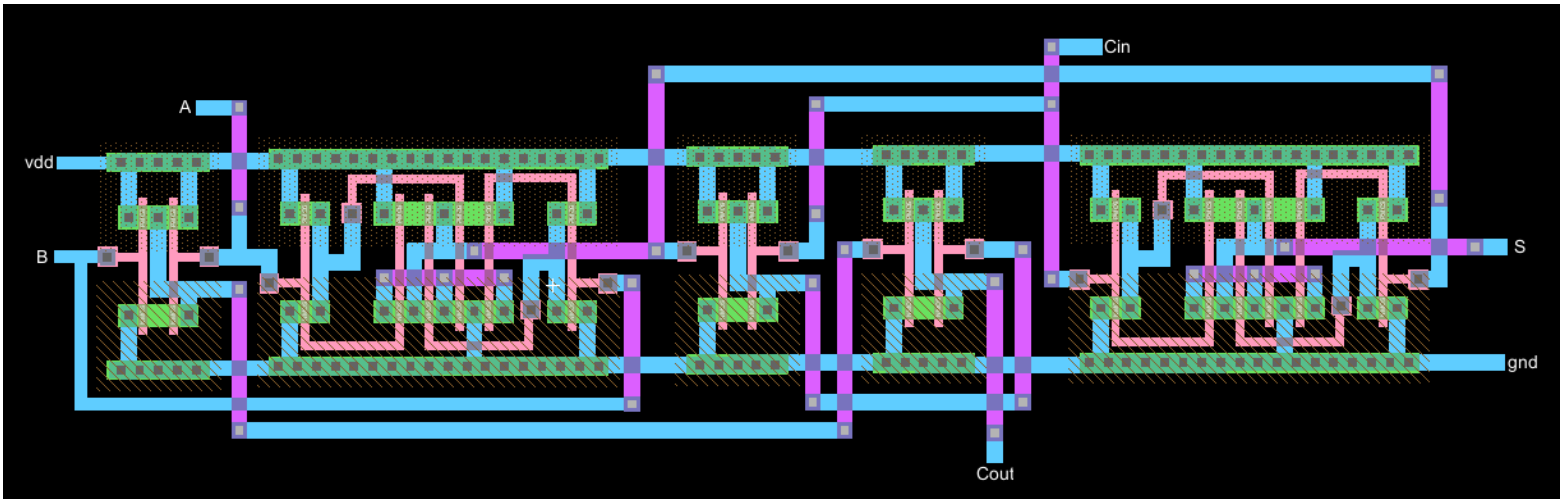

Figure 4.2: Layout of Full-Adder

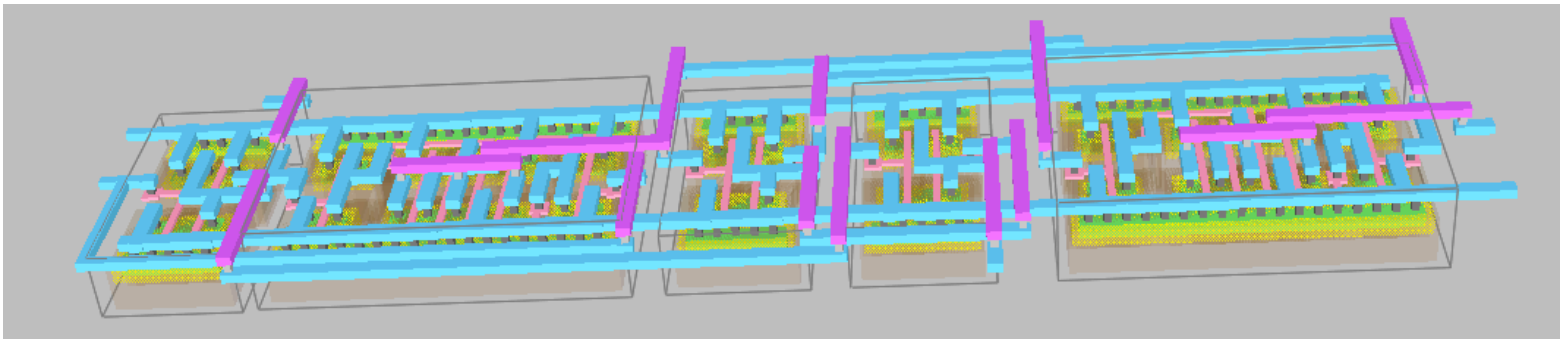

Figure 4.3: 3D View of Full-Adder Layout

Table 4.1 displays the truth table of a full-adder. A full-adder's functionality is to add three single-bit binary numbers–two operand bits and a carry-bit from a previous stage–and produce a sum bit and a carry-out bit

A	**B**	**C_{in}**	**S**	**C_{out}**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4.1: Full-Adder Truth Table

- Below is the simulation of a full-adder; we can analyze the functionality of the full-adder with the simulation. The simulation of the full-adder matches the truth table above.

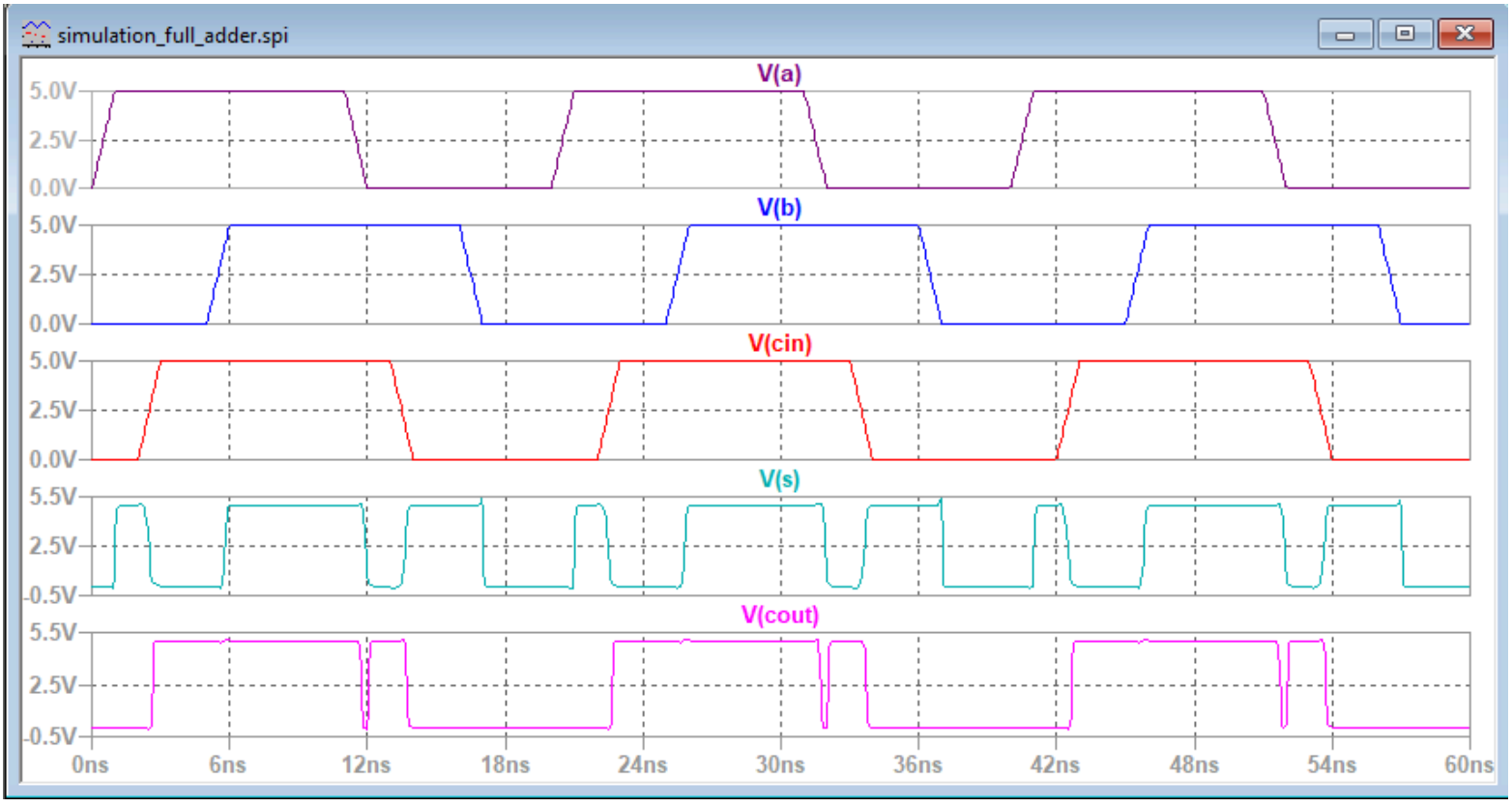

Figure 4.4: Full-Adder Truth Table Simulation

DRC & LVS NCC Check for Full-Adder

```
================================3614================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 8 networks
Checking cell 'full_adder{lay}'
        No errors/warnings found
Checking cell 'simulation_full_adder{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.043 secs)
================================3615================================
Hierarchical NCC every cell in the design: cell 'simulation_full_adder{sch}'  cell 'simulation_full_adder{lay}'
Comparing: lab_5_full_adder:NAND_2{sch} with: lab_5_full_adder:NAND_2{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: lab_5_full_adder:XOR_2{sch} with: lab_5_full_adder:XOR_2{lay}
  exports match, topologies match, sizes not checked in 0.004 seconds.
Comparing: lab_5_full_adder:full_adder{sch} with: lab_5_full_adder:full_adder{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: lab_5_full_adder:simulation_full_adder{sch} with: lab_5_full_adder:simulation_full_adder{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.011 seconds.
```