

# **Lab 2 Report**

## **Padframe DAC**

By Ogbonnaya Okorie

# Goal

Layout a padframe of 8 pins and connect a 5-bit DAC to the padframe. One pin will be left unused.

## Procedure

These are cells that we will be baselining the padframe DAC with. The “pad” cell as shown in figure 2.1 will be converted into a padframe array, in which we’ll connect the inout pins to the “dac” cell connections.

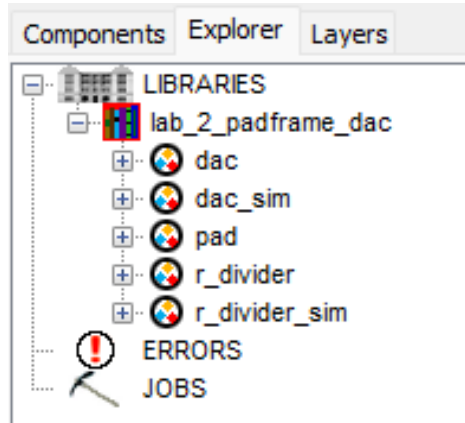


Figure 1.1: Padframe Library Baseline

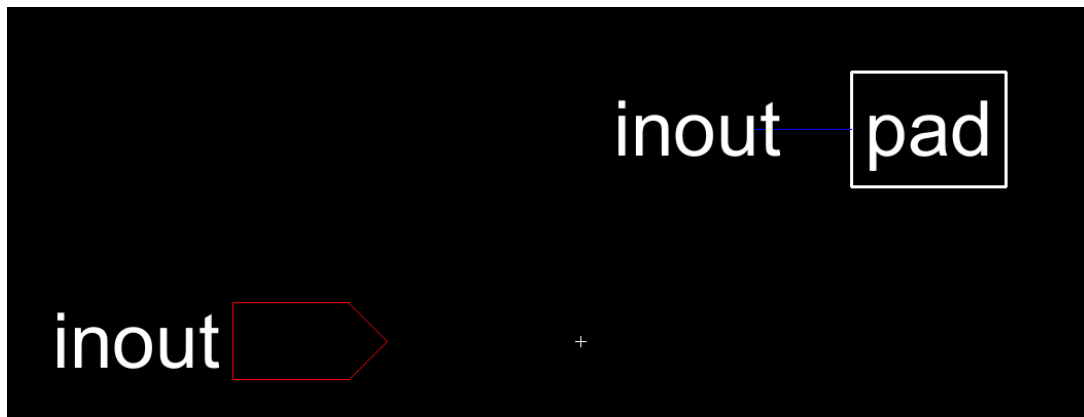


Figure 2.1: Pad Cell Schematic and Icon

- Below is the layout of the and 3D view of the “pad” cell that will be turned into an array for the padframe.

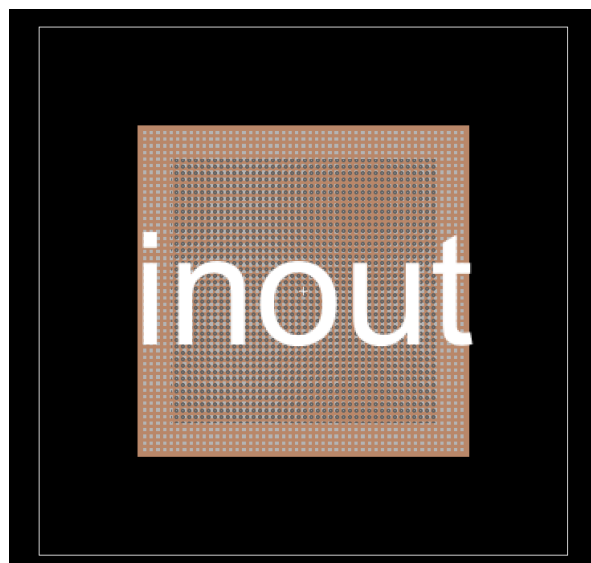


Figure 2.2: Pad Cell Layout

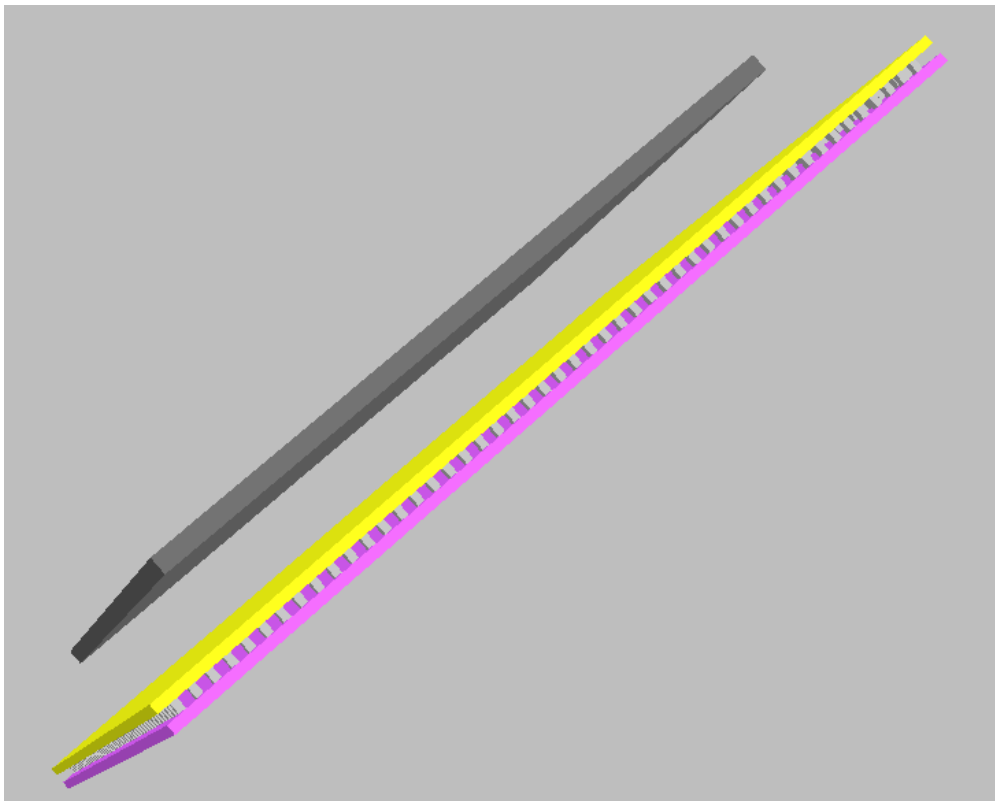


Figure 2.3: 3D View of Pad Layout

- Below is the schematic of the 5-bit DAC that will be connected to the padframe.

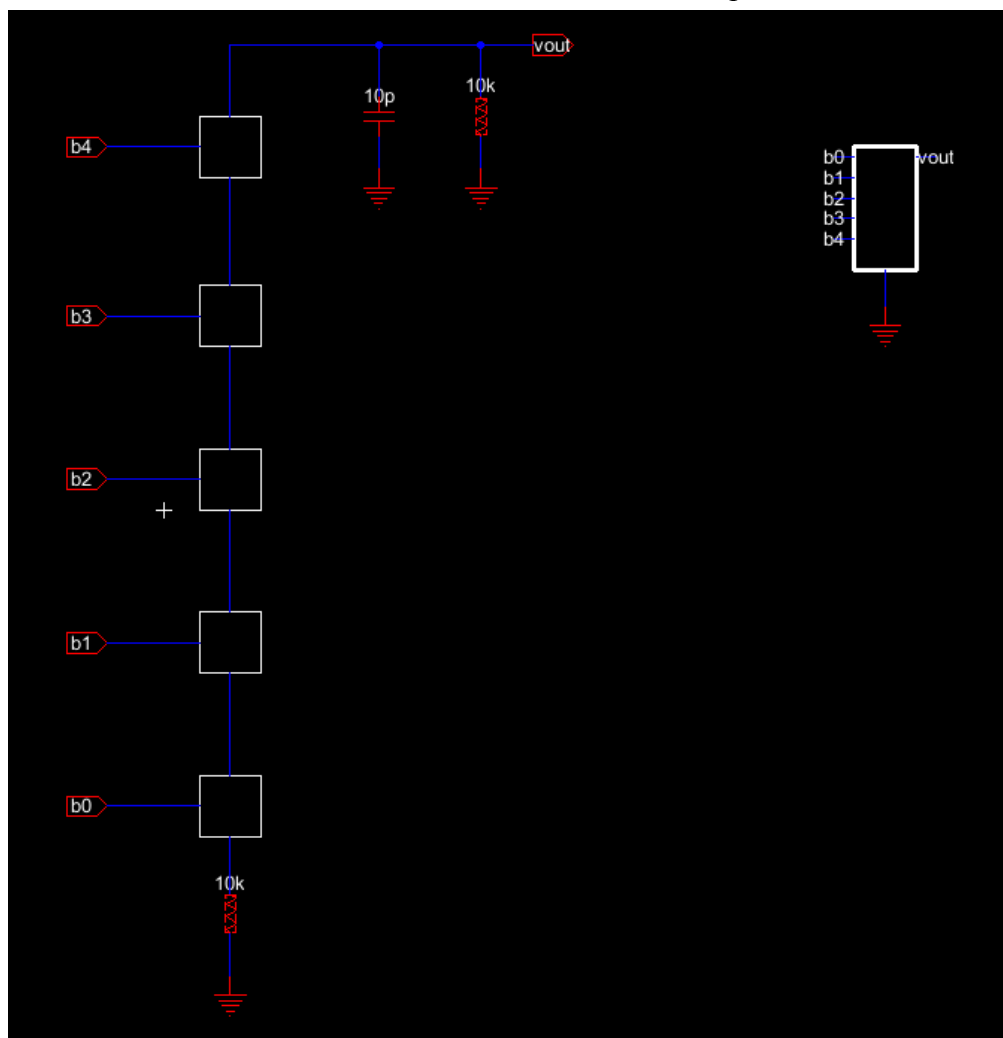


Figure 3.1: 5-bit DAC Schematic & Icon

- Below is the layout and 3D view of the 5-bit DAC. I included some spice code to confirm 5-bit DAC functionality, as shown in the simulation in Figure 3.3.

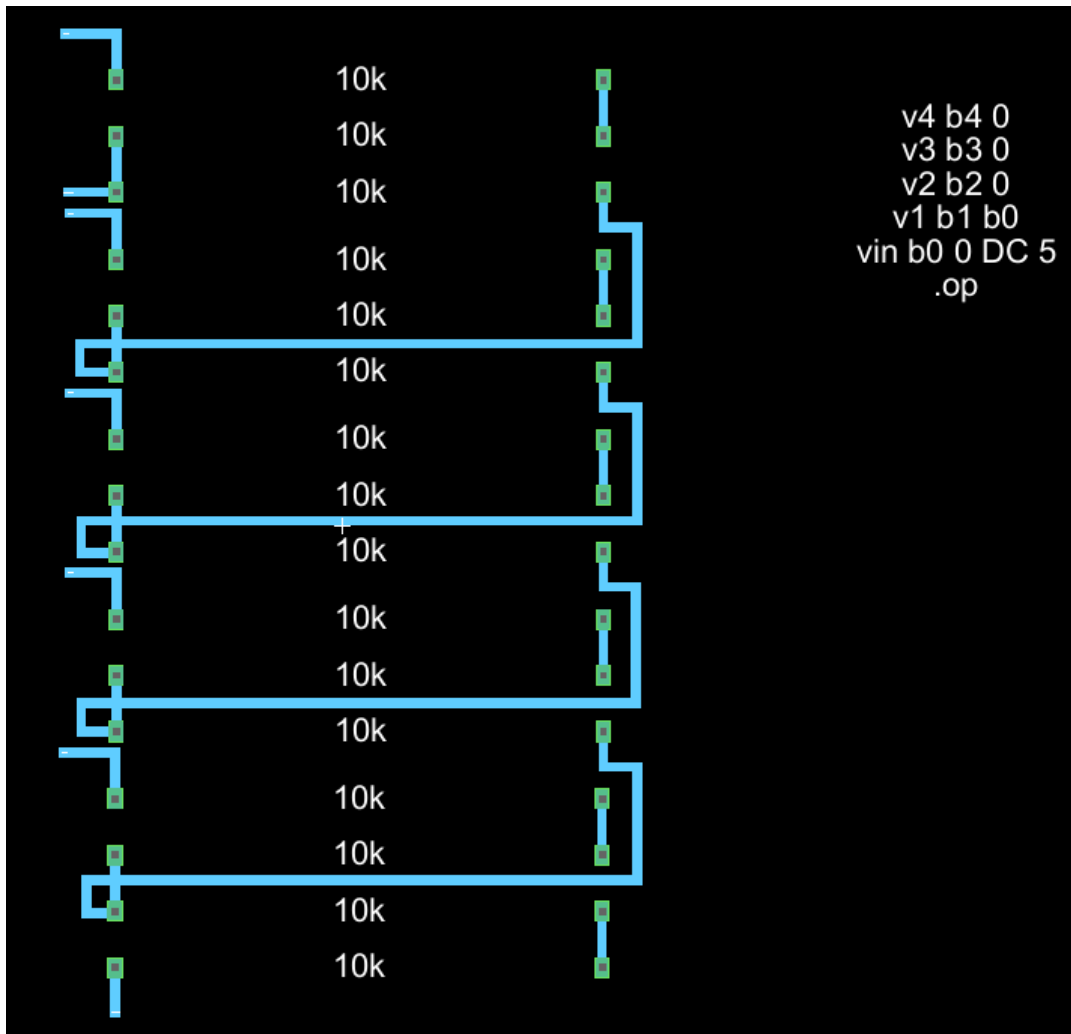


Figure 3.2: Layout of 5-bit DAC + Spice Code

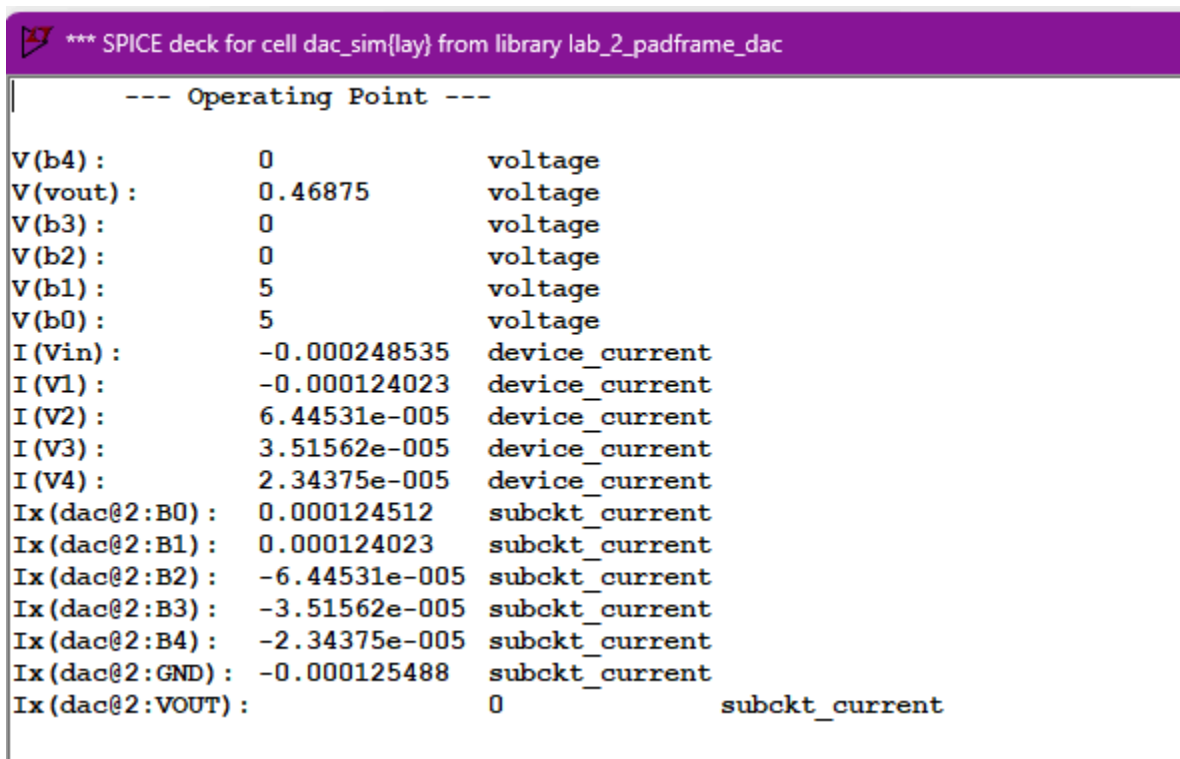


Figure 3.3: Simulation of 5-bit DAC

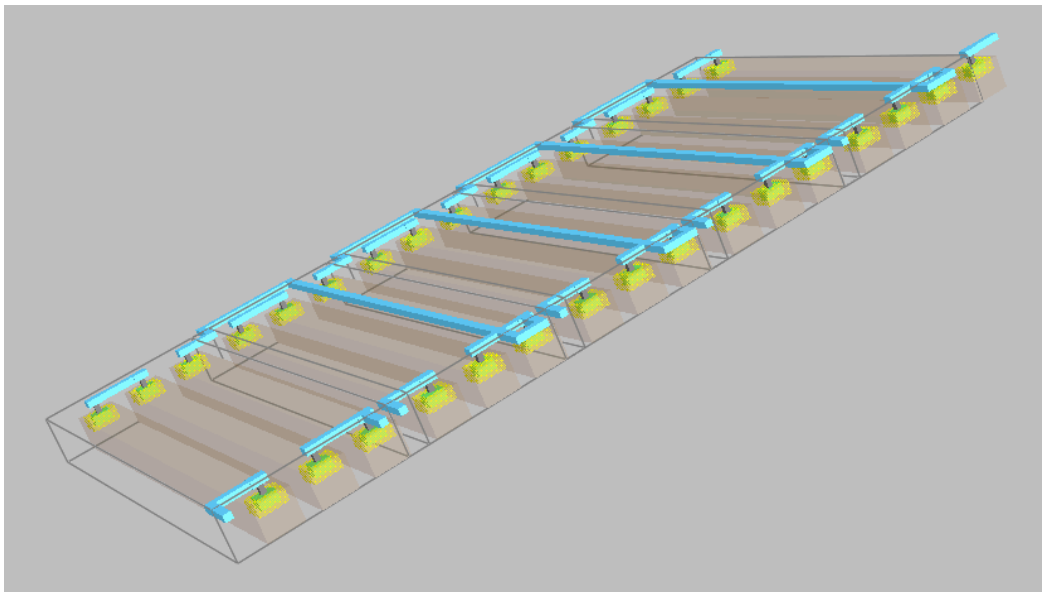


Figure 3.4: 3D View of 5-bit DAC Layout

Now that I know that I was able to successfully copy the 5-bit DAC design successfully and confirmed functionality, I will proceed on to designing the 5-bit padframe.

- Below is the view of the schematic and icon view of the padframe.

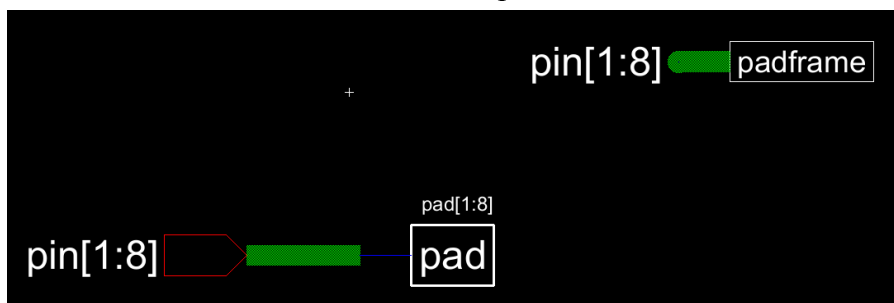


Figure 4.1: Padframe Schematic and Icon View

- Below is the layout and 3D view of the padframe with its 8 pins. The layout was created by making a 4x4 array of the “pad” cell and cutting the corners to get the 8 pins.

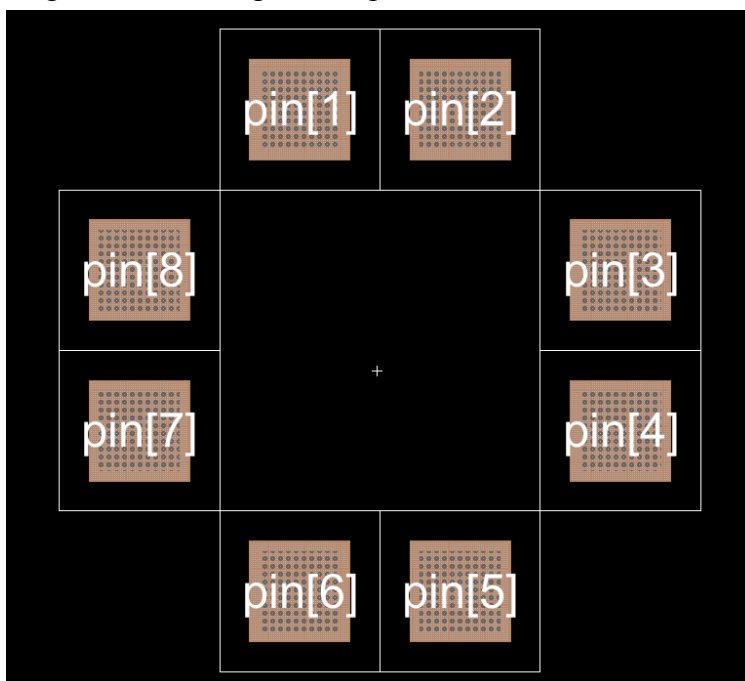


Figure 4.2: Padframe Layout

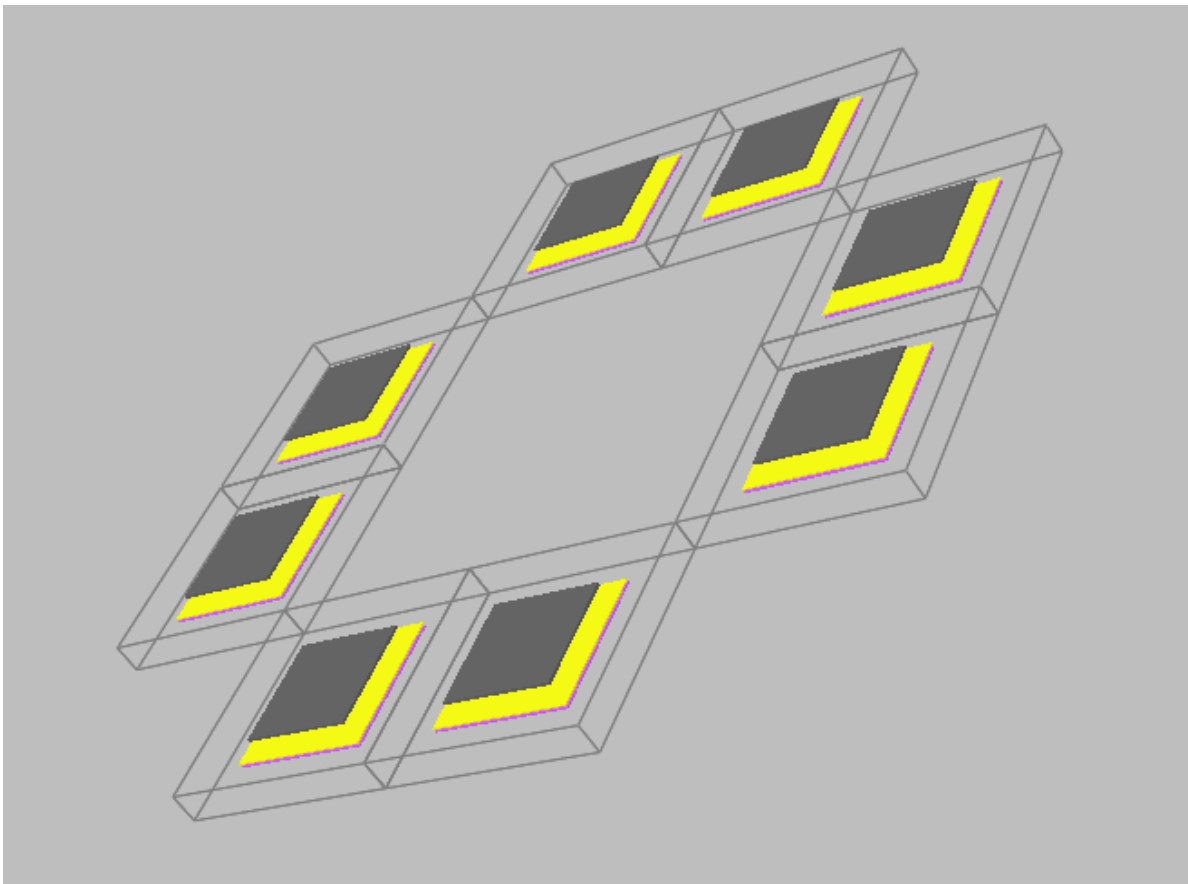


Figure 4.3: 3D View of Padframe

Now that we have the padframe layout, we can integrate the 5-bit DAC into the padframe and connect the DAC I/Os to the padframe pins.

- Below is the schematic and icon view of the DAC IC.
  - The pinout table and reasoning for selecting specific I/O pins will be explained in the next page.

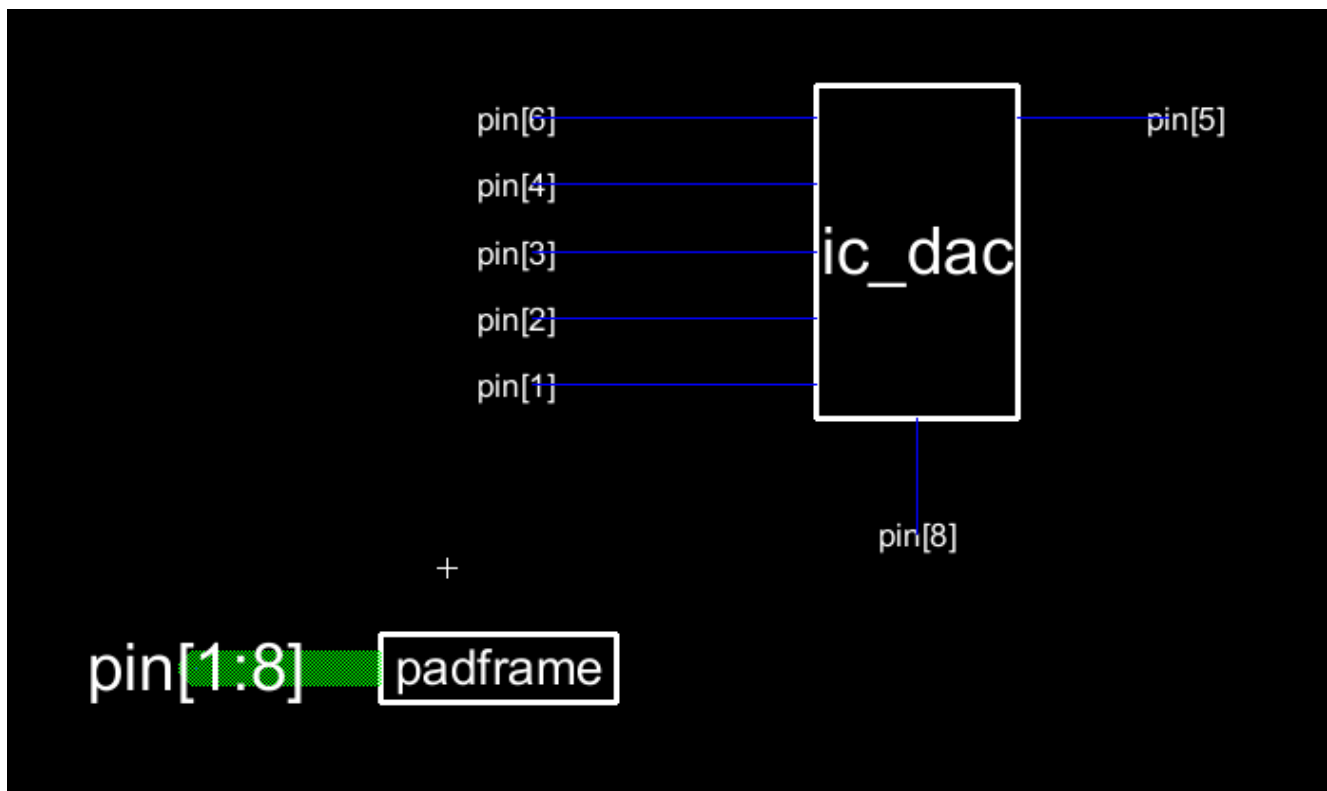


Figure 5.1: DAC IC Schematic and Icon View

- Here is the unconnected layout of the 5-bit DAC IC, just to get an idea of how it is before connecting the DAC to the padframe.
  - The 5-bit DAC is the blue layout in the middle of the image, surrounded by the padframe.

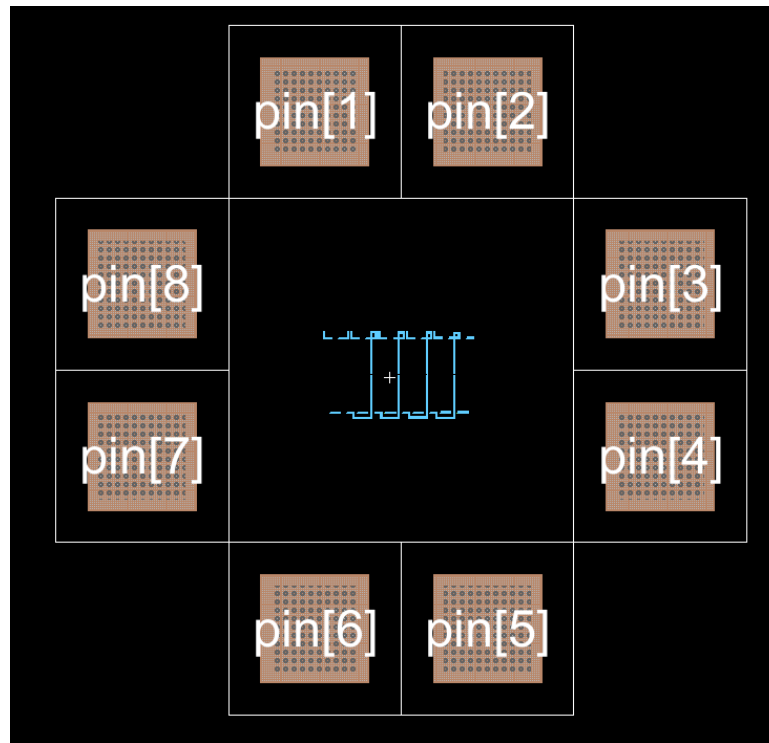


Figure 5.2: Layout of Unconnected Padframe DAC

- Recalling the DAC IC icon view in Figure 5.1, we have an *odd* way of selecting the DAC I/O to the pins, and that is because of how the 5-bit DAC is layed out.
  - Looking at the DAC left to right, the I/Os go from: gnd -> b0 -> b1 -> b2 -> b3 ->  $V_{out}$  -> b4.
  - We can't overlap nets or else we will get DRC errors, so we connect the DAC to the padframe as follows.

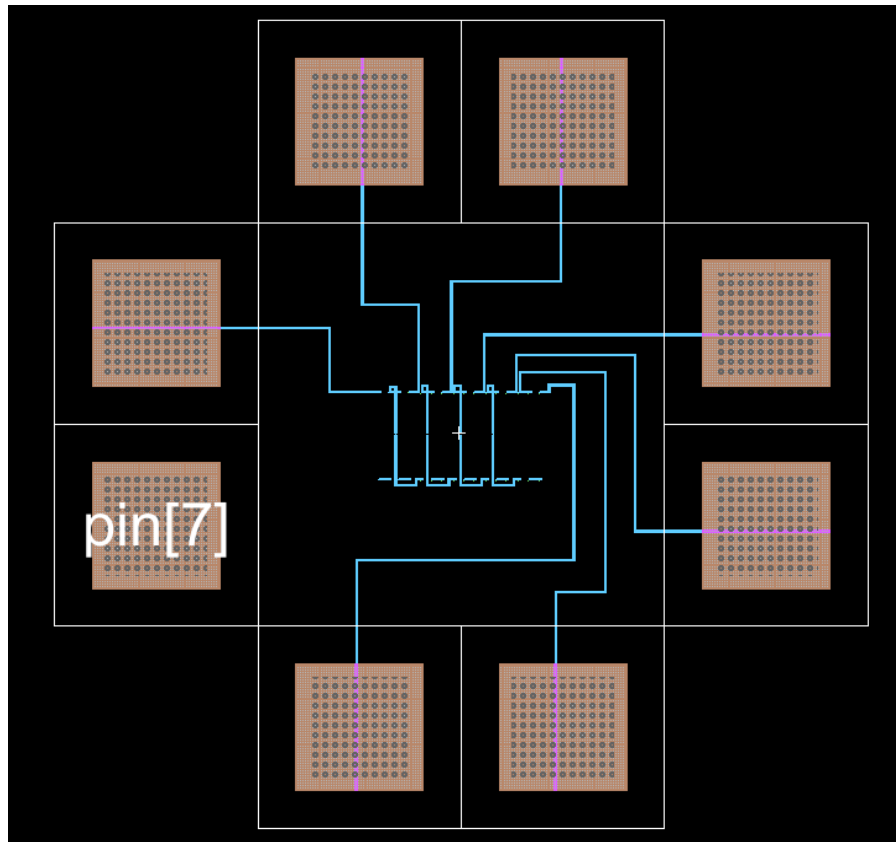


Figure 5.3: Layout of 5-bit DAC IC

- Below is the table of the connections of the 5-bit DAC relative to the padframe

5-bit DAC I/O	Padframe Pins
b4	pin[6]
b3	pin[4]
b2	pin[3]
b1	pin[2]
b0	pin[1]
gnd	pin[8]
V <sub>out</sub>	pin[5]

*Note: pin[7] in the padframe is unused*

Table 5.1: DAC IC Pin Connections

- Below is a 3D view of the 5-bit DAC IC

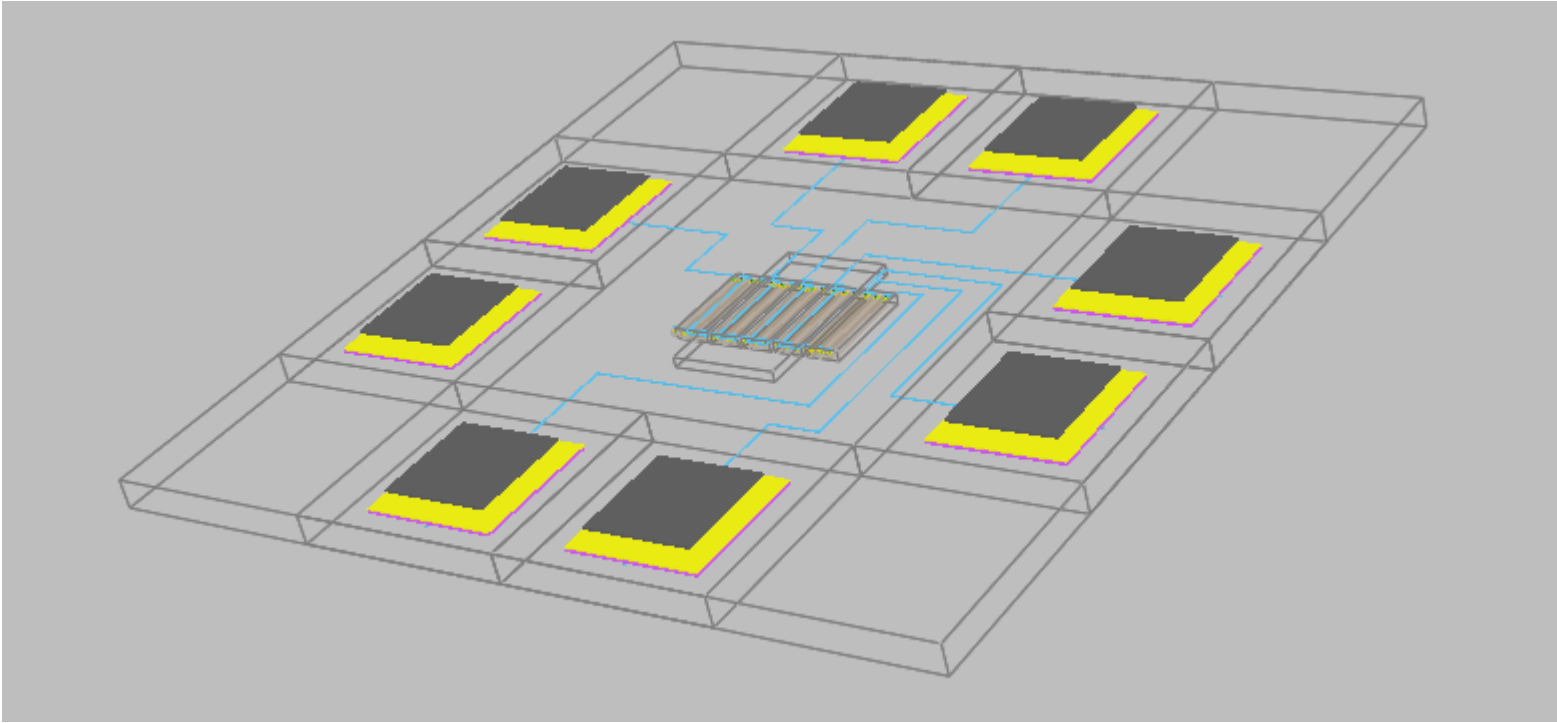


Figure 5.4: 3D View of 5-bit DAC IC



## DRC and LVS Check

```
Checking schematic cell 'pad{sch}'  
  No errors found  
Checking schematic cell 'padframe{sch}'  
  No errors found  
Checking schematic cell 'ic_dac{sch}'  
  No errors found  
Checking icon cell 'pad{ic}'  
  No errors found  
Checking icon cell 'padframe{ic}'  
  No errors found  
Checking icon cell 'ic_dac{ic}'  
  No errors found  
0 errors and 0 warnings found (took 0.0 secs)
```

Figure 6.1: Error Check on DAC IC Schematic

```
Running DRC with area bit on, extension bit on, Mosis bit  
Checking again hierarchy .... (0.0 secs)  
Found 9 networks  
0 errors and 0 warnings found (took 0.002 secs)
```

Figure 6.2: DRC Check on DAC IC Layout

```
Hierarchical NCC every cell in the design: cell 'ic_dac{sch}' cell 'ic_dac{lay}'  
Comparing: lab_2_padframe_dac:pad{sch} with: lab_2_padframe_dac:pad{lay}  
  exports match, topologies match, sizes not checked in 0.002 seconds.  
Comparing: lab_2_padframe_dac:padframe{sch} with: lab_2_padframe_dac:padframe{lay}  
  exports match, topologies match, sizes not checked in 0.003 seconds.  
Comparing: lab_2_padframe_dac:ic_dac{sch} with: lab_2_padframe_dac:ic_dac{lay}  
  exports match, topologies match, sizes not checked in 0.001 seconds.  
Summary for all cells: exports match, topologies match, sizes not checked  
NCC command completed in: 0.008 seconds.
```

Figure 6.3: NCC Check on DAC IC Layout