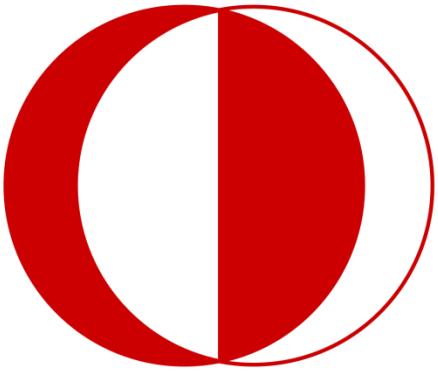

Middle East Technical University

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EE464 Hardware Project Final Report

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Introduction

In this hardware project, we are required to design an isolated DC-DC converter that includes magnetic design. We selected our topology from the given list on the hardware project page which is FOR#2. The features of this converter are given below:

- Minimum Input Voltage = 24 V
- Maximum Input Voltage = 48 V
- Output Voltage = 10 V
- Output Power = 48 W
- Output Volt. Peak-to-Peak Ripple = 2%
- Line Regulation = 2%
- Load Regulation = 2%

The reason behind this selection lies under the advantages of the Forward converter over the Flyback converter which is the other option for this project. The transformer in the Forward converter transfers energy instantly unlike Flyback converter which stores energy in the transformer's air gaps. The instant energy transfer allows us to construct a more ideal transformer with high magnetizing inductance and without an air gap. This transformer type provides much lower peak currents on both sides which lowers the copper losses. Another advantage of Forward converter is having the output inductor and freewheeling diode. These two components stabilize the output current, so the ripple of the secondary side current is smaller in Forward converter. Furthermore, since the output inductor is also the main energy storage element, output capacitor can be selected smaller and with a lower ESR value which results in lower output voltage ripples. In order to benefit from these advantages in our design, we chose to make a Forward converter in our hardware project. The overall block diagram of the project is given in Figure 1.

In this report, we present our solution approach for given project with magnetic designs, simulations including non-ideal characteristics of the converter, component selections, PCB design, efficiency and thermal analysis.

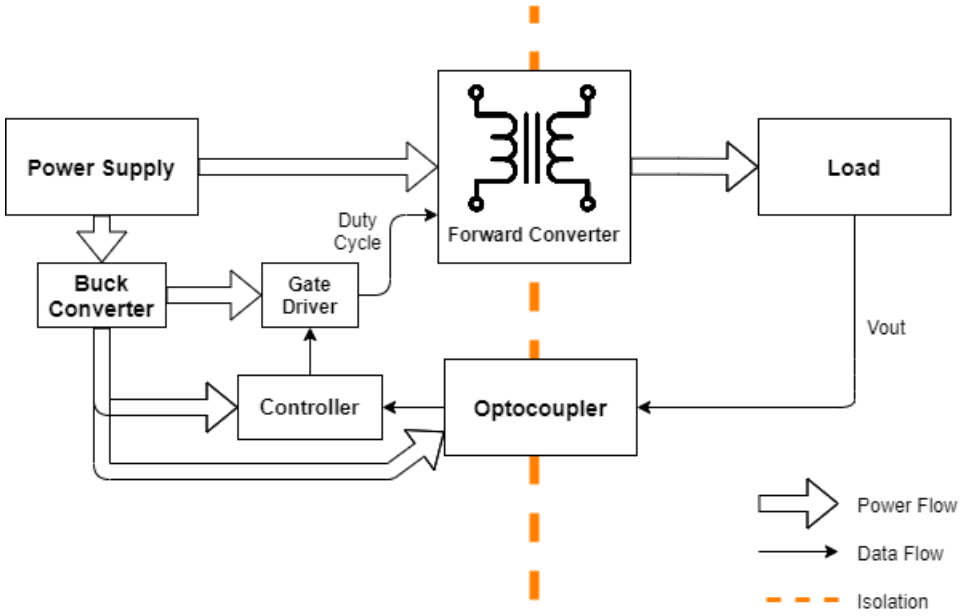


Figure 1. Overall block diagram

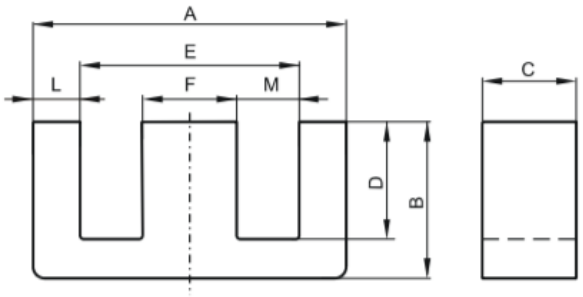
Transformer Design

In the early phases of this project we have designed a transformer according to available core list in the laboratory. Since we are not limited by these cores, we have revisited our transformer design that we completed for simulation report. In order to find a proper core, we first calculated required area product for our design according to equation (1).

$$W_a A_c = \frac{P_o * D_{cma}}{K * B_{max} * f_s} \tag{1}$$

Parameter	Description	Value
P_o	output power	48W
D_{cma}	current density	500 cir. mils/amp = 4A/mm^2
K	topology constant	0.0005
f_s	switch frequency	40 kHz
B_{max}	max flux density	1750 Gauss

According to equation (1) and above parameters, area product is calculated as 0.686. Then, we have selected 0P43009EC core whose area product is 0.74.



(mm)	Nominal:	Tol. min.:	Tol. max.:
A	30.95	-0.5	+ 0.5
B	13.1	-0.25	+ 0.25
C	9.4	-0.3	+ 0.3
D	8.5 Min.		
E	21.41 Min.		
F	9.4	-0.13	+ 0.13
L	4.29 Nom.		
M	6.0 Min.		
Eff. Parameters			
Ae mm ^{2}	Amin mm ^{2}	le mm	Ve mm ^{3}
83.2	83.2	61.9	5150

INDUCTANCE

AL value (nH/T²)	Test conditions
Nom: 3147 Min.: 2360	10 kHz, < 0.5 mT, 25 °C

MARKING

P
EC

Figure 2. Properties of 0P43009EC

We used formula (2) to find minimum number of primary winding not to saturate the core. By choosing $N_1 = N_{3(reset)}$, we limited the maximum duty ratio to 50% in order to reset the reset the transformer.

$$N_1 > \frac{V_{i,max} * D_{max}}{f_s * B_{sat} * A_e} \tag{2}$$

In equation (3), $V_{i,max} = 48V$, $D_{max} = 0.5$, $f_s = 40kHz$ and $B_{sat} = 0.3T$ and $A_e = 83.2\ \text{mm}^2$, for our core selection. For given parameters $N_1 > 24.1$, and we decided that $N_1 = 25$. As we mentioned in the previous parts, $N_1 = N_{3(reset)}$.

For a forward converter, input-output relationship is given by equation (3).

$$\frac{V_o}{V_i} = \frac{N_2}{N_1} * D \tag{3}$$

V_i=24V is the limiting input voltage since increases in V_i can be overcome by lowering duty ratio. We need V_o=10V at the output of the converter. However, since equation (3) is derived for ideal components, when we simulate the circuit considering non-idealities such as winding resistances and leakage inductance, we need to use higher number of turns for secondary winding. According to simulations setting N_2=40 turns gives good results. Hence, turns numbers of the windings are as follows, $N_1 = N_{3(reset)}$=25 turns, N_2=40 turns.

AWG-22 cable, 0.327 mm^2 cross section, is applicable for 40 kHz switching frequency. Primary winding RMS current value is $3.6A_{RMS}$. To have 4 A/mm^2 current density, 0.9 mm^2 conductor area is required. Hence, we need to parallel 3 wires and obtain 0.98 mm^2 conductor area for primary winding. Secondary RMS current is 2.22 A_{RMS} and 2 parallel AWG-22 cable results in 3.4 A/mm^2 current density. Since reset winding current is very small, we can use much thinner wire. However, to decrease copper loss, we use same AWG-22 cable for reset winding. Then, we have calculated the fill-factor of the transformer by equation (4) to check if the conductors fit in the window area of the selected core.

$$k = \frac{A_{conductor}}{A_{window}} = \frac{25 * (3 * 0.327 + 0.327) + 40 * 2 * 0.327}{102} = 0.58 \quad (4)$$

As shown above, filling factor is reasonable and selecting AWG-22 cable for reset winding is not problem.

To find magnetizing inductance of the transformer, we used inductance factor (A_L) given in the datasheet of the core. From equation (5), calculated that L_m=2mH.

$$L_m = A_L * N^2 \quad (5)$$

Mean length of the windings is calculated according to equation (6) and winding resistances are calculated form equation (7). Resistance of 1-meter AWG-22 cable is 53mΩ.

$$MLT = \left(\frac{E+F}{2}\right) * \pi = 48.4 \text{ mm} \quad (6)$$

$$R = \frac{(MLT * Turns)}{Number\ of\ parallels} * 53 \text{ m}\Omega \quad (7)$$

Calculated resistances for primary, secondary and reset windings are as follows: R_1= 21.38 mΩ, R_2= 51.3 mΩ, R_3= 64.13 mΩ. These resistances are used in simulations of the transformer.

Core manufacturer, Magnetics, provides equation (8) to calculate core loss of the transformer. Parameters in the original equation is replaced by the given values of the P type material.

$$P_{CL} = \frac{3.2 * f^{1.46} * B^{2.75} * (2.45 - 0.031 * T + 0.000165 * T^2)}{1000} * V_e = 845 \text{ mW} \quad (8)$$

Filter Inductor Design

The inductor that we have designed for the first simulation report suffers from saturation. In addition, there was significant current ripple in the inductor current. Hence, we redesigned the output inductor.

To have less than 10% inductor current ripple, 500µH inductance is required. We did not limit design with available cores in the laboratory, and we selected the cores after some iterations for Magnetics cores. Selected core is 0077258A7 and required number of turns is calculated according to equation (9).

$$N = \sqrt{\frac{L}{A_L}} \tag{9}$$

Calculating number of turns also required some iterations since inductance factor of the core changes with DC bias which is a function of turn number. At the end 88 turns is calculated to have 500µH inductance. For this turns number, A_L decreases to 65 nH/T^2, it was 121 nH/T^2 without DC bias. Since decreased 65 nH/T^2 value was used in equation (9), design iteration is competed.

As the output current is 4.8A in average, we need to use at least 1.31 mm^2 cross sectional area AWG#16 wire for inductor winding. However, we increased wire area to 2.63 mm^2 (AWG#13), since filling factor for 1.31 mm^2 was low. For AWG#13 wire choice, total area of the conductors become 231.5 mm^2 which results in k=0.54 fill-factor.

After we decided to use (AWG#13) cable, we calculated the resistance of the cable in equation (10) according to mean length per turn value of the core and resistivity of wire.

$$R = \frac{63.7\text{mm}}{\text{Turns}} * 88\ \text{Turns} * 6.57\ \ \Omega/\text{km} = 36.83\ \text{m}\Omega \tag{10}$$

For Kool Mµ-90 cores, core loss is calculated according to equation (11). In the equation below, $B_{pk} = \frac{B_{AC,max} - B_{AC,min}}{2}$. $B_{AC,max}$ and $B_{AC,min}$ values are calculated for maximum and minimum inductor currents. Equation (11) calculates 44mW core loss which is very low thanks to limited inductor current ripple.

$$P_{core} = 146.8 * {B_{pk}}^{2.022} * f^{1.334} * V_e \tag{11}$$

Simulations with Non-idealities

Simulink model built for the forward converter can be seen in Figure 3. The model includes non-idealities in the circuit, namely, voltage drop on diodes, on resistance of the MOSFET, ESR of capacitor and inductor. These are calculated or read from datasheets. Also, transformer magnetizing inductance is calculated as 2mH, and leakage inductance is added in series as 0.3mH.

Duty cycle is adjusted to achieve 10V output for input voltage limits 24V and 48V. For this range, duty cycle range is:

For Vin=24V, D=0.467

For Vin=48V, D=0.227

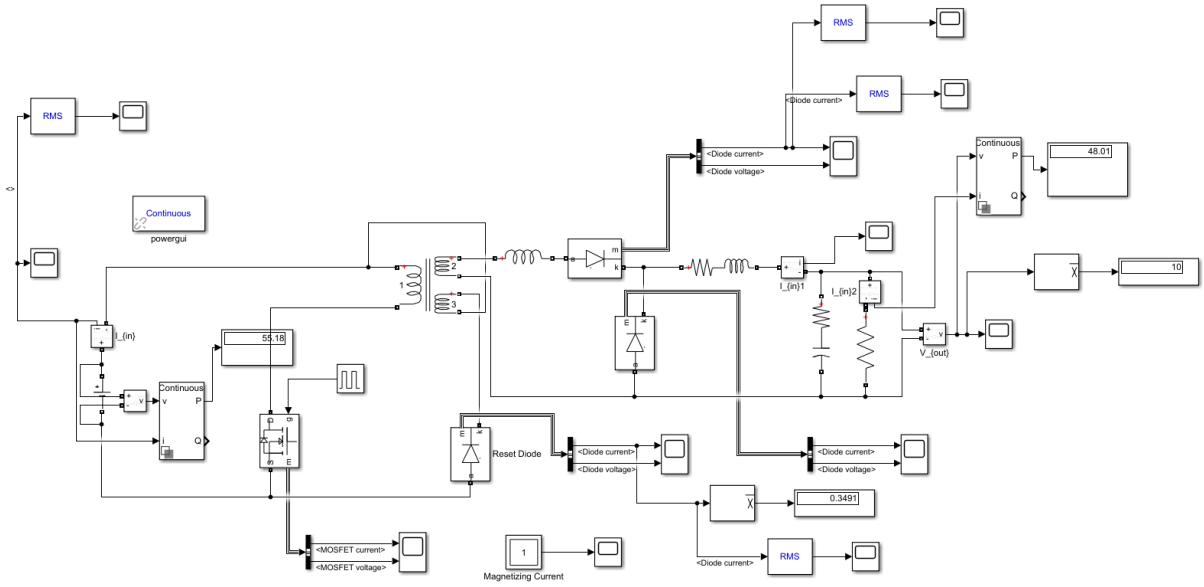


Figure 3. Simulink simulation circuit schematic

Output Voltage:

Waveforms for output voltage can be seen in Figure 4 and 5. Ripple values can be calculated from these waveforms. Peak to peak ripple as follows:

0.09/10 = 0.9% for Vin=24V

0.12/10 = 1.2% for Vin=48V

Maximum 2% peak to peak ripple requirement is therefore satisfied.

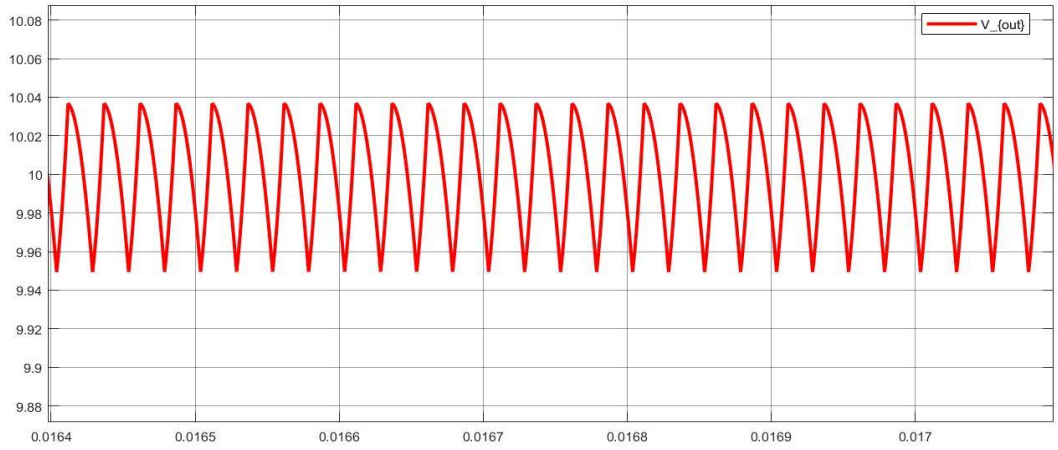


Figure 4. Output voltage waveform for Vin=24V

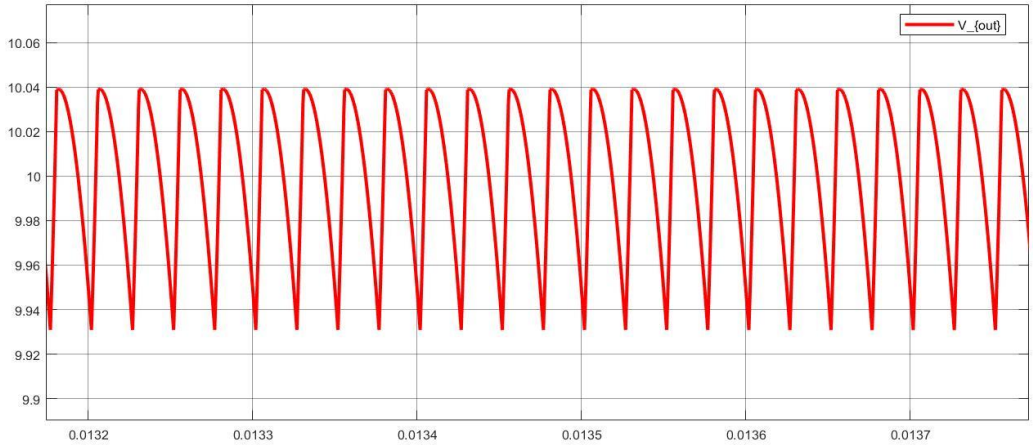


Figure 5. Output voltage waveform for Vin=48V

Inductor Current:

As shown in the Figure 6 and 7, inductor current ripple is around 10% and designed inductor provides low core loss due to low ripple.

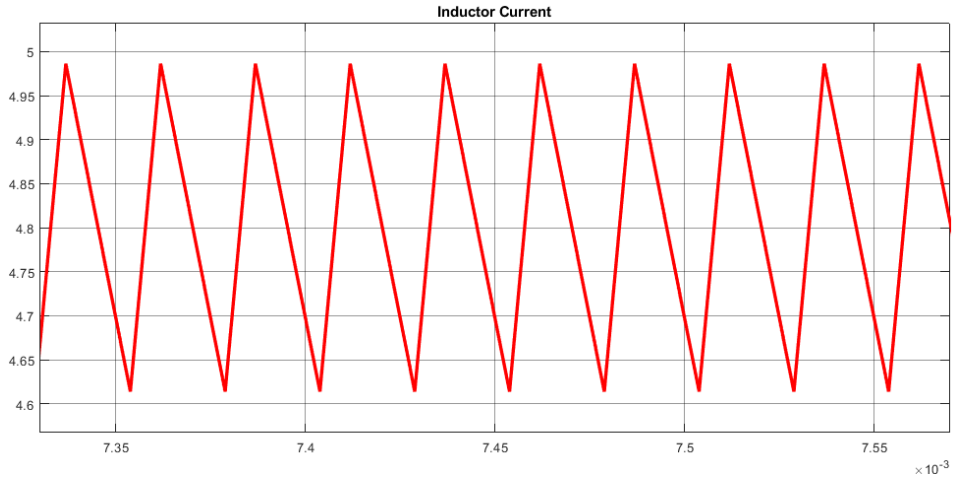


Figure 6. Inductor current waveform for Vin=24V

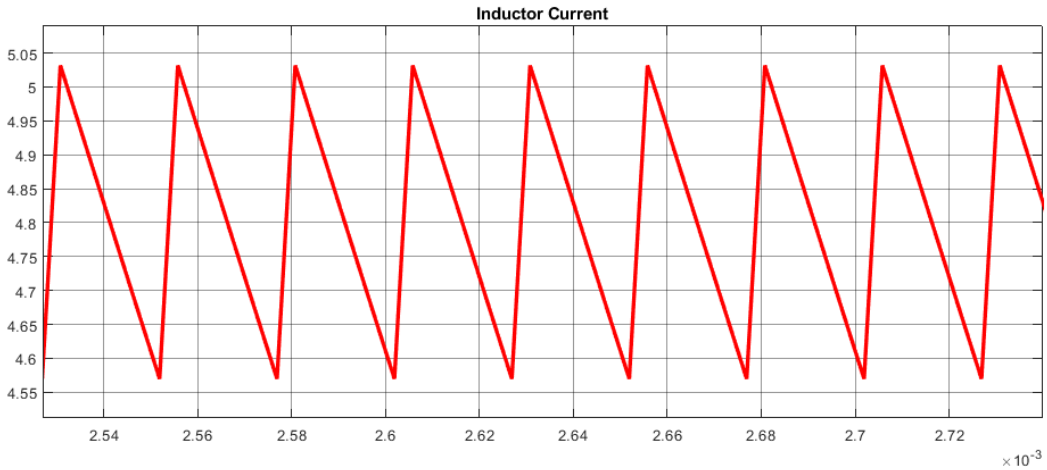


Figure 7. Inductor current waveform for Vin=48V

MOSFET Current and Voltage:

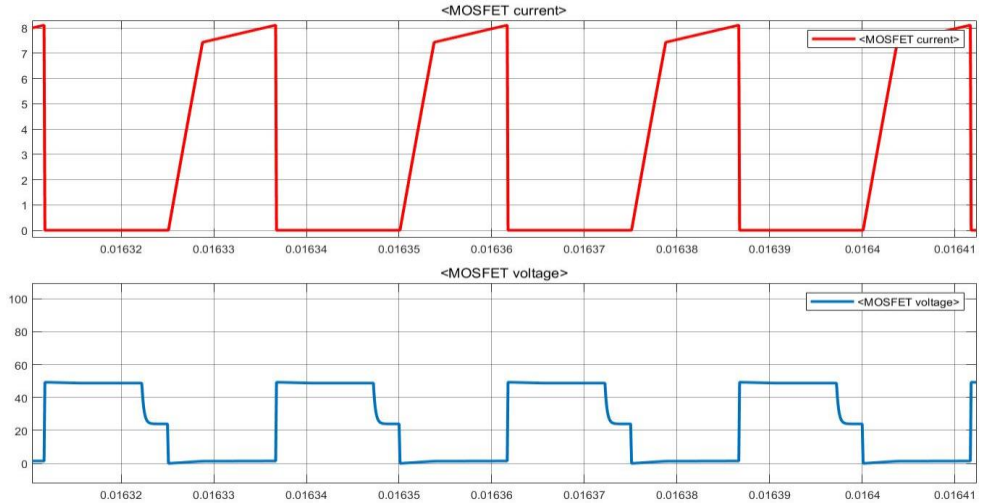


Figure 8. MOSFET Current and Voltage waveform for Vin=24V

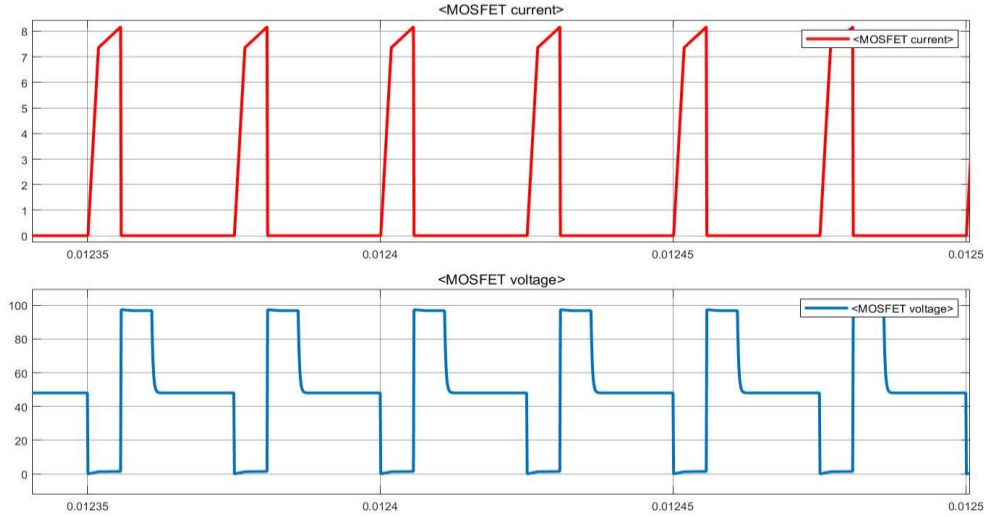


Figure 9. MOSFET Current and Voltage waveform for Vin=48V

Reset Diode Current and Voltage:

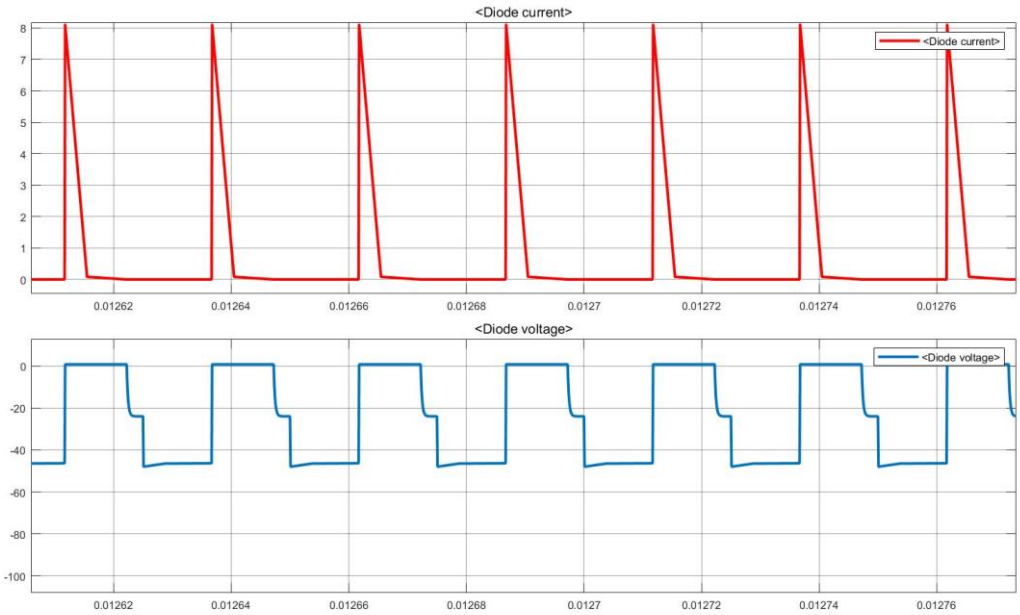


Figure 10. Reset Diode Current and Voltage waveform for Vin=24V

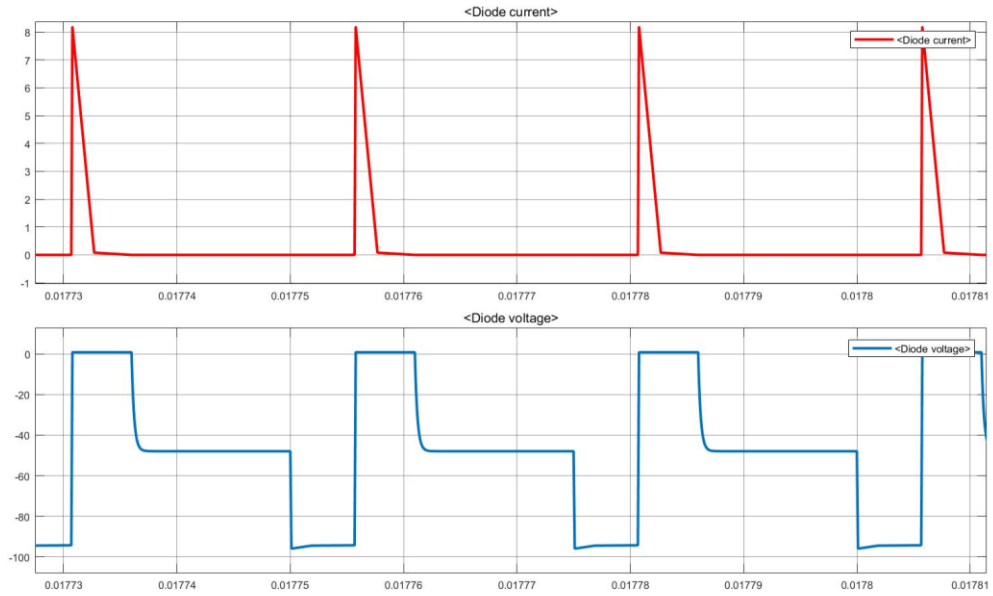


Figure 11. Reset Diode Current and Voltage waveform for Vin=48V

Secondary Diode Current and Voltage:

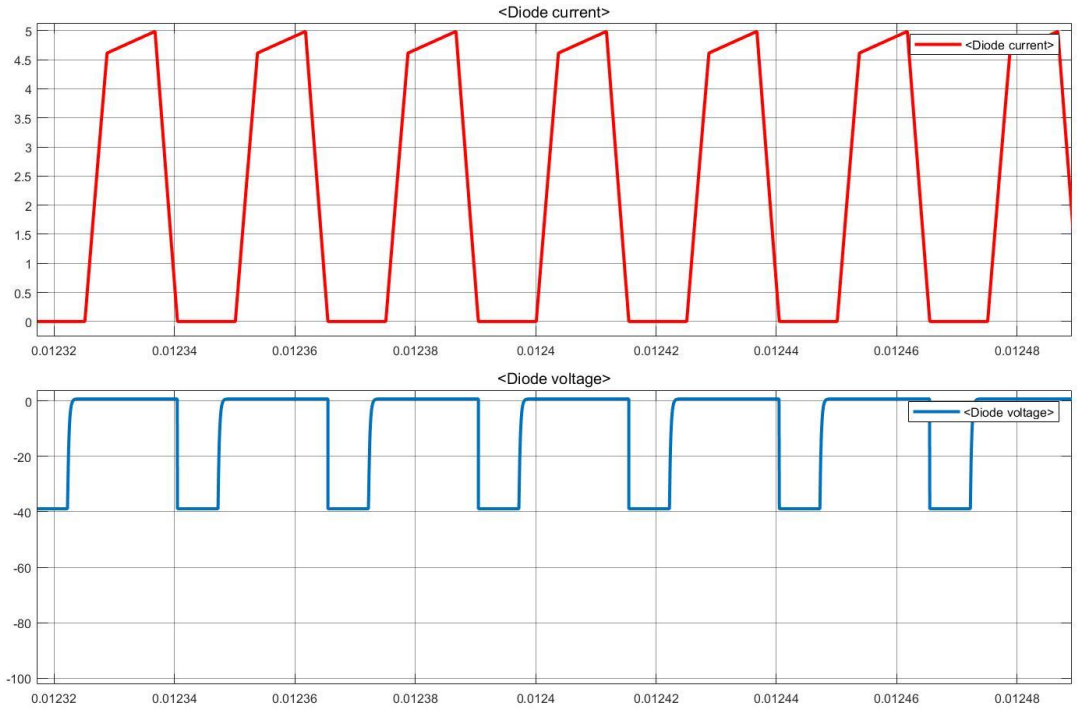


Figure 12. Secondary Diode Current and Voltage waveform for Vin=24V

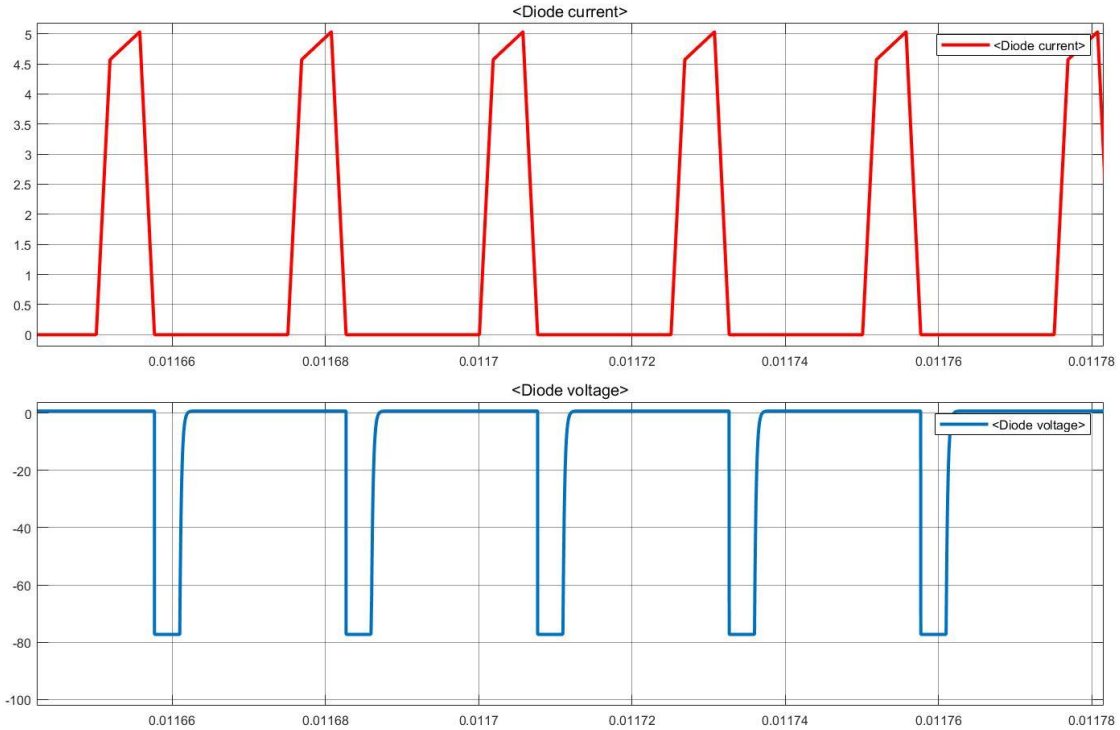


Figure 13. Secondary Diode Current and Voltage waveform for Vin=48V

Free Wheeling Diode Current and Voltage:

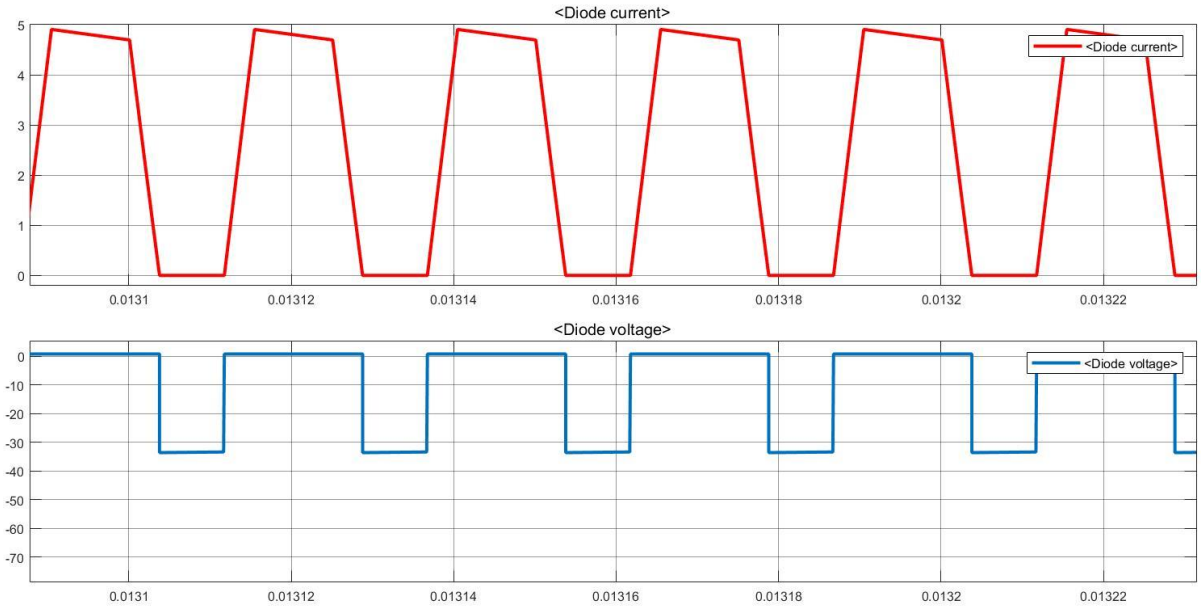


Figure 14. Free Wheeling Diode Current and Voltage waveform for Vin=24V

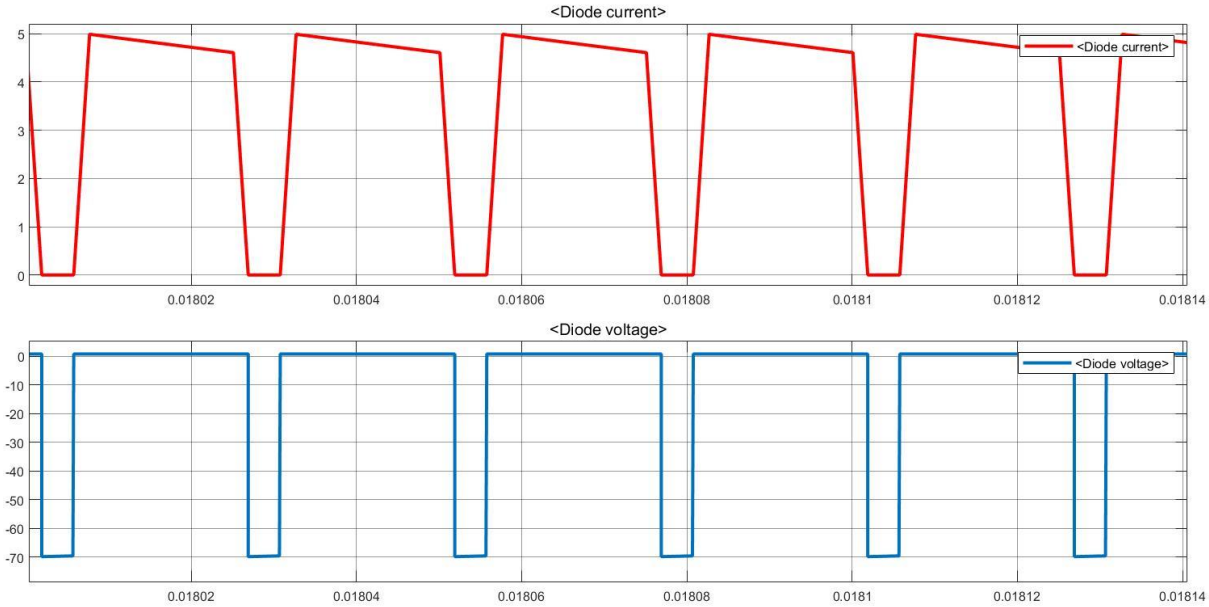


Figure 15. Free Wheeling Diode Current and Voltage waveform for Vin=48V

Component Selection

In our simulations, we tried to observe the critical limits of our components. Then we have selected components for our converter according to these limits. In general, we selected components which provides enough voltage and current margins. Provided safety margins were kept in a low level to decrease component costs.

Reset Diode:

For the primary side diode, the voltage on it is twice the input voltage which has a maximum value of 96 Volts. For the current limitations, the need is really small as indicated in Figure 10. Furthermore, since our working frequency is 40kHz, we searched for Schottky diodes that can switch fast. Our selection for the primary side diode is ***8TQ100*** which is a Schottky diode with a reverse voltage rating of 100 volts and current rating of 8 Amperes.

Secondary Diodes:

For the secondary side diodes (both secondary and freewheeling diodes), the needed voltage level is the same and around 80 volts and the current level is around 5 Amperes as indicated in Figures 13 and 15. Our selection for the secondary side diodes is ***TST20U100CC0G*** which is a diode array contains two diodes with a reverse voltage rating of 100 volts and a current rating of 10 Amperes.

Switching Device:

For the switching device, we are going to use a MOSFET which provides the needed fast switching action for our application. For the rating of the MOSFET, the maximum voltage on it is 96 Volts and the maximum current is around 8 Amperes as indicated in Figure 8. Our selection for switching device is ***IRLS640A*** which has a voltage rating of 200 Volts and a current rating of 9.8 Amperes.

Output Capacitor:

In the simulations, we observed a ripple less than 2% with a DC link capacitor of 33uF. The voltage on the capacitor is 10 Volts which is our output voltage. We searched for capacitors with low ESR value to keep the voltage ripple low and the selected capacitor is ***EEE-FT1E101AP*** which has a capacitance of 33uF and voltage rating of 25 Volts.

Buck Converter:

Maximum V_{GS} voltage of the MOSFET is 20V. To obtain gate driving voltage and to supply analog controller and optocoupler, we used D36V6F15 DC/DC voltage converter. Selected buck converter can convert 15.2-50V to 15V. Input of the converter is connected to main input of the circuit and between 24-48V. Output of the buck converter is fixed and 15V. Circuit schematic of the converter is given in Figure 16.

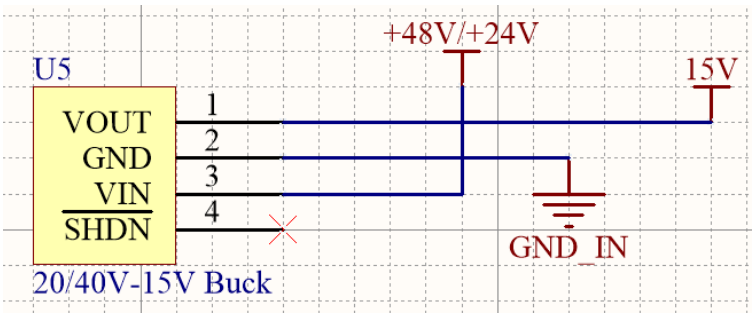


Figure 16. Circuit schematic of buck converter

Analog Optocoupler:

Since we need full isolation between input and output sides, we need to send the output voltage information to input side, where controller is placed, in an isolated way. We used TLP291 analog optocoupler to transfer voltage level to controller. Circuit schematic of the optocoupler is given in Figure 17. Depending on the output voltage level, optocoupler LED sends light to photoreceiver and voltage is read by controller. Supply voltage of the photoreceiver is taken from 15V output of buck converter IC. 15kΩ and 5kΩ resistors divides output voltage according to voltage reference of the controller.

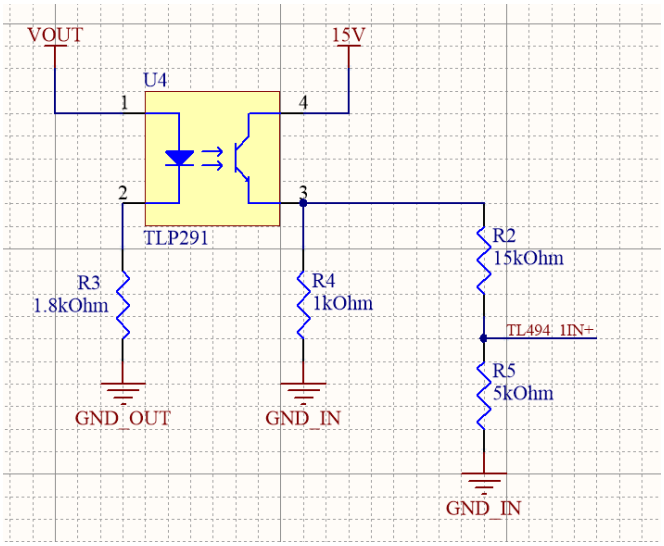


Figure 17. Circuit schematic of analog optocoupler

Gate Driver:

Analog controller cannot provide enough power to turn MOSFET on. We used ZXGD3009DY as a low side gate driver. It provides up to 40V 1A output current which is enough for our MOSFET application. Supply voltage is taken from output of the buck converter. Controller PWM output signal is connected to input of the driver and output is connected to gate of the MOSFET. Connections of the driver is given in Figure 18.

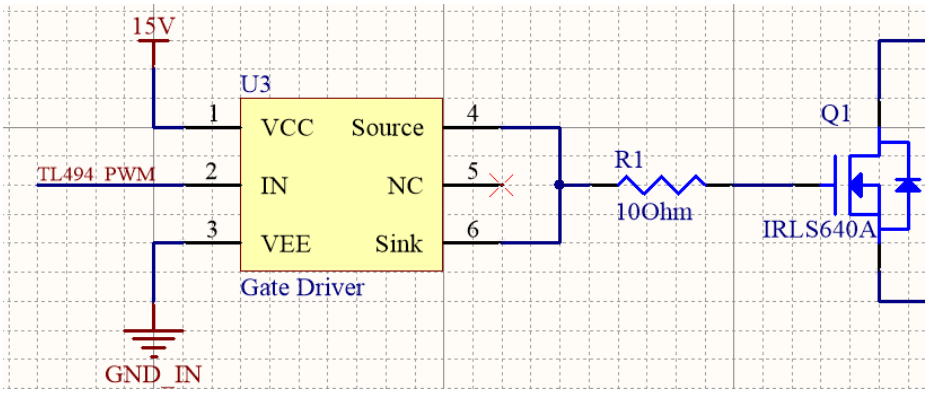


Figure 18. Circuit schematic of gate driver

Controller:

As a PWM generator and closed loop feedback control, analog controller TL494 is chosen because of its useful properties, which is listed in this part. The design is done using the datasheet of Texas Instruments as a guide. The simplified block diagram and pin layout for this controller can be seen in Figure 19 and 20.

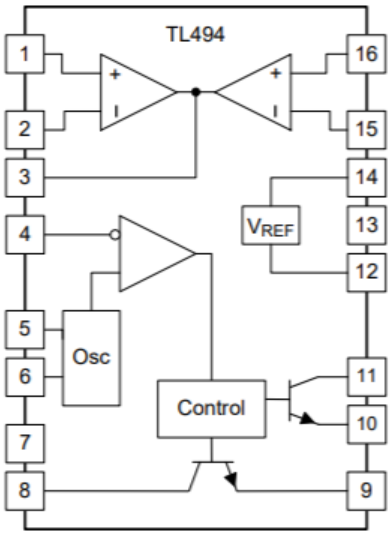
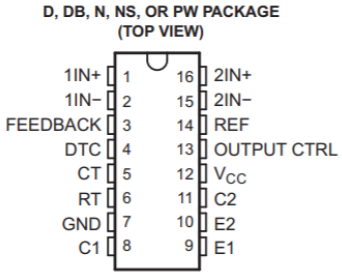


Figure 19. Simplified block diagram of TL494



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	1	I	Noninverting input to error amplifier 1
1IN-	2	I	Inverting input to error amplifier 1
2IN+	16	I	Noninverting input to error amplifier 2
2IN-	15	I	Inverting input to error amplifier 2
C1	8	O	Collector terminal of BJT output 1
C2	11	O	Collector terminal of BJT output 2
CT	5	—	Capacitor terminal used to set oscillator frequency
DTC	4	I	Dead-time control comparator input
E1	9	O	Emitter terminal of BJT output 1
E2	10	O	Emitter terminal of BJT output 2
FEEDBACK	3	I	Input pin for feedback
GND	7	—	Ground
OUTPUT CTRL	13	I	Selects single-ended/parallel output or push-pull operation
REF	14	O	5-V reference regulator output
RT	6	—	Resistor terminal used to set oscillator frequency
V_{CC}	12	—	Positive Supply

Figure 20. Pin layout of TL494 and their functions

1. Oscillator

   TL494 allows up to 300kHz oscillation frequency. We have decided to use 40kHz, which will be set with connecting a resistor and capacitor at RT and CT pins. Values of these will be selected using the following formula:

$$f_{osc} = \frac{1}{RT \times CT}$$

   RT=25kΩ
   CT=1nF

2. Closed loop feedback control

   TL494 have 2 error amplifiers, voltage and current feedback. Voltage feedback will be used in this project. Typical design of this part can be seen in Figure 21. R7/R5 ratio determines the gain, and higher gain makes the response faster and error smaller. However, it also decreases stability. Therefore, a gain of 10 will be chosen.

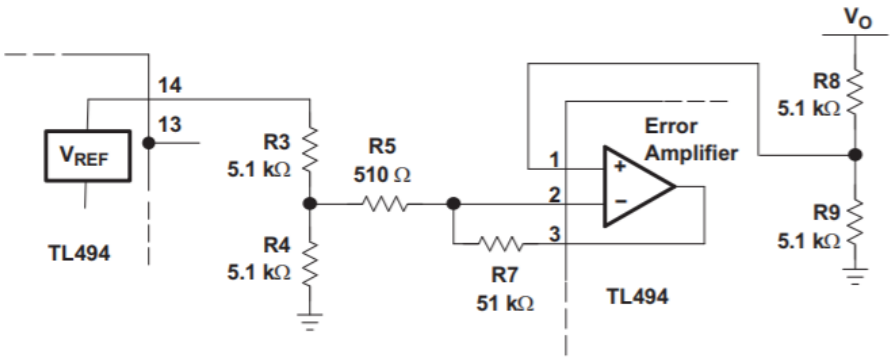


Figure 20. Error amplifier of TL494

R3=1kΩ

R4=1kΩ

R5=500Ω

R7=5kΩ

R8= 15kΩ (shown in the TL291 circuit schematic)

R9=5kΩ (shown in the TL291 circuit schematic)

3. Dead Time Control and Soft Start

TL494 allows to set a minimum dead time control, which can be used to limit duty cycle. DTC pin can be adjusted from 0 V to 3.3 V to achieve such limit. This is very helpful for forward converter, since duty cycle should be limited such that there is enough time to reset the transformer. In our case, N1/N3 is 1 and maximum duty cycle of 0.5 is allowed.

The controller also allows for a simple soft starting circuit using DTC pin. A typical circuit is given in Figure 21. Here, R6 and RT will act as a voltage divider and determine the dead time limit. In our case, they will be selected such that Pin 4 voltage is 1.6 V. From voltage division, R6/(RT+R6) should be equal to 1.6/5 and we have 0.5 duty cycle limit.

$$Ts = C2 \times R6$$

For a soft starting at 40-kHz, C2=22uF is selected and it provides 22ms soft start time which corresponds 880 switching cycle.

RT=2.2kΩ

R6=1kΩ

C2=22uF

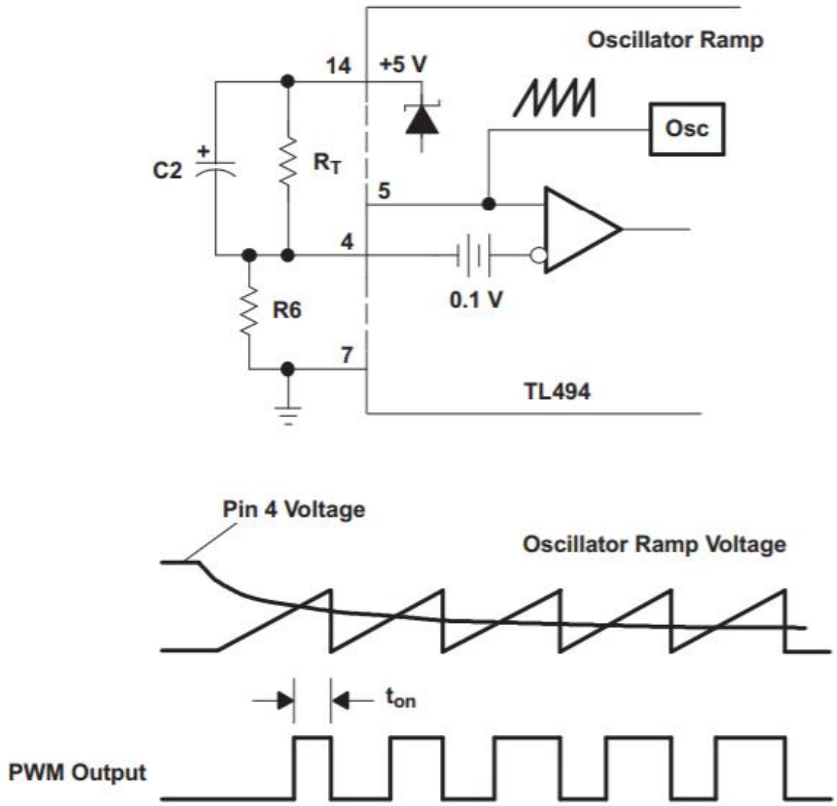


Figure 21. Soft start circuit

General circuit schematic of the controller is given in Figure 22.

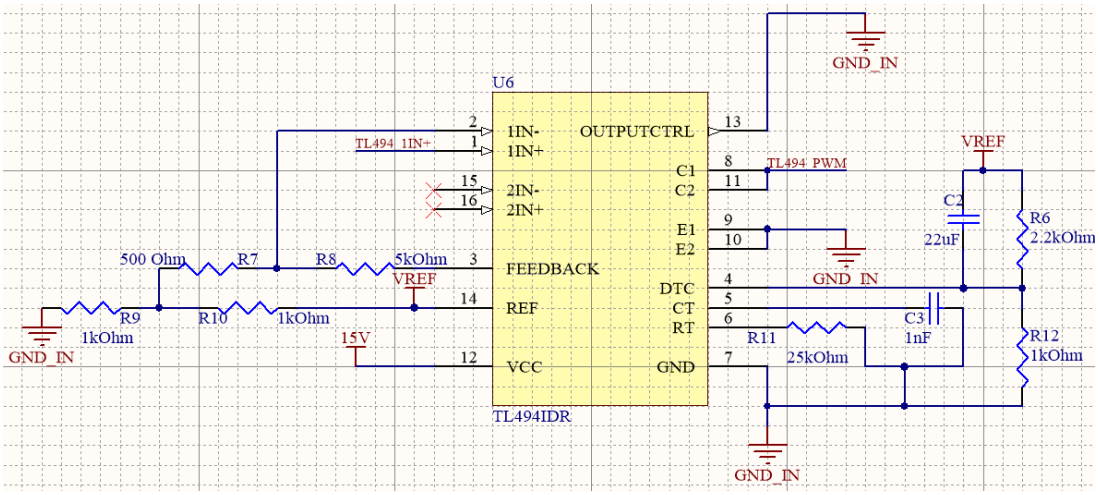


Figure 22. Circuit schematic of TL494 controller

Thermal Design

Since none of the components in the converter are ideal, all of them dissipate certain amount of heat. It is essential to calculate heat dissipation of these components and provide cooling in order to achieve a stable operating temperature without harming any of the components.

In this forward converter design, only the heating of semiconductors (MOSFET and diodes) will be considered since they are the main source of heating. Rest of the components are assumed to dissipate the heat without any additional cooling.

a) MOSFET:

MOSFET has conduction losses when it is on, which is calculated with the equation (12). Lowest value of 24V for input voltage was chosen, as well as rated output power, which are the worst cases for the thermal design. I_{DS} is the RMS current passing through MOSFET, which was found from simulations. R_{DS}=0.18Ω from the datasheet.

$$P_C = {I_{DS}}^2 * R_{DS} \tag{12}$$

For V_i=24V and D=0.467

I_{DS}=4.45A and P_C=3.564 W

Secondly, MOSFET also has switching losses. Switching losses are found using equations (13) and (14) where t_{on} and t_{off} are given in the datasheet. Assuming average voltage and current during those intervals as half of their DC values, total switching losses can be approximated.

$$P_{S,turn\ on} = t_{on} * V_{avg} * I_{avg} * f_s \tag{13}$$

$$P_{S,turn\ on} = 25ns * 12V * 4.05A * 40kHz$$

$$P_{S,turn\ on} = 0.0486\ W$$

Similarly, for turn off period,

$$P_{S,turn\ off} = t_{off} * V_{avg} * I_{avg} * f_s \tag{14}$$

$$P_{S,turn\ off} = 40ns * 24V * 4.05A * 40kHz$$

$$P_{S,turn\ off} = 0.155\ W$$

$$P_S = P_{S,turn\ on} + P_{S,turn\ off} = 0.204W$$

Therefore, total power dissipation of MOSFET is

$$P_{MOSFET} = 3.768W$$

Using Lamped Parameter Model, required heatsink thermal resistivity can be found using formula (15).

$$R_{heatsink} = \frac{T_{junction} - T_{ambient}}{P_{MOSFET}} - R_{junction-case} \quad (15)$$

Maximum operation junction temperature of MOSFET is given as 150 °C, for the design, junction temperature will be chosen as 120 °C. Ambient temperature is assumed to be 30 °C. Junction to case thermal resistivity of the MOSFET is given as 3.13 °C/W in the datasheet. Substituting these values, required heatsink thermal resistivity can be calculated as

$$R_{heatsink,max} = 20.75\ °C/W$$

Also, package type should be same with the MOSFET, which is TO-220 package.

Chosen heatsink: HSE-B1711-032

Rth= 20.27°C/W

TO-220 package (25x16x9 mm)

Figure 23. Heatsink chosen for MOSFET (HSE-B1711-032)

New junction operating temperature can be calculated with same assumed temperature values and with the chosen heatsink as follows:

$$T_{junction} = (R_{heatsink} + R_{junction-case}) * P_{MOSFET} + T_{ambient}$$

$$T_{junction} = 118.18\ °C$$

b) Reset Diode:

Magnetizing inductance of the transformer discharges through this diode. Maximum average current passes through diode happens at highest D value, and from simulations it is observed as

$I_{RD,avg} = 0.67A$. Maximum power loss happens at this current value, which is

$$P_{RD} = I_{RD,avg} * V_F$$

V_F=0.79V from datasheet. Therefore, power loss is $P_{RD} = 0{,}53\ W$.

Switching losses for this diode is very small and can be neglected.

With temperature assumptions similar to the MOSFET analysis, same equation (15) can be used to calculated required heatsink. Junction to case thermal resistivity is 2.5 °C/W (taken from the datasheet).

$$R_{heatsink} = \frac{T_{junction} - T_{ambient}}{P_{RD}} - R_{junction-case}$$

$$R_{heatsink} = \frac{120 - 30}{0.53} - 2.5$$

$$R_{heatsink,max} = 167.3\ °C/W$$

Chosen heatsink: V5274B-T

Package: TO-220 (same with the diode) 25x12x4.5mm

Rth=60.00°C/W

Figure 24. Heatsink chosen for reset diode (V5274B-T)

This heatsink was chosen because it had the highest thermal resistivity with this package type. Junction temperature can be recalculated with same assumptions as follows:

$$T_{junction} = (R_{heatsink} + R_{junction-case}) * P_{RD} + T_{ambient}$$

$$T_{junction} = 63.12\,°C$$

c) Secondary diodes:

2 secondary diodes carry current equal to output current, one in D and other one in 1-D period. They were chosen as a single package 3 leg diode. They will both be cooled with the same heatsink. As the duty cycle changes, one will dissipate more while the other one will less. Since they are on the same chip, it can be approximated that it has a constant current flow equal to output current, and voltage drop of 0.79V given in datasheet. Assuming rated output power, I_{out}=4.8A. Therefore, conduction losses will be simply,

$$P_c = \mathrm{I}_{out} * V_F = 4.8 * 0.79 = 3.80\,W$$

Switching losses are very small and they are neglected.

With similar steps as before, required heatsink thermal resistivity can be calculated as:

$$R_{heatsink} = \frac{120 - 30}{3.8} - 2.5$$

$$R_{heatsink,max} = 21.19\,℃/\mathrm{W}$$

Chosen heatsink: HSE-B1711-032

Rth= 20.27°C/W

TO-220 package (25x16x9 mm)

Figure 25. Heatsink chosen for secondary diodes (HSE-B1711-032)

$$T_{junction} = (R_{heatsink} + R_{junction-case}) * P_{SD} + T_{ambient}$$

$$T_{junction} = 116.5°C$$

PCB Design

For our designed forward converter, we have designed a printed circuit board after selecting all the components. Circuit schematic of the design is shown in Figure 26.

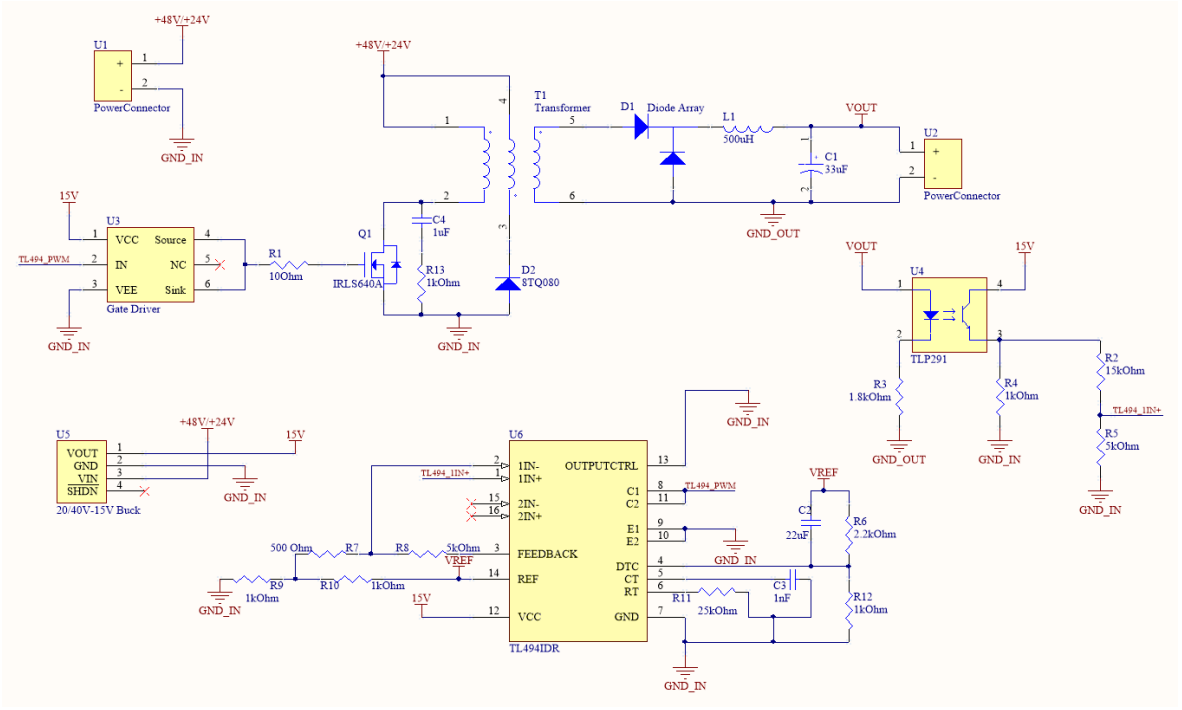


Figure 26. Circuit schematic of PCB design

PCB layout design is shown in Figure 27,28 and 29 which show top layout design, bottom layout design and combined top and bottom respectively.

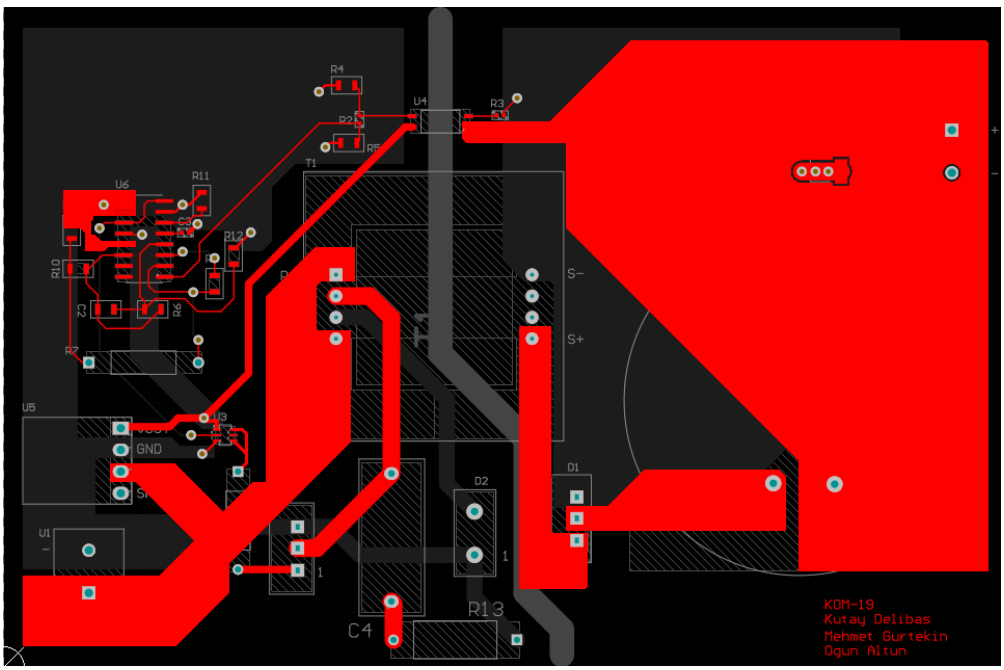


Figure 27. PCB top layout design

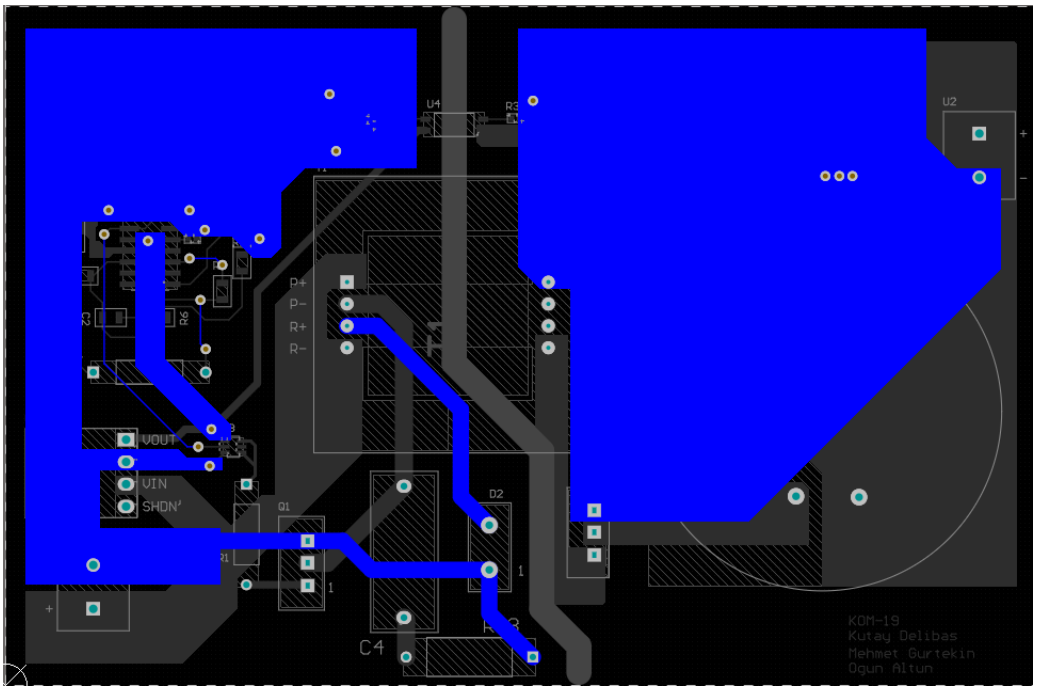


Figure 28. PCB bottom layout design

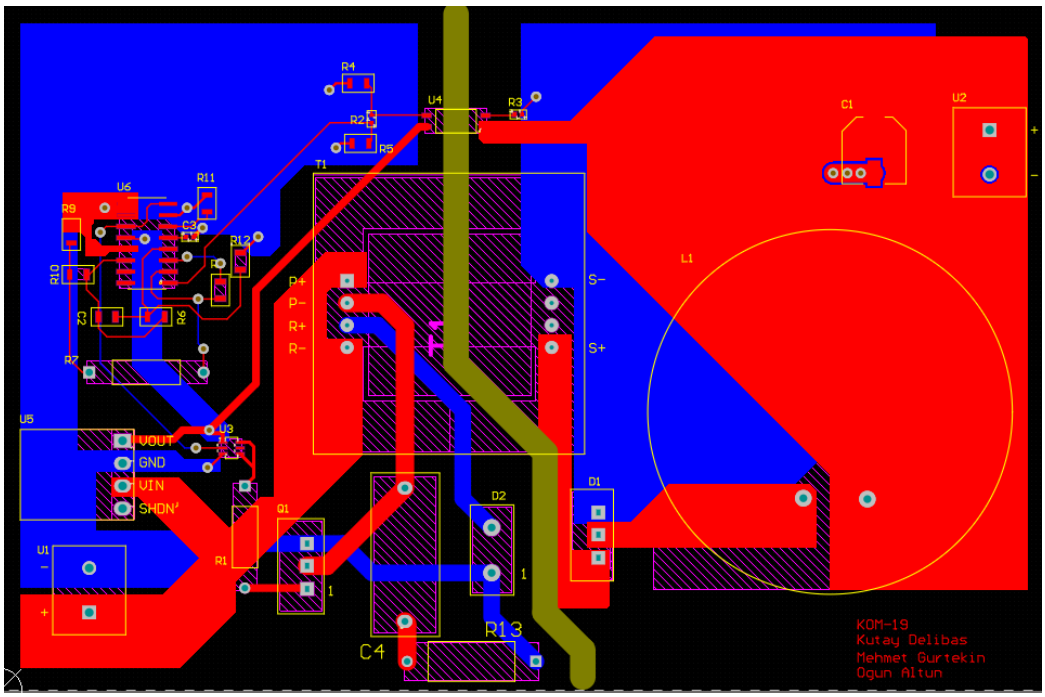


Figure 29. PCB overall layout design

Gerber production files are also given in the Git-Hub repository of the KOM-19 group.

3D model of the designed PCB is also generated and Figure 30 and 31 show 3D model from two different perspectives.

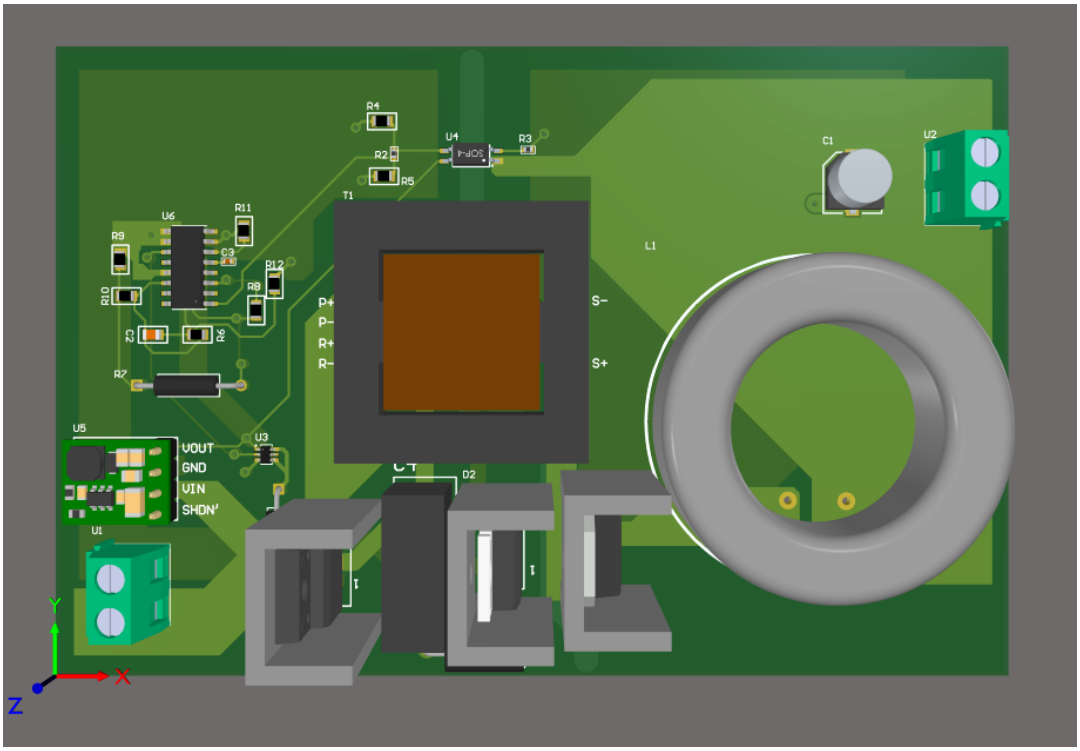


Figure 30. 3D model of PCB design, top view

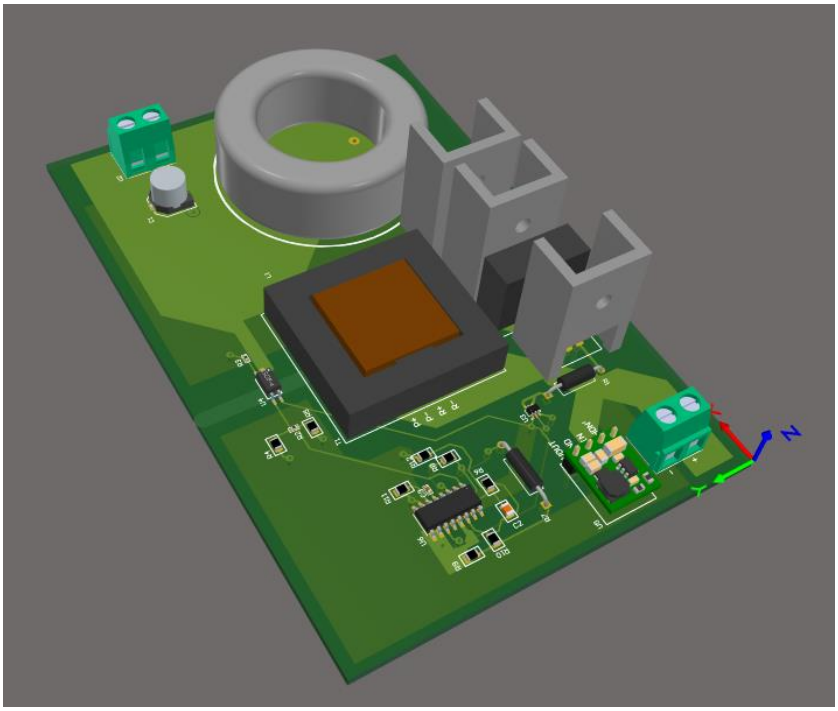


Figure 31. 3D model of PCB design, isometric view

Below table shows the bill of materials for the selected components for this design.

Comment	Designator	Digikey Part Number	Quantitiy	Price $
33uF	C1	EEE-FT1E101AP	1	0,64
22uF	C2	CL21A226KQCLRNC	1	0,19
1nF	C3	C0402C102K4RACTU	1	0,10
1uF	C4	ECWFE2W105K	1	0,63
Diode Array	D1	TST20U100CC0G	1	0,96
8TQ100	D2	8TQ100	1	0,76
500uH	L1	-	1	10,00
IRLS640A	Q1	IRLS640A	1	1,5
10Ohm	R1	CF14JT10R0	1	0,10
15kOhm	R2	CRGCQ0402F15K	1	0,10
1.8kOhm	R3	CRGCQ0402F1K8	1	0,10
1kOhm	R4, R9, R10, R12	RC0805JR-071KL	4	0,40
5kOhm	R5, R8	CRCW08055K00JNTA	2	0,24
2.2kOhm	R6	RC0805FR-072K2L	1	0,10
500Ohm	R7	CMF55500R00FKEB	1	0,58
25kOhm	R11	5-2176238-6	1	0,57
1kOhm	R13	FMP200JR-52-1K	1	0,34
Transformer	T1	-	1	1,00
PowerConnector	U1, U2	282836-2	2	1,42
Gate Driver	U3	ZXGD3009DYTA	1	0,41
TLP291	U4	TLP291(GB-TP,SE	1	0,09
15V Buck	U5	3797	1	4,95
TL494IDR	U6	TL494IDR	1	0,39
HeatSink1		V5274B-T	1	0,55
HeatSink2		HSE-B1711-032	2	0,56

Total cost of the components is **26.68$**. Moreover, we have got a manufacturing cost for our designed PCB from PCBWay for 1000 samples. Cost of the single PCB manufacturing is **1.13$** and final cost of the PCB became **27.81$**.

Efficiency Analysis

Output power of the converter that we have designed is 48W. The list of losses calculated in this report is as follows.

Transformer core loss: 845mW

Transformer copper loss: $R_{N1}*I_{N1,\,rms}^2 + R_{N2}*I_{N2,\,rms}^2 + R_{N3}*I_{N3,\,rms}^2$

$=21.4m\Omega*(3.6A_{RMS})^2+51.3m\Omega*(2.22A_{RMS})^2+64.13m\Omega*(1.4A_{RMS})^2 =656mW$

Inductor core loss: 44mW

Inductor copper loss: $R_L*I_L^2 = 36.83\ m\Omega*(2.22A)^2=182mW$

MOSFET losses: 3.768W

Reset diode losses: 0.53W

Secondary diodes losses: 3.8W

Then, overall efficiency of the converter is calculated by equation below.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{48\text{W}}{48\text{W} + 9.827\text{W}} = 83\%$$

Simulation of the converter in the Simulink supports this result with 83% efficiency for 24V input voltage.

Transfer Function Derivation

We need to derive the control to output transfer function of our topology to be able to design a controller for it. In order to derive the control to output transfer function, we can describe our circuit in terms of state-variable vector x which consists of the capacitor voltage and inductor current. Moreover, in this derivation we analyzed the circuit for switch is opened and closed separately and averaged them. Lastly, capital letters are used for DC values and small letters are used for AC values where every component can be written as a sum of its DC and AC components. We can write the state space equations during d.Ts as follows:

$$\frac{dx}{dt} = A_1 * x + B_1 * v_d \, , v_o = C_1 * x \tag{16}$$

Where v_d is the input and v_o is the output. We can write the state space equations during (1-d).Ts as follows:

$$\frac{dx}{dt} = A_2 * x + B_2 * v_d \, , v_o = C_2 * x \tag{17}$$

Averaging the equations (1) and (2) results in:

$$\frac{dx}{dt} = [A_1 * d + A_2 * (1-d)]x + [B_1 * d + B_2 * (1-d)]v_d \, , v_o = [C_1 * d + C_2 * (1-d)]x \tag{18}$$

In the first part of this equation, the coefficient of x can be called A, the coefficient of v_d can be called B and in the second part the coefficient of x can be called C. Moreover, in this equation every term can be separated to its DC and AC components (etc. x=X+x). The only component that is not separated is the input voltage which is assumed to have no AC component. When every term is separated and the products of two AC components are neglected, we obtain the following equations:

$$\frac{dx}{dt} = A * X + B * V_d + A * x + [(A_1 - A_2) * X + (B_1 - B_2) * V_d] * d \quad (19)$$

$$V_o + v_o = C * X + C * x + [(C_1 - C_2) * X] * d \quad (20)$$

At steady state conditions, AC terms can be neglected and results in a transfer function as follows:

$$\frac{V_o}{V_d} = -C * A^{-1} * B \quad (21)$$

Using Laplace transformation on the AC part of the equation (4) :

$$x(s) = [s * I - A]^{-1} * [(A_1 - A_2) * X + (B_1 - B_2) * V_d] * d(s) \quad (22)$$

Expressing x(s) in terms of d(s) and combining it with the Laplace of the ac part of the equation (5) results in a control to output transfer function as follows:

$$T(s) = \frac{v_o(s)}{d(s)} = C * [s * I - A]^{-1} * [(A_1 - A_2) * X + (B_1 - B_2) * V_d] + (C_1 - C_2) * X \quad (23)$$

In the figure below forward converter with the state variables is shown. For the switch on case (left hand side of the figure) KVL equations can be written as follows:

$$-\frac{N_2}{N_1} V_d + L * \frac{dx_1}{dt} + r_L * x_1 + R * \left(x_1 - C * \frac{dx_2}{dt}\right) = 0 \quad (24)$$

$$-x_2 - C * r_C * \frac{dx_2}{dt} + R * \left(x_1 - C * \frac{dx_2}{dt}\right) = 0 \quad (25)$$

For the switch off case the only difference is the Vd term in the equation (9) will be zero the rest are the same with the switch on case. From all of these equations and assuming that R is much bigger than $r_L \; and \; r_C$ gives us the following matrices:

$$A = A_1 = A_2 = \begin{bmatrix} \frac{-r_C * r_L}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{C*R} \end{bmatrix} \quad (26)$$

$$B = B_1 * D = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} * D * \frac{N_2}{N_1} \quad (27)$$

$$C = C_1 = C_2 = [r_C \quad 1] \quad (28)$$

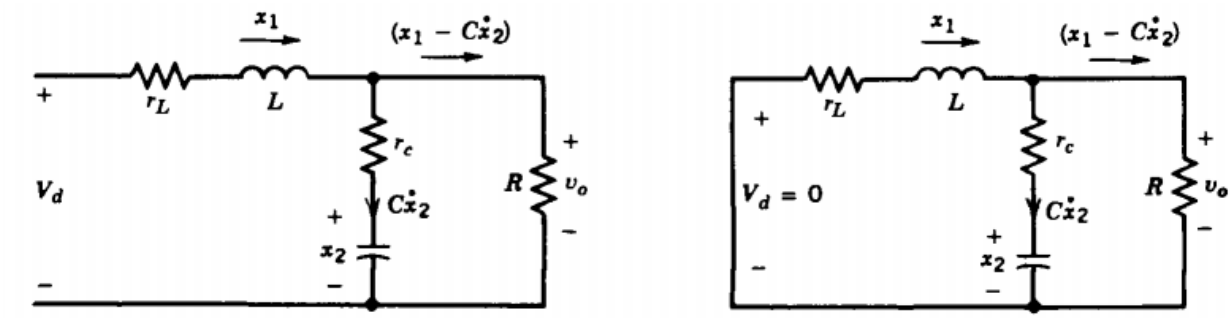


Figure 32. Forward converter secondary side with state variables

All of the matrices found in (26), (27), (28) can be implemented into equation (23). This implementation results in the control to output transfer function:

$$\frac{v_o(s)}{d(s)} = \frac{\frac{N_2}{N_1} * V_d * (1 + s * r_C * C)}{LC\{s^2 + s[\frac{1}{CR} + \frac{r_C * r_L}{L}] + \frac{1}{L*C}\}} \tag{29}$$

In order to make this transfer function fit in the standard form, following substitutions can be made:

$$\omega_0 = \frac{1}{\sqrt{L*C}} \tag{30}$$

$$£ = \frac{\frac{1}{CR} + \frac{r_C * r_L}{L}}{2 * \omega_0} \tag{31}$$

$$\omega_z = \frac{1}{r_C * C} \tag{32}$$

The transfer function with these implementations can be written as follows:

$$\frac{v_o(s)}{d(s)} = \frac{N_2}{N_1} * V_d * \frac{\omega_0^2}{\omega_z} * \frac{s + \omega_z}{s^2 + 2 * £ * \omega_0 * s + \omega_0^2} \tag{33}$$

Compensator Design

For the compensator design, we first need to find the pole/zero frequencies of the transfer function that we obtained and select a zero-crossover frequency. Zero- crossover frequency is selected as 1/5 to 1/10 of the frequency of switching. We selected it as 1/8 of out switching frequency which is 5kHz. Pole and zero frequencies are found from the equations below:

$$f_{pole} = \frac{1}{2 * \pi * \sqrt{L * C}}, \; f_{zero} = \frac{1}{2 * \pi * C * r_C} \tag{34}$$

The table below shows the important frequencies of this system:

F pole	F zero-crossover	F zero ESR	F switch
1.239 kHz	5 kHz	18.651 kHz	40 kHz

After finding these frequencies, the next step is selecting the compensator type. This selection made with a convention taken from the book the Dynamics and Control of Switched Electronic Systems. The convention is indicated in the figure below:

Compensator Type	Relative location of the crossover and power-stage frequencies
Type II (PI)	$F_{LC} < F_{ESR} < F_0 < F_S/2$
Type III-A (PID)	$F_{LC} < F_0 < F_{ESR} < F_S/2$
Type III-B (PID)	$F_{LC} < F_0 < F_S/2 < F_{ESR}$

Figure 33. Convention for compensator type selection

Using this convention with the frequencies that we found and indicated in the table above, gives us the result that Type III-A is the most suitable compensator type for our system.

In the Type III-A compensator approach poles and zeros of the compensator is selected as indicated below:

$$F_{Z2} = F_{LC}\,, F_{Z1} = 0.75 * F_{Z2}\,, F_{p2} = F_{ESR}\,, F_{p3} = \frac{F_S}{2} \tag{35}$$

The formulas of this poles and zero values can be seen below:

$$F_{Z1} = \frac{1}{2*\pi*R_{C1}*C_{C1}}\,, F_{Z2} = \frac{1}{2*\pi*C_{f3}*(R_{f1}+R_{f3})} \tag{36}$$

$$F_{p1} = 0, F_{p2} = \frac{1}{2*\pi*C_{f3}*R_{f3}}, F_{p3} = \frac{1}{2*\pi*C_{C2}*R_{C1}} \tag{37}$$

In order to find the circuit component values, it is needed to start with attaining a value to a capacitor. In our case we selected C_{f3} equal to 2.2nF. Moreover, the voltage level of the sawtooth wave and the reference voltage have to be selected beforehand and which are selected as 1.8 Volts and 0.9 Volts respectively which are standard selections. Then, when the formulas

given in equations (36) and (37) are used to find the required frequencies given in equation (35), the resulting circuit component values can be found as follows:

C_{C1}	C_{C2}	C_{f3}	R_{f1}	R_{f2}	R_{f3}	R_{C1}
19.5nF	1nF	2.2nF	54.5kΩ	5.4kΩ	3.88kΩ	8.8kΩ

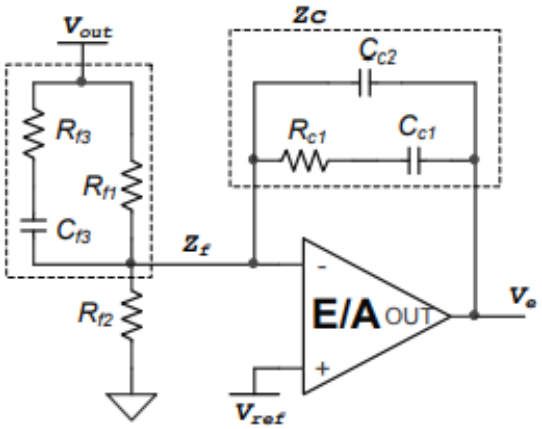


Figure 14. Type III compensator circuit schematic

Bode Plots

At first, we derived the transfer function of the forward converter. At the Figure 4 below the bode plot of this transfer function is indicated. Later, we designed a compensator in order to get a better response from our circuit. Figure 5 indicates the bode plot of the forward converter and compensator system. When we look at the bode plots, there are several differences that draws attention. Firstly, the gain of the compensated system is higher for small frequencies and stalls at high gains for a longer time. Moreover, for the higher frequencies the gain drops much faster in the compensated system. From the gain plots, one can observe that compensated system has higher DC gain and better filtering characteristics for harmonics. The desired characteristics for phase plots are having 180 degrees as the frequency increases (to filter out harmonics) and have a high phase margin (higher than 40 degrees). The uncompensated system has a good phase margin. However, as the frequency increases the phase angle stays at 90 degrees which is not desired. Type III compensator make the phase angle start from -90 degrees but thanks to the huge phase boost it still have 60 degrees phase margin and has phase angle 180 degrees for higher frequencies. To sum up all, the compensated system shows a desired behavior and its feasible for our system.

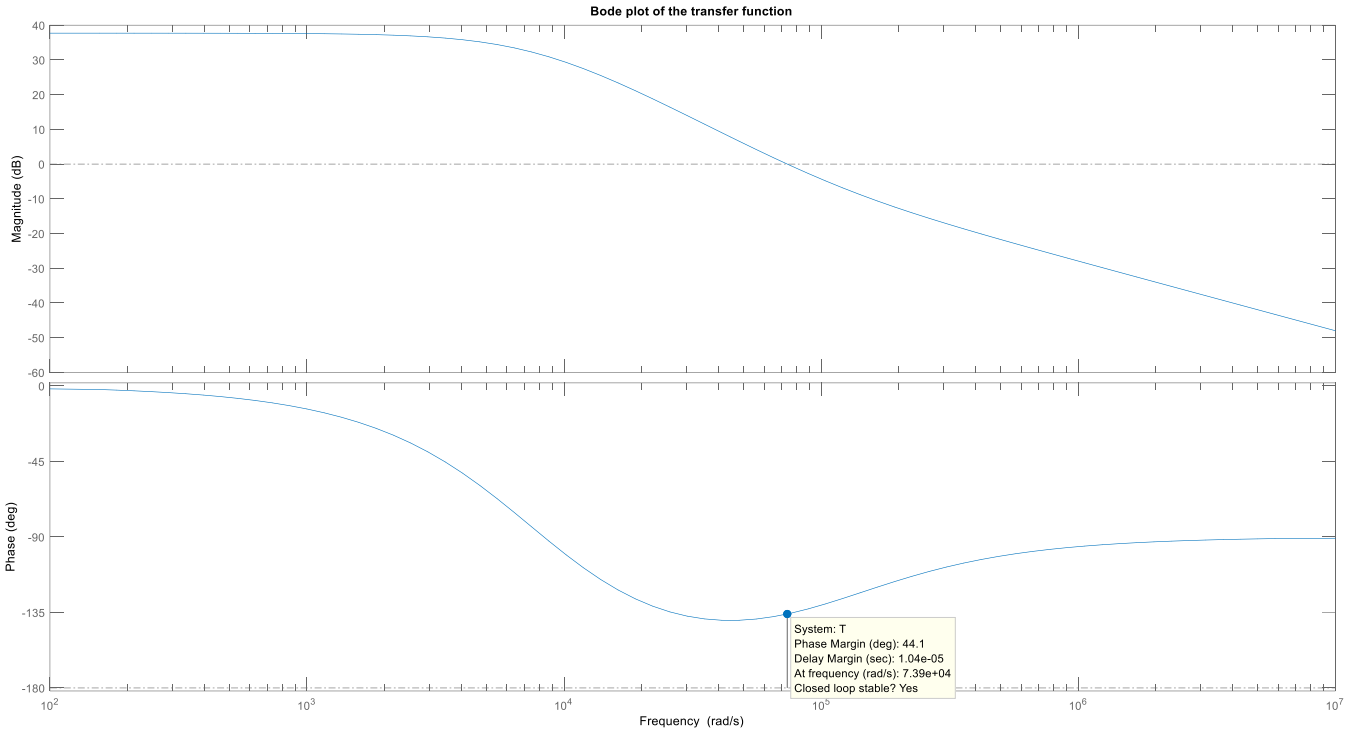


Figure 35. Bode plot of the forward converter topology

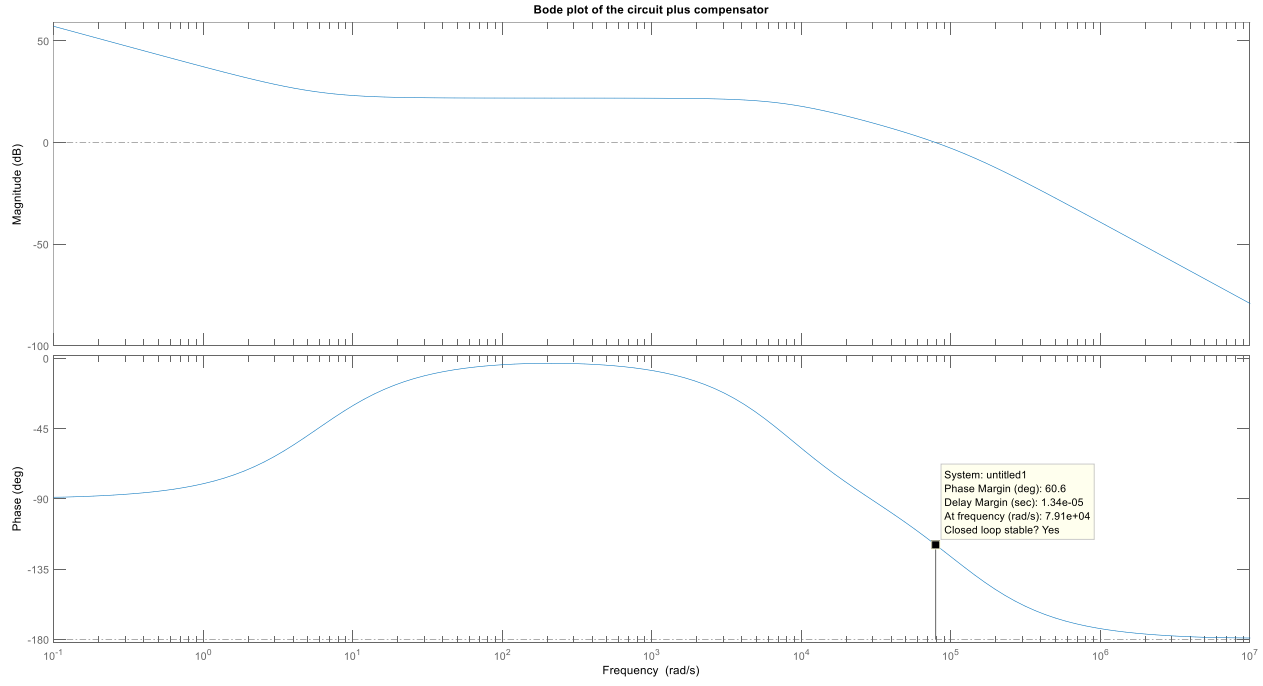


Figure 36. Bode plot of the forward converter with the compensator

Transient Response

After designing our compensator and checking its transfer function with the forward converter topology, we decided to check validity of our compensator by observing its transient response. In order to observe transient response, we created the circuit schematic in LTSpice as indicated in the Figure 6 below. We observed two transient responses which are load regulation and line regulation.

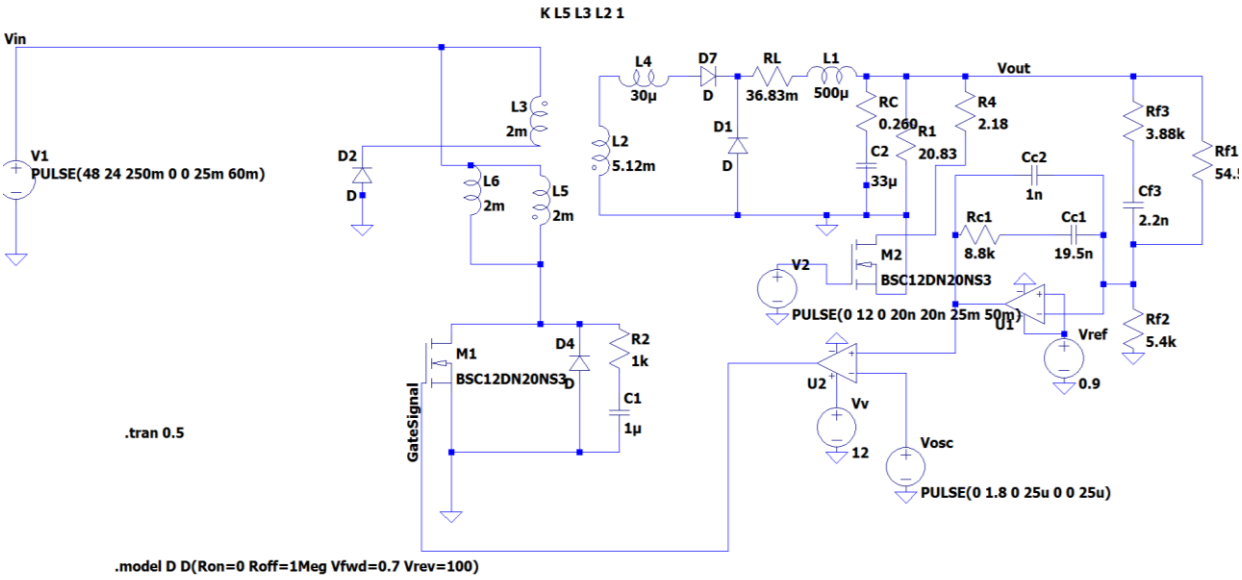


Figure 37. LTSpice schematic of compensated forward converter

Load Regulation

Load regulation is the deviation of the output voltage in percentage when the load resistance is changed from 10 times of its value to its original value or vice versa. At first load resistance is 2.083Ω and at t=25ms it is changed to 20.83Ω then at t=50ms it is returned back to 2.083Ω which is the original value. The output voltage behavior under these conditions is indicated in the Figure 7 below. At t=25ms the output voltage increases suddenly with the increasing output resistance, but it returns back to 10 volts in around 1ms. At t=50ms the output voltage decreases less than the increase at t=25ms and returns back to 10 volts in around 0.4ms.

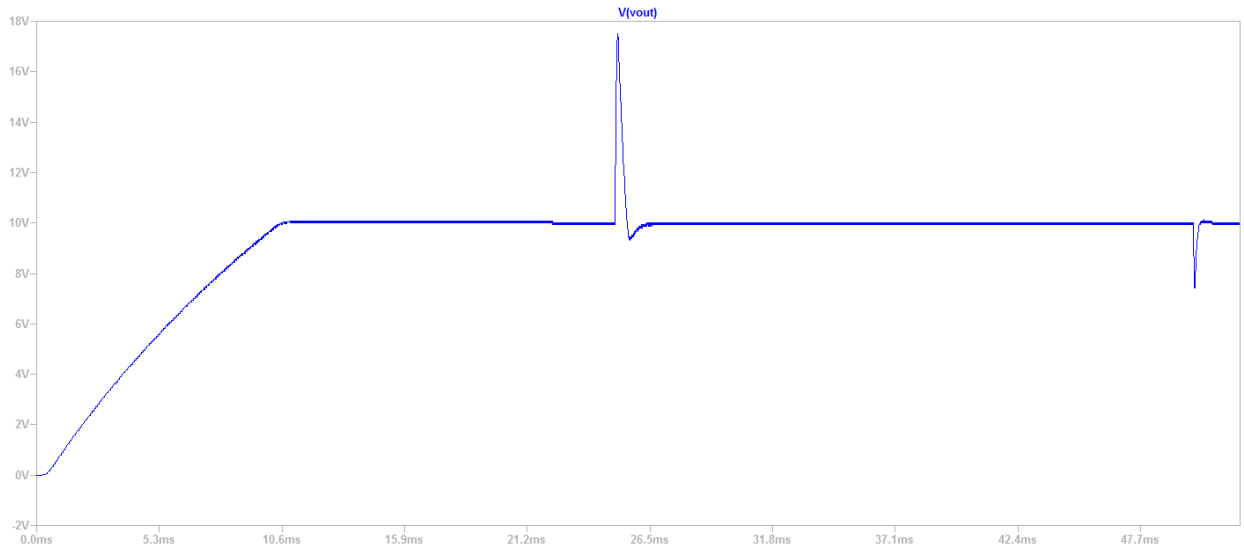


Figure 38. Output voltage characteristics when load is changed

Line Regulation

Line regulation is the deviation of the output voltage in percentage when the input voltage is changed from its maximum value to its minimum value or vice versa. At first the input voltage is 48 Volts and at t=25ms it is changed to 24 Volts and at t=35ms it is returned back to 48 Volts to be able to observe the transient changes with respect to input voltage change. When the input voltage is dropped to 24 volts and the output voltage drops a little bit and in 1.5ms it returns back to 10 volts again as indicated in the Figure 8 below. At the same time the increase in the PWM duty cycle can be seen in the Figure 9. At t=35ms the input voltage is increased to 48 Volts and the output voltage increases a little then it returns back to 10 volts in 1.5ms.

We looked at our system's transient response and from all of our observations we can clearly say that the compensator design is feasible for this project.

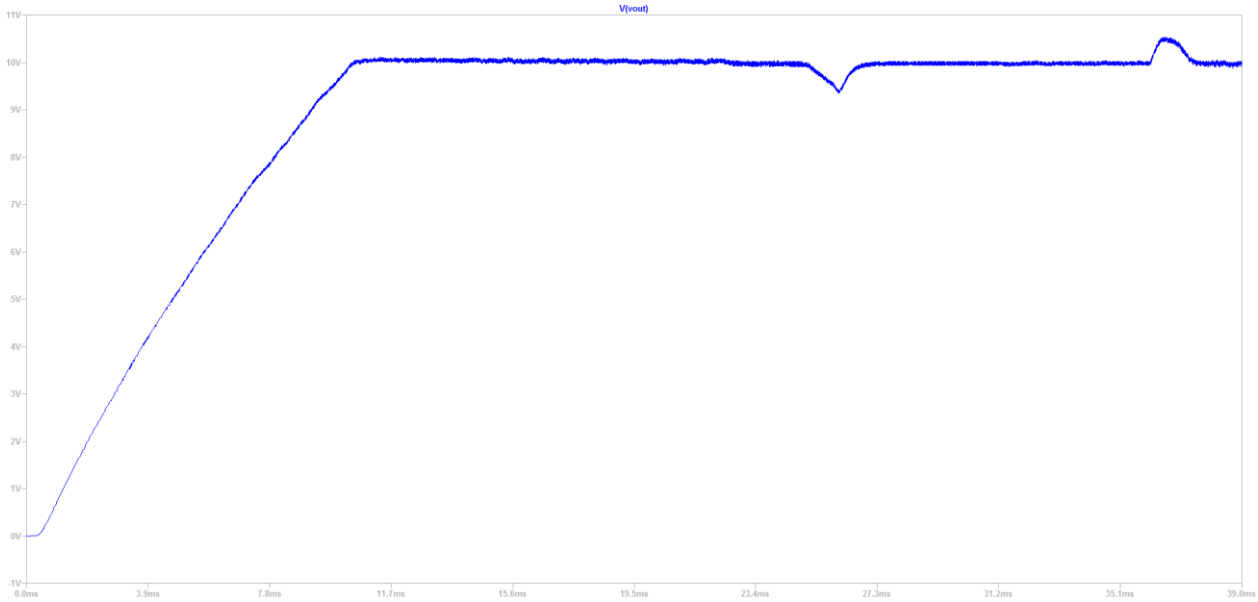


Figure 39. Output voltage characteristics when the input voltage is changed.

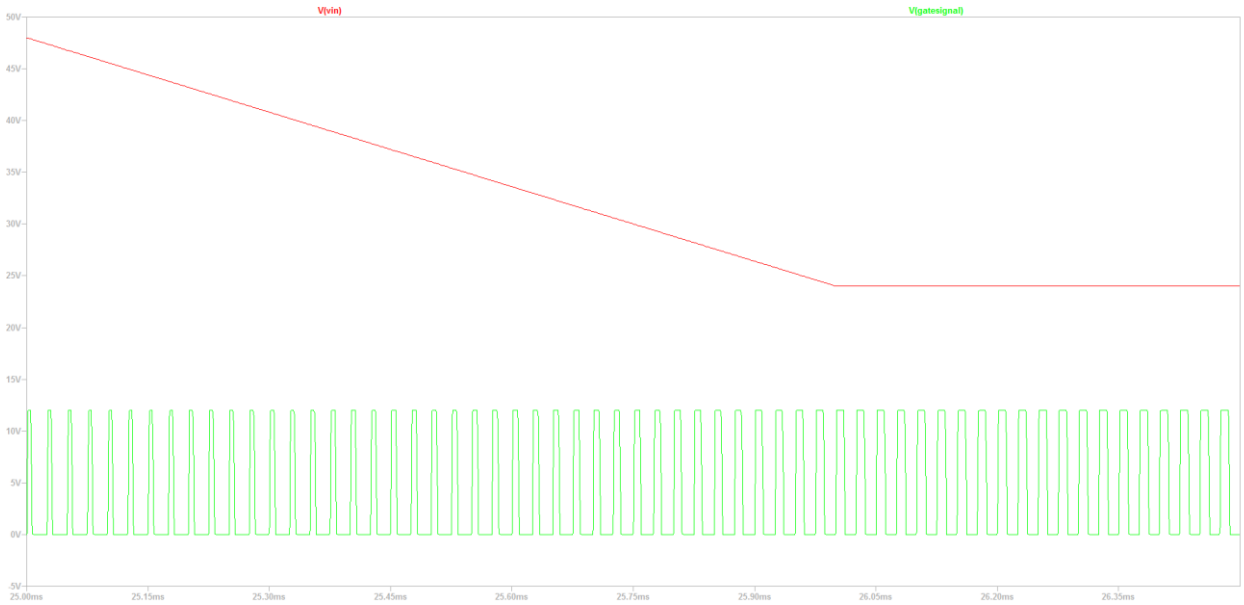


Figure 40. PWM characteristics when the input voltage is changed

Conclusion

Due to unusual circumstances of the semester, the hardware project was completed as a detailed design and simulation project instead. We have reviewed our design choices to fit a more proper design since available components on internet is superior to what was available in our laboratory and stores in Turkey. We first started with magnetic designs of transformer and inductor using several guides from websites such as Magnetics to determine proper cores for our design choices. Starting from Simulink simulation with ideal components, we have selected the products and added some non-idealities to observe their effect on the design. Turns ratio of the transformer is updated to overcome the losses in the system. Finally, after magnetic design is done, we could make a more realistic simulation with non-idealities of chosen products.

In addition, we have made thermal design in order to make the converter realizable as a hardware product since overheating is a big problem in power electronics. We aimed for stable operating temperatures and chose heatsinks for our semiconductor devices. Moreover, a PCB design and 3D view of it was made in order to determine and demonstrate the layout of the converter in a neat and safe way. Bill of materials of the design is calculated such that this design can be used for mass production. Efficiency is calculated as well.

Furthermore, transfer function of the converter was derived and frequency response of the converter and controller was observed. A type III-A compensator was used according to guidelines to make the converter more stable with a better phase margin. Line and load regulation of the converter is also tested.

To conclude, despite the pandemic, the project was further improved in detail and it can easily be manufactured using this paper as a guide.