Digital Logic Design LAB

FINAL PROJECT

6 BIT RANDOM NUMBER GENERATOR

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Section: **CS-A**

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Contents

Project Description:

We are designing a circuit that can randomly generate a 6-bit number when the instruction is given, or input is provided. Project is named as the 6-bit random generator and to make a circuit that can randomly generate 6-bit number we are allowed only to use flip flops IC's and other necessary IC's. We have to show the output in both binary and decimal form so a number will be in its binary as well as in decimal form.

Equipment used for the circuit:

Equipment used in the circuit for the designing of the 6-bit random generator circuit are:

- **Negative triggered J-k flip flops**
- **Seven segment BCD Display**
- **And Gate 7408**
- **Not gate**
- **And_3 gate 7411**
- **Push Button**
- **Logic Probe [Big]**
- **DC Clock**
- **Logic toggle**

Overview:

Basically what we will be doing is that we are producing a 6 bit counter that will provide random numbers up till 63, which is the highest 6-bit number. Whenever the push button is pressed, a 6-bit binary is generated, and it will be displayed on the logic probe. Now the problem here is that we have to display the binary into decimal also and binary is 6 bit and only a 4-bit binary can be used to display on seven segment display (excluding 10-15). So for that, we have to develop a logic that will convert a 6-bit binary into two BCD binaries and then that two 4 bit binary can be displayed on seven segment display. To be more explicit, we have to neglect values from 10 to 15 as it can't be displayed on one seven segment display and we have to develop a logic that converts 6-bit binary into two BCD. After that, we have to devise proper equations for the circuit. To devise equations we have to make truth table of our logic and then K-map and then equations.

Difficulties:

There are different points in this project where I stuck, and then I had to revisit my lectures and concepts about designing any circuit. First of all, to devise a logic to convert the 6-bit number into a binary of two BCD's was the most challenging part I spent almost most of my time deriving the

logic and then through truth table and K-map I was able to render equations on which I made my combinational circuit. Designing a Counter that produces 6-bit binary was easy as we have studied J-k flip flops in class and about counters also, so it was easy.

Circuit:

To explain the circuit, we will divide the circuit into two parts:

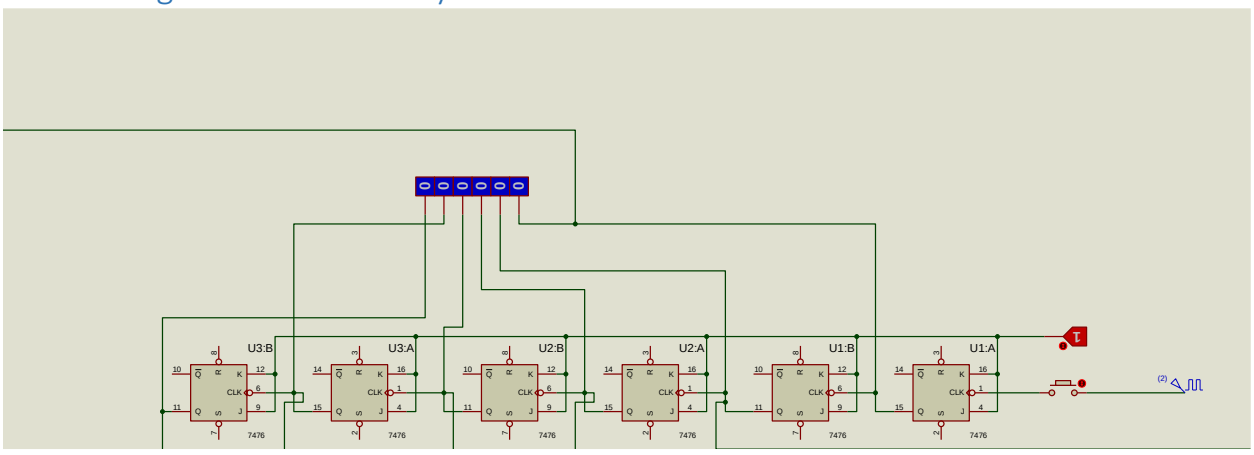
- 6 bit binary counter.
- Binary to decimal display.

In the first part, there is a 6 bit binary counter that displays the 6-bit random number in its binary form and to convert that binary into decimal we have to build another circuit which will be explained after that first we will discuss 6 bit binary counter.

6- Bit binary counter:

6 bit binary counter is a counter that is displaying us a binary of 6 bits. I built this binary counter using j-k flip flops.

Circuit Diagram of 6 bit binary counter:



The above circuit shows counter that is designed by j-k flip flop and a clock, and there is push-button attached to it. So working on the above circuit is as follows:

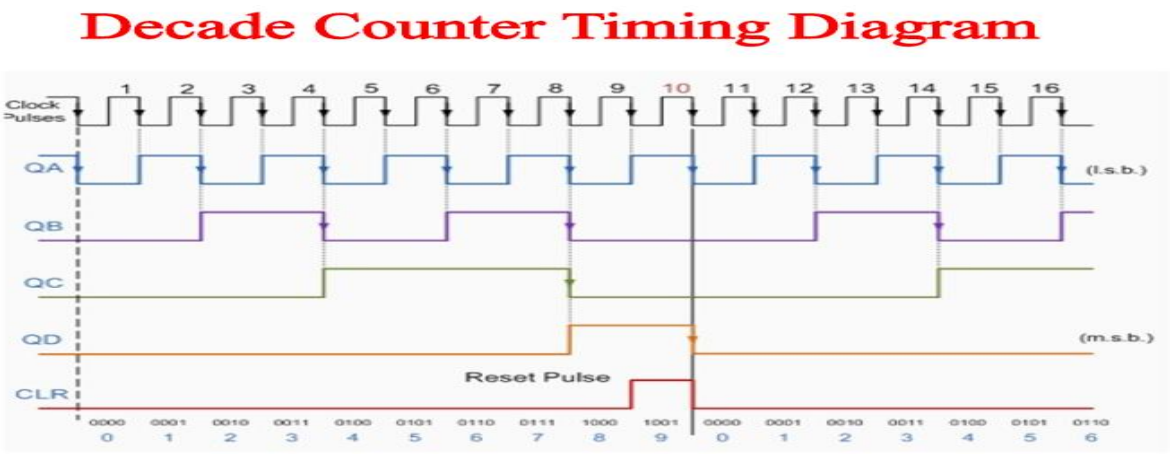
Working of Circuit:

The clock is creating a pulse, and JK flip flop is negative edge triggered that means whenever the pulse of the clock is going downwards it will generate output at Q or we can say JK flip flop will toggle. Following is the condition we are using to toggle the JK flip flop.

J	K	Clock	Q	Q’
1	1	Downward Pulse	Q’	Q_0

So basically in the above circuit, we are giving input of J and K flip flop one and whenever there is a pulse which has a negative edge or moving downwards, then J-k flip flop will toggle. When there is toggling on J-k flip flop, then we have output pulse generating at Q. so if we imagine only one JK Flip flop attached to the clock, then it will toggle between 1 and 0 continuously. As I have to produce a 6-bit number and there must be six binary outputs (000000-111111) and 1 JK flip flop will give only one output, and that output will toggle in between 1 and zero. So let’s say I will attach all the flip flops with clock and then see what happen. The output will be 000000 and then 111111. On the logic probe, it will display only these outputs. So the problem here is that it will only be giving me 6 bit maximum and minimum number but to produce every number I will be in need of combinations of that binary so to make it possible we don’t have to connect the clock of J-k flip flops to the same clock but we have to produce some timing difference for every flip flop so that it toggles at a different time and with respect to previous one so that we can have series of combinations and to do so we have to primarily focus on the clock of the next J-k flip flop, and it will be possible in this manner.

If we connect the output Q to clock of next J-k flip flop and we go on like this till the last j-k flip flop what will happen here is that there will be a timing difference for every J-k flip flop so it will be producing combinations of numbers. To understand it more clearly let’s look at the timing diagram of the four-bit counter.



So here we can see the next bit depends on the previous output from j-k flip flop basically it is creating timing difference, and we can calculate this from here.

If we see Q_0 and Q_1, they have different timing diagrams and the timing diagram of Q_1 depend on the pulse that is given from Q_0. So let's say Time period for Q_0 is T_A and time period for Q1 is T_b it is clear from the picture that

$$T_A=2T_B$$

So the frequency will be as follows

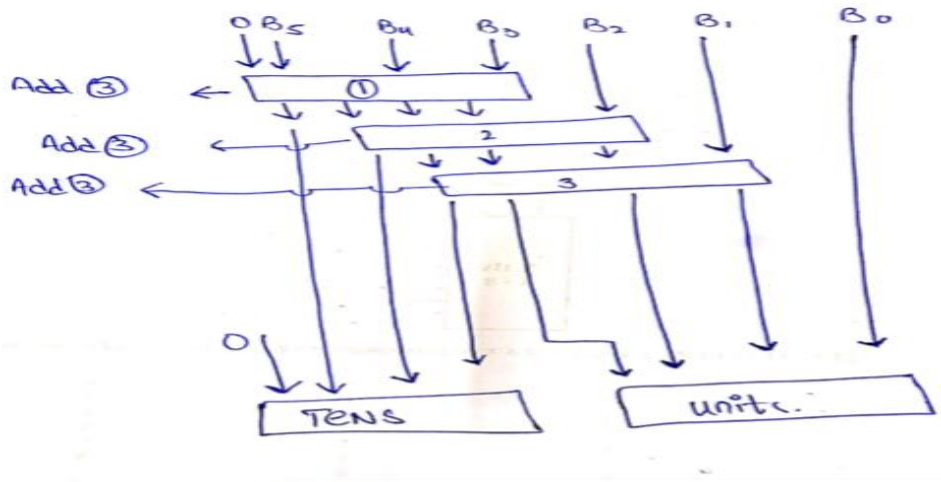
$$F_A=F_B/2$$

So this will move on for 6 bits, and every next J-k flip flop will be depending on the previous one, and this will create every possible combination for 6-bit binary and then it will be producing every 6-bit number which is till 63. To make these numbers random, I will be using a push-button whenever this push button is pressed it unknown numbers of pulses are generated from the clock, and a random binary is displayed on the Big Probe. That is how a 6-bit random binary is produced using negative triggered J-k flip flops and Push button and clock.

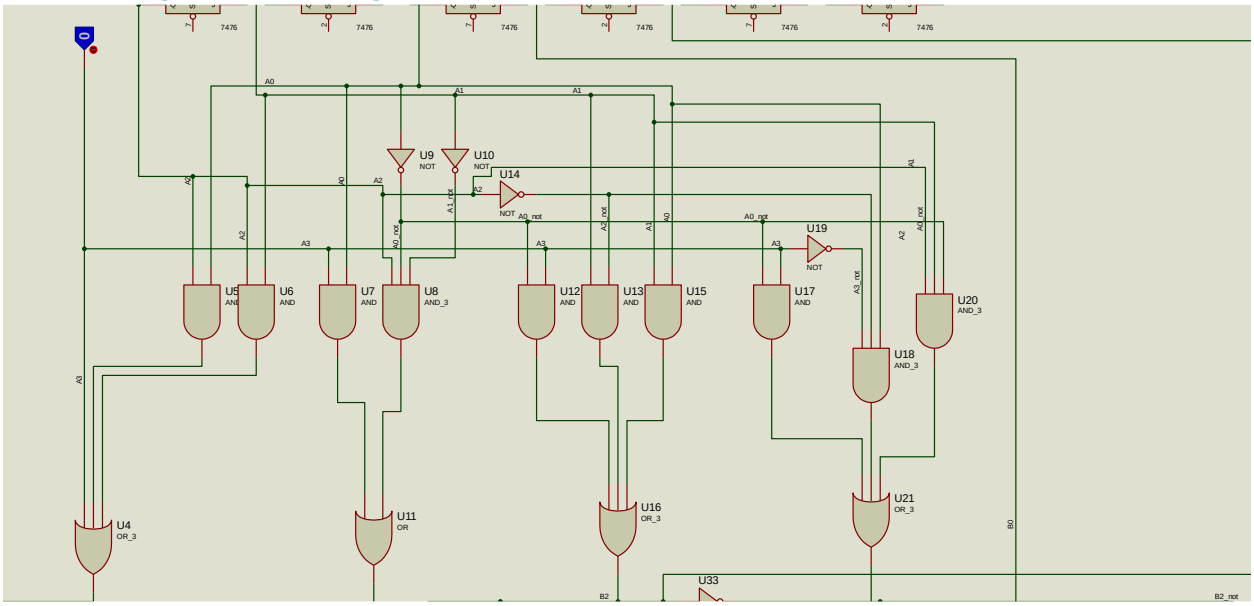
Binary to Decimal Display:

Binary to decimal display; this is the second part of the circuit. In this, we will be making a logic to convert binary which is 6 bit into two BCD binaries so that it can be displayed on the seven segment displays independently and to do so we will be using this logic. We will start from the most significant bit, and we will move to the least significant bit and starting with last three MSB, and then we will check whether that number is greater than or equal to 5 or not (>=5). If that number is more significant than equal to 5, then we will add 3 in it, and then we will do this repeatedly, and the flow chart of the logic is as follows:

Let's say we have a binary of 000000(o in 6 bits) to display it on two BCD seven segment displays this technique will be used:



Circuit Diagram of Adding 3:



Explanation:

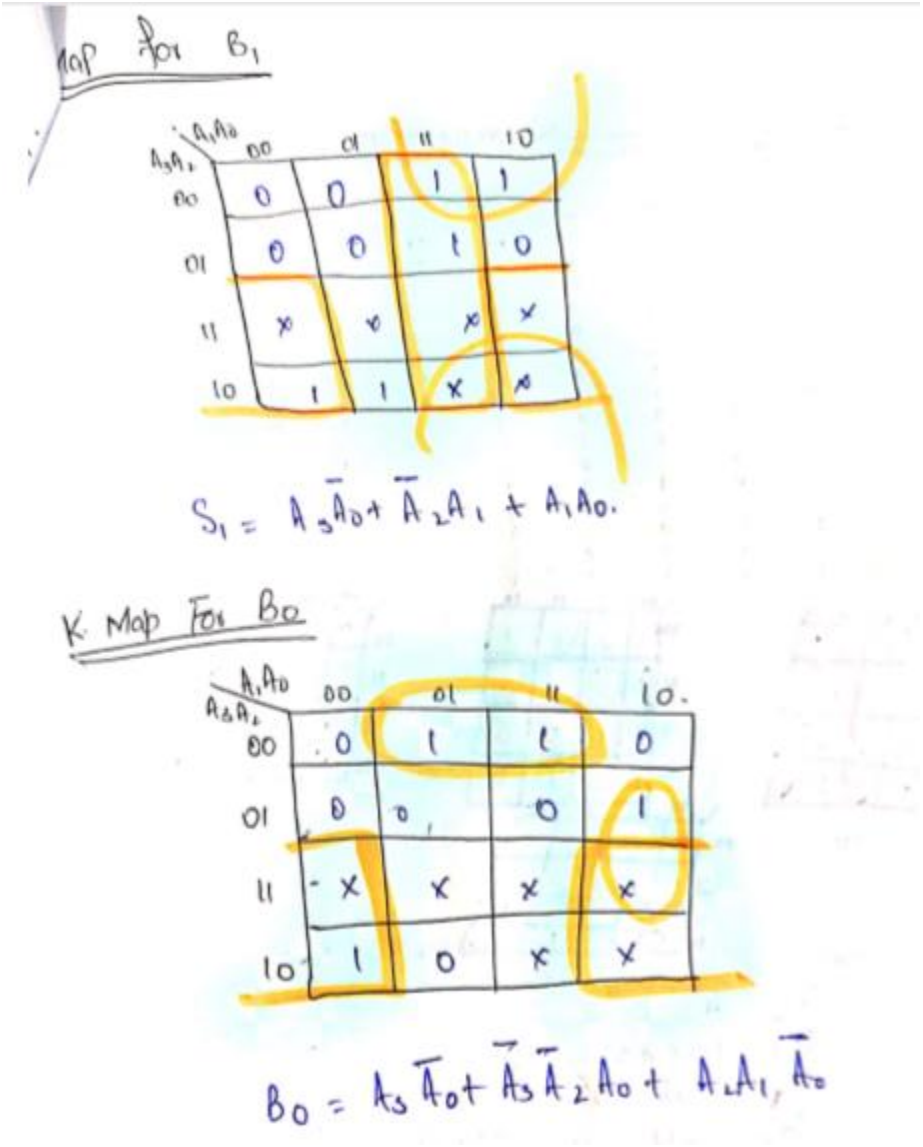
For the description of this circuit, we will be in need to explain it through truth table, here is the truth table for the Add-3 circuit.

Decimal	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	1	1	0	0	1
7	0	1	1	0	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				

When the number is lesser than five, the output binary B3B2B1B0 is same as the input, so there is no change, but when the number is five or more significant than five then there will be an addition of 3 in that value and the output will be changed. If the input is higher than nine, it will be don't care condition as it is of no use because I can't display it on the one seven-segment display.

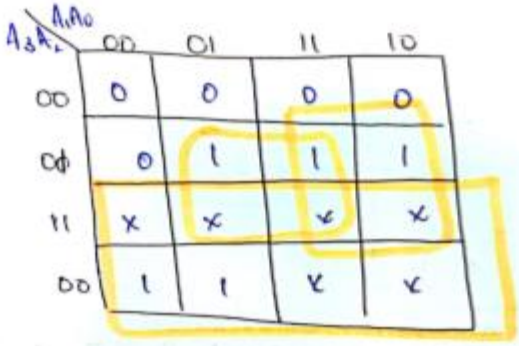
K-maps for This Truth table:

Following are the truth table from this K-map.



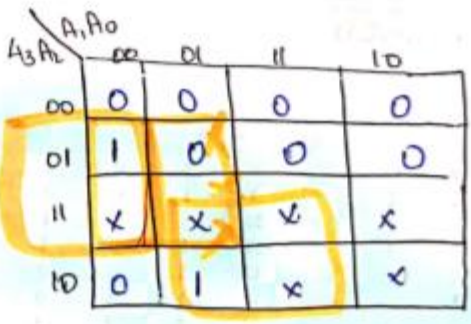
K- Map for other two output is as follows:

K-Map For B_3



$B_3 = A_3 + A_2 A_0 + A_2 A_1$

K-Map For B_2



$B_0 = A_3 A_0 + A_2 \overline{A_1}\,\overline{A_0}$ (compliment)

By making the groups, we devised the possible equations for the circuit and then from these simple equations we devised the circuit equation and then circuit to convert the number into BCD can be designed by using just combinational circuit.

Explanation of Logic:

What we are adding here is that I will start from the MSB and then I will move to LSB, and I will check binary three times. If that binary is more significant than five or equal to five, then I will add binary of three in it. If that number is not greater than five, later that binary will not be changed and returned as same. First, three most significant bits will be Tens, and the last four bits will be Units, and then these pins are connected to BCD 7 segment display which will display the binary.

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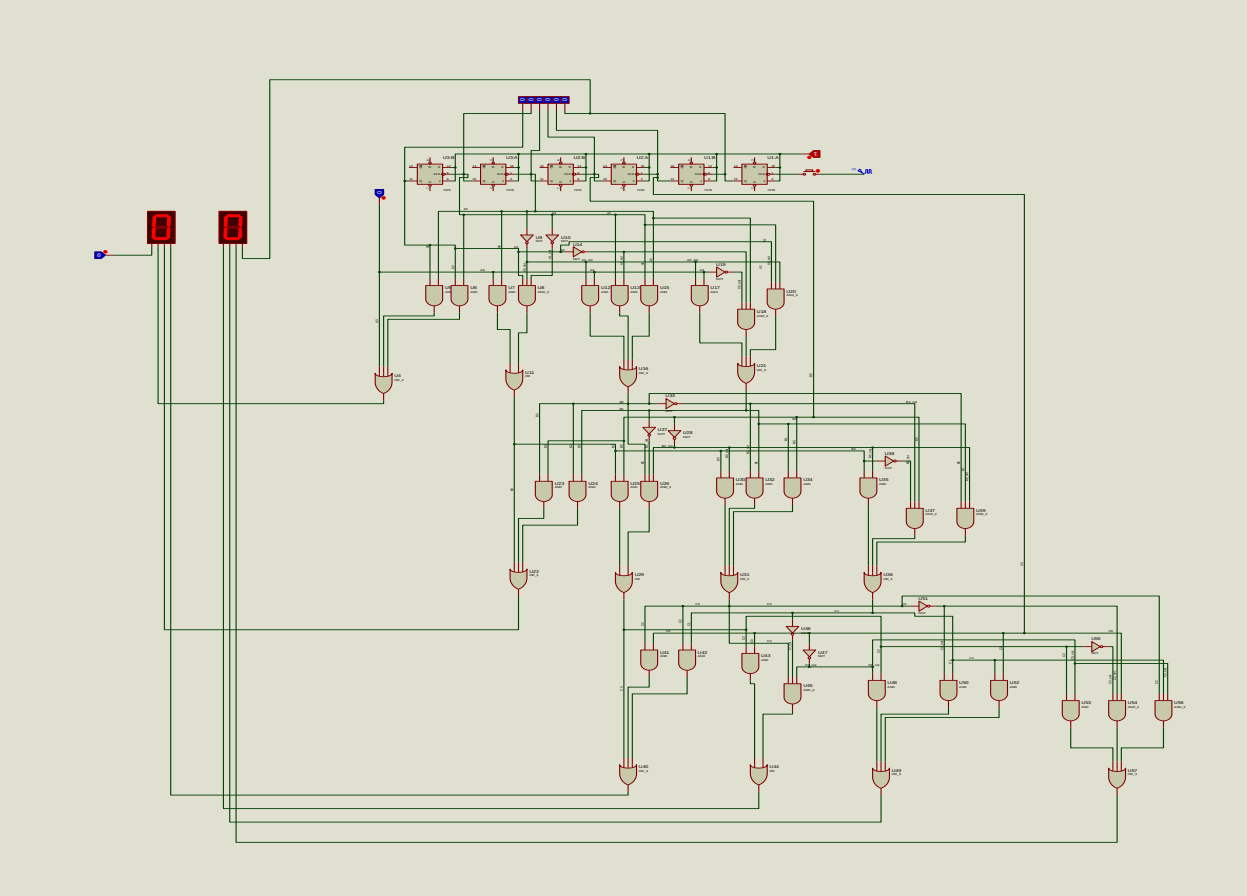
Learning Outcomes:

Through this project there is close understanding to devise a logic and how to build any circuit you want and how you can use basic gates to make your desired circuit and moreover through this, now I have more command on K-maps and deriving any circuit if asked. I also got to have more understanding of flip flops and how can I make counters and mod counters and basically now I am able to make any type of counter through flip flops.

How to Play It on Proteus:

To play this circuit on Proteus, open the given folder in which this circuit is present then hit the play button and then you will see that there will be no number generated in binary or either in decimal. To create a random number, you just have to press the push button, and then a random binary and its decimal form will be generated on the Big Probe and 7 Segment display

Complete Circuit Diagram:



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THE END