2. W65C22 FUNCTION DESCRIPTION

Table 2-1 W65C22 Memory Map of Internal Registers

Register Number	RS Coding				Register Designation	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
A	1	0	1	0	SR	Shift Register	
B	1	0	1	1	ACR	Auxiliary Control Register	
C	1	1	0	0	PCR	Peripheral Control Register	
D	1	1	0	1	IFR	Interrupt Flag Register	
E	1	1	1	0	IER	Interrupt Enable Register	
F	1	1	1	1	ORA/IRA	Same as Reg 1 except no "Handshake"	

2.1 Peripheral Data Ports

Both PA and PB operate in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the DDRA and DDRB specify which pins within the port bus are to be designated as inputs or outputs. Logic 0 in any bit position of the register will cause the corresponding pin to serve as an input; while a logic 1 will cause the pin to serve as an output.

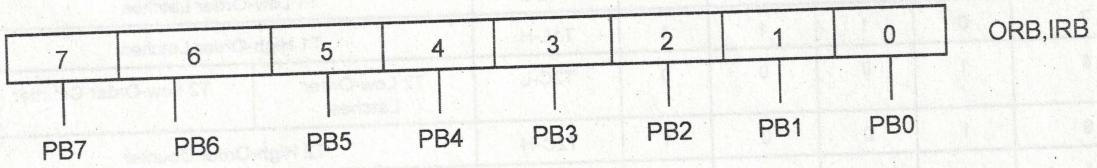
When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA & ORB). A Logic 1 in the ORA or ORB will cause the corresponding output line to go high, while logic 0 will cause the pin to go low. Under program control, data is written into the ORA or ORB bit positions corresponding to the output pins which have been programmed as outputs. Should data be written into bit positions corresponding to pins which have been programmed as input, the output pins will be unaffected.

When reading the Peripheral Port (PA or PB), the contents of the corresponding Input Register (IRA or IRB) is transferred onto the Data Bus. When the input latching feature is disabled, IRA will reflect the logic levels present on the PA bus pins. However, with input latching enabled and the selected active transition on Peripheral A Control 1 (CA1) having occurred, IRA will contain the data present on the PA bus lines at the time of the transition. In this case, once IRA has been read, it will appear transparent, reflecting the current state of the PA bus pins until the next CA1 latching transition.

With respect to IRB, it operates similar to IRA except that for those PB bus pins that have been programmed as outputs, there is a difference. When reading IRA, the logic level on the pins determines whether logic 1 or 0 is read. However, when reading IRB, the logic level stored in ORB is the logic level read. For this reason, those outputs which have large loading effects may cause the reading of IRA to result in the reading of a logic 0 when a 1 was actually programmed, and reading logic 1 when a 0 was programmed. However, when reading IRB, the logic level read will be correct, regardless of loading on the particular pin.

For information on formats and operation of the PA and PB registers, see Tables 2-2, 2-3 & 2-4. Note that the input latching modes are controlled by the Auxiliary Control Register (See Table 1-8).

Table 2-2 ORB, IRB Operation for Register 0 ($00)



Pin Data Direction Selection	WRITE	READ
DDRB="1" (Output)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no effect.
DDRB="0" (Input) (Input latching disabled)	MPU writes onto ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB="0" (Input) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.