Table 6-4 Operation, Operation Codes and Status Register

Mnemonic	Operation # Immediate Data ~ NOT → AND v OR ⊻ Exclusive OR	a	(a,x)	a,x	a,y	(a)	A	#	i	r	s	zp	(zp,x)	zp,x	zp,y	(zp)	(zp),y	Processor Status Register (P) *User Defined							
																		7	6	5	4	3	2	1	0
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	N	V	1	1	D	I	Z	C
ADC	A+M+C→A	6D		7D	79			69				65	61	75		72	71	N	V	.	.	.	.	Z	C
AND	A^M→A	2D		3D	39			29				25	21	35		32	31	N	.	.	.	.	.	Z	.
ASL	C←7 6 5 4 3 2 1 0←0	0E		1E			0A					06		16				N	.	.	.	.	.	Z	C
BBR0	Branch on bit 0 reset									0F								.	.	.	.	.	.	.	.
BBR1	Branch on bit 1 reset									1F								.	.	.	.	.	.	.	.
BBR2	Branch on bit 2 reset									2F								.	.	.	.	.	.	.	.
BBR3	Branch on bit 3 reset									3F								.	.	.	.	.	.	.	.
BBR4	Branch on bit 4 reset									4F								.	.	.	.	.	.	.	.
BBR5	Branch on bit 5 reset									5F								.	.	.	.	.	.	.	.
BBR6	Branch on bit 6 reset									6F								.	.	.	.	.	.	.	.
BBR7	Branch on bit 7 reset									7F								.	.	.	.	.	.	.	.
BBS0	Branch on bit 0 set									8F								.	.	.	.	.	.	.	.
BBS1	Branch on bit 1 set									9F								.	.	.	.	.	.	.	.
BBS2	Branch on bit 2 set									AF								.	.	.	.	.	.	.	.
BBS3	Branch on bit 3 set									BF								.	.	.	.	.	.	.	.
BBS4	Branch on bit 4 set									CF								.	.	.	.	.	.	.	.
BBS5	Branch on bit 5 set									DF								.	.	.	.	.	.	.	.
BBS6	Branch on bit 6 set									EF								.	.	.	.	.	.	.	.
BBS7	Branch on bit 7 set									FF								.	.	.	.	.	.	.	.
BCC	Branch C = 0									90								.	.	.	.	.	.	.	.
BCS	Branch if C=1									B0								.	.	.	.	.	.	.	.
BEQ	Branch if Z=1									F0								.	.	.	.	.	.	.	.
BIT	A ^ M	2C		3C				89				24		34				M_7	M_6	.	.	.	Z	.	.
BMI	Branch if N=0									30								.	.	.	.	.	.	.	.
BNE	Branch if Z=0									D0								.	.	.	.	.	.	.	.
BPL	Branch if N=0									10								.	.	.	.	.	.	.	.
BRA	Branch Always									80								.	.	.	.	.	.	.	.
BRK	Break										00							.	.	.	1	0	1	.	.
BVC	Branch if V=0									50								.	.	.	.	.	.	.	.
BVS	Branch if V=1									70								.	.	.	.	.	.	.	.
CLC	C → 0								18									.	.	.	.	.	.	.	0
CLD	0 → D								D8									.	.	.	.	0	.	.	.
CLI	0 → 1								58									.	.	.	.	.	0	.	.
CLV	0 → V								B8									.	0	.	.	.	.	.	.
CMP	A-M	CD		DD	D9			C9				C5	C1	D5		D2	D1	N	.	.	.	.	.	Z	C
CPX	X-M	EC						E0				E4						N	.	.	.	.	.	Z	C
CPY	Y-M	CC						C0				C4						N	.	.	.	.	.	Z	C
DEC	Decrement	CE		DE			3A					C6		D6				N	.	.	.	.	.	Z	.
DEX	X-1 → X								CA									N	.	.	.	.	.	Z	.
DEY	Y-1 → Y								88									N	.	.	.	.	.	Z	.
EOR	A v M → A	4D		5D	59			49				45	41	55		52	51	N	.	.	.	.	.	Z	.
INC	Increments	EE		FE			1A					E6		F6				N	.	.	.	.	.	Z	.
INX	X+1 → X								E8									N	.	.	.	.	.	Z	.
INY	Y+1 → Y								C8									N	.	.	.	.	.	Z	.
JMP	Jump to new location	4C	7C			6C												.	.	.	.	.	.	.	.

Mnemonic	Operation # Immediate Data ~ NOT ^ AND v OR xv Exclusive OR	a	(a,x)	a,x	a,y	(a)	A	#	i	r	s	zp	(zp,x)	zp,x	zp,y	(zp)	(zp),y	Processor Status Register (P) *User Defined							
																		7	6	5	4	3	2	1	0
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	N	V	1	1	D	I	Z	C
JSR	Jump to Subroutine	20																N	.	.	.	.	.	Z	.
LDA	M → A	AD		BD	B9			A9				A5	A1	B5		B2	B1	N	.	.	.	.	.	Z	.
LDX	M → X	AE			BE			A2				A6			B6			N	.	.	.	.	.	Z	.
LDY	M → Y	AC		BC				A0				A4		B4				N	.	.	.	.	.	Z	.
LSR	0 → 7 6 5 4 3 2 1 0 → C	4E		5E			4A					46		56				0	.	.	.	.	.	Z	C
NOP	No Operation								EA									.	.	.	.	.	.	.	.
ORA	A V M → A	0D		1D	19			09				05	01	15		12	11	N	.	.	.	.	.	Z	.
PHA	A → Ms, S-1 → S										48							.	.	.	.	.	.	.	.
PHP	P → Ms, S-1 → S										08							.	.	.	.	.	.	.	.
PHX	X → Ms, S-1 → S										DA							.	.	.	.	.	.	.	.
PHY	Y → Ms, S-1 → S										5A							.	.	.	.	.	.	.	.
PLA	S + 1→S, Ms → A										68							N	.	.	.	.	.	Z	.
PLP	S + 1→S, Ms → P										28							N	V	.	1	D	I	Z	C
PLX	S + 1→S, Ms → X										FA							N	.	.	.	.	.	Z	.
PLY	S + 1→S, Ms → Y										7A							N	.	.	.	.	.	Z	.
RMB0	Reset Memory Bit 0											07						.	.	.	.	.	.	.	.
RMB1	Reset Memory Bit 1											17						.	.	.	.	.	.	.	.
RMB2	Reset Memory Bit 2											27						.	.	.	.	.	.	.	.
RMB3	Reset Memory Bit 3											37						.	.	.	.	.	.	.	.
RMB4	Reset Memory Bit 4											47						.	.	.	.	.	.	.	.
RMB5	Reset Memory Bit 5											57						.	.	.	.	.	.	.	.
RMB6	Reset Memory Bit 6											67						.	.	.	.	.	.	.	.
RMB7	Reset Memory Bit 7											77						.	.	.	.	.	.	.	.
ROL	C←7 6 5 4 3 2 1 0 ← C	2E		3E			2A					26		36				N	.	.	.	.	.	Z	C
ROR	C→7 6 5 4 3 2 1 0 → C	6E		7E			6A					66		76				N	.	.	.	.	.	Z	C
RTI	Return from Interrupt										40							N	V	.	1	D	I	Z	C
RTS	Return from Subroutine										60							.	.	.	.	.	.	.	.
SBC	A - M - (~C) → A	ED		FD	F9			E9				E5	E1	F5		F2	F1	N	V	.	.	.	.	Z	C
SEC	1 → C								38									.	.	.	.	.	.	.	1
SED	1 → D								F8									.	.	.	.	1	.	.	.
SEI	1 → I								78									.	.	.	.	.	1	.	.
SMB0	Set Memory Bit 0											87						.	.	.	.	.	.	.	.
SMB1	Set Memory Bit 1											97						.	.	.	.	.	.	.	.
SMB2	Set Memory Bit 2											A7						.	.	.	.	.	.	.	.
SMB3	Set Memory Bit 3											B7						.	.	.	.	.	.	.	.
SMB4	Set Memory Bit 4											C7						.	.	.	.	.	.	.	.
SMB5	Set Memory Bit 5											D7						.	.	.	.	.	.	.	.
SMB6	Set Memory Bit 6											E7						.	.	.	.	.	.	.	.
SMB7	Set Memory Bit 7											F7						.	.	.	.	.	.	.	.
STA	A → M	8D		9D	99							85	81	95		92	91	.	.	.	.	.	.	.	.
STP	STOP (1→ PHI2)								DB									.	.	.	.	.	.	.	.
STX	X → M	8E										86			96			.	.	.	.	.	.	.	.