1st Year 2nd Semester

University of Dhaka

Department of Computer Science and Engineering

CSE-1204: Digital Logic Design Lab
Session: 2023-2024

Title of the Project:

Pressetable Digital Clock Implementation Using Synchronous Counters and 7-Segment Displays

Class Group: Odd

Lab Group: A-01

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Abstract

This project presents the design and implementation of a fully functional digital clock system using synchronous counter circuits and 7-segment display interfaces in the CircuitVerse simulation environment. The primary purpose is to create a real-time digital timekeeping system that displays hours, minutes, and seconds in a standard HH:MM:SS format using multiple 7-segment displays for clear visual representation.

The working principle is based on cascaded synchronous counters operating at different modulo values to achieve proper time counting. The system employs a base clock signal that drives a seconds counter (modulo-6 and modulo-10), which generates carry pulses to drive a minutes counter (also modulo-6 and modulo-10), which in turn provides carry signals to an hours counter (modulo-3 and modulo-10 for 24-hour format). Each counter stage consists of multiple flip-flops configured to count in BCD format, enabling direct interfacing with BCD-to-7-segment decoders.

The circuit incorporates six main counter modules representing tens and units of hours, minutes, and seconds, respectively. Each BCD output is connected to dedicated 7-segment display decoders that convert the 4-bit binary codes into appropriate segment control signals for the displays. The system includes proper reset functionality for time setting and synchronization. Besides, multiplexers and preset buttons are used to preset the clock at any time. The user has to give the number in the binary system to preset the clock.

Key outcomes include successful implementation of accurate timekeeping functionality, proper carry propagation between time units (seconds to minutes to hours), reliable BCD-to-7-segment decoding for all digits (0-9), and stable visual display representation. This digital clock demonstrates fundamental concepts in sequential logic design, timing circuits, and practical applications of counters in real-world systems.

Circuit Diagram

Digital Clock Circuit Implementation in CircuitVerse:

The circuit shows a comprehensive digital clock system with the following structure from right to left:

Time Display Units:

- **Seconds Display**: Two 7-segment displays showing tens and units of seconds (00-59)
- **Minutes Display**: Two 7-segment displays showing tens and units of minutes (00-59)
- **Hours Display**: Two 7-segment displays showing tens and units of hours (00-23)

Counter Architecture:

- **Seconds Counter**:
  - Units counter (0-9) with modulo-10 operation
  - Tens counter (0-5) with modulo-6 operation for proper 60-second cycle
- **Minutes Counter**:
  - Units counter (0-9) with modulo-10 operation
  - Tens counter (0-5) with modulo-6 operation for proper 60-minute cycle
- **Hours Counter**:
  - Units counter (0-9) with modulo-10 operation
  - Tens counter (0-2) with modulo-3 operation for 24-hour format

Signal Flow:

- **Master Clock**: Base timing signal (typically 1 Hz for real-time operation)
- **Carry Chain**: Overflow signals connecting seconds→minutes→hours
- **Reset Logic**: System-wide reset for time setting
- **Display Decoders**: BCD-to-7-segment conversion for each digit

Control Elements:

- **Clock Input**: Primary timing source
- **Preset Button**: For time initialization
- **Enable Signals**: Individual counter stage control

Presetting the clock:

- The clock can be preset at each block.
- The preset button is used for this purpose.
- The number being used for the preset is given by the user in binary.
  -

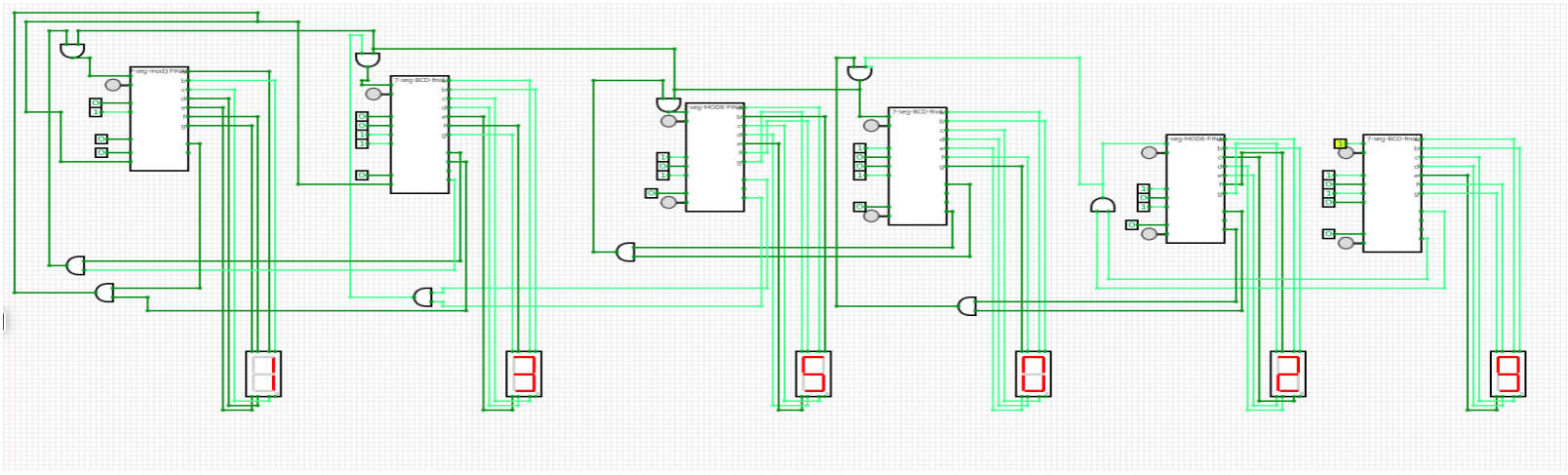

FIG: Presettable Digital Clock

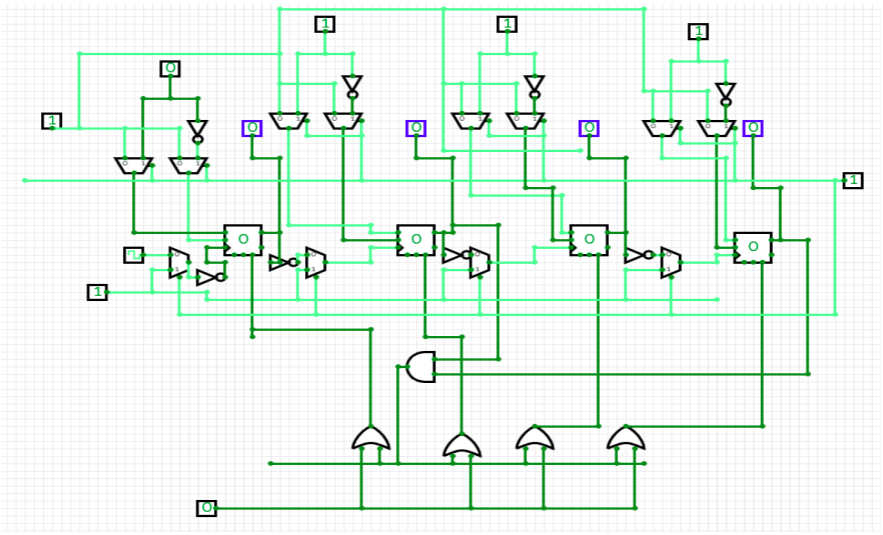

FIG: Pressetable Synchronous Counter

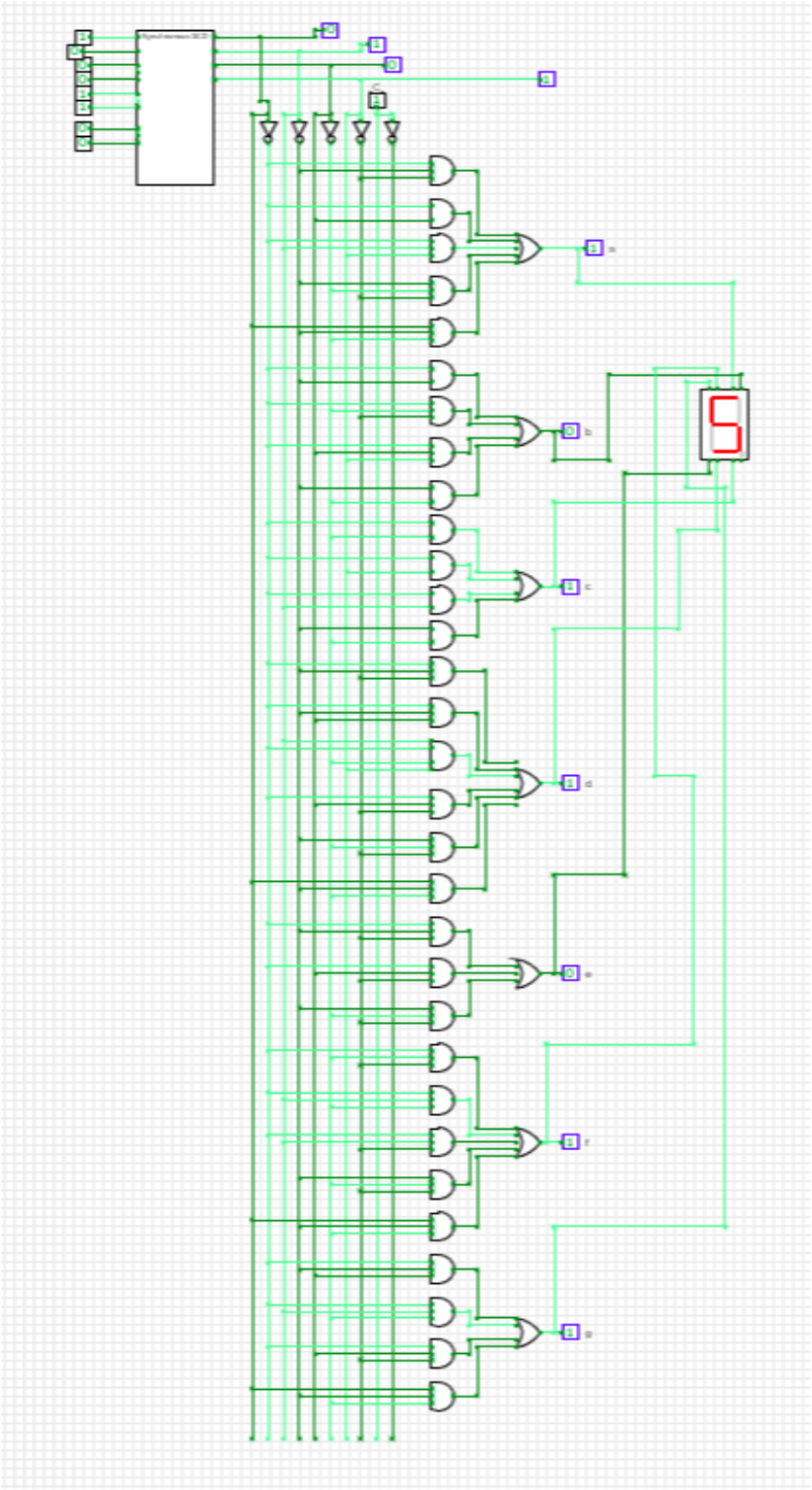

FIG: 7-Segment Display

List of Apparatus

Digital Logic Components:

1. **JK Flip-Flops**: 24 units total
    - 4 units per BCD counter
    - 6 BCD counters (2 each for hours, minutes, seconds)
2. **BCD-to-7-Segment Decoders**: 6 units
    - Individual decoder for each time digit display
3. **7-Segment Displays**: 6 units
    - 2 displays for hours (HH)
    - 2 displays for minutes (MM)
    - 2 displays for seconds (SS)
4. **Clock Generator**: 1 unit
    - 1 Hz frequency for real-time operation
    - Adjustable for testing purposes

5. **Multiplexer**:
    - Used for preset in synchronous mod-10 counter, mod-6 counter, and mod-3 counter.
    - First, the clock has to be stopped. Then it is preset to the number, given by the user in the binary system.
    - Using the preset button, the clock is preset to the desired number.
    - Finally, the clock is made to run.

Logic Gates:

6. AND Gates: Multiple units
- Carry generation logic
- Reset logic implementation
- Counter overflow detection

7. OR Gates: Multiple units
- Signal combination
- Reset distribution

8. NOT Gates: Multiple units
- Signal inversion
- Logic complementation

9. NAND Gates: Multiple units
- Alternative logic implementation
- Reset logic

Control Circuits:

10. **Reset Circuit**: 1 unit
    - Manual time setting capability
    - System initialization
11. **Modulo Logic Circuits**: 6 units
    - Modulo-10 for unit digits
    - Modulo-6 for tens of seconds and minutes
    - Modulo-3 for tens of hours (24-hour format)

Simulation Environment:

12. **CircuitVerse Digital Logic Simulator**
    - Web-based simulation platform
    - Real-time circuit simulation
    - Interactive testing environment
13. **Timing Analysis Tools**
    - Built-in timing diagram generation
    - Signal monitoring capabilities
    - Performance verification

Project Files and Documentation:

14. **Circuit Modules**:
    - Main circuit file
    - Sub-circuit modules (Synchronous BCD, 7-seg-BCD-final, etc.)
15. **Test Benches**:
    - Functional verification setups
    - Timing validation circuits

Technical Specifications:

- **Display Format**: HH:MM: SS (6-digit time display)
- **Counting Range**: 00:00:00 to 23:59:59 (24-hour format)
- **Update Rate**: 1 second intervals
- **Reset Capability**: Manual and automatic reset functions
- **Power Requirements**: Digital logic levels (simulated environment)
- **Presetting option:** Can be given using a binary number.