# Practice 1: Semi-Classical Monte Carlo Simulation of a Ballistic Transistor

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In the present report we summarize some of the results of interest obtained after manipulating the *transistor_MG.txt* scenario offered under the *examples* directory by the Bitlles software [1], following the practice guide. We employ the semi-classical mechanics module of the Bitlles simulator, where the electrons in the device are taken to be semi-classical point-like particles that obey effective mass Newton's laws and are affected by a self-consistent electric potential energy field given by the solution of the Poisson equation, using the positions of the electrons and fixed boundary conditions. Then, parameters like the instantaneous drain-source current $I_{DS}$ are computed in each time-step by counting the amount of discrete charges that cross a particular transversal section of the device. These electrons are likely injected from the source and drain following the probablity density given by the product of the Fermi-Dirac and density of states of the semiconductor.

## 1 Current-Voltage Characteristic Curves

We sweep the drain to source voltage fall $V_{DS}$ in the range (0,0.3) V in order to capture both the linear and the saturation regime of the transistor, where the transistor behaves respectively, as a gate voltage $V_{GS}$ controlled resistance or as an ideal current source. We do so for several values of gate voltage $V_{GS}$ in the range (-3.5, -0.1) V. For each combination $(V_{DS}, V_{GS})$, the simulator gives us the instantaneous current $I_{DS}$ in time, computed with the electron trajectories. These can be seen for each case in Figure 1, first column[1]. In order to emulate what we could measure with an ammeter, we compute the cumulative time averages, as seen in Figure 2, second column. Clearly, the current $I_{DS}$ approaches a stable average value for a not that long averaging window. This is the classically predicted current $I_{DS}$. We then plot in Figure 1, third column, the set of average current vs $V_{DS}$ curves obtained with them. Note that we also plot the standard deviation of each estimate. This noise represents the, so called, partition noise, due to the fact (at least in the simulator) that the charge elements employed to compute the current are in fact discrete packets in space, which can be reflected or not by the gate barrier. In Figure 1 fourth column, we represent the normalized auto-correlation $< I(t)I(t+\tau) >$ of each instantaneous current time series for different lags $\tau$, such that the ordinate axis represents its estimator, where:

$$< I(t)I(t+\tau) >= \frac{\mathbb{E}\Big[\Big(I_{DS}(t) - \mathbb{E}[I_{DS}]\Big)\Big(I_{DS}(t+\tau) - \mathbb{E}[I_{DS}]\Big)\Big]}{\mathbb{V}ar[I_{DS}]} \tag{1}$$

with $\mathbb{E}[\cdot]$ the time-series expectation and $\mathbb{V}ar[\cdot]$ the variance.

We see that the values of instantaneous current for successive time elements are strongly correlated for small lags. But when the average current is not close to zero (for rows c,d,e,f), even for more displaced lags the auto-correlation is still non-zero. These indicate that the apparently disconnected currents in time, shown in Figure 1 column one, are actually statistically connected in time, where the current at each time is statistically linked to the one at the next and the previous time. In a sense, this is a signature of a sort of non-Markovianity. That is, the fluctuations in the current are not due to a random independent variable at each time, not even they depend only on what value they had in the previous time, but they depend on the history of values taken previously. This is in agreement with the fact that, as far as the simulator is concerned, the process describing the current (the trajectories of the electrons) have a continous and deterministic nature.

[1] All the plots and post-processing was done using an ad hoc Python-script, whcich can be found in the Github repository of the practice [2].

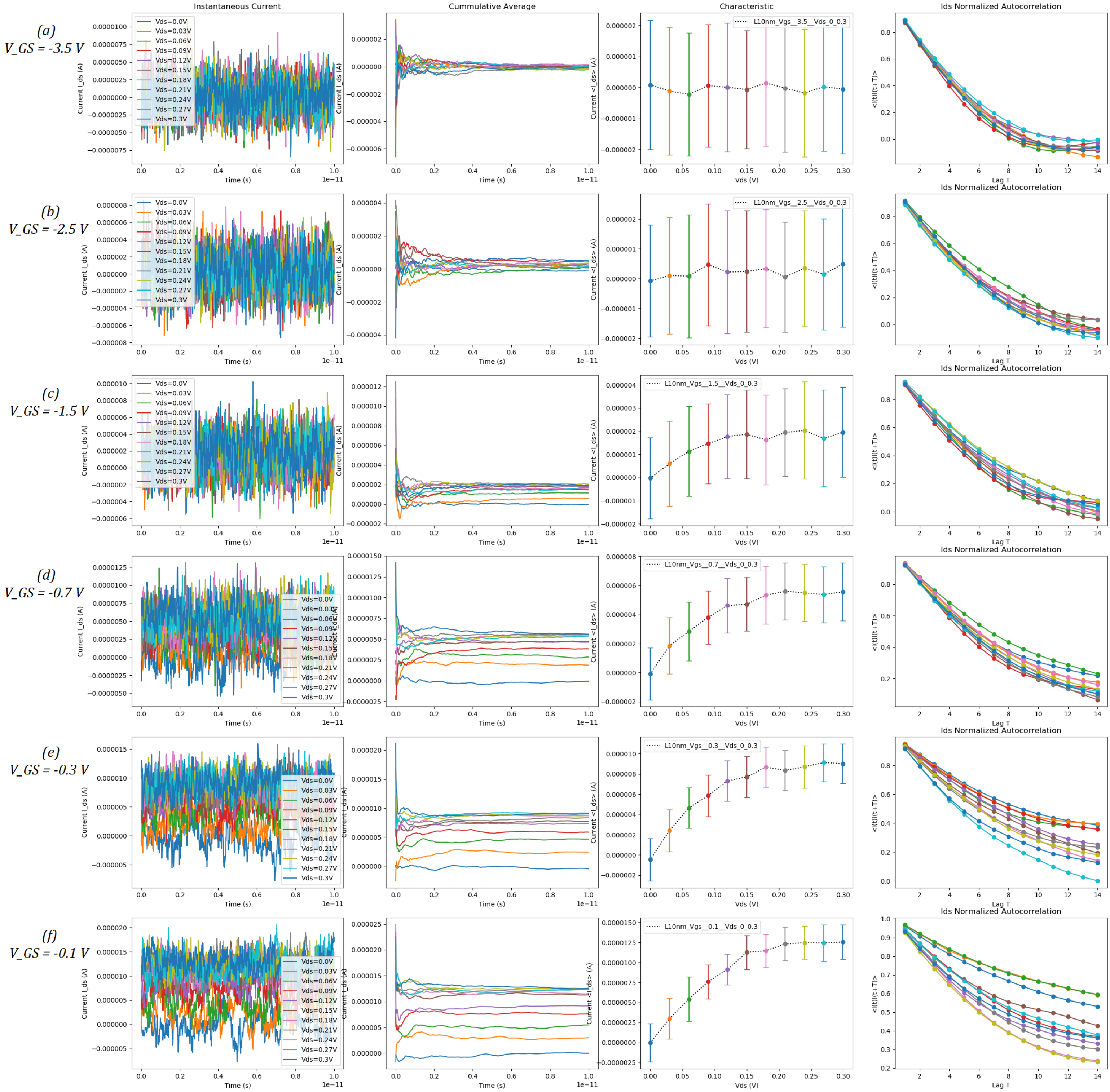



**Figure 1:** Data obtained simulating a total time of $10^{-11}s$, a single gate and a channel length of 10 nm. The first column shows instantaneous $I_{DS}$ current values at each simulation time for each of the $V_{DS}$ shown in the inset. The second column shows the cummulative avergaes of each instantaneous current curve. The third column shows the $10^{-11}s$ window time average of the instantaneous currents with the bars representing standard deviation. The fourth column shows the normalized autocorrelation of each time series for several different lags. The color code is preserved in each row, which is indicated in the insets of the first column.

We plot in Figure 2 the $I_{DS}$ vs $V_{DS}$ characteristic curves so obtained, for different gate voltages $V_{GS}$. We can clearly grasp even for these nanometric transistors the classical transistor characteristics, with the linear and saturation regimes, with a gate that is capable of switching-off the drain to source current.

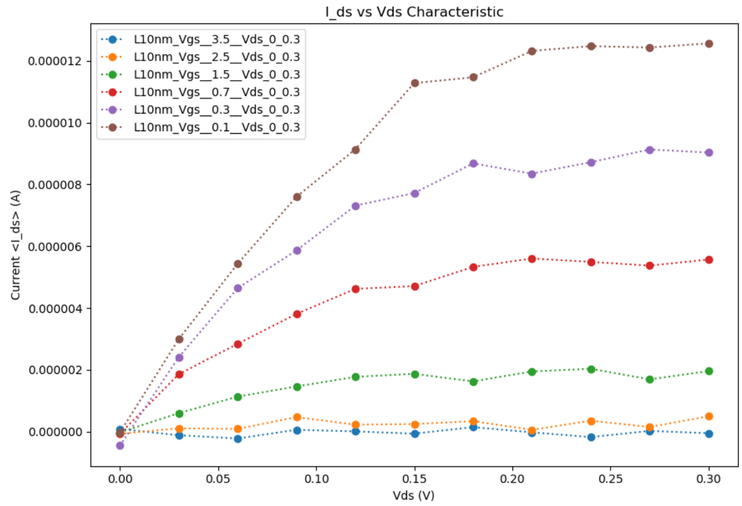



**Figure 2:** Time averaged $I_{DS}$ vs $V_{DS}$ characteristics for several different $V_{GS}$ (time average taken over $10^{-11}s$). The $V_{GS}$ value of each curve is $\{-3.5, -2.5, -1.5, -0.7, -0.3, -0.1\}$V respectively for colors $\{blue, orange, gree, red, violet, brown\}$. Data employed simulating a total time of $10^{-11}s$, a single gate and a channel length of 10 nm.

Finally, in Figure 3 we find the $I_{DS}$ vs $V_{GS}$ characteristic curves, as a function of $V_{DS}$, where we see that there is a range of threshold voltages such that only above them the current is made meaningful, irrespective of the $V_{DS}$ voltage.

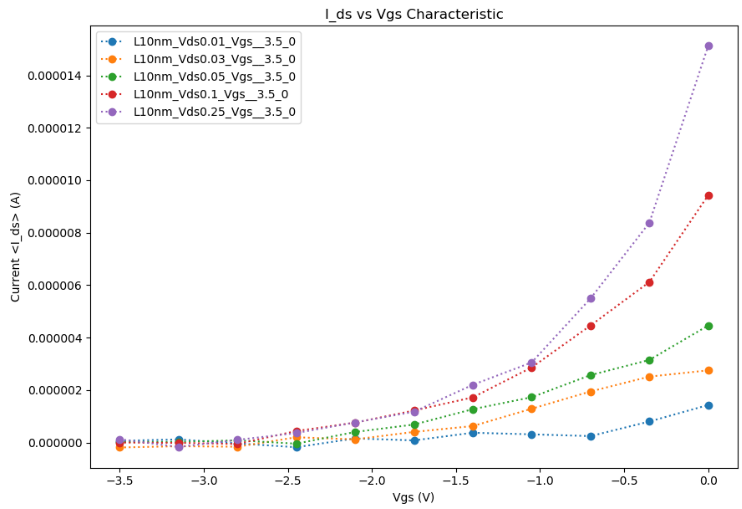
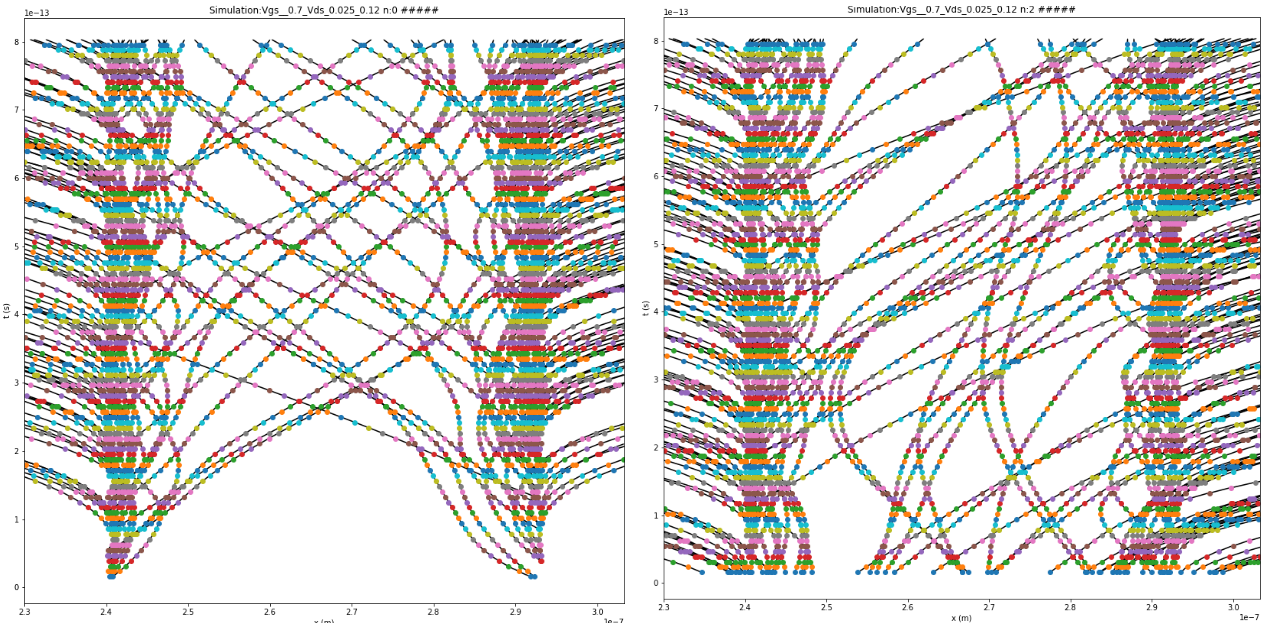



**Figure 3:** Time averaged $I_{DS}$ vs $V_{GS}$ characteristics for several different $V_{DS}$ (time average taken over $10^{-11}s$). The $V_{GS}$ value of each curve is $\{0.01, 0.03, 0.05, 0.1, 0.25\}$V respectively for colors $\{blue, orange, gree, red, violet\}$. Data employed simulating a total time of $10^{-11}s$, a single gate and a channel length of 10 nm.

## 2 Electron dwell time and the Current

Using the trajectory information of the simulations, we can estimate the dwell time of the electrons, as the time taken by an electron to literally cross the channel. If we then take the number of such electrons crossing the channel in a time interval, we could estimate the current through the channel, which should be compatible with the predicted $I_{DS}$.




**(a)** **(b)**

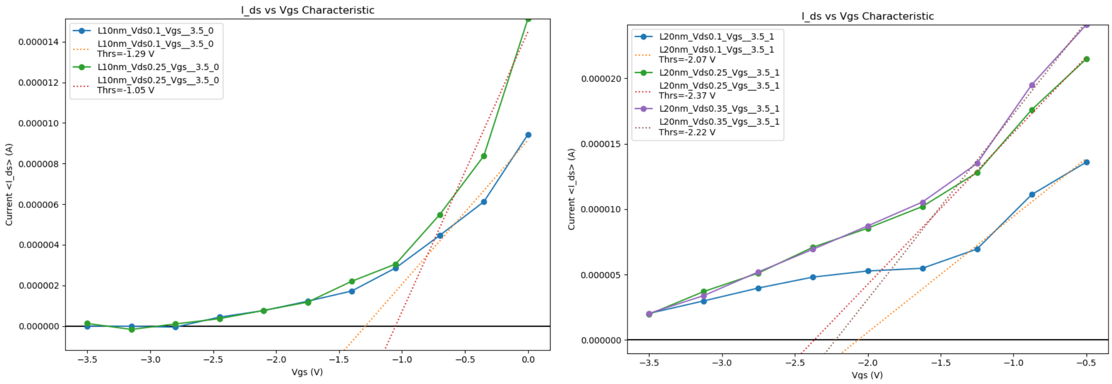
**Figure 4:** Space-time diagram for the electrons simulated using a fixed $V_{GS} = -0.7V$ and $V_{DS} \in \{0.025, 0.12\}$ for subfigures (a) and (b) respectively. The x axis represents the position along the channel, with the source in the left and the drain in the right (in units of $10^{-7}m$), while the y axis represents time (in units of $10^{-13}$s). The trajectories are reconstructed using the instantaneous velocity vector of the electrons.

We plot the space-time diagram along the channel length $x$, for two different cases of $V_{DS} \in \{0.025, 0.12\}$ and a fixed $V_{GS} = -0.7$, as can be seen in Figure 4. For the first case, we found an average $1.23 \cdot 10^{-6}$A current, and turns out, we can count in Figure 4 that about 6 electrons cross the channel (discounting the electrons that cross in the reverse direction) in the plotted time interval of $8 \cdot 10^{-13}s$. This would amount an estimated current of $1.2 \cdot 10^{-6}$A, in surprising agreement with the average one. We can also compute the average dwell time of the plot as $8 \cdot 10^{-13}s/6 = 1.33 \cdot 10^{-13}s$.

For the second case of Figure 4, we found an average current of $4.71 \cdot 10^{-6}$A, and in the figure, we can count that about 25 electrons cross the channel in the $8 \cdot 10^{-13}s$ range. This amounts an estimated current of $5 \cdot 10^{-6}A$, in excellent agreement with the average one. Finally, we can estimate the dwell time of the electrons in this case as $8 \cdot 10^{-13}s/25 = 3.2 \cdot 10^{-14}s$

## 3 Short Channel Effects

In Figure 5, we fit some lines to the $I_{DS}$ vs $V_{GS}$ curves of Figure 3 in their "transistor on" regime, in order to estimate the threshold voltage. The threshold voltage turns out to be quite different for each $V_{DS}$ voltage. This is a clear signature of the short-channel effects, since it is mainly due to the drain induced barrier lowering, where the equi-potentials of the drain voltage modify the lines that should be exculsively controlled by the gate. Nonetheless, we can estimate an average threshold voltage to be of -1.17 V, with a standard deviation of 0.119 V. It turns out that by making the length of the transistor longer, the standard deviation of the threshold voltages is reduced, which proves that it is indeed a short channel effect. In particular, with a length of $L = 20$ nm, the average threshold voltage is of -2.22V, with a now lower standard deviation of 0.098V.




**(a)** **(b)**

**Figure 5:** Time averaged $I_{DS}$ vs $V_{GS}$ characteristics for several different $V_{DS}$ (time average taken over $10^{-11}s$ for (a) and $2.5 \cdot 10^{-11}s$ for (b)). In (a) the channel length of the single gate transistor was set to 10 nm, while in (b) it was set to 20 nm. The $V_{GS}$ value of each curve is $\{0.1, 0.25\}$V respectively for colors $\{blue, orange\}$. Each curve has a fitted line in the "on" regime the intercept of which at $I_{DS} = 0$A estimates the threshold voltage.

In addition to the varying threshold voltage due to the intrusion of the drain voltage in the gate barrier, we can appreciate another short-channel effect by noticing that in the saturation region of the $I_{DS}$ vs $V_{DS}$ curves, the transistor is a non-ideal source, featuring a non-infinite resistance, which is increased (made more ideal) with a gate that has a greater influence on the channel. As plotted in Figure 6, the resistance of the ideally infinite resistance current source regime is invariably increased by surrounding the channel with more gates.

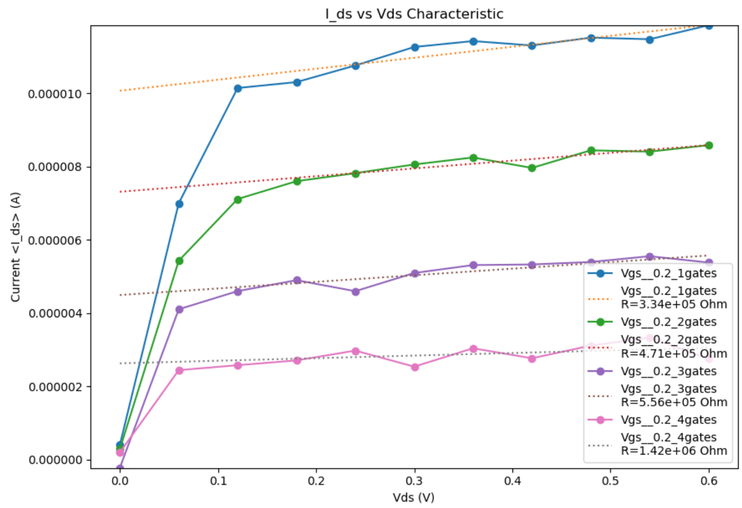
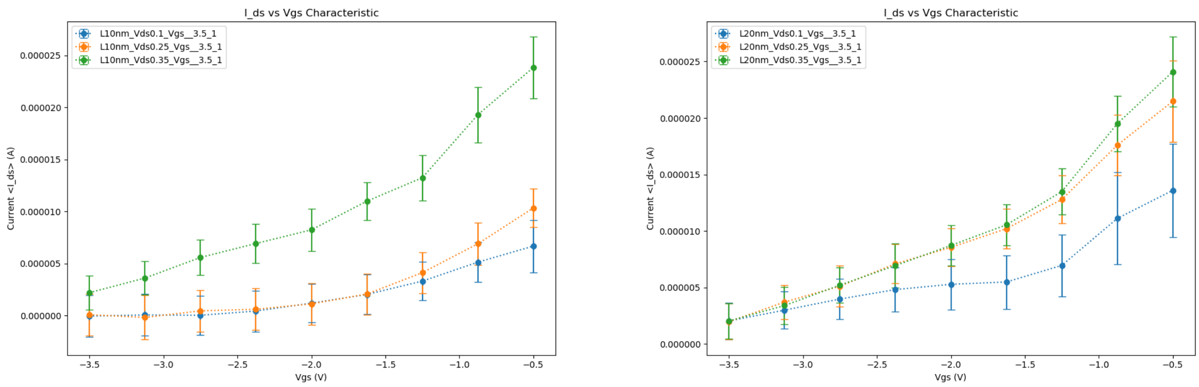



**Figure 6:** Time averaged $I_{DS}$ vs $V_{DS}$ characteristics for a same $V_{GS} = -0.2V$ on a 10 nm channel length, but an increasing number of gates surrounding the channel, where each gate is in a face of the prism channel (time averages taken over $10^{-11}s$). The gate number of each curve is $\{1, 2, 3, 4\}$ respectively for colors $\{blue, green, violet, pink\}$. To each curve a line is fitted in the saturation regime, the inverse of the slope of which gives us the resistance of each channel. Respectively for gate numbers $\{1, 2, 3, 4\}$, we obtain $\{3.34e5, 4.71e5, 5.56e5, 1, 42e6\}$, which increases monotonously, showing the greater control of the gate on the channel.

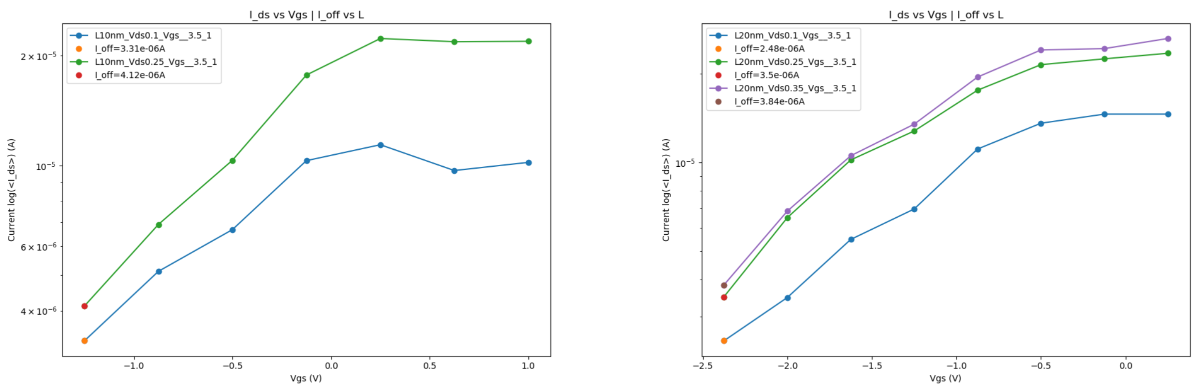
One could expect that the smaller the channel length of the nanotransistor, the partition noise would be more notable because less electrons would be present inside the channel at each time. This could be seen also as a sort of short channel effect. However, we find that the opposite appears in our simulations. After simulating the same transistor as the one of Figure 3, but now with length $L = 20$ nm, as it can be seen in Figure 7, the standard deviation of the instantaneous currents appear to be smaller for the shorter channel transistor. Be this or the opposite, if real experiments show a fixed trend for the partition noise when approaching the quantum regime, this could be an indicator of some sort of (perhaps Bohmian) particle nature of the electrons.




**(a)** **(b)**

**Figure 7:** Time averaged $I_{DS}$ vs $V_{GS}$ characteristics for several different $V_{DS}$ (time average taken over $10^{-11}s$ for (a) and $2.5 \cdot 10^{-11}s$ for (b)). In (a) the channel length of the single gate transistor was set to 10 nm, while in (b) it was set to 20 nm. The $V_{GS}$ value of each curve is $\{0.1, 0.25, 0.35\}$V respectively for colors $\{blue, orange, green\}$. The error bars show the standard deviation of the instantaneous currents.

Finally, in Figure 8, the intensity is plotted in logarithmic scale for the two transistor channel lengths, in order to acknowledge that there is a non-zero current flow even at a gate voltage in the theoretical "off" regime (below the average threshold voltage we found for each case in Figure 5), as long as $V_{DS}$ is non-zero. These are the so-called "off currents". It turns out that such currents are smaller (for a fixed $V_{DS}$) the longer the channel of the transistor. Thus, it seems that it may also be a short channel effect. Indeed, they are likely due to the lowering of the barrier induced by the drain voltage, which is more relevant the shorter the channel.




**(a)** **(b)**

**Figure 8:** Time averaged $I_{DS}$ vs $V_{GS}$ characteristics for several different $V_{DS}$ (time average taken over $10^{-11}s$ for (a) and $2.5 \cdot 10^{-11}s$ for (b)). In (a) the channel length of the single gate transistor was set to 10 nm, while in (b) it was set to 20 nm. The $V_{GS}$ value of each curve is $\{0.1, 0.25, 0.35\}$V respectively for colors $\{blue, orange, violet\}$. the $I_{off}$ currents of each case are defined below the threshold voltage obtained in Figure 4.

# References


[1] G. Albareda, D. Marian, A. Benali, A. Alarcón, S. Moises, and X. Oriols, "Bitlles: Electron transport simulation with quantum trajectories," *arXiv preprint arXiv:1609.06534*, 2016.

[2] "Github repository with the python script generated for the post-simulation data treatment." https://github.com/Oiangu9/_Miscellaneous/tree/main/NIC.