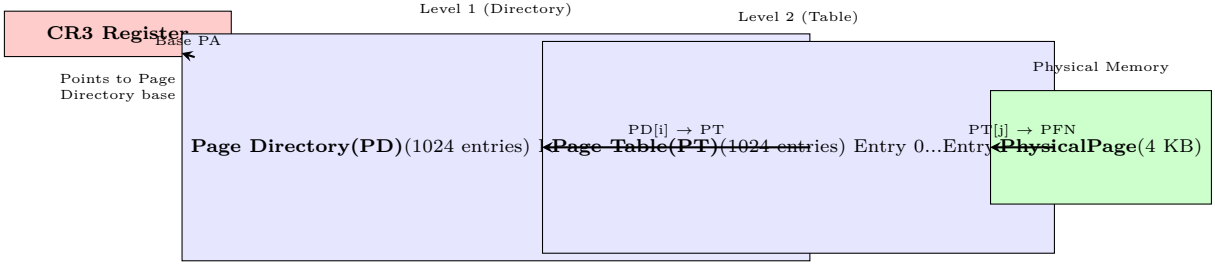
i386 2-Level Paging Hierarchy

Virtual Address (32-bit)

[31:22]	[21:12]	[11:0]
10 bits	10 bits	12 bits
PDE Index	PTE Index	Offset



Translation Steps:
1. VA[31:22] = PD index (i)
2. PD[i] → PT base addr
3. VA[21:12] = PT index (j)
4. PT[j] → page frame
5. VA[11:0] = offset
6. PA = frame + offset

Page Directory Entry (32-bit):
- [31:12] Page table base address
- [11:9] Available for OS use
- [8] Global (if CR4.PGE=1)
- [7] Page Size (0=4KB, 1=4MB)
- [6] Reserved (0)
- [5] Accessed
- [4] Cache disable (PCD)
- [3] Write-through (PWT)
- [2] User/Supervisor
- [1] Read/Write
- [0] Present

Page Table Entry (32-bit):
- [31:12] Physical frame address
- [11:9] Available for OS
- [8] Global page
- [7] Reserved (0)
- [6] Dirty (written)
- [5] Accessed
- [4] Cache disable
- [3] Write-through
- [2] User/Supervisor
- [1] Read/Write
- [0] Present

TLB Caches Translations
2 table lookups avoided on TLB hit (1 cycle) vs 2 memory accesses (200+ cycles)

Page Sizes:
- 4 KB (standard)
- 4 MB (PSE bit)

Address Space:
- 32-bit: 4 GB max

i386 Constants:
I386_VM_DIR_ENTRIES: 1024
I386_VM_PT_ENTRIES: 1024
I386_VM_DIR_ENT_SHIFT: 22
I386_VM_PT_ENT_SHIFT: 12
I386_PAGE_SIZE: 4096

MINIX i386 Details:
Standard 2-level paging
PSE enabled (CR4.PSE)
4 MB kernel mappings
1024 entries per level
Defined in vm.h:34,38