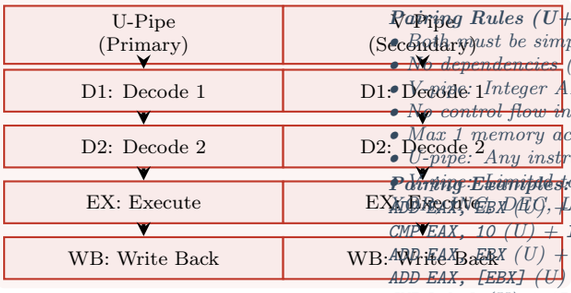
Intel Pentium (P5) Microarchitecture

First Superscalar x86 - Dual-Issue Pipeline (1993)

Specifications: 60-200 MHz, 3.1-3.3M transistors (0.8-0.35 µm), 273-pin PGA, 8 KB L1 I-cache + 8 KB L1 D-cache, 64-bit data bus, 32-bit address bus (4 GB physical), Superscalar (2-way), Branch prediction, APIC, FPU integrated, RDTSC instruction

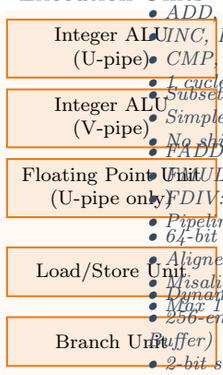
Dual-Issue Superscalar Pipeline



Pairing Rules (U+V):
- *Pair must be simple (no complex addressing)*
- *No dependencies (RAW, WAR, WAW)*
- *V-pipe: Integer ALU only (no FPU, no shifts)*
- *No control flow in V-pipe*
- *Max 1 memory access per pair*
- *U-pipe: Any instruction*
- *Pairing Eligible: MOV, ADD, SUB, CMP, AND, OR, XOR, INC, DEC, LEA*

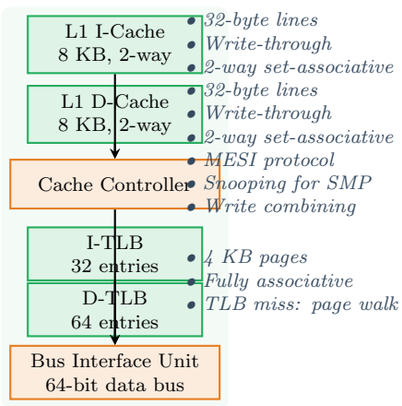
Pairing Examples:
- `ADD EAX, EBX` *(U)* + `MOV ECX, EDX` *(V)*
- `CMP EAX, 10` *(U)* + `INC EBX` *(V)*
- `ADD EAX, EBX` *(U)* + `SHL ECX, 4` *(V)* - *shift not allowed*
- `ADD EAX, [EBX]` *(U)* + `MOV ECX, [EDX]` *(V)* - *2 mem ops*
- `JMP label` *(U)* + `ADD EAX, EBX` *(V)* - *control flow*

Execution Units



- *ADD, SUB, AND, OR, XOR*
- *INC, DEC, NEG, NOT*
- *CMP, TEST*
- *1 cycle latency*
- *Subset of U-pipe ops*
- *Simple ops only*
- *No shifts, no multiply*
- *FADD: 3 cycles*
- *FMUL: 3 cycles*
- *FDIV: 39 cycles (FDIV bug!)*
- *Pipelined (3-stage)*
- *64-bit data bus*
- *Aligned access: 1 cycle*
- *Misaligned: 2 cycles*
- *Dynamic branch prediction*
- *Max 1 memory op per clock*
- *256-entry BTB (Branch Target Buffer)*
- *2-bit saturating counter*
- *Misprediction penalty: 3-4 cycles*

Cache Hierarchy



- *32-byte lines*
- *Write-through*
- *2-way set-associative*
- *32-byte lines*
- *Write-through*
- *2-way set-associative*
- *MESI protocol*
- *Snooping for SMP*
- *Write combining*
- *4 KB pages*
- *Fully associative*
- *TLB miss: page walk*

Register File

MMX Registers: *(added in Pentium MMX, 1997)*
- *MM0-MM7 (64-bit each)*
- *Aliased to FPU stack (no extra state)*
- *SIMD operations (Single Instruction, Multiple Data)*

Data Types:
- *8x 8-bit integers (packed bytes)*
- *4x 16-bit integers (packed words)*
- *2x 32-bit integers (packed dwords)*
- *1x 64-bit integer (quadword)*

Instructions:
- *PADDB/W/D: Packed add*
- *PSUBB/W/D: Packed subtract*
- *PMULL/H: Packed multiply*
- *PAND/OR/XOR: Packed logical*
- *PSLL/RL/RA: Packed shift*

Use Cases:
- *Graphics (pixel operations)*
- *Video encoding/decoding*
- *Audio processing*
- *Image filtering*

New in Pentium

***RDTSC** instruction*
Reads cycle counter
High-res timing
Ring 3 accessible

RDTSC Instruction Usage

Assembly:
```
rdtsc ; Read timestamp counter
; EDX:EAX = 64-bit cycle count
```
C Usage:
```
static inline uint64_t rdtsc(void) {
  uint32_t lo, hi;
  asm volatile("rdtsc":"=a"(lo),"=d"(hi));
  return ((uint64_t)hi << 32) | lo;
}
```
Timing Example:
```
uint64_t start = rdtsc();
/* code to measure */
uint64_t end = rdtsc();
printf("Cycles: %llu", end - start);
```

APIC (Advanced Programmable Interrupt Controller)

Features:
- *Per-CPU interrupt handling*
- *Inter-Processor Interrupts (IPI)*
- *Local timer interrupt*
- *Performance monitoring counter*
- *Thermal sensor interrupt*

Registers (MMIO):
- *Mapped at 0xFEE00000*

I/O APIC I/O APIC (External)
- *Externgl chip (on motherboard),*
- *Routes IRQs to Local APICs*
- *Supports up to 24 IRQs*
- *Programmable routing*
- *Edge or level-triggered*

Pentium FDIV Bug (1994)

Description: *Floating-point division bug in early Pentium (60-100 MHz) caused incorrect results for certain inputs.*
Example: `4195835.0 / 3145727.0` *should give* `1.333820449136241002` *but Pentium returned* `1.333739068902037589`
Root Cause: *Lookup table in FPU had 5 missing entries (out of 1066). Used in SRT division algorithm.*
Impact: *Intel initially downplayed issue ("affects 1 in 9 billion divisions"). Public outcry forced full recall.*
Cost: *$475 million USD replacement program. Major PR disaster for Intel.*
Detection: `cpuid` *instruction returns family=5, model=1 or 2. Check for errata via BIOS update or OS flag.*
Workaround: *Linux kernel detects and disables FPU if bug present, uses software floating-point emulation.*
Fixed: *Pentium 75 MHz and later (stepping C1 and beyond) have corrected lookup table.*

Performance Characteristics

IPC (Instructions Per Cycle):
- *Single-issue code: 0.5-0.8 IPC*
- *Dual-issue optimized: 1.5-1.8 IPC*
- *Ideal (all pairs): 2.0 IPC*

Latencies:
- *Integer ADD/SUB: 1 cycle*
- *Integer MUL: 10 cycles (non-pipelined)*
- *FP ADD: 3 cycles (pipelined)*
- *FP MUL: 3 cycles (pipelined)*
- *FP DIV: 39 cycles (non-pipelined)*
- *L1 cache hit: 1 cycle*
- *L1 cache miss (to memory): 30-50 cycles*

Branch Prediction:
- *Prediction rate: 80-90% (depends on code)*
- *Misprediction penalty: 3-4 cycles*
- *No speculative execution (unlike P6)*

Pentium vs 486:
- *2x performance on integer code (dual-issue)*
- *3-5x performance on FP code (pipelined FPU)*
- *Better branch prediction*
- *Larger caches (8KB vs 8KB unified on 486)*
- *Faster bus (60-66 MHz vs 33 MHz)*

Pentium Variants:
- *Pentium 60/66: 0.8 µm, 5V, 3.1M transistors*
- *Pentium 75-200: 0.6-0.35 µm, 3.3V, split voltage*
- *Pentium MMX: 0.35 µm, 2.8V, 4.5M transistors*
- *Pentium OverDrive: Socket upgrade for 486*

System Integration:
- *Socket 4 (Pentium 60/66, 273-pin PGA)*
- *Socket 5 (Pentium 75-200, 320-pin SPGA)*
- *Socket 7 (Pentium MMX, 321-pin SPGA)*
- *Chipsets: 430FX (Triton), 430HX, 430VX*

Operating Systems:
- *DOS (16-bit real mode)*
- *Windows 3.x (16-bit protected mode)*
- *Windows 95/98/NT (32-bit)*
- *Linux 1.x+ (full 32-bit support)*
- *MINIX 3 (uses protected mode, paging)*

Compilers:
- *GCC: -march=pentium*
- *MSVC: /G5*
- *ICC: -mtune=pentium*