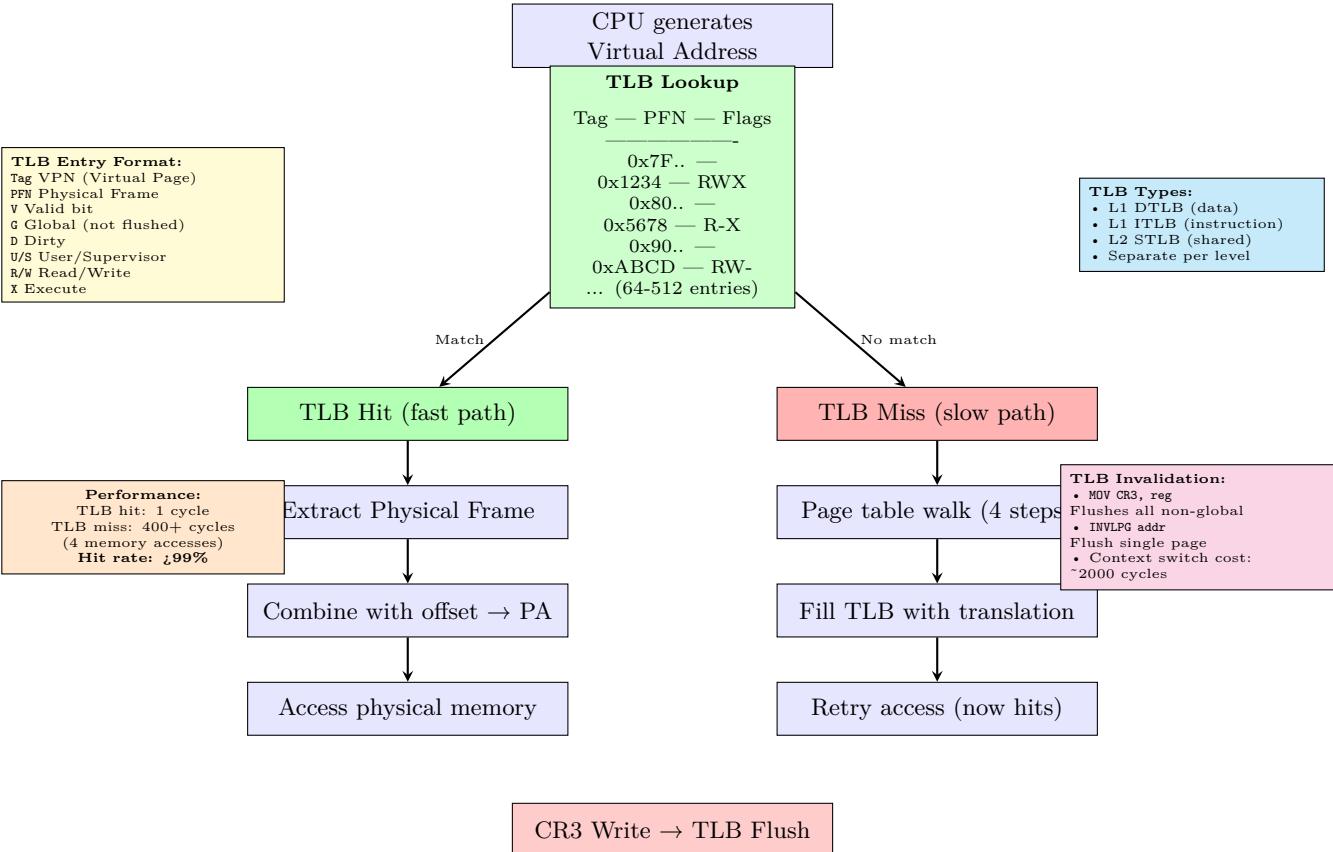


TLB Architecture & Operation



Example: Process A → Process B switch

1. Save Process A context
2. Write Process B's CR3 → **TLB flush**
3. Process B resumes with empty TLB
4. First ~100 memory accesses miss (slow)
5. TLB warms up, performance recovers