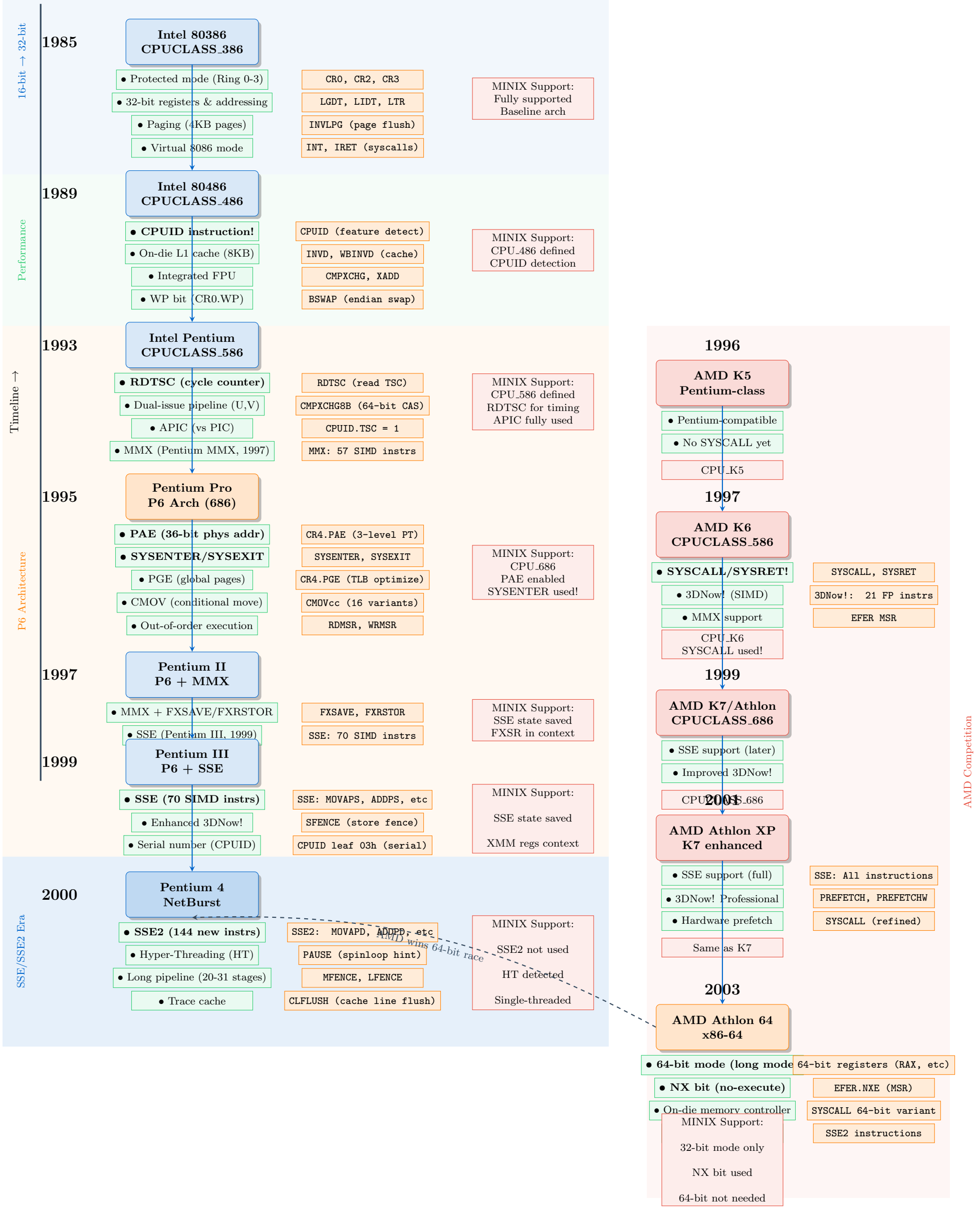
x86 CPU Architecture Evolution: 386 to Pentium 4

CPU Interface Features by Generation (1985-2004)



Key Innovations by Generation

386 (1985): Protected mode, paging, 32-bit - Foundation for modern OS
486 (1989): CPUID instruction enables runtime feature detection, on-die cache
Pentium (1993): RDTSC for precise timing, APIC for SMP, dual-issue superscalar
Pentium Pro (1995): PAE (¿4GB RAM), SYSENTER (fast syscalls), PGE (TLB optimization)
AMD K6 (1997): First to introduce SYSCALL/SYSRET (AMD-specific fast syscall)
Pentium II/III (1997-1999): SSE SIMD (70 instructions), FXSAVE for fast context switching

MINIX CPU Detection Strategy (from cputypes.h & specialreg.h):

1. Check for CPUID instruction (486+): If no CPUID, assume 386
2. Execute CPUID to get vendor (Intel/AMD/Cyrix/etc.) and family
3. Detect features: RDTSC, APIC, PAE, SYSENTER/SYSCALL, SSE, NX bit, etc.
4. Configure kernel based on available features (see features.md for full matrix)
5. At boot: Select fastest syscall mechanism (SYSCALL ¿ SYSENTER ¿ INT)
6. 32-bit mode: PAE enables NX bit; 64-bit features detected but not used

`cputypes.h:35-58` CPU class/type definitions `specialreg.h:37-200` CPUID flags, CR bits `features.md:1-13` MINIX support matrix