Digital Design and Computer Architecture LU

Lab Protocol

Exercise IV

Group 25

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Forwarding Simulation

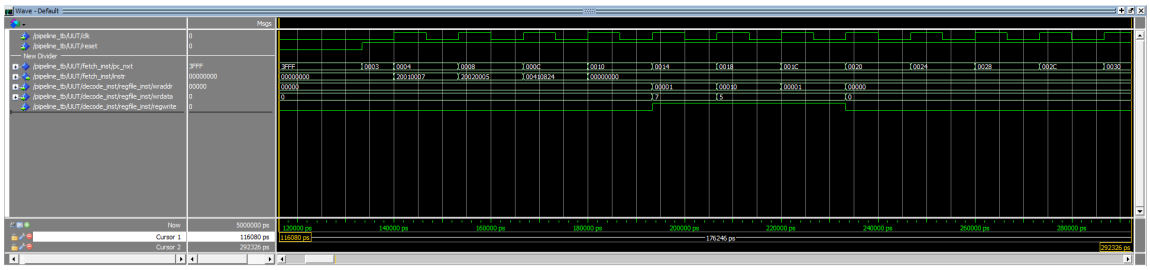

Figure 1: Simulation screenshot for Listing 1.

Make sure that at least the following signals are visible in Figure 1: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 1: Assembler example with forwarding

```
addi $1, $0, 7
addi $2, $0, 5
and $1, $2, $1
nop
nop
```

Branch Hazards Simulation

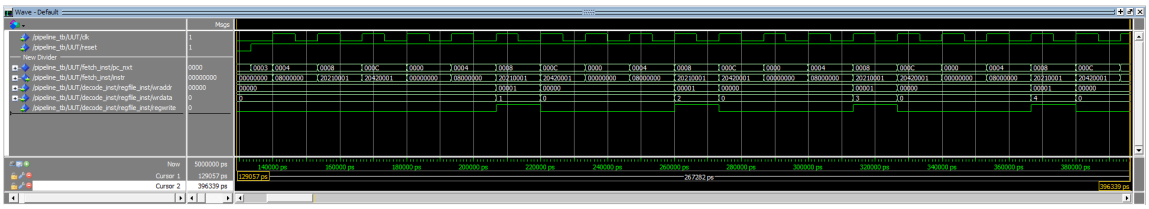

Figure 2: Simulation screenshot for Listing 2.

Make sure that at least the following signals are visible in Figure 2: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 2: Assembler example with branch delay slot

```
loop:   j loop
        addi $1, $1, 1
        addi $2, $2, 1
        nop
```

Synthesis Results

Table 1: Resource usage by entity, including resources used by sub-entities.

	LC Combinationals	LC Registers	Memory Bits
Fetch Stage	90	14	131072
Decode Stage	1486 (1312)	1070(46)	0
– Register File	174	1024	0
Execute Stage	1125 (624)	153	0
– ALU	501	0	0
Memory Stage	395 (232)	101	0
– Jump Unit	4	0	0
– Memory Unit	159	0	0
Write-Back Stage	49	71	0
Forwarding Unit	16	0	0
Control Unit	0	0	0
Sum	3161	1409	131072

Question: What is the maximum frequency of your design?

Answer: 100.41 MHz at 0C, 93.12 MHz at 85C in the slow Models and 182.98 MHz in the fast 0C Model (all Models with 1200mV)

Question: Where is the critical path of your design?

Answer: From mem_inst|sig_aluresult_in to exec_inst|sig_op_before_fwd.imm