Digital Design and Computer Architecture LU

Lab Protocol

Exercise III

Group 25

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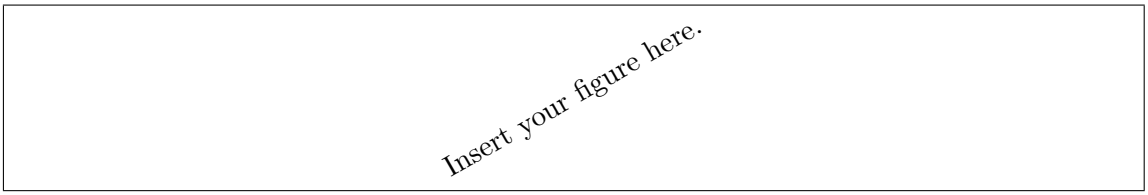

Figure 1: Simulation screenshot for Listing 1.

Make sure the following signals are visible in Figure 1 and the signal values are readable: the program counter in the fetch stage, the instruction being fetched, and the fields `address`, `rd`, `wr`, `byteena`, and `wrdata` in the `mem_out` signal coming out of the pipeline.

Listing 1: Assembler example without forwarding

```
        addi $1, $0, 0
        nop
        nop
loop:
        addi $1, $1, 1
        nop
        nop
        sw $1, 16($0)
        j loop
        nop
        nop
        nop
```