Contact

www.linkedin.com/in/loideyron (LinkedIn)
loideyron.github.io/ (Personal)

Top Skills

SystemVerilog
Universal Verification Methodology (UVM)
C

Languages

English (Full Professional)
Japanese (Elementary)
Filipino (Native or Bilingual)

Certifications

Fundamental Information Technology Engineers (FE) Certification
SystemVerilog Accelerated Verification with UVM v1.2.5 Exam

Honors-Awards

Honorable Mention
DOST-Science Education Institute Merit Scholarship

Lloyd Aaron Y.

Digital Design Verification at AIStorm INC
Villach, Carinthia, Austria

Summary

Digital Design Verification Engineer proficient in SystemVerilog + UVM, SVA, C/C++, and Specman-e.
Skilled in sub-system/block level verification on imaging IPs, controller IPs, and mixed-signal IPs.
Skilled in testbench development for reuse and portability (simulator, emulator, and FPGA platforms)
Experienced in both simulation and formal verification methodologies.

Interested in technical research and development related to semiconductors and embedded systems.

Experience

AIStorm INC

Senior Member of Technical Staff - Digital Verification
July 2022 - December 2023 (1 year 6 months)
Austria

Infineon Technologies

3 years 6 months

Senior Staff Engineer - Digital Design Verification
April 2021 - June 2022 (1 year 3 months)
Villach, Carinthia, Austria

Successfully performed digital functional verification of mixed signal IPs:
+ Block Level DV Lead (SV-UVM) : Digital PLL IP (High Performance Automotive Radar)
+ Block Level DV (SV-UVM) : ADC IP (Low Power Radar)
+ Formal (SVA, JasperGold Apps): Digital PLL IP, ADC IP
Successfully improved verification process/team:
+ Reuseable verification IP development - clocks, ahb i/f, spi i/f, common sva
+ Process improvement using Git/Bitbucket/Jira workflows, requirements traceability workflows

Digital Design Verification Engineer
January 2019 - April 2021 (2 years 4 months)
Villach, Carinthia, Austria

Successfully performed digital functional verification of mixed signal IPs:
+ Block Level DV (SV-UVM) : Digital PLL IP (automotive radar), Industrial Controller IP
+ Block Level DV (Specman-e): ADC IP (automotive microcontroller)
+ Formal (SVA, JasperGold Apps): Digital PLL IP, Clock Subsystem

Canon Information Technologies, Philippines Inc.
Principal Hardware Engineer
September 2015 - September 2018 (3 years 1 month)
Quezon City, Philippines

Successfully led the improvement of verification methodology to various digital systems, and IPs.
+ Verification Lead: Common Imaging Framework, Block/Subsystem DV for Imaging IP (SV-UVM)
+ Technical Lead - Verification Methodology Development: SV-UVM TB Reuse for Sim and Emu (PalladiumXP), In-house Portable Stimulus (Python), Assertion based Verification (SV-UVM, SVA)

Successfully developed testbenches for digital verification of imaging IPs:
+ Subsystem DV using XILINX FPGA and C-simulation
+ C/C++ Models and Tools for Image Processing IP

Successfully led verification project with a small core team as a project manager using Agile approach.

Canon Inc.
Intra-Company Assignee for Hardware Design Verification
September 2013 - September 2015 (2 years 1 month)
Tokyo, Japan

Successfully conceptualized and implemented advanced digital verification methodologies.
+ DV Methodology Development: SV-UVM TB acceleration for Emulation (PalladiumXP), Verilog-HW and C-SW co-emulation (PalladiumXP), FPGA Prototyping (XILINX), Synthesizeable DV IPs (SV), Formal Verification (SVA - Incisive Formal Verifier)
+ DV Lead between PH and JP sites

Canon Information Technologies, Philippines Inc.

5 years 11 months

Senior Hardware Engineer - Design Verification

April 2011 - September 2013 (2 years 6 months)

Quezon City, Philippines

Successfully led the development of verification strategies for advanced imaging subsystems.

+ Technical Lead - Block/Subsystem DV (Specman-e): Network-on-Chip Imaging Subsystem

Successfully performed digital function verification for system controller IPs:

+ Block Level DV (Specman-e): SD Card Controller IP, Memory Controller IP
+ Block Level DV (SV-UVM): AXI4 Interconnect IP

Hardware Engineer - Design Verification

November 2007 - April 2011 (3 years 6 months)

Quezon City, Philippines

Successfully performed digital functional verification for digital consumer IPs.

+ Block Level DV (Specman e) : Clock IPs, Tensilica Interconnect IPs, AHB/AXI Bus Infrastructure IPs, Image Encoder/Decoder IPs

Education

De La Salle University

BS, Computer Science, Major in Computer Systems Engineering · (2003 - 2007)

Manila Science High School

High School Diploma · (1999 - 2003)