

## Contact

[www.linkedin.com/in/](http://www.linkedin.com/in/)

## Top Skills

C

C++

SystemVerilog

## Languages

English (Full Professional)

Serbian (Native or Bilingual)

# Mikah Boller

Digital Design Verification Engineer

Serbia

## Summary

- Random constrained, metric driven verification
- SystemVerilog/UVM, Verilog, VHDL, C, C++, Java, Assembler, scripting (Python), version control (GIT, SVN, Design Sync, ClearCase)

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## Experience

Self-employed

Design Verification Engineer

February 2022 - Present (2 years)

ELSYS Eastern Europe

8 years 1 month

Design Verification Engineer

January 2017 - January 2022 (5 years 1 month)

Current Controller IC - Verification Team Lead

Power Steering Inverter Bridge - Verification Engineer

Automotive Power Management IC - Verification Team Lead

TOP-level verification

July 2016 - December 2016 (6 months)

Vision multi-processor SoC

IP Verification

January 2016 - June 2016 (6 months)

Verification of Power management IC for mobile applications (OVM/  
SystemVerilog)

TOP-level Verification

August 2015 - December 2015 (5 months)

Rotary encoder IC verification (SystemVerilog/UVM)

UVC development

February 2015 - July 2015 (6 months)

DMA, I2C, WB, SPI Phy and Data level UVCs development (SystemVerilog/UVM)

#### IP Verification

January 2015 - March 2015 (3 months)

WB2I2C bridge (SystemVerilog/UVM)

#### TOP-level Verification

April 2014 - January 2015 (10 months)

Power Management Unit, Clock System and Reset Controller (C, SystemVerilog, UVM)

#### Design and Verification Engineer

January 2014 - March 2014 (3 months)

- Digital design of UDP2OCP IP
- Training OCP Splitter and AMBA APB uVCs development

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## Education

School of Electrical Engineering, University of Belgrade, Serbia  
Bachelor's degree, Computer Science · (2009 - 2013)

Grammar School, Kragujevac, Serbia  
High School · (2006 - 2009)

School of Electrical Engineering, University of Belgrade - Master  
Degree Studies  
· (2013)