Contact

www.linkedin.com/in/angel-jose-soto-aa18b29 (LinkedIn)

Top Skills

Depuración de programas
Verilog
Diseño RTL

Languages

Español (Native or Bilingual)
Inglés (Full Professional)
Alemán (Limited Working)

Publications

A low noise digital readout system for scientific charge coupled devices

Optimal filter for noise reduction in CCD readout

Fully Integrated Single-Inductor Multiple-Output (SIMO) DC-DC Converter in CMOS 65 nm Technology

Design and simulation of the control architecture of a fully integrated Single Inductor Multiple output (SIMO) DC-DC converter

ASIC for Isolated Power Inverters

Patents

Vorrichtung und ein Verfahren zu Verminderung des Ringings in CAN Bussen

Can Bus Driver with Accelerated State Transition

Angel Jose Soto

Senior Staff Digital IC Design Engineer
Dresden, Saxony, Germany

Summary

Most people think that certain things should not mix, like analog and digital design. However, after being working on both sides, I can say that the perfect balance/challenge can be found in the Mixed-Signal.

So that is me, someone walking just in the middle, learning something new of both worlds every day.

Experience

indie Semiconductor

Senior Staff Digital IC Design Engineer
January 2023 - Present (1 year 1 month)
Dresde, Sajonia, Alemania

DMOS GmbH

4 years 6 months

Digital Mixed Signal Design

July 2019 - December 2022 (3 years 6 months)
Dresde y alrededores, Alemania

Mixed Signal Design and Simulation for speeding up the development of ASICs for automotive industry.

CAN FD, CAN FD Light, CAN XL. Digital Signal Processing for power electronic systems. Custom ASIC Design. SPAD sensor. Lidar IC development.

Digital Design Engineer

July 2018 - June 2019 (1 year)
Dresde y alrededores, Alemania

Using digital design approach for mixed-signal automotive and industrial ASIC design.

Mainly focused in CAN FD digital design. Self calibration and compensation. Patents generation.

CONICET

Professional Research Support - Profesional de Apoyo a la Investigación

June 2015 - June 2018 (3 years 1 month)

IIIE Bahía Blanca

ASIC and FPGA designs. The design of analogue, digital or mixed-signal ASICs in several processes depending on the requirements of the researchers. Further the design and implementation of digital parts in Xilinx's FPGA platforms for the test of ASIC and new digital processing architectures.

Universidad Nacional del Sur

10 years 3 months

Teaching Assistant A

May 2012 - June 2018 (6 years 2 months)

Teaching Assistant A for grade courses:

*Power Electronics

*Semiconducor Devices

PhD Student

October 2009 - March 2015 (5 years 6 months)

Universidad Nacional del Sur

The doctorate program was pointed to improve the power management of systems in a package. Two branches were developed:

-- The first branch was focused on coupled inductor filter technique on Magnetic Low-Temperature Co-fired Ceramic. A complete model of high current inductors on magnetic LTCC was carried on. The proposed model was simulated and adjusted on 3QD ANSYS and Maxwell 3D. Then a prototype was fabricated and tested in the laboratory. The results show 400% more attenuation at same filter volume.

-- The second branch pointed to fully integrated SIMO (Single Inductor Multiple Outputs) converter on a 65nm CMOS process development. A converter with two outputs and a boost-like architecture was proposed. At first, a golden model developed on PowerSim and then the complete implementation was carried on in Cadence Virtuoso environment and the DRV/LVS checks were run under Calibre Mentor Graphics tool.

Teaching Assistant B

April 2008 - August 2012 (4 years 5 months)

Universidad Nacional del Sur

Teaching Assistant B for grade courses:

*Semiconducor Devices
*Introduction to Electronics
*Power Electronics

Fermilab
Invited R&D Engineer
August 2017 - October 2017 (3 months)
Batavia, Illinois, Estados Unidos de America

Definition and implementation of firmware and software architecture for a new CCD acquisition system.

Fermilab
Invited R&D Engineer
February 2017 - March 2017 (2 months)
Batavia, Illinois, Estados Unidos de America

Collaboration in the architecture and firmware design on a new acquisition system for CCD sensors were the main objectives.

The networking and future work definition were the key factor of the stage.

INTI
Alumno
2009 - 2009 (less than a year)

SAYCE
Desarrollador Software
April 2006 - December 2006 (9 months)

Software developer. Development of software for ATMEL microcontrollers for projects related with FerroExpreso Pampeano (local train company). The projects:

--DC low voltage generator controller for locomotive control electronics. Replacement for old SCR controller with new switched power electronic controller PWM adaptable modulation.

--Development of speedometer for locomotives with low speed high precision.

Education

Universidad Nacional del Sur

Doctor of Philosophy (Ph.D.), Ingeniería · (2009 - 2015)

Faculté Polytechnique de Mons

Invited Student, Microelectronics, Design of a fully integrated SIMO converter · (2013 - 2013)

University of Arkansas

Invited Student, Topics: Magnetic LTCC · (2013 - 2013)

Universidad Nacional del Sur

Engineer's degree, Electrical and Electronics Engineering · (2002 - 2009)