Contact

www.linkedin.com/in/

Top Skills

Integrated Circuit Design
Hardware Architecture
Embedded Software

Languages

Ukrainian (Native or Bilingual)
English (Full Professional)
Deutsch (Elementary)

Certifications

Basic Static Timing Analysis v2.0 Exam
C++ Language Fundamentals v12.2 Exam
SystemVerilog Assertions v4.2 Exam
SystemVerilog Accelerated Verification with UVM v1.2.5 Exam

Bao Neilan

Principal Digital Design Engineer at Renesas Electronics
Austria

Summary

I like to manage non-standard technical tasks and organise talants into successfull team.

23 years of experience in the Electronic design at ASIC/FPGA/PCB/ Software levels, helps me to find a way.

My strong side is complex understanding of the Integrate Circuit (digital synchronous & asynchronous) development flow from Concept/RTL down to GDS/production.

The application areas include:
- Mixed Signal SoC,
- Self-Cheking & Fault Tolerant design,
- FuSa arhitecture,
- Low Power design (CDC/PDC/GALS),
- Asynchronous design (Petrify),
- DFT arhitecture,
- Verification (UVM, Formal)
- PMIC,
- Industrial Automatic,
- Measurement devices,
- Communication devices & protocols,
- CPU peripheral,
- Embeded soft, RTOS etc.

Experience

Renesas Electronics

Principal Digital Design Engineer / Design Lead
September 2021 - Present (2 years 5 months)
Austria

Work on 4 ASIC's

Dialog Semiconductor

Principal Digital Design Engineer / Design Lead

November 2019 - September 2021 (1 year 11 months)

Austria

- Close cooperation with customers.
Define system level requirements for final product and digital part. Write sytem and digital specifications (use UML for formalization). Support customer with problem solwing and product application.
- Organise team work of digital designers. Coordinate digital team with another departments.
- Estimate and plane resourcess and tasks.
- Design review (MDR, FDR) / Status reporting
- Resolve all techical blocking problems.
- Microarhitecture / RTL codding / LINT / LEC / CDC / STA / Synt, P&R / Silicon evaluation
- Digital IP concept, design & implementation
- Verification (UVM, Formal Functional, SVA)
- Asynchronous digital design (Petrify, FPGA prototyping)

Work on 3 ASIC's

NXP Semiconductors Austria

Principal Digital Design Engineer

September 2017 - October 2019 (2 years 2 months)

Austria

-IP Design (CPU peripheral, I2C, APB bus, Self-Cheking cirquits, etc). Concept, Specification & Implementation.
-Design flow scripting (LINT, CDC, Formal, SYNT, SIM) for Synopsys, Cadence, Mentor tools.
-Legacy IPs support, System debug, intensive Reverce Engineering (complex RTL/CDC/STA)
-Experiance with "big" project management (documentation, version control, bug tracking etc.).
- UVM (basic knowledge: TOP environment, UVC, reference model, user sequences, REG layer).
- Formal Functional Verification (basic knowledge, SVA)
- Firmware arhitecture (UML) & programming (ARM Cortex-M4 / C++ / FreeRTOS).

Work on 1 ASIC

Toshiba Electronics Europe GmbH

Senior Digital Design Engineer / Design Lead

January 2016 - September 2017 (1 year 9 months)

Austria

- Responsible for rapid ASIC prototyping (digital part) in R&D projects. Define metodology of managment and development process.
- Digital Design Lead of Mixed Signal SoC projects.
- Organise work of 15 designers include internal resourcess and outsource.
- Project management include Budget estimation, Resources & Tasks planning, Status reporting.
- Close work with Customer for System Specification definition, Change requests and silicon Evaluation support
- Develop and optimize unified design flow in Cadence / Synopsys environment (SP&R, DFT, Verification)
- Develop unified JTAG compliant Test Arhitecture for mixed signal IC
- Arhitecture design for ASIL-D compliant projects. Self checking, Fault tolerant design (SEU mitigating, TMR etc.)

Made 5 ASIC (4 ASIL-D compliant)

Melexis

11 years

ASIC Back-end Digital Design Engineer

May 2010 - December 2015 (5 years 8 months)

Tessenderlo, Flemish Region, Belgium

Focused on back-end design:

- Digital part SP&R, STA, DFT implementation for many IC's;
- Design flow scripting

R&D process support & improvement for time-to-market & risk minimization, quality increasing, reusing existing solutions and another.

Coaching people in terms of optimization specification requirements, tools usage, prevention production issues etc.

Problem solving in all steps of IC development flow.

SP&R of not fully synchronous digital part (45 gclk + 31 clk + 5 osc).

Made SP&R for 30 ASICs.

ASIC & FPGA Front-end Digital Design Engineer

2004 - May 2010 (6 years)

Tessenderlo, Flemish Region, Belgium

Focused on digital part R&D for mixed signal, FSM & processor based (uC), SoC IC's:

- Specification & Architecture design.
- RTL implementation & Functional verification (no experience in UVM).
- Design for Test (DFT) & design for debug and manufacturing.
- ATPG (StackAt, IDDQ, Delay, AtSpeed).
- IC problem debugging by EMMI, FIB, DALS, OBIRCH.
- FPGA prototyping.
- Real Time Embedded software for uC.
- Low power, Clock Domain Crossing (CDC) digital design.

Made 2 ASICs through entire flow of specification to prototypes & 11 ASICs partly in different flow steps.

JAVAD GNSS

2 years

Digital Design Engineer

2000 - 2000 (less than a year)
United States

Digital Design Engineer

2000 - 2000 (less than a year)
United States

Junior Digital Design Engineer

1998 - 2000 (2 years)
Moscow, Russian Federation

Made PCB schematic, layout & mechanical implementation of evaluation and test boards.

Education

Moscow Aviation Institute (State Technical University) (MAI)

Master of Science (MSc), Electronics · (1994 - 2000)

Cadence Design Systems Education Services

Trainings, Digital Design · (2004 - 2021)