No.	Cell Name	Pin	Type	Output enable BS Cell	Guard Value IN	Guard Value EX *
from tdi						
1	din0	D[0]	IN	-	*	0
2	dout0	D[0]	OUT	Nenout=0	0	*
3	din1	D[1]	IN	-	*	0
4	dout1	D[1]	OUT	Nenout=0	0	*
5	din2	D[2]	IN	-	*	0
6	dout2	D[2]	OUT	Nenout=0	0	*
7	din3	D[3]	IN	-	*	0
8	dout3	D[3]	OUT	Nenout=0	0	*
9	din4	D[4]	IN	-	*	0
10	dout4	D[4]	OUT	Nenout=0	0	*
11	din5	D[5]	IN	-	*	0
12	dout5	D[5]	OUT	Nenout=0	0	*
13	din6	D[6]	IN	-	*	0
14	dout6	D[6]	OUT	Nenout=0	0	*
15	din7	D[7]	IN	-	*	0
16	dout7	D[7]	OUT	Nenout=0	0	*
17	din8	D[8]	IN	-	*	0
18	dout8	D[8]	OUT	Nenout=0	0	*
19	din9	D[9]	IN	-	*	0
20	dout9	D[9]	OUT	Nenout=0	0	*
21	din10	D[10]	IN	-	*	0
22	dout10	D[10]	OUT	Nenout=0	0	*
23	din11	D[11]	IN	-	*	0
24	dout11	D[11]	OUT	Nenout=0	0	*
25	din12	D[12]	IN	-	*	0
26	dout12	D[12]	OUT	Nenout=0	0	*
27	din13	D[13]	IN	-	*	0
28	dout13	D[13]	OUT	Nenout=0	0	*
29	din14	D[14]	IN	-	*	0
30	dout14	D[14]	OUT	Nenout=0	0	*
31	din15	D[15]	IN	-	*	0
32	dout15	D[15]	OUT	Nenout=0	0	*
33	din16	D[16]	IN	-	*	0
34	dout16	D[16]	OUT	Nenout=0	0	*
35	din17	D[17]	IN	-	*	0
36	dout17	D[17]	OUT	Nenout=0	0	*
37	din18	D[18]	IN	-	*	0
38	dout18	D[18]	OUT	Nenout=0	0	*
39	din19	D[19]	IN	-	*	0
40	dout19	D[19]	OUT	Nenout=0	0	*
41	din20	D[20]	IN	-	*	0
42	dout20	D[20]	OUT	Nenout=0	0	*
43	din21	D[21]	IN	-	*	0
44	dout21	D[21]	OUT	Nenout=0	0	*
45	din22	D[22]	IN	-	*	0
46	dout22	D[22]	OUT	Nenout=0	0	*
47	din23	D[23]	IN	-	*	0
48	dout23	D[23]	OUT	Nenout=0	0	*

No.	Cell Name	Pin	Type	Output enable BS Cell	Guard Value IN	Guard Value EX *
49	din24	D[24]	IN	-	*	0
50	dout24	D[24]	OUT	Nenout=0	0	*
51	din25	D[25]	IN	-	*	0
52	dout25	D[25]	OUT	Nenout=0	0	*
53	din26	D[26]	IN	-	*	0
54	dout26	D[26]	OUT	Nenout=0	0	*
55	din27	D[27]	IN	-	*	0
56	dout27	D[27]	OUT	Nenout=0	0	*
57	din28	D[28]	IN	-	*	0
58	dout28	D[28]	OUT	Nenout=0	0	*
59	din29	D[29]	IN	-	*	0
60	dout29	D[29]	OUT	Nenout=0	0	*
61	din30	D[30]	IN	-	*	0
62	dout30	D[30]	OUT	Nenout=0	0	*
63	din31	D[31]	IN	-	*	0
64	dout31	D[31]	OUT	Nenout=0	0	*
65	cpa	CPA	IN	-	*	1
66	Nenout	-	OUTEN0	-	1	*
67	Nce		OUTEN0	-	1	*
68	lock	LOCK	OUT	Nce=0	0	*
69	bigend	BIGEND	IN	-	*	0
70	Ncpi	nCPI	OUT	Nce=0	0	*
71	dbe	DBE	IN	-	*	0
72	Nbw	nBW	OUT	Nce=0	0	*
73	mclk	MCLK	IN	-	*	0
74	Nwait	nWAIT	IN	-	*	0
75	lateabt	LATEABT	IN	-	*	1
76	prog32	PROG32	IN	-	*	1
77	data32	DATA32	IN	-	*	1
78	Nrw	nRW	OUT	Nce=0	0	*
79	Nopc	nOPC	OUT	Nce=0	0	*
80	Nmreq	nMREQ	OUT	Nce=0	0	*
81	seq	SEQ	OUT	Nce=0	0	*
82	abort	ABORT	IN	-	*	0
83	Nirq	nIRQ	IN	-	*	1
84	Nfiq	nFIQ	IN	-	*	1
85	Nreset	nRESET	IN	-	*	0
86	ale	ALE	IN	-	*	1
87	cpb	CPB	IN	-	*	1
88	Ntrans	nTRANS	OUT	Nce=0	0	*
89	a31	A[31]	OUT	ABE=1	0	*
90	a30	A[30]	OUT	ABE=1	0	*
91	a29	A[29]	OUT	ABE=1	0	*
92	a28	A[28]	OUT	ABE=1	0	*
93	a27	A[27]	OUT	ABE=1	0	*
94	a26	A[26]	OUT	ABE=1	0	*
95	a25	A[25]	OUT	ABE=1	0	*
96	a24	A[24]	OUT	ABE=1	0	*
97	a23	A[23]	OUT	ABE=1	0	*

No.	Cell Name	Pin	Type	Output enable BS Cell	Guard Value IN	Guard Value EX *
98	a22	A[22]	OUT	ABE=1	0	*
99	a21	A[21]	OUT	ABE=1	0	*
100	a20	A[20]	OUT	ABE=1	0	*
101	a19	A[19]	OUT	ABE=1	0	*
102	a18	A[18]	OUT	ABE=1	0	*
103	a17	A[17]	OUT	ABE=1	0	*
104	a16	A[16]	OUT	ABE=1	0	*
105	a15	A[15]	OUT	ABE=1	0	*
106	a14	A[14]	OUT	ABE=1	0	*
107	a13	A[13]	OUT	ABE=1	0	*
108	a12	A[12]	OUT	ABE=1	0	*
109	a11	A[11]	OUT	ABE=1	0	*
110	a10	A[10]	OUT	ABE=1	0	*
111	a09	A[9]	OUT	ABE=1	0	*
112	a08	A[8]	OUT	ABE=1	0	*
113	a07	A[7]	OUT	ABE=1	0	*
114	a06	A[6]	OUT	ABE=1	0	*
115	a05	A[5]	OUT	ABE=1	0	*
116	a04	A[4]	OUT	ABE=1	0	*
117	a03	A[3]	OUT	ABE=1	0	*
118	a02	A[2]	OUT	ABE=1	0	*
119	a01	A[1]	OUT	ABE=1	0	*
120	a00	A[0]	OUT	ABE=1	0	*
121	abe	ABE	INEN1	-	0	*
						to tdo

Table 25: Boundary Scan Signals & Pins

Key:

IN	Input pad
OUT	Output pad
NEN1	Input enable active high
OUTENO	Output enable active low
*	Guard Value for INTEST and EXTEST/CLAMP

9.0 DC Parameters

Subject to Change

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD	Supply voltage	VSS-0.3	VSS+7.0	V	1
Vin	Input voltage applied to any pin	VSS-0.3	VDD+0.3	V	1
Ts	Storage temperature	-40	125	deg C	1

Table 26: ARM60 DC Maximum Ratings

Note:

These are stress ratings only. Exceeding the absolute maximum ratings may permanently damage the device. Operating the device at absolute maximum ratings for extended periods may affect device reliability.

9.2 DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Supply voltage	4.5	5.0	5.5	V	
Vihc	IC input HIGH voltage	3.5		VDD	V	1,2
Vilc	IC input LOW voltage	0.0		1.5	V	1,2
Viht	IT/ITP input HIGH voltage	2.4		VDD	V	1,3,4
Vilt	IT/ITP input LOW voltage	0.0		0.8	V	1,3,4
Ta	Ambient operating temperature	0		70	deg.C	

Table 27: ARM60 DC Operating Conditions

Notes:

1. Voltages measured with respect to VSS.
2. IC - CMOS-level inputs
3. IT - TTL-level inputs (includes IT and ITOTZ pin types)
4. IT - TTL-level inputs with pullups

10.0 AC Parameters

***** Important Note - Provisional Figures *****

The timing parameters given here are preliminary data and subject to change when device characterisation is complete.

The AC timing diagrams presented in this section assume that the outputs of the ARM60 have been loaded with the capacitive loads shown in the `Test Load' column of *Table 28: AC Test Loads*. These loads have been chosen as typical of the type of system in which ARM60 might be employed.

The output drivers of the ARM60 are CMOS inverters which exhibit a propagation delay that increases linearly with the increase in load capacitance. An `Output derating' figure is given for each output driver, showing the approximate rate of increase of output time with increasing load capacitance.

Output Signal	Test Load (pF)	Output derating (ns/pF)
D[31:0]	50	0.072
A[31:0]	50	0.072
LOCK	25	0.072
nCPI	25	0.093
nMREQ	25	0.093
SEQ	25	0.093
nRW	25	0.072
nBW	25	0.072
nOPC	25	0.093
nTRANS	25	0.072
TDO	25	0.072

Table 28: AC Test Loads

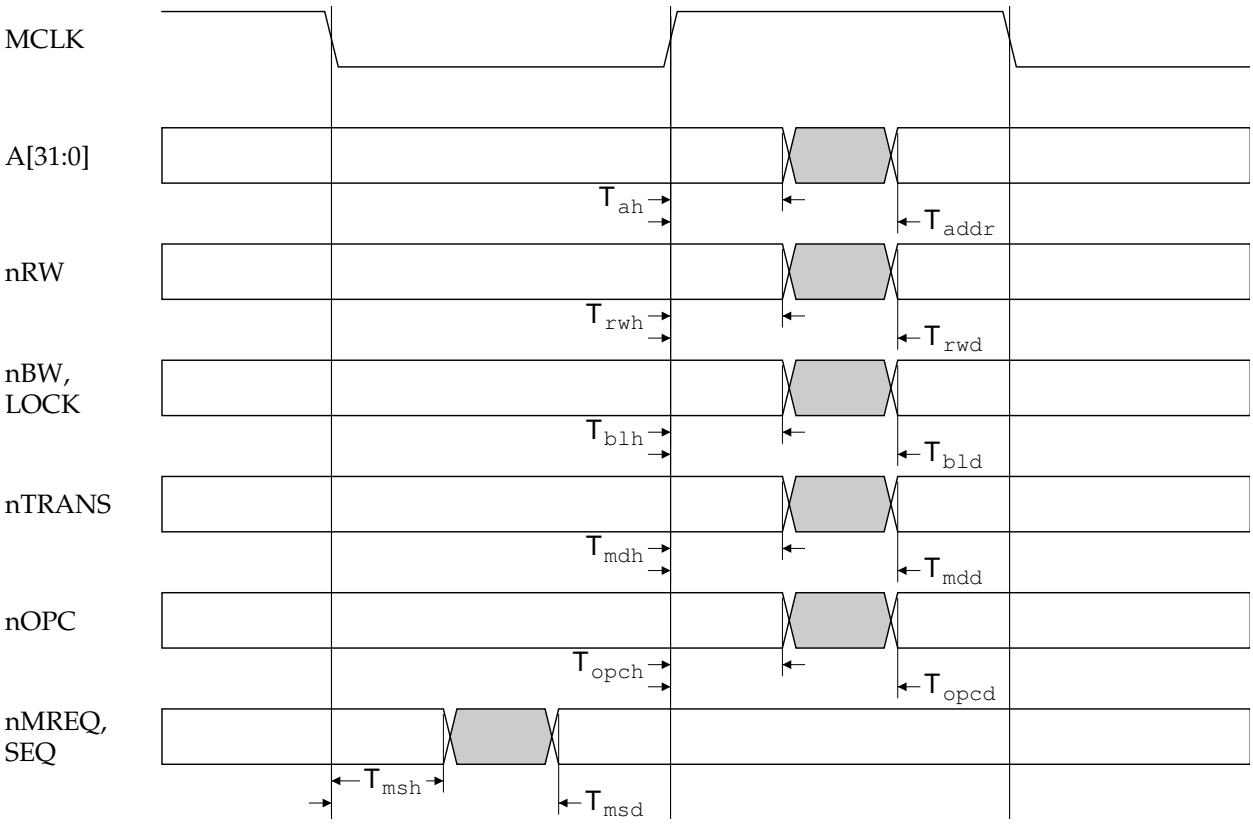

Figure 37: General Timings

Note: **nWAIT**, **ABE** and **ALE** are all HIGH during the cycle shown.

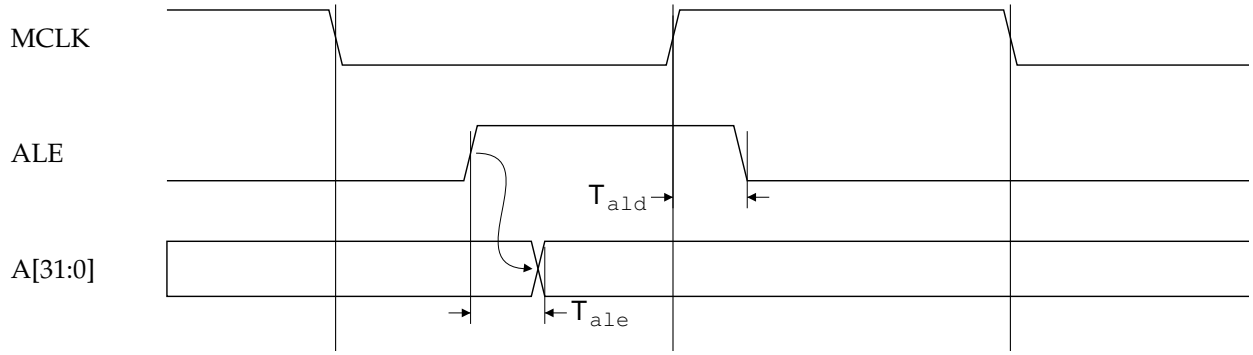

Figure 38: Address Timing

Note: Tald is the time by which **ALE** must be driven LOW in order to latch the current address in phase 2. If **ALE** is driven low after Tald, then a new address will be latched. **ABE** is high during the cycle shown.

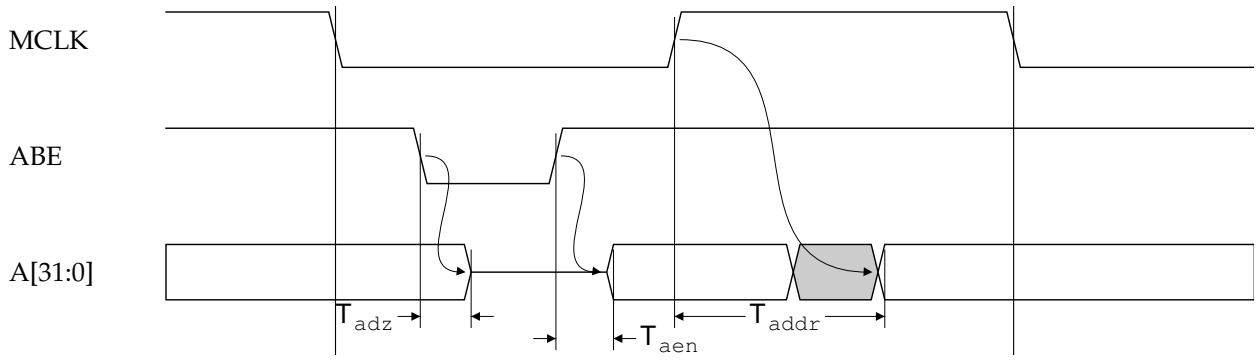

Figure 39: Address Control

Note: Tadz is the tristate turn off time, Taen is the address enable time (turn on), relative to **ABE**. **ALE** is high during the cycle shown.

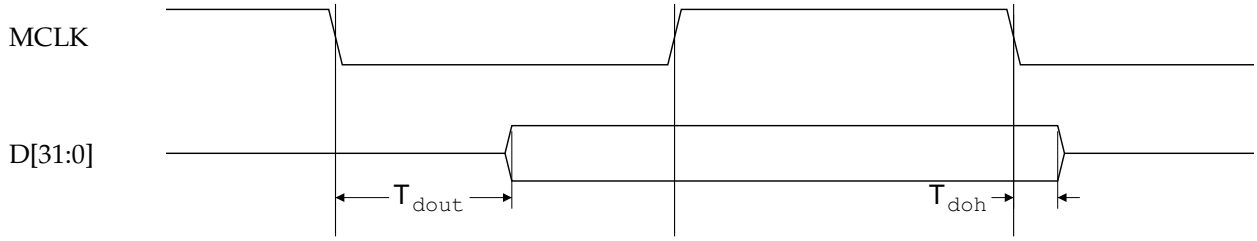

Figure 40: Data Write Cycle

Note: **DBE** is high during the cycle shown.

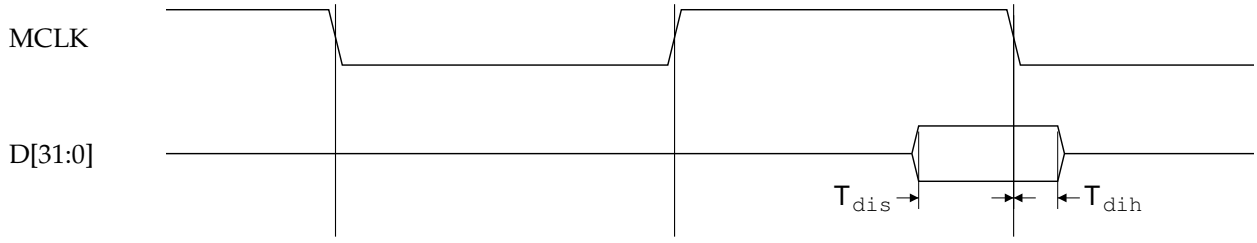

Figure 41: Data Read Cycle

Note: **DBE** is high during the cycle shown.

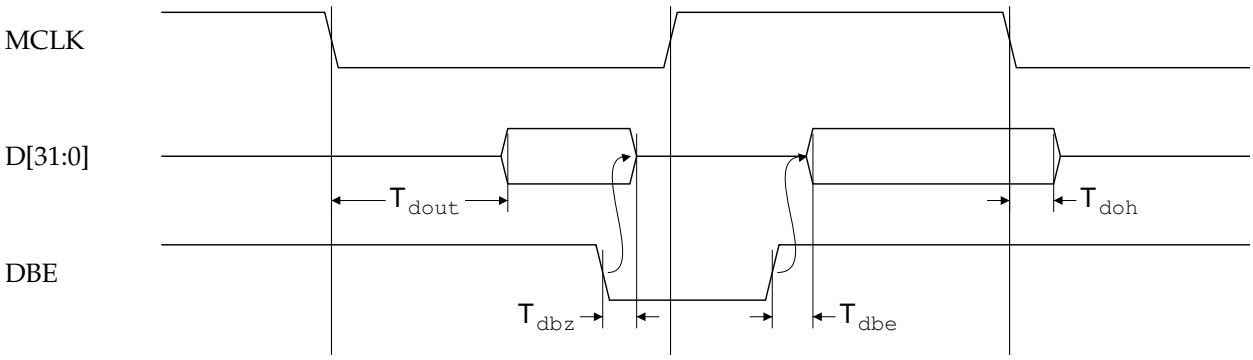

Figure 42: Data Bus Control

Note: The cycle shown is a data write cycle. Here, **DBE** has been used to modify the behaviour of the data bus.

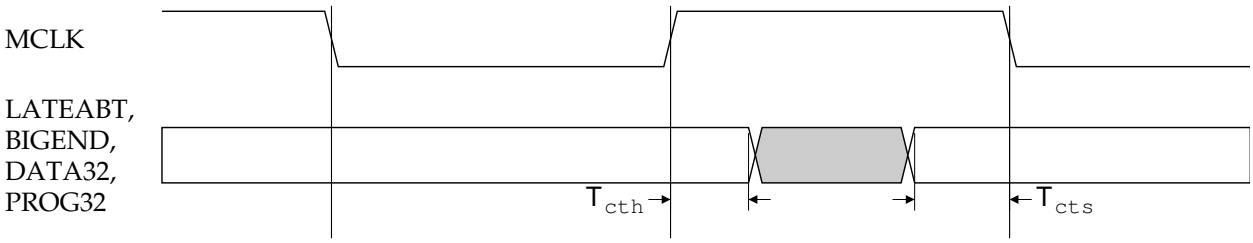

Figure 43: Configuration Pin Timing

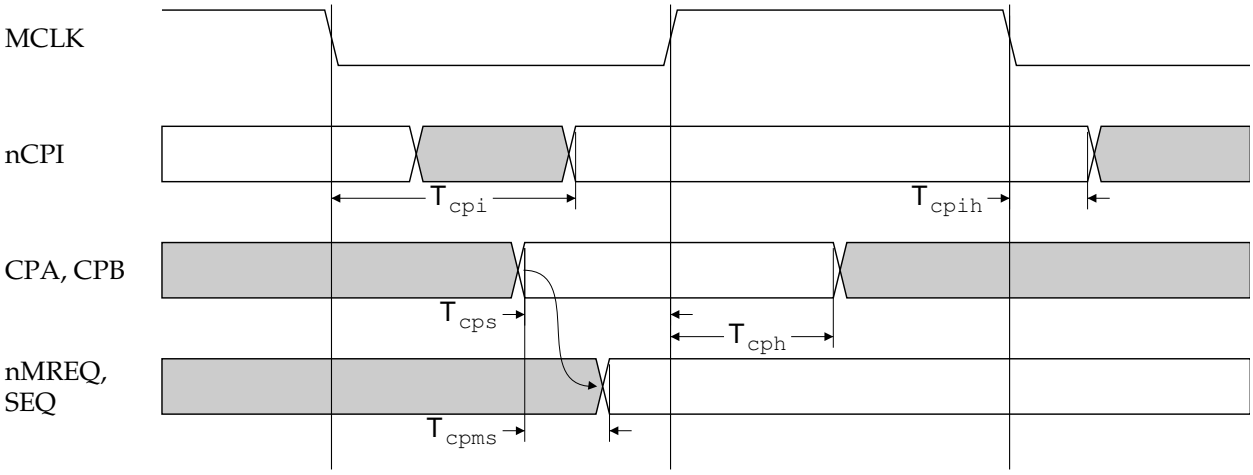

Figure 44: Coprocessor Timing

Note: Normally, **nMREQ** and **SEQ** become valid Tmsd after the falling edge of **MCLK**. In this cycle the ARM has been busy-waiting, waiting for a coprocessor to complete the instruction. If **CPA** and **CPB** change during phase 1, the timing of **nMREQ** and **SEQ** will depend on Tcpms. Most systems should be able to generate **CPA** and **CPB** during the previous phase 2, and so the timing of **nMREQ** and **SEQ** will always be Tmsd.

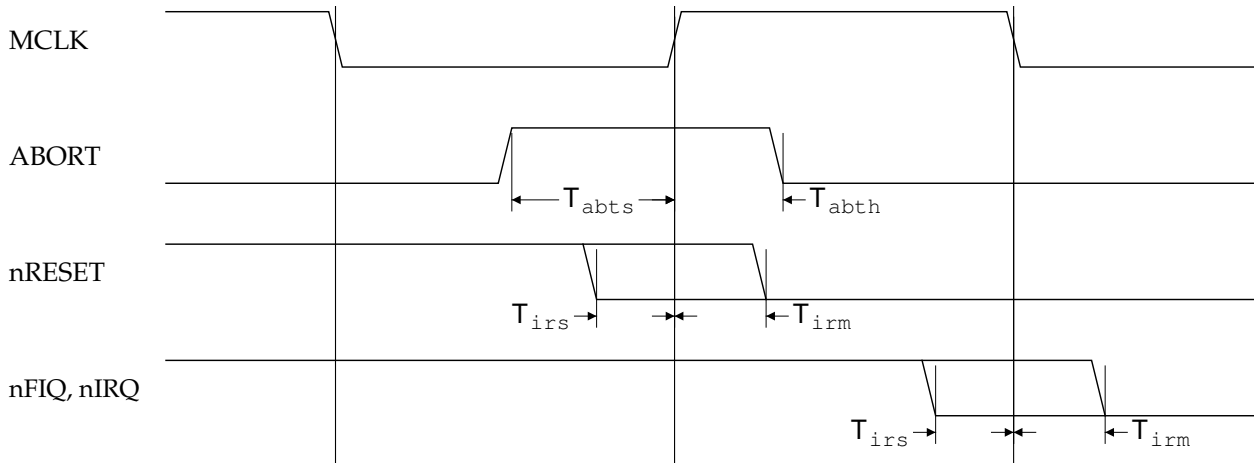

Figure 45: Exception Timing

Note: Tirs guarantees recognition of the interrupt (or reset) source by the corresponding clock edge. Tirm guarantees non-recognition by that clock edge. These inputs may be applied fully asynchronously where the exact cycle of recognition is unimportant.

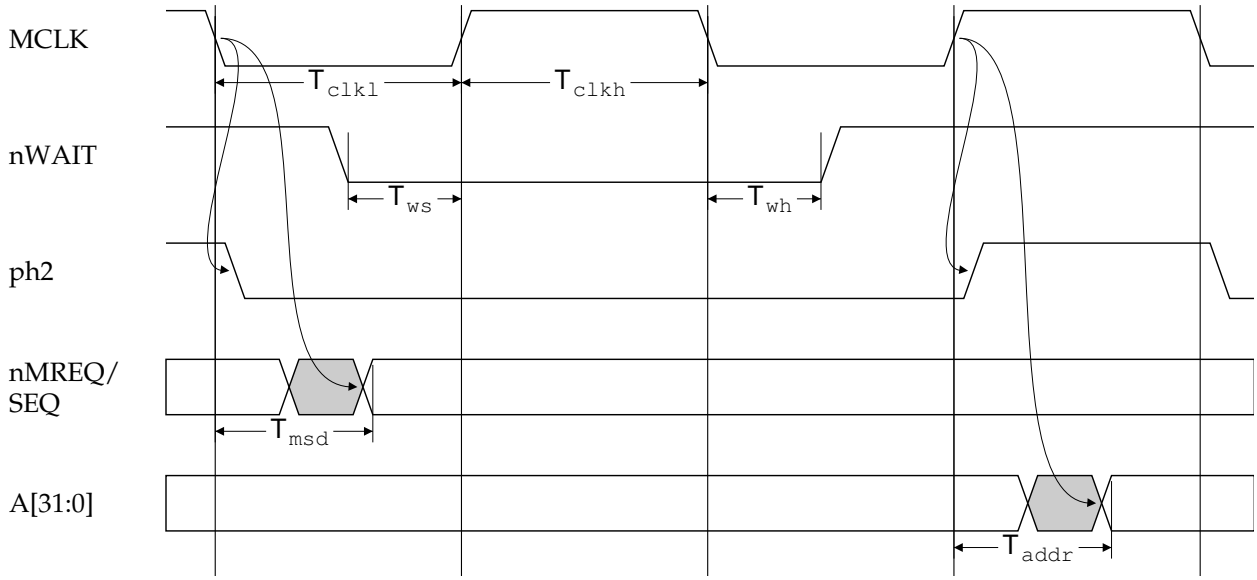

Figure 46: Clock Timing

Note: The ARM core is not clocked by the HIGH phase of **MCLK** enveloped by **nWAIT**. Thus, during the cycles shown, **nMREQ** and **SEQ** change once, during the first LOW phase of **MCLK**, and **A[31:0]** change once, during the second HIGH phase of **MCLK**. For reference, ph2 is shown. This is the internal clock from which the core times all its activity. This signal is included to show how the high phase of the external **MCLK** has been removed from the internal core clock.

Symbol	Parameter	Min	Max
Tckl	clock LOW time	21	
Tckh	clock HIGH time	21	
Tws	nWAIT setup to CKr	3	
Twh	nWAIT hold from CKf	3	
Tale	address latch open		4
Tald	address latch time		4
Taddr	CKr to address valid		12
Tah	address hold time		25
Tdbz	Data bus tristat time		18
Tdbe	Data bus enable time		11
Tdout	data out delay		17
Tdoh	data out hold	5	
Tdis	data in setup	0	
Tdih	data in hold	5	
Tabts	ABORT setup time	10	
Tabth	ABORT hold time	5	
Tirs	interrupt setup	6	
Tirm	Interrupt non-recognition time		TBD
Trwd	CKr to nRW valid		21
Trwh	nRW hold time	5	
Tmsd	CKf to nMREQ & SEQ		23
Tmsh	nMREQ & SEQ hold time	5	
Tbld	CKr to nBW & LOCK		21
Tblh	nBW & LOCK hold	5	
Tmdd	CKr to nTRANS		21
Tmdh	nTRANS	5	
Topcd	CKr to nOPC valid		11
Topch	nOPC hold time	5	
Tcps	CPA, CPB setup	7	
Tcph	CPA,CPB hold time	2	
Tcpms	CPA, CPB to nMREQ, SEQ		15
Tcpi	CKf to nCPI delay		11
Tcpih	nCPI hold time	5	
Tcts	Config setup time	10	
Tcth	Config hold time	5	

Table 29: Provisional AC Parameters (units of nS)

10.1 Notes on AC Parameters

All figures are provisional, and assume that 1 micron CMOS technology is used to fabricate the ASIC containing the ARM6.

11.0 Physical Details

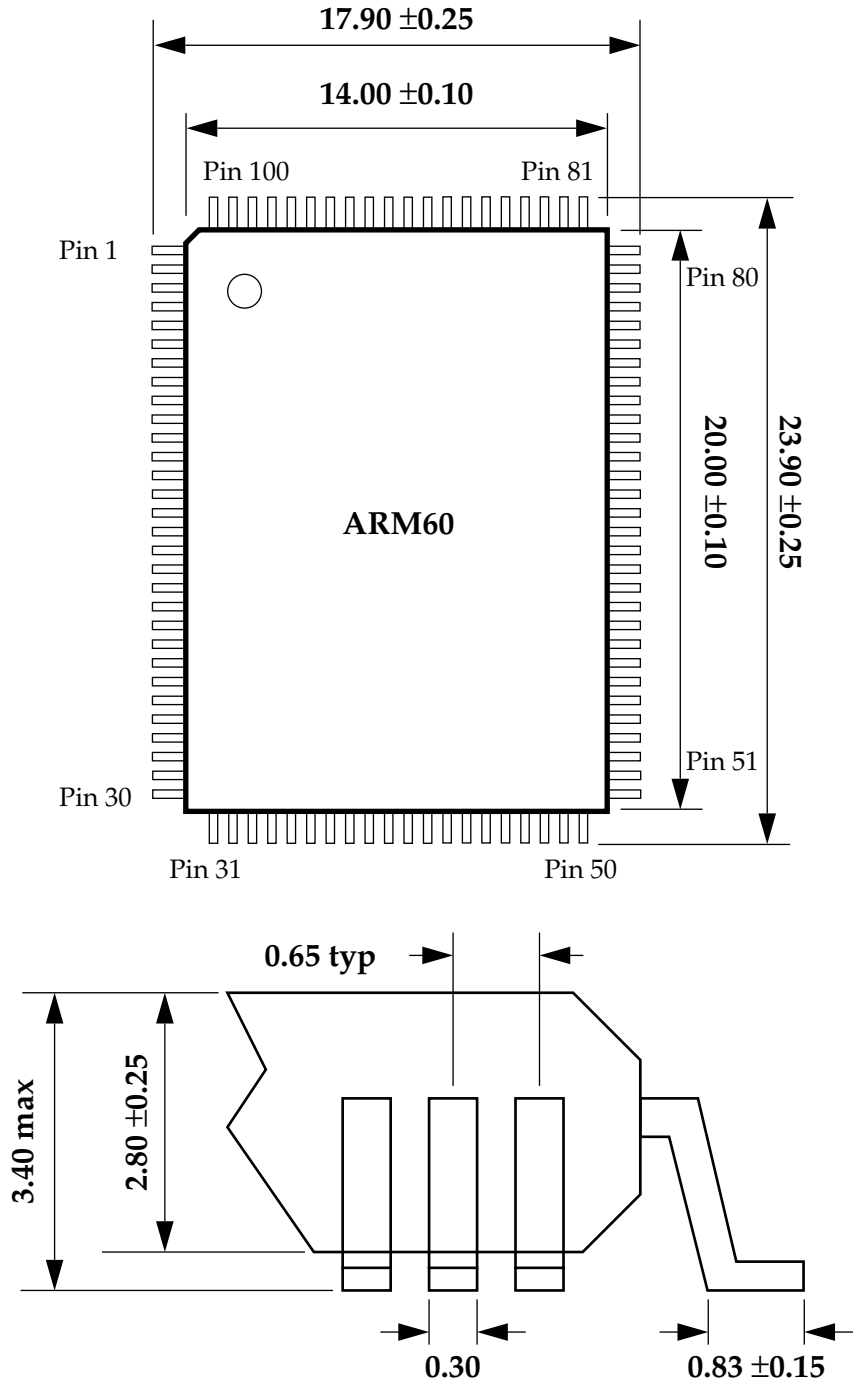

Figure 47: ARM60 100 Pin Metric Plastic QFP Mechanical Dimensions in mm

12.0 Pinout

Pin	Signal	Type
1	D[27]	i/o
2	D[28]	i/o
3	D[29]	i/o
4	D[30]	i/o
5	D[31]	i/o
6	CPA	i
7	Vss	-
8	Vdd	-
9	LOCK	o
10	BIGEND	i
11	nCPI	o
12	DBE	i
13	nBW	o
14	MCLK	i
15	nWAIT	i
16	LATEABT	i
17	PROG32	i
18	DATA32	i
19	nRW	o
20	nOPC	o
21	nMREQ	o
22	SEQ	o
23	ABORT	i
24	nIRQ	i
25	nFIQ	i
26	nRESET	i
27	ALE	i
28	CPB	i
29	nTRANS	o
30	A[31]	o
31	A[30]	o
32	A[29]	o
33	A[28]	o
34	A[27]	o
35	A[26]	o
36	A[25]	o
37	A[24]	o
38	A[23]	o
39	A[22]	o
40	A[21]	o
41	A[20]	o
42	A[19]	o
43	A[18]	o
44	A[17]	o
45	A[16]	o
46	A[15]	o
47	A[14]	o
48	A[13]	o
49	A[12]	o
50	A[11]	o
51	Vdd	-
52	Vss	-
53	A[10]	o
54	A[9]	o
55	A[8]	o
56	A[7]	o
57	A[6]	o
58	A[5]	o
59	A[4]	o
60	A[3]	o
61	A[2]	o
62	A[1]	o
63	A[0]	o
64	Vss	-
65	Vdd	-
66	ABE	i
67	TCK	i
68	TMS	i
69	nTRST	i
70	TDI	i
71	TDO	o
72	D[0]	i/o
73	D[1]	i/o
74	D[2]	i/o
75	D[3]	i/o
76	D[4]	i/o
77	D[5]	i/o
78	D[6]	i/o
79	D[7]	i/o
80	Vss	-
81	Vdd	-
82	D[8]	i/o
83	D[9]	i/o
84	D[10]	i/o
85	D[11]	i/o
86	D[12]	i/o
87	D[13]	i/o
88	D[14]	i/o
89	D[15]	i/o
90	D[16]	i/o
91	D[17]	i/o
92	D[18]	i/o
93	D[19]	i/o
94	D[20]	i/o
95	D[21]	i/o
96	D[22]	i/o
97	D[23]	i/o
98	D[24]	i/o
99	D[25]	i/o
100	D[26]	i/o

Table 30: Pinout - ARM60 100 pin Plastic Quad Flat Pack