SH-1: SH7020/SH7021 Product Brief

SH7000 Series 32-Bit RISC Embedded Controller

HITACHI

PMH11TO002D2
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Overview

The SH7000 series is a reduced instruction set computer (RISC) in which a Hitachi-original CPU and the peripheral functions required for system configuration are integrated onto a single chip.

The CPU has a RISC-type instruction set. Most instructions can be executed in one clock cycle, dramatically improving instruction execution speed. In addition the CPU has a 32-bit internal architecture for enhanced data-processing ability. As a result, the SH7020/SH7021 enable high-performance systems to be constructed with advanced functionality at low cost, even in applications such as real-time control that require operations at very high speeds.

This SH microcomputer includes peripheral functions such as large-capacity ROM, RAM, a direct memory access controller (DMAC), timers, serial communication interface (SCI), an interrupt controller, and I/O ports. External memory access support functions enable direct interface to PSRAM and DRAM. These features can drastically reduce system cost.

Features

- 20 MHz at 5 V, 12.5 MHz 3.3 V
- SH7020: 16-kbyte ROM with 1-kbyte RAM
- SH7021: 32-kbyte ROM/EPROM with 1-kbyte RAM
- RISC Central Processing Unit (CPU)
  - 32-bit internal data paths/16-bit external data paths
  - 16-bit fixed instruction set
  - Five-stage pipeline
  - Load/store register architecture
  - RISC instruction set optimized for C language
  - Sixteen 32-bit general registers, three 32-bit control registers, and four 32-bit system registers
- On-chip multiply and accumulate unit
  - Multiplication ($16 \times 16 \rightarrow 32$) executed in 1 to 3 cycles (50 ns to 150 ns)
  - MAC ($16 \times 16 + 42 \rightarrow 42$) executed in 2 to 3 cycles (100 ns to 150 ns)
- Processing states:
  - Power-on-reset/manual reset
  - Exception processing

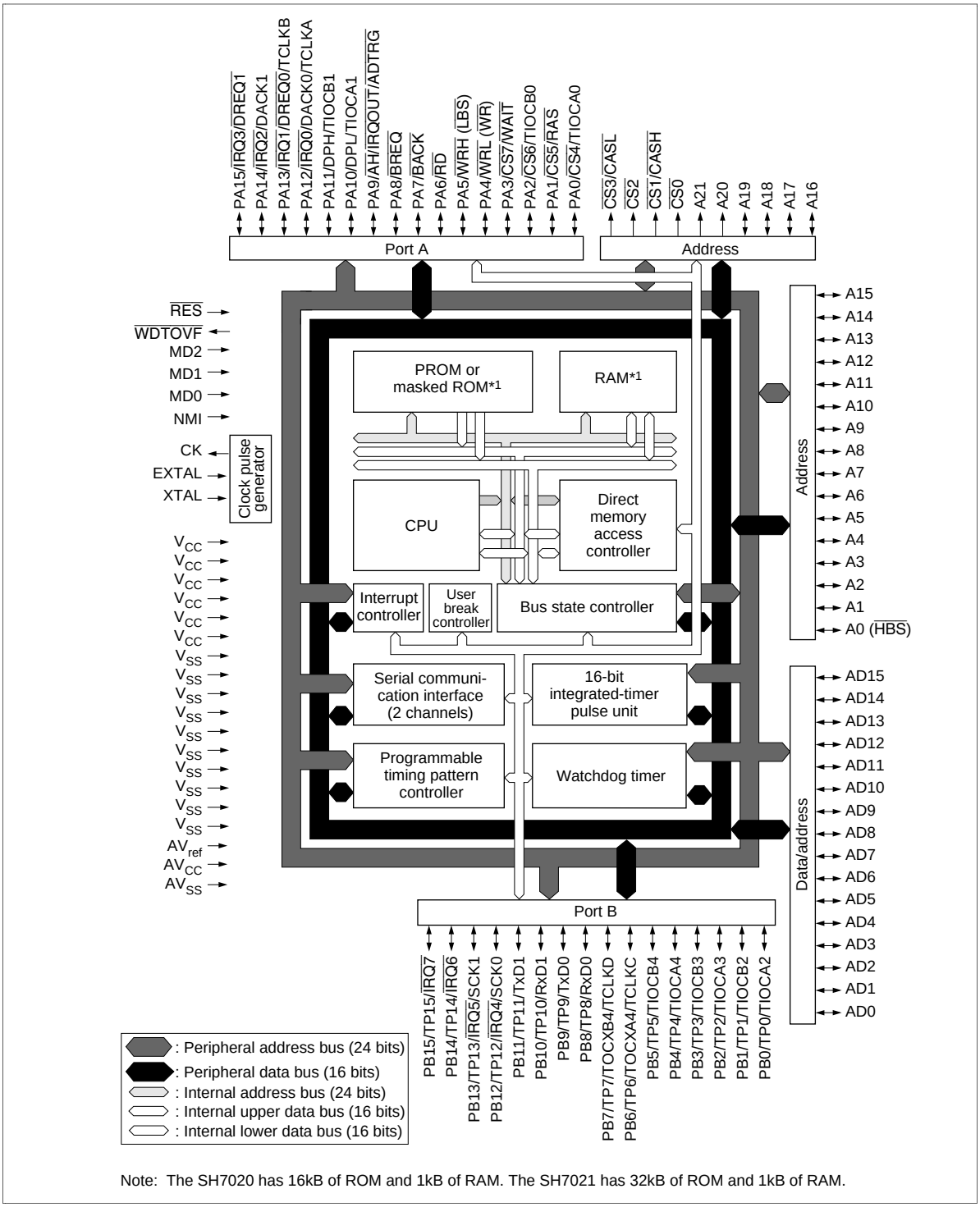
  - — Program execution
  - — Power-down
  - — Bus-released
- Bus State Controller (BSC)
  - — Supports interface to PSRAM, DRAM, ROM, and peripheral I/O
  - — DRAM refresh and burst access functions
  - — One-stage write buffer for improved system performance
  - — 16/8-bit bus width for addressing options
  - — Number of wait states variable
- Four-channel Direct Memory Access Controller (DMAC)
  - — DMA transfers between on-chip or external memory, I/O and peripheral modules
  - — Selectable priorities and modes
  - — Dual or single address transfer mode, external request resources mode and dual address transfer mode for internal request sources supported
- Interrupt Controller (INTC)
  - — 9 external interrupt pins
  - — 30 internal interrupt sources
  - — 16 programmable priority levels
- Five-channel, 16-bit Integrated Timer Unit (ITU)
  - — Ten waveforms can be output
  - — PWM modes
  - — Counters, input capture/measurement
- Watchdog Timer
- Programmable timing pattern controller with maximum 16-bit output (4 bits × 4 channels)
- Two-channel SCI with full duplex and asynchronous/synchronous selectable modes
- 32 I/O
- User Break Controller (UBC) for generating interrupts to simplify debugging
- Operating Temperature: –20°C to +75°C
- Package: 100-pin Thin Quad Flat Pack (TQFP)
- Process: 0.8 micron technology
- Complete development system support

Related Manuals

- *SH Series Overview*
- *SH7020, SH7021 Hardware Manual*
- *SH7000/7600 Programming Manual*

See also http://www.halsp.hitachi.com

Block Diagram



Note: The SH7020 has 16kB of ROM and 1kB of RAM. The SH7021 has 32kB of ROM and 1kB of RAM.

Block Diagram (SH7020/7021)

Instruction Set By Classification (Total: 56 Types)

Table 1 Data Transfer (5 Types)

Operation Code	Function
MOV	Data transfer, Immediate data transfer, Peripheral module and Structural data transfers
MOVA	Effective address transfer
MOVT	T-bit transfer
SWAP	Swap of upper and lower bytes
XTRCT	Extraction of middle of connected registers

Table 2 Arithmetic Operations (17 Types)

Operation Code	Function
ADD	Binary addition
ADDC	Binary addition with carry
ADDV	Binary addition with overflow check
CMP/cond.	Comparison
DIV1	Division
DIV0S	Initialization of signed division
DIV0U	Initialization of unsigned division
EXTS	Sign extension
EXTU	Zero extension
MAC	Multiplication and accumulation
MULS	Singed multiplication
MULU	Unsigned multiplication
NEG	Negation
NEGC	Negation with borrow
SUB	Binary subtraction
SUBC	Binary subtraction with borrow
SUBV	Binary subtraction with underflow check

Table 3 Logic Operations (6 Types)

Operation Code	Function
AND	Logic AND
NOT	Bit inversion
OR	Logical OR
TAS	Memory test and bit set
TST	Logical AND and T bit set
XOR	Exclusive OR

Table 4 Shift Instructions (10 Types)

Operation Code	Function
ROTL	One-bit left rotation
ROTR	One-bit right rotation
ROTCL	One-bit left rotation with T bit
ROTCR	One-bit right rotation with T bit
SHAL	One-bit arithmetic left shift
SHAR	One-bit arithmetic right shift
SHLL	One-bit logical left shift
SHLLn	n-bit logical left shift
SHLR	One-bit logical right shift
SHLRn	n-bit logical right shift

Table 5 Branch Instructions (7 Types)

Operation Code	Function
BF	Conditional branch (T = 0)
BT	Conditional branch (T = 1)
BRA	Unconditional branch
BSR	Branch to subroutine procedure
JMP	Unconditional branch
JSR	Branch to subroutine procedure
RTS	Return from subroutine procedure

Table 6 System Control (11 Types)

Operation Code	Function
CLRT	T bit clear
CLRMAC	MAC register clear
LDC	Load to control register
LDS	Load to system register
NOP	No operation
RTE	Return from exception processing
SETT	T bit set
SLEEP	Shift into power-down mode
STC	Storing control register data
STS	Storing system register data
TRAPA	Trap exception processing

DC Characteristics

Table 7 Current Consumption*[3], *[4]

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Ordinary operation	I_{CC}	—	65	80	mA	f = 12.5 MHz
Ordinary operation	I_{CC}	—	75	90	mA	f = 16.6 MHz
Ordinary operation	I_{CC}	—	90	100	mA	f = 20 MHz
Sleep	I_{CC}	—	30	50	mA	f = 12.5 MHz
Sleep	I_{CC}	—	35	55	mA	f = 16.6 MHz
Sleep	I_{CC}	—	40	60	mA	f = 20 MHz
Standby	I_{CC}	—	0.01	5	µA	Ta ≤ 50°C
Standby	I_{CC}	—	—	20.0	µA	50°C < Ta

Notes: Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 20 MHz, Ta = –20 to +75°C, Normal Products
Ta = –40 to +85°C for wide-temperature range products.

AC Characteristics

Table 8 LSI Clock Table

		Case A		Case B					
		12.5 MHz		16.6 MHz		20 MHz			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Figures**
EXTAL input high level pulse width	t_{EXH}	20	—	10	—	10	—	ns	1
EXTAL input low level pulse width	t_{EXL}	20	—	10	—	10	—	ns	
EXTAL input rise time	t_{EXr}	—	10	—	5	—	5	ns	
EXTAL input fall time	t_{EXf}	—	10	—	5	—	5	ns	
Clock cycle time	t_{cyc}	80	—	60	500	50	500	ns	1, 2
Clock high pulse width	t_{CH}	30	—	20	—	20	—	ns	2
Clock low pulse width	t_{CL}	30	—	20	—	20	—	ns	
Clock rise time	t_{Cr}	—	10	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	10	—	5	—	5	ns	
Reset oscillation settling time	t_{OSC1}	10	—	10	—	10	—	ms	3
Software standby oscillation settling time	t_{OSC2}	10	—	10	—	10	—	ms	

Note: Case A: V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C for normal products; Ta = –40 to +85°C for wide-temperature range products.

Case B: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, Ta = –20 to +75°C* for normal products; Ta = –40 to +85°C for wide-temperature range products.

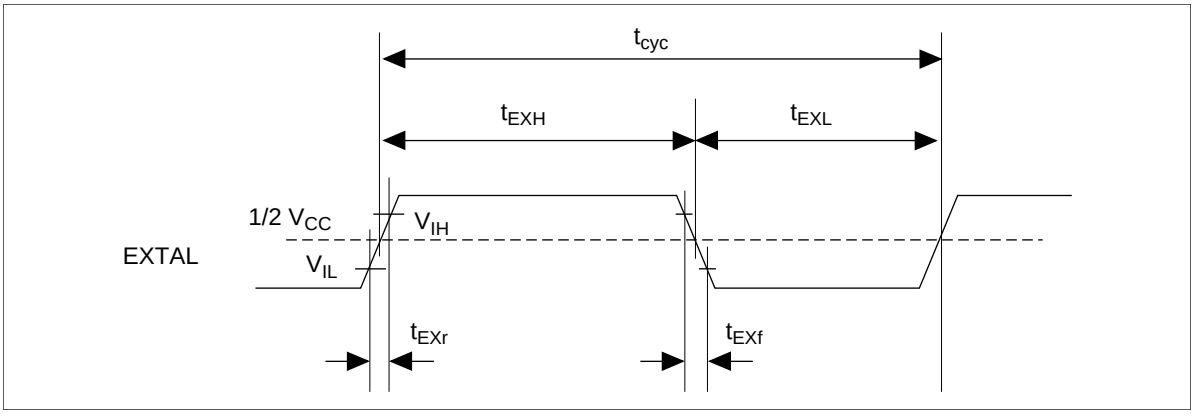


Figure 1 EXTAL Input Timing

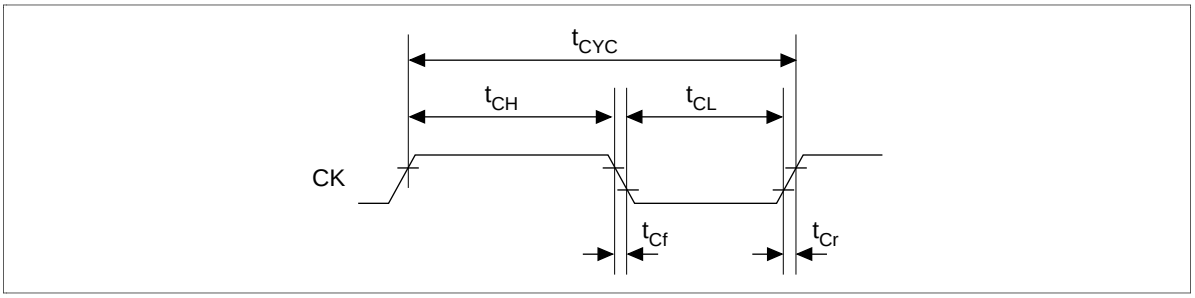


Figure 2 System Clock Timing

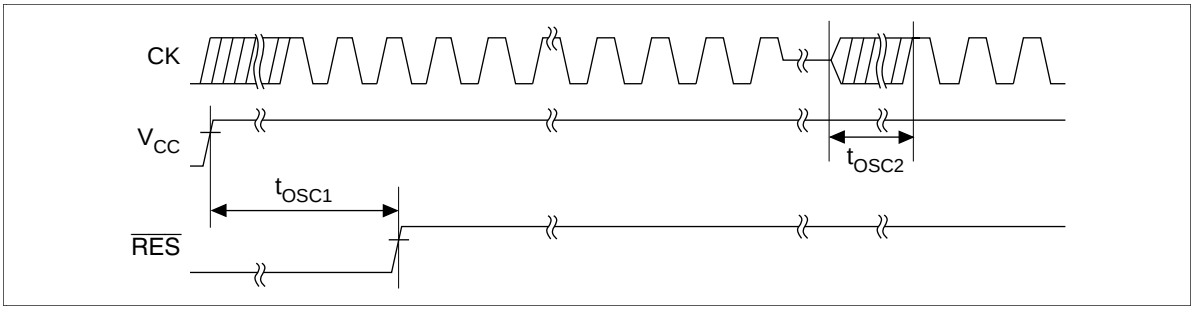
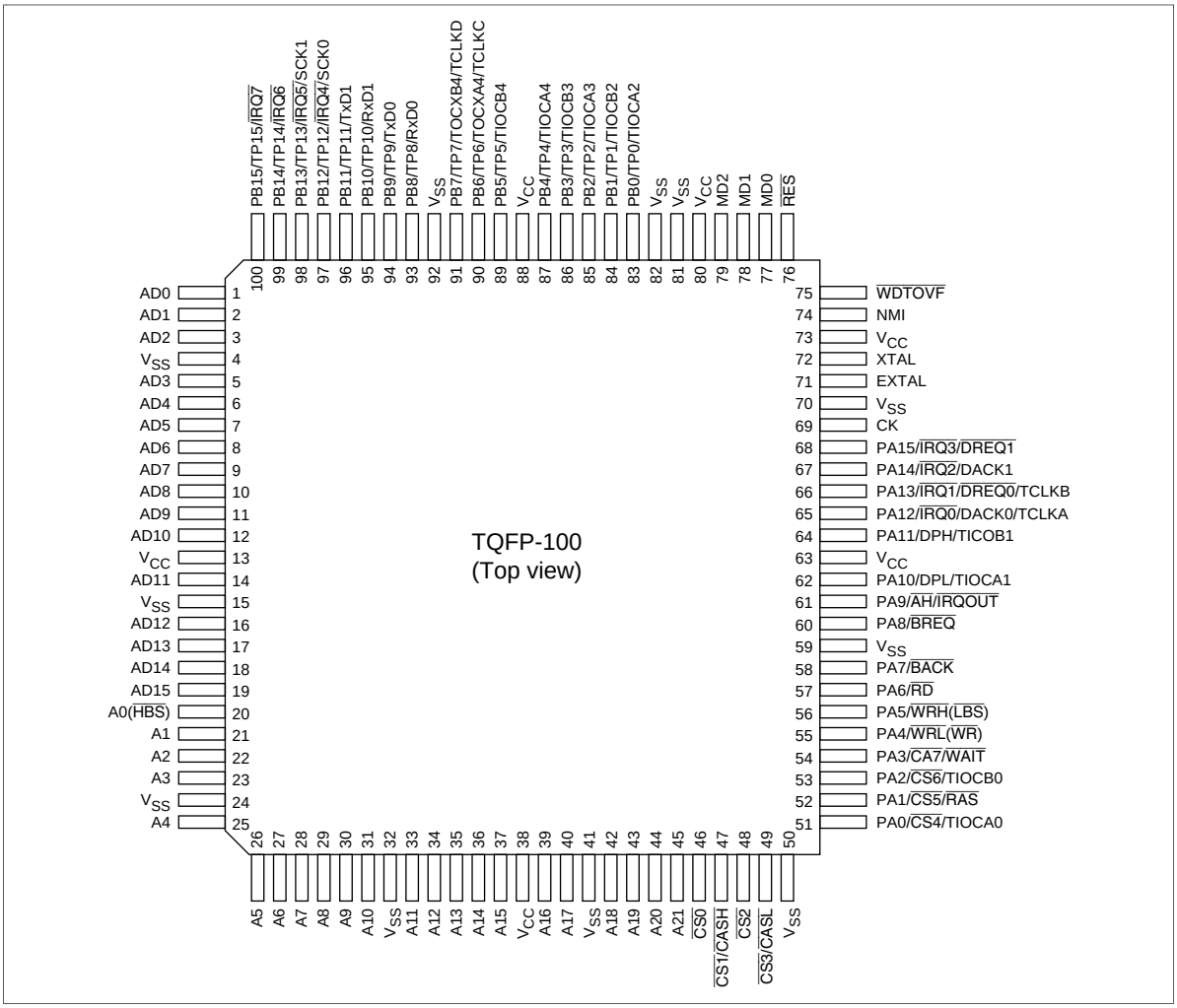


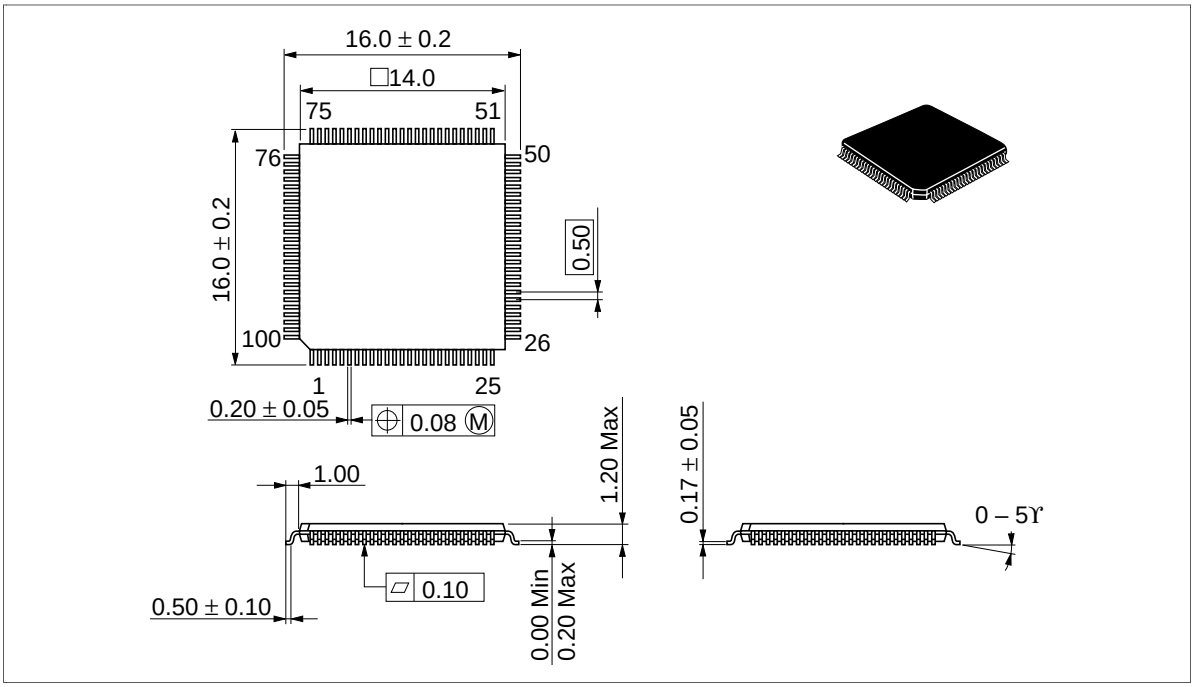
Figure 3 Oscillation Settling Time

Pin Diagrams



TQFP-100 (Top View)

Package Information



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