SH-2: SH7604 Product Brief

SH7600 Series 32-Bit RISC Embedded Processor

HITACHI

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Overview

The SH7600 Series is a reduced instruction set computer (RISC) that integrates a Hitachi-original RISC CPU and appropriate peripheral functions to minimize the components or modules required for system configuration.

The CPU has a RISC-type instruction set. Basic instructions can be executed in one clock cycle (36 ns), dramatically improving instruction execution speed. Operating up to 28.7 MHz, this processor also incorporates 4 kbytes of cache memory, a 32-bit internal architecture, and a 32-bit multiply and accumulate unit (MAC) for enhanced data-processing ability. As a result, the SH-2 enables high-performance systems to be constructed with advanced functionality at low cost, even in applications such as real-time control that require operations at very high speeds.

The SH7604 includes on-chip peripheral functions such as an interrupt controller, a direct memory access controller (DMAC), a division unit (DIVU), timers (free running timer/FRT and watchdog), and a serial communications interface (SCI). External memory support functions enable direct connection to SDRAM, DRAM, PSRAM, ROM, and peripheral I/O. Such features minimize the number of modules required for system configuration, and can reduce system costs.

Features

- 28.7 MHz at 5 V, 20 MHz at 3.3 V
- SH7604: 4-kbyte, Four-Way Set Associative Cache Memory
- RISC Central Processing Unit (CPU)
  - 32-bit internal data paths/32-bit external data paths
  - Five-stage pipeline
  - Sixteen 32-bit general registers, three 32-bit control registers, and four 32-bit system registers
- On-chip multiply and accumulate unit
  - Multiplication operations ($32 \times 32 \rightarrow 64$ bits) executed in 2 to 3 cycles
  - MAC operations ($32 \times 32 \rightarrow 64 + 64$ bits) executed in 2 to 3 cycles
- Operating modes:
  - Clock mode selected from the combination of an on-chip oscillator module, a double-frequency circuit, clock output, PLL synchronization, and 90° phase change
  - Slave/master mode
  - Processing mode

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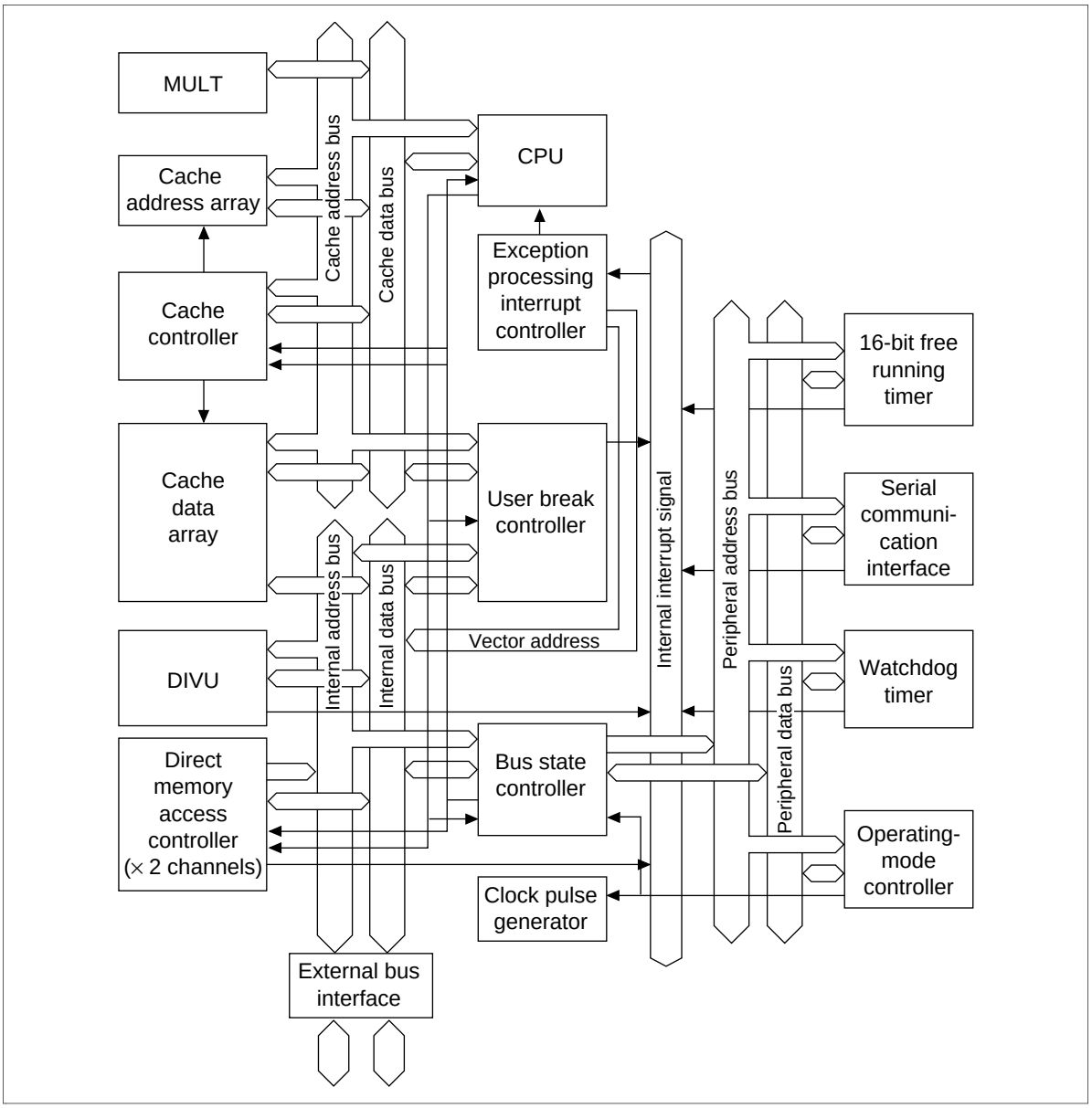
- Processing states:
  - — Power-on reset/manual reset
  - — Exception processing
  - — Program execution
  - — Power-down (sleep, standby, and moduel stop modes)
  - — Bus-released
  - — On-chip Lock Pulse Generator (CPG)
    Selectable double-frequency circuit, clock output, PLL synchronization or 90° phase change
- Bus State Controller (BSC)
  - — Supports interface to SDRAM, PSRAM, DRAM, ROM, and peripheral I/O
  - — Supports external memory (32/16/8-bit external data bus) access
  - — Memory refresh and burst access functions
  - — Wait states can be inserted by external WAIT signal
- Two-Channel Direct Memory Access Controller (DMAC)
  - — DMA transfers between external memory, external I/O, and on-chip peripheral modules
  - — Selectable priorities and modes
  - — Dual or single address transfer mode
- Division Unit (DIVU)
  - — 64/32 → 32…32 and 32/32 → 32…32 divisions
  - — Overflow interrupt
- Interrupt Controller (INTC)
  - — Five external interrupt pins
  - — Eleven internal interrupt sources
  - — Sixteen programmable priority levels
- 16-Bit Free Running Timer (FRT)
  - — Input selects from three internal/external clocks
  - — Input capture and output compare
  - — Counter overflow, compare match, and input capture interrupt
- Watchdog Timer (WDT)
- One-channel SCI with full duplex and asynchronous/synchronous selectable modes
- User Break Controller (UBC) for generating interrupts to simplify debugging
- Operating temperature: –20°C to 75°C
- Package: 144-pin Quad Flat Pack (QFP)
- Process: 0.8 micron technology
- Complete development system support

Related Manuals

- *SH Series Overview*
- *SH7604 Hardware Manual*
- *SH7000/7600 Programming Manual*

See also http://www.halsp.hitachi.com.

Block Diagram



Block Diagram (SH7604)

Instruction Set By Classification (Total: 61 Types)

Table 1 Data Transfer (5 Types)

Operation Code	Function
MOV	Data transfer, immediate data transfer, peripheral module, and structural data transfers
MOVA	Effective address transfer
MOVT	T-bit transfer
SWAP	Swap of upper and lower bytes
XTRCT	Extraction of middle of connected registers

Table 2 Arithmetic Operations (20 Types)

Operation Code	Function
ADD	Binary addition
ADDC	Binary addition with carry
ADDV	Binary addition with overflow check
CMP/cond.	Comparison
DIV1	Division
DIV0S	Initialization of signed division
DIV0U	Initialization of unsigned division
DMULS	Double-length signed multiplication
DMULU	Double-length unsigned multiplication
DT	Decrement and test
EXTS	Sign extension
EXTU	Zero extension
MAC	Multiplication and accumulation
MULS	Signed multiplication
MULU	Unsigned multiplication
NEG	Negation
NEGC	Negation with carry
SUB	Binary subtraction
SUBC	Binary subtraction with carry
SUBV	Binary subtraction with underflow check

Table 3 Logic Operations (6 Types)

Operation Code	Function
AND	Logic AND
NOT	Bit inversion
OR	Logical OR
TAS	Memory test and bit set
TST	Logical AND and T bit set
XOR	Exclusive OR

Table 4 Shift Instructions (10 Types)

Operation Code	Function
ROTL	One-bit left rotation
ROTR	One-bit right rotation
ROTCL	One-bit left rotation with T bit
ROTCR	One-bit right rotation with T bit
SHAL	One-bit arithmetic left shift
SHAR	One-bit arithmetic right shift
SHLL	One-bit logical left shift
SHLLn	n-bit logical left shift
SHLR	One-bit logical right shift
SHLRn	n-bit logical right shift

Table 5 Branch Instructions (9 Types)

Operation Code	Function
BF	Conditional branch (T = 0)
BT	Conditional branch (T = 1)
BRA	Unconditional branch
BRAF	Unconditional branch
BSR	Branch to subroutine procedure
BRSF	Branch to subroutine procedure
JMP	Unconditional branch
JSR	Branch to subroutine procedure
RTS	Return from subroutine procedure

Table 6 System Control (11 Types)

Operation Code	Function
CLRT	T bit clear
CLRMAC	MAC register clear
LDC	Load to control register
LDS	Load to system register
NOP	No operation
RTE	Return from exception processing
SETT	T bit set
SLEEP	Shift into power-down mode
STC	Storing control register data
STS	Storing system register data
TRAPA	Trap exception processing

DC Characteristics (5 V)

Table 7 DC Characteristics (Condition V_{CC} = 5.0 V ± 10%, Ta = –20 to +75° C)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Current consumption	Ordinary operation	I_{CC}	—	60	80	mA	f = 8 MHz
			—	80	100	mA	f = 16 MHz
			—	110	160	mA	f = 28.7 MHz
	Sleep		—	30	55	mA	f = 8 MHz
			—	50	70	mA	f = 16 MHz
			—	80	100	mA	f = 28.7 MHz
	Standby		—	1	15	µA	Ta ≤ 50°C
			—	—	60	µA	50°C < Ta

AC Characteristics (5 V)

Table 8 LSI Clock Timing (V_{CC} = 5.0 V ± 10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit
Operating frequency	f_{OP}	4	28.7	MHz
Clock cycle time	t_{cyc}	35	143*[1] or 250*[2]	ns
Clock high pulse width	t_{CH}	8*[1] or 15*[2]	—	ns
Clock low pulse width	t_{CL}	8*[1] or 15*[2]	—	ns
Clock rise time	t_{CR}	—	5	ns
Clock fall time	t_{CF}	—	5	ns
EXTAL clock input frequency	f_{EX}	4	8	MHz
EXTAL clock input cycle time	t_{EXcyc}	125	250	ns
EXTAL clock input low level pulse width	t_{EXL}	50	—	ns
EXTAL clock input high level pulse width	t_{EXH}	50	—	ns
EXTAL clock input rise time	t_{EXR}	—	5	ns
EXTAL clock input clock fall time	t_{EXF}	—	5	ns
Power-on oscillation settling time	t_{OSC1}	10	—	ms
Software standby oscillation settling time 1	t_{OSC2}	10	—	ms
Software standby oscillation settling time 2	t_{OSC3}	10	—	ms
PLL synchronization settling time	t_{PLL}	1	—	µs

Notes 1. With PLL circuit 1 operating.
2. With PLL circuit 1 not used.

DC Characteristics (3.3 V)

Table 9 DC Characteristics (Condition V_{CC} = 3.0 to 5.5 V, Ta = –20 to +75° C)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD5–MD0	V_{IH}	V_{CC}×0.9	—	V_{CC} + 0.3	V	During standby
			V_{CC}×0.9	—	V_{CC} + 0.3	V	Normal operation
	EXTAL, CKIO		V_{CC}×0.9	—	V_{CC} + 0.3	V	
	Other input pins		V_{CC}×0.7	—	V_{CC} + 0.3	V	
Input low-level voltage	$\overline{RES}$, NMI, MD5–MD0	V_{IL}	–0.3	—	V_{CC}×0.1	V	During standby
			–0.3	—	V_{CC}×0.1	V	Normal operation
	Other input pins		–0.3	—	V_{CC}×0.1	V	
Input leak current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD5–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Other input pins		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
3-state leak current (while off)	A26–A0, D31–D0, $\overline{BS}$, $\overline{CS3}$–$\overline{CS0}$, RD/$\overline{WR}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE3}$-$\overline{WE0}$, $\overline{RD}$, $\overline{IVECF}$	$\|I_{STI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low-level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input capacitance	$\overline{RES}$	Cin	—	—	15	pF	Vin = 0 V f = 1 MHz Ta = 25°C
	NMI		—	—	15	pF	
	All other input pins (D31–D0)		—	—	15	pF	

Table 9 DC Characteristics (Condition V_{CC} = 3.0 to 5.5 V, Ta = –20 to +75° C) (cont)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Current consump-tion	Ordinary operation	I_{CC}	—	25	30	mA	f = 8 MHz
			—	45	55	mA	f = 16 MHz
			—	60	70	mA	f = 28.7 MHz
	Sleep		—	15	20	mA	f = 8 MHz
			—	30	40	mA	f = 16 MHz
			—	40	50	mA	f = 28.7 MHz
	Standby		—	1	5	µA	Ta ≤ 50°C
			—	—	20	µA	50°C < Ta

Notes: 1. When no PLL is used, do not release the $PLLV_{CC}$ and $PLLV_{SS}$ pins. Connect $PLLV_{CC}$ to V_{CC} and $PLLV_{SS}$ to V_{SS}.
2. Current consumption values shown are the values at which all output pins are without load under conditions of V_{IH} min = V_{CC} - 0.5 V, V_{IL} max = 0.5 V.

AC Characteristics (3.3 V)

Table 10 Clock Timing (V_{CC} = 3.0 to 0.5 V, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit
Operating frequency	f_{OP}	4	20	MHz
Clock cycle time	t_{cyc}	35	143[*1] or 250[*2]	ns
Clock high pulse width	t_{CH}	8[*1] or 15[*2]	—	ns
Clock low pulse width	t_{CL}	8[*1] or 15[*2]	—	ns
Clock rise time	t_{CR}	—	5	ns
Clock fall time	t_{CF}	—	5	ns
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EXTAL clock input cycle time	t_{EXcyc}	125	250	ns
EXTAL clock input low level pulse width	t_{EXL}	50	—	ns
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EXTAL clock input rise time	t_{EXR}	—	5	ns
EXTAL clock input clock fall time	t_{EXF}	—	5	ns
Power-on oscillation settling time	t_{OSC1}	10	—	ms
Software standby oscillation settling time 1	t_{OSC2}	10	—	ms
Software standby oscillation settling time 2	t_{OSC3}	10	—	ms
PLL synchronization settling time	t_{PLL}	1	—	µs

Notes: 1. With PLL circuit 1 operating.
2. With PLL circuit 1 not used.

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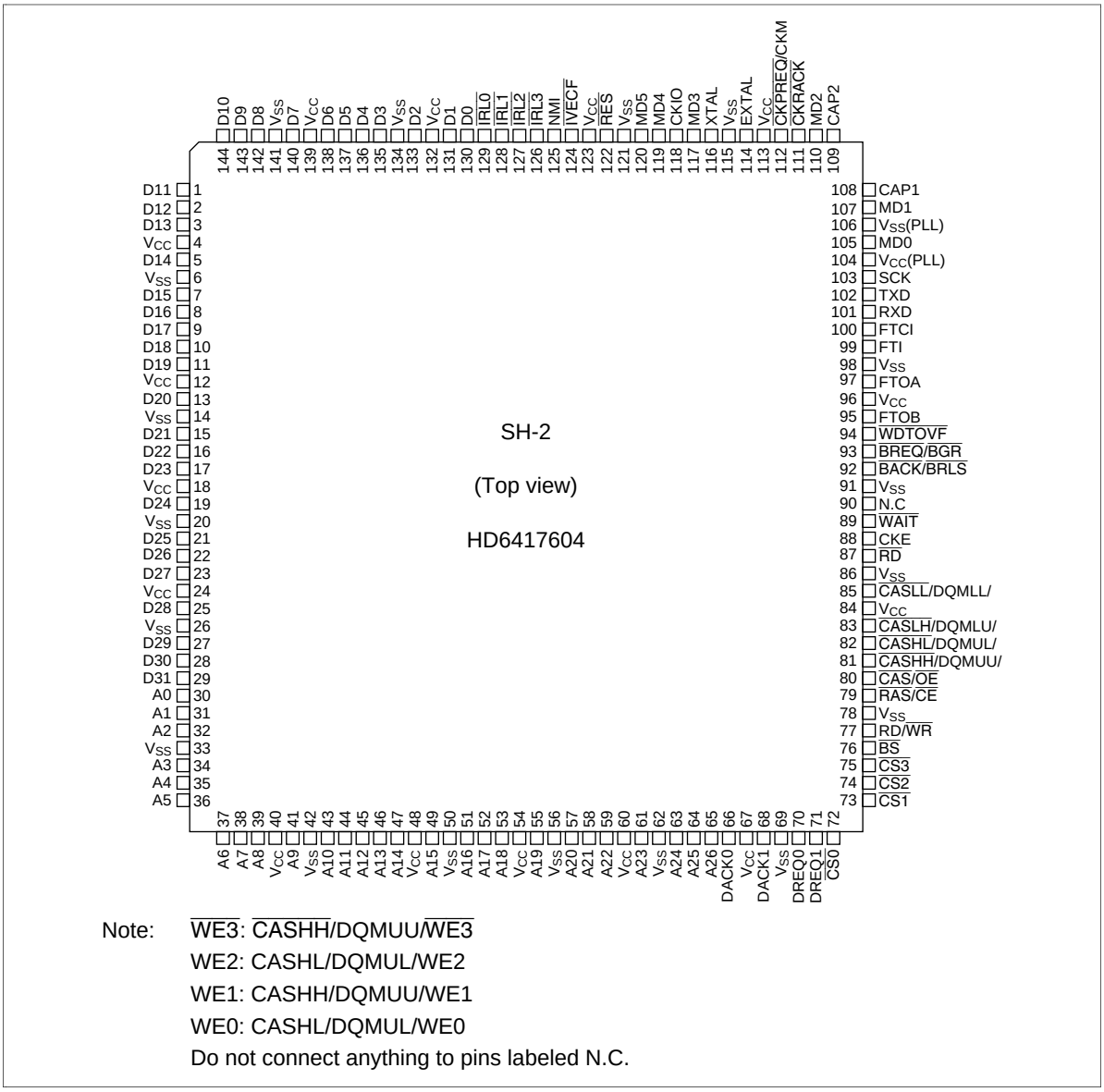
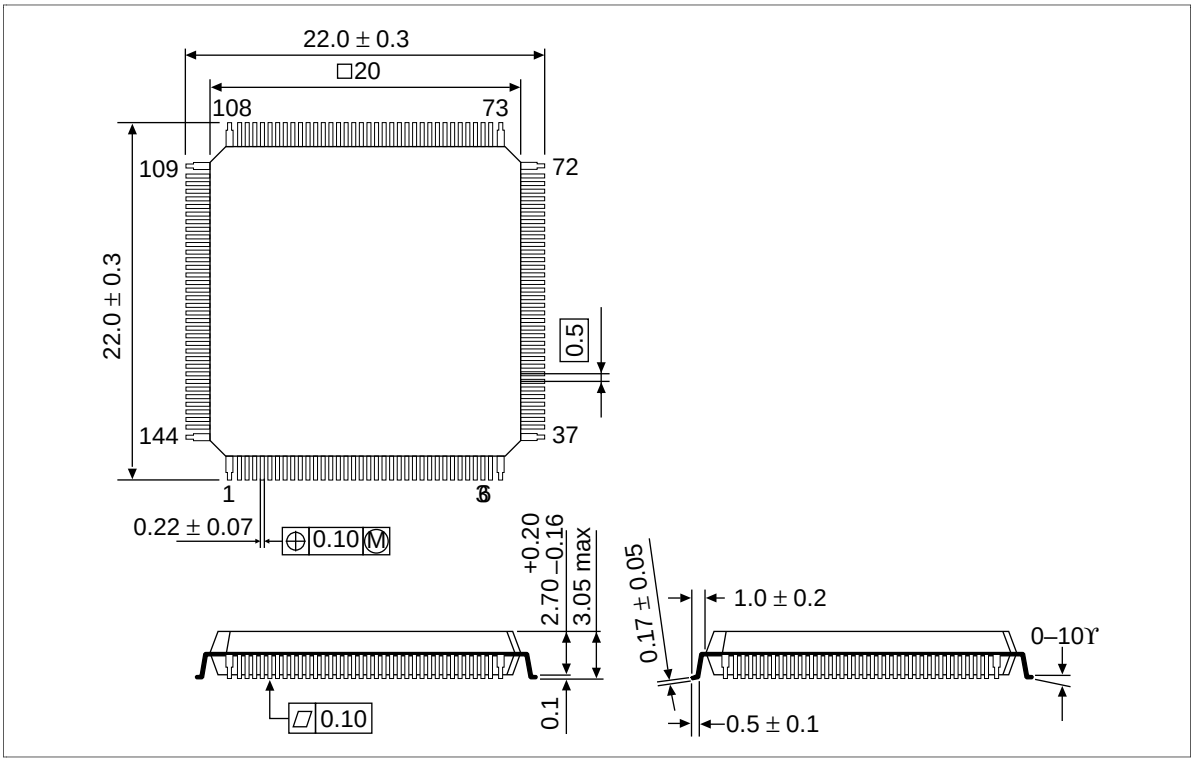
Pin Diagram



Note: WE3: CASHH/DQMUU/WE3
WE2: CASHL/DQMUL/WE2
WE1: CASHH/DQMUU/WE1
WE0: CASHL/DQMUL/WE0
Do not connect anything to pins labeled N.C.

Package Dimensions


22.0 ± 0.3
□20
108
73
109
72
22.0 ± 0.3
0.5
144
37
1
0.22 ± 0.07
0.10 M
+0.20
2.70 –0.16
3.05 max
0.17 ± 0.05
1.0 ± 0.2
0–10°
0.10
0.1
0.5 ± 0.1

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