

UTMI+ White Paper

Introduction

As people start using more and more mobile devices in their everyday lives, component manufacturers are stepping up to the plate by delivering more and more powerful devices that make our lives more interesting, connected, communicative, action-packed, productive, and a lot more fun. We are talking to each other more; sending images of our everyday lives to each other more; posting our images and our thoughts to the web more; and working and interacting in virtual space more. For example, you may not know where all your friends and co-workers are right now, but chances are you can contact them in minutes using a computer, beeper, mobile phone, or other mobile device.

If you don't have a mobile phone yet, you will get one soon. Once you have a mobile phone, you need a PDA to organize your life. Once you have a PDA, you need a digital camera to record your life and it just keeps getting more interesting. Once these mobile devices become so deeply engrained in your life, you wonder why you need to go back to the computer to download, upload, and synchronize each of the devices. The effort and the time it takes are annoying. You could be out doing things instead of stuck in front of an immobile PC. Well, other people have been wondering the same thing and they have been doing something about it. They created a standard that adds an important building block for direct, mobile-device communication. The standard is UTMI+.

UTMI+ specifies an interface for transceiver macrocells that are created by semiconductor companies and IP vendors for use by ASIC developers and component manufacturers to place in mobile devices so they can communicate directly to each other without requiring a host PC. The UTMI+ transceiver macrocell is a small and important building block for the future of mobile communication.

UTMI+ is:

- **USB 2.0^[1]** certified.
- **UTMI^[2]** compliant using UTMI+ Level 0.
- **On-The-Go^[3]** compliant using UTMI+ Level 1/2/3.

UTMI+ Implementation

The UTMI+ standard contains progressive levels of technology support because the complexity requirements for devices can vary widely. For example, in OTG devices, the complexity needed for the host controller block is directly dependent on the targeted peripheral list. The different UTMI+ levels allow the designer to implement an ASIC with the required complexity level without having to design in unused logic.

The levels provide a layered support structure:

- **Level 0** is fully compatible with UTMI.
- **Level 1** adds support for USB OTG dual-role devices that generate high-speed (HS) and full-speed (FS) traffic.
- **Level 2** adds support for generating low-speed (LS) traffic towards LS devices that are directly connected to the OTG device.
- **Level 3** adds support for using USB 2.0 FS hubs in the system. It lets the host controller part of the OTG dual-role device communicate with LS devices that are connected to a USB FS hub controller.

UTMI+ transceiver cores developed to a given level are compliant with all the lower level features. Figure 1 provides a general overview of how the different levels fit together.

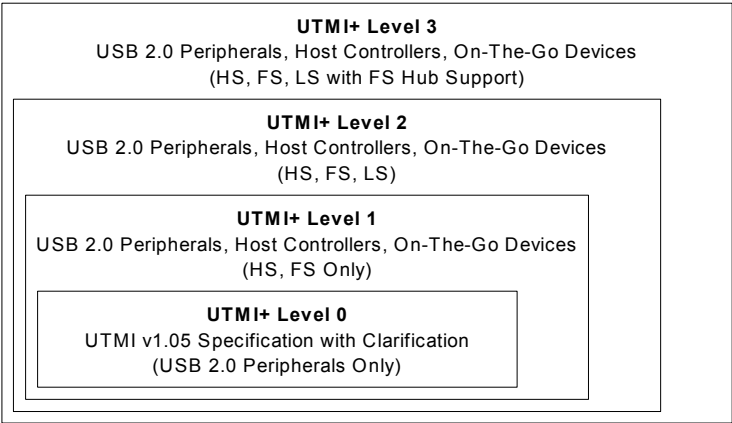


Figure 1 UTMI+ Levels

Level 0: USB 2.0 Peripheral Support

The base UTMI+ specification, Level 0, matches the UTMI specification pin-for-pin and provides a few clarifications to the UTMI specification. A UTMI+ transceiver core working at Level 0 can be used in a USB peripheral design to replace a UTMI transceiver. Because of limitations of the UTMI specification, transceiver cores working at Level 0 cannot be used to implement USB 2.0 Hosts or OTG peripherals without inserting additional logic. The Level 0 interface supports both 16 bit and 8 bit logic. The interface configuration shown in Figure 2 is for 16 bit high-speed logic, a subset of the pins can be used to match a UTMI interface for 8 bit logic for FS only or LS only devices.

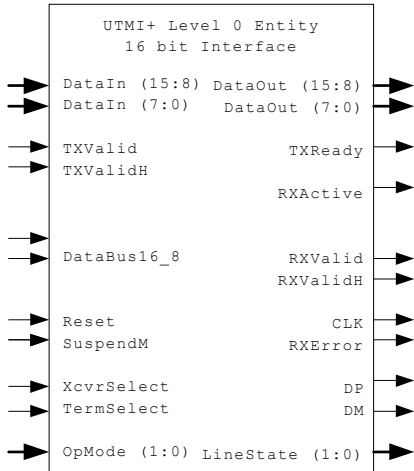


Figure 2 UTMI+ Level 0 Interface Entity Diagram

Use UTMI+ Level 1, 2, or 3 compliant transceiver cores for USB 2.0 Hosts and OTG devices.

Level 1: Level 0 + Hosts and OTG Devices (HS and FS only)

UTMI+ Level 1 interface compliant transceiver cores contain all the signals specified in UTMI+ Level 0 as well as twenty-one additional signals. These signals make the transceiver core compliant with the OTG standard. Devices created using this level can be used for peripherals, hosts, and OTG dual-role devices that support HS and FS traffic. See Figure 3 for a graphical representation of the UTMI+ Level 1/2/3 interface specifications.

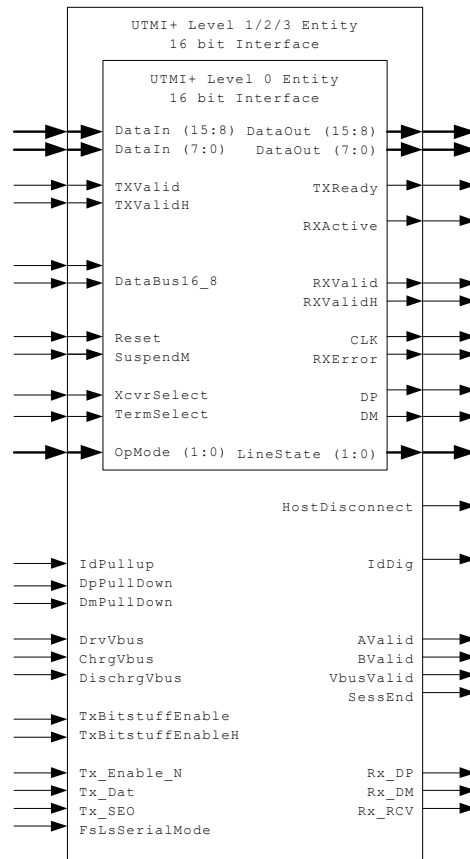


Figure 3 UMTI+ Level 1/2/3 Interface Entity Diagram

Depending on the requirements of the device under development a Level 2 or Level 3 compliant transceiver core may be required instead of a Level 1 core. For example, if a host controller requires communication with an LS device or an FS Hub, additional functions will be required that are part of Level 2 and Level 3 respectively.

Support for On-The-Go Devices

The OTG standard supports the design of portable devices, providing peripheral-to-peripheral connectivity without the requiring a host PC. It allows mobile phones, hand-helds, PDAs, keyboards, cameras, or anything with an OTG interface to be connected to each other as a peripheral, a host, or a dual-role device. Because of their added functionality, OTG devices require additional signals on the transceiver interface.

Some of the specialized requirements on a Level 1 transceiver interface are the ability to:

- Distinguish between mini-A and mini-B receptacles for dual-role devices.
- Sense the voltage level on the USB bus.

- Drive the USB bus power to feed current, charge, and discharge the Vbus.
- Control Dp and Dm pull down resistors.
- Detect a high-speed peripheral disconnect.

Additional UTMI+ Level 1 Signals

There are twenty-one additional signals for Level 1 compliant transceiver cores. Here is an introduction to the signals and their usage:

- **Avalid** indicates if an A-peripheral is attached.
- **Bvalid** indicates if a B-peripheral is attached.
- **DpPullDown** / **DmPullDown** are set to different levels depending on whether the device is acting as a host or a peripheral.
- **DrvVbus** is an enable signal for the Vbus that is optional for Level 1. Its use depends on whether an integrated charge pump is implemented or not. If the DrvVbus signal is active, the **DischrgVbus** and **ChrgVbus** signals are used to signal charging and discharging of the Vbus.
- **FsLsSerialMode** indicates how the digital core signals FS and LS packets to the transceiver. Packets are communicated either by a parallel interface or serial interface. This makes it possible to reuse an existing FS/LS host controller IP without changing its interface. The **Tx_Enable_N**, **Tx_DAT**, **Tx_Se0**, **Rx_DP**, **Rx_DM**, and **Rx_RCV** signals are active when the serial mode is used.
- **HostDisconnect** indicates when the host is disconnected from a peripheral.
- **IdDig** indicates the state of the ID pin on the USB mini receptacle making it possible to determine which type of plug is connected. To save power, the **IdPullup** signal determines when to sample the analog Id line.
- **OpMode** is extended to control all bits that are sent on the USB bus and to provide a HS keep-alive packet on the USB bus.
- **SessEnd** signals when the voltage on the Vbus is below the B-device session-end threshold.
- **TxBitstuffEnable** / **TxBitstuffEnableH** work with OpMode under certain conditions to provide Bitstuff information and transmission.
- **VbusValid** indicates whether or not the voltage on Vbus is at a valid level for operation.

Additional UTMI+ Level 1 Features

The features are:

- **Generation of Long EOP:** Most HS USB packets that are generated with an 8-bit EOP but, when an SOF is sent on the USB bus, the EOP must be 40 bits.
- **Data Line Pulsing:** Data line pulsing can be implemented using the XcvrSelect, DpPullDown, DmPullDown and TermSelect signals.
- **HS Keep-Alive Generation:** In certain cases, the debug port of an EHCI compliant host controller needs to transmit a HS keep-alive SYNC packet without any other data or EOP.

Using a UTMI+ Level 1 Transceiver Core in a USB 2.0 Peripheral

A UTMI+ Level 1 transceiver core can be used with an UTMI compliant SIE for a USB 2.0 peripheral by tying off or leaving open the twenty-one additional Level 1 signals.

Level 2: Level 1 + Direct Connection LS Support

UTMI+ Level 2 interface compliant transceiver cores are used for devices that handle LS traffic but don't require FS hub support. Level 2 covers all USB traffic described in the USB 2.0 specification with the exception of a host sending an LS packet to a USB LS device that is connected through an FS hub (PRE PID handling). For FS hub support, choose a Level 3 compliant transceiver core.

Some of the specialized requirements on a Level 2 compliant transceiver core is its ability to:

- Support the LS data rate.
- Generate LS keep-alive packets on LS USB ports.
- Control the LS edge rate.

Additional UTMI+ Level 2 Features

Transceiver cores that are interface compliant with UTMI+ Level 2 contain all the signals specified in UTMI+ Level 1 plus a few additional features.

The features are:

- **DrvVbus** is used for a transceiver implementation that supports an integrated charge pump. DrvVbus is mandatory for implementations using an SIE interface that is compliant with UTMI+ Level 2.
- **LineState** indicates SEO, J-State, K-State, or SE1 depending on the values of downstream and upstream facing ports.
- **LS keep-alive generation** on an LS bus requires the signals on UTMI+ level 2 interface to be asserted in a special order. The SIE sets TxValid with XcvrSelect in LS transceiver mode and TxData 0xA5 on the 8 LSB. The transceiver decodes this assertion and sends a low-speed keep-alive packet on the USB bus.
- **XcvrSelect** selects between HS, FS, and LS transceiver support.

Level 3: Level 2 + Full Speed Hub Support

UTMI+ Level 3 interface compliant transceiver cores are used when devices require FS hub support. They handle LS traffic that is sent from the host to the LS device using an FS hub. To use the additional functionality provided by this level, the host core must be able to generate preamble packets.

Some of the specialized requirements on a Level 3 compliant transceiver core is its ability to:

- Switch to an LS data rate within a transaction.
- Support LS preamble PID (PRE-PID)

Additional UTMI+ Level 3 Features

UTMI+ Level 3 interface compliant transceiver cores contain all the signals specified in UTMI+ Level 2 plus a few additional features.

The features are:

- **Multi-port host controllers** are supported. Transceiver IP vendors who want to support multi-port host applications can provide a mechanism to tie multiple transceivers to a single UTMI clock for connection to a single SIE in the host controller.
- **XcvrSelect** has four settings to select between: HS, FS, LS transceivers, and the ability to send or receive an LS packet on an FS bus. XcvrSelect controls a number of transceiver related elements: it selects the receiver; it is used as a gating term for enabling the HS, FS or LS Transmit Driver; and it switches internal UTMI clocks to shared logic.

Benefits

- Non-proprietary industry standard.
- Digital core reusability.
- OTG dual-role devices (DRD) supported.
- 1.5 Mbps, 12Mbps, and 480 Mbps data transfer rates are supported.
- 0.8 V to 5 V devices can be driven through the USB connector.
- Compatible with all previous USB standards: USB 1.1, USB 2.0, UTMI, and OTG.
- Compliant transceiver macrocell IPs are available from multiple sources.
- Transceiver cores are available in different levels of complexity to match device requirements.

Acronyms

Acronym	Definition
ASIC	Application Specific Integrated Circuit
DRD	Dual Role Devices
EOP	End of Packet
FS	Full Speed (12 Mbps)
HC	Host Controller
HNP	Host Negotiation Protocol
HS	High Speed (480 Mbps)
IP	Intellectual Property
LS	Low Speed (1.5 Mbps)
OTG	On-The-Go ^[3]
PDA	Portable Digital Assistant
PRE	Preamble
SIE	Serial Interface Engine
SoC	Systems on a Chip
SRP	Session Request Protocol
USB	Universal Serial Bus ^[3]
USB-IF	USB Implementers Forum
UTMI	USB 2.0 Transceiver Macrocell Interface ^[2]
UTMI+	UTMI extension supporting On-The-Go ^[1]

Relevant Documents

1. USB 2.0 Specification, April 27, 2000
2. USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, version 1.05, March 29, 2001
3. On-The-Go Supplement to the USB 2.0 Specification, revision 1.0, Dec 18, 2001
4. UTMI+ Specification, revision 0.9, February 21, 2003

UTMI+ Standards Group Member Companies

These UTMI+ member companies provided technical support toward the development of the UTMI+ Specification, revision 0.9, February 21, 2003:

- Cypress Semiconductor Corp.
- Gain
- Innovative
- MCCI
- Mentor Graphics
- Philips Semiconductors
- Portalplayer Inc.
- S3
- STMicroelectronics
- Synopsys
- TransDimension