

A working computer from Nand and DFF

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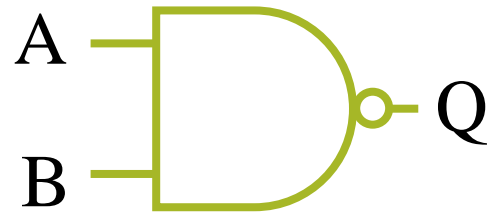
24/02/2021

About the project

1. Computer hardware
 - University individual project
 - Hardware Descriptive Language
2. Assembler
 - Individual project
 - C++
3. Nand & D Flip-flop calculator
 - Part of University team project
 - C++

Nand

What is Nand?

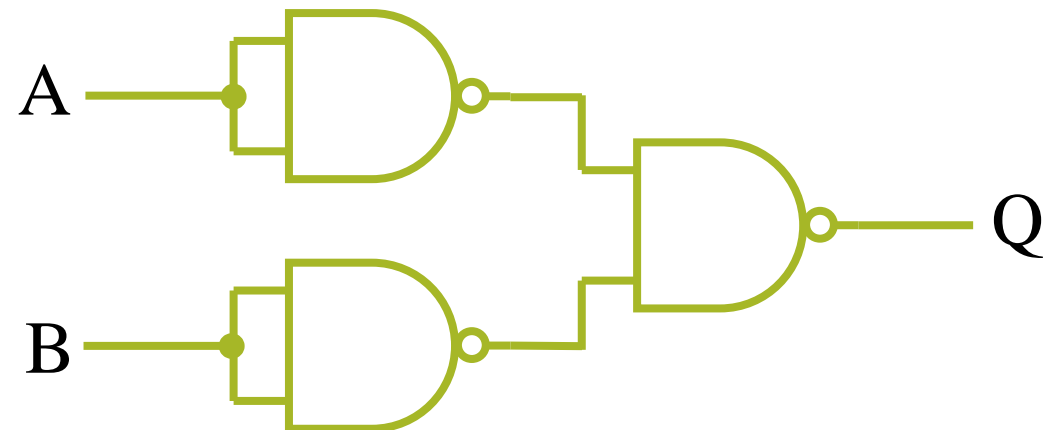


| A | B | Q |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Functional completeness

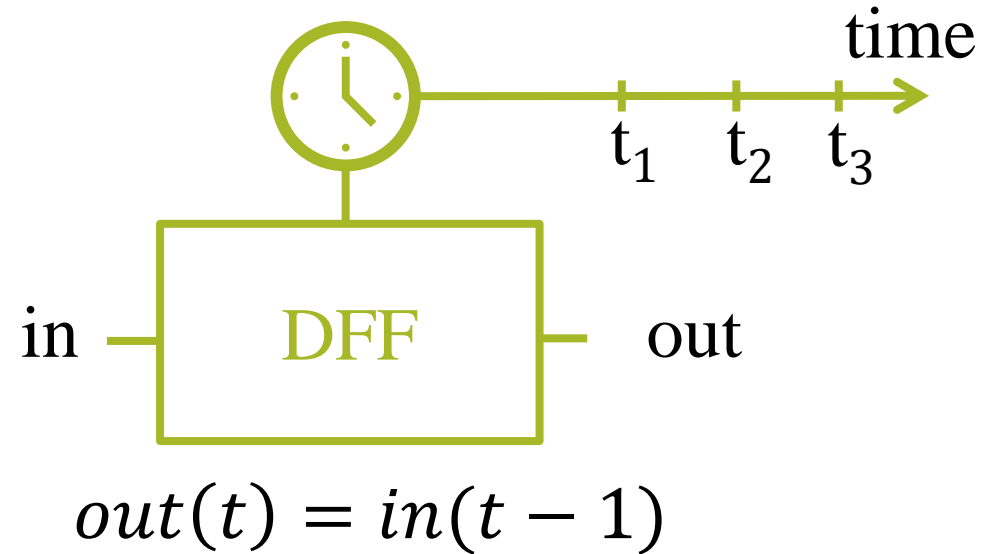
Any logic function can
be made from Nands!

Example: Or



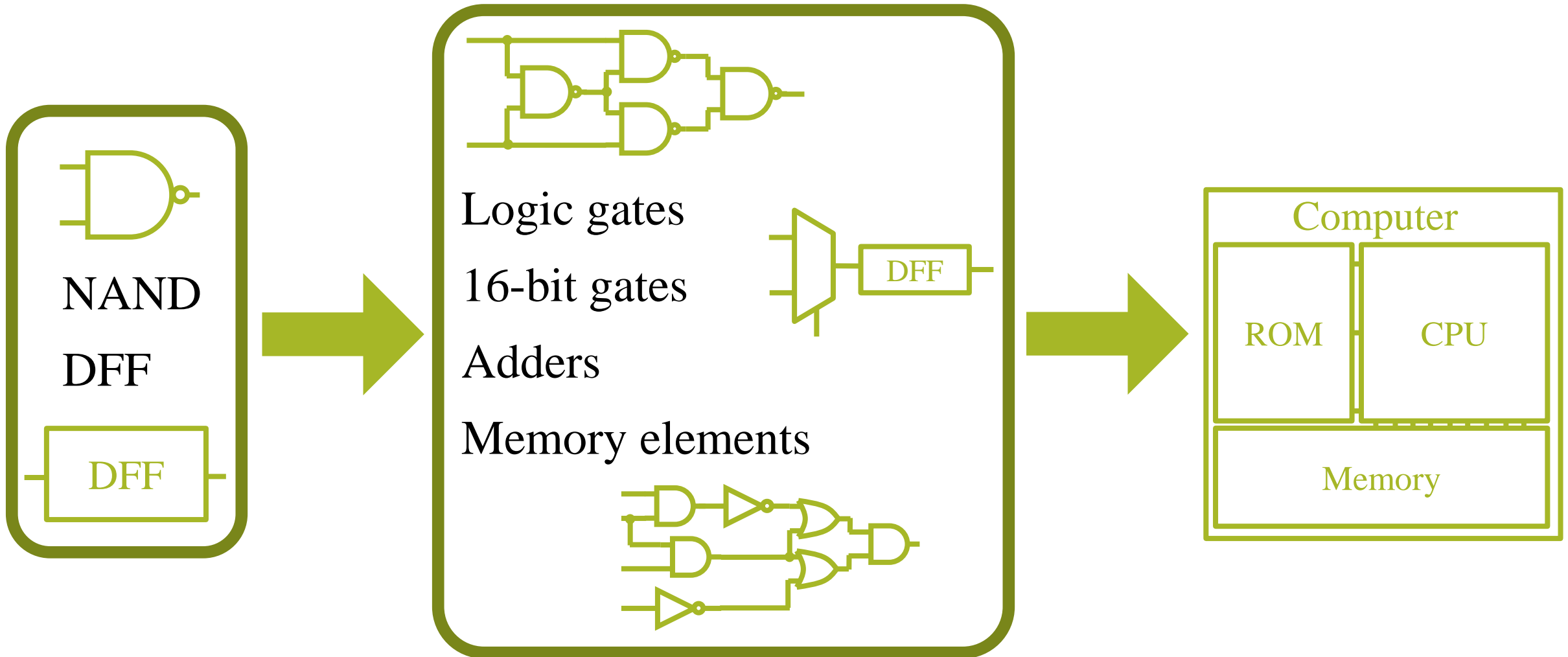
D Flip-Flop

What is D Flip-Flop (DFF)?



D Flip-Flop can be constructed from NANDs!

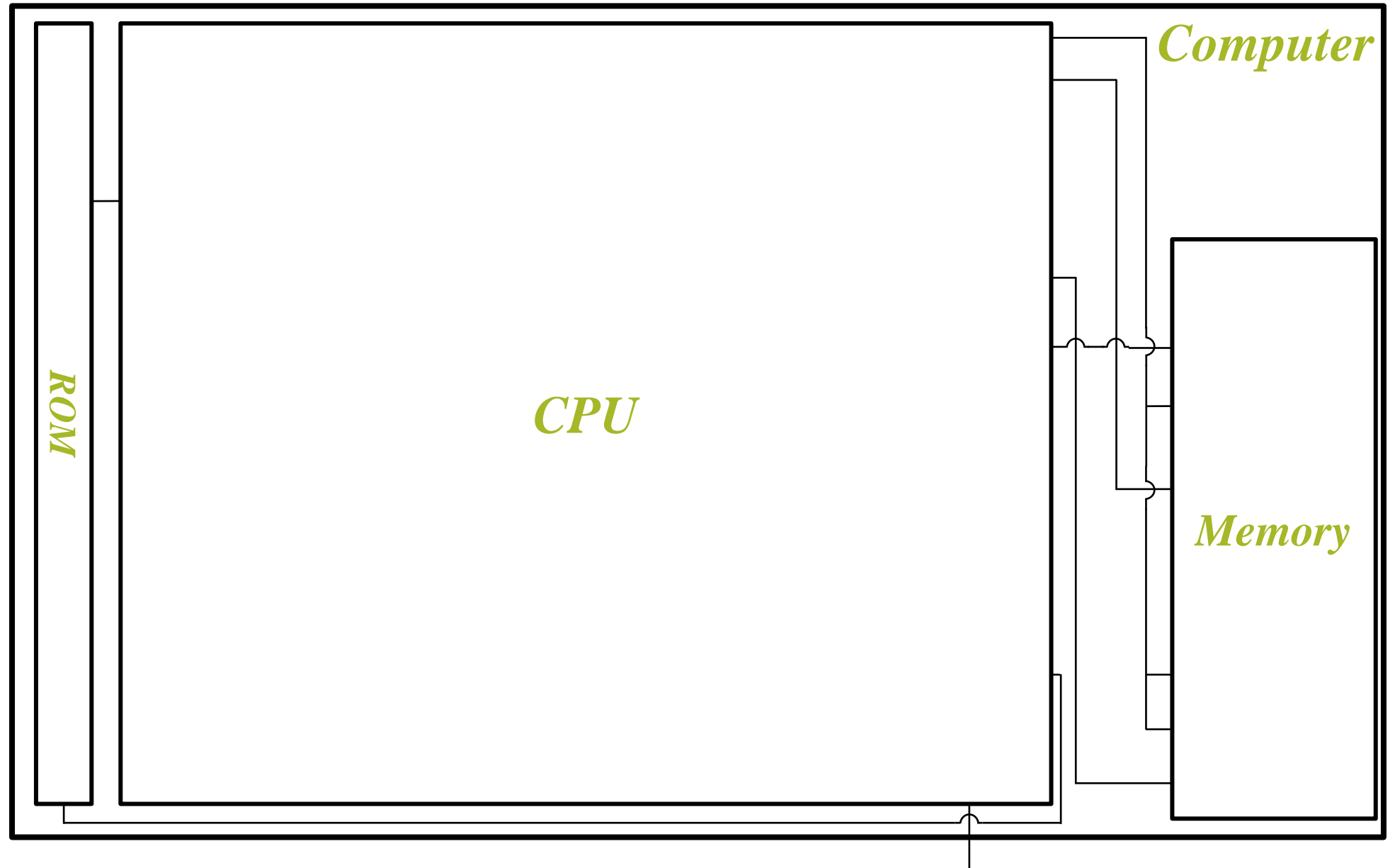
Implementing computer



Computer Diagram

- Memory
- ROM
- CPU

2,104,280 Nands
254,016 DFFs
in this design!



No internal structure shown here, can be provided only by request.

Memory

Random Access Memory (RAM)

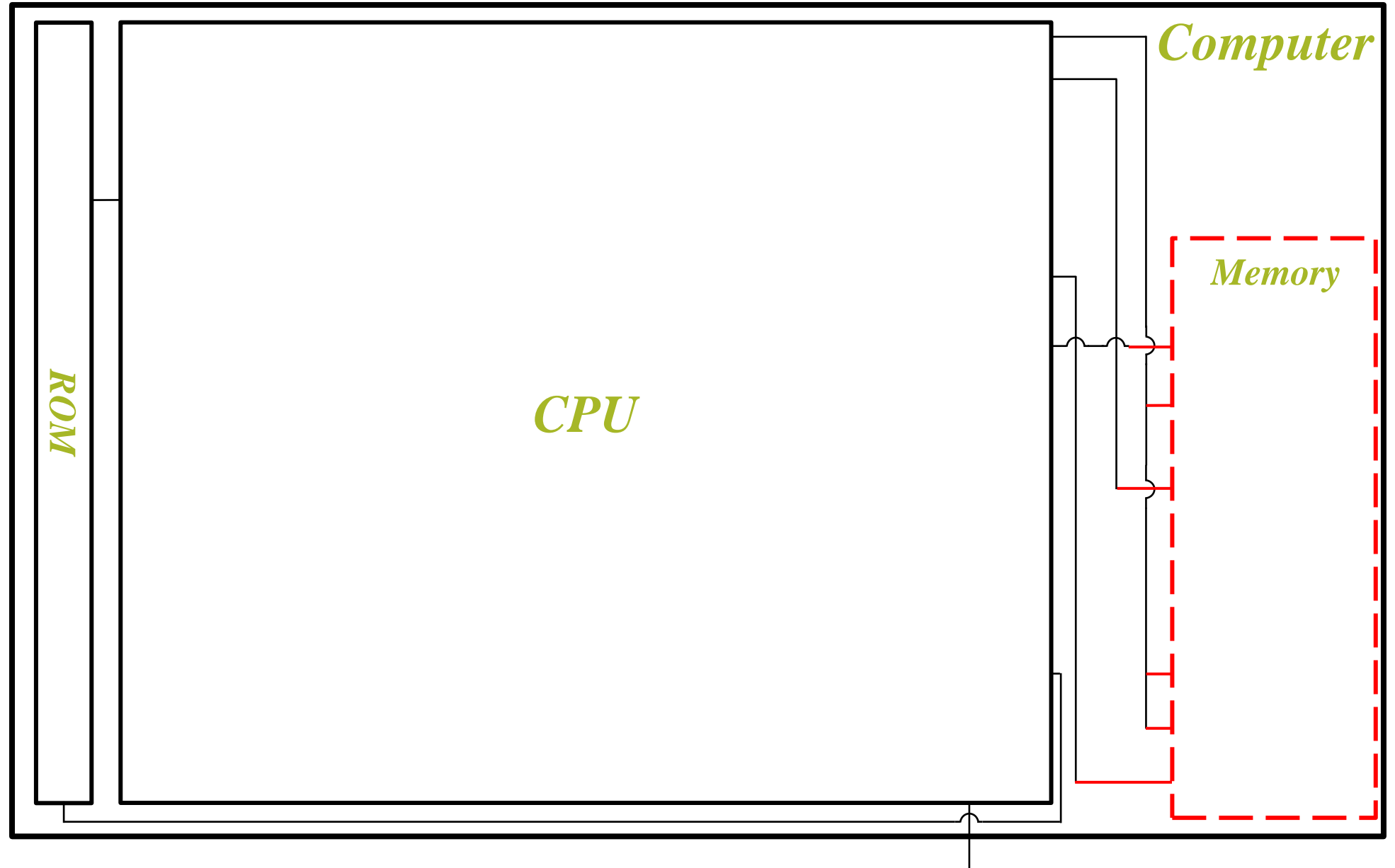
- 32 kB of data

Screen:

- 512×256 px
- 131072 bits
- 0 = white
- 1 = black

Keyboard:

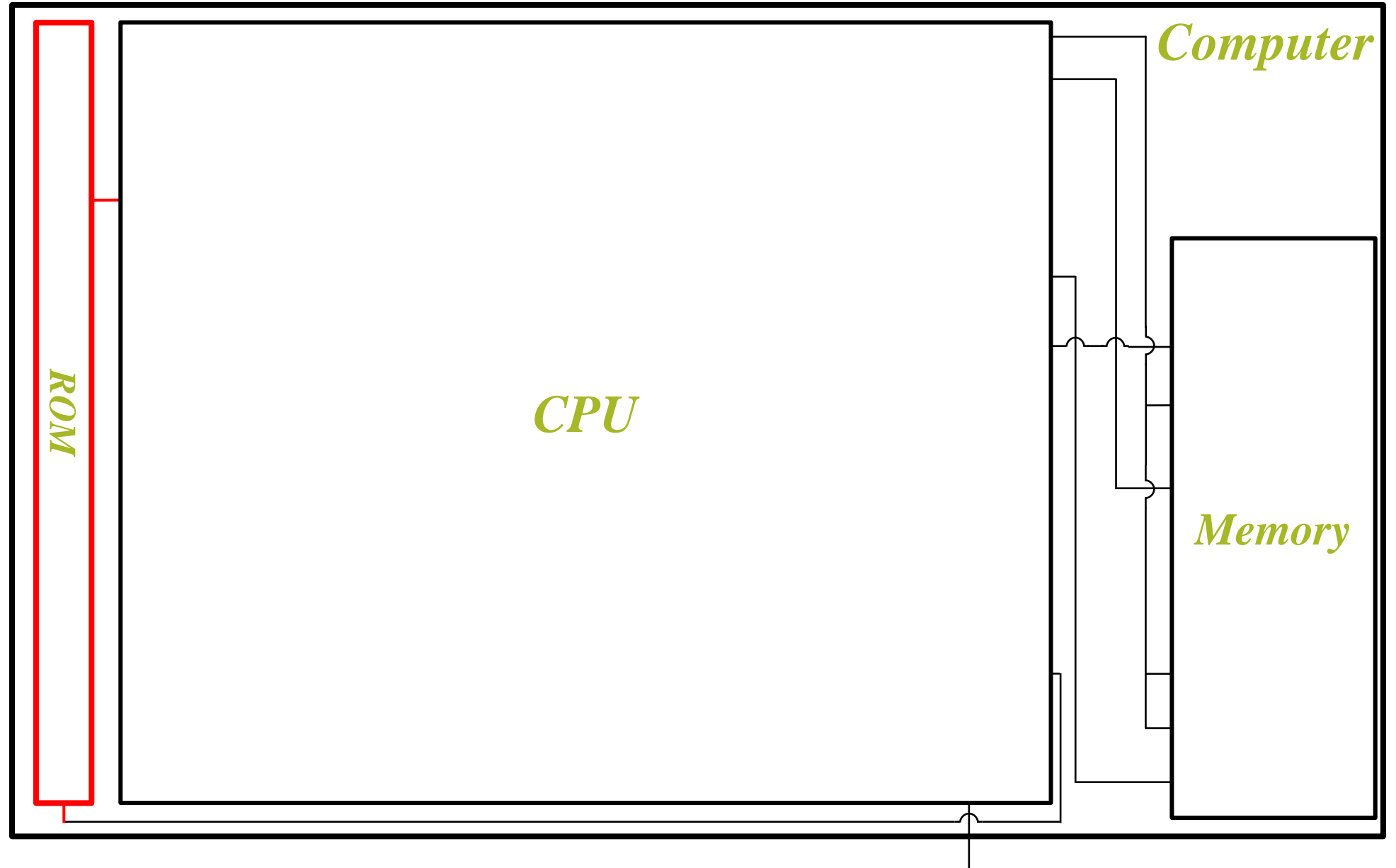
- 16 bit
- ASCII code



ROM

Read-Only
Memory (ROM):

- 64 kB of Instructions

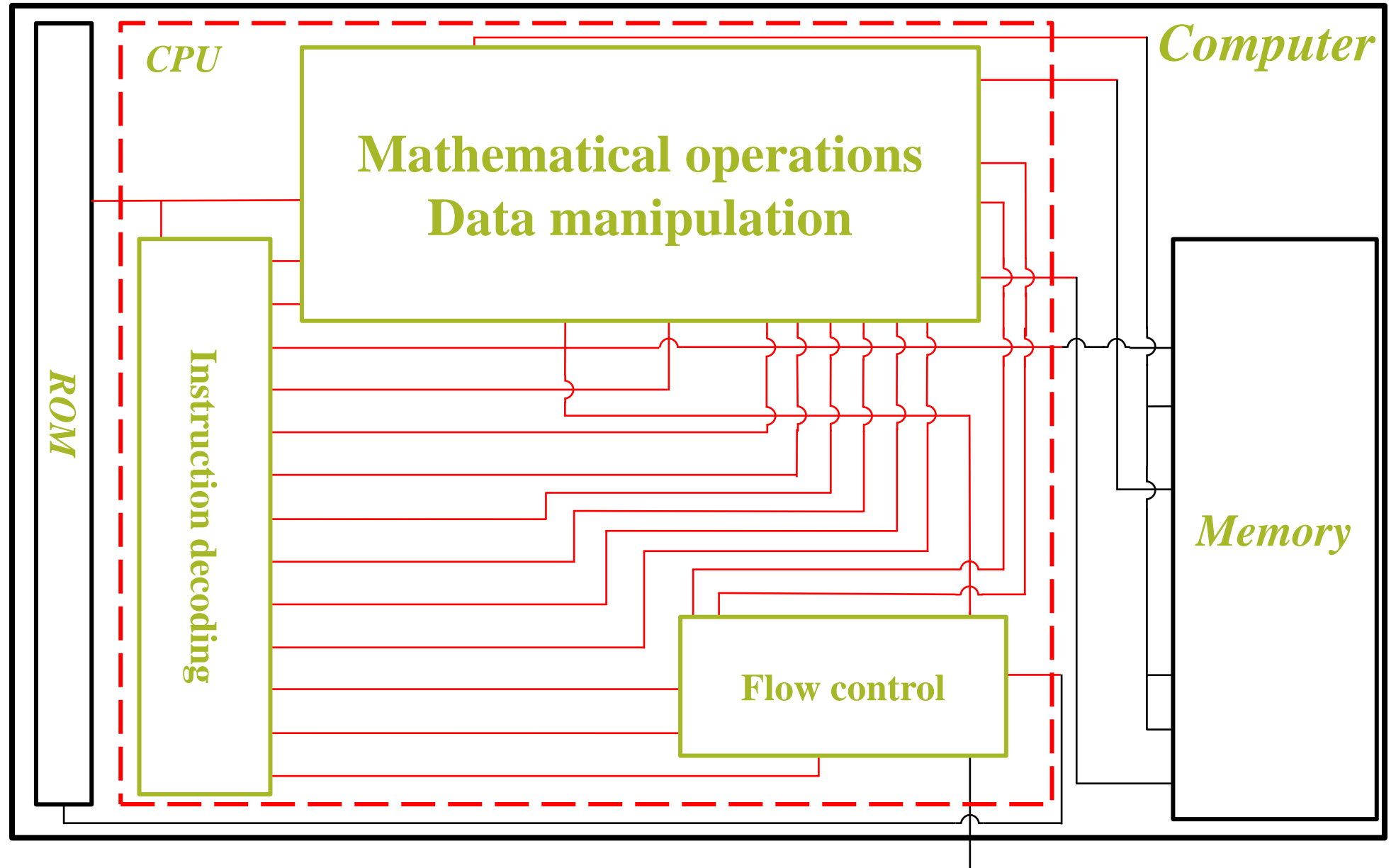


CPU

Central
Processing Unit
(CPU):

- Instruction decoding
- Mathematical operations & Data manipulation
- Flow control

Understanding
software helps
understanding
hardware!



Assembler

- Assembly language – human
- Binary code – computer hardware
- Assembler function: converting assembly language into binary code

The assembly process:

1. Removing spaces/comments
2. Replacing variables/labels
3. Parsing each line into fields
4. Translating fields into binary
5. Combining into result

Assembly process – Example

1. Removing all spaces and comments

| Before | | After | |
|--------|---------------------|-------|-----------|
| 0 | @R0 | 0 | @R0 |
| 1 | D = M | 1 | D=M |
| 2 | @result | 2 | @result |
| 3 | M = 0 | 3 | M=0 |
| 4 | (LOOP) | 4 | (LOOP) |
| 5 | @result | 5 | @result |
| 6 | M = D + M // update | 6 | M=D+M |
| 7 | @LOOP | 7 | @LOOP |
| 8 | D = D - 1; JGT | 8 | D=D-1;JGT |
| 9 | (END) | 9 | (END) |
| 10 | // endless loop | 11 | @END |
| 11 | @END | 12 | 0;JMP |
| 12 | 0; JMP | | |

Example

| Before | | | After | |
|--------|-----------------|---|-------|-----------|
| 8 | D = D - 1; JGT | → | 8 | D=D-1;JGT |
| 10 | // endless loop | → | 10 | |

Assembly process – Example

2. Replacing all variables and labels

| Before | | After | |
|--------|-----------|-------|-----------|
| 0 | @R0 | 0 | @0 |
| 1 | D=M | 1 | D=M |
| 2 | @result | 2 | @16 |
| 3 | M=0 | 3 | M=0 |
| 4 | (LOOP) | 5 | @16 |
| 5 | @result | 6 | M=D+M |
| 6 | M=D+M | 7 | @4 |
| 7 | @LOOP | 8 | D=D-1;JGT |
| 8 | D=D-1;JGT | 10 | @8 |
| 9 | (END) | 11 | 0;JMP |
| 11 | @END | | |
| 12 | 0;JMP | | |

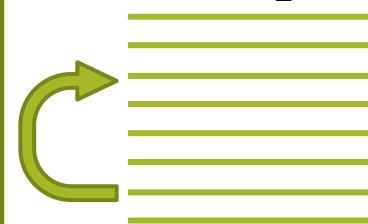
Variable – name for memory address

Example

| Before | | | After | |
|--------|---------|---|-------|-----|
| 2 | @result | → | 2 | @16 |

Label – name for a line

Loops



If/else



Example

| Before | | | After | |
|--------|--------|---|-------|----|
| 4 | (LOOP) | → | 4 | |
| 10 | @LOOP | → | 10 | @4 |

Assembly process – Example

3. Parsing each line into its fields

| Before | | After | | | |
|--------|-----------|-------|-------|------|------|
| | | A | value | | |
| | | C | comp | dest | jump |
| 0 | @0 | 0 A | 0 | | |
| 1 | D=M | 1 C | M | D | Null |
| 2 | @16 | 2 A | 16 | | |
| 3 | M=0 | 3 C | 0 | M | Null |
| 4 | @16 | 4 A | 16 | | |
| 5 | M=D+M | 5 C | D+M | M | Null |
| 6 | @4 | 6 A | 4 | | |
| 7 | D=D-1;JGT | 7 C | D-1 | D | JGT |
| 8 | @8 | 8 A | 8 | | |
| 9 | 0;JMP | 9 C | 0 | Null | JMP |

| Assembly code | |
|---------------|-------------------|
| A | @value |
| C | dest = comp; jump |

Example

| Before | | | After | | | |
|---------------|-----------|---|-------|--------------|-------------|-------------|
| A-instruction | | | | | | |
| | | | | <i>value</i> | | |
| 2 | @16 | → | A | 16 | | |
| C-instruction | | | | | | |
| | | | | <i>comp</i> | <i>dest</i> | <i>jump</i> |
| 7 | D=D-1;JGT | → | C | D-1 | D | JGT |

Assembly process – Example

4. Translating individual fields into binary

| Before | | | | After | | | |
|------------|--------------|-------------|-------------|--------------|------------------|-------------|-------------|
| A | <i>value</i> | | | A | <i>value</i> | | |
| C | <i>comp</i> | <i>dest</i> | <i>jump</i> | C | <i>comp</i> | <i>dest</i> | <i>jump</i> |
| 0 A | 0 | | | 0 0 | 0000000000000000 | | |
| 1 C | M | D | Null | 1 111 | 1110000 | 010 | 000 |
| 2 A | 16 | | | 2 0 | 0000000000010000 | | |
| 3 C | 0 | M | Null | 3 111 | 0101010 | 001 | 000 |
| 4 A | 16 | | | 4 0 | 0000000000010000 | | |
| 5 C | D+M | M | Null | 5 111 | 1000010 | 001 | 000 |
| 6 A | 4 | | | 6 0 | 0000000000000100 | | |
| 7 C | D-1 | D | JGT | 7 111 | 0001110 | 010 | 001 |
| 8 A | 8 | | | 8 0 | 0000000000001000 | | |
| 9 C | 0 | Null | JMP | 9 111 | 0101010 | 000 | 111 |

Example

| Before | | | | | After | | | |
|---------------|-------------|--------------|-------------|------------|----------|------------------|----------------|-----------------------|
| A-instruction | | | | | | | | |
| | | <i>value</i> | | | | <i>value</i> | | |
| 6 | A | 4 | | → | 0 | 0000000000000100 | | |
| C-instruction | | | | | | | | |
| | <i>comp</i> | <i>dest</i> | <i>jump</i> | | | <i>comp</i> | <i>dest</i> | <i>jump</i> |
| 7 | C | D-1 | D | JGT | → | 111 | 0101010 | 010 001 |

Assembly process – Example

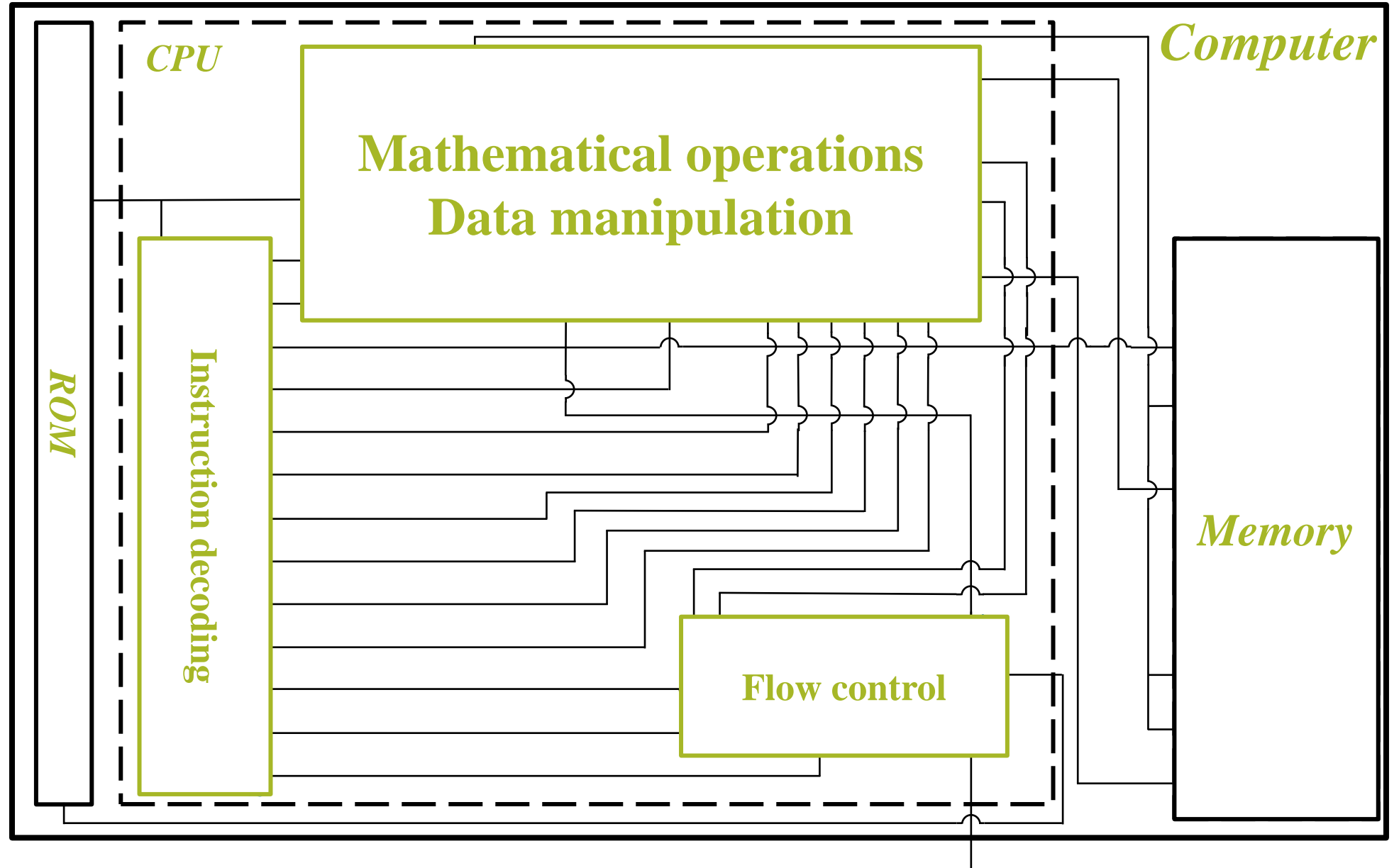
5. Combining translated fields into result

| Before | | | | | After | |
|--------|-----|------------------|-------------|-------------|-------|------------------|
| A | | <i>value</i> | | | | |
| C | | <i>comp</i> | <i>dest</i> | <i>jump</i> | | |
| 0 | 0 | 0000000000000000 | | | 0 | 0000000000000000 |
| 1 | 111 | 1110000 | 010 | 000 | 1 | 1111110000010000 |
| 2 | 0 | 0000000000010000 | | | 2 | 0000000000010000 |
| 3 | 111 | 0101010 | 001 | 000 | 3 | 1110101010001000 |
| 4 | 0 | 0000000000010000 | | | 4 | 0000000000010000 |
| 5 | 111 | 1000010 | 001 | 000 | 5 | 1111000010001000 |
| 6 | 0 | 0000000000000100 | | | 6 | 0000000000000100 |
| 7 | 111 | 0001110 | 010 | 001 | 7 | 1110001110010001 |
| 8 | 0 | 0000000000001000 | | | 8 | 0000000000001000 |
| 9 | 111 | 0101010 | 000 | 111 | 9 | 1110101010000111 |

Test correctness?

Load it into the computer!

CPU

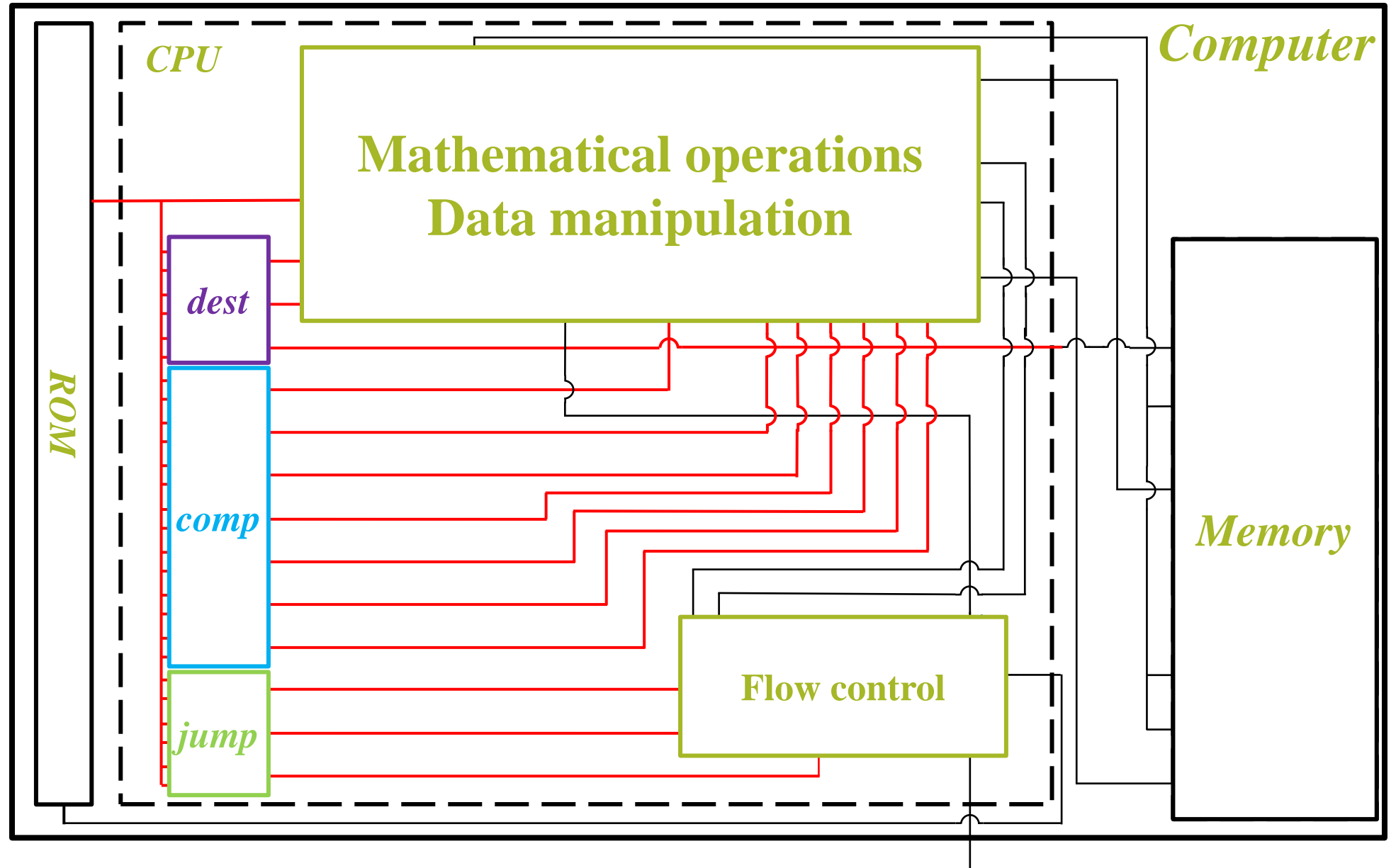


Instruction
decoding

A-instruction

C-instruction

| | Assembly code |
|----------|---|
| A | @ <i>value</i> |
| C | <i>dest</i> = <i>comp</i> ; <i>jump</i> |

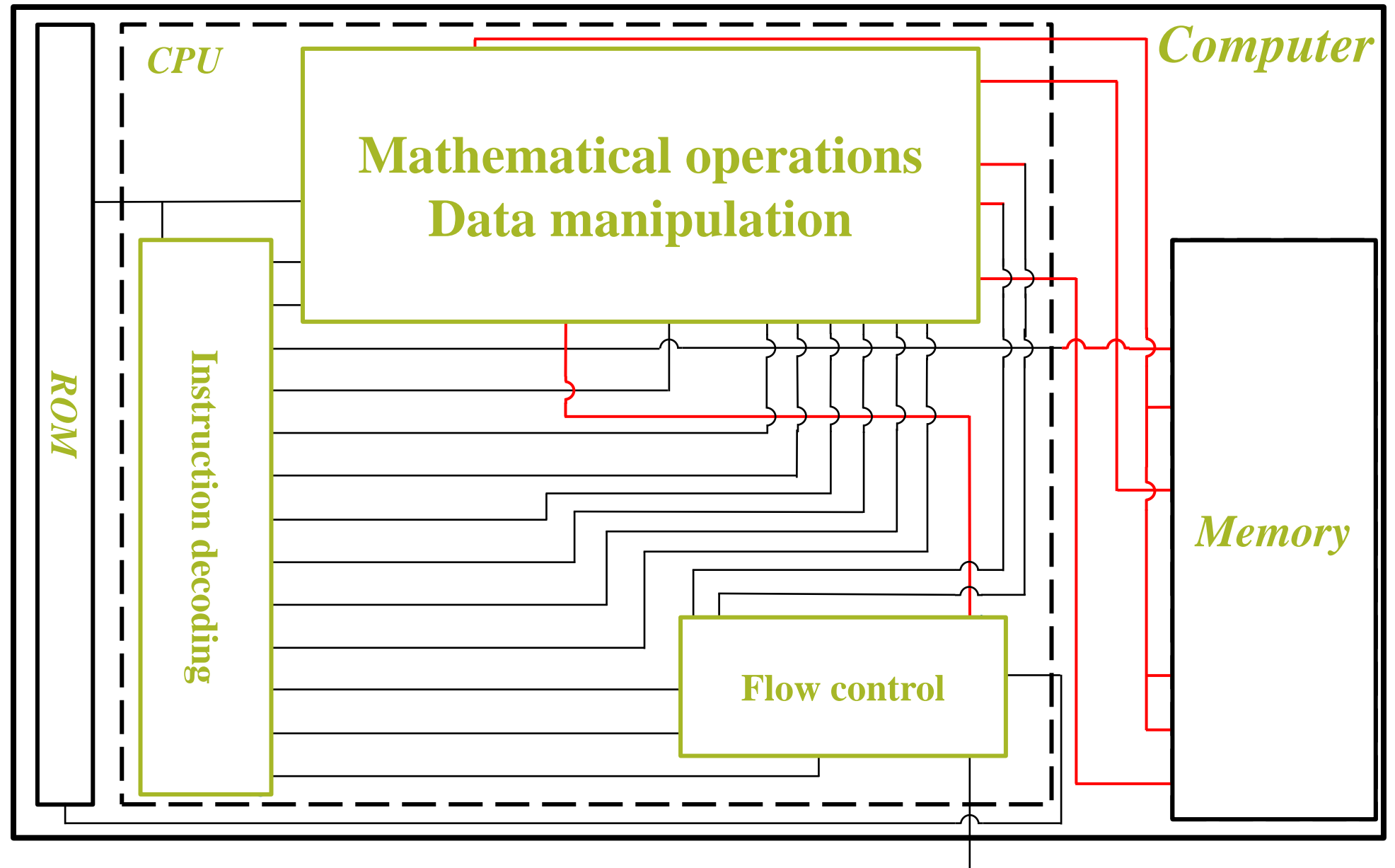


Execution

ARegister

DRegister

Arithmetic
Logic Unit

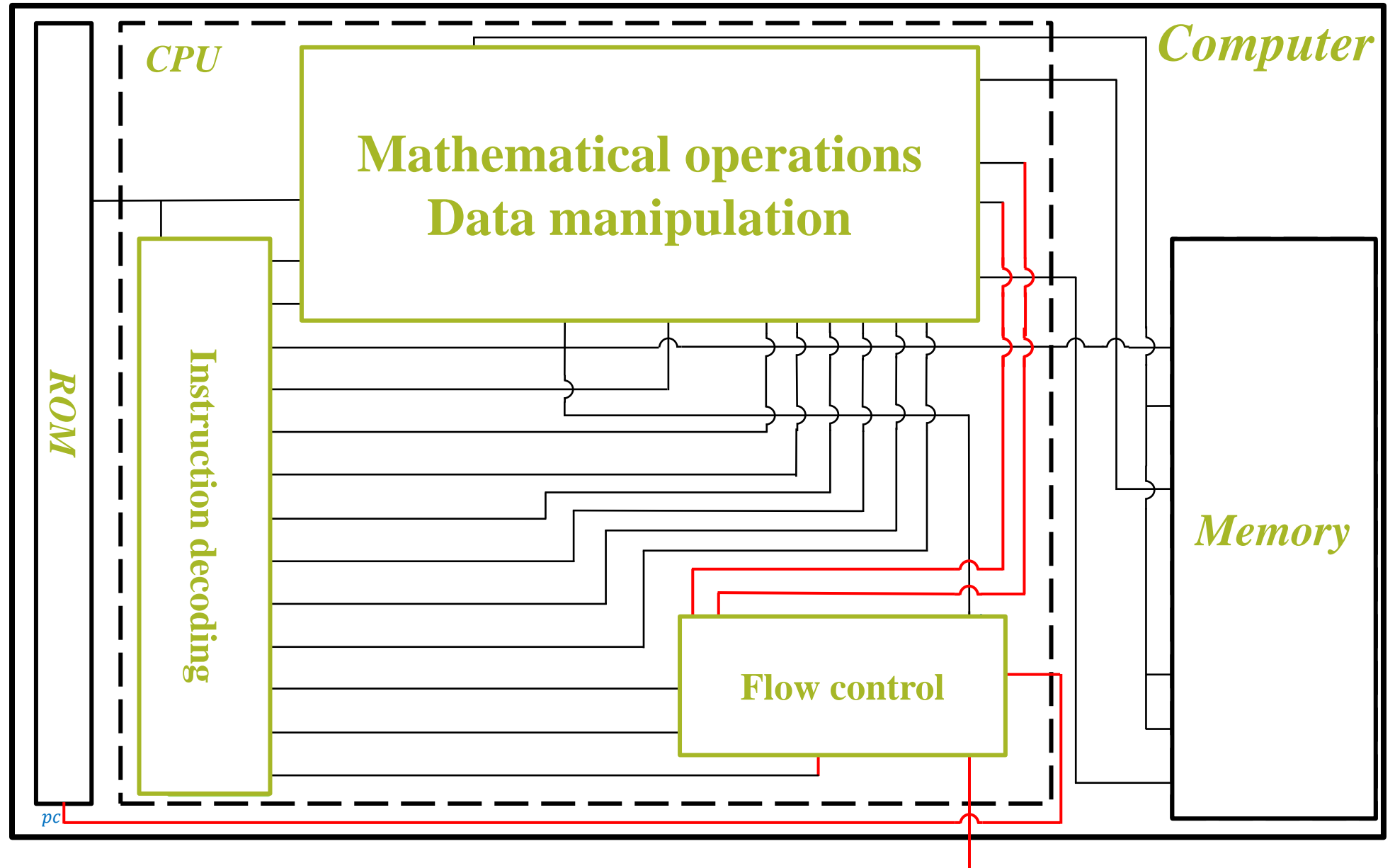


Flow control

Jump
conditions

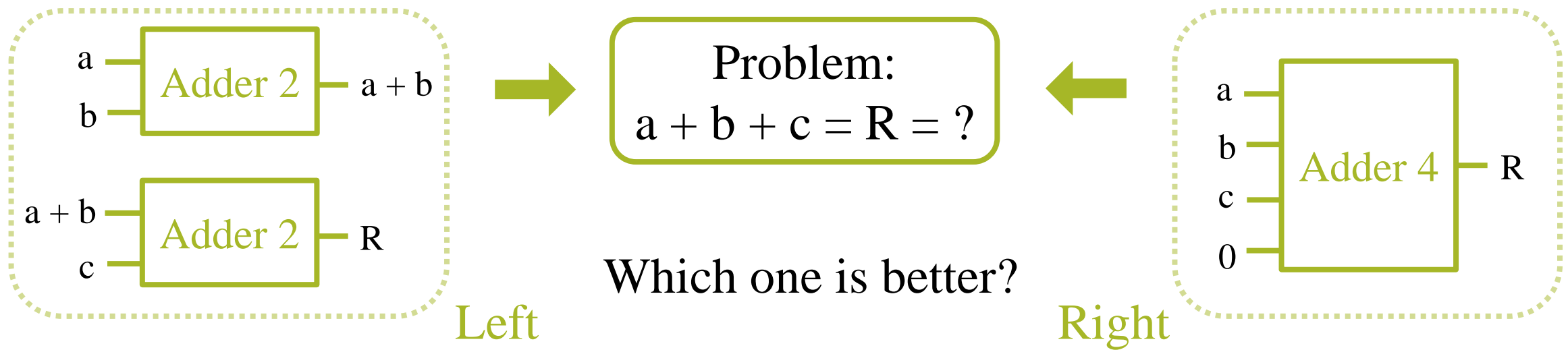
vs.

ALU output
flags



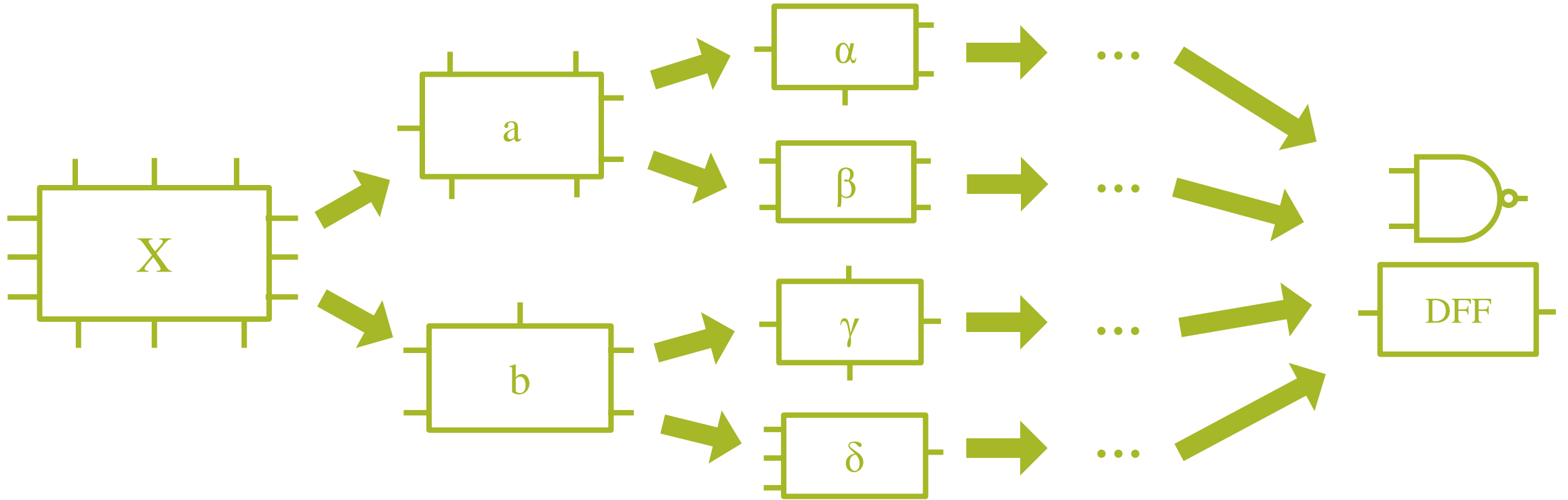
Improving the hardware design

- Fact: many ways of implementing the same functionality

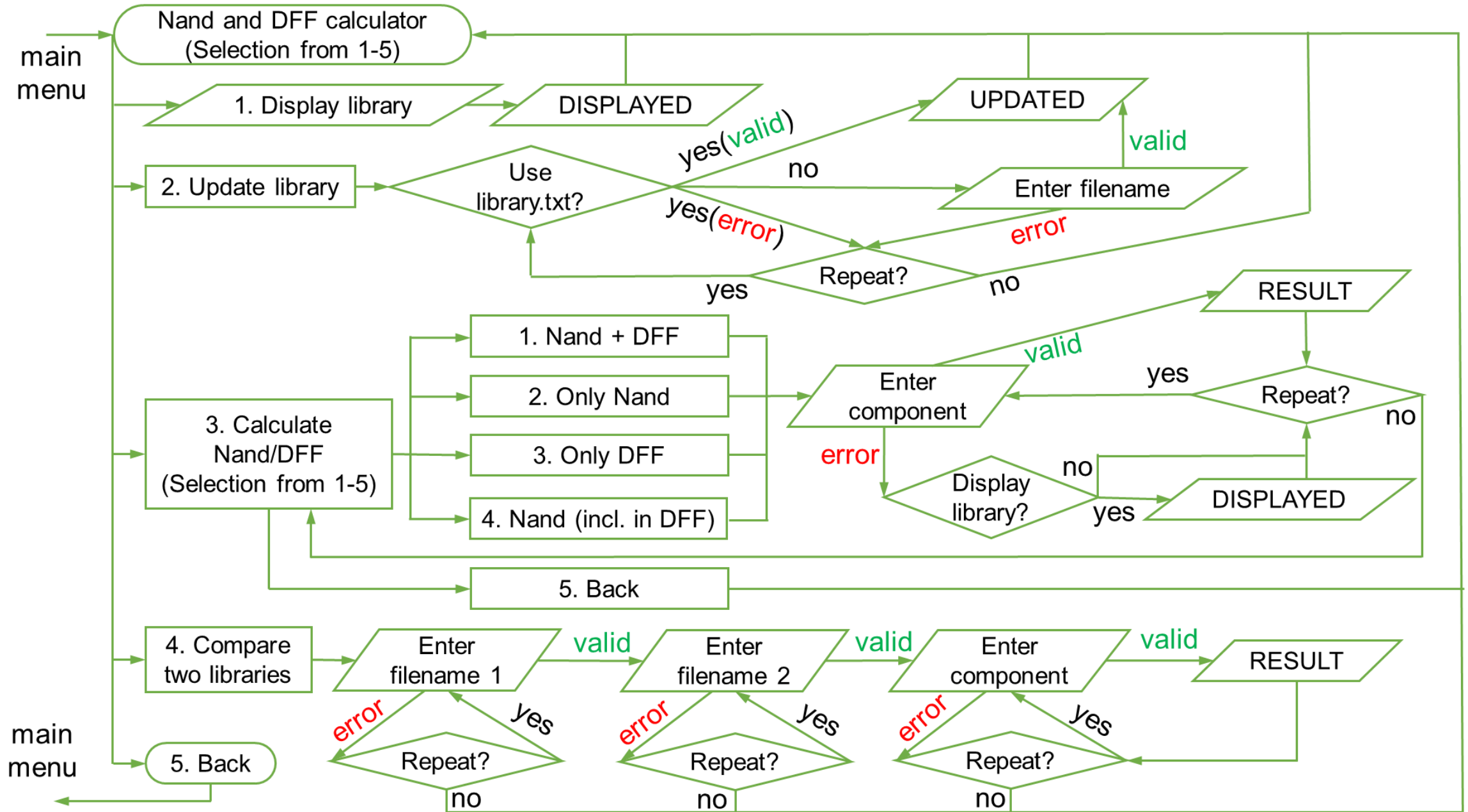


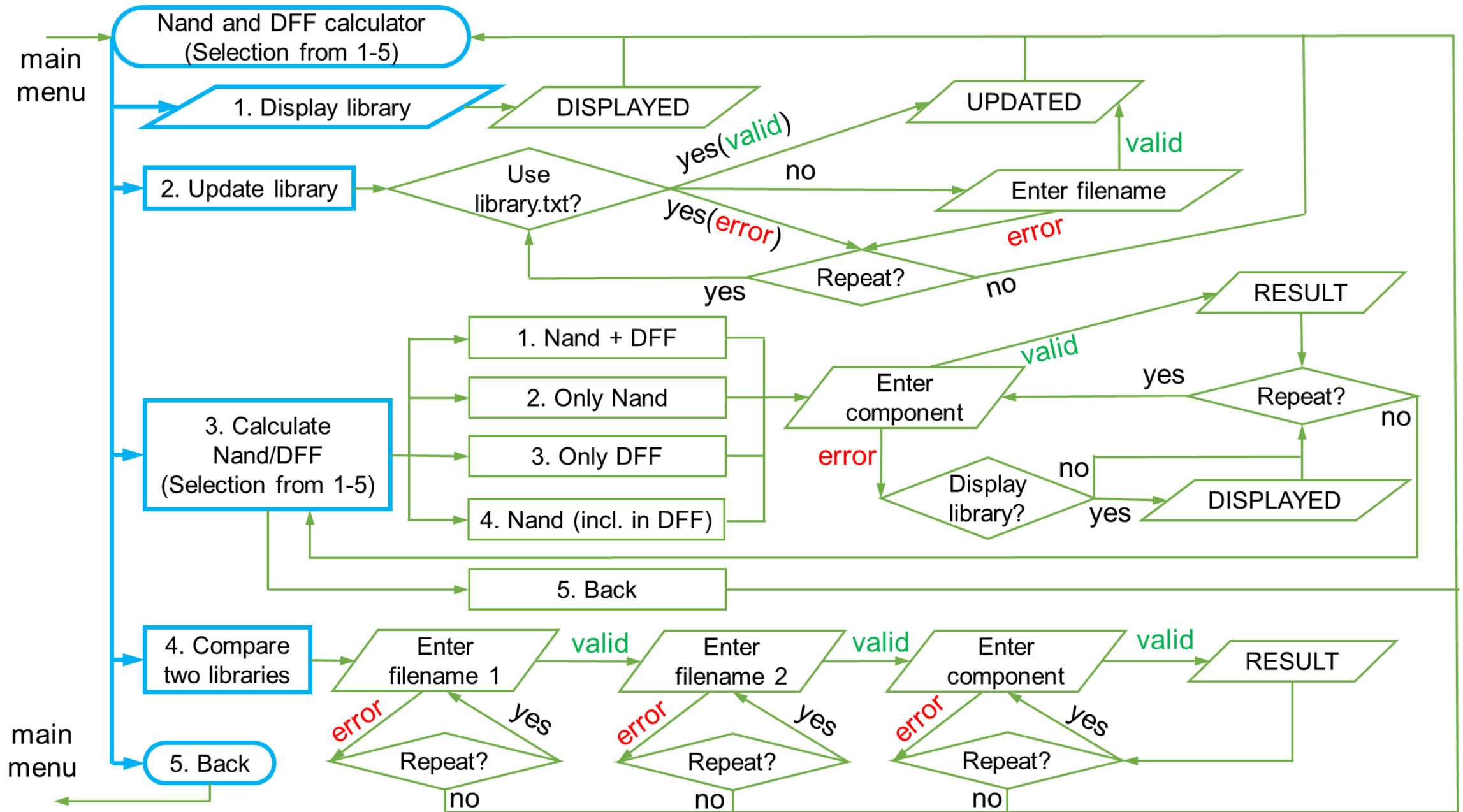
- Challenge: compare and find better ways

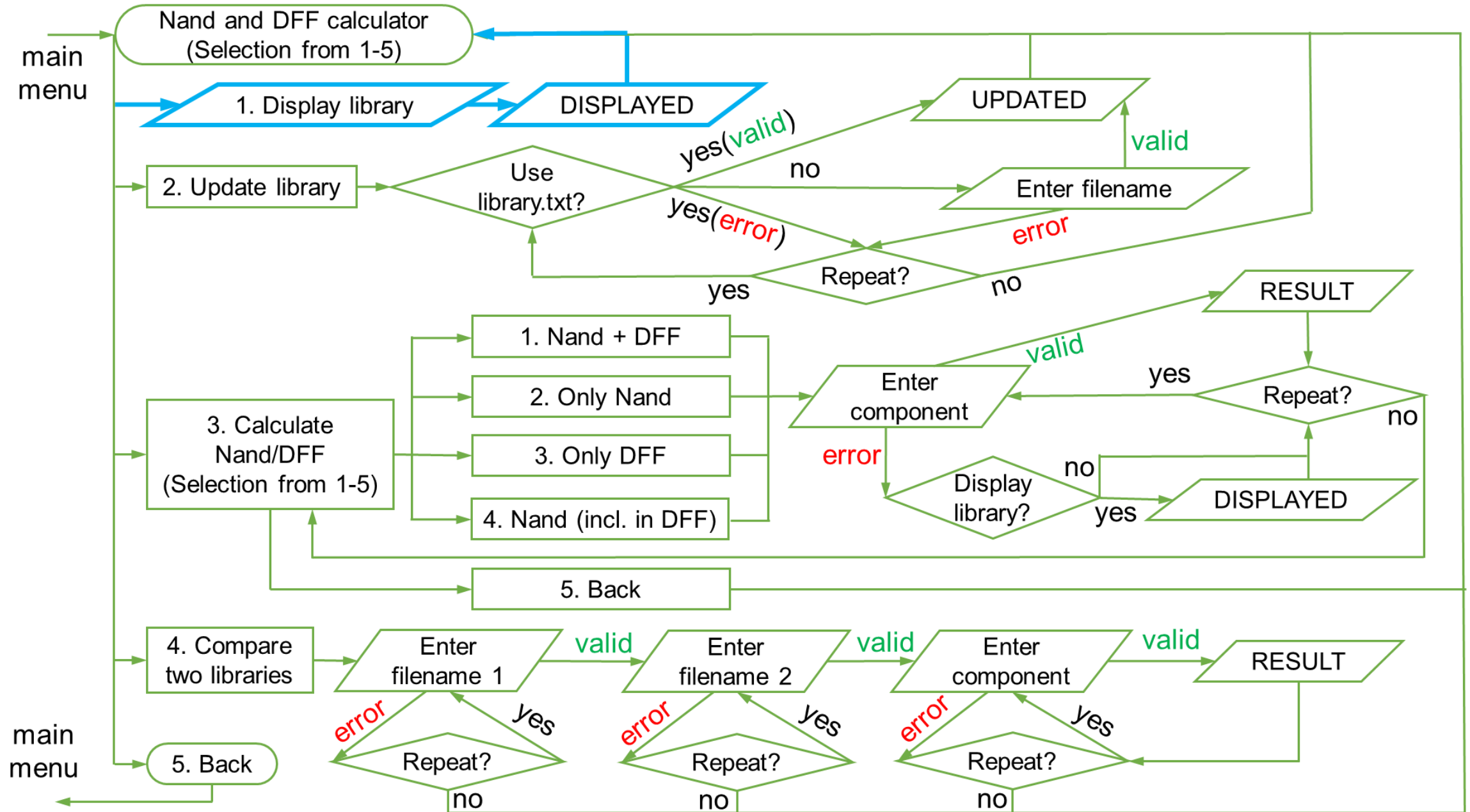
Nand & D Flip-flop calculator (transistor calculator in V2)

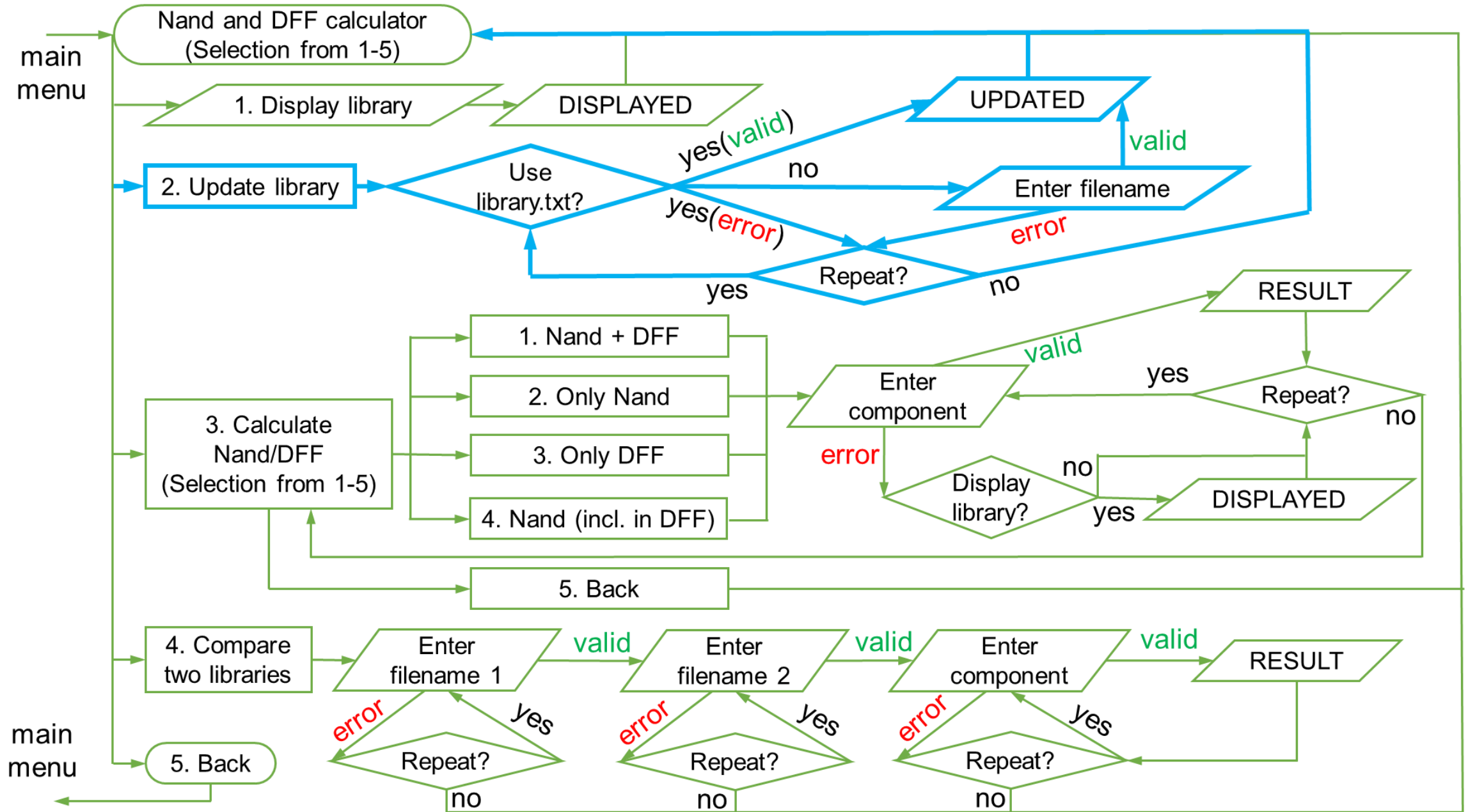


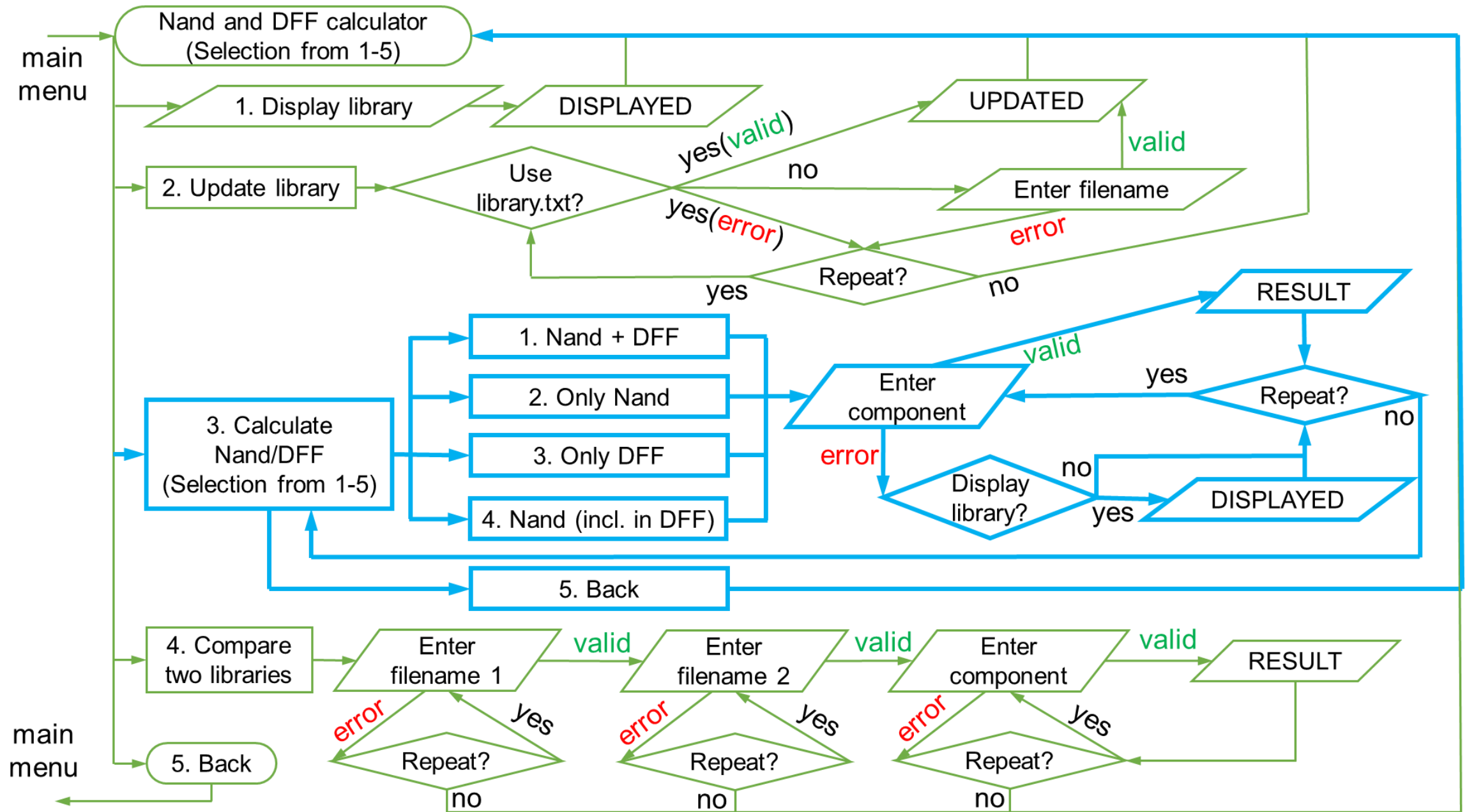
- Criteria: the number of Nands and DFFs (the number of transistors in V2)
- Program input: a text file with the structure of the desired component and subcomponents down to primitive components

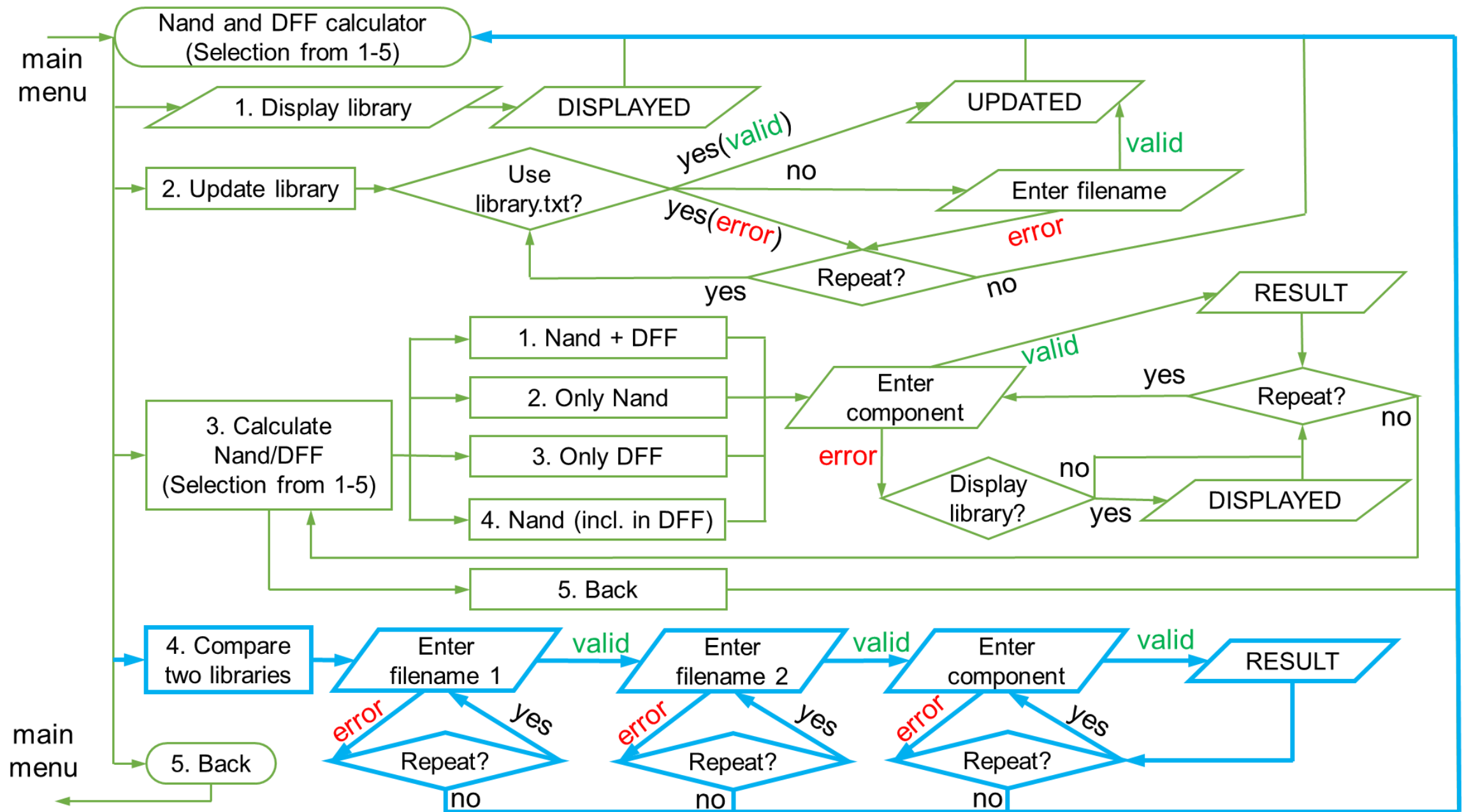




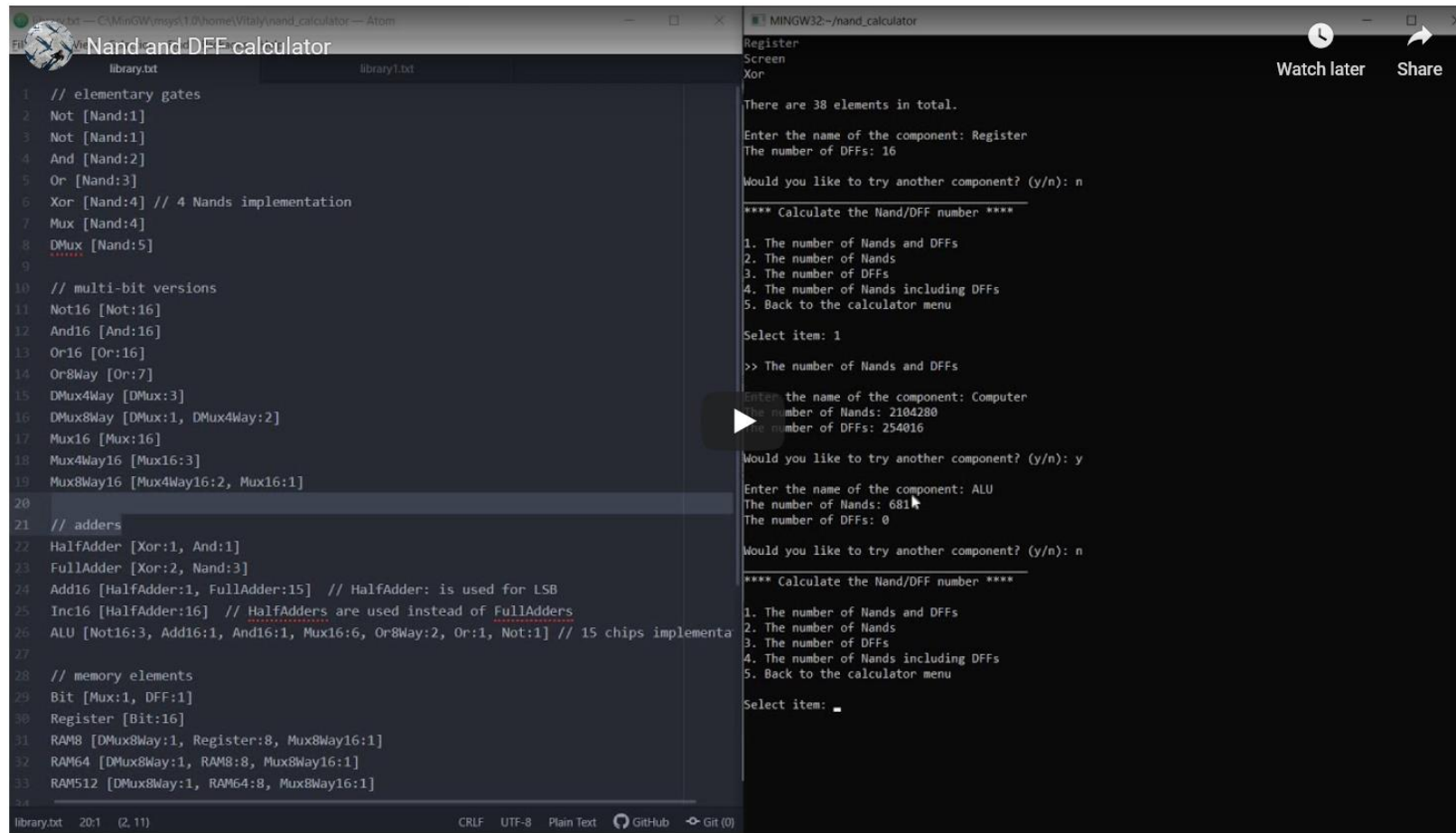








Demonstration



```
// elementary gates
1 Not [Nand:1]
2 Not [Nand:1]
3 And [Nand:2]
4 Or [Nand:3]
5 Xor [Nand:4] // 4 Nands implementation
6 Mux [Nand:4]
7 DMux [Nand:5]
8
9
10 // multi-bit versions
11 Not16 [Not:16]
12 And16 [And:16]
13 Or16 [Or:16]
14 Or8Way [Or:7]
15 DMux4Way [DMux:3]
16 DMux8Way [DMux:1, DMux4Way:2]
17 Mux16 [Mux:16]
18 Mux4Way16 [Mux16:3]
19 Mux8Way16 [Mux4Way16:2, Mux16:1]
20
21 // adders
22 HalfAdder [Xor:1, And:1]
23 FullAdder [Xor:2, Nand:3]
24 Add16 [HalfAdder:1, FullAdder:15] // HalfAdder: is used for LSB
25 Inc16 [HalfAdder:16] // HalfAdders are used instead of FullAdders
26 ALU [Not16:3, Add16:1, And16:1, Mux16:6, Or8Way:2, Or:1, Not:1] // 15 chips implementa
27
28 // memory elements
29 Bit [Mux:1, DFF:1]
30 Register [Bit:16]
31 RAM8 [DMux8Way:1, Register:8, Mux8Way16:1]
32 RAM64 [DMux8Way:1, RAM8:8, Mux8Way16:1]
33 RAM512 [DMux8Way:1, RAM64:8, Mux8Way16:1]
34
```

```
Register
Screen
Xor
Watch later Share

There are 38 elements in total.
Enter the name of the component: Register
The number of DFFs: 16
Would you like to try another component? (y/n): n

**** Calculate the Nand/DFF number ****

1. The number of Nands and DFFs
2. The number of Nands
3. The number of DFFs
4. The number of Nands including DFFs
5. Back to the calculator menu

Select item: 1

>> The number of Nands and DFFs
Enter the name of the component: Computer
The number of Nands: 2104280
The number of DFFs: 254016
Would you like to try another component? (y/n): y
Enter the name of the component: ALU
The number of Nands: 681
The number of DFFs: 0
Would you like to try another component? (y/n): n

**** Calculate the Nand/DFF number ****

1. The number of Nands and DFFs
2. The number of Nands
3. The number of DFFs
4. The number of Nands including DFFs
5. Back to the calculator menu

Select item: _
```



- Input file structure
- Output examples
- User guidance

https://youtu.be/_LZWHakxQ3Q