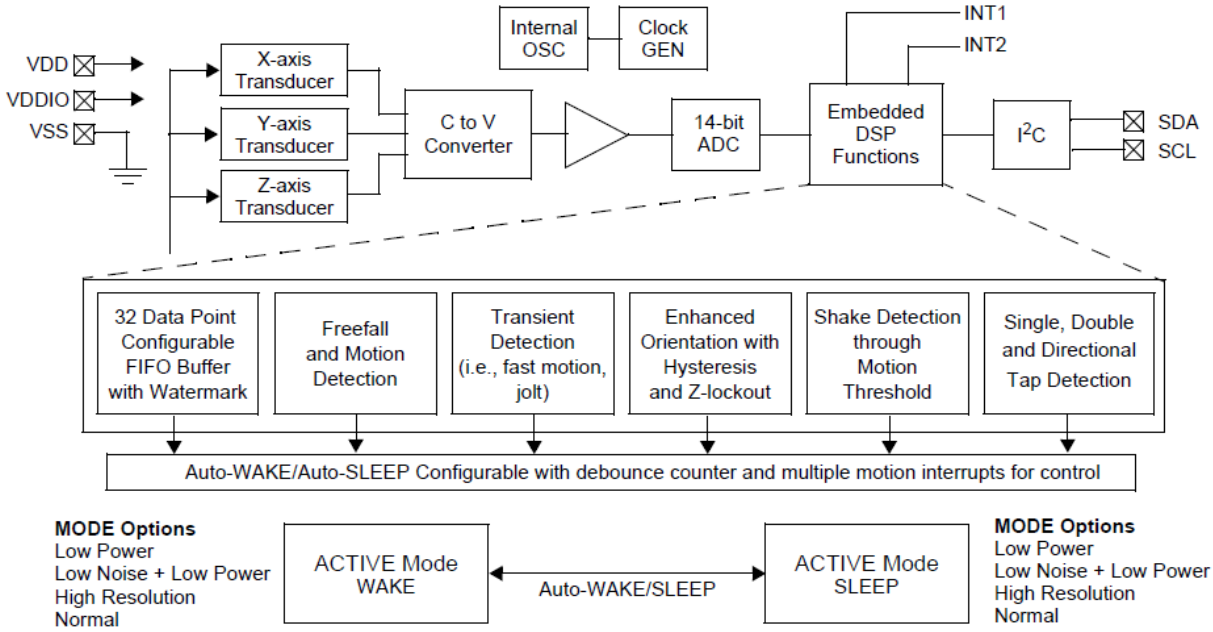
MMA8451Q 1.82

3-Axis, Digital Accelerometer

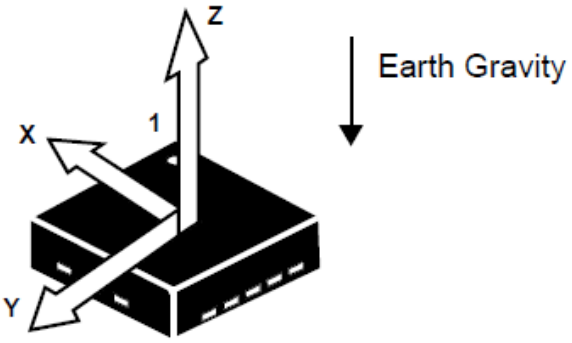
Description

- 1.95V to 3.6V
- Output Data Rates 1.56Hz to 800Hz
- I2C digital output interface
- Embedded Channels of motion detection
    - Frefall or motion detection
    - Pulse Detection
    - Jolt Detection
- High pass Filter
- 6uA to 165uA current consumption

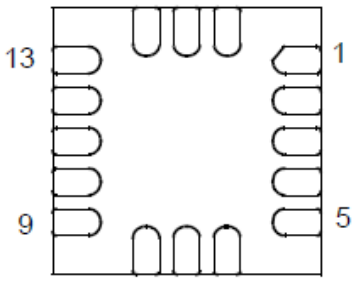
Block Diagram



Pin Connection



(TOP VIEW)
DIRECTION OF THE
DETECTABLE ACCELERATIONS



(BOTTOM VIEW)

Pin #	Pin Name	Description
1	VDDIO	Internal Power Supply (1.62V - 3.6V)
2	BYP	Bypass capacitor (0.1 µF)
3	DNC	Do not connect to anything, leave pin isolated and floating.
4	SCL	I^2C Serial Clock, open drain
5	GND	Connect to Ground
6	SDA	I^2C Serial Data
7	SA0	I^2C Least Significant Bit of the Device I^2C Address, I^2C 7-bit address = 0x1C (SA0=0), 0x1D (SA0=1).
8	NC	Internally not connected
9	INT2	Inertial Interrupt 2, output pin
10	GND	Connect to Ground
11	INT1	Inertial Interrupt 1, output pin
12	GND	Connect to Ground
13	NC	Internally not connected
14	VDD	Power Supply (1.95 V to 3.6 V)
15	NC	Internally not connected
16	NC	Internally not connected (can be GND or VDD)

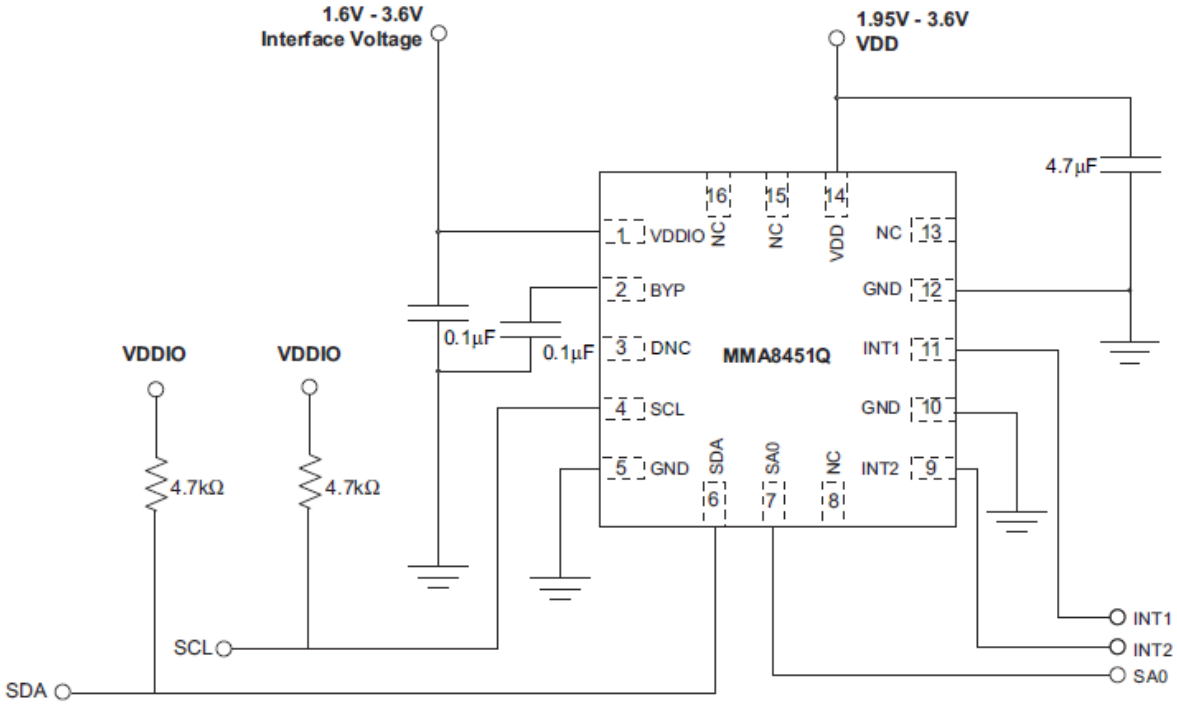
Mechanical Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Measurement Range[1]	FS[1:0] set to 00 2g Mode	FS		±2		g
	FS[1:0] set to 01 4g Mode			±4		
	FS[1:0] set to 10 8g Mode			±8		
Sensitivity	FS[1:0] set to 00 2g Mode	So		4096		counts/g
	FS[1:0] set to 01 4g Mode			2048		
	FS[1:0] set to 10 8g Mode			1024		
Sensitivity Accuracy[2]		Soa		±2.64		%
Sensitivity Change vs. Temperature	FS[1:0] set to 00 2g Mode	TCSo		±0.008		%/°C
	FS[1:0] set to 01 4g Mode					
	FS[1:0] set to 10 8g Mode					
Zero-g Level Offset Accuracy[3]	FS[1:0] 2g, 4g, 8g	TyOff		±17		mg
Zero-g Level Offset Accuracy Post Board Mount[4]	FS[1:0] 2g, 4g, 8g	TyOffPBM		±20		mg
Zero-g Level Change vs. Temperature	-40°C to 85°C	TCOff		±0.15		mg/°C
Self-Test Output Change[5] X Y Z	FS[1:0] set to 0 4g Mode	Vst		+181 +255 +1680		LSB
ODR Accuracy 2 MHz Clock				±2		%
Output Data Bandwidth		BW	ODR/3		ODR/2	Hz
Output Noise	Normal Mode ODR = 400 Hz	Noise		126		µg/√Hz
Output Noise Low Noise Mode[1]	Normal Mode ODR = 400 Hz	Noise		99		µg/√Hz
Operating Temperature Range		Top	-40		+85	°C

Electrical Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD(1)	1.95	2.5	3.6	V
Interface Supply Voltage		VDDIO(1)	1.62	1.8	3.6	V
Low Power Mode	ODR = 1.56 Hz	I_{dd}LP		6		µA
	ODR = 6.25 Hz			6		
	ODR = 12.5 Hz			6		
	ODR = 50 Hz			14		
	ODR = 100 Hz			24		
	ODR = 200 Hz			44		
	ODR = 400 Hz			85		
	ODR = 800 Hz			165		
Normal Mode	ODR = 1.56 Hz	I_{dd}		24		µA
	ODR = 6.25 Hz			24		
	ODR = 12.5 Hz			24		
	ODR = 50 Hz			24		
	ODR = 100 Hz			44		
	ODR = 200 Hz			85		
	ODR = 400 Hz			165		
	ODR = 800 Hz			165		
Current during Boot Sequence, 0.5 mSec max duration using recommended Bypass Cap	VDD = 2.5V	Idd Boot			1	mA
Value of Capacitor on BYP Pin	-40°C 85°C	Cap	75	100	470	nF
STANDBY Mode Current @25°C	VDD = 2.5V, VDDIO = 1.8V STANDBY Mode	I_{dd}Stby		1.8	5	µA
Digital High Level Input Voltage SCL, SDA, SA0		VIH	0.75*VDDIO			V
Digital Low Level Input Voltage SCL, SDA, SA0		VIL			0.3*VDDIO	V
High Level Output Voltage INT1, INT2	I_O = 500 µA	VOH	0.9*VDDIO			V
Low Level Output Voltage INT1, INT2	I_O = 500 µA	VOL			0.1*VDDIO	V
Low Level Output Voltage SDA	I_O = 500 µA	VOLS			0.1*VDDIO	V
Power on Ramp Time			0.001		1000	ms
Boot time	Time from VDDIO on and VDD > VDD min until I^2C is ready for operation, Cbyp = 100 nF	Tbt		350	500	µs
Turn-on time	Time to obtain valid data from STANDBY mode to ACTIVE mode.	Ton1		2/ODR + 1 ms		
Turn-on time	Time to obtain valid data from valid voltage applied.	Ton2		2/ODR + 2 ms		
Operating Temperature Range		Top	-40		+85	°C

Schematic


1.6V - 3.6V
Interface Voltage
1.95V - 3.6V
VDD
4.7µF
16
15
14
1 VDDIO
NC
NC
VDD
NC 13
2 BYP
GND 12
0.1µF
0.1µF
3 DNC
MMA8451Q
INT1 11
4 SCL
GND 10
5 GND
SDA
SA0
NC
INT2 9
6
7
8
VDDIO
VDDIO
4.7kΩ
4.7kΩ
INT1
INT2
SA0
SCL
SDA

Interrupt

INT_SOURCE System Interrupt Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT	—	SRC_DRDY

INT_SOURCE	Description
SRC_ASLP	Auto-SLEEP/WAKE interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt event that can cause a WAKE to SLEEP or SLEEP to WAKE system mode transition has occurred. Logic '0' indicates that no WAKE to SLEEP or SLEEP to WAKE system mode transition interrupt event has occurred. **WAKE to SLEEP** transition occurs when no interrupt occurs for a time period that exceeds the user specified limit (ASLP_COUNT). This causes the system to transition to a user specified low ODR setting. **SLEEP to WAKE** transition occurs when the user specified interrupt event has woken the system; thus causing the system to transition to a user specified high ODR setting. Reading the SYSMOD register clears the SRC_ASLP bit.
SRC_FIFO	FIFO interrupt status bit. Default value: 0. Logic '1' indicates that a FIFO interrupt event such as an overflow event or watermark has occurred. Logic '0' indicates that no FIFO interrupt event has occurred. FIFO interrupt event generators: FIFO Overflow, or (Watermark: F_CNT = F_WMRK) and the interrupt has been enabled. This bit is cleared by reading the F_STATUS register.
SRC_TRANS	Transient interrupt status bit. Default value: 0. Logic '1' indicates that an acceleration transient value greater than user specified threshold has occurred. Logic '0' indicates that no transient event has occurred. This bit is asserted whenever "EA" bit in the TRANS_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the TRANS_SRC register.
SRC_LNDPRT	Landscape/Portrait Orientation interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt was generated due to a change in the device orientation status. Logic '0' indicates that no change in orientation status was detected. This bit is asserted whenever "NEWLP" bit in the PL_STATUS is asserted and the interrupt has been enabled. This bit is cleared by reading the PL_STATUS register.
SRC_PULSE	Pulse interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt was generated due to single and/or double pulse event. Logic '0' indicates that no pulse event was detected. This bit is asserted whenever "EA" bit in the PULSE_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the PULSE_SRC register.
SRC_FF_MT	Freefall/Motion interrupt status bit. Default value: 0. Logic '1' indicates that the Freefall/Motion function interrupt is active. Logic '0' indicates that no Freefall or Motion event was detected. This bit is asserted whenever "EA" bit in the FF_MT_SRC register is asserted and the FF_MT interrupt has been enabled. This bit is cleared by reading the FF_MT_SRC register.
SRC_DRDY	Data Ready Interrupt bit status. Default value: 0. Logic '1' indicates that the X, Y, Z data ready interrupt is active indicating the presence of new data and/or data overrun. Otherwise if it is a logic '0' the X, Y, Z interrupt is not active. This bit is asserted when the ZYXOW and/or ZYXDR is set and the interrupt has been enabled. This bit is cleared by reading the X, Y, and Z data.

Transient (HPF) Acceleration Detection

The transient detection mechanism can be configured to raise an interrupt when the magnitude of the high-pass filtered acceleration threshold is exceeded. The TRANSIENT_CFG register is used to enable the transient interrupt generation mechanism for the three axes (X, Y, Z) of acceleration. There is also an option to bypass the high-pass filter. When the high-pass filter is bypassed, the function behaves similar to the motion detection.

Transient_CFG Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	ELE	ZTEFE	YTEFE	XTEFE	HPF_BYP

ELE	Transient event flags are latched into the TRANSIENT_SRC register. Reading of the TRANSIENT_SRC register clears the event flag. Default value: 0. 0: Event flag latch disabled; 1: Event flag latch enabled
ZTEFE	Event flag enable on Z transient acceleration greater than transient threshold event. Default value: 0. 0: Event detection disabled; 1: Raise event flag on measured acceleration delta value greater than transient threshold.
YTEFE	Event flag enable on Y transient acceleration greater than transient threshold event. Default value: 0. 0: Event detection disabled; 1: Raise event flag on measured acceleration delta value greater than transient threshold.
XTEFE	Event flag enable on X transient acceleration greater than transient threshold event. Default value: 0. 0: Event detection disabled; 1: Raise event flag on measured acceleration delta value greater than transient threshold.
HPF_BYP	Bypass High-Pass filter Default value: 0. 0: Data to transient acceleration detection block is through HPF 1: Data to transient acceleration detection block is NOT through HPF (similar to motion detection function)

TRANSIENT_SRC Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	EA	ZTRANSE	Z_Trans_Pol	YTRANSE	Y_Trans_Pol	XTRANSE	X_Trans_Pol

EA	Event Active Flag. Default value: 0. 0: no event flag has been asserted; 1: one or more event flag has been asserted.
ZTRANSE	Z transient event. Default value: 0. 0: no interrupt, 1: Z Transient acceleration greater than the value of TRANSIENT_THS event has occurred
Z_Trans_Pol	Polarity of Z Transient Event that triggered interrupt. Default value: 0. 0: Z event was Positive g, 1: Z event was Negative g
YTRANSE	Y transient event. Default value: 0. 0: no interrupt, 1: Y Transient acceleration greater than the value of TRANSIENT_THS event has occurred
Y_Trans_Pol	Polarity of Y Transient Event that triggered interrupt. Default value: 0. 0: Y event was Positive g, 1: Y event was Negative g
XTRANSE	X transient event. Default value: 0. 0: no interrupt, 1: X Transient acceleration greater than the value of TRANSIENT_THS event has occurred
X_Trans_Pol	Polarity of X Transient Event that triggered interrupt. Default value: 0. 0: X event was Positive g, 1: X event was Negative g

TRANSIENT_THS Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0

DBCNTM	Debounce counter mode selection. Default value: 0. 0: increments or decrements debounce; 1: increments or clears counter.
THS[6:0]	Transient Threshold: Default value: 000_0000.

The threshold THS[6:0] is a 7-bit unsigned number, 0.063g/LSB. The maximum threshold is 8g. Even if the part is set to full scale at 2g or 4g this function will still operate up to 8g. If the Low Noise bit is set in Register 0x2A, the maximum threshold to be reached is 4g.

Single, Double and Directional Tap Detection Registers

PULSE_CFG Pulse Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPA	ELE	ZDPEFE	ZSPEFE	YDPEFE	YSPEFE	XDPEFE	XSPEFE

DPA	Double Pulse Abort. Default value: 0. 0: Double Pulse detection is not aborted if the start of a pulse is detected during the time period specified by the PULSE_LTCY register. 1: Setting the DPA bit momentarily suspends the double tap detection if the start of a pulse is detected during the time period specified by the PULSE_LTCY register and the pulse ends before the end of the time period specified by the PULSE_LTCY register.
ELE	Pulse event flags are latched into the PULSE_SRC register. Reading of the PULSE_SRC register clears the event flag. Default value: 0. 0: Event flag latch disabled; 1: Event flag latch enabled
ZDPEFE	Event flag enable on double pulse event on Z-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
ZSPEFE	Event flag enable on single pulse event on Z-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
YDPEFE	Event flag enable on double pulse event on Y-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
YSPEFE	Event flag enable on single pulse event on Y-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
XDPEFE	Event flag enable on double pulse event on X-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled
XSPEFE	Event flag enable on single pulse event on X-axis. Default value: 0. 0: Event detection disabled; 1: Event detection enabled

PULSE_SRC Pulse Source Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EA	AxZ	AxY	AxX	DPE	PolZ	PolY	PolX

EA	Event Active Flag. Default value: 0. (0: No interrupt has been generated; 1: One or more interrupt events have been generated)
AxZ	Z-axis event. Default value: 0. (0: No interrupt; 1: Z-axis event has occurred)
AxY	Y-axis event. Default value: 0. (0: No interrupt; 1: Y-axis event has occurred)
AxX	X-axis event. Default value: 0. (0: No interrupt; 1: X-axis event has occurred)
DPE	Double pulse on first event. Default value: 0. (0: Single Pulse Event triggered interrupt; 1: Double Pulse Event triggered interrupt)
PolZ	Pulse polarity of Z-axis Event. Default value: 0. (0: Pulse Event that triggered interrupt was Positive; 1: Pulse Event that triggered interrupt was negative)
PolY	Pulse polarity of Y-axis Event. Default value: 0. (0: Pulse Event that triggered interrupt was Positive; 1: Pulse Event that triggered interrupt was negative)
PolX	Pulse polarity of X-axis Event. Default value: 0. (0: Pulse Event that triggered interrupt was Positive; 1: Pulse Event that triggered interrupt was negative)

PULSE_THSX, Y, Z Pulse Threshold for X, Y & Z Registers

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

THSX[6:0]	Pulse Threshold on X-axis. Default value: 000_0000.

The threshold values range from 1 to 127 with steps of 0.063g/LSB at a fixed 8g acceleration range, thus the minimum resolution is always fixed at 0.063g/LSB. If the Low Noise bit in Register 0x2A is set then the maximum threshold will be 4g. The PULSE_THSX, PULSE_THSY and PULSE_THSZ registers define the threshold which is used by the system to start the pulse detection procedure. The threshold value is expressed over 7-bits as an unsigned number.

PULSE_TMLT Pulse Time Window 1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMLT7	TMLT6	TMLT5	TMLT4	TMLT3	TMLT2	TMLT1	TMLT0

The bits TMLT7 through TMLT0 define the maximum time interval that can elapse between the start of the acceleration on the selected axis exceeding the specified threshold and the end when the acceleration on the selected axis must go below the specified threshold to be considered a valid pulse.

Min times:

ODR (Hz)	Max Time Range (s)				Time Step (ms)			
	Normal	LPLN	HighRes	LP	Normal	LPLN	HighRes	LP
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	20.4	0.638	40.8	20	80	2.5	160
1.56	5.1	20.4	0.638	40.8	20	80	2.5	160