CLRC663 8.41

High Performance NFC reader solution

Description

- Read/write mode supporting ISO/IEC 14443A/MIFARE
- Read/write mode supporting ISO/IEC 14443B
- Read/write mode supporting ISO/IEC 18000-3 mode 3/ EPC Class-1 HF
- Serial Peripheral Interface (SPI)
- 3V to 5V power Supply
- Up to 8 free programmable input/output pins

Power

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	5	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	[1]	3	5	V_{DD}	V
$V_{DD(TVDD)}$	TVDD supply voltage		3	5	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH [2]	-	8	40	nA
I_{DD}	supply current		-	17	20	mA
$I_{DD(TVDD)}$	TVDD supply current	[3][4]	-	100	200	mA
T_{amb}	ambient temperature		–25	+25	+85	°C
T_{stg}	storage temperature	no supply voltage applied	–40	+25	+100	°C

Block Diagram

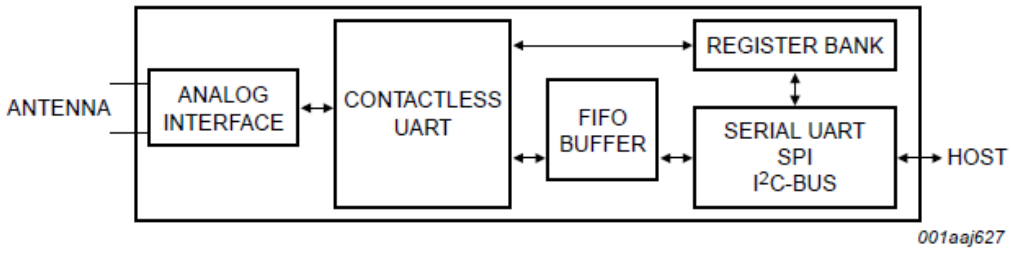
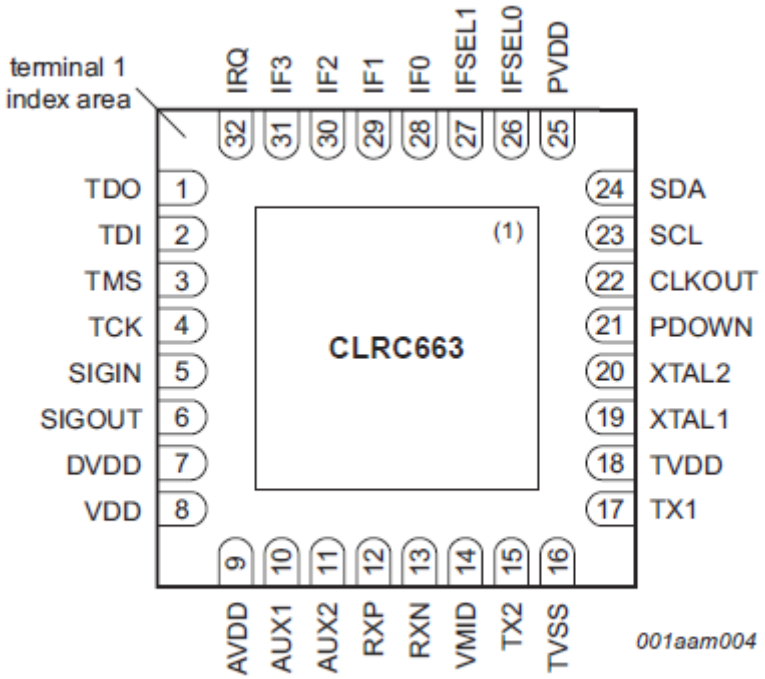


Fig 1. Simplified block diagram of the CLRC663

Pin Layout



Transparent top view

Interrupt Controller

- Two 8-bit interrupt registers IRQ0 and IRQ1 are implemented
    - Accompanied by two 8-bit interrupt enable registers IRQ0En and IRQ1En

Interrupt bit	Interrupt source	Is set automatically, when
Timer0Irq	Timer Unit	the timer register T0 CounterVal underflows
Timer1Irq	Timer Unit	the timer register T1 CounterVal underflows
Timer2Irq	Timer Unit	the timer register T2 CounterVal underflows
Timer3Irq	Timer Unit	the timer register T3 CounterVal underflows
TxIrq	Transmitter	a transmitted data stream ends
RxIrq	Receiver	a received data stream ends
IdleIrq	Command Register	a command execution finishes
HiAlertIrq	FIFO-buffer pointer	the FIFO data number has reached the top level as configured by the bit WaterLevel
LoAlertIrq	FIFO-buffer pointer	the FIFO data number has reached the bottom level as configured by the bit WaterLevel
ErrIrq	contactless UART	a communication error had been detected
LPCDIrq	LPCD	a card was detected when in low-power card detection mode
RxSOFIrq	Receiver	detection of a SOF or a subcarrier
GlobalIrq	all interrupt sources	will be set if another interrupt request source is set

Timers

Periodical trigger

If the bit T(x)Control. T(x)AutoRestart is set and the interrupt is activated, an interrupt request will be indicated periodically after every elapsed timer period.

Communication

Read Data

	byte 0	byte 1	byte 2	byte 3 to n-1	byte n	byte n+1
MOSI	address 0	address 1	address 2	……..	address n	00h
MISO	X	data 0	data 1	……..	data n – 1	data n

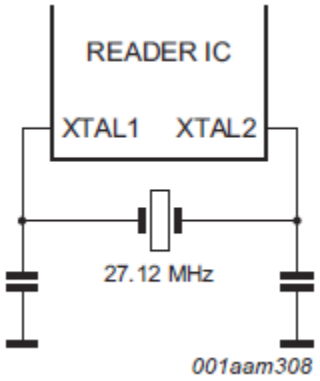
Write Data

	byte 0	byte 1	byte 2	3 to n-1	byte n	byte n + 1
MOSI	address 0	data 0	data 1	……..	data n – 1	data n
MISO	X	X	X	……..	X	X

Address Byte

7	6	5	4	3	2	1	0
address 6	address 5	address 4	address 3	address 2	address 1	address 0	1 (read) 0 (write)
MSB							LSB

Clock Generation



Crystal Requirements Recommendations

Symbol	Parameter	Conditions	Min	Typ	max	Unit
f_{xtal}	crystal frequency		-	27.12	-	MHz
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation		–250	-	+250	ppm
ESR	equivalent series resistance		-	50	100	Ω
C_L	load capacitance		-	10	-	pF
P_{xtal}	crystal power dissipation		-	50	100	µW

Interrupts

IRQ0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	Set	Hi AlertIrq	Lo AlertIrq	IdleIrq	TxIrq	RxIrq	ErrIrq	RxSOF Irq
Access rights	w	dy	dy	dy	dy	dy	dy	dy

Bit	Symbol	Description
7	Set	1: writing a 1 to a bit position 6..0 sets the interrupt request 0: Writing a 1 to a bit position 6..0 clears the interrupt request
6	HiAlerIrq	Set, when bit HiAlert in register Status1Reg is set. In opposition to HiAlert, HiAlertIrq stores this event and can only be reset if Set is cleared.
5	LoAlertIrq	Set, when bit LoAlert in register Status1 is set. In opposition to LoAlert, LoAlertIrq stores this event and can only be reset if Set is cleared
4	IdleIrq	Set, when a command terminates by itself e.g. when the Command changes its value from any command to the Idle command. If an unknown command is started, the Command changes its content to the idle state and the bit IdleIRq is set. Starting the Idle command by the Controller does not set bit IdleIRq. Can only be reset if Set is cleared.
3	TxIrq	Set, when data transmission is completed, which is immediately after the last bit is sent. Can only be reset if Set is cleared.
2	RxIrq	Set, when the receiver detects the end of a data stream. Note: This flag is no indication that the received data stream is correct. The error flags have to be evaluated to get the status of the reception. Can only be reset if Set is cleared.
1	ErrIrq	Set, when the one of the following errors is set: FifoWrErr, FiFoOvl, ProtErr, NoDataErr, IntegErr. Can only be reset if Set is cleared.
0	RxSOFIrq	Set, when a SOF or a subcarrier is detected. Can only be reset if Set is cleared.

IRQ1

Bit	7	6	5	4	3	2	1	0
Symbol	Set	GlobalIrq	LPCD_Irq	Timer4Irq	Timer3Irq	Timer2Irq	Timer1Irq	Timer0Irq
Access rights	w	dy	dy	dy	dy	dy	dy	dy

Bit	Symbol	Description
7	Set	1: writing a 1 to a bit position 5..0 sets the interrupt request 0: Writing a 1 to a bit position 5..0 clears the interrupt request
6	GlobalIrq	Set, if an enabled Irq occurs.
5	LPCD_Irq	Set if a card is detected in Low-power card detection sequence.
4	Timer4Irq	Set to logic 1 when Timer4 has an underflow.
3	Timer3Irq	Set to logic 1 when Timer3 has an underflow.
2	Timer2Irq	Set to logic 1 when Timer2 has an underflow.
1	Timer1Irq	Set to logic 1 when Timer1 has an underflow.
0	Timer0Irq	Set to logic 1 when Timer0 has an underflow.

IRQ0EN

Bit	7	6	5	4	3	2	1	0
Symbol	Irq_Inv	Hi AlertIrqEn	LoAlertIrqEn	IdleIrqEn	TxIrqEn	RxIrqEn	ErrIrqEn	RxSOFIrqEn
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Bit	Symbol	Description
7	Irq_Inv	Set to one the signal of the IRQ pin is inverted
6	Hi AlerIrqEn	Set to logic 1, it allows the High Alert interrupt Request (indicated by the bit HiAlertIrq) to be propagated to the GlobalIrq
5	Lo AlertIrqEn	Set to logic 1, it allows the Low Alert Interrupt Request (indicated by the bit LoAlertIrq) to be propagated to the GlobalIrq
4	IdleIrqEn	Set to logic 1, it allows the Idle interrupt request (indicated by the bit IdleIrq) to be propagated to the GlobalIrq
3	TxIRqEn	Set to logic 1, it allows the transmitter interrupt request (indicated by the bit TxtIrq) to be propagated to the GlobalIrq
2	RxIRqEn	Set to logic 1, it allows the receiver interrupt request (indicated by the bit RxIrq) to be propagated to the GlobalIrq
1	ErrIRqEn	Set to logic 1, it allows the Error interrupt request (indicated by the bit ErrorIrq) to be propagated to the GlobalIrq
0	RxSOFIrqEn	Set to logic 1, it allows the RxSOF interrupt request (indicated by the bit RxSOFIrq) to be propagated to the GlobalIrq

IRQ1EN

Bit	7	6	5	4	3	2	1	0
Symbol	IrqPushPull	IrqPinEn	LPCD_IrqEn	Timer4IrqEn	Timer3IrqEn	Timer2IrqEn	Timer1IrqEn	Timer0IrqEn
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Bit	Symbol	Description
7	IrqPushPull	Set to 1 the IRQ-pin acts as PushPull pin, otherwise it acts as OpenDrain pin
6	IrqPinEN	Set to logic 1, it allows the global interrupt request (indicated by the bit GlobalIrq) to be propagated to the interrupt pin
5	LPCD_IrqEN	Set to logic 1, it allows the LPCDinterrupt request (indicated by the bit LPCDIrq) to be propagated to the GlobalIrq
4	Timer4IRqEn	Set to logic 1, it allows the Timer4 interrupt request (indicated by the bit Timer4Irq) to be propagated to the GlobalIrq
3	Timer3IrqEn	Set to logic 1, it allows the Timer3 interrupt request (indicated by the bit Timer3tIrq) to be propagated to the GlobalIrq
2	Timer2IrqEn	Set to logic 1, it allows the Timer2 interrupt request (indicated by the bit Timer2Irq) to be propagated to the GlobalIrq
1	Timer1IrqEn	Set to logic 1, it allows the Timer1 interrupt request (indicated by the bit Timer1Irq) to be propagated to the GlobalIrq
0	Timer0IrqEn	Set to logic 1, it allows the Timer0 interrupt request (indicated by the bit Timer0Irq) to be propagated to the GlobalIrq

Timer Registers

TOControl

Bit	7	6	5	4	3	2	1	0
Symbol	T0StopRx	-	T0Start		T0AutoRestart	-	T0Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Bit	Symbol	Description
7	T0StopRx	If set, the timer stops immediately after receiving the first 4 bits. If cleared the timer does not stop automatically. Note: If LFO Trimming is selected by T0Start, this bit has no effect.
6	-	RFU
5 to 4	T0Start	00b: The timer is not started automatically 01b: The timer starts automatically at the end of the transmission 10b: Timer is used for LFO trimming without underflow (Start/Stop on PosEdge) 11b: Timer is used for LFO trimming with underflow (Start/Stop on PosEdge)
3	T0AutoRestart	1: the timer automatically restarts its count-down from T0ReloadValue, after the counter value has reached the value zero. 0: the timer decrements to zero and stops. The bit Timer1Irq is set to logic 1 when the timer underflows.
2	-	RFU
1 to 0	T0Clk	00b: The timer input clock is 13.56 MHz. 01b: The timer input clock is 211,875 kHz. 10b: The timer input clock is an underflow of Timer2. 11b: The timer input clock is an underflow of Timer1.

TOReloadHi

Bit	7	6	5	4	3	2	1	0
Symbol	T0Reload Hi							
Access rights	r/w							

Bit	Symbol	Description
7 to 0	T0ReloadHi	Defines the high byte of the reload value of the timer. With the start event the timer loads the value of the registers T0ReloadValHi, T0ReloadValLo. Changing this register affects the timer only at the next start event.

TOReloadLo

Bit	7	6	5	4	3	2	1	0
Symbol	T0ReloadLo							
Access rights	r/w							

Bit	Symbol	Description
7 to0	T0ReloadLo	Defines the low byte of the reload value of the timer. With the start event the timer loads the value of the T0ReloadValHi, T0ReloadValLo. Changing this register affects the timer only at the next start event.