IEEE P802.3bm™/D3.0

Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation Over Fiber Optic Cables

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2012. This amendment adds Physical Layer (PHY) specifications and management parameters for 40 Gb/s operation over single-mode fiber (40GBASE-ER4) and for 100 Gb/s operation over multimode fiber (100GBASE-SR4). This amendment also specifies a four-lane variant of the 100 Gigabit Attachment Unit Interface (CAUI-4) and optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over fiber optic cables. Draft D3.0 is prepared for initial Sponsor ballot. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2012 adds Physical Layer (PHY) specifications and management parameters for 40 Gb/s operation over single-mode fiber (40GBASE-ER4) and for 100 Gb/s operation over multimode fiber (100GBASE-SR4). This amendment also specifies a four-lane variant of the 100 Gigabit Attachment Unit Interface (CAUI-4) and optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over fiber optic cables.

Keywords: 100 Gb/s Ethernet; 100GBASE-ER4; 100GBASE-LR4; 100GBASE-SR10; 100GBASE-SR4; 40 Gb/s Ethernet; 40GBASE-ER4; 40GBASE-FR; 40GBASE-LR4; 40GBASE-SR4; CAUI-4; Energy Efficient Ethernet (EEE); Ethernet; forward error correction (FEC); IEEE Std 802.3bm; MMF; physical medium dependent (PMD) sublayer; SMF.

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3 Park Avenue, New York, NY 10016-5997, USA

PDF: ISBN 978-0-7381-xxxx-x STDxxxxx
Print: ISBN 978-0-7381-xxxx-x STDPDxxxxx

Introduction

Editor's Note (to be removed prior to publication):

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

One exception to IEEE style that is consciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecutively with arabic page numbers.

This introduction is not part of IEEE P802.3bm, IEEE Draft Standard for Ethernet. Amendment: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation Over Fiber Optic Cables.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3bm™-201x).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2012 and are not maintained as separate documents.

At the date of IEEE Std 802.3bm-201x publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2012

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 90 and Annex 83A through Annex 86A. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 89 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bk™-2013

Amendment 1—This amendment includes changes to EPON as defined in IEEE Std 802.3-2012 and adds the physical layer specifications and management parameters for EPON operation on point-to-multipoint passive optical networks supporting extended power budget classes of PX30 (29 dB for 1G-EPON), PX40 (33 dB for 1G-EPON), PRX40 (33 dB for 10/1G-EPON), and PR40 (33 dB for 10/10G-EPON).

IEEE Std 802.3bj™-201x

This amendment includes changes to IEEE Std 802.3-2012 and adds Clause 91 through Clause 94 as well as associated annexes. This amendment adds 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables.

IEEE Std 802.3bm™-201x

This amendment includes changes to IEEE Std 802.3-2012 and adds Clause 95 as well as associated annexes. This amendment adds Physical Layer (PHY) specifications and management parameters for 40 Gb/s operation over single-mode fiber (40GBASE-ER4) and for 100 Gb/s operation over multimode fiber (100GBASE-SR4). This amendment also specifies a four-lane variant of the 100 Gigabit Attachment Unit Interface (CAUI-4) and optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over fiber optic cables.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Errata, if any, for this and all other standards can be accessed at the following URL: http://standards.ieee.org/findstds/errata/index.html. Users are encouraged to check this URL for errata periodically.

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[Sponsor ballot
names to be added here]

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Contents

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NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

TO BE REMOVED PRIOR TO FINAL PUBLICATION: Reviewers and the publication editor should note that editing instructions have been written to minimize the probability of changes being lost at publication from other IEEE 802.3 amendment projects running in parallel (e.g., IEEE P802.3bj and IEEE P802.3bk) that modified the same text and tables.

1. Introduction

1.1.3.2 Compatibility interfaces

Change item m) as follows:

m) *100 Gigabit Attachment Unit Interface (CAUI-n)*. The CAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, and a four-lane version (CAUI-4) in Annex 83D and Annex 83E. No mechanical connector is specified for use with the CAUI-n. The CAUI-n is optional.

1.3 Normative references

Insert the following references in alphanumerical order:

IEC 61753-1:2007, Fibre optic interconnecting devices and passive components performance standard—Part 1: General and guidance for performance standards.

IEC 61754-7-1:201x, Fibre optic interconnecting devices and passive components—Fibre optic connector interfaces—Part 7-1: Type MPO connector family-Single fibre row.

[Editor's note (to be removed prior to publication) - IEC 61754-7-1 is currently in IEC approval process, expected publication August 2014. The connector types referenced here are currently described in IEC 61754-7.]

1.4 Definitions

Insert the following new definition into the list immediately after 1.4.53 (100GBASE-LR4 renumbered from 1.4.54 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.53a 100GBASE-SR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 95.)

Insert the following new definition into the list immediately after 1.4.60 (40GBASE-CR4 renumbered from 1.4.61 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.60a 40GBASE-ER4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 87.)

Change 1.4.73 (renumbered from 1.4.74 due to the deletion of 1.4.27 by IEEE Std 802.3bk-2013) as follows:

1.4.73 100 Gigabit Attachment Unit Interface (CAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Two widths of CAUI-n are defined: a ten-lane version (CAUI-10), and a four-lane version (CAUI-4). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, or Annex 83D and Annex 83E for CAUI-4.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphabetical order:

[Editor's note (to be removed prior to publication) - any new abbreviations to be added here.]

Change the abbreviation "CAUI" as follows:

CAUI-n	100 Gigabit Attachment Unit Interface over n lanes

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.2 Functional specifications

22.2.4 Management functions

22.2.4.3 Extended capability registers

22.2.4.3.1 PHY Identifier (Registers 2 and 3)

Insert the following note at the end of 22.2.4.3.1:

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. The definition of vendor specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or Company ID.

Editor's Note (to be removed prior to publication): inserted based on maintenance request 1252.
See http://www.ieee802.org/3/maint/requests/maint_1252.pdf

30. Management

30.5.1.1.2 aMAUType

Insert 40GBASE-ER4 PHY type into "APPROPRIATE SYNTAX" section of 30.5.1.1.2 after 40GBASE-LR4:

...

40GBASE-ER4	40GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with extended reach, as specified in Clause 87

...

Insert 100GBASE-SR4 PHY type into "APPROPRIATE SYNTAX" section of 30.5.1.1.2 immediately above 100GBASE-SR10:

...

100GBASE-SR4	100GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 95

...

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the identified reserved row in Table 45-3 (as modified by IEEE Std 802.3bj-201x) and insert four new rows immediately below the changed row as follows:

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.176 through 1.~~199~~178	Reserved	
1.179	CAUI-4 chip-to-module recommended CTLE	45.2.1.92a
1.180 through 1.183	CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 through lane 3	45.2.1.92b 45.2.1.92c
1.184 through 1.187	CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 3	45.2.1.92d 45.2.1.92e
1.188 through 1.199	Reserved	

Change the text of 45.2.1.3 to add a note as follows:

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number.

A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier to indicate that a unique identifier as described above is not provided.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. The definition of vendor specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or Company ID.

Editor's Note (to be removed prior to publication): inserted based on maintenance request 1252.
See http://www.ieee802.org/3/maint/requests/maint_1252.pdf

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as modified by IEEE Std 802.3bj-201x and IEEE Std 802.3bk-2013) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:10	Reserved	Value always 0, writes ignored	R/W
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7:6	Reserved	Value always 0, writes ignored	R/W

Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = reserved for future use 1 0 1 1 1 1 = 100GBASE-SR4 PMA/PMD ~~reserved for future use~~ 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 1 0 0 1 1 x = reserved for future use 1 0 0 1 0 1 = 40GBASE-ER4 PMA/PMD ~~reserved for future use~~ 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 1 1 1 1 0 = 10GBASE-PR-U4 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 1 1 1 0 0 = 10GBASE-PR-D4 0 1 1 0 1 1 = reserved 0 1 1 0 1 0 = 10GBASE-PR-U3 0 1 1 0 0 1 = 10GBASE-PR-U1 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 1 0 1 0 1 = 10GBASE-PR-D3 0 1 0 1 0 0 = 10GBASE-PR-D2 0 1 0 0 1 1 = 10GBASE-PR-D1 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	R/W

[a]R/W = Read/Write

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Change Table 45–9 (as modified by IEEE Std 802.3bj-201x) as follows:

Table 45–9—Transmit fault description location

PMA/PMD	Description location
10GBASE-KR	72.6.8
10GBASE-LRM	68.4.8
10GBASE-S, 10GBASE-L, 10GBASE-E	52.4.8
10GBASE-LX4	53.4.10
10GBASE-CX4	54.5.10
10GBASE-T	55.4.2.2
10GBASE-KX4	71.6.10
40GBASE-KR4	84.7.10
40GBASE-CR4, 100GBASE-CR10	85.7.10
40GBASE-SR4, 100GBASE-SR10	86.5.10
40GBASE-LR4, 40GBASE-ER4	87.5.10
40GBASE-FR	89.5.8
100GBASE-KP4	94.3.8
100GBASE-KR4	93.7.10
100GBASE-CR4	92.7.10
100GBASE-SR4	95.5.10
100GBASE-LR4, 100GBASE-ER4	88.5.10

45.2.1.7.5 Receive fault (1.8.10)

Change Table 45–10 (as modified by IEEE Std 802.3bj-201x) as follows:

Table 45–10—Receive fault description location

PMA/PMD	Description location
10GBASE-KR	72.6.9
10GBASE-LRM	68.4.9
10GBASE-S, 10GBASE-L, 10GBASE-E	52.4.9
10GBASE-LX4	53.4.11
10GBASE-CX4	54.5.11
10GBASE-T	55.4.2.4
10GBASE-KX4	71.6.11
40GBASE-KR4	84.7.11
40GBASE-CR4, 100GBASE-CR10	85.7.11
40GBASE-SR4, 100GBASE-SR10	86.5.11
40GBASE-LR4, 40GBASE-ER4	87.5.11
40GBASE-FR	89.5.9
100GBASE-KP4	94.3.9
100GBASE-KR4	93.7.11
100GBASE-CR4	92.7.11
100GBASE-SR4	95.5.11
100GBASE-LR4, 100GBASE-ER4	88.5.11

45.2.1.8 PMD transmit disable register (Register 1.9)

Change Table 45–11a (as inserted by IEEE Std 802.3bj-201x) as follows:

Table 45–11a—Transmit disable description location

PMA/PMD	Description location
10GBASE-KR	72.6.5
10GBASE-LRM	68.4.7
Other 10GBASE-R	52.4.7
10GBASE-LX4	53.4.7
10GBASE-CX4	54.5.6
10GBASE-T	55.4.2.3
10GBASE-KX4	71.6.6
40GBASE-KR4	84.7.6
40GBASE-CR4 and 100GBASE-CR10	85.7.6
40GBASE-SR4 and 100GBASE-SR10	86.5.7
40GBASE-LR4 and 40GBASE-ER4	87.5.7
40GBASE-FR	89.5.6
100GBASE-KP4	94.3.6.6
100GBASE-KR4	93.7.6
100GBASE-CR4	92.7.6
100GBASE-SR4	95.5.7
100GBASE-LR4 and 100GBASE-ER4	88.5.7

45.2.1.12 40G/100G PMA/PMD extended ability register (Register 1.13)

Change Table 45–15 (as modified by IEEE Std 802.3bj-201x) as follows:

Table 45–15—40G/100G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.13.15	PMA remote loopback ability	1 = PMA has the ability to perform a remote loopback function 0 = PMA does not have the ability to perform a remote loopback function	RO
1.13.14	100GBASE-CR4 ability	1 = PMA/PMD is able to perform 100GBASE-CR4 0 = PMA/PMD is not able to perform 100GBASE-CR4	RO
1.13.13	100GBASE-KR4 ability	1 = PMA/PMD is able to perform 100GBASE-KR4 0 = PMA/PMD is not able to perform 100GBASE-KR4	RO

Table 45–15—40G/100G PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.13.12	100GBASE-KP4 ability	1 = PMA/PMD is able to perform 100GBASE-KP4 0 = PMA/PMD is not able to perform 100GBASE-KP4	RO
1.13.11	100GBASE-ER4 ability	1 = PMA/PMD is able to perform 100GBASE-ER4 0 = PMA/PMD is not able to perform 100GBASE-ER4	RO
1.13.10	100GBASE-LR4 ability	1 = PMA/PMD is able to perform 100GBASE-LR4 0 = PMA/PMD is not able to perform 100GBASE-LR4	RO
1.13.9	100GBASE-SR10 ability	1 = PMA/PMD is able to perform 100GBASE-SR10 0 = PMA/PMD is not able to perform 100GBASE-SR10	RO
1.13.8	100GBASE-CR10 ability	1 = PMA/PMD is able to perform 100GBASE-CR10 0 = PMA/PMD is not able to perform 100GBASE-CR10	RO
1.13.7	100GBASE-SR4 ability	1 = PMA/PMD is able to perform 100GBASE-SR4 0 = PMA/PMD is not able to perform 100GBASE-SR4	RO
1.13.6~~7.5~~	Reserved	Ignore on read	RO
1.13.5	40GBASE-ER4 ability	1 = PMA/PMD is able to perform 40GBASE-ER4 0 = PMA/PMD is not able to perform 40GBASE-ER4	RO
1.13.4	40GBASE-FR ability	1 = PMA/PMD is able to perform 40GBASE-FR 0 = PMA/PMD is not able to perform 40GBASE-FR	RO
1.13.3	40GBASE-LR4 ability	1 = PMA/PMD is able to perform 40GBASE-LR4 0 = PMA/PMD is not able to perform 40GBASE-LR4	RO
1.13.2	40GBASE-SR4 ability	1 = PMA/PMD is able to perform 40GBASE-SR4 0 = PMA/PMD is not able to perform 40GBASE-SR4	RO
1.13.1	40GBASE-CR4 ability	1 = PMA/PMD is able to perform 40GBASE-CR4 0 = PMA/PMD is not able to perform 40GBASE-CR4	RO
1.13.0	40GBASE-KR4 ability	1 = PMA/PMD is able to perform 40GBASE-KR4 0 = PMA/PMD is not able to perform 40GBASE-KR4	RO

[a]RO = Read only

Insert 45.2.1.12.5a and 45.2.1.12.5b after 45.2.1.12.5 as follows:

45.2.1.12.5a 100GBASE-SR4 ability (1.13.7)

When read as a one, bit 1.13.7 indicates that the PMA/PMD is able to operate as a 100GBASE-SR4 PMA/PMD type. When read as a zero, bit 1.13.7 indicates that the PMA/PMD is not able to operate as a 100GBASE-SR4 PMA/PMD type.

45.2.1.12.5b 40GBASE-ER4 ability (1.13.5)

When read as a one, bit 1.13.5 indicates that the PMA/PMD is able to operate as a 40GBASE-ER4 PMA/PMD type. When read as a zero, bit 1.13.5 indicates that the PMA/PMD is not able to operate as a 40GBASE-ER4 PMA/PMD type.

Insert 45.2.1.92a through 45.2.1.92e after 45.2.1.92 as follows:

45.2.1.92a CAUI-4 chip-to-module recommended CTLE register (Register 1.179)

The assignment of bits in the CAUI-4 chip-to-module recommended CTLE register is shown in Table 45–71a.

Table 45–71a—CAUI-4 chip-to-module recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.179.15:5	Reserved	Value always 0, writes ignored	RO
1.179.4:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = reserved 1 0 1 x = reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = reserved	R/W
1.179.0	Reserved	Value always 0, writes ignored	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.92a.1 Recommended CTLE peaking (1.179.4:1)

The value of these bits sets the CTLE peaking value recommended by a host that implements the optional CAUI-4 chip-to-module interface defined in Annex 83E (see 83E.3.1.6). The module may optionally use this information to adjust its CTLE setting.

45.2.1.92b CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.180)

The assignment of bits in the CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–71b.

45.2.1.92b.1 Post-cursor setting (1.180.4:2)

The value of these bits sets the post-cursor coefficient c(1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1).

45.2.1.92b.2 Pre-cursor setting (1.180.1:0)

The value of these bits sets the pre-cursor coefficient c(–1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1).

45.2.1.92c CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers (Registers 1.181, 1.182, 1.183)

The CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers are defined similarly to register 1.180 (which is used for lane 0, see 45.2.1.92b) but for lanes 1 through 3 respectively.

Table 45–71b—CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.180.15:5	Reserved	Value always 0, writes ignored	RO
1.180.4:2	Post-cursor setting	4 3 2 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = –0.25 1 0 0 = –0.2 0 1 1 = –0.15 0 1 0 = –0.1 0 0 1 = –0.05 0 0 0 = 0	R/W
1.180.1:0	Pre-cursor setting	1 0 1 1 = –0.15 1 0 = –0.1 0 1 = –0.05 0 0 = 0	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.92d CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.184)

The assignment of bits in the CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–71c.

Table 45–71c—CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.184.15:5	Reserved	Value always 0, writes ignored	RO
1.184.4:2	Post-cursor setting	4 3 2 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = –0.25 1 0 0 = –0.2 0 1 1 = –0.15 0 1 0 = –0.1 0 0 1 = –0.05 0 0 0 = 0	R/W
1.184.1:0	Pre-cursor setting	1 0 1 1 = –0.15 1 0 = –0.1 0 1 = –0.05 0 0 = 0	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.92d.1 Post-cursor setting (1.184.4:2)

The value of these bits sets the post-cursor coefficient c(1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1).

45.2.1.92d.2 Pre-cursor setting (1.184.1:0)

The value of these bits sets the pre-cursor coefficient c(–1) for the CAUI-4 chip-to-chip transmitter equalization for the lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1).

45.2.1.92e CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers (Registers 1.185, 1.186, 1.187)

The CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers are defined similarly to register 1.184 (which is used for lane 0, see 45.2.1.92d) but for lanes 1 through 3 respectively.

69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

Subclause 69.1.3 has been renumbered to 69.1.2 by IEEE Std 802.3bj-201x.

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change items f) and g) (as respectively modified and inserted by IEEE Std 802.3bj-201x) as follows:

f) The PMA service interface, which, when physically implemented as XLAUI (40 Gigabit Attachment Unit Interface) or as CAUI-4 (100 Gigabit four-lane Attachment Unit Interface) at an observable interconnection port, uses a four-lane data path as specified in Annex 83A or Annex 83D, respectively.

g) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gigabit ten-lane Attachment Unit Interface) at an observable interconnection port, uses a ten-lane data path as specified in Annex 83A.

69.2 Summary of Backplane Ethernet Sublayers

69.2.3 Physical Layer signaling systems

Change Table 69-1a (as inserted by IEEE Std 802.3bj-201x) as follows:

Table 69–1a—Nomenclature and clause correlation for 40 Gb/s and 100 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause																
	73	74	78	81			82		83		83A		83D	84	91	93	94
	Auto-Negotiation	BASE-R FEC	Energy-Efficient Ethernet (EEE)	RS	XLGMII	CGMII	40GBASE-R PCS	100GBASE-R PCS	40GBASE-R PMA	100GBASE-R PMA	XLAUI	CAUI-10	CAUI-4	40GBASE-KR4 PMD	RS-FEC	100GBASE-KR4 PMD	100GBASE-KP4 PMA/PMD
40GBASE-KR4	M[a]	O[a]	O	M	O		M		M		O			M			
100GBASE-KR4	M		O	M		O		M		M		O	O		M	M	
100GBASE-KP4	M		O	M		O		M				O	O		M		M

[a]O = Optional, M = Mandatory

74. Forward Error Correction (FEC) sublayer for BASE-R PHYs

74.4 Inter-sublayer interfaces

Change the second paragraph of 74.4 as follows:

For 40GBASE-R and 100GBASE-R the FEC service interface can either connect to the PCS as illustrated in Figure 74–1 or the PMA as illustrated in Figure 83–2 where the FEC and PCS are in separate devices connected by XLAUI/CAUI-n.

74.5 FEC service interface

Change the third paragraph of 74.5 as follows:

Optional physical instantiations of the PMA service interface have been defined (see Clause 51, Annex 83A, ~~and~~ Annex 83B, Annex 83D, and Annex 83E). There is XSBI (10 Gigabit Sixteen-Bit Interface) for 10GBASE-R, XLAUI for 40GBASE-R and CAUI-n for 100GBASE-R. These physical instantiations, with a PMA if required, may also be used for the FEC service interface.

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

Change the third paragraph of 78.1 (as inserted by IEEE Std 802.3bj-201x) as follows:

EEE supports operation over twisted-pair cabling systems, twinax cable, electrical backplanes, optical fiber, the XGXS for 10 Gb/s PHYs, the XLAUI for 40 Gb/s PHYs and the CAUI-10 or CAUI-4 for 100 Gb/s PHYs. Table 78–1 lists the supported PHYs and interfaces and their associated clauses.

78.1.1 LPI Signaling

Change the fifth paragraph of 78.1.1 (as inserted by IEEE Std 802.3bj-201x) as follows:

Coding defined in Clause 83 also allows LPI transmit quiet and alert requests from the PCS to be signaled over the XLAUI and CAUI-n interfaces. The XLAUI and CAUI-n receive interfaces infer the quiet and alert requests from the data received over the interface and use that to recreate the transmit or receive direction signaling. See 83.5.11.1.

78.1.3 Reconciliation sublayer operation

78.1.3.3 PHY LPI operation

78.1.3.3.1 PHY LPI transmit operation

Change the last paragraph of 78.1.3.3.1 (as inserted by IEEE Std 802.3bj-201x) as follows:

For PHYs with an operating speed of 40 Gb/s or greater that implement the optional EEE capability, two modes of LPI operation may be supported: deep sleep and fast wake. Deep sleep refers to the mode for which the transmitter ceases transmission during Low Power Idle (as shown in Figure 78-3) and is equivalent to the only mechanism defined for PHYs with an operating speed less than 40 Gb/s. Deep sleep support is optional for PHYs with an operating speed of 40 Gb/s or greater that implement EEE with the exception of the PHYs noted in Table 78–1 which do not support deep sleep. Fast wake refers to the mode for which the transmitter continues to transmit signals during Low Power Idle so that the receiver can resume operation with a shorter wake time (as shown in Figure 78-3a). For transmit, other than the PCS encoding LPI, there is no difference between fast wake and normal operation. Fast wake support is mandatory for PHYs with an operating speed of 40 Gb/s or greater that implement EEE.

78.1.4 PHY types optionally supporting EEE

Change Table 78-1 (as modified by IEEE Std 802.3bj-201x) as follows:

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
10BASE-Te	14
100BASE-TX	24, 25
1000BASE-KX	70, 36
1000BASE-T	40
XGXS (XAUI)	47, 48
10GBASE-KX4	71, 48
10GBASE-KR	72, 51, 49, 74
10GBASE-T	55
XLAUI/CAUI-10[a]	83A
40GBASE-KR4	82, 83, 84, 74
40GBASE-CR4	82, 83, 85, 74
40GBASE-SR4[b]	82, 83, 86
40GBASE-FR[b]	82, 83, 89
40GBASE-LR4[b]	82, 83, 87
40GBASE-ER4[b]	82, 83, 87
CAUI-4[a]	83D
100GBASE-KP4	82, 91, 94
100GBASE-KR4	82, 83, 91, 93
100GBASE-CR10	82, 83, 85, 74
100GBASE-CR4	82, 83, 91, 92
100GBASE-SR10[b]	82, 83, 86
100GBASE-SR4[b]	82, 83, 91, 95
100GBASE-LR4[b]	82, 83, 88
100GBASE-ER4[b]	82, 83, 88

[a]XLAUI/CAUI-n shutdown is only supported when deep sleep is enabled.
[b]The deep sleep mode of EEE is not supported for this PHY.

78.5 Communication link access latency

Change the row for XLAUI/CAUI in Table 78-4 (as modified by IEEE Std 802.3bj-201x) as follows:

Change the title and first paragraph of 78.5.2 (as inserted by IEEE Std 802.3bj-201x) as follows:

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
100BASE-TX		30	20.5	5.0	15	10
1000BASE-T	Case-1	16.5	16.5	5.0	2.5	1.76
	Case-2	16.5	16.5	12.24	9.74	1.76
1000BASE-KX		13.26	11.25	5.0	6.5	1.76
XGXS (XAUI)		12.38	9.25	5.0	4.5	2.88
10GBASE-T	Case-1	7.36	7.36	4.48	0	2.88
	Case-2	4.48	4.48	1.6	0	2.88
10GBASE-KX4		12.38	9.25	5.0	4.5	2.88
10GBASE-KR	Case-1	15.38	12.25	5.0	7.5	2.88
	Case-2	17.38	14.25	5.0	9.5	2.88
40GBASE-R fast wake		0.34	0.3	0	0	0.25
40GBASE-CR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2
40GBASE-KR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2
100GBASE-R fast wake		0.34	0.3	0	0	0.25
100GBASE-CR10	Case-1	5.5	5.5	2	3	1
	Case-2	7.5	7.5	2	3	1
100GBASE-CR4		5.5	5.5	2	3	1
100GBASE-KR4		5.5	5.5	2	3	1
100GBASE-KP4		5.5	5.5	2	3	1
XLAUI/CAUI-n[a]		1				

[a] $T_{w\_sys\_tx}$ is increased by 1 μs for each instance of XLAUI/CAUI-n with shutdown enabled on the transmit path.The receiver should negotiate an increase for remote T_{w_sys} for the link partner of 1 μs for each instance of XLAUI/CAUI-n with shutdown enabled on the receive path.

78.5.2 40 Gb/s and 100 Gb/s PHY extension using XLAUI or CAUI-n

40 Gb/s ~~and 100 Gb/s~~ PHYs may be extended using XLAUI and 100 Gb/s PHYs may be extended using CAUI-10 or CAUI-4 as a physical instantiation of the inter-sublayer service interface to separate functions between devices. The LPI signaling can operate across XLAUI/CAUI-n with no change to the PHY timing parameters described in Table 78–4 or the operation of the Data Link Layer Capabilities negotiation described in 78.4.

If PMA Egress AUI Stop Enable (PEASE, see 83.3; MDIO register bit 1.7.8) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI/CAUI-n in the transmit direction to conserve energy. If PEASE is asserted, the RS defers sending data following deassertion of LPI by an additional time equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ as shown in Table 78–4 for each PMA with PEASE asserted (see 81.3a.2.1).

If PMA Ingress AUI Stop Enable (PIASE, see 83.3; MDIO register bit 1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI/CAUI-n in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} (equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI/CAUI-n as shown in Table 78–4) for each PMA with PIASE to be asserted before setting the PIASE bits.

80. Introduction to 40 Gb/s and 100 Gb/s networks

80.1 Overview

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

Change items c), d), and h) in 80.1.3 (as modified by IEEE Std 802.3bj-201x) as follows:

c) The PMA service interface, which, when physically implemented as XLAUI (40 Gigabit Attachment Unit Interface) or CAUI-4 (100 Gigabit four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A, ~~or~~ Annex 83B, Annex 83D, or Annex 83E.

d) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gigabit ten-lane Attachment Unit Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 83A or Annex 83B.

h) The MDIs as specified in Clause 84 for 40GBASE-KR4, in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, in Clause 87 for 40GBASE-LR4 and 40GBASE-ER4, in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4, ~~and~~ in Clause 92 for 100GBASE-CR4, and in Clause 95 for 100GBASE-SR4 all use a 4 lane data path.

80.1.4 Nomenclature

Insert new rows to Table 80-1 (as modified by IEEE Std 802.3bj-201x) as follows, with the 40GBASE-ER4 row immediately below 40GBASE-LR4 and the 100GBASE-SR4 row immediately above 100GBASE-SR10:

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
40GBASE-ER4	40 Gb/s PHY using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 87)
100GBASE-SR4	100 Gb/s PHY using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 95)

80.1.5 Physical Layer signaling systems

Table 80-2 was split into two tables (Table 80-2 and Table 80-2a) by IEEE Std 802.3bj-201x.

Change the text of 80.1.5 (as modified by IEEE Std 802.3bj-201x), change Table 80-2, replace Table 80-2a and insert Table 80-2b as follows:

This standard specifies a family of Physical Layer implementations. Table 80–2, ~~and~~ Table 80–2a, and Table 80–2b specify the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures must meet the requirements of the corresponding clauses.

Table 80–2—Nomenclature and clause correlation (40GBASE)

Nomenclature	Clause[a]															
	73	74	78	81		82	83	83A	83B	84	85	86	86A	87		89
	Auto-Negotiation	BASE-R FEC	EEE	RS	XLGMII	40GBASE-R PCS	40GBASE-R PMA	XLAUI	XLAUI	40GBASE-KR4 PMD	40GBASE-CR4 PMD	40GBASE-SR4 PMD	XLPPI	40GBASE-LR4 PMD	40GBASE-ER4 PMD	40GBASE-FR PMD
40GBASE-KR4	M	O	O	M	O	M	M	O		M						
40GBASE-CR4	M	O	O	M	O	M	M	O			M					
40GBASE-SR4			O	M	O	M	M	O	O			M	O			
40GBASE-FR			O	M	O	M	M	O	O							M
40GBASE-LR4			O	M	O	M	M	O	O				O	M		
40GBASE-ER4			O	M	O	M	M	O	O						M	

[a]O = Optional, M = Mandatory.

Table 80–2a—Nomenclature and clause correlation (100GBASE copper)

Nomenclature	Clause[a]													
	73	74	78	81		82	83	83A	83D	85	91	92	93	94
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-4	100GBASE-CR10 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD
100GBASE-KR4	M		O	M	O	M	M	O	O		M		M	
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M
100GBASE-CR4	M		O	M	O	M	M	O	O		M	M		
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M				

[a]O = Optional, M = Mandatory.

Table 80–2b—Nomenclature and clause correlation (100GBASE optical)

Nomenclature	Clause[a]														
	78	81		82	83	83A	83B	83D	83E	86	86A	88		91	95
	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	100GBASE-SR10 PMD	CPPI	100GBASE-LR4 PMD	100GBASE-ER4 PMD	RS-FEC	100GBASE-SR4 PMD
100GBASE-SR10	O	M	O	M	M	O	O	O	O	M	O				
100GBASE-SR4	O	M	O	M	M	O	O	O	O					M	M
100GBASE-LR4	O	M	O	M	M	O	O	O	O			M			
100GBASE-ER4	O	M	O	M	M	O	O	O	O				M		

[a]O = Optional, M = Mandatory.

80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers

Change the first paragraph of 80.2.3 (as modified by IEEE Std 802.3bj-201x) as follows:

80.2.3 Forward Error Correction (FEC) sublayers

A Forward Error Correction sublayer is available for all 40GBASE-R and 100GBASE-R copper and backplane PHYs as well as 100GBASE-SR4. It is optional for 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR4, 100GBASE-KR4, ~~and~~ 100GBASE-KP4, and 100GBASE-SR4 PHYs.

Change the second paragraph of 80.2.5 (as modified by IEEE Std 802.3bj-201x) as follows:

80.2.5 Physical Medium Dependent (PMD) sublayer

The 40GBASE-R, 100GBASE-R, and 100GBASE-P PMDs and their corresponding media are specified in Clause 84 through Clause 89, and Clause 92 through ~~Clause 94~~Clause 95.

80.4 Delay constraints

Insert new rows to Table 80-3 (as modified by IEEE Std 802.3bj-201x) as follows, with the 40GBASE-ER4 row immediately below 40GBASE-LR4 and the 100GBASE-SR4 row immediately above 100GBASE-SR10:

Table 80–3—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
40GBASE-ER4 PMD	1024	2	25.6	Includes 2 m of fiber. See 87.3.1.
100GBASE-SR4 PMD	2048	4	20.48	Includes 2 m of fiber. See 95.3.1.

[a] For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.110 for the definition of bit time.)
[b] For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

80.5 Skew constraints

Change the third, fourth and fifth paragraphs of 80.5 as follows:

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP1, SP2, and SP3 for the transmit direction and SP4, SP5, and SP6 for the receive direction as illustrated in Figure 80–4 (single XLAUI or CAUI-n interface) and Figure 80–5 (multiple XLAUI or CAUI-n interfaces).

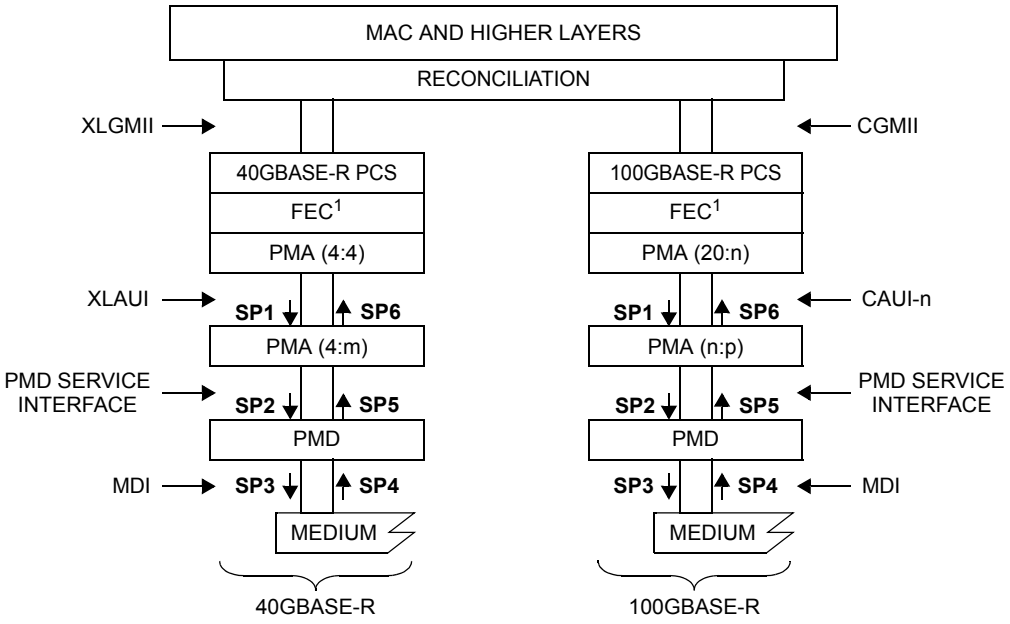
In the transmit direction, the Skew points are defined in the following locations:

— SP1 on the XLAUI/CAUI-n interface, at the input of the PMA closest to the PMD;
— SP2 on the PMD service interface, at the input of the PMD;
— SP3 at the output of the PMD, at the MDI.

In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD;
— SP5 on the PMD service interface, at the output of the PMD;
— SP6 on the XLAUI/CAUI-n interface, at the output of the PMA closest to the PCS.

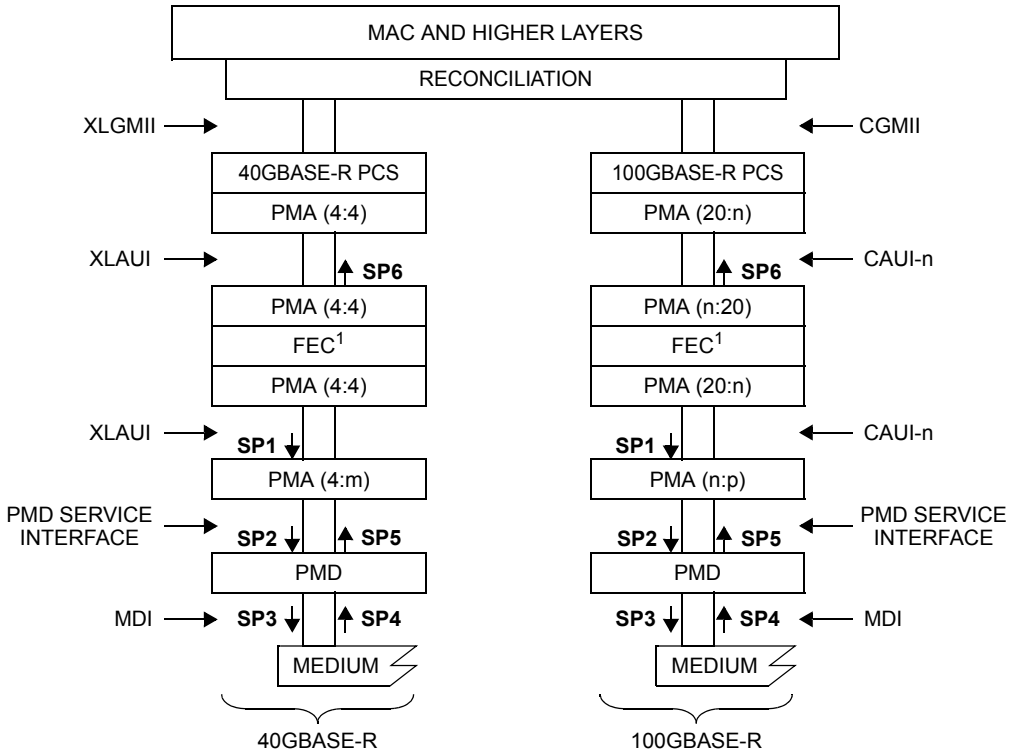
Replace Figure 80-4, Figure 80-5 and Figure 80-5a (as modified or inserted by IEEE Std 802.3bj-201x) for CAUI naming as follows:



CAUI-n = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

m = 1 or 4
n = 4 or 10
p = 4 or 10
NOTE1—CONDITIONAL BASED ON PHY TYPE

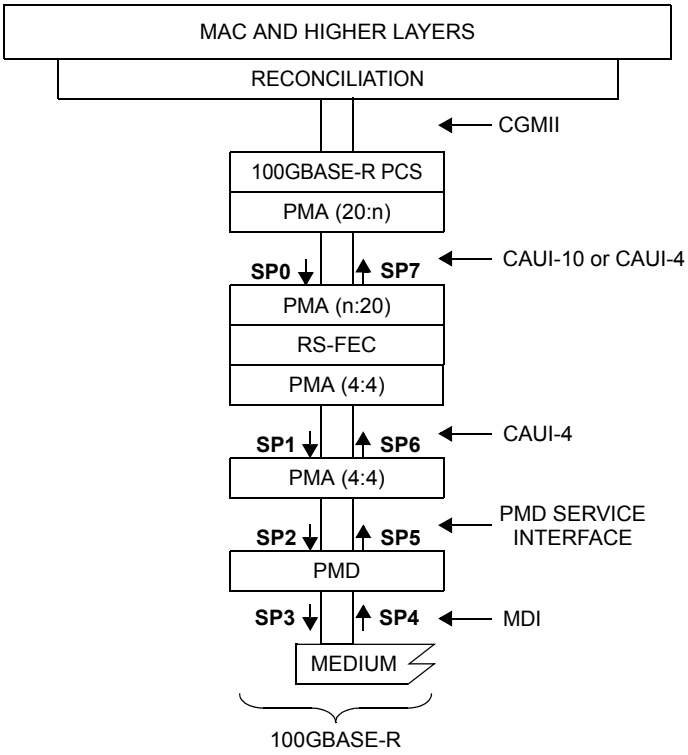
Figure 80–4—40GBASE-R and 100GBASE-R Skew points for single XLAUI or CAUI-n



CAUI-n = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

m = 1 or 4
n = 4 or 10
p = 4 or 10
NOTE1—CONDITIONAL BASED ON PHY TYPE

Figure 80–5—40GBASE-R and 100GBASE-R Skew points for multiple XLAUI or CAUI-n



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
n = 4 or 10

Figure 80–5a—100GBASE-R Skew points with RS-FEC and CAUI-n

Change Table 80-4 and Table 80-5 (as modified by IEEE Std 802.3bj-201x) as follows:

Table 80–4—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 40GBASE-R PCS lane (UI)[b]	Maximum Skew for 100GBASE-R PCS lane (UI)[c]	Notes[d]
SP0	29	N/A	≈ 150	See 83.5.3.1
SP1	29	≈ 299	≈ 150	See 83.5.3.1
SP2	43	≈ 443	≈ 222	See 83.5.3.3, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP3	54	≈ 557	≈ 278	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP4	134	≈ 1382	≈ 691	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP5	145	≈ 1495	≈ 748	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP6	160	≈ 1649	≈ 824	See 83.5.3.5
SP7	29	N/A	≈ 150	See 83.5.3.5
At PCS receive	180	≈ 1856	≈ 928	See 82.2.12
At RS-FEC transmit	49	N/A	≈ 253	See 91.5.2.2
At RS-FEC receive[e]	180	N/A	≈ 4641	See 91.5.3.1
At PCS receive (with RS-FEC)	49	N/A	≈ 253	See 82.2.12

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PCS lane signaling rate of 10.3125 GBd.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 100GBASE-R, based on 1 UI equals 193.939394 ps at PCS lane signaling rate of 5.15625 GBd.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.
[e]The skew at the RS-FEC receive is the skew between RS-FEC lanes. The symbol ≈ indicates approximate equivalent of maximum Skew in UI for RS-FEC lanes with a signaling rate of 25.78125 GBd.

Table 80–5—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 10.3125 GBd PMD lane (UI)[a]	Maximum Skew Variation for 25.78125 GBd PMD lane (UI)[b]	Notes[c]
SP0	0.2	≈ 2	N/A	See 83.5.3.1
SP1	0.2	≈ 2	N/A	See 83.5.3.1
SP2	0.4	≈ 4	≈ 10	See 83.5.3.3, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP3	0.6	≈ 6	≈ 15	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP4	3.4	≈ 35	≈ 88	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP5	3.6	≈ 37	≈ 93	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, ~~or~~ 94.3.4, or 95.3.2
SP6	3.8	≈ 39	≈ 98	See 83.5.3.5
SP7	0.2	≈ 2	N/A	See 83.5.3.5
At PCS receive	4	≈ 41	N/A	See 82.2.12
At RS-FEC transmit	0.4	N/A	≈ 10	See 91.5.2.2
At RS-FEC receive[d]	4	N/A	≈ 103	See 91.5.3.1
At PCS receive (with RS-FEC)	0.4	N/A	≈ 2	See 82.2.12

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PMD lane signaling rate of 10.3125 GBd.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 100GBASE-R, based on 1 UI equals 38.787879 ps at PMD lane signaling rate of 25.78125 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.
[d]The skew at the RS-FEC receive is the skew between RS-FEC lanes.

80.7 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 80.7 as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, Clause 73, Clause 74, Clause 81 through Clause 89, Clause 91 through ~~Clause 94~~Clause 95, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

81. Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation (XLGMII and CGMII)

81.3a LPI Assertion and Detection

81.3a.2 Transmit LPI state diagram

81.3a.2.1 Variables and counters

Change the last paragraph of 81.3a.2.1 (as inserted by IEEE Std 802.3bj-201x) as follows:

tw_timer

A timer that counts the time since the de-assertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2. If PMA Ingress AUI Stop Enable (PIASE) bit (1.7.9) is asserted for any of the PMA sublayers, the terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 plus additional time equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI and CAUI-n as shown in Table 78–4 for each PMA with PIASE to be asserted. The signal tw_timer_done is asserted when tw_timer reaches its terminal count.

81.3a.4 Considerations for receive system behavior

Change the second paragraph of 81.3a.4 (as inserted by IEEE Std 802.3bj-201x) as follows:

If the PMA Ingress AUI Stop Enable (PIASE) bit (1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI and CAUI-n in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} (equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI and CAUI-n as shown in Table 78–4) for each PMA with PIASE to be asserted before setting the PIASE bits.

82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.1 Overview

82.1.4 Inter-sublayer interfaces

Change the first paragraph of 82.1.4 (as modified by IEEE Std 802.3bj-201x) as follows:

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XLGMII/CGMII. The lower interface of the PCS connects to the PMA sublayer to support a PMD. If the optional FEC sublayer is implemented (see Clause 74) and an optional physical instantiation, i.e., XLAUI or CAUI-n, is not implemented directly below the PCS sublayer, then the lower interface connects to the FEC sublayer. For Physical Layers that use Clause 91 RS-FEC, if an optional physical instantiation, i.e. CAUI-n, is not implemented directly below the PCS sublayer, then the lower interface connects to the RS-FEC sublayer. The 40GBASE-R PCS has a nominal rate at the PMA/FEC service interface of 10.3125 Gtransfers/s per PCS lane, which provides capacity for the MAC data rate of 40 Gb/s. The 100GBASE-R PCS has a nominal rate at the PMA/FEC service interface of 5.15625 Gtransfers/s per PCS lane, which provides capacity for the MAC data rate of 100 Gb/s.

82.2 Physical Coding Sublayer (PCS)

Change the text of 82.2.6 as follows:

82.2.6 Block distribution

Once the data is encoded and scrambled, it is distributed to multiple PCS lanes, 66-bit blocks at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. This allows the PCS to support multiple physical lanes in the PMD and XLAUI or CAUI-n interfaces (see Annex 83A, ~~and~~ Annex 83B, Annex 83D, and Annex 83E). The 40GBASE-R PCS distributes the 66-bit blocks to 4 PCS lanes, and the 100GBASE-R PCS distributes the blocks to 20 PCS lanes. The distribution process is shown in Figure 82–6.

83. Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R

83.1 Overview

Change 83.1.1 (as modified by IEEE Std 802.3bj-201x) as follows:

83.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) that is common to two families of (40 Gb/s and 100 Gb/s) Physical Layer implementations, known as 40GBASE-R and 100GBASE-R. The PMA allows the PCS (specified in Clause 82) to connect in a media-independent way with a range of physical media. The 40GBASE-R PMA(s) can support any of the 40 Gb/s PMDs in Table 80–2. The 100GBASE-R PMA(s) can support any of the 100 Gb/s PMDs in Table 80–2a or Table 80–2b, but does not provide the PMD service interface for 100GBASE-KP4 (Clause 94). The terms 40GBASE-R and 100GBASE-R are used when referring generally to Physical Layers using the PMA defined in this clause.

40GBASE-R and 100GBASE-R can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

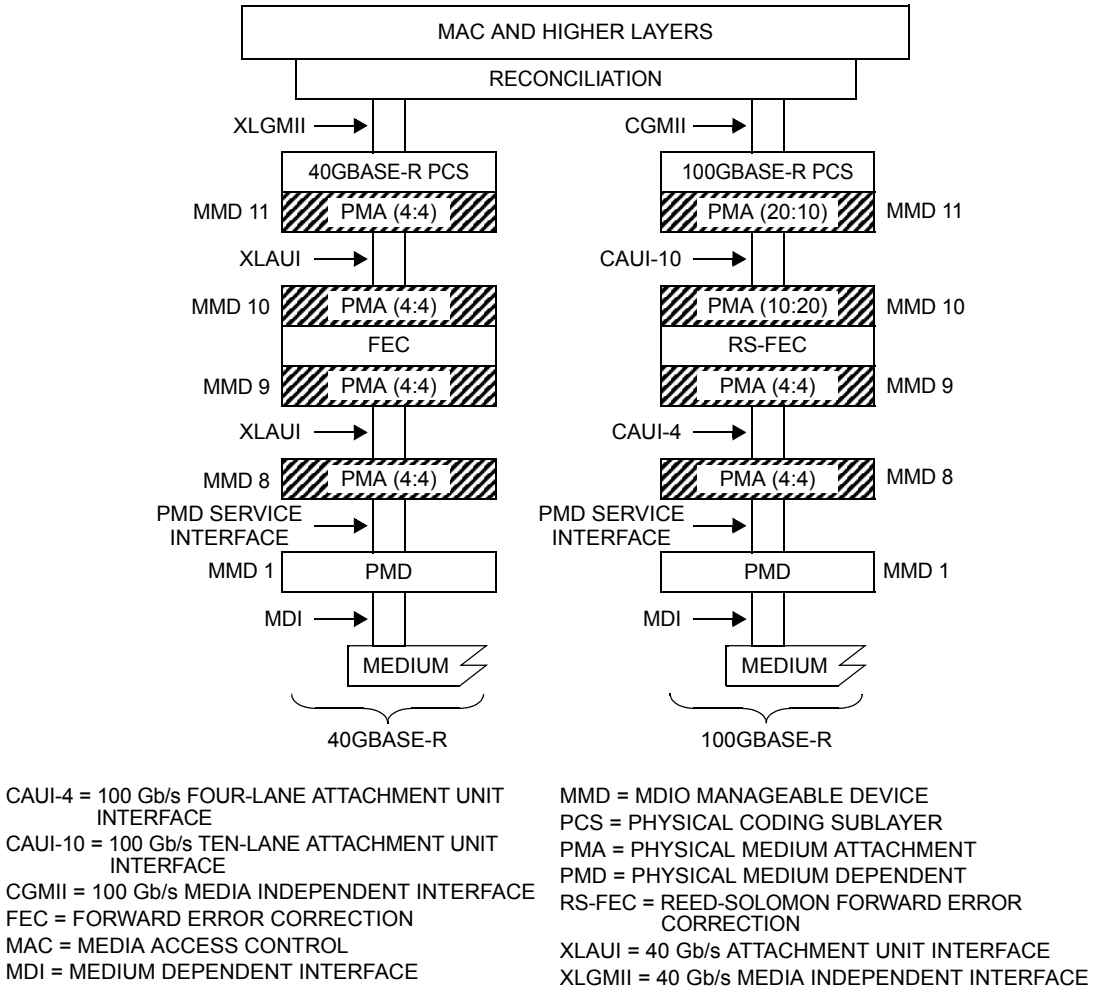
The interfaces for the inputs of the 40GBASE-R and 100GBASE-R PMAs are defined in an abstract manner and do not imply any particular implementation. The optional physical instantiation of the PMD service interfaces for 40GBASE-SR4, 40GBASE-LR4, and 100GBASE-SR10 PMDs, known as XLPPI and CPPI, are defined in Annex 86A. The PMD service interfaces for other PMDs are defined in an abstract manner according to 80.3.1. For 40GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as XLAUI, are defined in Annex 83A and Annex 83B. For 100GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as CAUI-n, are defined in Annex 83A, ~~and~~ Annex 83B, Annex 83D, and Annex 83E.

83.1.4 PMA sublayer positioning

Change the second paragraph of 83.1.4 as follows:

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, 10, and 11 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. If the PMD service interface is physically instantiated as nPPI (see Annex 86A), the PMA sublayer that is closest to the PMD will be addressed as MMD 8. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the PCS. The example shown in Figure 83–2 could be implemented with four addressable instances: MMD 8 addressing the lowest PMA sublayer (note that this cannot share MMD 1 with the PMD as they are not packaged together in this example), MMD 9 addressing the PMA sublayer above the XLAUI/CAUI-4 below the FEC, MMD 10 addressing the PMA sublayer below the XLAUI/CAUI-10 above the FEC, and MMD 11 addressing the PMA sublayer closest to the PCS.

Replace Figure 83-2 and change items b) and c) of 83.1.4 as follows:



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83–2—Example 40GBASE-R and 100GBASE-R PMA layering

b) XLAUI and CAUI-n are physical instantiations of the connection between two adjacent PMA sublayers.
   1) As a physical instantiation, it defines electrical and timing specification as well as requiring a receive re-timing function
   2) XLAUI is a 10.3125 GBd by 4 lane physical instantiation of the respective 40 Gb/s connection
   3) CAUI-10 is a 10.3125 GBd by 10 lane physical instantiation of the respective 100 Gb/s connection
   4) CAUI-4 is a 25.78125 GBd by 4 lane physical instantiation of the respective 100 Gb/s connection

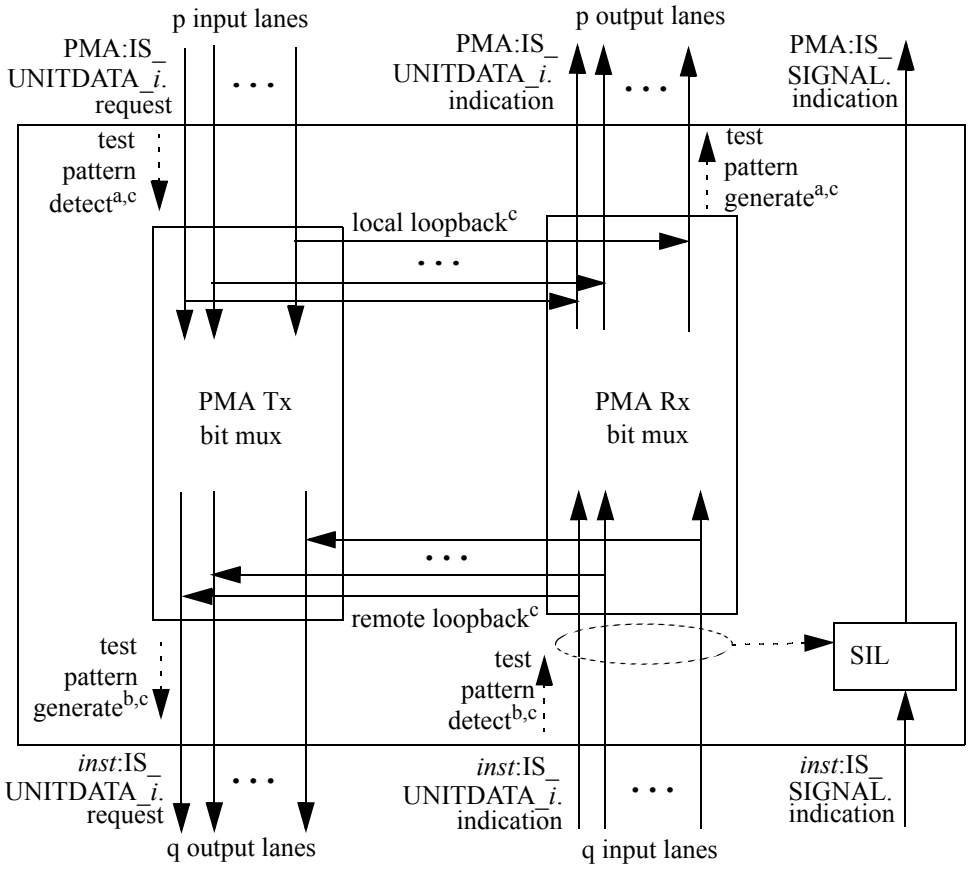
c) The abstract inter-sublayer service interface can be physically instantiated as a XLAUI or CAUI-n, using associated PMAs to map to the appropriate number of lanes.

83.2 PMA Interfaces

Change the third paragraph of 83.2 and replace Figure 83-5 (for naming of CAUI-n) as follows:

Figure 83–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

— The aggregate rate supported (40GBASE-R or 100GBASE-R).
— The numbers of input and output lanes in each direction.
— Whether the PMA is adjacent to a physically instantiated interface (XLAUI/CAUI-n above or below, or PMD service interface below).
— Whether the PMA is adjacent to the PCS (or adjacent to FEC when FEC is adjacent to the PCS).
— Whether the PMA is adjacent to the PMD.



inst PMD, PMA, or FEC, depending on which sublayer is below this PMA
SIL Signal Indication Logic

[a] If physically instantiated interface (XLAUI/CAUI-n) immediately above this PMA.
[b] If physically instantiated interface (XLAUI/CAUI-n or PMD service interface) immediately below this PMA, or if this is the closest PMA to the PMD.
[c] Optional.

Figure 83–5—PMA Functional Block Diagram

83.3 PMA service interface

Change the fifth paragraph of 83.3 as follows:

In the Tx direction, if the bit from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (XLAUI/CAUI-n), clock and data are recovered on the lane receiving the bit. The bit is routed through the PMA to an output lane through a process that may demultiplex PCSLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs to output lanes. The bit is sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (*k* not necessarily equal to *i*) primitive (see 83.4).

83.4 Service interface below PMA

Change the third and fifth paragraphs of 83.4 as follows:

The number of lanes q for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane *i* = 0 to q – 1 of the service interface below the PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., XLAUI/CAUI-n or nPPI), otherwise the service interface is specified only abstractly. The interface between the PMA and the sublayer below consists of q lanes for data transfer and a status indicating a good signal sent by the sublayer below the PMA (see Figure 83–5).

In the Rx direction, if the bit is received over a physically instantiated interface (XLAUI/CAUI-n or nPPI), clock and data are recovered on the lane receiving the bit. The bit is routed through the PMA to an output lane toward the PMA client through a process that may demultiplex PCSLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs to output lanes, and finally sending the bit on an output lane to the PMA client using the PMA:IS_UNITDATA_*k*.indication (*k* not necessarily equal to *i*) primitive at the PMA service interface.

83.5 Functions within the PMA

Change 83.5.1 as follows:

83.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as XLAUI/CAUI-n, the PMA shall meet the electrical and timing specifications in Annex 83A, ~~or~~ Annex 83B, Annex 83D, or Annex 83E as appropriate. If the interface between the sublayer below the PMA and the PMA is physically instantiated as XLAUI/CAUI-n or nPPI, the PMA shall meet the electrical and timing specifications at the service interface as specified in Annex 83A, Annex 83B, Annex 83D, Annex 83E, or Annex 86A as appropriate.

83.5.3 Skew and Skew Variation

Change 83.5.3.a (as inserted by IEEE Std 802.3bj-201x) as follows:

83.5.3.a Skew generation toward SP0

In an implementation with one or more physically instantiated CAUI-n interfaces, the PMA that sends data in the transmit direction toward the CAUI-n that is closest to the RS-FEC (SP0 in Figure 80–5a) shall pro-

duce no more than 29 ns of Skew between PCSLs toward the CAUI-n, and no more than 200 ps of Skew Variation.

Change 83.5.3.1, 83.5.3.2 and 83.5.3.3 as follows:

83.5.3.1 Skew generation toward SP1

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, the PMA that sends data in the transmit direction toward the XLAUI/CAUI-n that is closest to the PMD (SP1 in Figure 80–4 and Figure 80–5) shall produce no more than 29 ns of Skew between PCSLs toward the XLAUI/CAUI-n, and no more than 200 ps of Skew Variation.

83.5.3.2 Skew tolerance at SP1

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the XLAUI/CAUI-n (SP1 in Figure 80–4 and Figure 80–5) shall tolerate the maximum amount of Skew Variation allowed at SP1 (200 ps) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

83.5.3.3 Skew generation toward SP2

In an implementation with a physically instantiated PMD service interface, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 400 ps of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 80–4 and Figure 80–5). If there is a physically instantiated XLAUI/CAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 200 ps of Skew Variation.

Change 83.5.3.5 and 83.5.3.6 as follows:

83.5.3.5 Skew generation at SP6

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, at SP6 (the receive direction of the XLAUI/CAUI-n closest to the PCS), the PMA or group of PMAs between the PMD and the XLAUI/CAUI-n closest to the PCS shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the XLAUI/CAUI-n in the Rx direction. If there is a physically instantiated PMD service interface as well, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

83.5.3.6 Skew tolerance at SP6

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, the PMA between the XLAUI/CAUI-n closest to the PCS and the PCS shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of PCSLs on lanes sent in the receive direction towards the PCS.

Change 83.5.3.7 (as inserted by IEEE Std 802.3bj-201x) as follows:

83.5.3.7 Skew generation towards SP7

In an implementation with one or more physically instantiated CAUI-n interfaces and RS-FEC, at SP7 (the receive direction of the CAUI-n closest to the PCS), the PMA or group of PMAs between the RS-FEC and

the CAUI-n closest to the PCS shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the CAUI-n in the Rx direction.

Change 83.5.6 as follows:

83.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA, or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

- Annex 83A, which specifies the XLAUI/CAUI-10 interface for chip-to-chip applications.
- Annex 83B, which specifies the XLAUI/CAUI-10 interface for chip-to-module applications.
- Annex 83D, which specifies the CAUI-4 interface for chip-to-chip applications.
- Annex 83E, which specifies the CAUI-4 interface for chip-to-module applications.
- 86.2, which specifies the PMD service interface for 40GBASE-SR4 and 100GBASE-SR10 PMDs.
- 87.2, which specifies the PMD service interface for 40GBASE-LR4 and 40GBASE-ER4 PMDs.
- Annex 86A, which specifies the Parallel Physical Interface (XLPPI and CPPI), an optional physical instantiation of the PMD service interface for 40GBASE-SR4, 40GBASE-LR4, and 100GBASE-SR10 PMDs.

83.5.10 PMA test patterns (optional)

Change the first and last paragraphs of 83.5.10 as follows:

Where the output lanes of the PMA appear on a physically instantiated interface XLAUI/CAUI-n or the PMD service interface (whether or not it is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external testing equipment.

Transmit square wave test-pattern mode optionally applies to each lane of the Tx direction PMA towards a physically instantiated XLAUI/CAUI-n or towards the PMD service interface whether or not it is physically instantiated. The ability to perform this function is indicated by the Square_wave_ability status variable. If a Clause 45 MDIO is implemented, the Square_wave_ability status variable is accessible through the Square wave test ability bit 1.1500.12 (see 45.2.1.99). If implemented, the transmit square wave test-pattern mode is enabled by control variables Square_wave_enable_0 through Square_wave_enable_9. If a Clause 45 MDIO is implemented, these control variables are accessible through the square wave testing control and status register bits 1.1510.0 through 1.1510.9 (limited to the number of lanes of the service interface below the PMA, see 45.2.1.101). When enabled, the PMA shall generate a square wave test pattern (8 ones followed by 8 zeros) on the square wave enabled lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. Lanes for which square wave is not enabled will transmit normal data resulting from the bit multiplexing operations described in 83.5.2 or test patterns as determined by other registers. When transmit square wave test pattern is disabled for all lanes, the PMA will perform normal operation performing bit multiplexing as described in 83.5.2 or transmit test patterns as determined by other registers.

Change the text of 83.5.11 (as inserted by IEEE Std 802.3bj-201x) as follows:

83.5.11 Energy Efficient Ethernet

When the optional Energy Efficient Ethernet (EEE) deep sleep capability is supported and the PMA service interface is physically instantiated as XLAUI or CAUI-n the additional functions listed in this subclause are required. These functions enable the communication of service interface parameters that are essential to the

operation of the EEE deep sleep capability. The timing parameters for EEE operation are shown in Table 83–1a.

83.5.11.3 Additional transmit functions in the Tx direction

Change the second and third paragraphs of 83.5.11.3 (as inserted by IEEE Std 802.3bj-201x) as follows:

If XLAUI or CAUI-n is permitted to shut down (see 83.3), the variable aui_tx_mode shall be assigned the current value of tx_mode with the following exception. When tx_mode transitions from DATA to QUIET, the value of aui_tx_mode is held at DATA and the timer pma_quiet_timer (T_{pq}) is started. If tx_mode is QUIET when the timer expires, then aui_tx_mode is set to QUIET. If tx_mode is set to a value other than QUIET before the timer expires, then aui_tx_mode is set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_tx_mode shall be assigned the value DATA.

Change 83.5.11.4 (as inserted by IEEE Std 802.3bj-201x) as follows:

83.5.11.4 Additional receive functions in the Tx direction

For a PMA that is separated from the PCS by XLAUI or CAUI-n, the value of tx_mode shall be assigned as follows: If the PMA quiet signal is detected, the value of tx_mode is set to QUIET. If the PMA alert signal is detected, the value of tx_mode is set to ALERT. Otherwise, the value of tx_mode is DATA.

If XLAUI or CAUI-n is permitted to shut down (see 83.3), then the variable aui_rx_mode shall be assigned as follows: The variable aui_rx_mode is initialized to DATA upon PMA power on or reset. When the PMA quiet signal is detected, the timer hold_off_timer (T_{ho}) is started. If the PMA alert signal is not detected before the timer expires, then aui_rx_mode is set to QUIET and SIGNAL_DETECT is set to FAIL. While aui_rx_mode is QUIET, it shall be set to DATA when SIGNAL_DETECT transitions from FAIL to OK. The value of tx_mode is inferred to be ALERT and the timer alert_timer (T_a) started upon a transition of aui_rx_mode from QUIET to DATA. The value of ALERT shall be held until alert_timer expires after which the value of tx_mode shall be set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_rx_mode shall be assigned the value DATA.

PMA functions in the Tx direction may be disabled in order to conserve energy while aui_rx_mode is QUIET.

83.5.11.5 Additional transmit functions in the Rx direction

Change the first, third and fourth paragraphs of 83.5.11.5 (as inserted by IEEE Std 802.3bj-201x) as follows:

For a PMA that is separated from the PCS by XLAUI or CAUI-n, the value of rx_mode shall be assigned as follows. The value of rx_mode is initialized to DATA upon PMA power on or reset. When the PMA quiet signal is detected, the timer hold_off_timer (T_{ho}) is started. If the PMA alert signal is not detected before the timer expires, then rx_mode is set to QUIET. While rx_mode is QUIET, it shall be set to DATA when the PMA alert signal is detected or energy_detect (or SIGNAL_OK) transitions from false to true.

If XLAUI or CAUI-n is permitted to shut down (see 83.3), the variable aui_tx_mode shall be assigned the current value of rx_tx_mode with the following exception. When rx_tx_mode transitions from DATA to QUIET, the value of aui_tx_mode is held at DATA and the timer pma_quiet_timer (T_{pq}) is started. If rx_tx_mode is QUIET when the timer expires, then aui_tx_mode is set to QUIET. If rx_tx_mode is set to a value other than QUIET before the timer expires, then aui_tx_mode is set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_tx_mode shall be assigned the value DATA.

83.5.11.6 Additional receive functions in the Rx direction

Change the first, third and fourth paragraphs of 83.5.11.6 (as inserted by IEEE Std 802.3bj-201x) as follows:

For a PMA that is separated from the PMD by XLAUI or CAUI-n, the value of energy_detect shall be assigned as follows. The value of energy_detect is initialized to true upon PMA power on or reset. When the value of rx_mode is set to QUIET, the value of energy_detect is set to false. The value of energy_detect is set to true when the PMA alert signal is detected or SIGNAL_DETECT transitions from FAIL to OK.

If XLAUI or CAUI-n is permitted to shut down (see 83.3), then the variable aui_rx_mode shall be assigned as follows. The variable aui_rx_mode is initialized to DATA upon PMA power on or reset. When the PMA quiet signal is detected, the timer hold_off_timer (T_{ho}) is started. If the PMA alert signal is not detected before the timer expires, then aui_rx_mode is set to QUIET. While aui_rx_mode is QUIET, it shall be set to DATA when SIGNAL_DETECT transitions from FAIL to OK. The value of tx_mode is assigned to be ALERT and the timer alert_timer (T_a) started upon a transition of aui_rx_mode from QUIET to DATA. The value of ALERT shall be held until alert_timer expires after which the value of tx_mode shall be set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_rx_mode shall be assigned the value DATA.

83.7 Protocol implementation conformance statement (PICS) proforma for Clause 83, Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R[1]

83.7.3 Major capabilities/options

Change items *USP1SP6, *DSP1SP6, UNAUI, and DNAUI as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*USP1SP6	Physically instantiated XLAUI or CAUI-n above (toward PCS)	83.5.3		O	Yes [ ] No [ ]
*DSP1SP6	Physically instantiated XLAUI or CAUI-n below (toward PMD)	83.5.3		O	Yes [ ] No [ ]
UNAUI	Electrical and timing requirements of Annex 83A or Annex 83B or Annex 83D or Annex 83E as appropriate met by upstream XLAUI/CAUI-n	83.5.1, 83.5.5		USP1SP6: M	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
DNAUI	Electrical and timing requirements of Annex 83A or Annex 83B or Annex 83D or Annex 83E as appropriate met by downstream XLAUI/CAUI-n	83.5.1, 83.5.5		DSP1SP6: M	Yes [ ] No [ ]

83.7.4 Test patterns

Change items *JTP1 and *JTP2 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*JTP1	Physically Instantiated XLAUI/CAUI-n between PMA and PMA client	83.5.10		O	Yes [ ] No [ ]
*JTP2	Physically Instantiated XLAUI/CAUI-n between PMA and sublayer below the PMA, or adjacent to PMD whether or not PMD service interface is physically instantiated as nPPI	83.5.10		O	Yes [ ] No [ ]

Change the title of 83.7.7 and items RXDS and TXDS (as inserted by IEEE Std 802.3bj-201x) as follows:

83.7.7 EEE deep sleep with XLAUI/CAUI-n

Item	Feature	Subclause	Value/Comment	Status	Support
RXDS	XLAUI/CAUI-n deep sleep Rx direction	83.5.11		LPI*USP1SP6:M or LPI*DSP1SP6:M	Yes [ ] No [ ]
TXDS	XLAUI/CAUI-n deep sleep Tx direction	83.5.11		LPI*USP1SP6:M or LPI*DSP1SP6:M	Yes [ ] No [ ]

85. Physical Medium Dependent sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10

85.1 Overview

Change the row for CAUI and insert a new row for CAUI-4 immediately below the changed row in Table 85-1 as follows:

Table 85–1—Physical Layer clauses associated with the 40GBASE-CR4 and 100GBASE-CR10 PMDs

Associated clause	40GBASE-CR4	100GBASE-CR10
83A—CAUI-10	Not applicable	Optional
83D—CAUI-4	Not applicable	Optional

85.3 PCS requirements for Auto-Negotiation (AN) service interface

Change the last paragraph of 85.3 (as inserted by IEEE Std 802.3bj-201x) as follows:

The 40GBASE-CR4 PHY may be extended using XLAUI a physical instantiation of the inter-sublayer service interface between devices. Similarly, the 100GBASE-CR10 PHY may be extended using CAUI-n. If XLAUI or CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

85.13 Protocol implementation conformance statement (PICS) proforma for Clause 85, Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10

85.13.3 Major capabilities/options

Change item CAUI and insert a new row for CAUI-4 immediately below it as follows:

Item[a]	Feature	Subclause	Value/Comment	Status	Support
CAUI-10	CAUI-10	85.1		O	Yes [ ] No [ ]
CAUI-4	CAUI-4	85.1		O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

86. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE–SR4 and 100GBASE–SR10

86.1 Overview

Change Table 86-1 as follows:

Table 86–1—Physical Layer clauses associated with the 40GBASE-SR4 and 100GBASE-SR10 PMDs

Associated clause	40GBASE–SR4	100GBASE–SR10
81—RS	Required	Required
81—XLGMII[a]	Optional	Not applicable
81—CGMII[a]	Not applicable	Optional
82—PCS for 40GBASE-R	Required	Not applicable
82—PCS for 100GBASE-R	Not applicable	Required
83—PMA for 40GBASE-R4	Required	Not applicable
83—PMA for 100GBASE-R10	Not applicable	Required
83A—XLAUI[b]	Optional	Not applicable
83A—CAUI-10[b]	Not applicable	Optional
83B—Chip-to-module XLAUI[b]	Optional	Not applicable
83B—Chip-to-module CAUI-10[b]	Not applicable	Optional
83D—CAUI-4	Not applicable	Optional
83E—Chip-to-module CAUI-4	Not applicable	Optional
86A—XLPPI	Optional	Not applicable
86A—CPPI	Not applicable	Optional
78—Energy Efficient Ethernet	Optional	Optional

[a] XLGMII and CGMII are optional interfaces. However, if the appropriate interface is not implemented, a conforming implementation must behave functionally as though the RS, and XLGMII or CGMII, were present.
[b] If XLAUI or CAUI-n is present, there is at least a PMA between the XLAUI or CAUI-n and the PMD.

Insert the following at the end of 86.1:

40GBASE-SR4 and 100GBASE-SR10 PHYs with the optional Energy Efficient Ethernet (EEE) capability may enter the fast wake Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

86.8 Definitions of optical and dual-use parameters and measurement methods

86.8.4 Optical parameter definitions

86.8.4.7 Stressed receiver sensitivity

Change 86.8.4.7 item h) as follows:

h) Where nPPI or XLAUI/CAUI-n is exposed, a PMD receiver is considered compliant if it meets the module electrical output specifications at TP4 given in Table 86A–3 for nPPI, or the requirements in Table 83B–3 for XLAUI/CAUI-10, or the requirements in Table 83E–3 for CAUI-4.

Change the title of Clause 87 as follows:

87. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE–LR4 and 40GBASE–ER4

Change 87.1 (including Figure 87-1) as follows:

87.1 Overview

This clause specifies the 40GBASE–LR4 PMD and the 40GBASE–ER4 PMD together with the single-mode fiber medium. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 87–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 87–1—Physical Layer clauses associated with the 40GBASE-LR4 and 40GBASE-ER4 PMDs

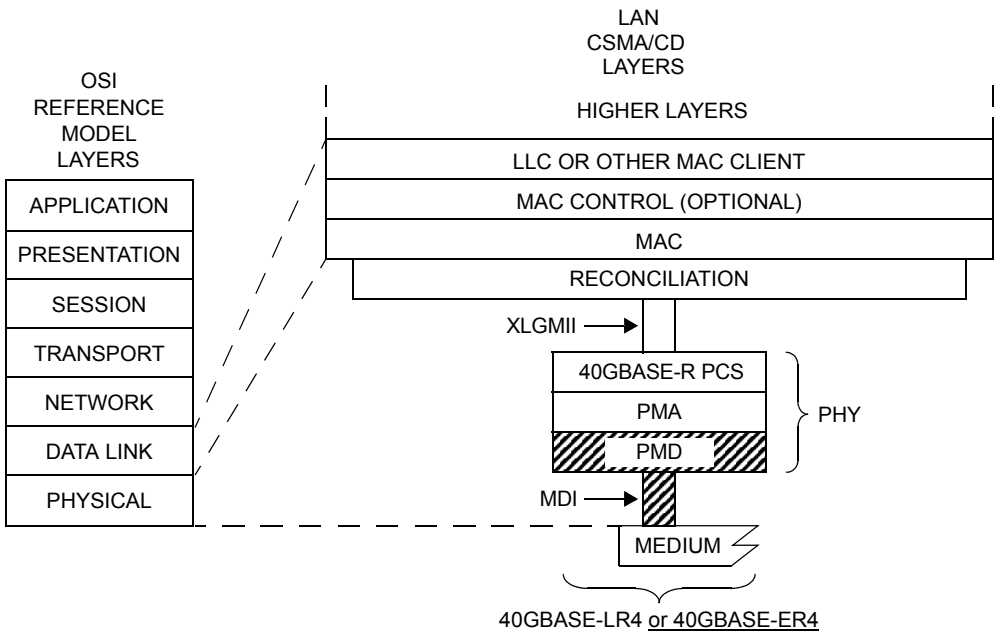
Associated clause	40GBASE–LR4	40GBASE–ER4
81—RS	Required	Required
81—XLGMII[a]	Optional	Optional
82—PCS for 40GBASE-R	Required	Required
83—PMA for 40GBASE-R	Required	Required
83A—XLAUI	Optional	Optional
83B—Chip-to-module XLAUI	Optional	Optional
86A—XLPPI	Optional	Not applicable
78—Energy Efficient Ethernet	Optional	Optional

[a]The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation must behave functionally as though the RS and XLGMII were present.

Figure 87–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

40GBASE-LR4 and 40GBASE-ER4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Change the first and fourth paragraphs of 87.2 as follows:



LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

LR = PMD FOR SINGLE-MODE FIBER — 10 km
ER = PMD FOR SINGLE-MODE FIBER — 40 km

Figure 87–1—40GBASE-LR4 and 40GBASE-ER4 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 CSMA/CD LAN model

87.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 40GBASE-LR4 and 40GBASE-ER4 PMDs. The service interfaces for ~~this~~ these PMDs are ~~is~~ described in an abstract manner and do~~es~~ not imply any particular implementation, although an optional implementation of the PMD service interface, the 40 Gb/s Parallel Physical Interface (XLPPI), is specified in Annex 86A. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 40GBASE-LR4 and 40GBASE-ER4 PMDs have ~~has~~ four parallel bit streams, hence i = 0 to 3.

87.3 Delay and Skew

Change 87.3.1 as follows:

87.3.1 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 40GBASE-LR4 or 40GBASE-ER4 PMD including 2 m of fiber in one direction shall be no more than 1024 bit times (2

pause_quanta or 25.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

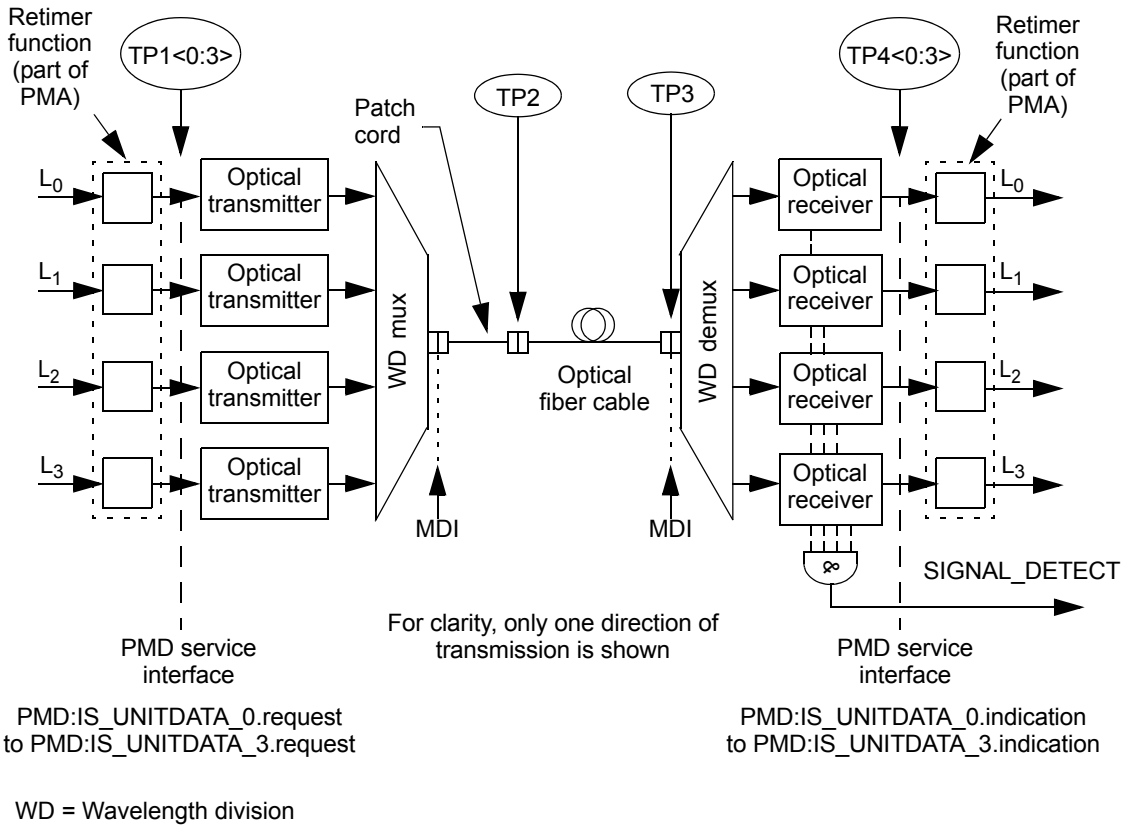
Change 87.5 as follows:

87.5 PMD functional specifications

The 40GBASE–LR4 and 40GBASE–ER4 PMDs performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

87.5.1 PMD block diagram

Change the title of Figure 87-2 as follows:



NOTE—Specification of the retimer function is beyond the scope of this standard.

Figure 87–2—Block diagram for 40GBASE–LR4 and 40GBASE–ER4 transmit/receive paths

Change 87.6 as follows (make no change to Table 87-2):

87.6 Wavelength-division-multiplexed lane assignments

The wavelength range for each lane of the 40GBASE–LR4 and 40GBASE–ER4 PMDs is defined in Table 87–5. The center wavelengths are members of the CWDM wavelength grid defined in ITU-T G.694.2 and are spaced at 20 nm.

NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement.

Change 87.7 (including the title) as follows:

87.7 PMD to MDI optical specifications for 40GBASE–LR4 and 40GBASE–ER4

The operating ranges for the 40GBASE–LR4 and 40GBASE–ER4 PMDs are ~~is~~ defined in Table 87–6. A 40GBASE–LR4 or 40GBASE–ER4 compliant PMD operates on type B1.1, B1.3 or B6_a single-mode fibers according to the specifications defined in Table 87–14. A PMD that exceeds the required operating range while meeting all other optical specifications is considered compliant (e.g., a 40GBASE–LR4 PMD operating at 12.5 km meets the operating range requirement of 2 m to 10 km).

The 40GBASE-ER4 PMD interoperates with the 40GBASE–LR4 PMD provided that the channel requirements defined in 87.12 are met.

Table 87–6—40GBASE–LR4 and 40GBASE–ER4 operating ranges

PMD type	Required operating range
40GBASE–LR4	2 m to 10 km
40GBASE–ER4	2 m to 30 km
	2 m to 40 km[a]

[a]Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for B1.1, B1.3, or B6_a single-mode fiber.

Change 87.7.1 (including the title and Table 87-7) as follows:

87.7.1 40GBASE–LR4 and 40GBASE–ER4 transmitter optical specifications

The 40GBASE–LR4 transmitter shall meet the specifications defined in Table 87–7 per the definitions in 87.8. The 40GBASE–ER4 transmitter shall meet the specifications defined in Table 87–7 per the definitions in 87.8.

Table 87–7—40GBASE-LR4 and 40GBASE-ER4 transmit characteristics

Description	~~Value~~ 40GBASE-LR4	40GBASE-ER4	Unit
Signaling rate, each lane (range)	10.3125 ± 100 ppm		GBd
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	8.3	10.5	dBm
Average launch power, each lane (max)	2.3	4.5	dBm
Average launch power, each lane[a] (min)	–7	–2.7	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3.5	5	dBm
Optical Modulation Amplitude (OMA), each lane (min)[b]	–4	0.3	dBm
Difference in launch power between any two lanes (OMA) (max)	6.5	4.7	dB
Launch power in OMA minus TDP, each lane (min)	–4.8	–0.5	dBm
Transmitter and dispersion penalty (TDP), each lane (max)	2.6		dB
Average launch power of OFF transmitter, each lane (max)	–30		dBm
Extinction ratio (min)	3.5	5.5	dB
$RIN_{20}OMA$ (max)	–128		dB/Hz
Optical return loss tolerance (max)	20		dB
Transmitter reflectance[c] (max)	–12		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		

[a]Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDP < 0.8 dB, the OMA (min) must exceed this value.
[c]Transmitter reflectance is defined looking into the transmitter.

Change 87.7.2 (including the title and Table 87–8) as follows:

87.7.2 40GBASE–LR4 and 40GBASE–ER4 receive optical specifications

The 40GBASE–LR4 receiver shall meet the specifications defined in Table 87–8 per the definitions in 87.8.
The 40GBASE–ER4 receiver shall meet the specifications defined in Table 87–8 per the definitions in 87.8.

Table 87–8—40GBASE–LR4 and 40GBASE–ER4 receive characteristics

Description	~~Value~~ 40GBASE-LR4	40GBASE-ER4	Unit
Signaling rate, each lane (range)	10.3125 ± 100 ppm		GBd
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5		nm
Damage threshold[a] (min)	3.3	3.8	dBm
Average receive power, each lane (max)	2.3	–4.5	dBm
Average receive power, each lane[b] (min)	–13.7	–21.2	dBm
Receive power, each lane (OMA) (max)	3.5	–4	dBm
Difference in receive power between any two lanes (OMA) (max)	7.5	7	dB
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA), each lane[c] (max)	–11.5	–19	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane (max)	12.3		GHz
Stressed receiver sensitivity (OMA), each lane[d] (max)	–9.6	–16.8	dBm
Conditions of stressed receiver sensitivity test:			
Vertical eye closure penalty,[e] each lane	1.9	2.2	dB
Stressed eye J2 Jitter,[e] each lane	0.3		UI
Stressed eye J9 Jitter,[e] each lane	0.47		UI

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA), each lane (max) is informative.
[d]Measured with conformance test signal at TP3 (see 87.8.11) for BER = 10^{-12}.
[e]Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Change 87.7.3 (including the title and Table 87–9) as follows:

87.7.3 40GBASE–LR4 and 40GBASE–ER4 illustrative link power budgets

~~An illustrative~~ Illustrative power budgets and penalties for 40GBASE–LR4 and 40GBASE–ER4 channels are shown in Table 87–9.

Table 87–9—40GBASE–LR4 and 40GBASE–ER4 illustrative link power budgets

Parameter	~~Value~~ 40GBASE-LR4	40GBASE-ER4		Unit
Power budget (for max TDP)	9.3	21.1		dB
Operating distance	10	30	40[a]	km
Channel insertion loss[~~b~~]	6.7[b]	16.5[b]	18.5[a]	dB
Maximum discrete reflectance	–26	–26		dB
Allocation for penalties[c] (for max TDP)	2.6	2.6		dB
Additional insertion loss allowed	0	2	0	dB

[a]Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than the worst case for B1.1, B1.3, or B6_a single-mode cabled optical fiber
[b]The channel insertion loss is calculated using the maximum distance specified in Table 87–6 and cabled optical fiber attenuation of 0.47 dB/km at 1264.5 nm plus an allocation for connection and splice loss given in 87.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

87.8 Definition of optical parameters and measurement methods

87.8.1 Test patterns for optical parameters

Change Table 87–11 as follows:

Table 87–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.3
Side mode suppression ratio	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	—
Average optical power	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.4
Optical modulation amplitude (OMA)	Square wave or 4	87.8.5
Transmitter and dispersion penalty (TDP)	3 or 5	87.8.6
Extinction ratio	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.7

Table 87–11—Test-pattern definitions and related subclauses *(continued)*

Parameter	Pattern	Related subclause
$RIN_{20}OMA$	Square wave or 4	87.8.8
Transmitter optical waveform	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.9
Stressed receiver sensitivity	3 or 5	87.8.11
Calibration of OMA for receiver tests	Square wave or 4	87.8.11
Vertical eye closure penalty calibration	3 or 5	87.8.11
Receiver 3 dB electrical upper cutoff frequency	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.12

Change 87.8.4 as follows:

87.8.4 Average optical power

The average optical power of each lane shall be within the limits given in Table 87–7 ~~for 40GBASE–LR4~~ if measured using the methods given in IEC 61280–1–1, with the sum of the optical power from all of the lanes not under test below –30 dBm, per the test setup in Figure 53–6.

Change 87.8.6 as follows:

87.8.6 Transmitter and dispersion penalty

Transmitter and dispersion penalty (TDP) shall be as defined in 52.9.10 with the exception that each optical lane is tested individually using an optical filter to separate the lane under test from the others. The measurement procedure for 40GBASE–LR4 and 40GBASE–ER4 is detailed in 87.8.6.1 to 87.8.6.4.

The optical filter passband ripple shall be limited to 0.5 dB peak-to-peak and the isolation is chosen such that the ratio of the power in the lane being measured to the sum of the powers of all of the other lanes is greater than 20 dB (see ITU-T G.959.1 Annex B). The lanes not under test shall be operating with PRBS31 or valid 40GBASE-~~LR4~~R bit streams.

Change 87.8.6.2 as follows:

87.8.6.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 87–12.

A 40GBASE–LR4 or 40GBASE–ER4 transmitter is to be compliant with a total dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion” columns specified in Table 87–12 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

Table 87–12—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]
	Minimum	Maximum		
40GBASE–LR4	$0.2325 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.2325 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	20 dB
40GBASE–ER4	$0.93 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.93 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	20 dB

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 10 km for 40GBASE–LR4 and 40 km for 40GBASE–ER4.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The optical return loss is applied at TP2.

The channel provides an optical return loss specified in Table 87–12. The state of polarization of the back reflection is adjusted to create the greatest RIN.

Change 87.8.7 as follows:

87.8.7 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 87–7 ~~for 40GBASE–LR4~~ if measured using the methods specified in IEC 61280–2–2, with the sum of the optical power from all of the lanes not under test below –30 dBm. The extinction ratio is measured using the test pattern defined in Table 87–11.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 87–11).

Change the first paragraph of 87.8.11 as follows:

87.8.11 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 87–8 ~~for 40GBASE–LR4~~ if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2. The BER is required to be met for the lane under test on its own.

Change the first paragraph of 87.8.11.5 as follows:

87.8.11.5 Stressed receiver conformance test procedure for WDM conformance testing

The receiver tests requiring the TP3 conformance test signal are performed on a per lane basis. For each lane, the stressed receiver sensitivity is defined with the transmit section in operation on all four lanes and with the receive lanes not under test also in operation. Pattern 3 or Pattern 5, or a valid 40GBASE–R signal is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal. All test sources are modulated simultaneously, using valid 40GBASE-~~LR4~~R signals. The transmitter of the transceiver under test is operating with test patterns as defined in Table 87–11.

87.9 Safety, installation, environment, and labeling

Change the first paragraph of 87.9.2 as follows:

87.9.2 Laser safety

40GBASE–LR4 and 40GBASE–ER4 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825–1 and IEC 60825–2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Change the first paragraph of 87.9.4 as follows:

87.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 40GBASE–LR4 or 40GBASE–ER4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

Change 87.9.4.1 as follows:

87.9.4.1 Electromagnetic emission

A system integrating a 40GBASE–LR4 or 40GBASE–ER4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

87.10 Fiber optic cabling model

Change Table 87-14 as follows:

Table 87–14—Fiber optic cabling (channel) characteristics ~~for 40GBASE–LR4~~

Description	~~Value~~ 40GBASE-LR4	40GBASE-ER4		Unit
Operating distance (max)	10	30	40	km
Channel insertion loss[a, b] (max)	6.7	18.5		dB
Channel insertion loss (min)	0	9		dB
Positive dispersion[b] (max)	33.5	100.5	134	ps/nm
Negative dispersion[b] (min)	–59.5	–178.5	–238	ps/nm
DGD_max[c]	10	12		ps
Optical return loss (min)	21	21		dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1264.5 nm to 1337.5 nm.
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system must tolerate.

Change 87.11 as follows:

87.11 Characteristics of the fiber optic cabling (channel)

The 40GBASE–LR4 and 40GBASE–ER4 fiber optic cabling shall meet the specifications defined in Table 87–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

87.11.1 Optical fiber cable

Change Table 87-15 as follows:

Table 87–15—Optical fiber and cable characteristics ~~for 40GBASE–LR4~~

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.47[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.47 dB/km at 1264.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation at 10 km for 40GBASE–LR4 or 40 km for 40GBASE–ER4.

Change the first paragraph of 87.11.3 as follows:

87.11.3 Medium Dependent Interface (MDI) requirements

The 40GBASE–LR4 or 40GBASE–ER4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 87–6). Examples of an MDI include the following:

Insert a new subclause 87.12 as follows:

87.12 Requirements for interoperation between 40GBASE-LR4 and 40GBASE-ER4

The 40GBASE-LR4 and 40GBASE-ER4 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 40GBASE-LR4 given in Table 87–14 are met, with the exception of the maximum and minimum channel insertion loss values which are given in Table 87–16 for the two link directions separately.

Table 87–16—Channel insertion loss requirements for interoperation

Direction	Min loss	Max loss	Unit
40GBASE-LR4 Transmitter to 40GBASE-ER4 Receiver	7.5	14.2	dB
40GBASE-ER4 Transmitter to 40GBASE-LR4 Receiver	2.2	11	dB

Change the title of 87.12 (re-numbered to 87.13 by the insertion of 87.12 above) as follows:

87.13 Protocol implementation conformance statement (PICS) proforma for Clause 87, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4[2]

Change the first paragraph of 87.12.1 (re-numbered to 87.13.1 by the insertion of 87.12 above) as follows:

87.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 87, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4, shall complete the following protocol implementation conformance statement (PICS) proforma.

87.13.2 Identification

87.13.2.2 Protocol summary

Change Identification of protocol standard as follows:

IEEE Std 802.3-2012, Clause 87, Physical Medium Dependent sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4

87.13.3 Major capabilities/options

Change item LR4 and insert item ER4 after item LR4 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*LR4	40GBASE-LR4 PMD	87.7	Device supports requirements for 40GBASE-LR4 PHY	O.1	Yes [ ] No [ ]
*ER4	40GBASE-ER4 PMD	87.7	Device supports requirements for 40GBASE-ER4 PHY	O.1	Yes [ ] No [ ]

Change title of 87.12.4 (re-numbered to 87.13.4 by the insertion of 87.12 above) as follows:

87.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Change 87.12.4.3 (re-numbered to 87.13.4.3 by the insertion of 87.12 above) as follows:

87.13.4.3 PMD to MDI optical specifications for 40GBASE-LR4

Item	Feature	Subclause	Value/Comment	Status	Support
XLLR1	Transmitter meets specifications in Table 87–7	87.7.1	Per definitions in 87.8	LR4:M	Yes [ ] N/A [ ]
XLLR2	Receiver meets specifications in Table 87–8	87.7.2	Per definitions in 87.8	LR4:M	Yes [ ] N/A [ ]

Insert 87.13.4.3a after 87.12.4.3 (re-numbered to 87.13.4.3 by the insertion of 87.12 above) as follows:

87.13.4.3a PMD to MDI optical specifications for 40GBASE-ER4

Item	Feature	Subclause	Value/Comment	Status	Support
XLER1	Transmitter meets specifications in Table 87–7	87.7.1	Per definitions in 87.8	ER4:M	Yes [ ] N/A [ ]
XLER2	Receiver meets specifications in Table 87–8	87.7.2	Per definitions in 87.8	ER4:M	Yes [ ] N/A [ ]

88. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE–LR4 and 100GBASE–ER4

88.1 Overview

Change Table 88-1 as follows:

Table 88–1—Physical Layer clauses associated with the 100GBASE-LR4 and 100GBASE-ER4 PMDs

Associated clause	100GBASE–LR4	100GBASE–ER4
81—RS	Required	Required
81—CGMII[a]	Optional	Optional
82—PCS for 100GBASE-R	Required	Required
83—PMA for 100GBASE-R	Required	Required
83A—CAUI-10	Optional	Optional
83B—Chip-to-module CAUI-10	Optional	Optional
83D—CAUI-4	Optional	Optional
83E—Chip-to-module CAUI-4	Optional	Optional
78—Energy Efficient Ethernet	Optional	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.

Insert the following at the end of 88.1:

100GBASE-LR4 and 100GBASE-ER4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

89. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-FR

89.1 Overview

Change Table 89-1 as follows:

Table 89–1—Physical Layer clauses associated with the 40GBASE-FR PMD

Associated clause	40GBASE-FR
81—RS	Required
81—XLGMII[a]	Optional
82—PCS for 40GBASE-R	Required
83—PMA for 40GBASE-R	Required
83A—XLAUI	Optional
83B—Chip-to-module XLAUI	Optional
78—Energy Efficient Ethernet	Optional

[a]The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation must behave functionally as though the RS and XLGMII were present.

Insert the following at the end of 89.1:

40GBASE-FR PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.2 FEC service interface

Change the second paragraph of 91.2 (as introduced by IEEE Std 802.3bj-201x) as follows:

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (refer to Annex 83A or Annex 83D) in which case a PMA is the client of the FEC service interface.

91.3 PMA compatibility

Change the second paragraph of 91.3 as follows:

In addition, all PMA service interfaces between the RS-FEC sublayer and the PMD sublayer are required to consist of four or fewer upstream lanes and four or fewer downstream lanes. A consequence of this constraint is that a physical instantiation of the 10-lane PMA service interface (CAUI-10) may not be used below the RS-FEC sublayer.

91.5 Functions within the RS-FEC sublayer

91.5.2 Transmit function

91.5.2.7 Reed-Solomon encoder

Change the second paragraph of 91.5.2.7 as follows:

When used to form a 100GBASE-CR4, ~~or~~ 100GBASE-KR4, or 100GBASE-SR4 PHY, the RS-FEC sublayer shall implement RS(528,514). When used to form a 100GBASE-KP4 PHY, the RS-FEC sublayer shall implement RS(544,514). Each k-symbol message corresponds to twenty 257-bit blocks produced by the transcoder. Each code is based on the generating polynomial given by Equation (91–1)

91.5.3 Receive function

91.5.3.3 Reed-Solomon decoder

Change the second, third and last paragraphs of 91.5.3.3 as follows:

When used to form a 100GBASE-CR4, ~~or~~ 100GBASE-KR4, or 100GBASE-SR4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=7 symbol errors in a codeword. When used to form a 100GBASE-KP4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_correction_ability variable (see 91.6.3). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 91.6.1). This option shall not be used when the RS-FEC sublayer is used to form part of a 100GBASE-SR4 PHY.

When the RS-FEC sublayer is used to form a 100GBASE-CR4, ~~or~~ 100GBASE-KR4, or 100GBASE-SR4 PHY, the symbol error threshold shall be K=417. When the RS-FEC sublayer used to form a 100GBASE-KP4 PHY, the symbol error threshold shall be K=6380.

91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs[3]

Add a row for item *SR4 in the table in 91.7.3 immediately below the row for *KP4 as follows:

91.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*SR4	100GBASE-SR4		Used to form complete 100GBASE-SR4 PHY	O	Yes [ ] No [ ]

91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sub-layer for 100GBASE-R PHYs

Change item TF10 in the table in 91.7.4.1 as follows:

91.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF10	Reed-Solomon encoder for 100GBASE-CR4 or 100GBASE-KR4 or 100GBASE-SR4	91.5.2.7	RS(528,514)	KR4:M or SR4:M	Yes [ ] N/A [ ]

[3]*Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Insert new rows for items RF4a and RF4b and change item RF9 in the table in 91.7.4.2 as follows:

91.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF4a	Reed-Solomon decoder for 100GBASE-SR4	91.5.3.3	Corrects any combination of up to *t*=7 symbol errors in a codeword	SR4:M	Yes [ ] N/A [ ]
RF4b	Error correction bypass for 100GBASE-SR4	91.5.3.3	Error correction is not bypassed	SR4:M	Yes [ ] N/A [ ]
RF9	Symbol error threshold for 100GBASE-CR4, ~~and~~ 100GBASE-KR4, and 100GBASE-SR4	91.5.3.3	*K*=417	BEI* KR4:M or BEI*SR 4:M	Yes [ ] N/A [ ]

92. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4

92.1 Overview

Change the row for CAUI and insert a new row for CAUI-4 immediately below the changed row in Table 92-1 as follows:

Table 92–1—Physical Layer clauses associated with the 100GBASE-CR4 PMD

Associated clause	100GBASE-CR4
83A—CAUI-10	Optional
83D—CAUI-4	Optional

92.3 PCS requirements for Auto-Negotiation (AN) service interface

Change the last paragraph of 92.3 as follows:

The 100GBASE-CR4 PHY may be extended using CAUI-n as a physical instantiation of the inter-sublayer service interface between devices. If CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

92.14 Protocol implementation conformance statement (PICS) proforma for Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4

92.14.3 Major capabilities/options

Change item CAUI and insert a new row for CAUI-4 immediately below it as follows:

Item[a]	Feature	Subclause	Value/Comment	Status	Support
CAUI-10	CAUI-10	92.1	Interface is supported	O	Yes [ ] No [ ]
CAUI-4	CAUI-4	92.1	Interface is supported	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

93. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4

93.1 Overview

Change the row for CAUI and insert a new row for CAUI-4 immediately below the changed row in Table 93-1 as follows:

Table 93–1—Physical Layer clauses associated with the 100GBASE-KR4 PMD

Associated clause	100GBASE-KR4
83A—CAUI-10	Optional
83D—CAUI-4	Optional

93.3 PCS requirements for Auto-Negotiation (AN) service interface

Change the last paragraph of 93.3 as follows:

The 100GBASE-KR4 PHY may be extended using CAUI-n as a physical instantiation of the inter-sublayer service interface between devices. If CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

93.11 Protocol implementation conformance statement (PICS) proforma for Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4

93.11.3 Major capabilities/options

Change item CAUI and insert a new row for CAUI-4 immediately below it as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
CAUI-10	CAUI-10	93.1	Interface is supported	O	Yes [ ] No [ ]
CAUI-4	CAUI-4	93.1	Interface is supported	O	Yes [ ] No [ ]

94. Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KP4

94.1 Overview

Change the row for CAUI and insert a new row for CAUI-4 immediately below the changed row in Table 94-1 as follows:

Table 94–1—Physical Layer clauses associated with the 100GBASE-KP4 PMD

Associated clause	100GBASE-KP4
83A—CAUI-10	Optional
83D—CAUI-4	Optional

94.3 Physical Medium Dependent (PMD) Sublayer

94.3.2 PCS requirements for Auto-Negotiation (AN) service interface

Change the last paragraph of 94.3.2 as follows:

The 100GBASE-KP4 PHY may be extended using CAUI-n as a physical instantiation of the inter-sublayer service interface between devices. If CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

94.6 Protocol implementation conformance statement (PICS) proforma for Clause 94, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KP4

94.6.3 Major capabilities/options

Change item CAUI and insert a new row for CAUI-4 immediately below it as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
CAUI-10	CAUI-10	94.1	Interface is supported	O	Yes [ ] No [ ]
CAUI-4	CAUI-4	94.1	Interface is supported	O	Yes [ ] No [ ]

Insert the new clauses and corresponding annexes as follows:

95. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4

95.1 Overview

This clause specifies the 100GBASE-SR4 PMD together with the multimode fiber medium. The PMD sublayer provides a point-to-point 100 Gb/s Ethernet link over four pairs of multimode fiber, up to at least 100 m. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 95–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 95–1—Physical Layer clauses associated with the 100GBASE-SR4 PMD

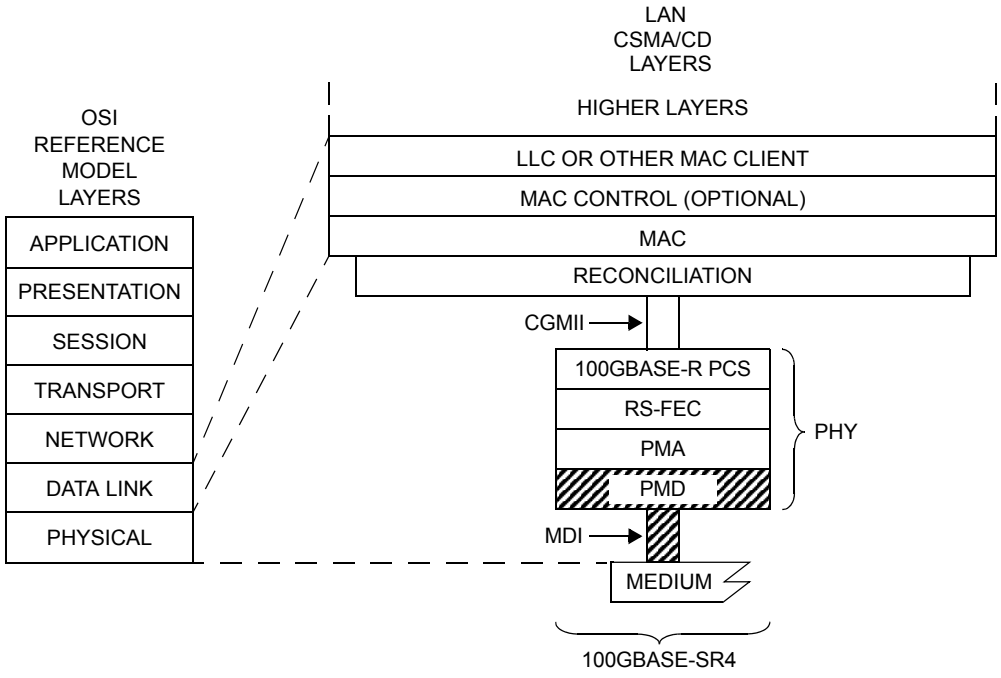
Associated clause	100GBASE-SR4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
83—PMA for 100GBASE-R	Required
91—RS-FEC[b]	Required
83A—CAUI-10	Optional
83B—Chip-to-module CAUI-10[c]	Optional
83D—CAUI-4	Optional
83E—Chip-to-module CAUI-4	Optional
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]The option to bypass the Clause 91 RS-FEC correction function may is not supported.
[c]This option requires the RS-FEC sublayer to be within the module. See 91.3.

Figure 95–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

100GBASE-SR4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.).



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
SR = PMD FOR MULTIMODE FIBER

Figure 95–1—100GBASE-SR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

95.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 5×10^{-5} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.210a) of less than 6.2×10^{-10} for 64-octet frames with minimum inter-packet gap when processed according to Clause 91.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum inter-packet gap when processed according to Clause 91.

95.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-SR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-SR4 PMD has four parallel bit streams, hence i = 0 to 3.

In the transmit direction, the PMA continuously sends four parallel bit streams to the PMD, one per lane, each at a nominal signaling rate of 25.78125 GBd. The PMD converts these streams of bits into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel bit streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service primitive defined in 80.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_bit parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 95.1.1.

95.3 Delay and Skew

95.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-SR4 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

95.3.2 Skew constraints

The Skew (relative delay) between the lanes must be kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP0 to SP7 shown in Figure 80–5a.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1 with the exception that the clock and data recovery units' high-frequency corner bandwidths are 10 MHz.

95.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 95–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 95–3.

Table 95–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0

Table 95–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0

95.5 PMD functional specifications

The 100GBASE-SR4 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

95.5.1 PMD block diagram

The PMD block diagram is shown in Figure 95–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 95.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 95.11.3). Unless specified otherwise, all receiver measurements and tests defined in 95.8 are made at TP3.

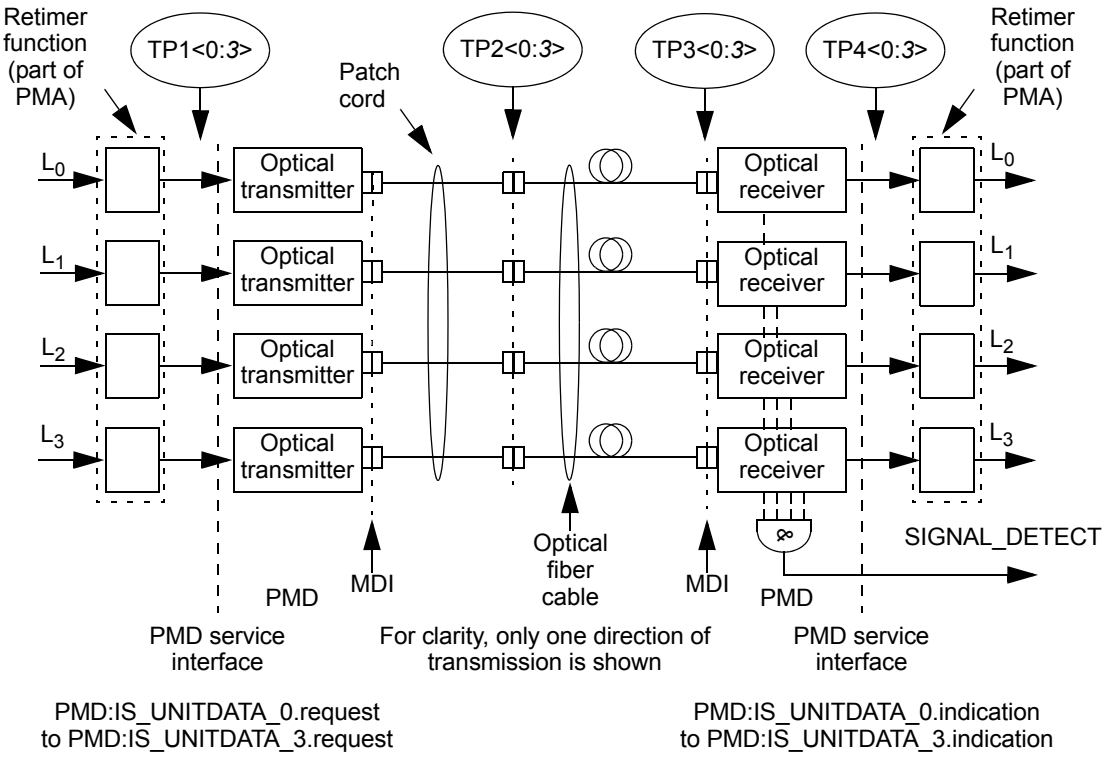


Figure 95–2—Block diagram for 100GBASE-SR4 transmit/receive paths

TP1<0:3> and TP4<0:3> are informative reference points that may be useful to implementors for testing components (these test points will not typically be accessible in an implemented system).

95.5.2 PMD transmit function

The PMD Transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signal streams. The four optical signal streams shall then be delivered to the MDI, which contains four parallel light paths for transmit, according to the transmit optical specifications in this clause. The higher optical power level in each signal stream shall correspond to tx_bit = one.

95.5.3 PMD receive function

The PMD Receive function shall convert the four parallel optical signal streams received from the MDI into separate bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal stream shall correspond to rx_bit = one.

95.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 95–4. The PMD receiver is not required to verify whether a compliant 100GBASE-SR4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 95–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 95–7) AND (compliant 100GBASE-SR4 signal input)]	OK
All other conditions	Unspecified

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

95.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 95–4.

95.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

95.5.7 PMD global transmit disable function (optional)

The PMD_global_transmit_disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 95–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable to one, turning off the optical transmitter in each lane.

95.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD_transmit_disable_*i* (where *i* represents the lane number in the range 0:3) function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 95–6.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the optical transmitter in each lane.

If the optional PMD_transmit_disable_*i* function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

95.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.1.

95.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

95.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

95.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 100GBASE-SR4. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the RS-FEC sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 95.11.3.1.

95.7 PMD to MDI optical specifications for 100GBASE-SR4

The operating range for the 100GBASE-SR4 PMD is defined in Table 95–5. A 100GBASE-SR4 compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3) or type A1a.3 (OM4), according to the specifications defined in Table 95–12. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-SR4 PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m).

Table 95–5—100GBASE-SR4 operating range

PMD type	Required operating range[a]
100GBASE-SR4	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4

[a]The RS-FEC correction function may not be bypassed for any operating distance.

95.7.1 100GBASE-SR4 transmitter optical specifications

Each lane of a 100GBASE-SR4 transmitter shall meet the specifications in Table 95–6 per the definitions in 95.8.

Table 95–6—100GBASE-SR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
RMS spectral width[a]	0.6	nm
Average launch power, each lane (max)	2.4	dBm
Average launch power, each lane (min)	–9.1	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Optical Modulation Amplitude (OMA), each lane (min)[b]	–7.1	dBm
Launch power in OMA minus TDP (min)	–8	dBm
Transmitter and dispersion penalty (TDP), each lane (max)	5	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio (min)	2	dB
Optical return loss tolerance (max)	12	dB
Encircled flux[c]	≥ 86% at 19 μm ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}	

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDP < 0.9 dB, the OMA (min) must exceed this value.
[c]If measured into type A1a.2 or type A1a.3 50 μm fiber in accordance with IEC 61280-1-4.

95.7.2 100GBASE-SR4 receive optical specifications

Each lane of a 100GBASE-SR4 receiver shall meet the specifications in Table 95–7 per the definitions in 95.8.

Table 95–7—100GBASE-SR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–11	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	–5.6	dBm
Conditions of stressed receiver sensitivity test:		
Vertical eye closure penalty (VECP),[d] lane under test	4.2	dB
Stressed eye J2 Jitter,[d] lane under test	0.41	UI
Stressed eye J4 Jitter,[d] lane under test	0.55	UI
OMA of each aggressor lane	3	dBm
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.
[d]Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

95.7.3 100GBASE-SR4 illustrative link power budget

An illustrative power budget and penalties for 100GBASE-SR4 channels are shown in Table 95–8.

95.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

Table 95–8—100GBASE-SR4 illustrative link power budget

Parameter	OM3	OM4	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700	MHz.km
Power budget (for max TDP)	8.2		dB
Operating distance	0.5 to 70	0.5 to 100	m
Channel insertion loss[b]	1.8	1.9	dB
Allocation for penalties[c] (for max TDP)	6.3		dB
Additional insertion loss allowed	0.1	0	dB

[a]per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 95–5 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 95.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

95.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 95–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 95–10 may be used to perform that test. As Pattern 3 is more demanding than Pattern 5 (which itself is the same or more demanding than other 100GBASE-R bit streams) an item that is compliant using Pattern 5 is considered compliant even if it does not meet the required limit using Pattern 3. The test patterns used in this clause are shown in Table 95–9.

Table 95–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5[a]	RS-FEC encoded scrambled idle	82.2.10[a]

[a]The pattern defined in 82.2.10 as encoded by Clause 91 RS-FEC for 100GBASE-SR4

95.8.1.1 Multi-lane testing considerations

TDP is defined for each lane, at the BER specified in 95.1.1 on that lane. Stressed receiver sensitivity is defined for an interface at the BER specified in 95.1.1. The interface BER is the average of the four BERs of the receive lanes when they are stressed.

Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (RS-FEC encoded scrambled idle) give the interface BER if all lanes are stressed at the same time.

Table 95–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 5 or valid 100GBASE-SR4 signal	95.8.2
Average optical power	3, 5 or valid 100GBASE-SR4 signal	95.8.3
Optical modulation amplitude (OMA)	Square wave or 4	95.8.4
Transmitter and dispersion penalty (TDP)	3 or 5	95.8.5
Extinction ratio	3, 5 or valid 100GBASE-SR4 signal	95.8.6
Transmitter optical waveform	3, 5 or valid 100GBASE-SR4 signal	95.8.7
Stressed receiver sensitivity	3 or 5	95.8.8
Vertical eye closure penalty calibration	3 or 5	87.8.11

If each lane is stressed in turn, the BER is diluted by the three unstressed lanes, and the BER for that stressed lane alone must be found, e.g., by multiplying by four if the unstressed lanes have low BER. To allow TDP measurement with Pattern 5, unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by copying the contents of the transmit lanes not under BER test to the error detector by other means. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA or VMA) for a particular situation is used, and for counter-propagating lanes, the minimum transition time is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane.

95.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 95–6 if measured per TIA/EIA-455-127-A or IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 95–10.

95.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 95–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 95–10.

95.8.4 Optical Modulation Amplitude (OMA)

OMA shall be within the limits given in Table 95–6 if measured as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern, with the exception that each optical lane is tested individually. See 95.8.1 for test pattern information.

95.8.5 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) shall be as defined for 10GBASE-S in 52.9.10 with the following exceptions:

a) Each optical lane is tested individually with all other lanes in operation.

b) The test pattern is as defined in Table 95–10

c) The transmitter is tested using an optical channel with an optical return loss of 12 dB.

d) The reference transmitter rise/fall times should be less than 12 ps at 20% to 80%, and should pass the eye mask test of 95.8.7. The reference transmitter optical waveform is measured for vertical eye closure penalty (VECP), as defined in Equation (52-4), but evaluated at ± 0.11 UI from the eye center, using a receiver with a fourth-order Bessel-Thomson filter response with a bandwidth of 12.6 GHz.

e) The reference receiver (including the effect of the decision circuit) has a fourth-order Bessel-Thomson filter response with a bandwidth of 12.6 GHz. The transversal filter of 52.9.10.3 is not used.

f) The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 10 MHz and a slope of 20 dB/decade.

g) The reference sensitivity S and the measurement P_DUT are both measured with the sampling instant displaced from the eye center by ± 0.11 UI. Because the reference sensitivity test is done with a restricted bandwidth receiver, a correction is required to calculate S. S is equal to the measured sensitivity minus the measured reference transmitter VECP from item d). For each of the two cases (early and late), if P_DUT(i) is larger than S(i), the TDP(i) for the transmitter under test is the difference between P_DUT(i) and S(i), i.e. TDP(i) = P_DUT(i) – S(i). Otherwise, TDP(i) = 0. The TDP is the larger of the two TDP(i).

h) The test setup illustrated in Figure 52-12 shows the reference method. Other measurement implementations may be used with suitable calibration.

i) TDP is defined for each lane, at the BER specified in 95.1.1 and is for the lane under test on its own. See 95.8.1.1 for multi-lane pattern considerations.

NOTE—Sampling instant offsets have to be calibrated because practical receivers and decision circuits have noise and timing impairments. One method of doing this is via a jitter bathtub method using a known low-jitter signal.

95.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 95–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using one of the test patterns specified for extinction ratio in Table 95–10.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 95–10).

95.8.7 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86-4 with the Transmitter eye mask coordinates in Table 95–6. The transmitter optical waveform of a port transmitting the test pattern specified in Table 95–10 shall meet

specifications according to the methods specified in 86.8.4.6.1 with the exception that the clock recovery unit's high-frequency corner bandwidth is 10 MHz. The filter nominal reference frequency f_r is 19.34 GHz and the filter tolerances are as specified for STM-64 in ITU-T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response.

95.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the method defined by 95.8.8.1 and 95.8.8.5, with the conformance test signal at TP3 as described in 95.8.8.2.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Pattern 3 or Pattern 5, or a valid 100GBASE-SR4 signal, is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal. The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.

95.8.8.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 95–3. The patterns used for the received compliance signal are specified in Table 95–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 95.8.8.2, and has sinusoidal jitter applied as specified in 95.8.8.5. A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The low-pass filter is used to create ISI-induced vertical eye closure penalty (VECP). The low-pass filter, when combined with the E/O converter, should have a frequency response that results in the appropriate level of initial vertical eye closure before the sinusoidal terms are added.

The sinusoidal amplitude interferer 1 causes jitter that is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferers, and the low-pass filter are adjusted so that the VECP, stressed eye J2 Jitter, and stressed eye J4 Jitter specifications given in Table 95–7 are met simultaneously while also passing the stressed receiver eye mask in Table 95–7 according to the methods specified in 95.8.7 (the random noise effects such as RIN, or random clock jitter, do not need to be minimized).

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized.

The stressed receiver conformance signal verification is described in 95.8.8.4.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 95–7. Pattern 3 or Pattern 5, or a valid 100GBASE–SR4 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 100GBASE-SR4 the relevant BER is the interface BER at the PMD service interface. The interface BER is the average of the four BER of the receive lanes when stressed: see 95.8.1.1. If present, the RS-FEC

sublayer can measure the interface symbol error ratio at its input. If each lane is stressed in turn, the PMD interface BER is the average of the BERs of all the lanes when stressed: see 95.8.1.1.

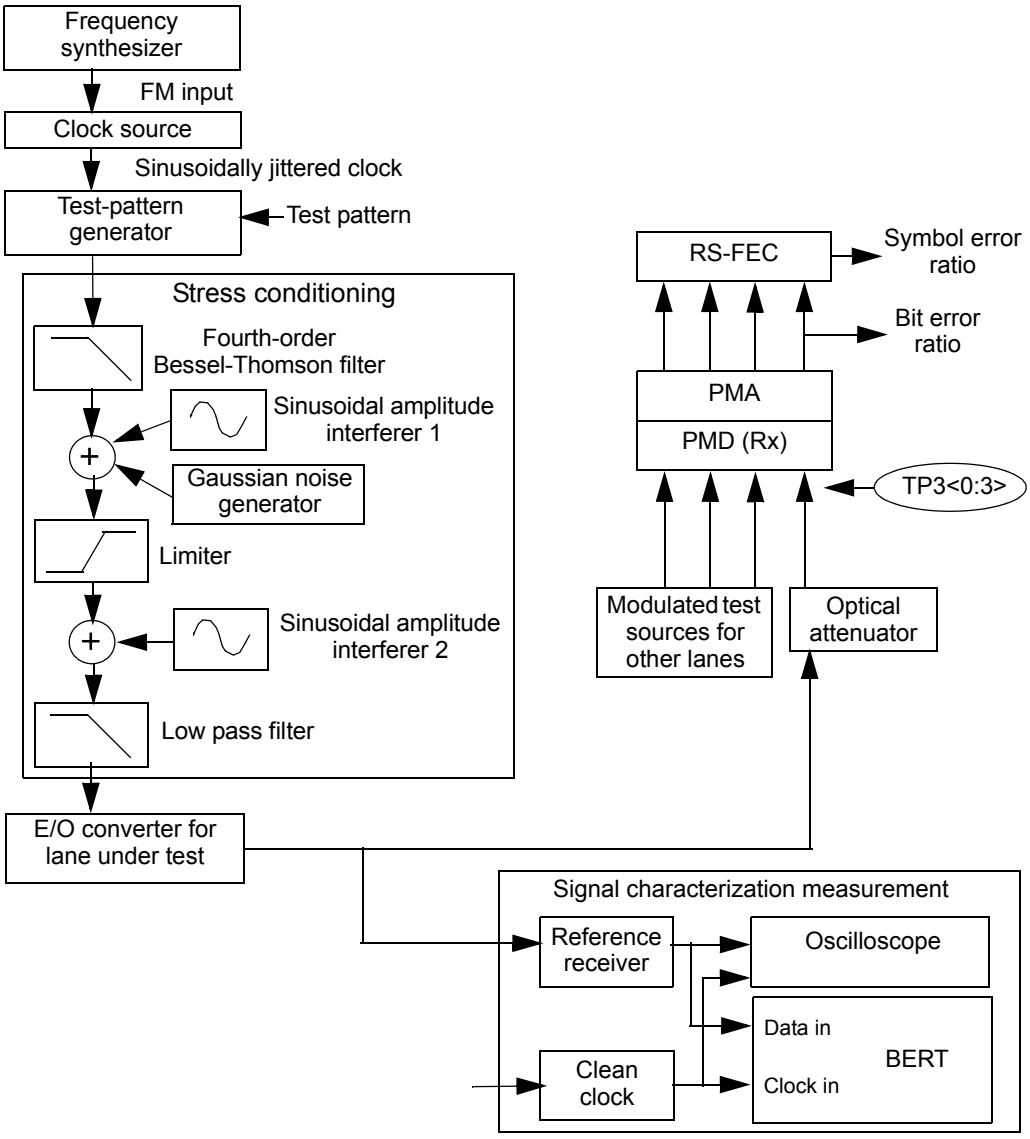


Figure 95–3—Stressed receiver conformance test block diagram

95.8.8.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver of the lane under test meets BER requirements with near worst-case waveforms at TP3.

The primary parameters of the conformance test signal are vertical eye closure penalty (VECP), stressed eye J2 Jitter and stressed eye J4 Jitter. VECP is measured at the time center of the eye, half way between the normalized times of 0 and 1 on the unit interval (UI) scale as determined by the eye crossing means. VECP is given by Equation (87-1), and illustrated in Figure 87-4 (see 87.8.11.2). Stressed eye J2 Jitter and stressed eye J4 jitter are defined in 95.8.8.3.

An example stressed receiver conformance test setup is shown in Figure 95–3, however any approach that modulates or creates the appropriate levels and frequencies of the VECP and jitter components is acceptable.

Residual low probability noise and jitter should be minimized so that the outer slopes of the final amplitude histograms are as steep as possible.

The following steps describe a possible method for setting up and calibrating a stressed eye conformance signal when using a stressed receiver conformance test setup as shown in Figure 95–3:

1) Set the signaling rate of the test pattern generator to meet the requirements in Table 95–7.
2) With the sinusoidal interferers and sinusoidal jitter turned off, set the extinction ratio of the E/O to approximately the minimum specified in Table 95–6.
3) The required values of VECP, J2 Jitter and J4 Jitter of the stressed receiver conformance signal are given in Table 95–7.

   With the sinusoidal interferers and sinusoidal jitter turned off, greater than two thirds of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the low-pass filter. Any remaining VECP must be created with sinusoidal interferer 2 or sinusoidal jitter.

   The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate.

   Sinusoidal jitter is added as specified in Table 95–11. When calibrating the conformance signal, the sinusoidal jitter frequency should be well within the 10 MHz to 10 times LB as defined in Table 95–11.

   Iterate the adjustments of sinusoidal interferers and Gaussian noise generator until the values of VECP, stressed eye J2 Jitter and stressed eye J4 Jitter meet the requirements in Table 95–7, and sinusoidal jitter above 10 MHz is as specified in Table 95–11.

Each receiver lane is conformance tested in turn. The source for the lane under test is adjusted to supply a signal at the input to the receiver under test at the "Stressed receiver sensitivity (OMA), each lane (max)" specified in Table 95–7, and the test sources for the other lanes is set to the "OMA of each aggressor lane" specified in Table 95–7.

95.8.8.3 J2 and J4 Jitter

J2 Jitter is defined as the time interval at the average optical power level that includes all but 10^{-2} of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram. If measured using an oscilloscope, the histogram should include at least 10 000 hits, and should be taken over about 1% of the signal amplitude. If measured by plotting BER vs. decision time, J2 is the time interval between the two points with a BER of 2.5×10^{-3}.

J4 Jitter is defined as the time interval at the average optical power level that includes all but 10^{-4} of the jitter distribution. If measured using an oscilloscope, the histogram should include at least 1 000 000 hits, and should be taken over about 1% of the signal amplitude. If measured by plotting BER vs. decision time, J4 is the time interval between the two points with a BER of 2.5×10^{-5}.

95.8.8.4 Stressed receiver conformance test signal verification

The stressed receiver conformance test signal can be verified using an optical reference receiver with an ideal fourth-order Bessel-Thomson response with a reference frequency f_r of 19.34 GHz. Use of G.691

tolerance filters may significantly degrade this calibration. The clock output from the clock source in Figure 95–3 will be modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye J2 Jitter and stressed eye J4 Jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 95–3) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system will result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the reference O/E, filters and BERT and/or to correct for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this standard, it is recommended that the implementor fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 95.8.8.2 and 95.8.8.5.

95.8.8.5 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 95–11.

Table 95–11—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	$5 \times 10^5 / f$
10 MHz $< f \leq 10\ LB$[a]	0.05

[a]*LB* = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

95.9 Safety, installation, environment, and labeling

95.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

95.9.2 Laser safety

100GBASE-SR4 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[4]

95.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

95.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-SR4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

95.9.5 Electromagnetic emission

A system integrating a 100GBASE-SR4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

95.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

95.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-SR4).

Labeling requirements for Hazard Level 1M lasers are given in the laser safety standards referenced in 95.9.2.

[4]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

95.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 95–4.

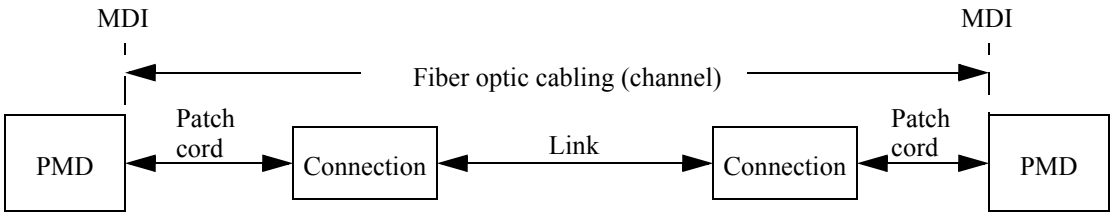


Figure 95–4—Fiber optic cabling model

The channel insertion loss is given in Table 95–12. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, modal dispersion, reflections and losses of all connectors and splices meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1:2009. As OM4 optical fiber meets the requirements for OM3, a channel compliant to the "OM3" column may use OM4 optical fiber, or a combination of OM3 and OM4. The term channel is used here for consistency with generic cabling standards.

Table 95–12—Fiber optic cabling (channel) characteristics for 100GBASE-SR4

Description	OM3	OM4	Unit
Operating distance (max)	70	100	m
Cabling Skew (max)	79		ns
Cabling Skew Variation[a] (max)	2.4		ns
Channel insertion loss[b] (max)	1.8	1.9	dB
Channel insertion loss (min)	0		dB

[a]An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.
[b]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

95.11 Characteristics of the fiber optic cabling (channel)

The 100GBASE-SR4 fiber optic cabling shall meet the specifications defined in Table 95–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

95.11.1 Optical fiber cable

The fiber contained within the 100GBASE-SR4 fiber optic cabling shall comply with the specifications and parameters of Table 95–13. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 95–12.

Table 95–13—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	Unit
Nominal core diameter	50		μm
Nominal fiber specification wavelength	850		nm
Effective modal bandwidth (min)[c]	2000	4700	MHz.km
Cabled optical fiber attenuation (max)	3.5		dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		ps/nm^2 km

[a]IEC 60793-2-10 type A1a.2
[b]IEC 60793-2-10 type A1a.3
[c]When measured with the launch conditions specified in Table 95–6

95.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 95–4, consists of a mated pair of optical connectors.

95.11.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports 3 connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 95–12 are met. However, the loss of a single connection shall not exceed 0.75 dB

95.11.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

95.11.3 Medium Dependent Interface (MDI)

The 100GBASE-SR4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 95–4). The 100GBASE-SR4 PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 95–5. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;
b) PMD receptacle.

95.11.3.1 Optical lane assignments

The four transmit and four receive optical lanes of 100GBASE-SR4 shall occupy the positions depicted in Figure 95–5 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused.

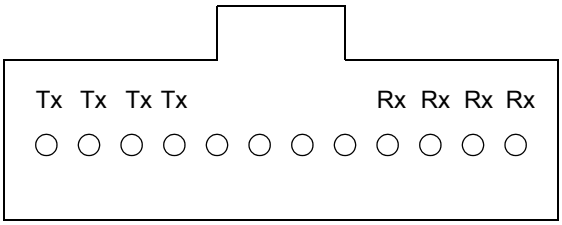


Figure 95–5—100GBASE-SR4 optical lane assignments

95.11.3.2 Medium Dependent Interface (MDI) requirements

The MDI adapter or receptacle shall meet the dimensional specifications for interface 7-1-3: *MPO adapter interface - opposed keyway configuration*, or interface 7-1-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4: *MPO female plug connector, flat interface for 2 to 12 fibres*, as defined in IEC 61754-7-1. The MDI shall optically mate with the plug on the optical fiber cabling. Figure 95–6 shows an MPO female plug connector with flat interface, and an MDI.

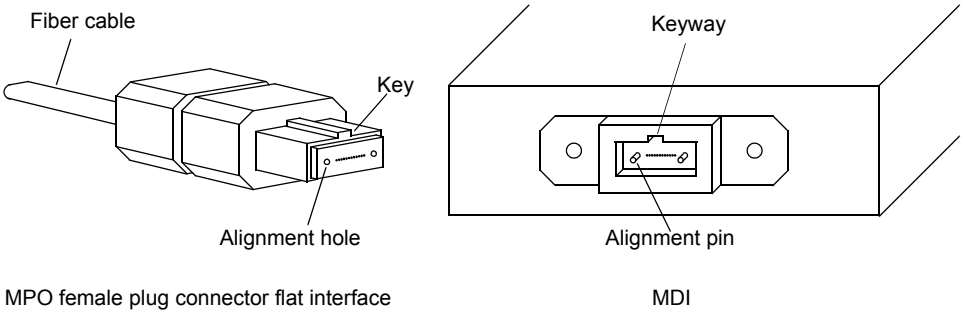


Figure 95–6—MPO female plug with flat interface and MDI

The MDI shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 95.5.1, not at the MDI.

95.12 Protocol implementation conformance statement (PICS) proforma for Clause 95, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4[5]

95.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 95, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

95.12.2 Identification

95.12.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

95.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bm-201x, Clause 95, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bm-201x.)	

Date of Statement	

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

95.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
SR4	100GBASE-SR4 PMD	95.7	Device supports requirements for 100GBASE-SR4 PHY	O	Yes [ ] No [ ]
*INS	Installation / cable	95.11	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CTP1	Reference point TP1 exposed and available for testing	95.5.1	This point may be made available for use by implementors to certify component conformance	O	Yes [ ] No [ ]
CTP4	Reference point TP4 exposed and available for testing	95.5.1	This point may be made available for use by implementors to certify component conformance	O	Yes [ ] No [ ]
CDC	Delay constraints	95.3.1	Device conforms to delay constraints	M	Yes [ ]
CSC	Skew constraints	95.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	95.4	Registers and interface supported	O	Yes [ ] No [ ]

95.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4

95.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Compatible with 100GBASE-R RS-FEC, PCS, and PMA	95.1		M	Yes [ ]
CF2	Integration with management functions	95.1		O	Yes [ ] No [ ]
CF3	Bit error ratio	95.1.1	Meets the BER specified in 95.1.1	M	Yes [ ]
CF4	Transmit function	95.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
CF5	Mapping between optical signal and logical signal for transmitter	95.5.2	Higher optical power is a one	M	Yes [ ]
CF6	Receive function	95.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
CF7	Conversion of four optical signals to four electrical signals	95.5.3	For delivery to the PMD service interface	M	Yes [ ]
CF8	Mapping between optical signal and logical signal for receiver	95.5.3	Higher optical power is a one	M	Yes [ ]
CF9	Global Signal Detect function	95.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
CF10	Global Signal Detect behavior	95.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
CF11	Lane-by-lane Signal Detect function	95.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 95–4	MD:O	Yes [ ] No [ ] N/A [ ]
CF12	PMD reset function	95.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

95.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	Management register set	95.4		MD:M	Yes [ ] N/A [ ]
CM2	Global transmit disable function	95.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM3	PMD_lane_by_lane_transmit_ disable function	95.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM4	PMD lane-by-lane transmit disable	95.5.8	Disables each optical transmitter independently if CM3 = No	!MD:O	Yes [ ] No [ ]
CM5	PMD_fault function	95.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM6	PMD_transmit_fault function	95.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
CM7	PMD_receive_fault function	95.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

95.12.4.3 PMD to MDI optical specifications for 100GBASE-SR4

Item	Feature	Subclause	Value/Comment	Status	Support
CSR1	Transmitter meets specifications in Table 95–6	95.7.1	Per definitions in 95.8	M	Yes [ ] N/A [ ]
CSR2	Receiver meets specifications in Table 95–7	95.7.2	Per definitions in 95.8	M	Yes [ ] N/A [ ]

95.12.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Measurement cable	95.8	2 m to 5 m in length	M	Yes [ ]
COM2	Center wavelength and spectral width	95.8.2	Per TIA/EIA-455-127-A or IEC 61280-1-3 under modulated conditions	M	Yes [ ]
COM3	Average optical power	95.8.3	Per IEC 61280-1-1	M	Yes [ ]
COM4	OMA measurements	95.8.4	Each lane	M	Yes [ ]
COM5	Transmitter and dispersion penalty	95.8.5	Each lane	M	Yes [ ]
COM6	Extinction ratio	95.8.6	Per IEC 61280-2-2	M	Yes [ ]
COM7	Transmit eye	95.8.7	Each lane	M	Yes [ ]
COM8	Stressed receiver sensitivity	95.8.8	See 95.8.8	M	Yes [ ]

95.12.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CES1	General safety	95.9.1	Conforms to IEC 60950-1	M	Yes [ ]
CES2	Laser safety—IEC Hazard Level 1	95.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
CES3	Electromagnetic interference	95.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

95.12.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
COC1	Fiber optic cabling	95.11	Meets requirements specified in Table 95–12	INS:M	Yes [ ] N/A [ ]
COC2	Maximum discrete reflectance	95.11.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
COC3	MDI layout	95.11.3.1	Optical lane assignments per Figure 95–5	M	Yes [ ]
COC4	MDI dimensions	95.11.3.2	Per IEC 61754-7-1 interface 7-1-3 or interface 7-1-10	M	Yes [ ]
COC5	Cabling connector dimensions	95.11.3.2	Per IEC 61754-7-1 interface 7-1-4	INS:M	Yes [ ] N/A [ ]
COC6	MDI mating	95.11.3.2	MDI optically mates with plug on the cabling	M	Yes [ ]
COC7	MDI requirements	95.11.3.2	Meets IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]

Annex A

(informative)

Bibliography

Insert the following reference in alphabetical order and renumber the list:

[Bx1] OIF-CEI-03.1, Common Electrical I/O (CEI)—Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O.

[Editor's note (to be removed prior to publication) - The OIF CEI-28G-VSR specification is currently in the OIF publication process, and is expected to be published as part of OIFCEI-03.1 in early 2014.]

Annex 83A

(normative)

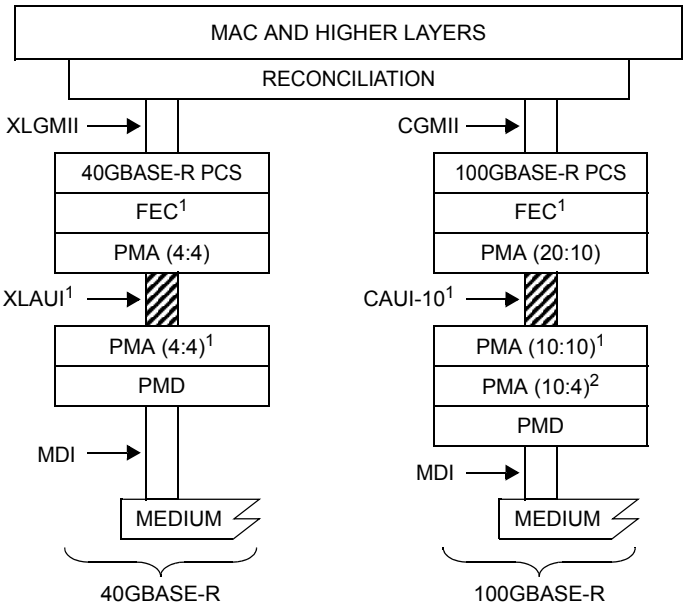
Change Title of Annex 83A as follows:

40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)

Change 83A.1, 83A.1.1, 83A.1.2, and replace Figure 83A-1 as follows:

83A.1 Overview

This annex defines the functional and electrical characteristics for the optional 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10). Figure 83A–1 shows the relationships of the XLGMII, PMA, XLAUI, and PMD for 40 Gb/s and CGMII, PMA, CAUI-10, and PMD for 100 Gb/s.



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE
NOTE 2—CONDITIONAL BASED ON PMD TYPE

Figure 83A–1—Example relationship of XLAUI and CAUI-10 to IEEE 802.3 CSMA/CD LAN model

The purpose of the optional XLAUI or CAUI-10 is to provide a flexible chip-to-chip and chip-to-module interconnect for 40 Gb/s or 100 Gb/s components. Annex 83A provides compliance requirements for XLAUI/CAUI-10 transmitters and receivers while Annex 83B specifies the electrical requirements for the chip-to-module interconnection.

The XLAUI/CAUI-10 allows interconnect distances of approximately 25 cm over printed circuit board including one connector, see 83A.4.

An example application of CAUI-10 includes providing a physical connection between a ten-lane 100 Gb/s PMA and a 10:4 PMA mapping element. An example application of XLAUI is to provide lane extension for interfacing MAC and PHY components in a 40 Gb/s Ethernet system distributed across a circuit board.

The optional XLAUI/CAUI-10 interface has the following characteristics:

a) Independent transmit and receive data paths
b) Differential AC coupled signaling with low voltage swing
c) Self-timed interface
d) Shared technology with other 40 Gb/s or 100 Gb/s interfaces
e) Utilization of 64B/66B coding

83A.1.1 Summary of major concepts

The following is a list of the major concepts of XLAUI and CAUI-10:

a) The optional XLAUI/CAUI-10 interface can be inserted between PMA layers in the IEEE 802.3 CSMA/CD LAN model to transparently enable chip-to-chip communication
b) The XLAUI is organized into four lanes, the CAUI-10 is organized into ten lanes
c) The XLAUI/CAUI-10 interface is a parallel electrical interface with each lane running at a nominal rate of 10.3125 Gb/s

83A.1.2 Rate of operation

The XLAUI interface supports the 40 Gb/s data rate and the CAUI-10 interface supports the 100 Gb/s data rate. For 40 Gb/s applications, the data stream shall be presented in four lanes as described in Clause 83. For 100 Gb/s applications, the data stream shall be presented in ten lanes as described in Clause 83. The data is 64B/66B coded. The nominal signaling rate for each lane in both 40 Gb/s and 100 Gb/s applications shall be 10.3125 Gb/s.

Change 83A.2 (including the title) and replace Figure 83A-2 as follows:

83A.2 XLAUI/CAUI-10 link block diagram

XLAUI/CAUI-10 link is illustrated in Figure 83A–2. XLAUI/CAUI-10 channel is defined from the transmit pad to the receive pad including any AC coupling in the path.

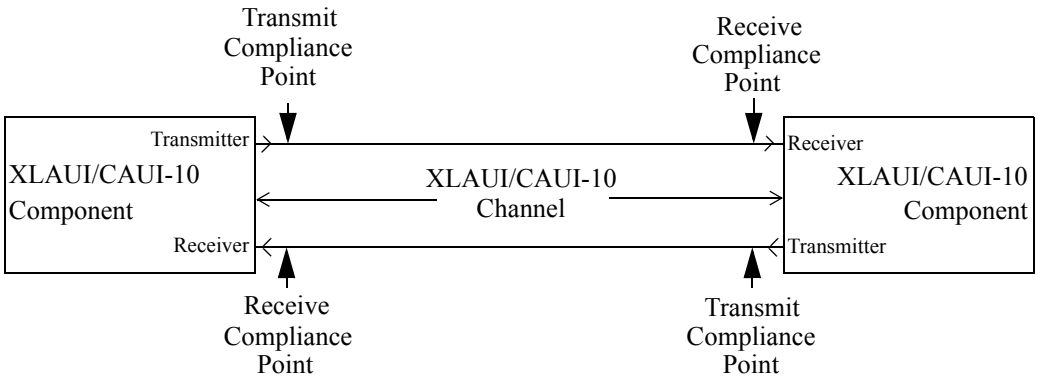


Figure 83A–2—Definition of transmit and receive compliance points

Change 83A.3 (including the title), 83A.3.1, and 83A.3.2 as follows:

83A.3 XLAUI/CAUI-10 electrical characteristics

The electrical characteristics of the XLAUI/CAUI-10 interface are specified such that they can be applied within a variety of 40 Gb/s Ethernet or 100 Gb/s Ethernet equipment types. The electrical characteristics for XLAUI/CAUI-10 shall meet the specifications defined in 83A.3.1, 83A.3.2, 83A.3.3, and 83A.3.4.

83A.3.1 Signal levels

The XLAUI/CAUI-10 is a low-swing AC coupled differential interface. AC coupling allows for interoperability between components operating from different supply voltages. Differential signal swings are defined in the following subclauses, and depend on several factors such as transmitter de-emphasis and transmission line losses.

83A.3.2 Signal paths

The XLAUI/CAUI-10 signal paths are point-to-point connections. Each path corresponds to a XLAUI/CAUI-10 lane, and is comprised of two complementary signals making a balanced differential pair. For XLAUI, there are four differential paths in each direction for a total of eight pairs, or sixteen connections. For CAUI-10, there are ten differential paths in each direction for a total of twenty pairs, or 40 connections.

Change 83A.3.2a (as inserted by IEEE Std 802.3bj-201x) as follows:

83A.3.2a EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1) then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI-10 shutdown.

If the EEE capability includes XLAUI/CAUI-10 shutdown (see 78.5.2) then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal

0xFF00 which is transmitted across the XLAUI/CAUI-10. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction XLAUI/CAUI-10 transmitter is disabled as specified in 83A.3.3.1.1. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the XLAUI/CAUI-10. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction XLAUI/CAUI-10 transmitter is disabled as specified in 83A.3.3.1.1

Change the text of 83A.3.3 as follows:

83A.3.3 Transmitter characteristics

The XLAUI/CAUI-10 transmitter characteristics measured at the transmitter compliance point are specified in Table 83A–1. The XLAUI/CAUI-10 signaling rate shall be the signaling rate defined in Table 83A–1.

Change the third paragraph of 83A.3.3.1 as follows:

83A.3.3.1 Output amplitude

See Figure 83A–5 for an illustration of absolute driver output voltage limits, definition of differential peak-to-peak amplitude, and definition of the parameters used to calculate de-emphasis. SLi<P> and SLi<N> are positive and negative sides of a differential signal pair for lane i (i = 0, 1, 2, 3 for XLAUI. For CAUI-10 i = 0:9).

Change 83A.3.3.1.1 (as inserted by IEEE Std 802.3bj-201x) as follows:

83A.3.3.1.1 Amplitude and swing

For EEE capability with XLAUI/CAUI-10 shutdown, the XLAUI/CAUI-10 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction. Furthermore, the XLAUI/CAUI-10 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

Change 83A.3.3.6 (as inserted by IEEE Std 802.3bj-201x) as follows:

83A.3.3.6 Global transmit disable function

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction XLAUI/CAUI-10 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction XLAUI/CAUI-10 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in 83A.3.3.1.1.

83A.3.4 Receiver characteristics

Change the text of 83A.3.4.2 as follows:

83A.3.4.2 Input signal definition

A compliant input signal to a XLAUI/CAUI-10 receiver has characteristics determined by a compliant XLAUI/CAUI-10 driver and channel. The input signal definition satisfies the eye mask defined in Table 83A–2 and Figure 83A–9. Input signal jitter does not exceed the jitter tolerance requirements specified in 83A.3.4.6. Stressed receiver measurement requirements are specified in 83A.5.2.

Change 83A.3.4.5 and the text of 83A.3.4.6 as follows:

83A.3.4.5 AC coupling

The XLAUI/CAUI-10 receiver shall be AC coupled to the XLAUI/CAUI-10 transmitter to allow for maximum interoperability between various 10 Gb/s components. AC coupling is considered to be part of the receiver for the purposes of this specification except when interfacing with modules defined in Annex 83B or explicitly stated otherwise. It should be noted that there may be various methods for AC coupling in actual implementations.

83A.3.4.6 Jitter tolerance

The XLAUI/CAUI-10 receiver shall have a peak-to-peak total jitter amplitude tolerance of at least the minimum total input jitter tolerance defined in Table 83A–2. This total jitter is composed of two components: deterministic jitter and random jitter. Deterministic jitter tolerance shall be at least the minimum deterministic input jitter tolerance defined in Table 83A–2. The XLAUI/CAUI-10 receiver shall tolerate sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 83A–12. This sub-component of deterministic jitter is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

Change 83A.3.4.7 (as inserted by IEEE Std 802.3bj-201x) as follows:

83A.3.4.7 Global energy detect function

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and XLAUI/CAUI-10 shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the XLAUI/CAUI-10 for the ingress direction SIGNAL_DETECT is set to FAIL following a transition from aui_rx_mode = DATA to aui_rx_mode = QUIET. When aui_rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input detects an ALERT signal driven from the XLAUI/CAUI-10 link partner. While aui_rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is applied to the channel.

Change the first and last paragraphs of 83A.4 as follows:

83A.4 Interconnect characteristics

This ~~section~~ subclause describes recommended characteristics which are used to characterize a XLAUI/CAUI-10 channel as shown in Figure 83A–2. The value for differential insertion loss is summarized in Equation (83A–9) and illustrated in Figure 83A–13. The value for minimum return loss is summarized in Equation (83A–10) and illustrated in Figure 83A–14. The channel is terminated with 100 Ω differential impedance. Other impairments such as crosstalk can have a material impact on the link performance and should be minimized.

The XLAUI/CAUI-10 is primarily intended as a point-to-point interface of up to approximately 25 cm between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). Longer reaches for the XLAUI/CAUI-10 may be achieved by the use of better PCB materials, as the performance of an actual XLAUI/CAUI-10 interconnect is highly dependent on the implementation.

Change 83A.5, 83A.5.1, and 83A.5.2 (including Figure 83A-15) as follows:

83A.5 Electrical parameter measurement methods

This subclause describes the measurement methodology that is to be used to verify XLAUI/CAUI-10 compliance. Eye templates are measured with AC coupling and centered at 0 V differential. The signal waveform, eye, and jitter may be measured using a receiver with at least an equivalent 12 GHz low-pass filter response. Jitter values and eye masks are specified for BER 10^{-12}.

83A.5.1 Transmit jitter

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The test pattern for jitter measurements shall be PRBS31 test pattern in 83.5.10 or scrambled idle in 82.2.10. Crossing times are defined with respect to the mid-point (0 V) of the AC coupled differential signal. De-emphasis shall be off during jitter testing. Transmit de-emphasis off state is defined by any setting that gives optimal performance for transmitter jitter and eye mask evaluation. All XLAUI/CAUI-10 transmitter lanes shall be active and all XLAUI/CAUI-10 receive lanes shall be receiving maximum amplitude and fastest rise time (as defined in Table 83A–1) during transmit jitter testing to ensure maximum lane-lane crosstalk is included in the jitter evaluation.

83A.5.2 Receiver tolerance

The XLAUI/CAUI-10 jitter tolerance test setup in Figure 83A–15 or its equivalent shall meet the receiver eye mask defined in Table 83A–2. Applied jitter is measured using the methodology described in Annex 48B.3. Deterministic jitter is added to a clean test pattern by adding sinusoidal jitter as defined in 83A.3.4.6, along with low-pass filter stress, followed by a limiting function, and frequency-dependent attenuation. The low-pass filter stress is added until the 0.34 UI Deterministic Jitter is achieved. Frequency-dependent attenuation is then added using PCB trace or frequency-dependent attenuation which emulates PCB loss. Frequency-dependent attenuation is added until 0.42 UI Deterministic Jitter is achieved. Random jitter is added to the test signal using an interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from 50 MHz to 6 GHz with a crest factor of no less than 5. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask defined in Table 83A–2. All

XLAUI/CAUI-10 lanes shall be active during jitter tolerance testing. The PRBS31 pattern defined in 83.5.10 or scrambled idle defined in 82.2.10 is used for evaluating XLAUI/CAUI-10 jitter tolerance.

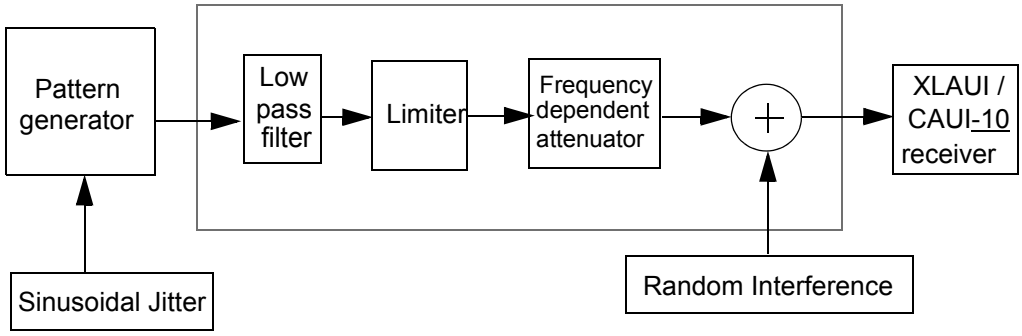


Figure 83A–15—Stressed-eye and jitter tolerance test setup

83A.6 Environmental specifications

Change 83A.6.4, and 83A.6.5 as follows:

83A.6.4 Electromagnetic compatibility

A system integrating the XLAUI/CAUI-10 shall comply with applicable local and national codes for the limitation of electromagnetic interference.

83A.6.5 Temperature and humidity

A system integrating the XLAUI/CAUI-10 is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

Change the title of 83A.7 as follows:

83A.7 Protocol implementation conformance statement (PICS) proforma for Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)[6]

Change the first paragraph of 83A.7.1 as follows:

83A.7.1 Introduction

The supplier of a XLAUI/CAUI-10 implementation that is claimed to conform to Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10), shall complete the following protocol implementation conformance statement (PICS) proforma.

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

83A.7.2 Identification

83A.7.2.2 Protocol summary

Change Identification of protocol standard as follows:

IEEE Std 802.3-201x, Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)

83A.7.3 Major capabilities/options

Change items NOL, RATE, IO, and *LPI (as inserted by IEEE Std 802.3bj-201x) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	XLAUI is organized into four lanes, CAUI-10 is organized into ten lanes	83A.1.2	See Clause 83	M	Yes [ ]
RATE	Each XLAUI/CAUI-10 lane operates at 10.3125 Gb/s	83A.1.2	10.3125 Gb/s (nominal)	M	Yes [ ]
IO	Meets XLAUI/CAUI-10 Electrical Characteristics	83A.3	Supports transmit and receive compliance points	M	Yes [ ]
*LPI	Support for CAUI-10 shut-down	83A.3.2a		O	Yes [ ] No [ ]

Change the titles of 83A.7.4 as follows:

83A.7.4 XLAUI/CAUI-10 transmitter requirements

Change items TC11 and TC12 (as inserted by IEEE Std 802.3bj-201x) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
TC11	Amplitude & swing for XLAUI/CAUI-10 shutdown	83A.3.3.1.1		LPI:M	Yes [ ]
TC12	Transmit disable for XLAUI/CAUI-10 shutdown	83A.3.3.6		LPI:M	Yes [ ]

Change the titles of 83A.7.5 as follows:

83A.7.5 XLAUI/CAUI-10 receiver requirements

Change item RC8 (as inserted by IEEE Std 802.3bj-201x) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
RC8	Signal detect for XLAUI/CAUI-10 shutdown	83A.3.4.7		LPI:M	Yes [ ]

83A.7.6 Electrical measurement methods

Change items EM4 and EM5 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
EM4	Meet jitter tolerance requirement with all XLAUI/CAUI-10 channels active	83A.5.2	Yes	M	Yes [ ]
EM5	XLAUI/CAUI-10 Jitter Tolerance Test Pattern	83A.5.2	PRBS31 or scrambled idle	M	Yes [ ]

Annex 83B

(normative)

Change Title of Annex 83B as follows:

Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)

Change the first paragraph of 83B.1, replace Figure 83B-3, and change Table 83B-1 as follows:

83B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10). The purpose of this annex is to provide electrical characteristics and associated compliance points for pluggable module applications that use the XLAUI/CAUI-10 interface and shall use the same number of lanes and signaling rate defined in Annex 83A. Figure 83B–3 and Table 83B–1 summarize an example differential insertion loss budget associated with the chip-to-module application. The insertion loss of Equation (83A–9), excluding a 0.5 dB connector loss at 5.15625 GHz, is linearly scaled to 7.9 dB loss at 5.15625 GHz for the host XLAUI/CAUI-10 component, and 2.1 dB loss at 5.15625 GHz for the module as per Table 83B–1 and Equation (83B–1) for the host and Equation (83B–2) for the module. Tradeoffs can be made between the host PCB insertion loss and the connector loss. Equation (83B–1) is illustrated in Figure 83B–1 and Equation (83B–2) is illustrated in Figure 83B–2.

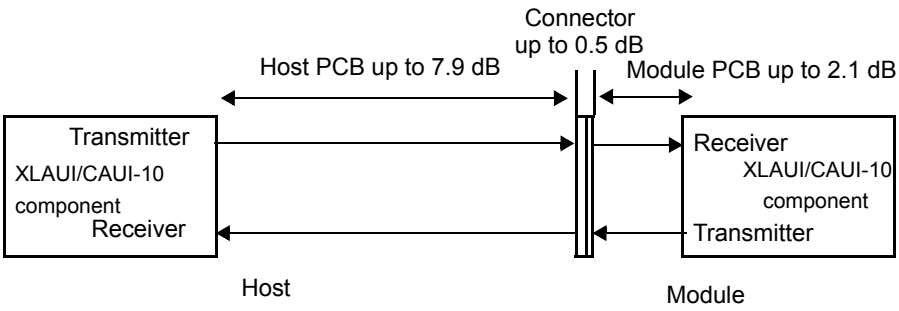


Figure 83B–3—Chip-to-module loss budget at 5.15625 GHz

Table 83B–1—Chip-to-module loss budget

Section	Differential insertion loss max. (at 5.15625 GHz)
Host XLAUI/CAUI-10 component to connector	7.9 dB
Connector loss	0.5 dB
Connector to module XLAUI/CAUI-10 component	2.1 dB

Change the title and first paragraph of 83B.2, replace Figure 83B-5, and replace Figure 83B-7 as follows:

83B.2 Compliance point specifications for chip-to-module XLAUI/CAUI-10

The chip-to-module XLAUI/CAUI-10 interface specifies compliance points around the module connector as depicted in Figure 83B–5 and Figure 83B–7. Chip-to-module devices shall meet the electrical characteristics defined in 83B.2, 83B.2.1, 83B.2.2, and 83B.2.3. Compliance points are defined to ensure interoperability between hosts and modules. A Module Compliance Board (MCB) is used to isolate the characteristics of the module, and a Host Compliance Board (HCB) is used to isolate the characteristics of the host. Figure 83B–5 and Figure 83B–7 include the loss associated with the HCB and MCB at 5.15625 GHz.

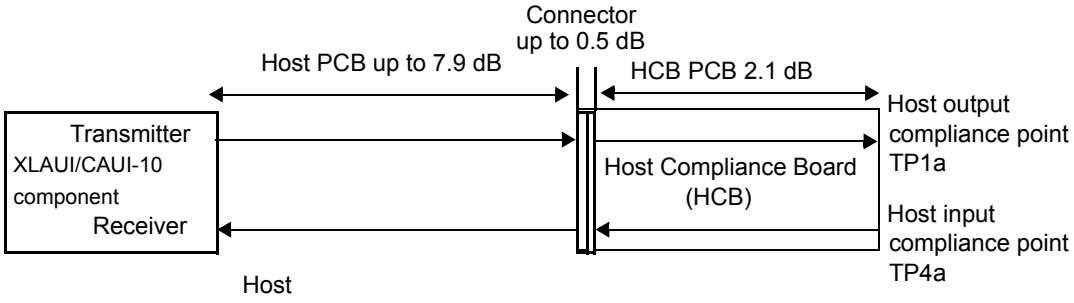


Figure 83B–5—Chip-to-module HCB insertion loss budget at 5.15625 GHz

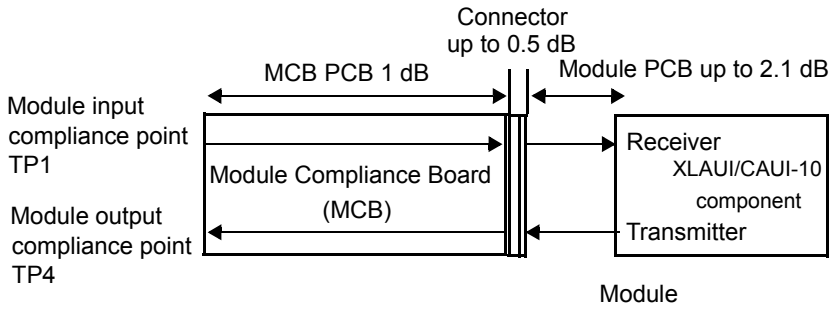


Figure 83B–7—Chip-to-module with MCB insertion loss budget at 5.15625 GHz

Change the first paragraph of 83B.2.1 as follows:

83B.2.1 Module specifications

A module that uses XLAUI/CAUI-10 to interface with a host shall meet the characteristics outlined in Table 83B–2 and Table 83B–3 when measured using the MCB and HCB (where the HCB is used to calibrate inputs to the module). Table 83B–2 also lists the equivalent test points for the XLPPI/CPPI (see Figure 86–3).

Change the first paragraph of 83B.2.2 as follows:

83B.2.2 Host specifications

A host that uses XLAUI/CAUI-10 to interface with a module shall meet the characteristics outlined in Table 83B–4 and Table 83B–5 when measured using the HCB and MCB (where MCB is used to calibrate inputs to the host). Table 83B–4 also lists the equivalent test points for the XLPPI/CPPI.

Change the text of 83B.2.3 and replace Figure 83B-10 as follows:

83B.2.3 Host input signal tolerance

Host XLAUI/CAUI-10 jitter tolerance evaluation shall be defined by a stressed input signal that comprises 0.25 UI Deterministic Jitter, and 0.15 UI random jitter for BER 10^{-12}. Deterministic Jitter is added to a clean test pattern as sinusoidal jitter defined in 83A.3.4.6. The limited low-pass filter stress is added until the 0.22 UI Deterministic Jitter is achieved. Frequency-dependent attenuation is then added using PCB trace or frequency-dependent attenuation that emulates PCB loss. Frequency-dependent attenuation is added until 0.25 UI Deterministic Jitter is achieved. Random jitter is added to the test signal using an interference generator, which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from 50 MHz to 6 GHz with a crest factor of no less than 5. Figure 83B–10 depicts a XLAUI/CAUI-10 jitter tolerance test setup. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask illustrated in Figure 83A–9 with the values for X1, X2, Y1, Y2 given in Table 83B–3. All XLAUI/CAUI-10 lanes shall be active during jitter tolerance testing. The PRBS31 pattern defined in 83.5.10 or scrambled idle defined in 82.2.10 is used for evaluating XLAUI/CAUI-10 jitter tolerance.

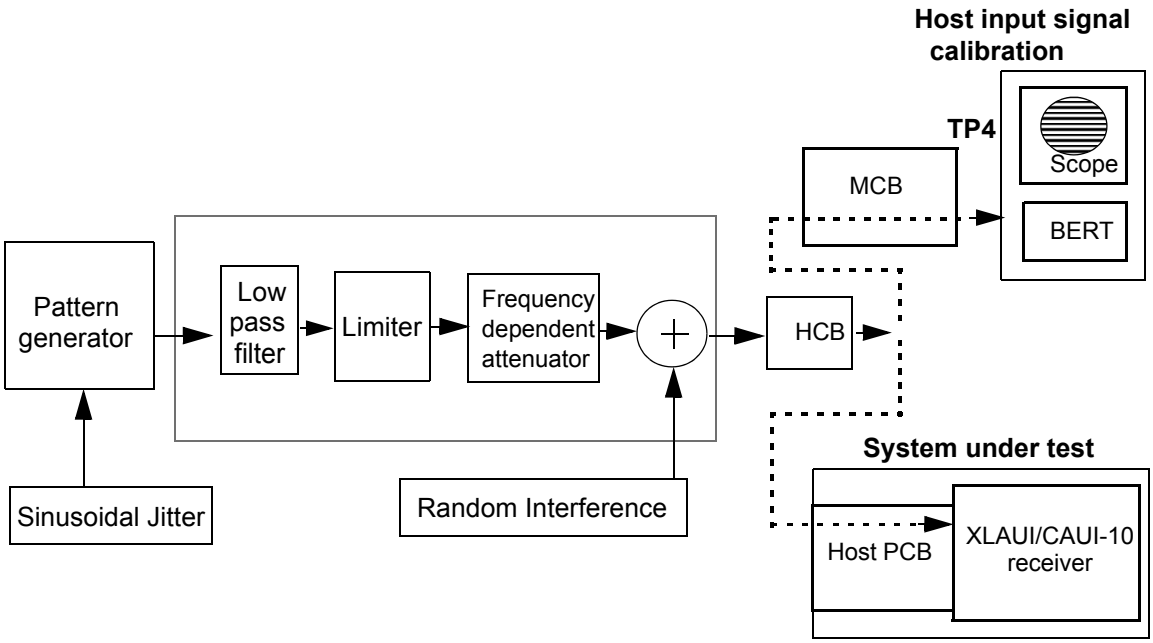


Figure 83B–10—Stressed-eye and jitter tolerance test setup

83B.3 Environmental specifications

Change 83B.3.4 and 83B.3.5 as follows:

83B.3.4 Electromagnetic compatibility

A system integrating the XLAUI/CAUI-10 shall comply with applicable local and national codes for the limitation of electromagnetic interference.

83B.3.5 Temperature and humidity

A system integrating the XLAUI/CAUI-10 is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

Change the title of 83B.4 as follows:

83B.4 Protocol implementation conformance statement (PICS) proforma for Annex 83B, Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)[7]

[7]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

Change the first paragraph of 83B.4.1 as follows:

83B.4.1 Introduction

The supplier of a chip-to-module XLAUI/CAUI-10 implementation that is claimed to conform to Annex 83B, Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10), shall complete the following protocol implementation conformance statement (PICS) proforma.

83B.4.2 Identification

83B.4.2.2 Protocol summary

Change Identification of protocol standard as follows:

IEEE Std 802.3-201x, Annex 83B, Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)

83B.4.3 Major capabilities/options

Change items NOL, RATE, and IO as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	XLAUI is organized into four lanes, CAUI-10 is organized into ten lanes	83A.1.2	See Clause 83	M	Yes [ ]
RATE	Each XLAUI/CAUI-10 lane operates at 10.3125 Gb/s	83A.1.2	10.3125 Gb/s (nominal)	M	Yes [ ]
IO	Meets chip-to-module XLAUI/CAUI-10 Electrical Characteristics	83B.2	Supports host/module compliance points	M	Yes [ ]

83B.4.4 Module requirements

Change item MC1 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	XLAUI/CAUI-10 compliant module	83B.2.1	Meets require-ments defined in Table 83B–2 and Table 83B–3	M	Yes [ ]

83B.4.5 Host requirements

Change items HC1 and HC2 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
HC1	XLAUI/CAUI-10 compliant host	83B.2.2	Meets requirements defined in Table 83B–4 and Table 83B–5	M	Yes [ ]
HC2	All XLAUI/CAUI-10 lanes active during jitter evaluation	83B.2.3	Yes	M	Yes [ ]

Annex 83C

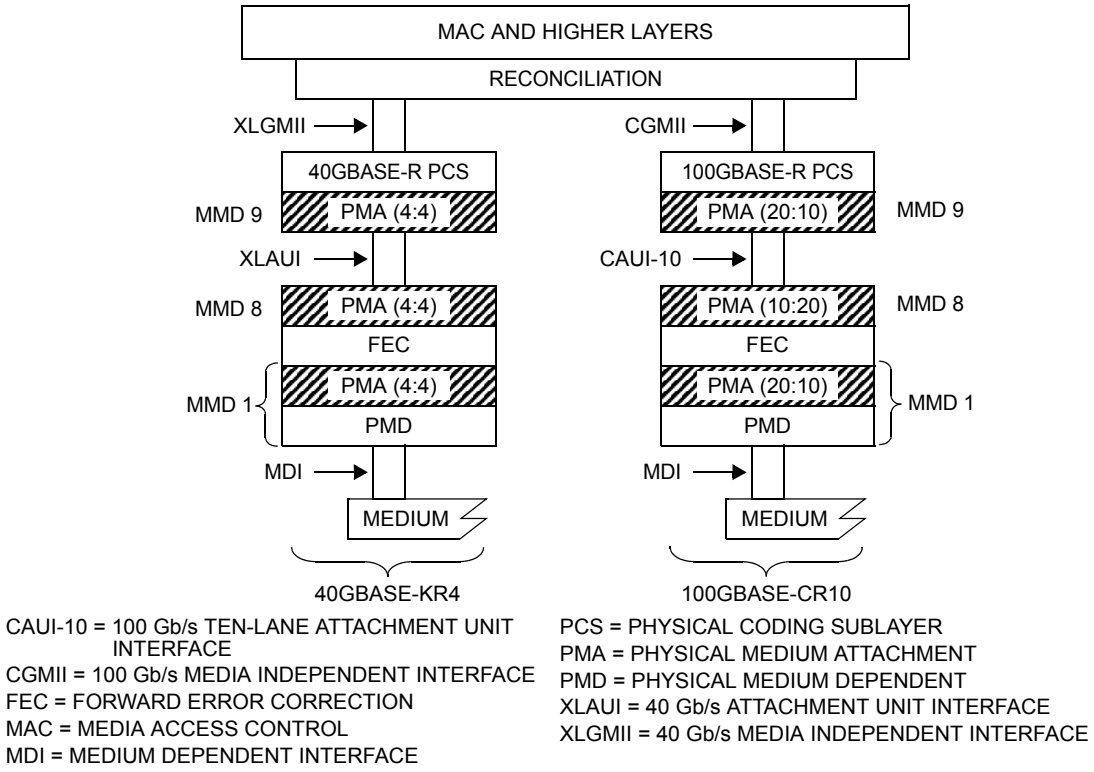
(informative)

PMA sublayer partitioning examples

83C.1 Partitioning examples with FEC

83C.1.2 FEC implemented with PMD

Replace Figure 83C-2 as follows:



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–2—Example FEC implemented with PMD

83C.1a Partitioning examples with RS-FEC

Change the title of 83C.1a.2 as follows:

83C.1a.2 Single CAUI-10 with RS-FEC

Replace Figure 83C-2b (as inserted by IEEE Std 802.3bj-201x) as follows:

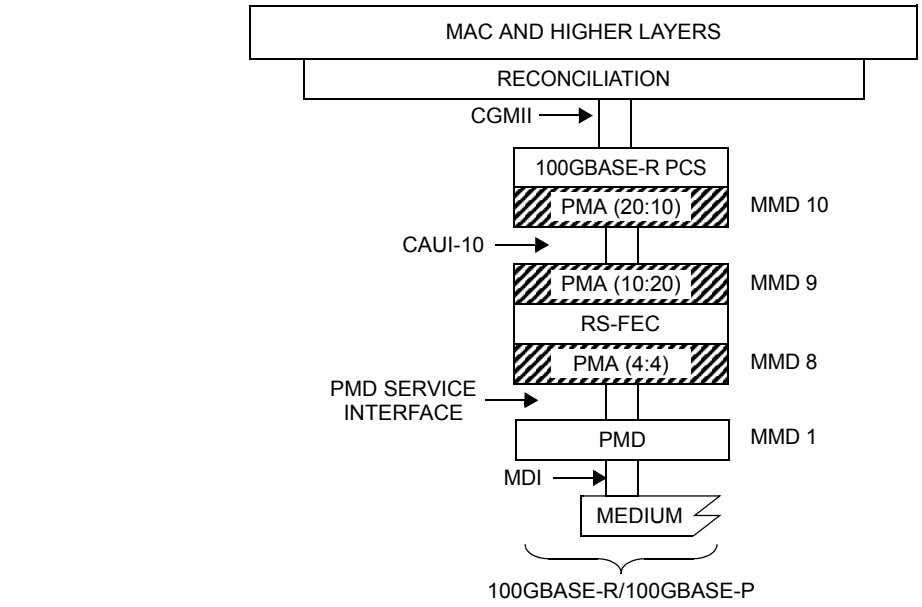


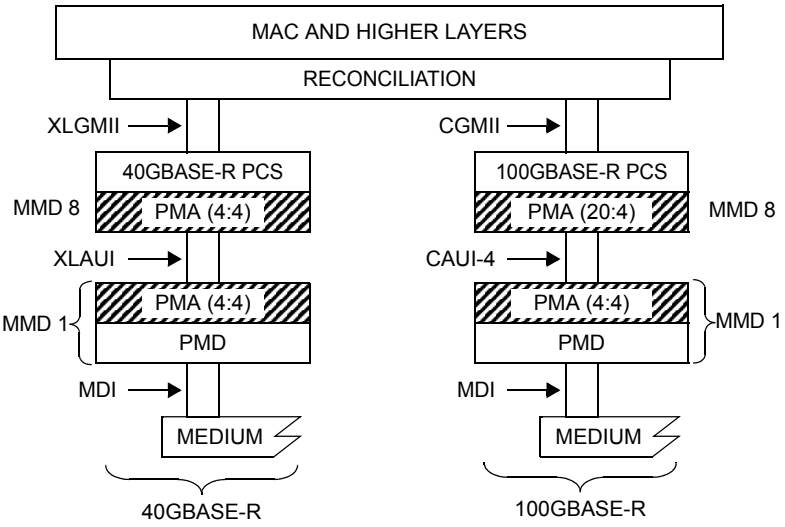
Figure 83C–2b—Example single CAUI-10 with RS-FEC

83C.2 Partitioning examples without FEC

Change the title of 83C.2.2 as follows:

83C.2.2 Single XLAUI/CAUI-4 without FEC

Replace Figure 83C-4 as follows:



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–4—Example single XLAUI/CAUI-4 without FEC

83C.2.3 Separate SERDES for optical module interface

Replace Figure 83C-5 as follows:

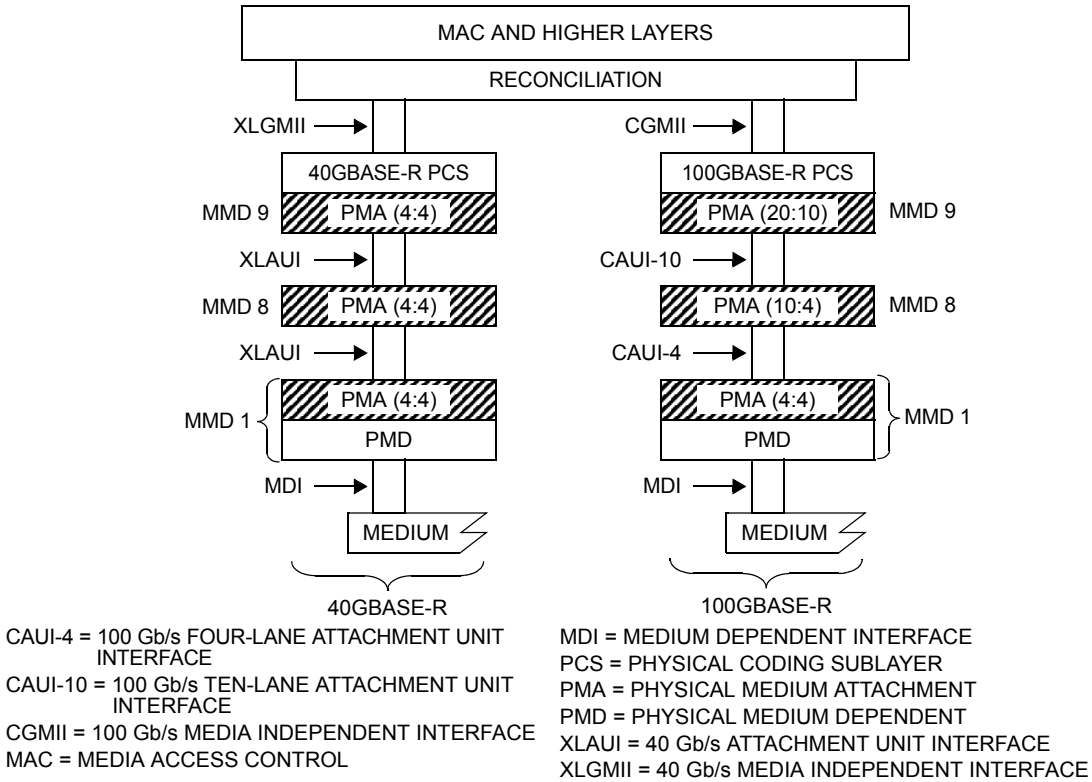


Figure 83C–5—Separate SERDES for optical module interface

Annex 83D

(normative)

Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4). Figure 83D–1 shows an example relationship of the CAUI-4 chip-to-chip interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-chip interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

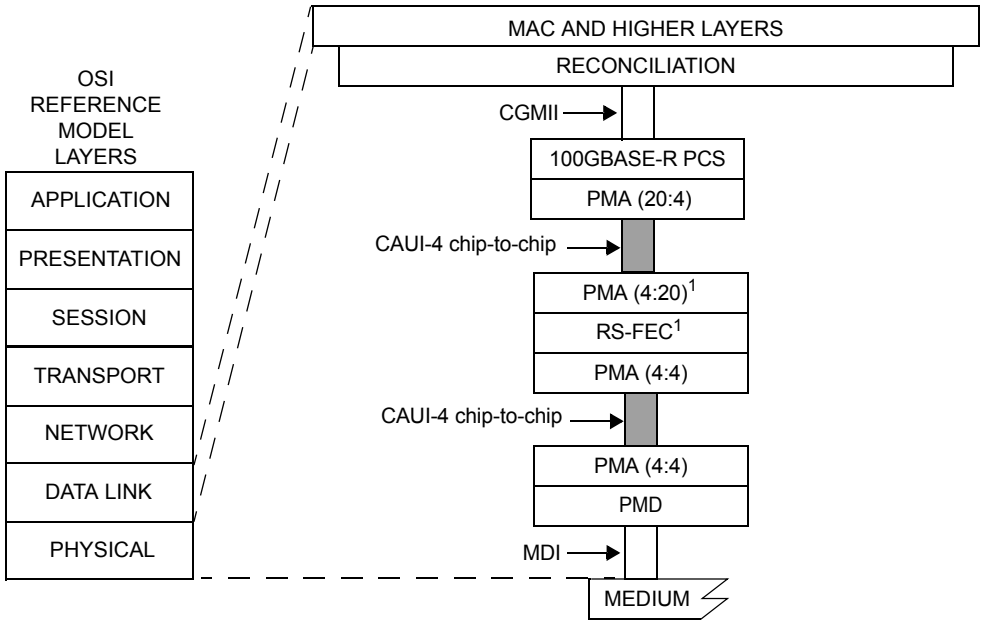


Figure 83D–1—Example CAUI-4 chip-to-chip relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model

The CAUI-4 bidirectional link is described in terms of a CAUI-4 transmitter, a CAUI-4 channel, and a CAUI-4 receiver. Figure 83D–2 depicts a typical CAUI-4 application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the informative differential insertion loss budget associated with the chip-to-chip application. The CAUI-4 chip-to-chip interface comprises independent data paths in each direction. Each data path contains four differential lanes which are AC coupled. The nominal signaling rate for each lane is 25.78125 GBd. The CAUI-4 transmitter on each end of the link is adjusted based on channel knowl-

edge to an approximate setting with the adaptive or adjustable receiver performing the remainder of the equalization. Operation and control of this receiver is outside the scope of this standard.

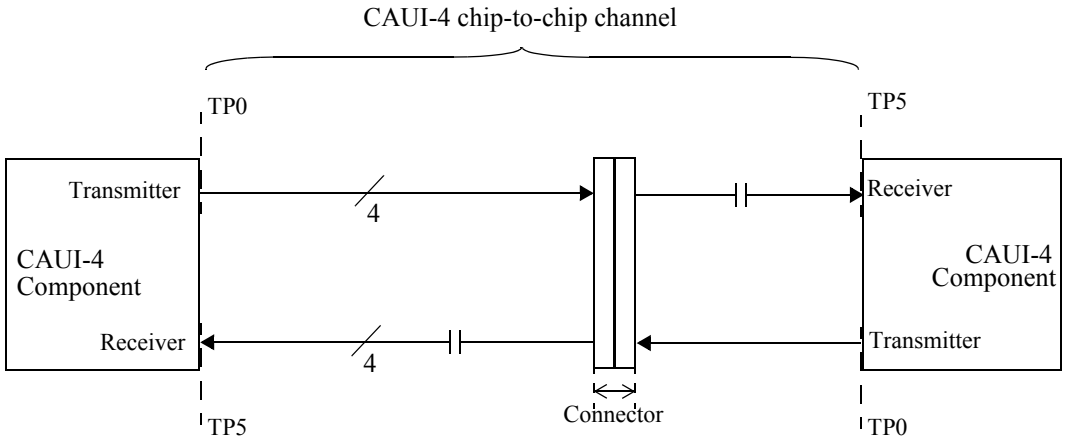


Figure 83D–2—Typical CAUI-4 chip-to-chip application

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower due to the channel ILD, return loss, and crosstalk.

$$Insertion\_loss(f) \le \left\{ \begin{array}{cc} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \le f < 12.89 \\ -17.851 + 2.936f & 12.89 \le f < 25.78 \end{array} \right\} \text{ (dB)} \qquad \text{(83D–1)}$$

where

f is the frequency in GHz
Insertion_loss(f) is the informative CAUI-4 chip-to-chip insertion loss

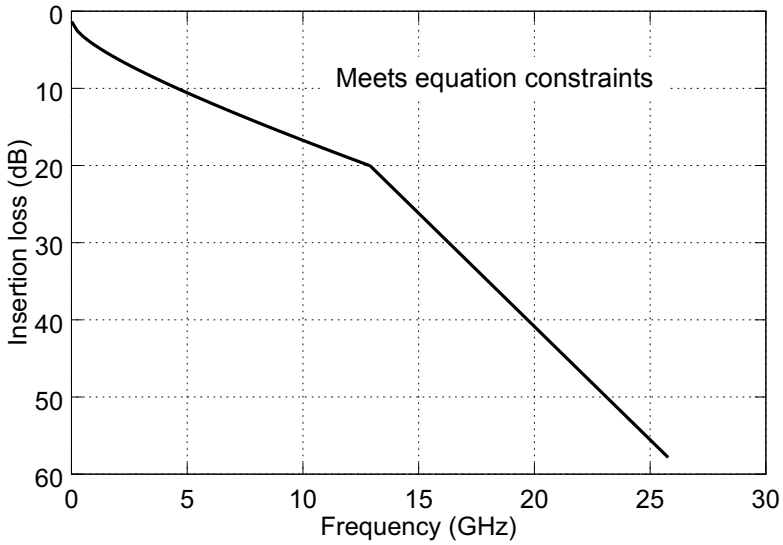


Figure 83D–3—CAUI-4 chip-to-chip channel insertion loss

83D.2 CAUI-4 chip-to-chip compliance point definition

The electrical characteristics for the CAUI-4 chip-to-chip interface are defined at compliance points for the transmitter (TP0a) and receiver (TP5a) respectively. The location of TP0a and electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93-5 and 93.8.1.1 respectively. The location of TP5a and electrical characteristics of the test fixture used to measure the receiver are defined in Figure 93-10 and 93.8.2.1 respectively.

83D.3 CAUI-4 chip-to-chip electrical characteristics

83D.3.1 CAUI-4 transmitter characteristics

A CAUI-4 chip-to-chip transmitter shall meet the specifications defined in Table 83D–1 if measured at TP0a. While the CAUI-4 chip-to-chip transmitter requirements are similar to those in Clause 93, they differ

Table 83D–1—CAUI-4 transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (range)	93.8.1.2	25.78125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
Common-mode AC output voltage (max, RMS)	93.8.1.3	12	mV
Differential output return loss (min)	93.8.1.4	Equation (93-3)	dB
Common-mode output return loss (min)	93.8.1.4	Equation (93-4)	dB
Output waveform[a] Steady state voltage v_f(max) Steady state voltage v_f(min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 93.8.1.5.2 93.8.1.5.2 93.8.1.5.2 83D.3.1.1 83D.3.1.1	 0.6 0.4 0.71 x v_f Table 83D–2 Table 83D–3	 V V V — —
Signal-to-noise-and-distortion ratio (min)	93.8.1.6	27	dB
Output Jitter (max) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak[b] Effective total uncorrelated jitter, peak-to-peak[bc]	92.8.3.9	 0.035 0.1 0.26	 UI UI UI

[a]The state of the transmit equalizer is controlled by management interface.
[b]Effective bounded uncorrelated jitter and effective total uncorrelated jitter are measured as defined in 92.8.3.9.2 except that the range for fitting $CDFL_i$ and $CDFR_i$, as defined in 92.8.3.9.2 c), shall be from 10^{-4} to 2.5 x 10^{-3}
[c]Effective total uncorrelated jitter, peak-to-peak is specified to a 10^{-15} probability

in that they do not assume transmitter training or a back-channel communications path. Also, the transmit output waveform is not manipulated via a PMD control function (see 93.7.12).

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

83D.3.1.1 Transmitter equalization settings

The CAUI-4 chip-to-chip transmitter includes programmable equalization to compensate for the frequency-dependent loss of the channel and to facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 83D–4. The transmitter output equalization is characterized using the linear fit method described in 93.8.1.5.1 where the state of the CAUI-4 transmit output is manipulated via management. The pre-cursor tap value c(–1) and the post-cursor tap value c(1) are controlled independently of each other. The pre-cursor equalization ratio R_{pre} for each pre-cursor tap setting is shown in Table 83D–2 where R_{pre} is defined to be (c(0)–(c(–1))/(c(0)+c(–1)) and the post-cursor tap setting c(1) is 0. The post-cursor equalization ratio R_{pst} for each post-cursor tap setting is shown in Table 83D–3 where R_{pst} is defined to be (c(0)–c(1))/(c(0)+c(1)) and the pre-cursor tap setting c(–1) is 0.

If a Clause 45 MDIO is implemented, the c(–1) and c(1) coefficients are accessible through registers 1.180 through 1.187 (see 45.2.1.92b through 45.2.1.92e).

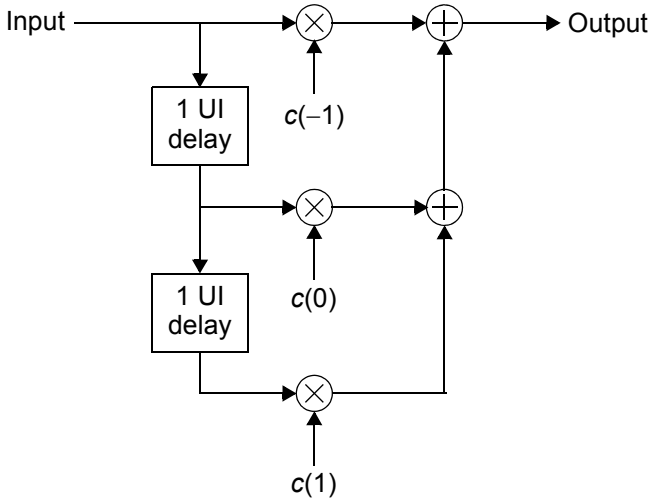


Figure 83D–4—Transmit equalizer functional model

.

Table 83D–2—Pre-cursor equalization

Pre-cursor equalization setting	Value
R_{pre} at tap setting 0	1 ±12.5%
R_{pre} at tap setting 1	1.11 ±12.5%
R_{pre} at tap setting 2	1.25 ±12.5%
R_{pre} at tap setting 3	1.43 ±12.5%

Table 83D–3—Post-cursor equalization

Post-cursor equalization setting	Value
R_{pst} at tap setting 0	1 ±12.5%
R_{pst} at tap setting 1	1.11 ±12.5%
R_{pst} at tap setting 2	1.25 ±12.5%
R_{pst} at tap setting 3	1.43 ±12.5%
R_{pst} at tap setting 4	1.67 ±12.5%
R_{pst} at tap setting 5	2 ±12.5%

83D.3.2 Optional EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78 and 78.3) then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI-4 shutdown.

If the EEE capability includes CAUI-4 shutdown (see 78.5.2) then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction CAUI-4 transmitter is disabled as specified below. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction CAUI-4 transmitter is disabled as specified below.

For EEE capability with CAUI-4 shutdown, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction. Furthermore, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction CAUI-4 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction CAUI-4 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in this section.

83D.3.3 CAUI-4 receiver characteristics

A CAUI-4 chip-to-chip receiver shall meet the specifications defined in Table 83D–4 if measured at TP5a.

Table 83D–4—CAUI-4 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	93.8.2.2	Equation (93-3)	dB
Differential to common mode input return loss	93.8.2.2	Equation (93-5)	dB
Interference tolerance	83D.3.3.1	Table 83D–5	—
Jitter tolerance[a]	93.8.2.4	Table 93-7	—

[a]When referencing 93.8.2.4 the following modifications are required: Test transmitter shown in Figure 93-12 meets 83D.3.1 specifications, test channel meets the requirements of the interference tolerance test channel using Test 2 values from Table 83D–5, bit error ratio better than 10^{-15} for the receiver jitter tolerance test.

83D.3.3.1 Receiver interference tolerance

The receiver shall satisfy the requirements for interference tolerance defined in Table 83D–5. The interference tolerance test uses the method described in Annex 93C as specified by 93.8.2.3, with the following exceptions:

a) The parameters in Table 83D–5 replace the parameters in Table 93-6.

b) The transmitter taps are set via management to the optimal transmitter equalizer settings described in 83D.3.1.1.

Table 83D–5—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Bit error ratio[ab]	—	10^{-15}	—	10^{-15}	—
Insertion loss at 12.89 GHz[c]	—	20	—	10	dB
Coefficients of fitted insertion loss[d] a_0 a_1 a_2 a_4	 -1 0 0 0	 2 2.937 1.599 0.03	 -1 0 0 0	 1 0.817 0.801 0.01	 dB dB/GHz$^{1/2}$ dB/GHz dB/GHz^2
RSS_DFE4	0.05	—	0.025	—	—
COM including effects of broadband noise	—	2	—	2	dB

[a]Bit error ratio replaces the RS symbol error ratio measurement in 93.8.2.3
[b]Maximum BER assumes errors are not correlated to ensure sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard
[c]Measured between TPt and TP5 (see Figure 93C-4)
[d]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with f_{min} = 0.05 GHz, and f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz

83D.3.4 Global energy detect function for optional EEE operation

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and CAUI-4 shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the CAUI-4 for the ingress direction SIGNAL_DETECT is set to FAIL following a transition from aui_rx_mode = DATA to aui_rx_mode = QUIET. When aui_rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input detects an ALERT signal driven from the CAUI-4 link partner. While aui_rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is applied to the channel.

83D.4 CAUI-4 chip-to-chip channel characteristics

The Channel Operating Margin (COM), computed using the procedure in Annex 93A and the parameters in Table 83D–6, shall be greater than or equal to 2 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization coefficients.

Table 83D–6—Channel Operating Margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended board capacitance	 C_d z_p z_p C_b	 2.5×10^{-4} 12 30 1.8×10^{-4}	 nF mm mm nF
Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain	g_{DC}	Table 83D–7	dB
Continuous time filter, zero frequency	f_z	Table 83D–7	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	Table 83D–7	GHz

Table 83D–6—Channel Operating Margin parameters *(continued)*

Parameter	Symbol	Value	Units
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 Av A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Level separation mismatch ratio	R_{LM}	1	
Transmitter signal-to-noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit, for n = 1 to N_b	$b_{max}(n)$	0.3	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_o	5.2×10^{-4}	V^2/GHz
Target detector error ratio	DER_0	10^{-15}	—

Table 83D–7—Reference CTLE coefficients

g_{DC}	f_{p1}	f_{p2}	f_z
-1	18.6	14.1	9.385
-2	18.6	14.1	8.937
-3	15.6	14.1	8.018
-4	15.6	14.1	7.861
-5	15.6	14.1	7.75
-6	15.6	14.1	7.67
-7	15.6	14.1	7.609
-8	15.6	14.1	7.566
-9	15.6	14.1	7.531
-10	15.6	14.1	7.503
-11	15.6	14.1	7.483
-12	15.6	14.1	7.466

83D.5 Protocol implementation conformance statement (PICS) proforma for Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)[8]

83D.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

83D.5.2 Identification

83D.5.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83D.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bm-201x, Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bm-201x.)	

Date of Statement	

[8]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

83D.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC coupled lanes	83D.1	Four independent data paths in each direction	M	Yes [ ]
*CHAN	Channel	83D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*LPI	Support for CAUI-4 shutdown	83D.3.2		O	Yes [ ] No [ ]

83D.5.4 PICS proforma tables for chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83D.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	83D.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	83D.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	83D.3.1	less than our equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	83D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output	83D.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	83D.3.1	Meets Equation (93-3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	83D.3.1	Meets Equation (93-4) constraints	M	Yes [ ]
TC8	Output wave form	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Amplitude and swing for CAUI-4 shutdown	83D.3.2		LPI:M	Yes [ ]
TC11	Transmit disable for CAUI-4 shutdown	83D.3.2		LPI:M	Yes [ ]

83D.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	93.8.2.2	Meets Equation (93-3) constraints	M	Yes [ ]
RC2	Differential to common mode input return loss	93.8.2.2	Meets Equation (93-5) constraints	M	Yes [ ]
RC3	Interference tolerance	83D.3.3.1	Satisfy requirements in Table 83D–5	M	Yes [ ]
RC4	Jitter Tolerance	93.8.2.4	Satisfy requirements in Table 93-7	M	Yes [ ]
RC5	Signal detect for CAUI-4 shutdown	83D.3.4		LPI:M	Yes [ ]

83D.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	83D.4	Greater than or equal to 2 dB	CHAN:M	Yes [ ]

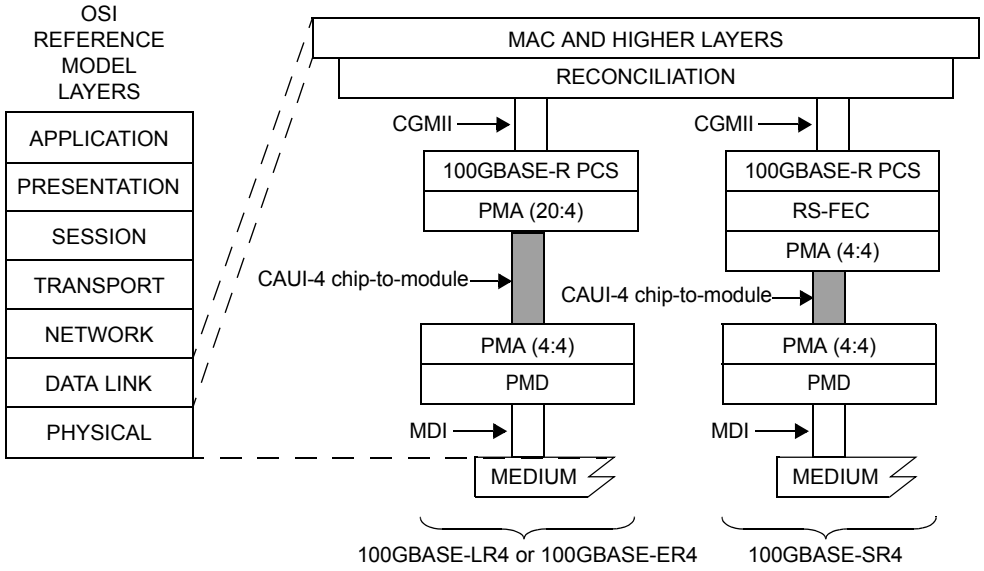
Annex 83E

(normative)

Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4). Figure 83E–1 shows the relationship of the CAUI-4 chip-to-module interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-module interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with pluggable module interfaces.



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83E–1—Example CAUI-4 chip-to-module relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model

The CAUI-4 link is described in terms of a host CAUI-4 component, a CAUI-4 channel with associated insertion loss, and a module CAUI-4 component. Figure 83E–2 and Equation (83E–1) depict a typical CAUI-4 application, and summarize the differential insertion loss budget associated with the chip-to-module application which is shown in Figure 83E–3. The CAUI-4 chip-to-module interface comprises independent data paths in each direction. Each data path contains four differential lanes which are AC coupled within the module. The nominal signaling rate for each lane is 25.78125 GBd. The chip-to-module interface is defined

using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [Bx1].

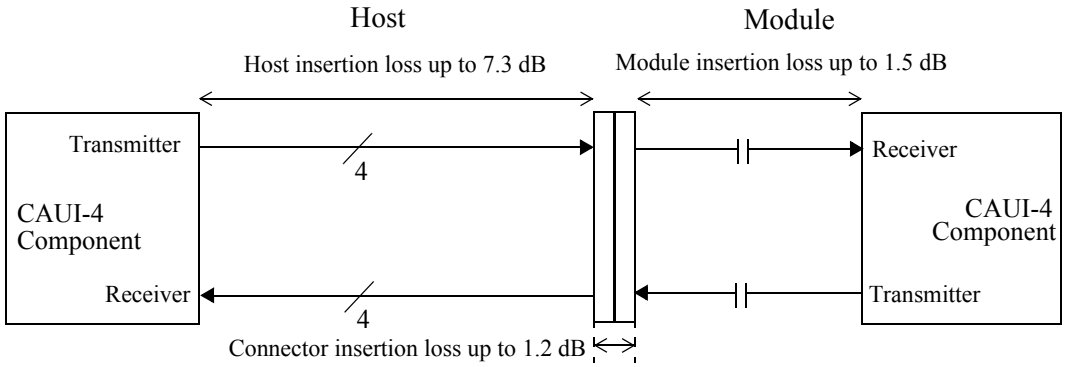


Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

$$Insertion\_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f < 18.75 \end{cases} \text{ (dB)} \qquad \text{(83E–1)}$$

where

f is the frequency in GHz
Insertion_loss(f) is the CAUI-4 chip-to-module insertion loss

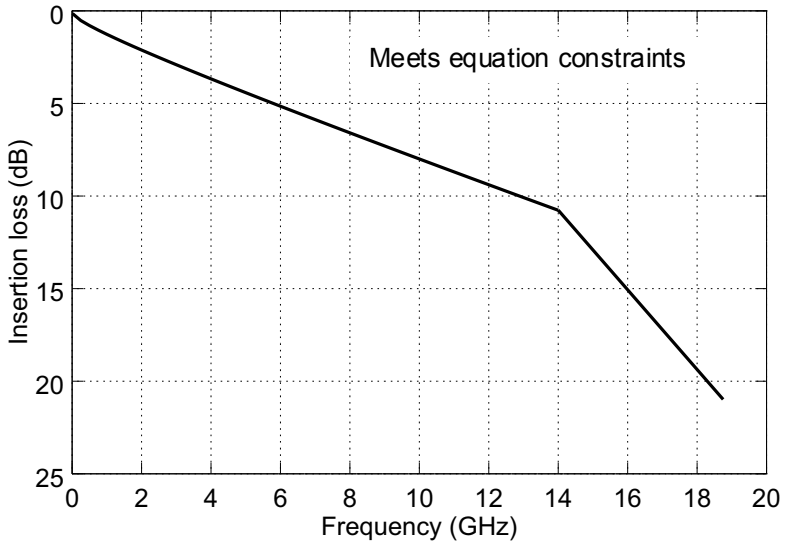


Figure 83E–3—CAUI-4 chip-to-module channel insertion loss

83E.2 CAUI-4 chip-to-module compliance point definitions

The electrical characteristics for the CAUI-4 chip-to-module interface are defined at compliance points for the Host and Module respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 83E–4 depicts the location of compliance points when measuring Host CAUI-4 compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. Similarly, the input of the HCB at TP4a is used to verify the host input compliance.

Figure 83E–5 depicts the location of compliance points when measuring Module CAUI-4 compliance. The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. Similarly, the input of the MCB at TP1 is used to verify the module input compliance. Additional details on the requirements for the MCB and HCB are given in 83E.4.1

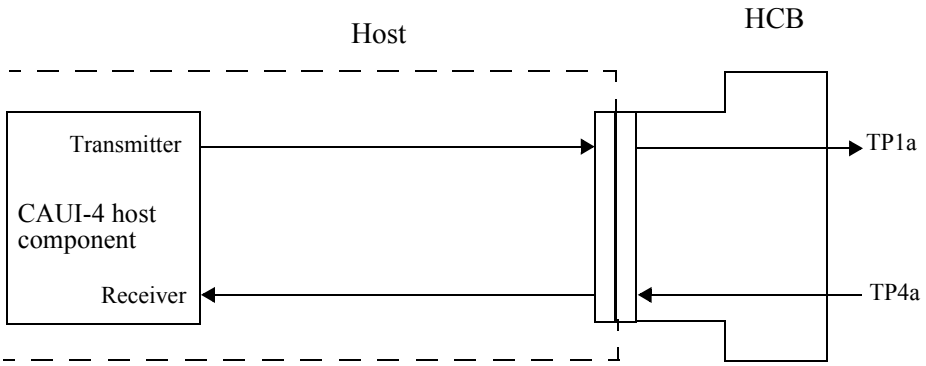


Figure 83E–4—Host CAUI-4 Compliance Points

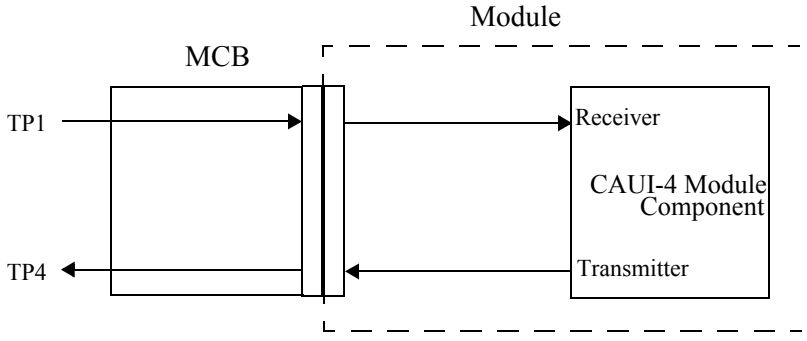


Figure 83E–5—Module CAUI-4 Compliance Points

83E.3 CAUI-4 chip-to-module electrical characteristics

83E.3.1 CAUI-4 host output characteristics

A CAUI-4 host output shall meet the specifications defined in Table 83E–1 if measured at TP1a.

Table 83E–1—CAUI-4 host output characteristics (at TP1a)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
DC common-mode output voltage (max)	83E.3.1.2	2.8	V
DC common-mode output voltage (min)	83E.3.1.2	–0.3	V
Single-ended output voltage (max)	83E.3.1.2	3.3	V
Single-ended output voltage (min)	83E.3.1.2	–0.4	V
Common-mode AC output voltage (max, RMS)	83E.3.1.2	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	83E.3.1.2	 35 900	mV
Eye width (min)	83E.3.1.6	0.46	UI
Eye height, differential (min)	83E.3.1.6	95	mV
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%)	83E.3.1.5	10	ps

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

83E.3.1.1 Signaling rate and range

The CAUI-4 signaling rate is 25.78125 GBd ± 100 ppm per lane. This translates to a nominal unit interval of 38.787879 ps.

83E.3.1.2 Signal levels

The peak-to-peak differential voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 83E–6.

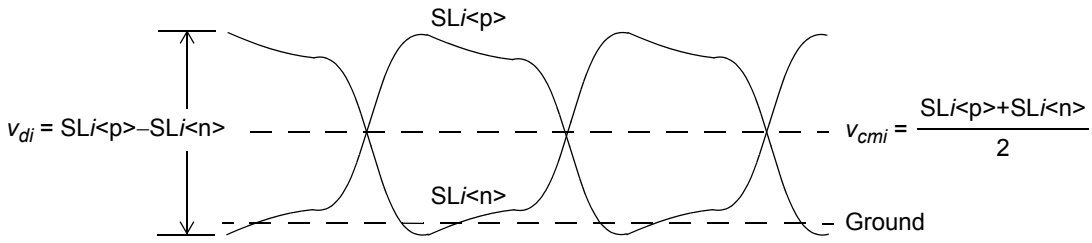


Figure 83E–6—Voltage definitions

The peak-to-peak differential output voltage is less than or equal to 900 mV. The peak-to-peak differential output voltage is less than or equal to 35 mV when the transmitter is disabled.

The DC common-mode output voltage is between –0.3 V and 2.8 V with respect to signal ground. The AC common-mode output voltage is less than or equal to 17.5 mV RMS with respect to signal ground.

83E.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (83E–2) and illustrated in Figure 83E–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$RLd(f) \geq \begin{Bmatrix} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{Bmatrix} \text{ (dB)} \qquad \text{(83E–2)}$$

where

f is the frequency in GHz
RLd is the CAUI-4 chip-to-module host output differential return loss

Common to differential output conversion return loss, in dB, of the output is shown in Equation (83E–3) and illustrated in Figure 83E–8

$$RLdc(f) \geq \begin{Bmatrix} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{Bmatrix} \text{ (dB)} \qquad \text{(83E–3)}$$

where

f is the frequency in GHz
RLdc is the CAUI-4 chip-to-module output common to differential mode conversion return loss

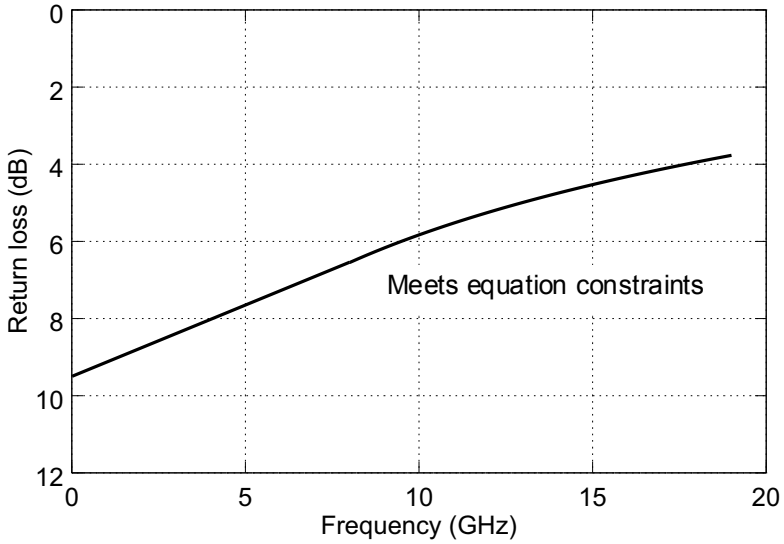


Figure 83E–7—Output differential return loss

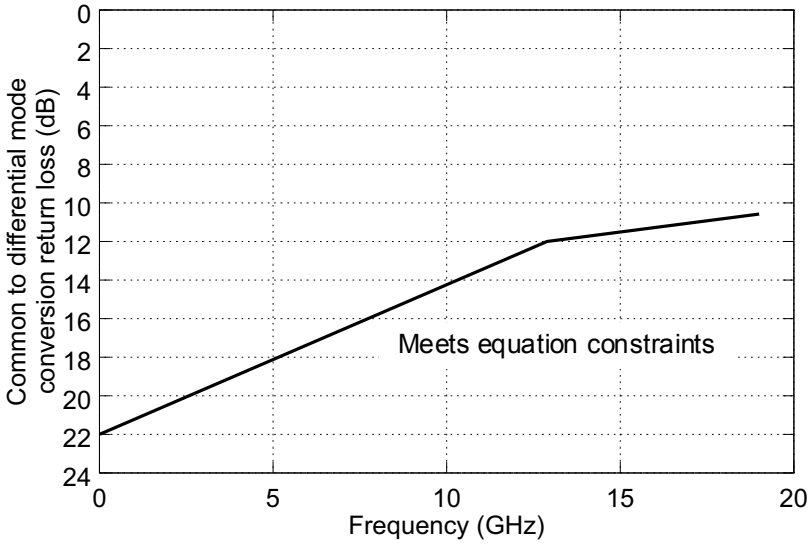


Figure 83E–8—Output common to differential mode conversion return loss

83E.3.1.4 Differential termination mismatch

Differential termination mismatch is defined in 86A.5.3.2.

83E.3.1.5 Transition time

The transition times (rise and fall times) are defined in 86A.5.3.3.

83E.3.1.6 Host output eye width and eye height

Host output eye width is greater than 0.46 UI. Host output eye height is greater than 95 mV. Figure 83E–9 depicts an example host output eye width and eye height test configuration. Host output eye width and eye height are measured at TP1a using compliance boards defined in 83E.2. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.1.6.1. The recommended CTLE peaking value is provided to the module via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.92a). Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP4 with target differential peak-to-peak amplitude of 900 mV and target transition time of 19 ps.

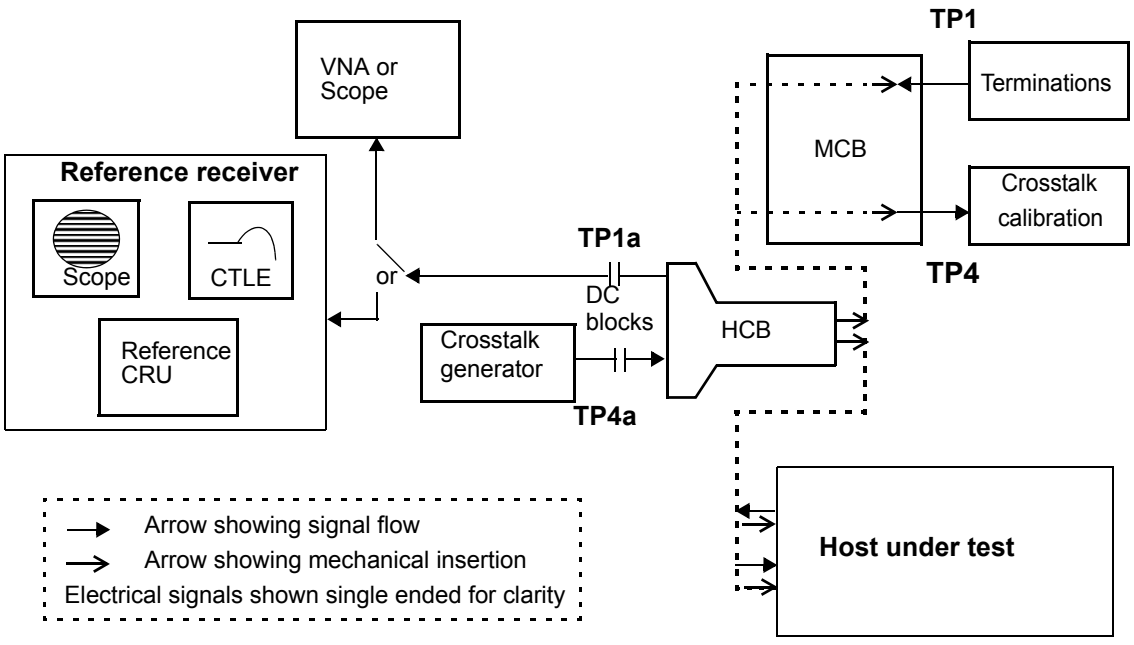


Figure 83E–9—Example host output test configuration

83E.3.1.6.1 Reference receiver for host output eye width and eye height evaluation

The reference receiver is used to measure host eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4) with coefficients given in Table 83E–2 and illustrated in Figure 83E–10. The equalizer may be implemented in software, however the measured signal is not averaged.

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)} \quad (83E–4)$$

where

$H(f)$	is the CTLE transfer function
G	is the CTLE gain
P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
j	is the square root of –1
f	is the frequency in GHz

Table 83E–2—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

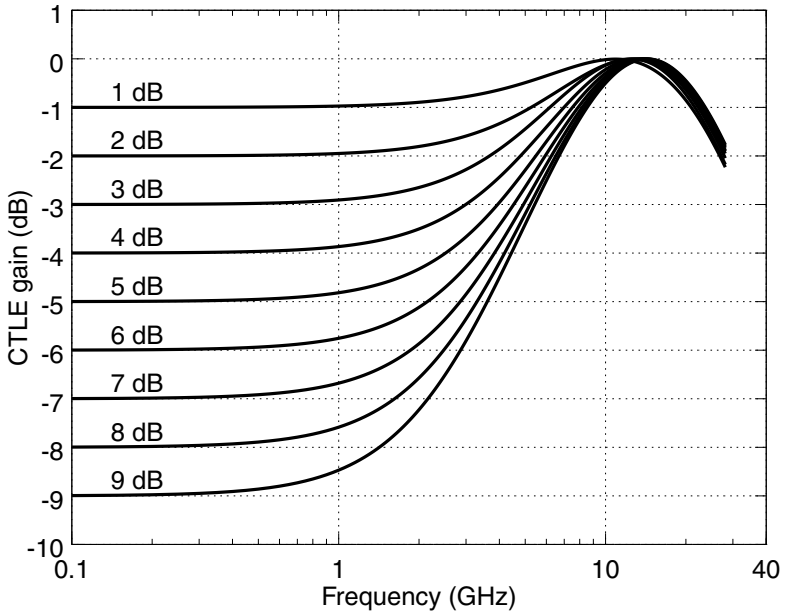


Figure 83E–10—Selectable continuous time linear equalizer (CTLE) characteristic

83E.3.2 CAUI-4 module output characteristics

A CAUI-4 module output shall meet the specifications defined in Table 83E–3 if measured at TP4. A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

Table 83E–3—CAUI-4 module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
Common-mode AC output voltage (max, RMS)	83E.3.1.2	17.5	mV
Differential output voltage (max)	83E.3.1.2	900	mV
Eye width (min)	83E.3.2.1	0.57	UI
Eye height, differential (min)	83E.3.2.1	228	mV
Vertical eye closure (max)	83E.4.2.1	5.5	dB
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E–3)	dB

Table 83E–3—CAUI-4 module output characteristics (at TP4) *(continued)*

Parameter	Reference	Value	Units
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%)	83E.3.1.5	9.5	ps
DC common mode voltage (min)[a]	83E.3.1.2	–350	mV
DC common mode voltage (max)[a]	83E.3.1.2	2850	mV

[a]DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

83E.3.2.1 Module output eye width and eye height

Module output eye width is greater than 0.57 UI. Module output eye height is greater than 228 mV. Figure 83E–11 depicts an example module output eye width and eye height test configuration. Module output eye width and eye height are measured at TP4 using compliance boards defined in 83E.2. The module output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.2.1.1. Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of 19 ps.

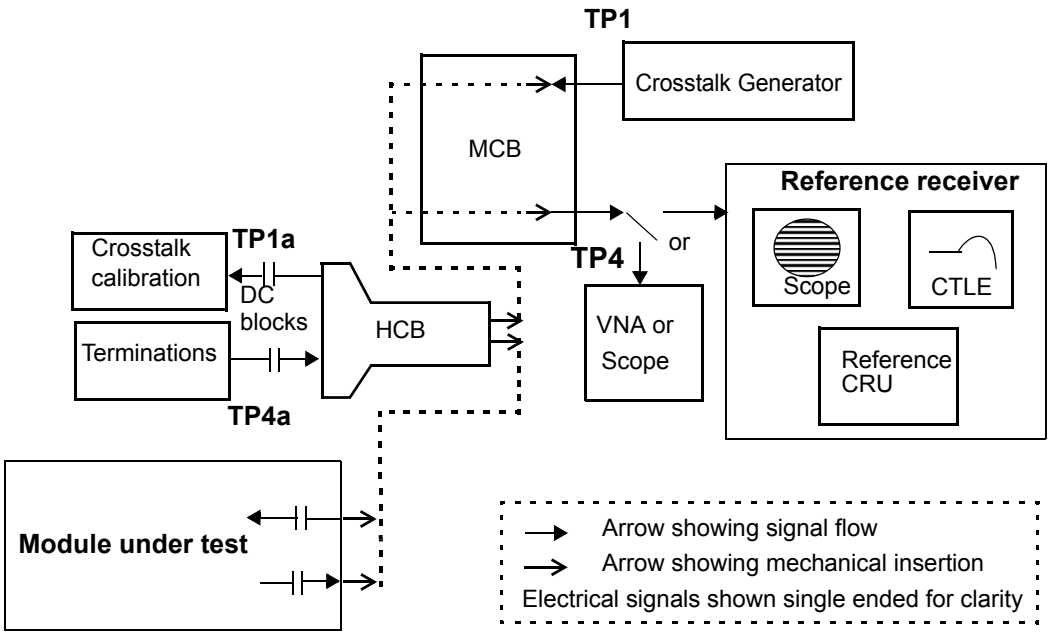


Figure 83E–11—Example module output test configuration

83E.3.2.1.1 Reference receiver for module output eye width and eye height evaluation

A reference receiver is used to measure module eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4) with coefficients given in the first two rows of Table 83E–2. The equalizer may be implemented in software, however the measured signal is not averaged. Either of the two equalizer settings may be used to meet the output eye width and eye height requirement.

83E.3.3 CAUI-4 host input characteristics

A CAUI-4 host input shall meet the specifications defined in Table 83E–4 if measured at the appropriate test point.

Table 83E–4—CAUI-4 host input characteristics

Parameter	Reference	Test Point	Value	Units
Bit error ratio (max)[a]	83E.3.3.1	TP4a	10^{-15}	
Signaling rate, per lane (range)	83E.3.1.1	TP4a	25.78125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	83E.3.1.2	TP4	900	mV
Differential input return loss (min)	83E.3.3.2	TP4a	Equation (83E–5)	dB
Differential to common mode input return loss (min)	83E.3.3.2	TP4a	Equation (83E–6)	dB
Host stressed input test	83E.3.3.3	TP4	See 83E.3.3.3	
Differential termination mismatch (max)	83E.3.1.4	TP4a	10	%
Common Mode Voltage[b] Min Max	83E.3.1.2	TP4a	 –0.3 2.8	V

[a]Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard.
[b]Generated by host, referred to host ground.

83E.3.3.1 Input bit error ratio

The CAUI-4 chip-to-module host input is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.3.3.

83E.3.3.2 Input return loss

The differential input return loss, in dB, of the input is shown in Equation (83E–5) and illustrated in Figure 83E–12. The reference impedance for differential return loss measurements is 100 Ω.

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(83E–5)}$$

where

f is the frequency in GHz
RLd is the CAUI-4 chip-to-module input differential return loss

Differential to common mode input return loss, in dB, of the input is shown in Equation (83E–6) and illustrated in Figure 83E–13.

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(83E–6)}$$

where

f is the frequency in GHz
$RLcd$ is the CAUI-4 chip-to-module input differential to common mode input return loss

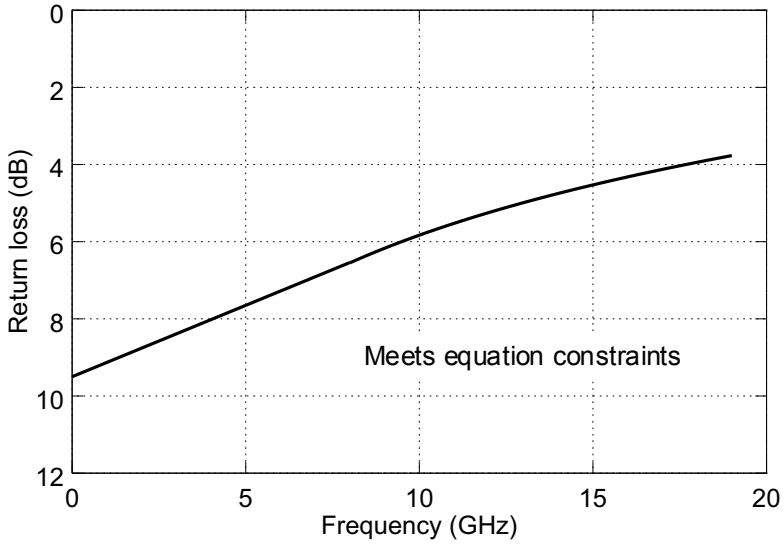


Figure 83E–12—Differential input return loss

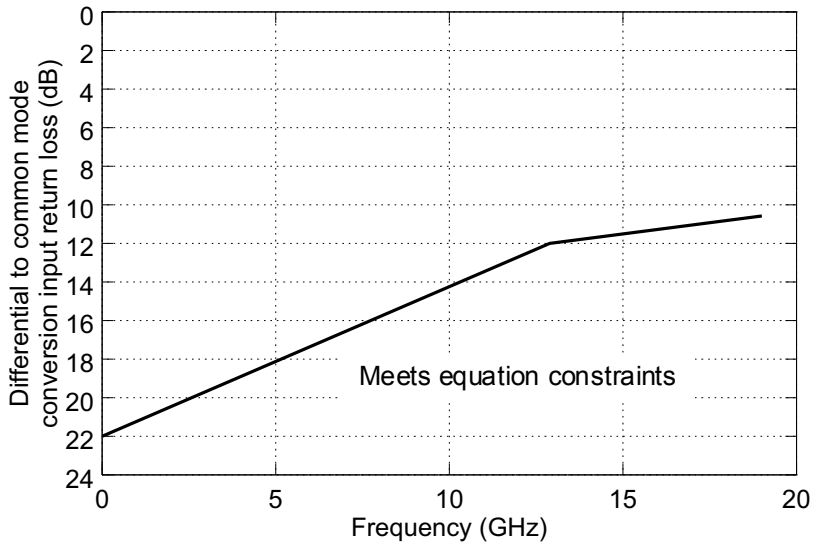


Figure 83E–13—Differential to common mode conversion input return loss

83E.3.3.3 Host stressed input test

The host stressed input tolerance is measured using the procedure defined in 83E.3.3.3.1. The input shall satisfy the input tolerance defined in Table 83E–5.

Table 83E–5—Host stressed input parameters

Parameter	Value
Eye width	0.57 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye height	228 mV

83E.3.3.3.1 Host stressed input test procedure

The host stressed input test is summarized in Figure 83E–14. The stress signal is applied at TP4a, and is calibrated at TP4. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 (PRBS9, see Table 86-11). The reference receiver includes a selectable software CTLE given by Equation (83E–4) and the first two rows of Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern. The amount of applied peak-to-peak sinusoidal jitter used for the host stressed input test is given in Table 83E–5. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS11. The data rate should be approximately $1/10^{th}$ of the stressed pattern data rate (2.578 GBd). The clock source for the PRBS

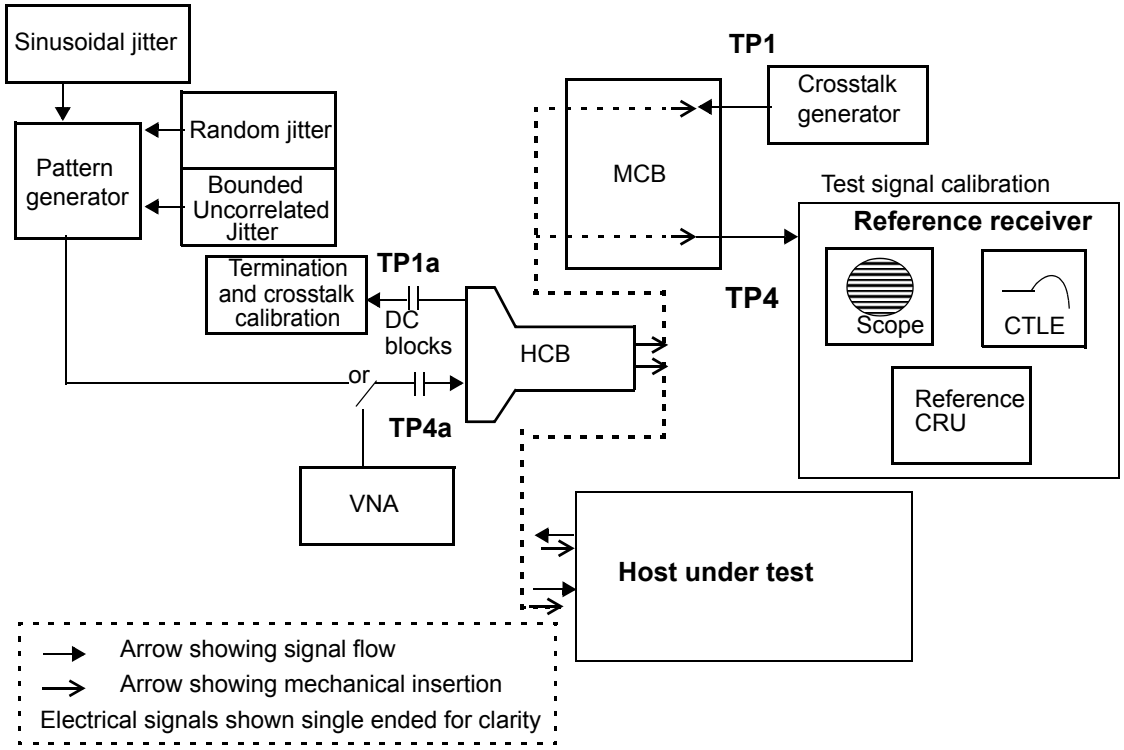


Figure 83E–14—Example host stressed input test

generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–6. The target pattern generator 20% to 80% transition in the host stressed input test is 9.5 ps.

Table 83E–6—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total jitter at BER of 10^{-15}
[b]Random jitter at BER of 10^{-15}
[c]As defined in 92.8.3.10.1

The counter propagating crosstalk channels during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 19 ps as measured at TP1a. The crosstalk signal is calibrated with Pattern 4 (PRBS9, see Table 86-11). The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the stressed input test. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least

31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

Eye height and eye width are then measured at TP4 using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude is adjusted to result in the eye height and eye width given in Table 83E–5 using the reference receiver.

A host input test signal should have a vertical eye closure in the range of 4.5 dB to 5.5 dB with a target value of 5 dB.

The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the input test which is conducted by inserting the HCB into the host under test.

83E.3.4 CAUI-4 module input characteristics

A CAUI-4 module input shall meet the specifications defined in Table 83E–7 if measured at the appropriate test point.

Table 83E–7—CAUI-4 module input characteristics

Parameter	Reference	Test Point	Value	Units
Bit error ratio (max)[a]	83E.3.4.1	TP1	10^{-15}	
Signaling rate per lane (range)	83E.3.1.1	TP1	25.78125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	83E.3.1.2	TP1a	900	mV
Differential input return loss (min)	83E.3.3.2	TP1	Equation (83E–5)	dB
Differential to common mode input return loss (min)	83E.3.3.2	TP1	Equation (83E–6)	dB
Differential termination mismatch (max)	83E.3.1.4	TP1	10	%
Module stressed input test	83E.3.4.2	TP1a	See 83E.3.4.2	
Single-ended voltage tolerance (min)	83E.3.1.2	TP1a	–0.4	V
Single-ended voltage tolerance (max)	83E.3.1.2	TP1a	3.3	V
DC common mode voltage (min)[b]	83E.3.1.2	TP1	–350	mV
DC common mode voltage (max)[b]	83E.3.1.2	TP1	2850	mV

[a]Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard.
[b]DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

83E.3.4.1 Input bit error ratio

The CAUI-4 module input is defined to operate at a bit error ratio (BER) better than 10^{-15} for an input signal defined by 83E.3.4.2.

83E.3.4.2 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 83E.3.4.2.1. The input shall satisfy the input tolerance defined in Table 83E–8.

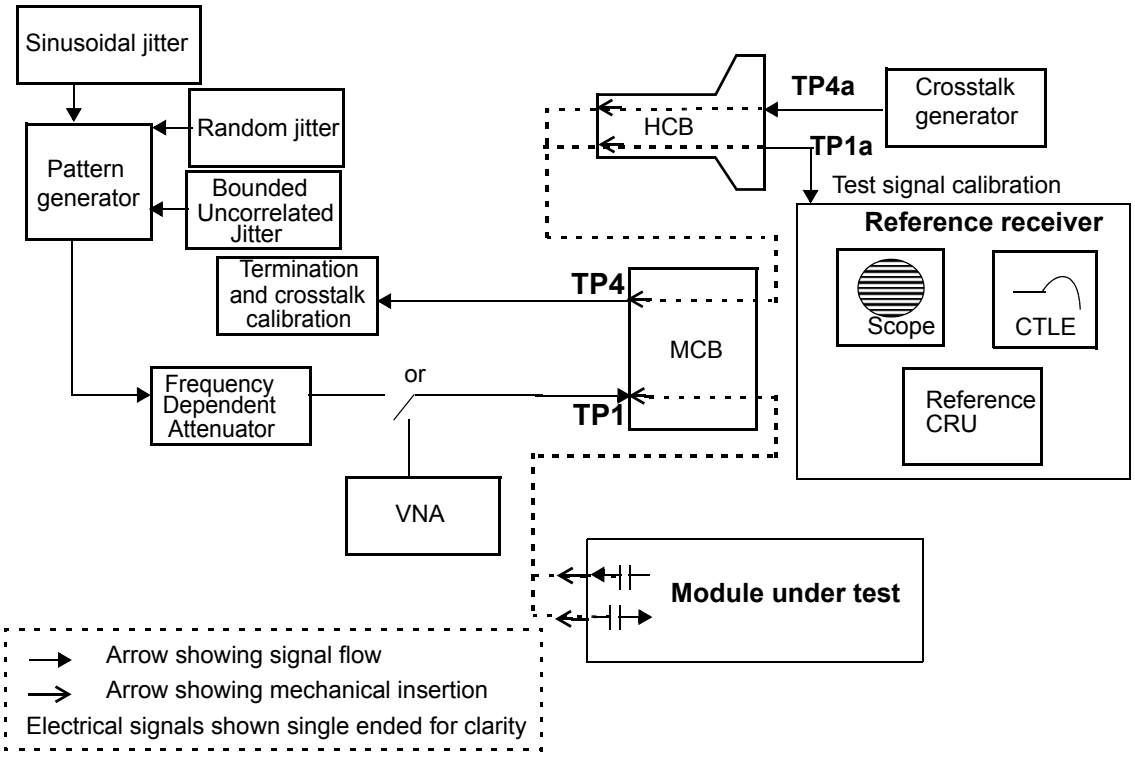


Figure 83E–15—Example module stressed input test

Table 83E–8—Module stressed input parameters

Parameter	Value
Eye width	0.46 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye height	95 mV

83E.3.4.2.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 83E–15. The stress signal is applied at TP1, and is calibrated at TP1a. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 (PRBS9, see Table 86-11). The reference receiver includes a selectable software CTLE given by Equation (83E–4) and Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel, and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 83E–8. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all

stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS11. The data rate should be approximately $1/10^{th}$ of the stressed pattern data rate (2.578 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–9. The target pattern generator 20% to 80% transition in the module stressed input test is 9.5 ps. The return loss of the test system as measured at TP1 meets the specification given in Equation (83E–2).

Table 83E–9—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total jitter at BER of 10^{-15}
[b]Random jitter at BER of 10^{-15}
[c]As defined in 92.8.3.10.1

The counter propagating crosstalk channels during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 19 ps as measured at TP4. The crosstalk signal is calibrated with Pattern 4 (PRBS9, see Table 86-11). The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the stressed input test. Patterns 3 and 5 are described in Table 86-11. For the case of Pattern 3, with at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes being active during the stressed input test.

Two levels of frequency dependent attenuation are used for the module stressed input test: high loss, and low loss. For the high loss case, frequency dependent attenuation is added such that from the output of the pattern generator to TP1a is 10.25 dB loss at 12.89 GHz. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. For the low loss case, discrete frequency dependent attenuation is removed such that from the output of the pattern generator to TP1a comprises the mated HCB/MCB pair as described in 83E.4.1. Eye height and eye width are then measured at TP1a using the setting of the software CTLE which maximizes the product of eye height and eye width based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted to result in the eye height and eye width given in Table 83E–8 using the reference receiver. In both the low loss and high loss cases, the module under test is provided with the reference CTLE setting used to meet eye width and eye height requirements via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.169 (see 45.2.1.92a). The module under test is evaluated with three *Recommended_CTLE_value* values for both the high loss test and low loss test. These are: a) the CTLE setting used to meet eye width and eye height requirements, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2.

The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the input test which is conducted by inserting the module into the MCB.

83E.4 CAUI-4 measurement methodology

This subclause describes common measurement tools and methodologies to be used for the CAUI-4 chip-to-module interface. Details of HCB and MCB characteristics are given in 83E.4.1 and details of the eye diagram measurement methodology are given in 83E.4.2.

83E.4.1 HCB / MCB characteristics

HCB characteristics are described in 92.11.1 where the HCB performs the equivalent function as the TP2 or TP3 test fixture. The MCB characteristics are described in 92.11.2 where the MCB performs the equivalent functionality as the cable assembly test fixture.

83E.4.2 Eye width and eye height measurement method

Eye diagrams in CAUI-4 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is Pattern 4 (PRBS9, see Table 86-11). The following procedure should be used to obtain eye height and eye width parameters:

1) Capture Pattern 4 using a clock recovery unit with a corner frequency of 10 MHz and slope of 20 dB/decade and a minimum sampling rate of 3 samples per bit. Collect sufficient samples equivalent to at least 4 million bits to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-6} without extrapolation.
2) Apply the reference receiver including the appropriate CTLE to the captured signal. For modules, any single CTLE setting as described in 83E.3.2.1.1 which meets both eye width and eye height requirements is acceptable. For host compliance, the CTLE peaking in the reference receiver shall be set to one of three values. These are: a) the recommended CTLE peaking value provided by the host, b) the value 1 dB higher if present in Table 83E–2, c) the value 1 dB lower if present in Table 83E–2. Any of the three CTLE settings that meets both eye width and eye height defined in Table 83E–1 is acceptable.
3) Use the differential equalized signal from step 2 to construct the CDF of the jitter zero crossing for both the left edge (CDFL) and right edge (CDFR), as a distance from the center of the eye. Calculate the eye width (EW6) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits. For a pattern with 50% transition density the maximum value for the CDFL and CDFR will be 0.5. The CDFL and CDFR are equivalent to bath tub curves where the BER is plotted versus sampling time.
4) Leveraging the Dual-Dirac jitter model described in 48B.1.1, estimate the random jitter. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDFL and CDFR to yield the random jitter on the left edge (RJL) and the random jitter on the right edge (RJR) respectively. The eye width is then given by Equation (83E–7)

$$EW15 = EW6 - 3.19 \times (RJR + RJL) \quad (83E–7)$$

where

$EW15$	is the eye width extrapolated to 10^{-15} probability
$EW6$	is the eye width at 10^{-6} probability
RJL	is the RMS value of the jitter estimated from CDFL

RJR is the RMS value of the jitter estimated from the CDFR

5) Use the differential equalized signal from step 2 to construct the CDF of the signal voltage in the central 5% of the eye, for both logic 1 (CDF1) and logic 0 (CDF0), as a distance from the center of the eye. Calculate the eye height (EH6) as the difference in voltage between CDF1 and CDF0 with a value of 10^{-6}. CDF0 and CDF1 are calculated as the cumulative sum of histograms of the voltage at the top and bottom of the eye normalized by the total number of sampled bits. For a well balanced number of ones and zeros the maximum value for CDF0 and CDF1 will be 0.5.

6) Apply the Dual-Dirac and tail fitting techniques to CDF1 and CDF0 to estimate the noise at the middle of the eye. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} and 10^{-6} of CDF1 and CDF0 to yield relative noise one (RN1) and relative noise zero (RN0). The eye height is then given by Equation (83E–8)

$$EH15 = EH6 - 3.19 \times (RN0 + RN1) \quad (83E–8)$$

where

*EH*15 is the eye height extrapolated to 10^{-15} probability
*EH*6 is the eye height at 10^{-6} probability
*RN*1 is the RMS value of the noise estimated from CDF1
*RN*0 is the RMS value of the noise estimated from CDF0

83E.4.2.1 Vertical eye closure

Vertical eye closure is calculated using Equation (83E–9)

$$VEC = 20\log\left(\frac{AV}{EH15}\right) \quad (83E–9)$$

where

VEC is vertical eye closure in dB
AV is the eye amplitude of the equalized waveform. Eye amplitude is defined as the mean value of logic one minus the mean value of logic zero in the central 5% of the eye
*EH*15 is given in equation Equation (83E–8)

83E.5 Protocol implementation conformance statement (PICS) proforma for Annex 83E, Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)[9]

83E.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 83E, Chip-to-module four-lane 100 Gb/s Attachment Unit Interface (CAUI-4), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

83E.5.2 Identification

83E.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83E.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bm-201x, Annex 83E, Chip-to-module four-lane 100 Gb/s Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bm-201x.)	

Date of Statement	

[9]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

83E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC coupled lanes	83E.1	Four independent data paths in each direction	M	Yes [ ]

83E.5.4 PICS proforma tables for chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	83E.3.1.2	less than our equal to 35 mV	M	Yes [ ]
TH4	DC common-mode voltage	83E.3.1.2	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output	83E.3.1.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	83E.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	83E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	83E.3.1.6	0.46 UI	M	Yes [ ]
TH12	Eye height	83E.3.1.6	95 mV	M	Yes [ ]
TH13	Crosstalk source	83E.3.1.6	Asynchronous crosstalk source using Pattern 5, Pattern 3 or valid 100GBASE-R signal	M	Yes [ ]

83E.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output	83E.3.1.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	83E.3.1.4	Less than 10%	M	Yes [ ]
TM8	Transition time	83E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TM9	Eye width	83E.3.1.6	0.57 UI	M	Yes [ ]
TM10	Eye height	83E.3.1.6	228 mV	M	Yes [ ]
TM11	Crosstalk source	83E.3.1.6	Asynchronous crosstalk source using Pattern 5, Pattern 3 or valid 100GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	83E.4.2.1	5.5 dB (max)	M	Yes [ ]

83E.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	BER	83E.3.3.1	10^{-15}	M	Yes [ ]
RH2	Differential input return loss	83E.3.3.2	Equation (83E–5)	M	Yes [ ]
RM3	Reference impedance for input return loss	83E.3.3.2	100 Ω.	M	Yes [ ]
RH4	Differential to common mode input return loss	83E.3.3.2	Equation (83E–6)	M	Yes [ ]
RH5	Stressed input test	83E.3.3.3	Satisfy requirements in Table 83E–5	M	Yes [ ]

83E.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	BER	83E.3.3.1	10^{-15}	M	Yes [ ]
RM2	Differential input return loss	83E.3.3.2	Equation (83E–5)	M	Yes [ ]
RM3	Reference impedance for input return loss	83E.3.3.2	100 Ω.	M	Yes [ ]
RM4	Differential to common mode input return loss	83E.3.3.2	Equation (83E–6)	M	Yes [ ]
RM5	Stressed input test	83E.3.4.2	Satisfy requirements in Table 83E–8	M	Yes [ ]

Annex 93A

(normative)

Specification methods for electrical channels

93A.1 Channel Operating Margin

Change Table 93A-2 (as inserted by IEEE Std 802.3bj-201x) as follows:

Table 93A–2—Physical Layer specifications that employ COM

Physical Layer	Parameter values
100GBASE-KR4 (Clause 93)	Table 93-8
100GBASE-KP4 (Clause 94)	Table 94-17
CAUI-4 (Annex 83D)	Table 83D–6