Information technology —
Telecommunications and information exchange between systems —
Local and metropolitan networks — specific requirements
Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications —

Amendment: Physical Layer and Management Parameters for 10 Gb/s Operation — Type 10GBASE-T

Sponsor

LAN MAN Standards Committee
of the
IEEE Computer Society

This Draft amendment to IEEE Std. 802.3 provides support to extend 10 Gb/s operation over ISO/IEC 11801:2002 Class E and Class F channels with a new Physical Layer (PHY) device. The PHY is known as 10GBASE-T. This draft D1.2 is being circulated as part of Task Force Ballot. The formal expiration date of this draft is January 29, 2005.

Revisions to IEEE P802.3REVam, Clause 1

EDITORIAL NOTES - This revision is based on the current edition of IEEE P802.3REVam. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

1.3 Normative references

Insert the following normative reference in alphabetic order.

TBD

1.4 Definitions

Insert the following definition in alphabetic order:

1.4.xxx 10GBASE-T: IEEE 802.3 Physical Layer specification for a 10 Gb/s LAN using four pairs of Class E or Class F balanced copper cabling. (See IEEE 802.3 Clause 55.)

1.4.xxx DSQ128: A 128 point double square (DSQ) constellation mapping is used in 10GBASE-T. This constellation can be obtained by taking a 2D constellation with 16-level pulse amplitude modulation (PAM16) on each dimension and eliminating half the points to create a checker board pattern. (See IEEE 802.3 Clause 55.)

1.4.xxx 64B/65B transmission code: A 64-bit block that is scrambled and prepended with a single bit to indicate whether the block contains data only or a mix of data and control information. (See IEEE 802.3 Clause 55.)

1.4.xxx LDPC(1723,2048) frame: 64B/65B transmission code blocks mapped into a low density parity check (LDPC) frame with 1723 coded bits, 325 check bits and 1536 uncoded bits. (See IEEE 802.3 Clause 55).

Change the following definitions to include reference to Clause 55:

1.4.xxx Physical Coding Sublayer (PCS): Within IEEE 802.3, a sublayer used in certain port types to couple the Media Independent Interface (MII), Gigabit Media Independent Interface (GMII) or 10 Gigabit Media Independent Interface (XGMII) and the Physical Medium Attachment (PMA). The PCS contains the functions to encode data bits for transmission via the PMA and to decode the received conditioned signal from the PMA. There are several PCS structures. (For example see IEEE 802.3 Clauses 23, 24, 32, 36, 40, 48, ~~and~~ 49, and 55.)

1.4.xxx Physical Layer entity (PHY): Within IEEE 802.3, the portion of the Physical Layer between the Medium Dependent Interface (MDI) and the Media Independent Interface (MII), Gigabit Media Independent Interface (GMII) or 10 Gigabit Media Independent Interface (XGMII), consisting of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and, if present, the WAN Interface Sublayer

(WIS) and Physical Medium Dependent (PMD) sublayers. The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium. (For example see IEEE 802.3 Clauses 23–26, 32, 36, 40, 48-54, 55, 58-63, 65 and 66.)

1.4.xxx Physical Medium Attachment (PMA) sublayer: Within 802.3, that portion of the Physical Layer that contains the functions for transmission, reception, and (depending on the PHY) collision detection, clock recovery and skew alignment. (For example see IEEE 802.3, Clauses 7, 12, 14, 16, 17, 18, 23, 24, 32, 36, 40, 51, 55, 62, 63 and 66.)

1.5 Abbreviations

Insert the following abbreviations in alphabetic order:

CAT6	Category 6 balanced cabling
DSQ	double square
LDPC	low density parity check

Revisions to ANSI/IEEE Std 802.3, 2002, Clause 28

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 1.0, September 2004	First draft for IEEE P802.3an Task Force review.
Draft 1.1, October 2004	Second draft for IEEE P802.3an Task Force review.
Draft 1.2, December 2004	Third draft for IEEE P802.3an Task Force review.

28. Physical Layer link signaling for 10 Mb/s, 100 Mb/s, ~~and~~ 1000 Mb/s, and 10Gb/s Auto-Negotiation on twisted pair

Change title of Clause to include 10Gbps

28.1 Overview

28.1.1 Scope

Clause 28 describes the Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. The normative definitions for all extensions to Auto-Negotiation and all related register assignments for this standard are documented in .

The objective of the Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-Negotiation is performed using a modified 10BASE-T link integrity test pulse sequence, such that no packet or upper layer protocol overhead is added to the network devices (see Figure 28–1). Auto-Negotiation does not test the link segment characteristics (see 28.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10BASE-T, 100BASE-TX, and 100BASE-T4 compatible devices to be recognized, even though they may not provide Auto-Negotiation.

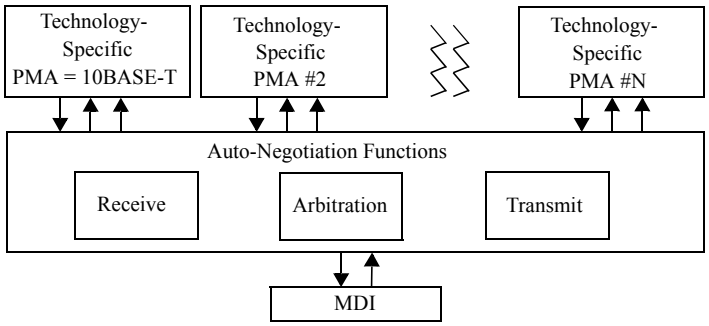


Figure 28–1—High-level model

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse (Figure 14–12). This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst. Each device capable of Auto-Negotiation issues FLP Bursts at power up, on command from management, or due to user interaction. The FLP Burst consists of a series of link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word that identifies

the operational modes supported by the remote device, as well as some information used for the Auto-Negotiation function's handshake mechanism.

To maintain interoperability with existing 10BASE-T devices, the function also supports the reception of 10BASE-T compliant link integrity test pulses. 10BASE-T link pulse activity is referred to as the Normal Link Pulse (NLP) sequence and is defined in 14.2.1.1. A device that fails to respond to the FLP Burst sequence by returning only the NLP sequence is treated as a 10BASE-T compatible device.

28.1.2 Application perspective/objectives

The Auto-Negotiation function is designed to be expandable and allow IEEE 802.3 compatible devices using an eight-pin modular connector to self-configure a jointly compatible operating mode. Implementation of the Auto-Negotiation function is optional. However, it is highly recommended that this method alone be utilized to perform the negotiation of the link operation.

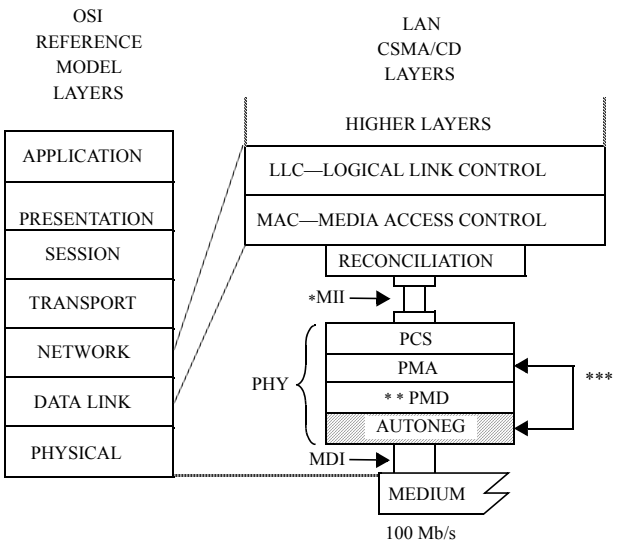
The following are the objectives of Auto-Negotiation:

a) Must interoperate with the IEEE 802.3 10BASE-T installed base.
b) Must allow automatic upgrade from the 10BASE-T mode to the desired "High-Performance Mode."
c) Requires that the 10BASE-T data service is the Lowest Common Denominator (LCD) that can be resolved. A 10BASE-T PMA is not required to be implemented, however. Only the NLP Receive Link Integrity Test function is required.
d) Reasonable and cost-effective to implement.
e) Must provide a sufficiently extensible code space to
    1) Meet existing and future requirements.
    2) Allow simple extension without impacting the installed base.
    3) Accommodate remote fault signals.
    4) Accommodate link partner ability detection.
f) Must allow manual or Network Management configuration to override the Auto-Negotiation.
g) Must be capable of operation in the absence of Network Management.
h) Must not preclude the ability to negotiate "back" to the 10BASE-T operational mode.
i) Must operate when
    1) The link is initially electrically connected.
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
j) The Auto-Negotiation function may be enabled by automatic, manual, or Network Management intervention.
k) Completes the base page Auto-Negotiation function in a bounded time period.
l) Will provide the basis for the link establishment process in future CSMA/CD compatible LAN standards that use an eight-pin modular connector.
m) Must not cause corruption of IEEE 802.3 Layer Management statistics.
n) Operates using a peer-to-peer exchange of information with no requirement for a master device (not master-slave).
o) Must be robust in the UTP cable noise environment.
p) Must not significantly impact EMI/RFI emissions.

28.1.3 Relationship to ISO/IEC 8802-3

The Auto-Negotiation function is provided at the Physical Layer of the OSI reference model as shown in Figure 28–2. Devices that support multiple modes of operation may advertise this fact using this function. The actual transfer of information of ability is observable only at the MDI or on the medium. Auto-Negotiation signaling does not occur across either the AUI or MII. Control of the Auto-Negotiation function may be supported through the Management Interface of the MII or equivalent. If an explicit embodiment of the MII is supported, the control and status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 28.2.4. If a physical embodiment of the MII manage-

ment is not present, then it is strongly recommended that the implementation provide control and status mechanisms equivalent to those described in Clause 22 and 28.2.4 for manual and/or management interaction.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
*** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.

Figure 28–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

28.1.4 Compatibility considerations

The Auto-Negotiation function is designed to be completely backwards compatible and interoperable with 10BASE-T compliant devices. In order to achieve this, a device supporting the Auto-Negotiation function must provide the NLP Receive Link Integrity Test function as defined in Figure 28–18. The Auto-Negotiation function also supports connection to 100BASE-TX and 100BASE-T4 devices without Auto-Negotiation through the Parallel Detection function. Connection to technologies other than 10BASE-T, 100BASE-TX, or 100BASE-T4 that do not incorporate Auto-Negotiation is not supported.

Implementation of the Auto-Negotiation function is optional. For CSMA/CD compatible devices that use the eight-pin modular connector of ISO/IEC 8877: 1992 and that also encompass multiple operational modes, if a signaling method is used to automatically configure the preferred mode of operation, then the Auto-Negotiation function shall be used in compliance with Clause 28. If the device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities, the device shall implement the Auto-Negotiation function as administered by this specification. All future CSMA/CD implementations that use an eight-pin modular connector shall be interoperable with devices supporting Clause 28. If the implementor of a non-CSMA/CD eight-pin modular device wishes to assure that its operation does not conflict with CSMA/CD devices, then adherence to Clause 28 is recommended.

While this Auto-Negotiation function must be implemented in CSMA/CD compatible devices that utilize the eight-pin modular connector, encompass multiple operational modes, and offer an Auto-Negotiation mechanism, the use of this function does not mandate that the 10BASE-T packet data communication service must exist. A device that employs this function must support the 10BASE-T Link Integrity Test function through the NLP Receive Link Integrity Test state diagram. The device may also need to support other technology-dependent link test functions depending on the modes supported. Auto-Negotiation does not perform cable tests, such as detect number of conductor pairs (if more than two pairs are required) or cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring CRC or framing errors) to determine if the link segment is adequate.

28.1.4.1 Interoperability with existing 10BASE-T devices

During Auto-Negotiation, FLP Bursts separated by 16 ± 8 ms are transmitted. The FLP Burst itself is a series of pulses separated by 62.5 ± 7 μs. The timing of FLP Bursts will cause a 10BASE-T device that is in the LINK TEST PASS state to remain in the LINK TEST PASS state while receiving FLP Bursts. An Auto-Negotiation able device must recognize the NLP sequence from a 10BASE-T Link Partner, cease transmission of FLP Bursts, and enable the 10BASE-T PMA, if present. If the NLP sequence is detected and if the Auto-Negotiation able device does not have a 10BASE-T PMA, it will cease transmission of FLP Bursts, forcing the 10BASE-T Link Partner into the LINK TEST FAIL state(s) as indicated in Figure 14–6.

NOTE—Auto-Negotiation does not support the transmission of the NLP sequence. The 10BASE-T PMA provides this function if it is connected to the MDI. In the case where an Auto-Negotiation able device without a 10BASE-T PMA is connected to a 10BASE-T device without Auto-Negotiation, the NLP sequence is not transmitted because the Auto-Negotiation function has no 10BASE-T PMA to enable that can transmit the NLP sequence.

28.1.4.2 Interoperability with Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the base Link Code Word from the FLP Burst, and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's base Link Code Words by responding with FLP Bursts containing the Acknowledge Bit set. After both devices complete acknowledgment, and optionally, Next Page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in . It may subsequently be the responsibility of a technology-dependent link integrity test function to verify operation of the link prior to enabling the data service.

28.1.4.3 Cabling compatibility with Auto-Negotiation

Provision has been made within Auto-Negotiation to limit the resulting link configuration in situations where the cabling may not support the highest common capability of the two end points. The system administrator/installer must take the cabling capability into consideration when configuring a hub port's advertised capability. That is, the advertised capability of a hub port should not result in an operational mode that is not compatible with the cabling.

28.2 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PMA type, where more than one PMA type may exist. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the Auto-Negotiation Transmit, Receive, Arbitration, and NLP Receive Link Integrity Test functions and comply with the state diagrams of Figures 28–15 to 28–18. The Auto-Negotiation functions shall interact with the technology-dependent PMAs through the Technology-Dependent Interface. Technology-dependent PMAs include, but are not limited to, 100BASE-TX and

100BASE-T4. Technology-dependent link integrity test functions shall be implemented and interfaced to only if the device supports the given technology. For example, a 10BASE-T and 100BASE-TX Auto-Negotiation able device must implement and interface to the 100BASE-TX PMA/link integrity test function, but does not need to include the 100BASE-T4 PMA/Link Integrity Test function. The Auto-Negotiation function shall provide an optional Management function that provides a control and status mechanism.

28.2.1 Transmit function requirements

The Transmit function provides the ability to transmit FLP Bursts. The first FLP Bursts exchanged by the Local Device and its Link Partner after Power-On, link restart, or renegotiation contain the base Link Code Word defined in 28.2.1.2. The Local Device may modify the Link Code Word to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multimode devices may Auto-Negotiate to a mode lower in priority than the highest common local ability.

28.2.1.1 Link pulse transmission

Auto-Negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link. Compliant 10BASE-T MAUs transmit link integrity test pulses as a mechanism to determine if the link segment is operational in the absence of packet data. The 10BASE-T NLP sequence is a pulse (Figure 14–12) transmitted every 16 ± 8 ms while the data transmitter is idle.

Auto-Negotiation substitutes the FLP Burst in place of the single 10BASE-T link integrity test pulse within the NLP sequence (Figure 28–3). The FLP Burst encodes the data that is used to control the Auto-Negotiation function. FLP Bursts shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PMA has been enabled.

FLP Bursts were designed to allow use beyond initial link Auto-Negotiation, such as for a link monitor type function. However, use of FLP Bursts beyond the current definition for link startup shall be prohibited. Definition of the use of FLP Bursts while in the FLP LINK GOOD state is reserved.

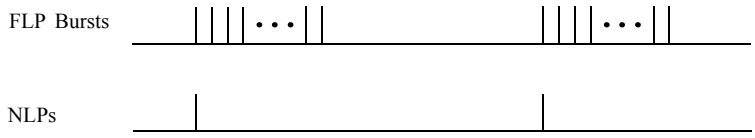


Figure 28–3—FLP Burst sequence to NLP sequence mapping

28.2.1.1.1 FLP burst encoding

Change subclause 28.2.1.1.1 as follows

FLP Bursts shall be composed of link pulses meeting the requirements of Figure 14–12. A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. Clock pulses are differentiated from data pulses by the spacing between pulses as shown in Figure 28–5 and enumerated in Table 28–1. Extended FLP Bursts contain 97 pulse positions with 49 clock pulses and 48 data pulses.

The encoding of data using pulses in an FLP Burst is illustrated in Figure 28–4.

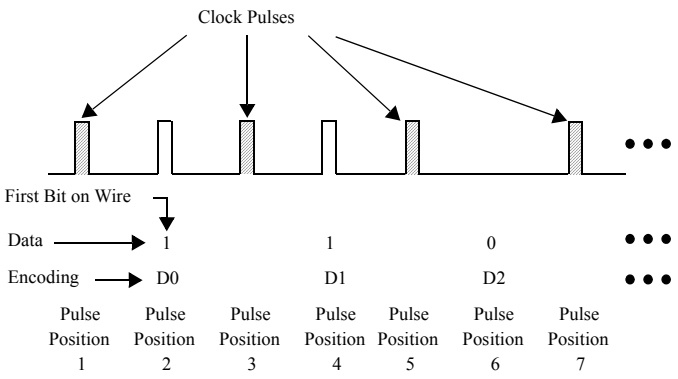


Figure 28–4—Data bit encoding within FLP Bursts

28.2.1.1.2 Transmit timing

The first pulse in an FLP Burst shall be defined as a clock pulse. Clock pulses within an FLP Burst shall be spaced at 125 ± 14 µs. If the data bit representation of logic one is to be transmitted, a pulse shall occur 62.5 ± 7 µs after the preceding clock pulse. If a data bit representing logic zero is to be transmitted, there shall be no link integrity test pulses within 111 µs of the preceding clock pulse.

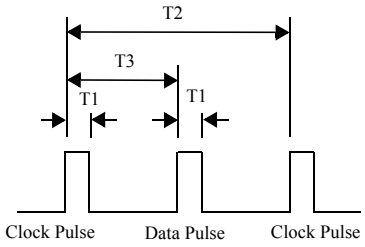


Figure 28–5—FLP Burst pulse-to-pulse timing

Change Figure 28-6 to include "or T7" next to T6, and change subclause as follows:

The first link pulse in consecutive FLP Bursts shall occur at either 16 ± 8 ms interval or 8.25 ± .25 ms intervalwhen using non optimized FLP Burst to FLP Burst timing, see parameters T6 and T7 in (Figure 28–6). The first link pulse in consecutive FLP Bursts shall occur at a 8.25 ± .25 ms interval when using optimized FLP Burst to FLP Burst timing for devices supporting Extended Next Pages, see parameter T7 in (Figure 28–6). Optimized FLP Burst to FLP Burst limits are intended to reduce negotiation time

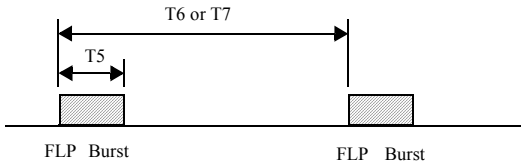


Figure 28–6—FLP Burst to FLP Burst timing

Table 28–1—FLP Burst timing summary

#	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–12)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	µs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs
T4	Pulses in a Burst	17		~~33~~ 97	#
T5	Burst Width		2 for 16-bit 6 for 48-bit		ms
T6	FLP Burst to FLP Burst	8	16	24	ms
T7	Optimized FLP Burst to FLP Burst	8		8.5	ms

28.2.1.2 Link Code Word encoding

Change Table 28-1 to show 97 Max pulses in row T4 , change T5, and add row T7 as follows:

The base Link Code Word (base page) transmitted within an FLP Burst shall convey the encoding shown in Figure 28–7. The Auto-Negotiation function may support additional pages using the Next Page function. Encodings for the Link Code Word(s) used in Next Page exchange are defined in 28.2.3.4. In an FLP Burst, D0 shall be the first bit transmitted.

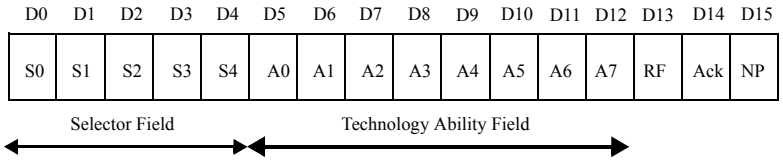


Figure 28–7—Base page encoding

28.2.1.2.1 Selector Field

Selector Field (S[4:0]) is a five bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector Field shall not be transmitted.

28.2.1.2.2 Technology Ability Field

Technology Ability Field (A[7:0]) is an eight bit wide field containing information indicating supported technologies specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector is described in Annex 28B.2 and in . Multiple technologies may be advertised in the Link Code Word. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a Link Partner and to resolve multiple common modes.

NOTE—While devices using a Selector Field value other than the IEEE 802.3 Selector Field value are free to define the Technology Ability Field bits, it is recommended that the 10BASE-T bit be encoded in the same bit position as in the

IEEE 802.3 selector. A common bit position can be important if the technology using the other selector will ever coexist on a device that also offers a 10BASE-T mode.

28.2.1.2.3 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base Link Code Word. The default value is logic zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the Auto-Negotiation advertisement register (Register 4) is set to logic one, the RF bit in the transmitted base Link Code Word is set to logic one. When the RF bit in the received base Link Code Word is set to logic one, the Remote Fault bit in the MII status register (Register 1) will be set to logic one, if the MII management function is present.

The Remote Fault bit shall be used in accordance with the Remote Fault function specifications (28.2.3.5).

28.2.1.2.4 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. The Acknowledge Bit is encoded in bit D14 regardless of the value of the Selector Field or Link Code Word encoding. If no Next Page information is to be sent, this bit shall be set to logic one in the Link Code Word after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logic one after the device has successfully received at least three consecutive and matching FLP Bursts (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the Auto-Negotiation Next Page transmit register (Register 7). In order to save the current received Link Code Word, it must be read from the Auto-Negotiation link partner ability register (Register 6) before the Next Page of transmit information is loaded into the Auto-Negotiation Next Page transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the Link Code Word shall be transmitted six to eight (inclusive) times.

28.2.1.2.5 Next Page

Next Page (NP) is encoded in bit D15 regardless of the Selector Field value or Link Code Word encoding. Support for transmission and reception of additional Link Code Word encodings is optional. If Next Page ability is not supported, the NP bit shall always be set to logic zero. If a device implements Next Page ability and wishes to engage in Next Page exchange, it shall set the NP bit to logic one. A device may implement Next Page ability and choose not to engage in Next Page exchange by setting the NP bit to a logic zero. The Next Page function is defined in 28.2.3.4.

28.2.1.3 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PMA to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Transmit Switch function shall connect only the FLP Burst generator controlled by the Transmit State Diagram, Figure 28–15, to the MDI.

When a PMA is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

28.2.2 Receive function requirements

The Receive function detects the NLP sequence using the NLP Receive Link Integrity Test function of Figure 28–18. The NLP Receive Link Integrity Test function will not detect link pass based on carrier sense.

The Receive function detects the FLP Burst sequence, decodes the information contained within, and stores the data in rx_link_code_word[16:1]. The Receive function incorporates a receive switch to control connection to the 100BASE-TX or 100BASE-T4 PMAs in addition to the NLP Receive Link Integrity Test function, excluding the 10BASE-T Link Integrity Test function present in a 10BASE-T PMA. If Auto-Negotiation detects link_status=READY from any of the technology-dependent PMAs prior to FLP Burst detection, the autoneg_wait_timer (28.3.2) is started. If any other technology-dependent PMA indicates link_status=READY when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the Link Partner using the base page and will flag this in the Local Device by setting the Parallel Detection Fault bit (6.4) in the Auto-Negotiation expansion register. If a 10BASE-T PMA exists above the Auto-Negotiation function, it is not permitted to receive MDI activity in parallel with the NLP Receive Link Integrity Test function or any other technology-dependent function.

28.2.2.1 FLP Burst ability detection and decoding

In Figures 28–8 to 28–10, the symbol "t_0=0" indicates the event that caused the timers described to start, and all subsequent times given are referenced from that point. All timers referenced shall expire within the range specified in Table 28–9 in 28.3.2.

The Receive function shall identify the Link Partner as Auto-Negotiation able if it receives 6 to 17 (inclusive) consecutive link pulses that are separated by at least flp_test_min_timer time (5–25 µs) but less than flp_test_max_timer time (165–185 µs) as shown in Figure 28–8. The information contained in the FLP Burst that identifies the Link Partner as Auto-Negotiation able shall not be passed to the Arbitration function if the FLP Burst is not complete. The Receive function may use the FLP Burst that identifies the Link Partner as Auto-Negotiation able for ability matching if the FLP Burst is complete. However, it is not required to use this FLP Burst for any purpose other than identification of the Link Partner as Auto-Negotiation able. Implementations may ignore multiple FLP Bursts before identifying the Link Partner as Auto-Negotiation able to allow for potential receive equalization time.

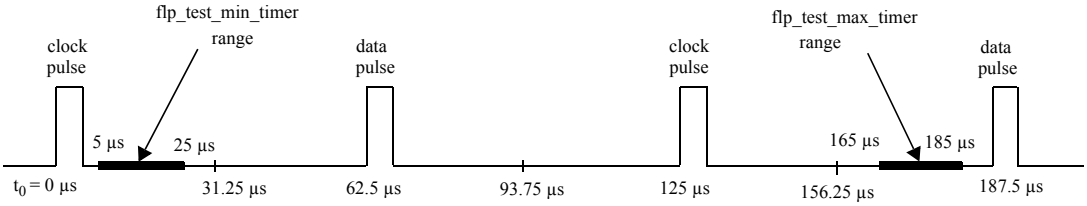


Figure 28–8—FLP detect timers (flp_test_min/max_timers)

The Receive function captures and decodes link pulses received in FLP Bursts. The first link pulse in an FLP Burst shall be interpreted as a clock link pulse. Detection of a clock link pulse shall restart the data_detect_min_timer and data_detect_max timer. The data_detect_min/max_timers enable the receiver to distinguish data pulses from clock pulses and logic one data from logic zero data, as follows:

a) If, during an FLP Burst, a link pulse is received when the data_detect_min_timer has expired while the data_detect_max_timer has not expired, the data bit shall be interpreted as a logic one (Figure 28–9).
b) If, during an FLP Burst, a link pulse is received after the data_detect_max_timer has expired, the data bit shall be interpreted as a logic zero (Figure 28–9) and that link pulse shall be interpreted as a clock link pulse.

As each data bit is identified it is stored in the appropriate rx_link_code_word[16:1] element.

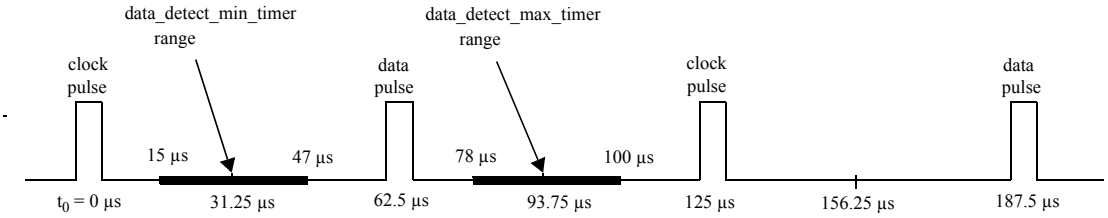
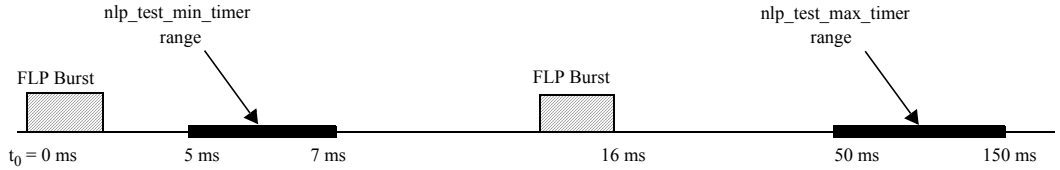


Figure 28–9—FLP data detect timers (data_detect_min/max_timers)

FLP Bursts conforming to the nlp_test_min_timer and nlp_test_max_timer timing as shown in Figure 28–10 shall be considered to have valid separation.



NOTE—The reference for the starting of the nlp_test_min_timer is from the beginning of the FLP Burst, as shown by t_0, while the reference for the starting of the nlp_test_max_timer is from the expiration of the nlp_test_min_timer.

Figure 28–10—FLP Burst timer (nlp_test_min/max_timers)

28.2.2.2 NLP detection

NLP detection is accomplished via the NLP Receive Link Integrity Test function in Figure 28–18. The NLP Receive Link Integrity Test function is a modification of the original 10BASE-T Link Integrity Test function (Figure 14–6), where the detection of receive activity will not cause a transition to the LINK TEST PASS state during Auto-Negotiation. The NLP Receive Link Integrity Test function also incorporates the Technology-Dependent Interface requirements.

28.2.2.3 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PMA once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Receive Switch function shall connect both the FLP Burst receiver controlled by the Receive state diagram, Figure 28–16, and the NLP Receive Link Integrity Test state diagram, Figure 28–18, to the MDI. During Auto-Negotiation, the Receive Switch function shall also connect the 100BASE-TX and 100BASE-T4 PMA receivers to the MDI if the 100BASE-TX and/or 100BASE-T4 PMAs are present.

When a PMA is connected to the MDI through the Receive Switch function, the signals at the PMA shall conform to all of the PHY's specifications.

28.2.2.4 Link Code Word matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in 28.3.1.

28.2.3 Arbitration function requirements

The Arbitration function ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgment, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PMA via the Technology-Dependent Interface (28.2.6).

28.2.3.1 Parallel detection function

The Local Device detects a Link Partner that supports Auto-Negotiation by FLP Burst detection. The Parallel Detection function allows detection of Link Partners that support 100BASE-TX, 100BASE-T4, and/or 10BASE-T, but do not support Auto-Negotiation. Prior to detection of FLP Bursts, the Receive Switch shall direct MDI receive activity to the NLP Receive Link Integrity Test state diagram, 100BASE-TX and 100BASE-T4 PMAs, if present, but shall not direct MDI receive activity to the 10BASE-T or any other PMA. If at least one of the 100BASE-TX, 100BASE-T4, or NLP Receive Link Integrity Test functions establishes link_status=READY, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=READY indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PMA indicating link_status=READY. If a PMA is enabled, the Arbitration function shall set link_control=DISABLE to all other PMAs and indicate that Auto-Negotiation has completed. On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the link partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function.

NOTE 1—Native 10BASE-T devices will be detected by the NLP Receive Link Integrity Test function, an integrated part of the Auto-Negotiation function. Hence, Parallel Detection for the 10BASE-T PMA is not required or allowed.

NOTE 2—When selecting the highest common denominator through the Parallel Detection function, only the half-duplex mode corresponding to the selected PMA may automatically be detected.

28.2.3.2 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PMAs and halt any transmit data and link pulse activity until the break_link_timer expires (28.3.2). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The Local Device shall resume Auto-Negotiation after the break_link_timer has expired by issuing FLP Bursts with the base page valid in tx_link_code_word[16:1].

Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PMA an opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PMA still indicates link_status=FAIL or link_status=READY.

28.2.3.3 Priority Resolution function

Since a Local Device and a Link Partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PMA enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the Local Device and Link Partner that has the highest priority as defined in . This technology is referred to as the Highest Common Denominator, or HCD, technology. If the Local Device receives a Technology Ability Field with a bit set that is reserved, the Local Device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the FLP LINK GOOD CHECK state. In

the event that a technology is chosen through the Parallel Detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of "NULL," indicating that no PMA receives link_control=ENABLE, and link_status_[HCD]=FAIL.

28.2.3.4 Next Page function

The Next Page function uses the standard Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data. Data is carried by optional Next Pages of information, which follow the transmission and acknowledgment procedures used for the base Link Code Word. Two types of Next Page encodings are defined: Message Pages and Unformatted Pages.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

Next Page operation is controlled by the same two mandatory control bits, Next Page and Acknowledge, used in the Base Link Code Word. Setting the NP bit in the Base Link Code Word to logic one indicates that the device is Next Page Able. If both a device and its Link Partner are Next Page Able, then Next Page exchange may occur. If one or both devices are not Next Page Able, then Next Page exchange will not occur and, after the base Link Code Words have been exchanged, the FLP LINK GOOD CHECK state will be entered. The Toggle bit is used to ensure proper synchronization between the Local Device and the Link Partner.

Next Page exchange occurs after the base Link Code Words have been exchanged. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages. Two message encodings are defined: Message Pages, which contain predefined 11 bit codes, and Unformatted Pages. Unformatted Pages can be combined to send extended messages. If the Selector Field values do not match, then each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be interpreted. If the Selector Field values match, then the convention governing the use of Message Pages shall be as defined by the Selector Field value definition. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Message Pages with Null message codes and the NP bit set to logic zero while its Link Partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages with Null message codes as the end of its Link Partner's Next Page information.

28.2.3.4.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 28–11 and Figure 28–12 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10–D0 shall be encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero.

Insert subclause 28.3.4.2 as follows and renumber subsequent subclauses. Insert figure 28-13 and renumber following figures.

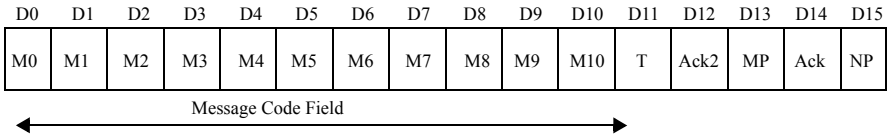


Figure 28–11—Message Page encoding

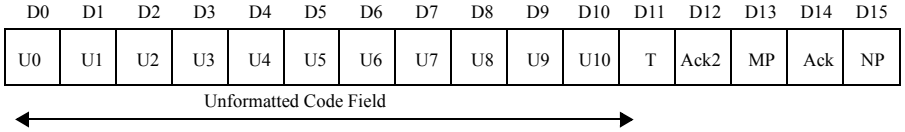


Figure 28–12—Unformatted Page encoding

28.2.3.4.2 Extended Next Page encodings

Extended Next Pages shall use the encoding shown in Figure 28-13 for the message code field, flags field, and unformatted code field. The Message Code Field contains the 11-bit Message Code value. The 5-bit flags field contains the NP, Ack, MP, Ack2, and T bits. The Unformatted Code Field contains a 32-bit value..

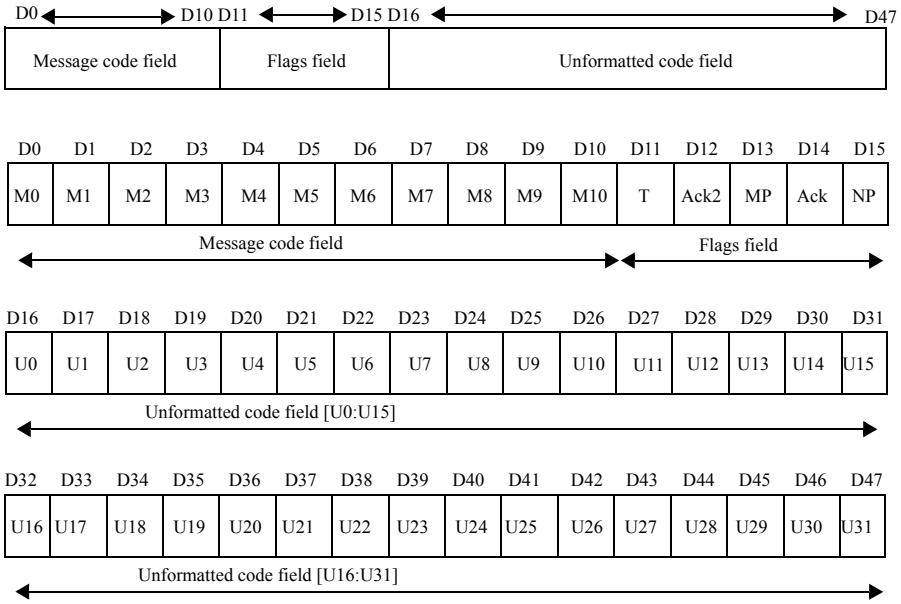


Figure 28–13—Extended Next Page Encoding

28.2.3.4.3 Next Page

Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows:

logic zero = last page.
logic one = additional Next Page(s) will follow.

28.2.3.4.4 Acknowledge

As defined in 28.2.1.2.4.

28.2.3.4.5 Message Page

Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

28.2.3.4.6 Acknowledge 2

Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = cannot comply with message.
logic one = will comply with message.

28.2.3.4.7 Toggle

Toggle (T) is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows:

logic zero = previous value of the transmitted Link Code Word equalled logic one.
logic one = previous value of the transmitted Link Code Word equalled logic zero.

28.2.3.4.8 Message Page encoding

Message Pages are formatted pages that carry a single predefined Message Code, which is enumerated in Annex 28C. Two-thousand and forty-eight Message Codes are available. The allocation of these codes will be controlled by the contents of Annex 28C. If the Message Page bit is set to logic one, then the bit encoding of the Link Code Word shall be interpreted as a Message Page.

28.2.3.4.9 Message Code Field

Message Code Field (M[10:0]) is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

28.2.3.4.10 Unformatted Page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining 11 bits may take on an arbitrary value. If the Message Page bit is set to logic zero, then the bit encoding of the Link Code Word shall be interpreted as an Unformatted Page.

28.2.3.4.11 Unformatted Code Field

Unformatted Code Field (U[10:0]) is an eleven bit wide field, which may contain an arbitrary value.

Insert subclause 28.2.3.4.12 and renumber following subclauses

28.2.3.4.12 Extended Next Page encoding

Extended Next Pages carry a single predefined Message Code (M[10:0]), which is enumerated in Annex 28C, and a single 32-bit Unformatted Code ([U31:0]), which may contain an arbitrary value.

28.2.3.4.13 Use of Next Pages

Change bullet (d) as follows in subclause 28.2.3.4.13

a) Both devices must indicate Next Page ability for either to commence exchange of Next Pages.
b) If both devices are Next Page able, then both devices shall send at least one Next Page.
c) Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.
d) A Message Code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted, and can carry information that defines how the Unformated Message Code in an Extended Next Page should be interpreted.
e) If a Message Code references Unformatted Pages, the Unformatted Pages shall immediately follow the referencing Message Code in the order specified by the Message Code.
f) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.

28.2.3.4.14 MII register requirements

The Next Page Transmit register defined in 28.2.4.1.6 shall hold the Next Page to be sent by Auto-Negotiation. Received Next Pages may be stored in the Auto-Negotiation link partner ability register.

28.2.3.5 Remote fault sensing function

The Remote Fault function may indicate to the Link Partner that a fault condition has occurred using the Remote Fault bit and, optionally, the Next Page function.

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault bit shall be optional. If the Local Device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault bit indication, then it shall transmit the Remote Fault bit with the value contained in the Auto-Negotiation advertisement register bit (4.13).

A Local Device may indicate it has sensed a fault to its Link Partner by setting the Remote Fault bit in the Auto-Negotiation advertisement register and renegotiating.

If the Local Device sets the Remote Fault bit to logic one, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes have been specified for this purpose.

The Remote Fault bit shall remain set until after successful negotiation with the base Link Code Word, at which time the Remote Fault bit shall be reset to a logic zero. On receipt of a base Link Code Word with the Remote Fault bit set to logic one, the device shall set the Remote Fault bit in the MII status register (1.4) to logic one if the MII management function is present.

28.2.4 Management function requirements

Editors' Notes: *To be removed prior to final publication.*

The necessary management additions for 10GBASE-T, including Clause 45 registers and modifications to existing registers, will be added in a later draft.

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.

28.2.4.1 Media Independent Interface

The Auto-Negotiation function shall have five dedicated registers:

a) MII control register (Register 0).
b) MII status register (Register 1).
c) Auto-Negotiation advertisement register (Register 4).
d) Auto-Negotiation link partner ability register (Register 5).
e) Auto-Negotiation expansion register (Register 6).

If the Next Page function is implemented, the Auto-Negotiation next page transmit register (Register 7) shall be implemented.

28.2.4.1.1 MII control register

MII control register (Register 0) provides the mechanism to disable/enable and/or restart Auto-Negotiation. The definition for this register is provided in 28.2.4.1.

The Auto-Negotiation function shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13 and 0.8 shall have no effect on the link configuration, and the Auto-Negotiation process will determine the link configuration. If bit 0.12 is cleared to logic zero, then bits 0.13 and 0.8 will determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

A PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall be initiated by setting bit 0.9 to a logic one. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, then this bit will have no meaning, and should be written as zero. This bit is self-clearing. The Auto-Negotiation process shall not be affected by clearing this bit to logic zero.

28.2.4.1.2 MII status register

The MII status register (Register 1) includes information about all modes of operations supported by the Local Device's PHY, the status of Auto-Negotiation, and whether the Auto-Negotiation function is supported by the PHY or not. The definition for this register is provided in 28.2.4.2.

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of Registers 4, 5, and 6 are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of Registers 4, 5, and 6 are meaningless.

A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

When read as logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

When read as a one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

28.2.4.1.3 Auto-Negotiation advertisement register (Register 4) (R/W)

This register contains the Advertised Ability of the PHY. (See Table 28–2). The bit definition for the base page is defined in 28.2.1.2. On power-up, before Auto-Negotiation starts, this register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4.12:5) is set based on the values set in the MII status register (Register 1) (1.15:11) or equivalent. See also .

Table 28–2—Advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

Only the bits in the Technology Ability Field that represent the technologies supported by the Local Device may be set. Any of the Technology Ability Field bits that may be set can also be cleared by management before a renegotiation. This can be used to enable management to Auto-Negotiate to an alternate common mode.

The management entity may initiate renegotiation with the Link Partner using alternate abilities by setting the Selector Field (4.4:0) and Technology Ability Field (4.12:5) to indicate the preferred mode of operation and setting the Restart Auto-Negotiation bit (0.9) in the control register (Register 0) to logic one.

Any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a renegotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be examined by software to determine the highest common denominator technology.

28.2.4.1.4 Auto-Negotiation link partner ability register (Register 5) (RO)

All of the bits in the Auto-Negotiation link partner ability register are read only. A write to the Auto-Negotiation link partner ability register shall have no effect.

This register contains the Advertised Ability of the Link Partner's PHY. (See Tables 28–3 and 28–4.) The bit definitions shall be a direct representation of the received Link Code Word (Figure 28–7). Upon successful completion of Auto-Negotiation, status register (Register 1) Auto-Negotiation Complete bit (1.5) shall be set to logic one. If the Next Page function is supported, the Auto-Negotiation link partner ability register may be used to store Link Partner Next Pages.

Table 28–3—Link partner ability register bit definitions (Base Page)

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

Table 28–4—Link partner ability register bit definitions (Next Page)

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.3.4	RO
5.14	Acknowledge	See 28.2.3.4	RO
5.13	Message Page	See 28.2.3.4	RO
5.12	Acknowledge 2	See 28.2.3.4	RO
5.11	Toggle	See 28.2.3.4	RO
5.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

The values contained in this register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or, if used with Next Page exchange, after the Page Received bit (6.1) has been set to logic one.

NOTE—If this register is used to store Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

28.2.4.1.5 Auto-Negotiation expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register shall have no effect. (See Table 28–5.)

Bits 6.15:5 are reserved for future Auto-Negotiation expansion.

The Parallel Detection Fault bit (6.4) shall be set to logic one to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires. The Parallel Detection Fault bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

Table 28–5—Expansion register bit definitions

Bit(s)	Name	Description	R/W	Default
6.15:5	Reserved	Write as zero, ignore on read	RO	0
6.4	Parallel Detection Fault	1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able	RO	0
6.2	Next Page Able	1 = Local Device is Next Page able 0 = Local Device is not Next Page able	RO	0
6.1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able	RO	0

The Link Partner Next Page Able bit (6.3) shall be set to logic one to indicate that the Link Partner supports the Next Page function. This bit shall be reset to logic zero to indicate that the Link Partner does not support the Next Page function.

The Next Page Able bit (6.2) shall be set to logic one to indicate that the Local Device supports the Next Page function. The Next Page Able bit (6.2) shall be set to logic zero if the Next Page function is not supported.

The Page Received bit (6.1) shall be set to logic one to indicate that a new Link Code Word has been received and stored in the Auto-Negotiation link partner ability register. The Page Received bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

The Link Partner Auto-Negotiation Able bit (6.0) shall be set to logic one to indicate that the Link Partner is able to participate in the Auto-Negotiation function. This bit shall be reset to logic zero if the Link Partner is not Auto-Negotiation able.

28.2.4.1.6 Auto-Negotiation Next Page transmit register (Register 7) (R/W)

The Auto-Negotiation Next Page Transmit register contains the Next Page Link Code Word to be transmitted when Next Page ability is supported. (See Table 28–6.) The contents are defined in 28.2.3.4. On power-up, this register shall contain the default value of 2001H, which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid Next Page Message Code that the device wishes to transmit. Writing to this register shall set mr_next_page_loaded to true.

28.2.4.1.7 Auto-Negotiation Link Partner Ability register (Register 8) (RO)

Support for 100BASE-T2 and 1000BASE-T requires support for Next Page and the provision of an Auto-Negotiation Link Partner Next Page Ability register (register 8) to store Link Partner Next Pages as shown in Table 28–7. All of the bits in the Auto-Negotiation Link Partner Next Page Ability register are read only. A write to the Auto-Negotiation Link Partner Next Page Ability register shall have no effect.

Table 28–6—Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0, ignore on read	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code field	See 28.2.3.4	R/W

The values contained in this register are only guaranteed to be valid after the Page Received bit (6.1) has been set to logical one or once Auto-Negotiation has successfully completed, as indicated by bit 1.5.

NOTE—If this register is used to store multiple Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

Table 28–7—Link Partner Next Page Ability register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	see 28.2.3.4	RO
8.14	Acknowledge	see 28.2.3.4	RO
8.13	Message Page	see 28.2.3.4	RO
8.12	Acknowledge 2	see 28.2.3.4	RO
8.11	Toggle	see 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	see 28.2.3.4	RO

28.2.4.1.8 State diagram variable to MII register mapping

The state diagrams of Figures 28–15 to 28–18 generate and accept variables of the form “mr_x,” where x is an individual signal name. These variables comprise a management interface that may be connected to the MII management function or other equivalent function. Table 28–8 describes how the MII registers map to the management function interface signals.

Table 28–8—State diagram variable to MII register mapping

State diagram variable	MII register
mr_adv_ability[16:1]	4.15:0 Auto-Negotiation advertisement register
mr_autoneg_complete	1.5 Auto-Negotiation Complete
mr_autoneg_enable	0.12 Auto-Negotiation Enable

Table 28–8—State diagram variable to MII register mapping *(continued)*

State diagram variable	MII register
mr_lp_adv_ability[16:1]	5.15:0 Auto-Negotiation link partner ability register
mr_lp_autoneg_able	6.0 Link Partner Auto-Negotiation Able
mr_lp_np_able	6.3 Link Partner Next Page Able
mr_main_reset	0.15 Reset
mr_next_page_loaded	Set on write to Auto-Negotiation Next Page Transmit register; cleared by Arbitration state diagram
mr_np_able	6.2 Next Page Able
mr_np_tx[16:1]	7.15:0 Auto-Negotiation Next Page Transmit Register
mr_page_rx	6.1 Page Received
mr_parallel_detection_fault	6.4 Parallel Detection Fault
mr_restart_negotiation	0.9 Auto-Negotiation Restart
set if Auto-Negotiation is available	1.3 Auto-Negotiation Ability

28.2.4.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

28.2.5 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability[16:1]. A device shall comply with all Next Page function requirements, including the provision of the mr_np_able, mr_lp_np_able, and mr_next_page_loaded variables (or their logical equivalents), in order to permit the NP bit to be set to logic one in the transmitted Link Code Word.

NOTE—Storage of a valid base Link Code Word is required to prevent a deadlock situation where negotiation must start again while Next Pages are being transmitted. If a shared transmit register were used, then renegotiation could not occur when Next Pages were being transmitted because the base Link Code Word would not be available. This requirement can be met using a number of different implementations, including use of temporary registers or register stacks.

28.2.6 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

28.2.6.1 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS, repeater client, or Auto-Negotiation function a means of determining the validity of received code elements.

28.2.6.1.1 Semantics of the service primitive

PMA_LINK.indicate(link_status)

The link_status parameter shall assume one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled (READY), intact and enabled (OK), or not intact (FAIL). When link_status=FAIL or link_status=READY, the PMA_CARRIER.indicate and PMA_UNITDATA.indicate primitives are undefined.

28.2.6.1.2 When generated

A technology-dependent PMA and the NLP Receive Link Integrity Test state diagram (Figure 28–18) shall generate this primitive to indicate the value of link_status.

28.2.6.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagrams of Figure 28–17.

28.2.6.2 PMA_LINK.request

This primitive is generated by Auto-Negotiation to allow it to enable and disable operation of the PMA.

28.2.6.2.1 Semantics of the service primitive

PMA_LINK.request(link_control)

The link_control parameter shall assume one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

The link_control=SCAN_FOR_CARRIER mode is used by the Auto-Negotiation function prior to receiving any FLP Bursts or link_status=READY indications. During this mode, the PMA shall search for carrier and report link_status=READY when carrier is received, but no other actions shall be enabled.

The link_control=DISABLE mode shall be used by the Auto-Negotiation function to disable PMA processing.

The link_control=ENABLE mode shall be used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions.

28.2.6.2.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagrams of Figure 28–16 and Figure 28–17.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINK.request(DISABLE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINK.request(link_control) is implementation dependent.

28.2.6.2.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the NLP Receive Link Integrity Test state diagram (Figure 28–18) and the receiving technology-dependent link integrity test function, based on the intent specified in the primitive semantics.

28.2.6.3 PMA_LINKPULSE.request

This primitive is generated by Auto-Negotiation to indicate that a valid Link Pulse, as transmitted in compliance with Figure 14–12, has been received.

28.2.6.3.1 Semantics of the service primitive

PMA_LINKPULSE.request (linkpulse)

The linkpulse parameter shall assume one of two values: TRUE or FALSE.

The linkpulse=FALSE mode shall be used by the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.

The linkpulse=TRUE mode shall be used by the Auto-Negotiation function to indicate that a valid Link Pulse has been received.

28.2.6.3.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–16.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request (FALSE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINKPULSE.request (linkpulse) is implementation dependent.

28.2.6.3.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.3 State diagrams and variable definitions

Change subclause 28.3 as follows

The notation used in the state diagrams (Figures 28–15 to 28–18) follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the “mr_x” notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the MII interface are covered in 28.2.4 and 22.2.4, and Clause 45 MDIO management interface. The variables, timers, and counters used in the state diagrams are defined in 28.3, 14.2.3, and 28.2.6.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram, Arbitration state diagram, and NLP Receive Link Integrity Test state diagram as depicted in 28.3. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

The functional reference diagram (Figure 28–14) provides a generic example, illustrated with initial PMA implementations and showing the mechanism for expansion. New PMAs are documented in .

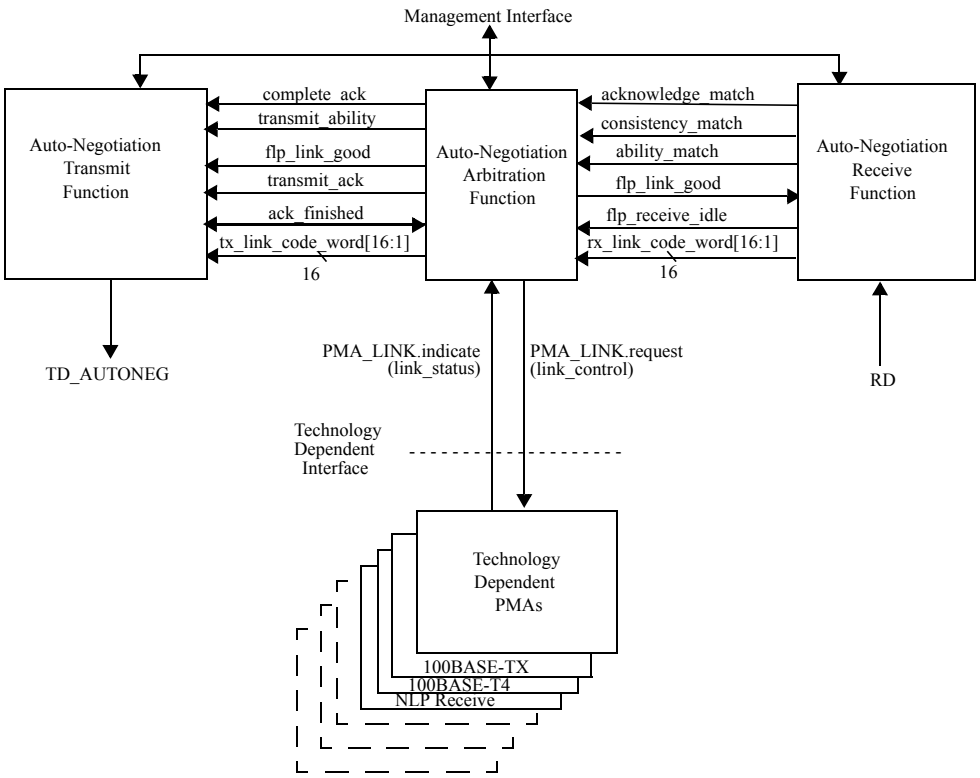


Figure 28–14—Functional reference diagram

28.3.1 State diagram variables

Insert the page_size variable to subclause 28.3.1

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all;	represents all specific technology-dependent PMAs supported in the Local Device and the NLP Receive Link Integrity Test state diagram.
1GigT;	represents that the 1000BASE-T PMA is the signal source.
HCD;	represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function. To select 10BASE-T, LIT is used instead of NLP to enable the full 10BASE-T Link Integrity Test function state diagram.
notHCD;	represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function.
TX;	represents that the 100BASE-TX PMA is the signal source.
T4;	represents that the 100BASE-T4 PMA is the signal source.
NLP;	represents that the NLP Receive Link Integrity Test function is the signal source.
PD;	represents all of the following that are present: 100BASE-TX PMA, 100BASE-T4 PMA, and the NLP Receive Link Integrity Test state diagram.
LIT;	represents the 10BASE-T Link Integrity Test function state diagram is the signal source or destination.

Variables with [16:1] appended to the end of the variable name indicate arrays that can be directly mapped to 16-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

— Any integer.
— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bit.

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the MII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive Link Code Words match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive Link Code Words have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive Link Code Words have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [16:1]

A 16-bit array that contains the last Link Code Word that caused ability_match = true. For each element in the array:

Values: zero; data bit is logicial zero.
one; data bit is logical one.

ack_finished

Status indicating that the final remaining_ack_cnt Link Code Words with the Ack bit set have been transmitted.

Values: false; more Link Code Words with the Ack bit set to logic one must be transmitted.
true; all remaining Link Code Words with the Ack bit set to logic one have been transmitted.

acknowledge_match

Indicates that three consecutive Link Code Words match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive Link Code Words have not been received with the Acknowledge bit set (default).
true; three matching and consecutive Link Code Words have been received with the Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial Link Code Word encoding used to communicate the device's abilities.

Values: false; a page other than base Link Code Word is being transmitted.
true; the base Link Code Word is being transmitted.

complete_ack

Controls the counting of transmitted Link Code Words that have their Acknowledge bit set.

Values: false; transmitted Link Code Words with the Acknowledge bit set are not counted (default).
true; transmitted Link Code Words with the Acknowledge bit set are counted.

consistency_match

Indicates that the Link Code Word that caused ability_match to be set is the same as the Link Code Word that caused acknowledge_match to be set.

Values: false; the Link Code Word that caused ability_match to be set is not the same as the Link Code Word that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
true; the Link Code Word that caused ability_match to be set is the same as the Link Code Word that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

desire_np

Status indicating that the Local Device desires to engage in Next Page exchange. This information comes from the setting of the NP bit in the base Link Code Word stored in the Auto-Negotiation

advertisement register (Register 4).

Values: false; Next Page exchange is not desired.
true; Next Page exchange is desired.

flp_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).
true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

flp_receive_idle

Indicates that the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

Values: false; the Receive state diagram is not in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state (default).
true; the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

incompatible_link

Parameter used following Priority Resolution to indicate the resolved link is incompatible with the Local Device settings. A device's ability to set this variable to true is optional.

Values: false; A compatible link exists between the Local Device and Link Partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control

This variable is defined in 28.2.6.2.1.

link_status

This variable is defined in 28.2.6.1.1.

linkpulse

This variable is defined in 28.2.6.3.1.

Values: false; linkpulse is set to false after any Receive State Diagram state transition (default).
true; linkpulse is set to true when a valid Link Pulse is received.

mr_autoneg_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable

Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[16:1]

A 16-bit array that contains the Advertised Abilities Link Code Word.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_adv_ability[16:1]

A 16-bit array that contains the Link Partner's Advertised Abilities Link Code Word. For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_np_able

Status indicating whether the Link Partner supports Next Page exchange.

Values: false; the Link Partner does not support Next Page exchange.
true; the Link Partner supports Next Page exchange.

mr_np_able

Status indicating whether the Local Device supports Next Page exchange.

Values: false; the Local Device does not support Next Page exchange.
true; the Local Device supports Next Page exchange.

mr_lp_autoneg_able

Status indicating whether the Link Partner supports Auto-Negotiation.

Values: false; the Link Partner does not support Auto-Negotiation.
true; the Link Partner supports Auto-Negotiation.

mr_main_reset

Controls the resetting of the Auto-Negotiation state diagrams.

Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded

Status indicating whether a new page has been loaded into the Auto-Negotiation Next Page Transmit register (Register 7).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[16:1]

A 16-bit array that contains the new Next Page to transmit. For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the Link Code Word has been written to mr_lp_adv_ability[16:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault

Error condition indicating that while performing Parallel Detection, either flp_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the Auto-Negotiaion expansion register.

1) link_status_ [NLP] = READY

2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; Exactly one of the above three indications was true when the autoneg_wait_timer expired, and flp_receive_idle = true.
true; either zero or more than one of the above three indications was true when the autoneg_wait_timer expired, or flp_receive_idle = false.

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values: false; renegotiation is not taking place.
true; renegotiation is started.

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

page_size

Condition indicating the size of Next Page that the device is prepared to transmit and receive.

Values: 16; the device does not support extended Next Pages or is not in the process of transmitting or receiving extended Next Pages(default).
48; the device supports extended Next Pages and is in the process of transmitting or receiving extended Next Pages.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low power mode set via MII control register bit 0.11.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

rx_link_code_word[16:1]

A 16-bit array that contains the data bits to be received from an FLP Burst.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that flp_receive_idle = true and only one the of the following indications is being received:

1) link_status_[NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; either zero or more than one of the above three indications are true or flp_receive_idle = false.
true; Exactly one of the above three indications is true and flp_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: idle; Auto-Negotiation prevents transmission of all link pulses on the MDI.
link_test_pulse; Auto-Negotiation causes a single link pulse as defined by Figure 14–12 to be transmitted on the MDI.

toggle_rx

Flag to keep track of the state of the Link Partner's Toggle bit.

Values: 0; Link Partner's Toggle bit equals logic zero.
1; Link Partner's Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the Local Device's Toggle bit.

Values: 0; Local Device's Toggle bit equals logic zero.
1; Local Device's Toggle bit equals logic one.

transmit_ability

Controls the transmission of the Link Code Word containing tx_link_code_word[16:1].

Values: false; any transmission of tx_link_code_word[16:1] is halted (default).
true; the transmit state diagram begins sending tx_link_code_word[16:1].

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[16:1] to be transmitted.

Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[16:1] to a logic zero (default).
true; sets the Acknowledge bit in the transmitted tx_link_code_word[16:1] to a logic one.

transmit_disable

Controls the transmission of tx_link_code_word[16:1].

Values: false; tx_link_code_word[16:1] transmission is allowed (default).
true; tx_link_code_word[16:1] transmission is halted.

tx_link_code_word[16:1]

A 16-bit array that contains the data bits to be transmitted in an FLP Burst. This array may be loaded from mr_adv_ability or mr_np_tx.
For each element within the array:

Values: Zero; data bit is logical zero.
One; data bit is logical one.

28.3.2 State diagram timers

Change nlp_test_min_timer as follows

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer

Timer for the amount of time to wait before evaluating the number of link integrity test functions with link_status=READY asserted. The autoneg_wait_timer shall expire 500–1000 ms from the

assertion of link_status=READY from the 100BASE-TX PMA, 100BASE-T4 PMA, or the NLP Receive State diagram.

break_link_timer
: Timer for the amount of time to wait in order to assure that the Link Partner enters a Link Fail state. The timer shall expire 1200–1500 ms after being started.

data_detect_max_timer
: Timer for the maximum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_max_timer shall expire 78–100 μs from the last clock pulse.

data_detect_min_timer
: Timer for the minimum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_min_timer shall expire 15–47 μs from the last clock pulse.

flp_test_max_timer
: Timer for the maximum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_min_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_max_timer shall expire 165–185 μs from the last link pulse.

flp_test_min_timer
: Timer for the minimum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_max_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_min_timer shall expire 5–25 μs from the last link pulse.

interval_timer
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 55.5–-69.5 μs from each clock pulse and data bit.

link_fail_inhibit_timer
: Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750–1000 ms after entering the FLP LINK GOOD CHECK state.

NOTE—The link_fail_inhibit_timer expiration value must be greater than the time required for the Link Partner to complete Auto-Negotiation after the Local Device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state. The maximum time difference between a Local Device and its Link Partner completing Auto-Negotiation is

(Maximum FLP Burst to FLP Burst separation) × (Maximum number of FLP Bursts needed to complete acknowledgment) = (24 ms) × (8 bursts) = 192 ms.

For example, 100BASE-T4 requires approximately 460 ms to enter link_status=OK for a total minimum link_fail_inhibit_timer time of 652 ms. The lower bound for the link_fail_inhibit_timer was chosen to provide adequate margin for the current technologies and any future PMAs.

nlp_test_max_timer
: Timer for the maximum time that no FLP Burst may be seen before forcing the receive state diagram to the IDLE state. The nlp_test_max_timer shall expire 50–150 ms after being started or restarted.

nlp_test_min_timer
: Timer for the minimum time between two consecutive FLP Bursts. The nlp_test_min_timer shall expire 5–7 ms after being started or restarted~~.~~ for devices that do not support extended Next Pages,

and shall expire 6.5–7 ms after being started or restarted for devices that do support extended Next Pages.

transmit_link_burst_timer

Timer for the separation of a transmitted FLP Burst from the next FLP Burst. The transmit_link_burst_timer shall expire 5.7-22.3 ms after the last transmitted link pulse in an FLP Burst.

Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
autoneg_wait_timer	500		1000	ms
break_link_timer	1200		1500	ms
data_detect_min_timer	15		47	µs
data_detect_max_timer	78		100	µs
flp_test_min_timer	5		25	µs
flp_test_max_timer	165		185	µs
interval_timer	55.5	62.5	69.5	µs
link_fail_inhibit_timer	750		1000	ms
nlp_test_max_timer	50		150	ms
nlp_test_min_timer	5		7	ms
transmit_link_burst_timer	5.7	14	22.3	ms

28.3.3 State diagram counters

Chage rx_bit_cnt and tx_bit_cnt as follows:

flp_cnt

A counter that may take on integer values from 0 to 17. This counter is used to keep a count of the number of FLPs detected to enable the determination of whether the Link Partner supports Auto-Negotiation.

Values: not_done; 0 to 5 inclusive.
done; 6 to 17 inclusive.
init; counter is reset to zero.

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional Link Code Words with the Acknowledge Bit set to logic one to be sent to ensure that the Link Partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to ~~17~~ (page_size+1). This counter is used to keep a count of data bits received from an FLP Burst and to ensure that when erroneous extra pulses are received, the first ~~16~~ page_size bits are kept while the rest are ignored. When this variable reaches ~~16 or 17~~ page_size or (page_size+1), enough data bits have been received. This counter does not increment beyond ~~17~~ (page_size+1) and does not return to 0 until it is reinitialized.

Values: not_done; 1 to ~~15~~ (page_size-1) inclusive.
done; ~~16 or 17~~ page_size or (page_size+1)
init; counter is reset to zero.
rx_bit_cnt_check; 10 to 17 inclusive.

tx_bit_cnt

A counter that may take on integer values from 1 to ~~17~~ (page_size+1). This counter is used to keep a count of data bits sent within an FLP Burst. When this variable reaches ~~17~~ (page_size+1), all data bits have been sent.

Values: not_done; 1 to ~~16~~ page_size inclusive.
done; ~~17~~ (page_size+1).
init; counter is initialized to 1.

28.3.4 State diagrams

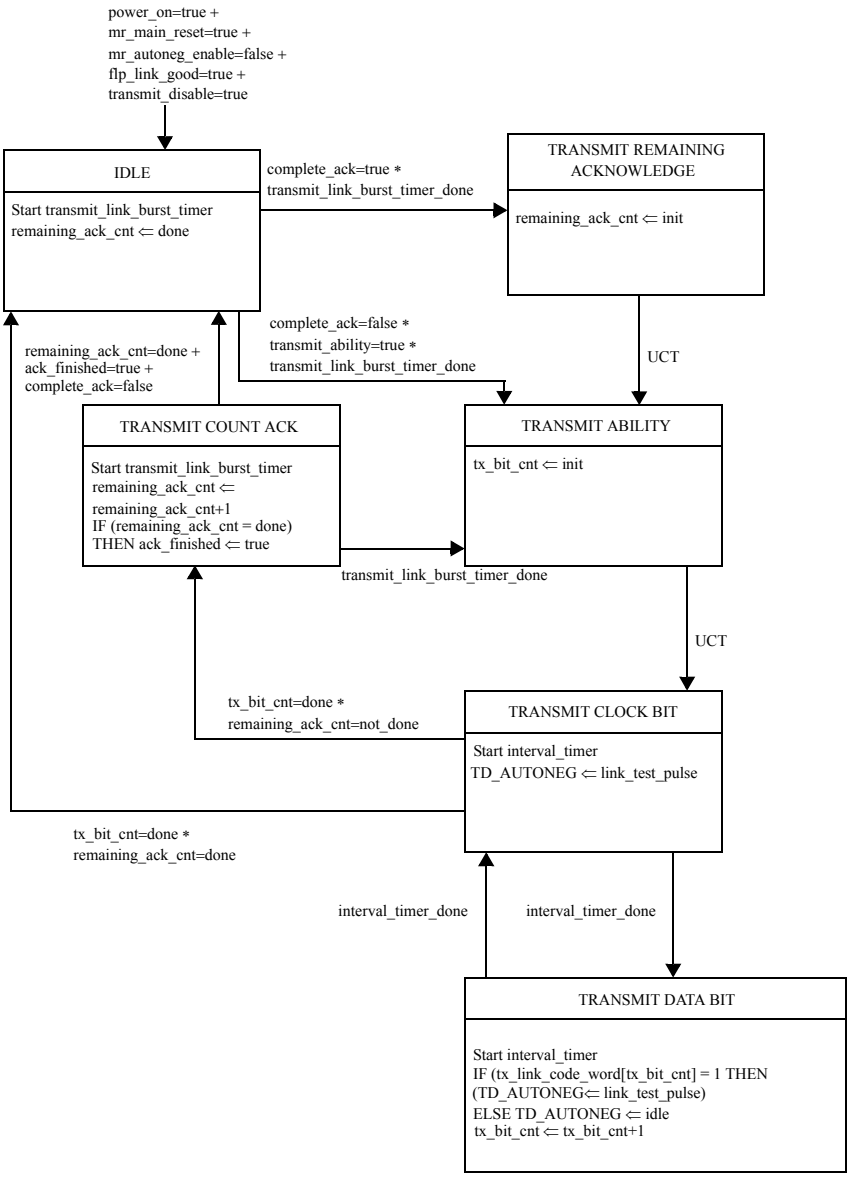


Figure 28–15—Transmit state diagram

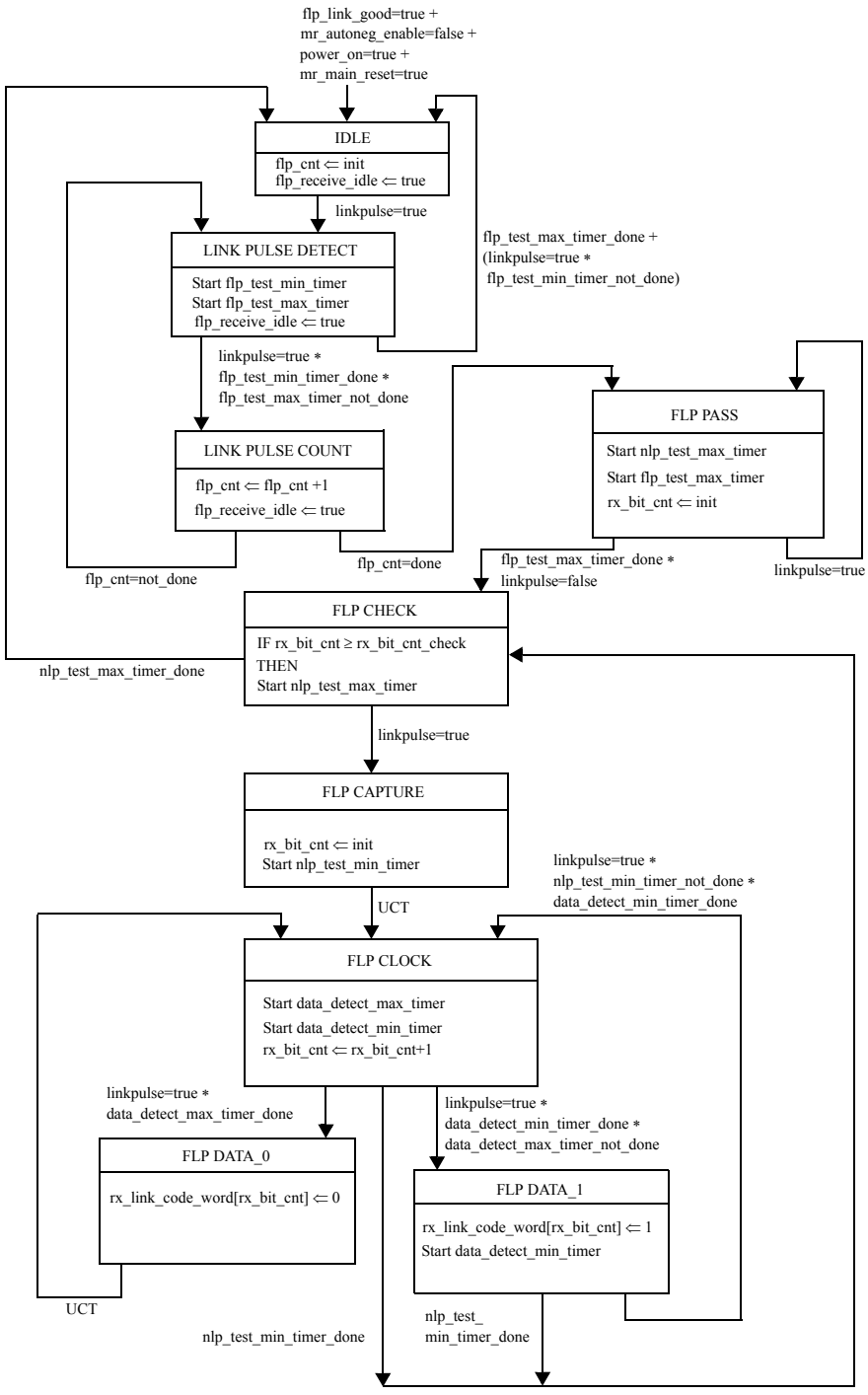
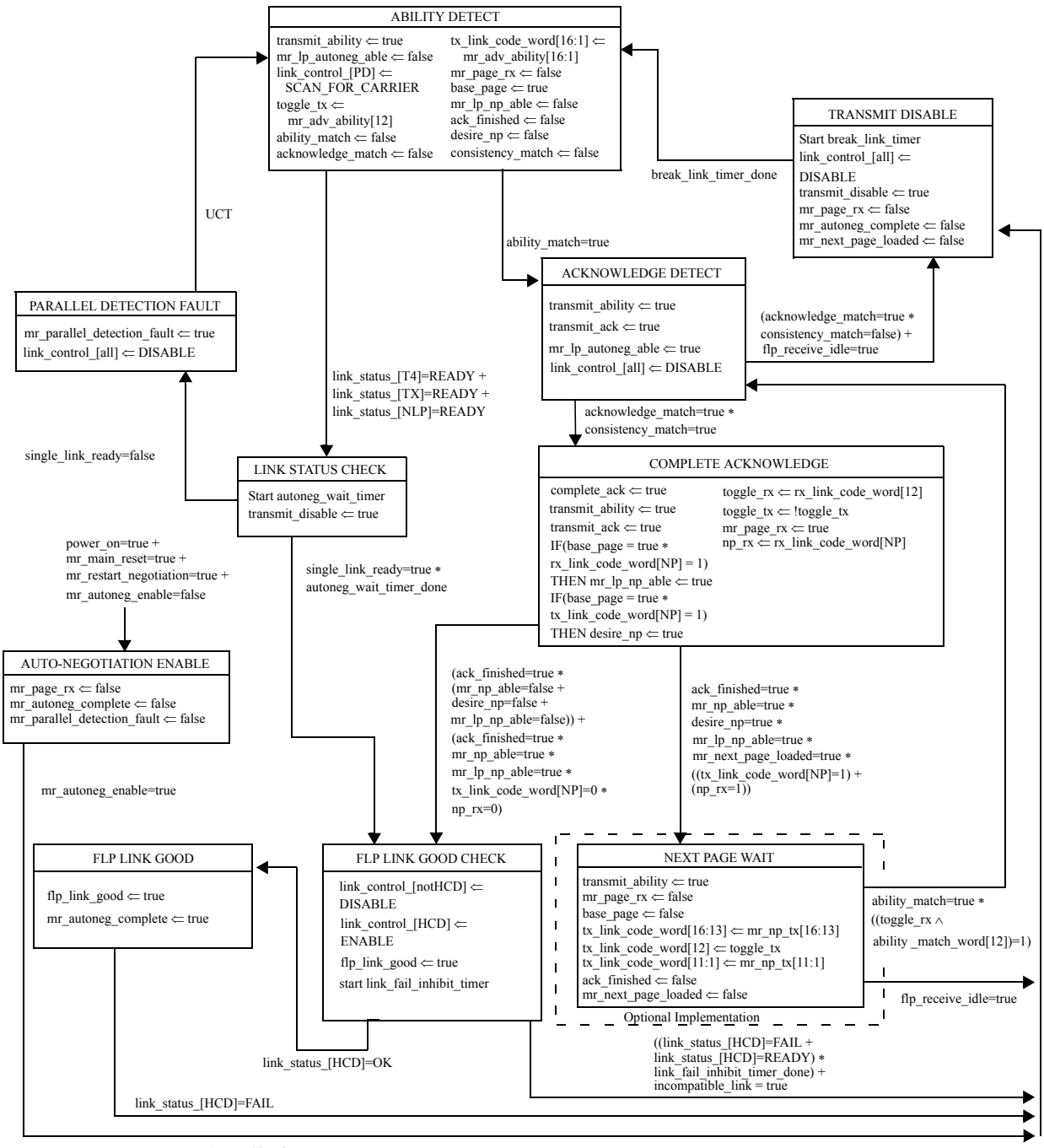


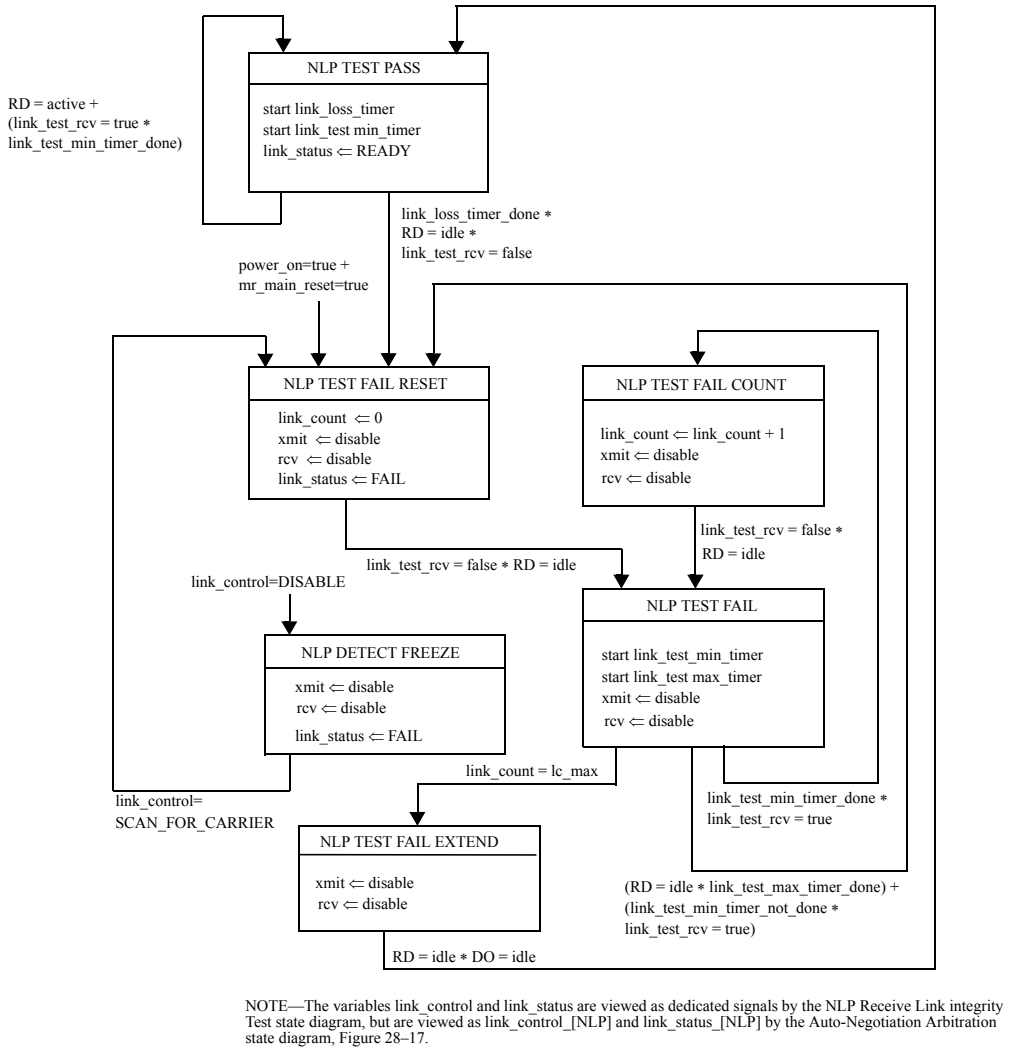
Figure 28–16—Receive state diagram



NOTE—The transition from COMPLETE ACKNOWLEDGE to FLP LINK GOOD CHECK can be simplified to "ack_finished=true" if the optional Next Page function is not supported.

NOTE—ability_match, acknowledge_match, single_link_ready, consistency_match, and incompatible_link are set according to the variable definitions and are not set explicitly in the state diagrams.

Figure 28–17—Arbitration state diagram



NOTE—The variables link_control and link_status are viewed as dedicated signals by the NLP Receive Link integrity Test state diagram, but are viewed as link_control_[NLP] and link_status_[NLP] by the Auto-Negotiation Arbitration state diagram, Figure 28–17.

Figure 28–18—NLP Receive Link Integrity Test state diagram

28.4 Electrical specifications

The electrical characteristics of pulses within FLP Bursts shall be identical to the characteristics of NLPs and shall meet the requirements of Figure 14–12.

It is the responsibility of the technology-specific Transmit and Receive functions to interface to the MDI correctly.

NOTE—The requirements relative to the interface to the MDI are specified via the Transmit Switch and Receive Switch functions.

28.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, ~~and~~ 1000 Mb/s, and 10Gb/s Auto-Negotiation on twisted pair[1]

Change title of subclause 28.5 to include 10Gb/s

28.5.1 Introduction

Change subclauses 28.5.1 and 28.5.2.2 to include 10Gb/s, and 28.5.2.2 to update the year and standard name

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, ~~and~~ 1000 Mb/s, and 10Gb/s Auto-Negotiation on twisted pair, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

28.5.2 Identification

28.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

28.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std ~~802.3-2002~~ 802.3an-200X, Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, ~~and~~ 1000 Mb/s, and 10Gb/s Auto-Negotiation on twisted pair
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Have any Exception items been required?No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std ~~802.3-2002~~ 802.3an-200X.)

Date of Statement	

28.5.3 Major capabilities/options

Change subclause 28.5.3 as follows

Item	Feature	Subclause	Status	Support	Value/comment
10BT	Implementation supports a 10BASE-T data service	28.1.2	O		N/A
*NP	Implementation supports Next Page function	28.1.2	O		N/A
*MII	Implementation supports the ~~MII~~ Clause 22 Management Interface	28.1.2	O/1		N/A
MGMT	Implementation supports a non-~~MII~~ Clause 22 Management Interface	28.1.2	O/1		N/A
*MDIO	Implementation supports the Clause 45 Management Interface	28.1.2	O/1		N/A
*NOM	Implementation does not support management	28.1.2	O/1		N/A
*RF	Implementation supports Remote Fault Sensing	28.2.3.5	O		N/A
*ENP	Implementation supports Extended Next Pages	28.2.3.4.2	O		N/A

28.5.4 PICS proforma tables for Physical Layer link signaling for 10 Mb/s, 100 Mb/s, ~~and~~ 1000 Mb/s, and 10Gb/s Auto-Negotiation on twisted pair

Change title of subclause 28.5.4 to include 10Gb/s

28.5.4.1 Scope

Item	Feature	Subclause	Status	Support	Value/comment
1	MII Management Interface control and status registers	28.1.3	MII:M		Implemented in accordance with the definitions in Clause 22 and 28.2.4
2	CSMA/CD compatible devices using an eight-pin modular connector and using a signaling method to automatically configure the preferred mode of operation	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
3	Device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
4	Future CSMA/CD implementations that use an eight-pin modular connector	28.1.4	M		Interoperable with devices compliant with Clause 28

28.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Status	Support	Value/comment
1	Transmit	28.2	M		Complies with Figure 28–15
2	Receive	28.2	M		Complies with Figure 28–16
3	Arbitration	28.2	M		Complies with Figure 28–17
4	NLP Receive Link Integrity Test	28.2	M		Complies with Figure 28–18
5	Technology-Dependent Interface	28.2	M		Complies with 28.2.6
6	Technology-dependent link integrity test	28.2	M		Implemented and interfaced to for those technologies supported by device
7	Management	28.2	O		MII based or alternate management

28.5.4.3 Transmit function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	FLP Burst transmission	28.2.1.1	M		Not transmitted once Auto-Negotiation is complete and highest common denominator PMA has been enabled. Prohibited other than for link start-up
2	FLP Burst composition	28.2.1.1.1	M		Pulses in FLP Bursts meet the requirements of Figure 14–12
3	FLP Burst pulse definition	28.2.1.1.1	M		17 odd-numbered pulse positions represent clock information; 16 even-numbered pulse positions represent data information
4	The first pulse in an FLP Burst	28.2.1.1.2	M		Defined as a clock pulse for timing purposes
5	FLP Burst clock pulse spacing	28.2.1.1.2	M		Within an FLP Burst, spacing is 125 ± 14 µs
6	Logic one data bit representation	28.2.1.1.2	M		Pulse transmitted 62.5 ± 7 µs after the preceding clock pulse
7	Logic zero data bit representation	28.2.1.1.2	M		No link integrity test pulses within 111 µs of the preceding clock pulse
8	Consecutive FLP Bursts	28.2.1.1.2	M		The first link pulse in each FLP Burst is separated by 16 ± 8 ms
9	FLP Burst base page	28.2.1.2	M		Conforms to Figure 28–7
10	FLP Burst bit transmission order	28.2.1.2	M		Transmission is D0 first to D15 last
11	Selector Field values	28.2.1.2.1	M		Only defined values transmitted
12	Technology Ability Field values	28.2.1.2.2	M		Implementation supports a data service for each ability set in the Technology Ability Field
13	Remote Fault bit	28.2.1.2.3	M		Used in accordance with the Remote Fault function specifications
14	Acknowledge bit set, no Next Page to be sent	28.2.1.2.4	M		Set to logic one in the Link Code Word after the reception of at least three consecutive and consistent FLP Bursts
15	Acknowledge bit set, Next Page to be sent	28.2.1.2.4	NP:M		Set to logic one in the transmitted Link Code Word after the reception of at least three consecutive and consistent FLP Bursts and the current receive Link Code Word is saved

28.5.4.3 Transmit function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
16	Number of Link Code Words sent with Acknowledge bit set	28.2.1.2.4	M		6 to 8 inclusive after COMPLETE ACKNOWLEDGE state entered
17	Device does not implement optional Next Page ability	28.2.1.2.5	M		NP=0 in base Link Code Word
18	Device implements optional Next Page ability and wishes to engage in Next Page exchange	28.2.1.2.5	NP:M		NP=1 in base Link Code Word
19	Transmit Switch function on completion of Auto-Negotiation	28.2.1.3	M		Enables the transmit path from a single technology-dependent PMA to the MDI once the highest common denominator has been selected
20	Transmit Switch function during Auto-Negotiation	28.2.1.3	M		Connects FLP Burst generator governed by Figure 28–15 to the MDI
21	Signals presented at MDI after connection through Transmit Switch from PMA	28.2.1.3	M		Conform to appropriate PHY specifications

28.5.4.4 Receive function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	Timer expiration	28.2.2.1	M		Timer definition in 28.3.2, values shown in Table 28–9
2	Identification of Link Partner as Auto-Negotiation able	28.2.2.1	M		Reception of 6 to 17 (inclusive) consecutive link pulses separated by at least flp_test_min_timer time but less than flp_test_max_timer time
3	First FLP Burst identifying Link Partner as Auto-Negotiation able	28.2.2.1	M		Data recovered is discarded if FLP Burst is incomplete
4	First link pulse in an FLP Burst	28.2.2.1	M		Interpreted as a clock link pulse
5	Restart of the data_detect_min_timer and data_detect_max_timer	28.2.2.1	M		Detection of a clock link pulse (Figure 28–9)
6	Reception of logic one	28.2.2.1	M		Link pulse received between greater than data_detect_min_timer time and less than data_detect_max_timer time after a clock pulse (Figure 28–9)

28.5.4.4 Receive function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
7	Reception of logic zero	28.2.2.1	M		Link pulse received after greater than data_detect_max_timer time after clock pulse, is treated as clock pulse (Figure 28–9)
8	FLP Bursts separation	28.2.2.1	M		Conforms to the nlp_test_min_timer and nlp_test_max_timer timing (Figure 28–10)
9	Receive Switch function on completion of Auto-Negotiation	28.2.2.3	M		Enables the receive path from the MDI to a single technology-dependent PMA once the highest common denominator has been selected
10	Receive Switch function during Auto-Negotiation	28.2.2.3	M		Connects the MDI to the FLP and NLP receivers governed by Figures 28–16 and 28–18, and to the 100BASE-TX and 100BASE-T4 receivers if present
11	Signals presented to PMA after connection through Receive Switch from MDI	28.2.2.3	M		Conform to appropriate PHY specifications
12	Generation of ability_match, acknowledge_match, and consistency_match	28.2.2.4	M		Responsibility of Receive function in accordance with 28.3.1

28.5.4.5 Arbitration functions

Item	Feature	Subclause	Status	Support	Value/comment
1	MDI receive connection during Auto-Negotiation, prior to FLP detection	28.2.3.1	M		Connected to the NLP Receive Link Integrity Test state diagram, and the link integrity test functions of 100BASE-TX and/or 100BASE-T4. Not connected to the 10BASE-T or any other PMA
2	Parallel detection operational mode selection	28.2.3.1	M		Set link_control=ENABLE for the single PMA indicating link_status=READY when the autoneg_wait_timer expires
3	Parallel detection PMA control	28.2.3.1	M		Set link_control=DISABLE to all PMAs except the selected operational PMA and indicate Auto-Negotiation has completed

28.5.4.5 Arbitration functions ***(continued)***

Item	Feature	Subclause	Status	Support	Value/comment
4	Parallel detection setting of link partner ability register	28.2.3.1	M		On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the link partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function
5	Response to renegotiation request	28.2.3.2	M		Disable all technology-dependent link integrity test functions and halt transmit activity until break_link_timer expires
6	Auto-Negotiation resumption	28.2.3.2	M		Issue FLP Bursts with base page valid in tx_link_code_word[16:1] after break_link_timer expires
7	Priority resolution	28.2.3.3	M		Single PMA connected to MDI is enabled corresponding to Technology Ability Field bit common to both Local/Link Partner Device and that has highest priority as defined by
8	Effect of receipt of reserved Technology Ability Field bit on priority resolution	28.2.3.3	M		Local Device ignores during priority resolution
9	Effect of parallel detection on priority resolution	28.2.3.3	M		Local Device considers technology identified by parallel detection as HCD
10	Values for HCD and link_status_[HCD] in the event there is no common technology	28.2.3.3	M		HCD=NULL link_status_[HCD]=FAIL
11	Message Page to Unformatted Page relationship for non-matching Selector Fields	28.2.3.4	NP:M		Each series of Unformatted Pages is preceded by an Message Page containing a message code that defines how the following Unformatted Page(s) will be interpreted
12	Message Page to Unformatted Page relationship for matching Selector Fields	28.2.3.4	NP:M		Use of Message Pages is specified by the Selector Field value
13	Transmission of Null message codes	28.2.3.4	NP:M		Sent with NP=0 on completion of all Next Pages while Link Partner continues to transmit valid Next Page information
14	Reception of Null message codes	28.2.3.4	NP:M		Recognized as indicating end of Link Partner's Next Page information

28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
15	Next Page encoding	28.2.3.4.1	NP:M		Comply with Figures 28–11 and 28–12 for the NP, Ack, MP, Ack2, and T bits
16	Message/Unformatted Code Field	28.2.3.4.1	NP:M		D10-D0 encoded as Message Code Field if MP=1 or Unformatted Code Field if MP=0
17	NP bit encoding	28.2.3.4.3	NP:M		Logic 0=last page, logic 1=additional Next Page(s) follow
18	Message Page bit encoding	28.2.3.4.5	NP:M		Logic 0=Unformatted Page, logic 1=Message Page
19	Ack2 bit encoding	28.2.3.4.6	NP:M		Logic 0=cannot comply with message; logic 1= will comply with message
20	Toggle	28.2.3.4.7	NP:M		Takes the opposite value of the Toggle bit in the previously exchanged Link Code Word
21	Toggle encoding	28.2.3.4.7	NP:M		Logic zero = previous value of the transmitted Link Code Word equalled logic one Logic one = previous value of the transmitted Link Code Word equalled logic zero
22	Message Page encoding	28.2.3.4.8	NP:M		If MP=1, Link Code Word interpreted as Message Page
23	Message Code Field	28.2.3.4.9	NP:M		Combinations not shown in are reserved and may not be transmitted
24	Unformatted Page encoding	28.2.3.4.10	NP:M		If MP=0, Link Code Word interpreted as Unformatted Page
25	Minimum Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, both send a minimum of one Next Page
26	Multiple Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, exchange continues until neither Local/Remote Device has additional information; device sends Next Page with Null Message Code if it has no information to transmit
27	Unformatted Page ordering	28.2.3.4.13	NP:M		Unformatted Pages immediately follow the referencing Message Code in the order specified by the Message Code
28	Next Page Transmit register	28.2.3.4.14	NP:M		Defined in 28.2.4.1.6

28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
29	Next Page receive data	28.2.3.4.14	NP:O		May be stored in Auto-Negotiation link partner ability register
30	Remote Fault sensing	28.2.3.5	RF:M		Optional
31	Transmission of RF bit by Local Device	28.2.3.5	M		If Local Device has no method to set RF bit, it must transmit RF bit with value of RF bit in Auto-Negotiation advertisement register (4.13)
32	RF bit reset	28.2.3.5	M		Once set, the RF bit remains set until successful renegotiation with the base Link Code Word
33	Receipt of Remote Fault indication in Base Link Code Word	28.2.3.5	MII:M		Device sets the Remote Fault bit in the MII status register (1.4) to logic one if MII is present

28.5.4.6 Management function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	Mandatory MII registers for Auto-Negotiation	28.2.4.1	MII:M		Registers 0, 1, 4, 5, 6
2	Optional MII register for Auto-Negotiation	28.2.4.1	MII* NP:M		Register 7
3	Auto-Negotiation enable	28.2.4.1.1	MII:M		Set control register Auto-Negotiation Enable bit (0.12)
4	Manual Speed/Duplex settings	28.2.4.1.1	MII:M		When bit 0.12 set, control register Speed Detection (0.13) and Duplex Mode (0.8) are ignored, and the Auto-Negotiation function determines link configuration
5	Control register (Register 0) Restart Auto-Negotiation (0.9) default	28.2.4.1.1	MII:M		PHY returns value of one in 0.9 until Auto-Negotiation has been initiated
6	Control register (Register 0) Restart Auto-Negotiation (0.9) set	28.2.4.1.1	MII:M		When 0.9 set, Auto-Negotiation will (re)initiate. On completion, 0.9 will be reset by the PHY device. Writing a zero to 0.9 at any time has no effect
7	Control register (Register 0) Restart Auto-Negotiation (0.9) reset	28.2.4.1.1	MII:M		0.9 is self-clearing; writing a zero to 0.9 at any time has no effect
8	Status register (Register 1) Auto-Negotiation Complete (1.5) reset	28.2.4.1.2	MII:M		If bit 0.12 reset, or a PHY lacks the ability to perform Auto-Negotiation, (1.5) is reset

28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
9	Status register (Register 1) Remote Fault (1.4)	28.2.4.1.2	MII:M		Set by the PHY and remains set until either the status register is read or the PHY is reset
10	Advertisement register power on default	28.2.4.1.3	MII:M		Selector field as defined in Annex 28A; Ack=0; Technology Ability Field based on MII status register (1.15:11) or logical equivalent
11	Link partner ability register read/write	28.2.4.1.4	MII:M		Read only; write has no effect
12	Link partner ability register bit definitions	28.2.4.1.4	MII:M		Direct representation of the received Link Code Word (Figure 28–7)
13	Status register (Register 1) Auto-Negotiation Complete (1.5) set	28.2.4.1.4	MII:M		Set to logic one upon successful completion of Auto-Negotiation
14	Auto-Negotiation expansion register (Register 6)	28.2.4.1.5	MII:M		Read only; write has no effect
15	Link Partner Auto-Negotiation Able bit (6.0)	28.2.4.1.5	MII:M		Set to indicate that the Link Partner is able to participate in the Auto-Negotiation function
16	Page Received bit (6.1) set	28.2.4.1.5	MII:M		Set to indicate that a new Link Code Word has been received and stored in the Auto-Negotiation link partner ability register
17	Page Received bit (6.1) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)
18	The Next Page Able bit (6.2) set	28.2.4.1.5	NP* MII:M		Set to indicate that the Local Device supports the Next Page function
19	The Link Partner Next Page Able bit (6.3) set	28.2.4.1.5	MII:M		Set to indicate that the Link Partner supports the Next Page function
20	Parallel Detection Fault bit (6.4) set	28.2.4.1.5	MII:M		Set to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires
21	Parallel Detection Fault bit (6.4) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)
22	Next Page Transmit register default	28.2.4.1.6	NP* MII:M		On power-up, contains value of 2001 H

28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
23	Write to Next Page Transmit register	28.2.4.1.6	NP* MII:M		mr_next_page_loaded set to true
24	Absence of management function	28.2.5	NOM:M		Advertised abilities provided through a logical equivalent of mr_adv_ability[16:1]
25	Next Page support in absence of MII management	28.2.5	NOM:M		Device must provide logical equivalent of mr_np_able, mr_lp_np_able, or mr_next_page_loaded variables in order to set NP bit in transmitted Link Code Word

28.5.4.7 Technology-dependent interface

Item	Feature	Subclause	Status	Support	Value/comment
1	PMA_LINK.indicate(link_status) values	28.2.6.1.1	M		link_status set to READY, OK or FAIL
2	PMA_LINK.indicate(link_status) generation	28.2.6.1.2	M		Technology-dependent PMA and NLP Receive Link Integrity Test state diagram (Figure 28–18) responsibility
3	PMA_LINK.indicate(link_status), effect of receipt	28.2.6.1.3	M		Governed by the state diagram of Figure 28–17
4	PMA_LINK.request(link_control) values	28.2.6.1.3	M		link_control set to SCAN_FOR_CARRIER, DISABLE, or ENABLE
5	Effect of link_control=SCAN_FOR_CARRIER	28.2.6.2.1	M		PMA to search for carrier and report link_status=READY when carrier is received, but no other actions are enabled
6	Effect of link_control=DISABLE	28.2.6.2.1	M		Disables PMA processing
7	Effect of link_control=ENABLE	28.2.6.2.1	M		Control passed to a single PMA for normal processing functions
8	PMA_LINK.request(link_control) generation	28.2.6.2.2	M		Auto-Negotiation function responsibility in accordance with Figures 28–16 and 28–17
9	PMA_LINK.request(link_control) default upon power-on, reset, or release from power-down	28.2.6.2.2	M		link_control = DISABLE state to all technology-dependent PMAs
10	PMA_LINK.request(link_control) effect of receipt	28.2.6.2.3	M		Governed by Figure 28–18 and the receiving technology-dependent link integrity test function

28.5.4.7 Technology-dependent interface *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
11	The linkpulse parameter shall	28.2.6.3.1	M	Yes [ ]	TRUE or FALSE.
12	The linkpulse=FALSE shall be used	28.2.6.3.1	M	Yes [ ]	By the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.
13	The linkpulse=TRUE shall be used	28.2.6.3.1	M	Yes [ ]	By the Auto-Negotiation function to indicate that a valid Link Pulse has been received.
14	The Auto-Negotiation function shall generate linkpulse	28.2.6.3.2	M	Yes [ ]	To indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–16.
15	Upon power-on or reset, if Auto-Negotiation is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request(FALSE) message shall be	28.2.6.3.2	M	Yes [ ]	Issued to all technology-dependent PMAs.
16	The effect of the receipt of linkpulse shall be governed	28.2.6.3.3	M	Yes [ ]	By the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.5.4.8 State diagrams

Item	Feature	Subclause	Status	Support	Value/comment
1	Adherence to state diagrams	28.3	M		Implement all features of Figures 28–15 to 28–18. Identified options to Figures 28–15 to 28–18 are permitted
3	Ambiguous requirements	28.3	M		State diagrams take precedence in defining functional operation
4	autoneg_wait_timer	28.3.1	M		Expires between 500–1000 ms after being started
5	break_link_timer	28.3.2	M		Expires between 1200–1500 ms after being started
6	data_detect_min_timer	28.3.2	M		Expires between 15–47 μs from the last clock pulse
7	data_detect_max_timer	28.3.2	M		Expire between 78–100 μs from the last clock pulse
8	flp_test_max_timer	28.3.2	M		Expires between 165–185 μs from the last link pulse
9	flp_test_min_timer	28.3.2	M		Expires between 5–25 μs from the last link pulse

28.5.4.8 State diagrams ***(continued)***

Item	Feature	Subclause	Status	Support	Value/comment
10	interval_timer	28.3.2	M		Expires 55.5–69.5 μs from each clock pulse and data bit
11	link_fail_inhibit_timer	28.3.2	M		Expires 750–1000 ms after entering the FLP LINK GOOD CHECK state
12	nlp_test_max_timer	28.3.2	M		Expires between 50–150 ms after being started if not restarted
13	nlp_test_min_timer	28.3.2	M		Expires between 5–7 ms after being started if not restarted
14	transmit_link_burst_timer	28.3.1	M		Expires 5.7–22.3 ms after the last transmitted link pulse in an FLP Burst

28.5.4.9 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/comment
1	Pulses within FLP Bursts	28.4	M		Identical to the characteristics of NLPs and meet the requirements of Figure 14–12

28.5.4.10 Auto-Negotiation annexes

Item	Feature	Annex	Status	Support	Value/comment
1	Selector field, S[4:0] values in the Link Code Word	Annex 28A	M		Identifies base message type as defined by Table 28A–1
2	Selector field reserved combinations	Annex 28A	M		Transmission not permitted
3	Relative priorities of the technologies supported by the IEEE 802.3 Selector Field value	28B.3	M		Defined in Annex 28B.3
4	Relative order of the technologies supported by IEEE 802.3 Selector Field	28B.3	M		Remain unchanged
5	Addition of new technology	28B.3	M		Inserted into its appropriate place in the priority resolution hierarchy, shifting technologies of lesser priority lower in priority
6	Addition of vendor-specific technology	28B.3	M		Priority of IEEE 802.3 standard topologies maintained, vendor-specific technologies to be inserted into an appropriate location
7	Message Code Field	Annex 28C	NP:M		Defines how following Unformatted Pages (if applicable) are interpreted
8	Message Code Field reserved combinations	Annex 28C	NP:M		Transmission not permitted
9	Auto-Negotiation reserved code 1	28C.1	NP:M		Transmission of M10 to M0 equals 0, not permitted
10	Null Message Code	28C.2	NP:M		Transmitted during Next Page exchange when the Local Device has no information to transmit and Link Partner has additional pages to transmit
11	Remote Fault Identifier Message Code	28C.5	NP:M		Followed by single Unformatted Page to identify fault type with types defined in 28C.5

28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/comment
12	Organizationally Unique Identifier Message Code	28C.6	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of OUI (bits 23:13) with MSB in U10; Second Unformatted Page contains next most significant 11 bits of OUI (bits 12:2), with MSB in U10; Third Unformatted Page contains the least significant 2 bits of OUI (bits 1:0) with MSB in U10, bits U8:0 contains user-defined code specific to OUI; Fourth Unformatted Page contains user-defined code specific to OUI
13	PHY Identifier Message Code	28C.7	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of PHY ID (2.15:5) with MSB in U10; Second Unformatted Page contains PHY ID bits 2.4:0 to 3.15:10, with MSB in U10; Third Unformatted Page contains PHY ID bits 3.9:0, with MSB in U10, and U0 contains user-defined code specific to PHY ID; Fourth Unformatted Page contains user-defined code specific to PHY ID
14	Auto-Negotiation reserved code 2	28C.8	NP:M		Transmission of M10 to M0 equals 1, not permitted

28.6 Auto-Negotiation expansion

Auto-Negotiation is designed in a way that allows it to be easily expanded as new technologies are developed. When a new technology is developed, the following things must be done to allow Auto-Negotiation to support it:

a) The appropriate Selector Field value to contain the new technology must be selected and allocated.
b) A Technology bit must be allocated for the new technology within the chosen Selector Field value.
c) The new technology's relative priority within the technologies supported within a Selector Field value must be established.

Code space allocations are enumerated in Annex 28A, , and Annex 28C. Additions and insertions to the annexes are allowed. No changes to existing bits already defined are allowed.

Revisions to ANSI/IEEE Std 802.3, 2002, Annex 28B

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

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Annex 28B

(normative)

IEEE 802.3 Selector Base Page definition

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the base page encoding.

As new IEEE 802.3 LAN technologies are developed, a reserved bit in the Technology Ability field may be assigned to each technology by the standards body.

The new technology will then be inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation standard. The relative hierarchy of the existing technologies will not change, thus providing backward compatibility with existing Auto-Negotiation implementations.

It is important to note that the reserved bits are required to be transmitted as logic zeros. This guarantees that devices implemented using the current priority table will be forward compatible with future devices using an updated priority table.

28B.1 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

28B.2 Technology Ability Field bit assignments

The Technology bit field consists of bits D5 through D12 (A0–A7, respectively) in the IEEE 802.3 Selector Base Page. Table 28B–1 summarizes the bit assignments.

Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Setting Bit A5 or Bit A6 indicates that the DTE has implemented both the optional MAC control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium. The encoding of Bits A5 and A6 is specified in Table 28B–2.

Change Table 28B-1 as follows:
- Change bit A7 to "Extended Next Page"

Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair category 3
A1	10BASE-T full duplex	Two-pair category 3
A2	100BASE-TX	Two-pair category 5
A3	100BASE-TX full duplex	Two-pair category 5
A4	100BASE-T4	Four-pair category 3

Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A5	PAUSE operation for full duplex links	Not applicable
A6	Asymmetric PAUSE operation for full duplex Links	Not applicable
A7	~~Reserved for future technology~~ Extended Next Page	Not applicable

Table 28B–2—Pause encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

28B.3 Priority resolution

Since two devices may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

Insert "10GBASE-T full duplex" as bullet (a) and renumber other bullets in subclause 28B.3

a) 10GBASE-T full duplex
b) 1000BASE-T full duplex
c) 1000BASE-T
d) 100BASE-T2 full duplex
e) 100BASE-TX full duplex
f) 100BASE-T2
g) 100BASE-T4
h) 100BASE-TX
i) 10BASE-T full duplex
j) 10BASE-T

The rationale for this hierarchy is straightforward. 10BASE-T is the lowest common denominator and therefore has the lowest priority. Full duplex solutions are always higher in priority than their half duplex counterparts. 1000BASE-T has a higher priority than 100 Mb/s technologies. 100BASE-T2 is ahead of 100BASE-TX and 100BASE-T4 because 100BASE-T2 runs across a broader spectrum of copper cabling and can support a wider base of configurations. 100BASE-T4 is ahead of 100BASE-TX because 100BASE-T4 runs across a broader spectrum of copper cabling. The relative order of the technologies specified herein

shall not be changed. As each new technology is added, it shall be inserted into its appropriate place in the list, shifting technologies of lesser priority lower in priority. If a vendor-specific technology is implemented, the priority of all IEEE 802.3 standard technologies shall be maintained, with the vendor specific technology inserted at any appropriate priority location.

The use of the PAUSE operation for full duplex links (as indicated by bits A5 and A6) is orthogonal to the negotiated data rate, medium, or link technology. The setting of these bits indicates the availability of additional DTE capability when full duplex operation is in use. The PAUSE function shall be enabled according to Table 28B–3 only if the Highest Common Denominator is a full duplex technology. There is no priority resolution associated with the PAUSE operation.

Table 28B–3—Pause resolution

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	Don't care	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don't care	1	Don't care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

Insert the following text in subclause 28B.3

The use of Extended Next Page (as indicated by bit A7) is orthogonal to the negotiated date rate, medium, or link technology. This ability shall be enabled at the end of base page exchange when both sides have indicated that they support the ability. Otherwise the ability shall be disabled.

28B.4 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a Message Code that defines how the following Unformatted Pages will be used.

Next Page message codes should be allocated globally across Selector Field values so that meaningful communication is possible between technologies using different Selector Field values.

Revisions to ANSI/IEEE Std 802.3, 2002, Annex 28C

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

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Annex 28C

(normative)

Next Page Message Code Field definitions

The Message Code Field of a message page used in Next Page exchange shall be used to identify the meaning of a message. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

Insert the following text in subclause 28C. ChangeTable 28C-1 as follows, substituting "X" for all items in the M10 column and rename rows 9 - 2047 as indicated

The Message Code Field uses an 11-bit binary encoding that allows 2048 messages to be defined. All Message Codes not specified shall be reserved for IEEE use or allocation. Bit M10 of the Message Code Field indicates the use of 48-bit extended next pages. When Bit M10 is a one, the next page will contain 48 bits, and when Bit M10 is a zero, the next page will contain 16 bits.

Extended Next Pages may be used to send multiple 16-bit next pages in the following manner. The 11-bit Message Code Field is mapped to bits M0:10 of the extended next page, and the first two unformatted pages associated with the Message Code Field are mapped to bits U0:U10 and U16:U26, respectively of the extended next page. Additional unformatted pages would be mapped to bits M0:10, U0:10, and U16:26 of subsequent extended next pages. Any unused bits in the extended next page are transmitted as zero or one and ignored by the receiver.

Table 28C–1—Message code field values

Message Code #	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message Code Description
0	X	0	0	0	0	0	0	0	0	0	0	Reserved for future Auto-Negotiation use
1	X	0	0	0	0	0	0	0	0	0	1	Null Message
2	X	0	0	0	0	0	0	0	0	1	0	One UP with Technology Ability Field follows
3	X	0	0	0	0	0	0	0	0	1	1	Two UPs with Technology Ability Field follow
4	X	0	0	0	0	0	0	0	1	0	0	One UP with Binary coded Remote fault follows
5	X	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	X	0	0	0	0	0	0	0	1	1	0	PHY Identifier Tag Code
7	X	0	0	0	0	0	0	0	1	1	1	100BASE-T2 Technology Message Code. 100BASE-T2 Ability Page to follow using Unformatted Next Page

Table 28C–1—Message code field values *(continued)*

8	X	0	0	0	0	0	0	1	0	0	0	1000BASE-T Technology Message Code. Two 1000BASE-T Ability Pages to follow using Unformatted Next Pages.
9	X	0	0	0	0	0	0	1	0	0	1	10GBASE-T Technology Message Code (extended next page)
10.....	X	0	0	0	0	0	0	1	0	1	0	Reserved for future Auto-Negotiation use
.....1023	X	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

28C.1 Message code #0—Auto-Negotiation reserved code 1

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.2 Message code #1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 28.2.3.4 for more details.

28C.3 Message code #2—Technology Ability extension code 1

This Message Code is reserved for future expansion of the Technology Ability Field and indicates that a defined user code with a specific Technology Ability Field encoding follows.

28C.4 Message code #3—Technology Ability extension code 2

This Message Code is reserved for future expansion of the Technology Ability Field and indicates that two defined user codes with specific Technology Ability Field encodings follow.

28C.5 Message code #4—Remote fault number code

This Message Code shall be followed by a single user code whose encoding specifies the type of fault that has occurred. The following user codes are defined:

0: RF Test
This code can be used to test Remote Fault operation.
1: Link Loss
2: Jabber
3: Parallel Detection Fault
This code may be sent to identify when bit 6.4 is set.

28C.6 Message code #5—Organizationally Unique Identifier (OUI) tag code

The OUI Tagged Message shall consist of a single message code of 0000 0000 0101 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the OUI (bits 23:13) with the most significant bit in bit 10 of the user code. The second user code shall contain the next most significant 11 bits of the OUI (bits 12:2) with the most significant bit in bit 10 of the user code. The third user code shall contain the remaining least significant 2 bits of the OUI (bits 1:0) with the most significant bit in bit 10 of the user code. Bits 8:0 of the fourth user contain a user-defined user code value that is specific to the OUI transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the OUI transmitted.

28C.7 Message code #6—PHY identifier tag code

The PHY ID tag code message shall consist of a single message code of 0000 0000 0110 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the PHY ID (2.15:5) with the most significant bit in bit 10 of the user code. The second user code shall contain bits 2.4:0 to 3.15:10 of the PHY ID with the most significant bit in bit 10 of the user code. The third user code shall contain bits 3.9:0 of the PHY ID with the most significant bit in bit 10 of the user code. Bit 0 in the third user code shall contain a user-defined user code value that is specific to the PHY ID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the PHY ID transmitted.

28C.8 Message code #2047— Auto-Negotiation reserved code 2

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.9 Message code #7—100BASE-T2 technology message code

Clause 32 (100BASE-T2) uses Next Page Message Code 7 to indicate that T2 implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages which contain information defined in 32.5.4.2.

28C.10 Message Code #8—1000BASE-T technology message code

Clause 40 (1000BASE-T) uses Next Page Message Code 8 to indicate that 1000BASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages that contain information defined in 40.5.1.2.

Insert the following subclause 28C.11

28C.11 Message Code #9—10GBASE-T and 1000BASE-T technology message code

#CrossRef# Clause 55 (10GBASE-T) uses Next Page Message Code 9 to indicate that 10GBASE-T and 1000BASE-T abilities are contained within this extended Next Page. The Next Page that contains this information is defined in #CrossRef# TBD. This page shall not be sent if extended next page mode is disabled.

Revisions to ANSI/IEEE Std 802.3, 2002, Annex 28D

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

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Annex 28D

(normative)

Description of extensions to Clause 28 and associated annexes

28D.1 Introduction

This annex is to be used to document extensions and modifications to Clause 28 required by IEEE 802.3 clauses and other standards that use Auto-Negotiation and that were approved after June 1995. It provides a single location to define such extensions and modifications without changing the basic contents of Clause 28.

Subclause 28D.2 lists those clauses and standards that require extensions to Clause 28 and provides pointers to the subclauses where those extensions are listed.

28D.2 Extensions to Clause 28

28D.2.1 Extensions required for Clause 31 (full duplex)

Clause 31 (full duplex) requires the use of Auto-Negotiation. Extensions to Clause 28 and associated annexes required for the correct operation of full duplex are shown in 28D.3.

28D.2.2 Extensions required for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) requires the use of Auto-Negotiation. Extensions to Clause 28 required for correct operation of 100BASE-T2 are shown in 28D.4.

28D.3 Extensions for Clause 31

Full duplex requires the use of bit A5 in the Technology Ability Field of the IEEE 802.3 Selector Base Page. (This bit is also defined as MII bit 4.10.) This bit was previously defined as “reserved for future technology.”

Bit	Technology	Minimum cabling requirement
A5	PAUSE operation for full duplex links	Not applicable

Bit A5 (PAUSE operation for full duplex links) signifies that the DTE has implemented both the optional MAC Control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium.

28D.4 Extensions for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 32.5.

Auto-Negotiation is mandatory for 100BASE-T2 (32.1.3.4).

100BASE-T2 introduces the concept of MASTER and SLAVE to define DTEs and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER/SLAVE status (32.5.4.3).

100BASE-T2 uses unique next page transmit and receive registers (MII Registers 8, 9 and 10) in conjunctions with Auto-Negotiation. These registers are in addition to Registers 0–7 as defined in 28.2.4 (32.5.2).

100BASE-T2 use of Auto-Negotiation generates information which is stored in configuration and status bits defined for the MASTER-SLAVE Control register (MII Register 9) and the MASTER-SLAVE Status register (MII Register 10).

100BASE-T2 requires an ordered exchange of next page messages (32.5.1).

100BASE-T2 parameters are configured based on information provided by the ordered exchange of next page messages.

100BASE-T2 adds new message codes to be transmitted during Auto-Negotiation (32.5.4.2).

100BASE-T2 adds 100BASE-T2 full duplex and half duplex capabilities to the priority resolution table (28B.3) and MII Status Register (22.2.4.2).

T2 is defined as a valid value for “x” in 28.3.1 (e.g., link_status_T2). T2 represents that the 100BASE-T2 PMA is the signal source.

28D.5 Extensions required for Clause 40 (1000BASE-T)

Clause 40 (1000BASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 40.5.

a) Auto-Negotiation is mandatory for 1000BASE-T. (40.5.1)
b) 1000BASE-T requires an ordered exchange of Next Page messages. (40.5.1.2)
c) 1000BASE-T parameters are configured based on information provided by the ordered exchange of NEXT Page messages.
d) 1000BASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.(40.5.2)
e) 1000BASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2 and 40.5.1.1), which are required in addition to registers 0-8 as defined in 28.2.4.
f) 1000BASE-T adds new message codes to be transmitted during Auto-Negotiation. (40.5.1.3)
g) 1000BASE-T adds 1000BASE-T full duplex and half duplex capabilities to the priority resolution table. (28B.3) and MII Extended Status Register (22.2.2.4)
h) 1000BASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_1GigT.) 1GigT represents that the 1000BASE-T PMA is the signal source.

Insert the following subclause 28D.6

28D.6 Extensions required for #CrossRef# Clause 55 (10GBASE-T)

Clause 55 (10GBASE-T) makes special use of Auto-Negotiation and requires additional MDIO registers. This use is summarized below. Details are provided in 55.6.

a) Auto-Negotiation is mandatory for 10GBASE-T.
b) 10GBASE-T requires an ordered exchange of Next Page messages.
c) 10GBASE-T parameters are configured based on information provided by the ordered exchange of NEXT Page messages.
d) 10GBASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.
e) 10GBASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MDIO registers TBD.
f) 10GBASE-T adds new message codes to be transmitted during Auto-Negotiation.
g) 10GBASE-T adds 10GBASE-T full duplex capabilities to the priority resolution table (28B.3) and TBD.
h) 10GBASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_10GigT.) 10GigT represents that the 10GBASE-T PMA is the signal source.

Revisions to IEEE P802.3REVam, Clause 44

EDITORIAL NOTES - This revision is based on the current edition of IEEE P802.3REVam. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

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Change the SECTION FOUR title to include Clause 55:

SECTION FOUR: This section includes Clause 44 through Clause ~~54~~55 and Annex 44A through Annex 50A.

44. Introduction to 10 Gb/s baseband network

44.1 Overview

44.1.1 Scope

Change the first paragraph of 44.1.1 to read:

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, ~~and~~ 10GBASE-EW, and 10GBASE-T.

10 Gigabit Ethernet extends the IEEE 802.3 MAC beyond 1000 Mb/s to 10 Gb/s. The bit rate is faster and the bit times are shorter—both in proportion to the change in bandwidth. The minimum packet transmission time has been reduced by a factor of ten. A rate control mode (see 4.2.3.2.2) is added to the MAC to adapt the average MAC data rate to the SONET/SDH data rate for WAN-compatible applications of this standard. Achievable topologies for 10 Gb/s operation are comparable to those found in 1000BASE-X full duplex mode and equivalent to those found in WAN applications.

10 Gigabit Ethernet is defined for full duplex mode of operation only.

44.1.2 Objectives

Insert new objective g) and shift existing objective g) to h):

The following are the objectives of 10 Gigabit Ethernet:

a) Support the full duplex Ethernet MAC.
b) Provide 10 Gb/s data rate at the XGMII.
c) Support LAN PMDs operating at 10 Gb/s, and WAN PMDs operating at SONET STS-192c/SDH VC-4-64c rate.
d) Support cable plants using optical fiber compliant with ISO/IEC 11801: 1995.
e) Allow for a nominal network extent of up to 40 km.
f) Support operation over a twinaxial cable assembly for wiring closet and data center applications.

g) Support operation over selected copper medium from ISO/IEC 11801:2002.
h) Support a BER objective of 10^{-12}.

44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

Change Figure 44-1 to include 10GBASE-T:

10 Gigabit Ethernet couples the IEEE 802.3 (CSMA/CD) MAC to a family of 10 Gb/s Physical Layers. The relationships among 10 Gigabit Ethernet, the IEEE 802.3 (CSMA/CD) MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 44–1.

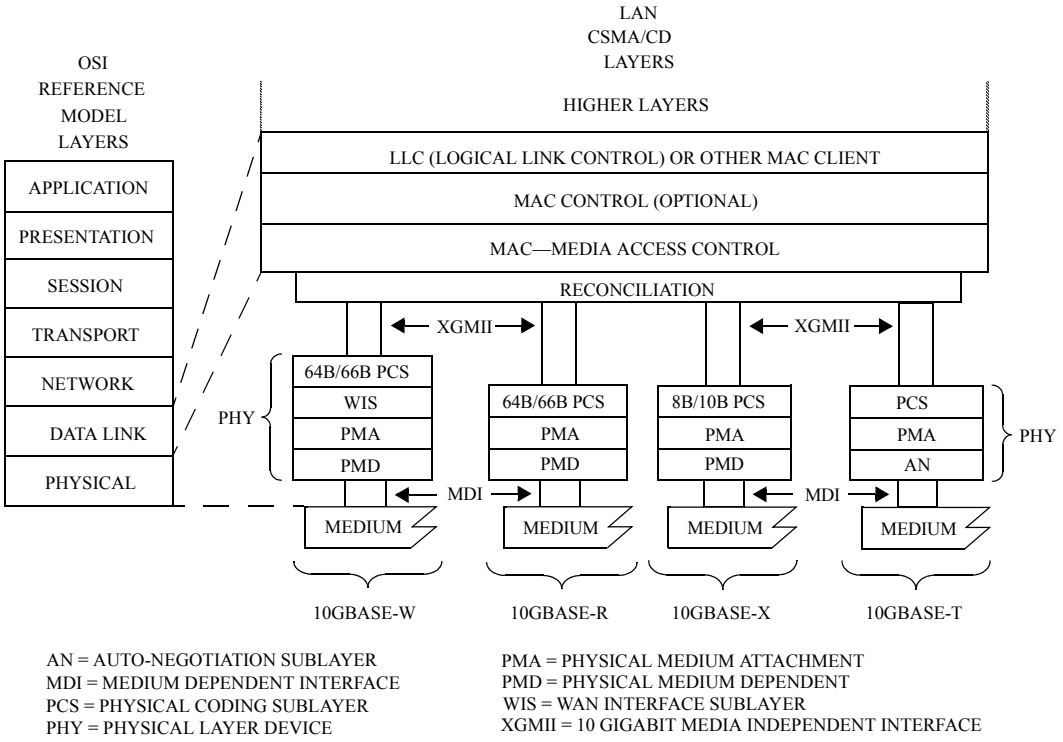


Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

Insert reference to Clause 55 for 10GBASE-T in bullet d):

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XGMII, which, when implemented at an observable interconnection port, uses a four octet-wide data path as specified in Clause 46.
b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.
c) The PMA Service Interface, which, when physically implemented as the XSBI (10 Gigabit Sixteen Bit Interface) at an observable interconnection port, uses a 16-bit-wide data path as specified in Clause 51.
d) The MDI as specified in Clause 53 for 10GBASE-LX4, in Clause 54 for 10GBASE-CX4, in Clause 55 for 10GBASE-T and in Clause 52 for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

The 10 Gigabit Media Independent Interface (Clause 46) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY). This XGMII supports 10 Gb/s operation through its 32-bit-wide transmit and receive data paths. The Reconciliation Sublayer provides a mapping between the signals provided at the XGMII and the MAC/PLS service definition.

Change to add reference to Clause 55:

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clauses 47, 48, ~~and~~ 49, and 55.

44.1.4.2 XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)

The 10 Gigabit Attachment Unit Interface (Clause 47) provides an interconnection between two XGMII Extender sublayers to increase the reach of the XGMII. This XAUI supports 10 Gb/s operation through its four-lane, differential-pair transmit and receive paths. The XGXS provides a mapping between the signals provided at the XGMII and the XAUI.

44.1.4.3 Management interface (MDIO/MDC)

The MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

44.1.4.4 Physical Layer signaling systems

Insert 10GBASE-T into Table 44-1:

This standard specifies a family of Physical Layer implementations. The generic term 10 Gigabit Ethernet refers to any use of the 10 Gb/s IEEE 802.3 MAC (the 10 Gigabit Ethernet MAC) coupled with any IEEE 802.3 10GBASE physical layer implementation. Table 44–1 specifies the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures shall meet the requirements of the corresponding clauses.

The term 10GBASE-X, specified in Clause 48, Clause 53, and Clause 54, refers to a specific family of physical layer implementations based upon 8B/10B data coding method. The 10GBASE-X family of physical layer implementations is composed of 10GBASE-LX4 and 10GBASE-CX4.

The term 10GBASE-R, specified in Clauses 49, 51, and 52, refers to a specific family of physical layer implementations based upon 64B/66B data coding method. The 10GBASE-R family of physical layer implementations is composed of 10GBASE-SR, 10GBASE-LR, and 10GBASE-ER.

The term 10GBASE-W, specified in Clause 49 to Clause 52, refers to a specific family of physical layer implementations based upon STS-192c/SDH VC-4-64c encapsulation of 64B/66B encoded data. The 10GBASE-W family of physical layer standards has been adapted from the ANSI T1.416-1999 (SONET STS-192c/SDH VC-4-64c) physical layer specifications. The 10GBASE-W family of physical layer implementations is composed of 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

All 10GBASE-R and 10GBASE-W PHY devices share a common PCS specification (see Clause 49). The 10GBASE-W PHY devices also require the use of the WAN Interface Sublayer, (WIS) (Clause 50).

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause									
	48	49	50	51	52			53	54	55
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane electrical PMD	Twisted-pair PCS & PMA
10GBASE-SR		M[a]		M	M					
10GBASE-SW		M	M	M	M					
10GBASE-LX4	M							M		
10GBASE-CX4	M								M	
10GBASE-LR		M		M		M				
10GBASE-LW		M	M	M		M				
10GBASE-ER		M		M			M			
10GBASE-EW		M	M	M			M			
10GBASE-T										M

[a]M = Mandatory

Insert text for 10GBASE-T:

The term 10GBASE-T, specified in Clause 55, refers to a specific physical layer implementation based upon 64B/65B data coding placed in a low density parity check (LDPC) frame which is mapped to a 128 double-square (128DSQ) constellation for transmission on 4-pair, twisted-pair copper cabling.

Change last paragraph of 44.1.4.4 to include Clause 55:

Specifications of each physical layer device are contained in Clause 52 through Clause ~~54~~55 inclusive.

44.1.4.5 WAN Interface Sublayer (WIS), type 10GBASE-W

The WIS provides a 10GBASE-W device with the capability to transmit and receive IEEE 802.3 MAC frames within the payload envelope of a SONET STS-192c/SDH VC-4-64c frame.

44.1.5 Management

Managed objects, attributes, and actions are defined for all 10 Gigabit Ethernet components. Clause 30 consolidates all IEEE 802.3 management specifications so that 10/100/1000 Mb/s and 10 Gb/s agents can be managed by existing network management stations with little or no modification to the agent code.

44.2 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

44.3 Delay constraints

Insert entry into Table 44-2 for 10GBASE-T round trip delays:

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 44–2 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay in bit time as specified in 1.4 and pause_quanta as specified in 31B.2.

Table 44–2—Round-trip delay constraints (informative)

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC, RS and MAC Control	8192	16	See 46.1.4.
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2048	4	See 48.5.
10GBASE-R PCS	3584	7	See 49.2.15.
10GBASE-T PCS and PMA	TBD	TBD	See TBD.
WIS	14336	28	See 50.3.7.
LX4 PMD	512	1	Includes 2 meters of fiber. See 53.2.
CX4 PMD	512	1	See 54.3
Serial PMA and PMD	512	1	Includes 2 meters of fiber. See 52.2.

Equation (44–1) specifies the calculation of bit time per meter of fiber or electrical cable based upon the parameter *n*, which represents the ratio of the speed of electromagnetic propagation in the fiber or electrical cable to the speed of light in a vacuum. The value of *n* should be available from the fiber or electrical cable manufacturer, but if no value is known then a conservative delay estimate can be calculated using a default value of $n = 0.66$. The speed of light in a vacuum is $c = 3 \times 10^8$ m/s. Table 44–3 can be used to convert fiber or electrical cable delay values specified relative to the speed of light or in nanoseconds per meter.

$$\text{cable delay} = \frac{10^{10}}{nc} \text{ BT/m} \qquad (44\text{–}1)$$

44.4 Protocol Implementation Conformance Statement (PICS) proforma

Change reference to be Clause 55:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clause 45 through Clause ~~54~~55, demonstrates compliance by completing a Protocol Implementation Conformance Statement (PICS) proforma.

Table 44–3—Conversion table for cable delays

Speed relative to c	ns/m	BT/m
0.40	8.33	83.3
0.50	6.67	66.7
0.51	6.54	65.4
0.52	6.41	64.1
0.53	6.29	62.9
0.54	6.17	61.7
0.55	6.06	60.6
0.56	5.95	59.5
0.57	5.85	58.5
0.58	5.75	57.5
0.5852	5.70	57.0
0.59	5.65	56.5
0.60	5.56	55.6
0.61	5.46	54.6
0.62	5.38	53.8
0.63	5.29	52.9
0.64	5.21	52.1
0.65	5.13	51.3
0.654	5.10	51.0
0.66	5.05	50.5
0.666	5.01	50.1
0.67	4.98	49.8
0.68	4.90	49.0
0.69	4.83	48.3
0.7	4.76	47.6
0.8	4.17	41.7
0.9	3.70	37.0

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 10 Gigabit Ethernet PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

44.5 Relation of 10 Gigabit Ethernet to other standards

Suitable entries for Table G1 of ISO/IEC 11801: 1995, Annex G, would be as follows:

a) Within the section Optical Link:
CSMA/CD 10GBASE-SR ISO/IEC 8802-3/ PDAM 26

b) Within the section Optical Link:
CSMA/CD 10GBASE-SW ISO/IEC 8802-3/PDAM 26

c) Within the section Optical Link:
CSMA/CD 10GBASE-LR ISO/IEC 8802-3/PDAM 26

d) Within the section Optical Link:
CSMA/CD 10GBASE-LW ISO/IEC 8802-3/PDAM 26

e) Within the section Optical Link:
CSMA/CD 10GBASE-ER ISO/IEC 8802-3/PDAM 26

f) Within the section Optical Link:
CSMA/CD 10GBASE-EW ISO/IEC 8802-3/PDAM 26

g) Within the section Optical Link:
CSMA/CD 10GBASE-LX4 ISO/IEC 8802-3/PDAM 26

A suitable entry for Table G5 of ISO/IEC 11801: 1995, Annex G, is exemplified in Table 44–4.

Table 44–4—Table G5 of ISO/IEC 11801: 1995

	Fibre			**Optical link per Clause 8**								
	per Clauses 5, 7, and 8			**Horizontal**			**Building backbone**			**Campus backbone**		
	62.5/ 125 μm MMF	**50/125 μm MMF**	**10/125 μm SMF**	**62.5/ 125 μm MMF**	**50/ 125 μm MMF**	**10/ 125 μm SMF**	**62.5/ 125 μm MMF**	**50/ 125 μm MMF**	**10/ 125 μm SMF**	**62.5/ 125 μm MMF**	**50/ 125 μm MMF**	**10/ 125 μm SMF**
8802-3: 10GBASE-SR	I	I		I	N		I	I		I	I	
8802-3: 10GBASE-SW	I	I		I	N		I	I		I	I	
8802-3: 10GBASE-LR	I	I	I	I	I	N	I	I	N	I	I	N
8802-3: 10GBASE-LW	I	I	I	I	I	N	I	I	N	I	I	N
8802-3: 10GBASE-ER			I			N			N			N
8802-3: 10GBASE-EW			I			N			N			N
8802-3: 10GBASE-LX4	I	I	I	N	N	N	N	N	N	N	N	N
NOTE—"N" denotes normative support of the media in the standard. "I" denotes that there is information in the International Standard regarding operation on this media.												

Revisions to ANSI/IEEE Std 802.3, 2002, Clause 45

EDITORIAL NOTES - This supplement is based on the current edition of IEEE Std 802.3, 2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3an.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 1.2, December 2004	Third draft for IEEE P802.3an Task Force review.

45. Management Data Input/Output (MDIO) Interface

45.1 Overview

This clause defines the logical and electrical characteristics of an extension to the two signal Management Data Input/Output (MDIO) Interface specified in Clause 22.

The purpose of this extension is to provide the ability to access more device registers while still retaining logical compatibility with the MDIO interface defined in Clause 22. Clause 22 specifies the MDIO frame format and uses an ST code of 01 to access registers. In this clause, additional registers are added to the address space by defining MDIO frames that use an ST code of 00.

This extension to the MDIO interface is applicable to the following:

— Implementations that operate at speeds of 10 Gb/s and above
— Implementations of 10PASS-TS and 2BASE-TL subscriber network Physical layer devices
— Implementations of 10, 100 or 1000 Mb/s with additional management functions beyond those defined in Clause 22

The MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

Throughout this clause, an “a.b.c” format is used to identify register bits, where “a” is the device address, “b” is the register address, and “c” is the bit number within the register.

45.1.1 Summary of major concepts

The following are major concepts of the MDIO Interface:

a) Preserve the management frame structure defined in 22.2.4.5.
b) Define a mechanism to address more registers than specified in 22.2.4.5.
c) Define ST and OP codes to identify and control the extended access functions.
d) Provide an electrical interface specification that is compatible with common digital CMOS ASIC processes.

45.1.2 Application

This clause defines a management interface between Station Management (STA) and the sublayers that form a Physical Layer device (PHY) entity. Where a sublayer, or grouping of sublayers, is an individually manageable entity, it is known as an MDIO Manageable Device (MMD). This clause allows a single STA, through a single MDIO interface, to access up to 32 PHYs (defined as PRTAD in the frame format defined in 45.3) consisting of up to 32 MMDs as shown in Figure 45–1. The MDIO interface can support up to a maximum of 65 536 registers in each MMD.

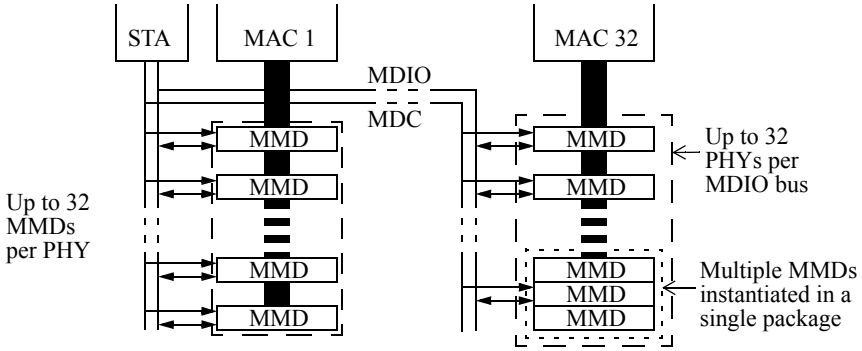


Figure 45–1—DTE and MMD devices

45.2 MDIO Interface Registers

The management interface specified in Clause 22 provides a simple, two signal, serial interface to connect a Station Management entity and a managed PHY for providing access to management parameters and services. The interface is referred to as the MII management interface.

The MDIO interface is based on the MII management interface, but differs from it in several ways. The MDIO interface uses indirect addressing to create an extended address space allowing a much larger number of registers to be accessed within each MMD. The MDIO address space is orthogonal to the MII management interface address space. The mechanism for the addressing is defined in 45.3. The MDIO electrical interface operates at lower voltages than those specified for the MII management interface. The electrical interface is specified in 45.4. For cases where a single entity combines Clause 45 MMDs with Clause 22 registers, then the Clause 22 registers may be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. The list of possible MMDs is shown in Table 45–1. The PHY XS and DTE XS devices are the two partner devices used to extend the interface that sits immediately below the Reconciliation Sublayer. For 10 Gigabit Ethernet, the interface extenders are defined as the XGXS devices. For 10PASS-TS and 2BASE-TL, control and monitoring of the TC sublayer is defined in the TC MMD. For 10, 100 and 1000 Mb/s PHYs, further management capability is defined in the Clause 22 extension MMD.

10PASS-TS and 2BASE-TL each have two port sub-types, 10PASS-TS-O, 10PASS-TS-R, 2BASE-TL-O and 2BASE-TL-R. Hereafter, referred to generically as -O and -R. The -O sub-type corresponds to the port located at the service provider end of a subscriber link (the central office end). The -R sub-type corresponds to the port located at the subscriber end of a subscriber link (the remote end). See 61.1 for more information.

Some register behaviour may differ based on the port sub-type. In the case where a register's behaviour or definition differs between port sub-types, it is noted in the register description and in the bit definition tables (denoted by "O:" and "R:" in the R/W column).

The Clause 22 extension MMD allows new features to be added to 10, 100 and 1000 Mb/s PHYs beyond those already defined in Clause 22.

If a device supports the MDIO interface it shall respond to all possible register addresses for the device and return a value of zero for undefined and unsupported registers. Writes to undefined registers and read-only

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC
7 through 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

registers shall have no effect. The operation of an MMD shall not be affected by writes to reserved and unsupported register bits, and such register bits shall return a value of zero when read.

In the case of two registers that together form a 32-bit counter, whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, the value being latched before the contents of the most significant 16 bits are driven on the MDIO interface and the contents of both registers is cleared to all zeros. A subsequent read from the least significant 16-bit register will return the least significant 16 bits of the latched value, but will not change the contents of the register pair. Writing to these registers has no effect. Counters that adhere to this behaviour are marked in their bit definition tables with the tag “MW = Multi-word”.

To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

Some of the bits within MMD registers are defined as latching low (LL) or latching high (LH). When a bit is defined as latching low and the condition for the bit to be low has occurred, the bit shall remain low until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors. When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

For multi-bit fields, the lowest numbered bit of the field in the register corresponds to the least significant bit of the field.

Figure 45–2 describes the signal terminology used for the MMDs.

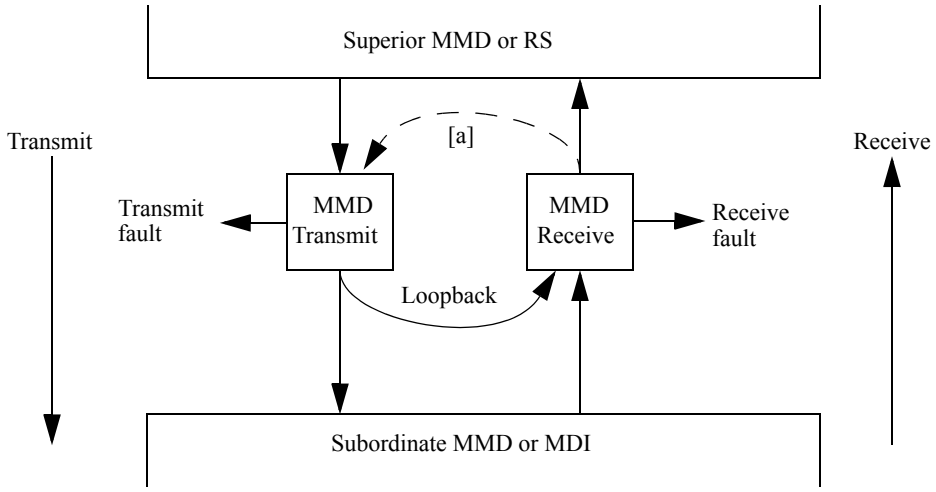


Figure 45–2—MMD signal terminology

[a] Direction of the optional PHY XS loopback

Each MMD contains registers 5 and 6, as defined in Table 45–2a. Bits read as a one in this register indicate which MMDs are instantiated within the same package as the MMD being accessed. Bit 5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. Bit 6.13 indicates that Clause 22 functionality is extended using the Clause 45 electrical interface through MMD 29. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.1 PMA/PMD registers

The assignment of registers in the PMA/PMD is shown in Table 45–2.

Insert registers 1.129 through 1.131. Renumber reserved registers to end with 1.128 and restart with 1.132.

Table 45–2— Devices in package registers bit definitions

Bit(s)[a]	Name	Description	R/W[b]
m.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
m.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
m.6.13	Clause 22 extension present	1 = Clause 22 extension present in package 0 = Clause 22 extension not present in package	RO
m.6.12:0	Reserved	Ignore on read	RO
m.5.15:7	Reserved	Ignore on read	RO
m.5.6	TC present	1 = TC present in package 0 = TC not present in package	RO
m.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
m.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
m.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
m.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
m.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
m.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]m = address of MMD accessed (see Table 45–1)
[b]RO = Read Only

Table 45–3—PMA/PMD registers

Register address	Register name
1.0	PMA/PMD control 1
1.1	PMA/PMD status 1
1.2, 1.3	PMA/PMD device identifier
1.4	PMA/PMD speed ability
1.5, 1.6	PMA/PMD devices in package
1.7	10G PMA/PMD control 2
1.8	10G PMA/PMD status 2
1.9	10G PMD transmit disable
1.10	10G PMD receive signal detect

Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name
1.11	10G PMA/PMD extended ability register
1.12, 1.13	Reserved
1.14, 1.15	PMA/PMD package identifier
1.16 through 1.29	
1.30	10P/2B PMA/PMD control
1.31	10P/2B PMA/PMD status
1.32	10P/2B link partner PMA/PMD control[a]
1.33	10P/2B link partner PMA/PMD status[a]
1.34, 1.35	Reserved
1.36	10P/2B link loss counter
1.37	10P/2B RX SNR margin
1.38	10P/2B link partner RX SNR margin[a]
1.39	10P/2B line attenuation
1.40	10P/2B link partner line attenuation[a]
1.41	10P/2B line quality thresholds
1.42	2B link partner line quality thresholds[a]
1.43	10P FEC correctable errors counter
1.44	10P FEC uncorrectable errors counter
1.45	10P link partner FEC correctable errors[a]
1.46	10P link partner FEC uncorrectable errors[a]
1.47	10P electrical length
1.48	10P link partner electrical length[a]
1.49	10P PMA/PMD general configuration[a]
1.50	10P PSD configuration[a]
1.51, 1.52	10P downstream data rate configuration[a]
1.53	10P downstream Reed-Solomon configuration[a]
1.54, 1.55	10P upstream data rate[a]
1.56	10P upstream Reed-Solomon configuration[a]
1.57, 1.58	10P tone group
1.59, 1.60, 1.61, 1.62, 1.63	10P tone control parameters[a]
1.64	10P tone control action[a]
1.65, 1.66, 1.67	10P tone status
1.68	10P outgoing indicator bits
1.69	10P incoming indicator bits
1.70	10P cyclic extension configuration
1.71	10P attainable downstream data rate
1.72 through 1.79	Reserved

Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name
1.80	2B general parameter
1.81 through 1.88	2B PMD parameters
1.89	2B code violation errors counter
1.90	2B link partner code violation errors[a]
1.91	2B errored seconds counter
1.92	2B link partner errored seconds[a]
1.93	2B severely errored seconds counter
1.94	2B link partner severely errored seconds[a]
1.95	2B LOSW counter
1.96	2B link partner LOSW[a]
1.97	2B unavailable seconds counter
1.98	2B link partner unavailable seconds[a]
1.99	2B state defects
1.100	2B link partner state defects[a]
1.101	2B negotiated constellation
1.102 through 1.109	2B extended PMD parameters
1.110 through 1.128	Reserved
1.129	10GBASE-T status
1.130	10GBASE-T THP setting
1.132	10GBASE-T TX power level setting
1.133 through 1.32 767	Reserved
1.32 768 through 1.65 535	Vendor specific

[a]Register is defined only for -O port types and is reserved for -R ports

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

The assignment of bits in the PMA/PMD control 1 register is shown in Table 45–4. The default value for each bit of the PMA/PMD control 1 register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.0.14	Reserved	Value always 0, writes ignored	R/W
1.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
1.0.12	Reserved	Value always 0, writes ignored	R/W
1.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.0.10:7	Reserved	Value always 0, writes ignored	R/W
1.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
1.0.1	Reserved	Value always 0, writes ignored	R/W
1.0.0	PMA loopback	1 = Enable PMA Loopback mode 0 = Disable PMA Loopback mode	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.1.1 Reset (1.0.15)

Resetting a PMA/PMD is accomplished by setting bit 1.0.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 1.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.0.15. During a reset, a PMD/PMA shall respond to reads from register bits 1.0.15 and 1.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

45.2.1.1.2 Low power (1.0.11)

A PMA/PMD may be placed into a low-power mode by setting bit 1.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.0.11 is zero.

NOTE—This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

45.2.1.1.3 Speed selection (1.0.13,1.0.6, 1.0.5:2)

Speed selection bits 1.0.13 and 1.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PMA/PMD may be selected using bits 5 through 2. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. A PMA/PMD may ignore writes to the PMA/PMD speed selection bits that select speeds it has not advertised in the PMA/PMD speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD speed selection defaults to a supported ability.

When set to 0001, bits 5:2 select the use of the 10PASS-TS or 2BASE-TL PMA/PMD. More specific mode selection is performed using the 10P/2B PMA control register (45.2.1.11).

45.2.1.1.4 PMA loopback (1.0.0)

The PMA shall be placed in a Loopback mode of operation when bit 1.0.0 is set to a one. When bit 1.0.0 is set to a one, the PMA shall accept data on the transmit path and return it on the receive path.

The loopback function is mandatory for the 10GBASE-X port type and optional for all other port types, except 2BASE-TL and 10PASS-TS, which do not support loopback. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

The default value of bit 1.0.0 is zero.

NOTE—The signal path through the PMA that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PMA circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

The assignment of bits in the PMA/PMD status 1 register is shown in Table 45–5. All the bits in the PMA/PMD status 1 register are read only; therefore, a write to the PMA/PMD status 1 register shall have no effect.

Table 45–5—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1.15:8	Reserved	Ignore when read	RO
1.1.7	Fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.1.6:3	Reserved	Ignore when read	RO
1.1.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
1.1.1	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.1.2.1 Fault (1.1.7)

Fault is a global PMA/PMD variable. When read as a one, bit 1.1.7 indicates that either (or both) the PMA or the PMD has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 1.1.7 indicates that neither the PMA nor the PMD has detected a fault condition. For 10 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one. For 10PASS-TS or 2BASE-TL operations, when read as a one, a fault has been detected and more detailed information is conveyed in 45.2.1.16, 45.2.1.39, 45.2.1.40, and 45.2.1.55.

45.2.1.2.2 Receive link status (1.1.2)

When read as a one, bit 1.1.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

While a 10PASS-TS or 2BASE-TL PMA/PMD is initializing, this bit shall indicate receive link down (see 45.2.1.12).

45.2.1.2.3 Low-power ability (1.1.1)

When read as a one, bit 1.1.1 indicates that the PMA/PMD supports the low-power feature. When read as a zero, bit 1.1.1 indicates that the PMA/PMD does not support the low-power feature. If a PMA/PMD supports the low-power feature, then it is controlled using the low-power bit 1.0.11.

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

The assignment of bits in the PMA/PMD speed ability register is shown in Table 45–6.

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.4.15:3	Reserved for future speeds	Value always 0, writes ignored	RO
1.4.2	10PASS-TS capable	1 = PMA/PMD is capable of operating as 10PASS-TS 0 = PMA/PMD is not capable of operating as 10PASS-TS	RO
1.4.1	2BASE-TL capable	1 = PMA/PMD is capable of operating as 2BASE-TL 0 = PMA/PMD is not capable of operating as 2BASE-TL	RO
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.1.4.1 10PASS-TS capable (1.4.2)

When read as a one, bit 1.4.2 indicates that the PMA/PMD is able to operate as 10PASS-TS. When read as a zero, bit 1.4.2 indicates that the PMA/PMD is not able to operate as 10PASS-TS.

45.2.1.4.2 2BASE-TL capable (1.4.1)

When read as a one, bit 1.4.1 indicates that the PMA/PMD is able to operate as 2BASE-TL. When read as a zero, bit 1.4.1 indicates that the PMA/PMD is not able to operate as 2BASE-TL.

45.2.1.4.3 10G capable (1.4.0)

When read as a one, bit 1.4.0 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 1.4.0 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s.

45.2.1.5 PMA/PMD devices in package (Registers 1.5 and 1.6)

The assignment of bits in the PMA/PMD devices in package registers is shown in Table 45–2a.

When read as a one, a bit in the PMA/PMD devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PMA/PMD devices in package registers. Bit 1.5.0 is used to indicate that Clause 22 functionality

Table 45–7— PMA/PMD devices in package registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
1.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
1.6.13:0	Reserved	Ignore on read	RO
1.5.15:6	Reserved	Ignore on read	RO
1.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
1.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
1.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
1.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
1.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
1.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]RO = Read Only

has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.1.6 10G PMA/PMD control 2 register (Register 1.7)

The assignment of bits in the 10G PMA/PMD control 2 register is shown in Table 45–8.

45.2.1.6.1 PMA/PMD type selection (1.7.2:0)

Change "2" to "3". Insert "2" after status. Change table by renumbering "3" to "4" in row on and "2" to "3" in row 2. Change row 2 column 3 by adding a new most significant bit "3" sub column and by adding text for 10GBASE-T.

The PMA/PMD type of the 10G PMA/PMD shall be selected using bits ~~2~~ 3 through 0. The PMA/PMD type abilities of the 10G PMA/PMD are advertised in bits 9 and 7 through 0 of the 10G PMA/PMD status 2 register and bit 0 of the 10G PMA/PMD extended ability register. A 10G PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised in the status 2 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD type selection defaults to a supported ability.

Table 45–8—10G PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:~~4~~3	Reserved	Value always 0, writes ignored	R/W
1.7.~~2~~3:0	PMA/PMD type selection	3 2 1 0 1 0 0 0 = 10GBASE-T PMA/PMD type 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

[a]R/W = Read/Write

45.2.1.7 10G PMA/PMD status 2 register (Register 1.8)

The assignment of bits in the 10G PMA/PMD status 2 register is shown in Table 45–9. All the bits in the 10G PMA/PMD status 2 register are read only; a write to the 10G PMA/PMD status 2 register shall have no effect.

Table 45–9—10G PMA/PMD status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
1.8.9	Extended abilities	1 = PMA/PMD has extended abilities listed in register 1.11 0 = PMA/PMD does not have extended abilities	RO
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO
1.8.0	PMA loopback ability	1 = PMA has the ability to perform a loopback function 0 = PMA does not have the ability to perform a loopback function	RO

[a]RO = Read Only, LH = Latching High

45.2.1.7.1 Device present (1.8.15:14)

When read as <10>, bits 1.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 1.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.1.7.2 Transmit fault ability (1.8.13)

When read as a one, bit 1.8.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.8.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.7.3 Receive fault ability (1.8.12)

When read as a one, bit 1.8.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.8.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.7.4 Transmit fault (1.8.11)

Insert reference to clause 55 for defination of transmit fault.

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for serial PMDs is given in 52.4.8. The description of the transmit fault function for WWDM PMDs is given in 53.4.10. The description of the transmit fault function for the 10GBASE-CX4 PMD is given in 54.5.10. The description of the transmit fault function for 10GBASE-T PMA is given in TBD (55.x.x). The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

45.2.1.7.5 Receive fault (1.8.10)

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for serial PMDs is given in 52.4.9. The description of the receive fault function for WWDM PMDs is given in 53.4.11. The description of the receive fault function for the 10GBASE-CX4 PMD is given in 54.5.11. The description of the receive fault function for 10GBASE-T PMA is given in TBD (55.x.x). The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.10 is zero.

45.2.1.7.6 PMA/PMD extended abilities (1.8.9)

When read as a one, bit 1.8.9 indicates that the PMA/PMD has extended abilities listed in register 1.11. When read as a zero, bit 1.8.9 indicates that the PMA/PMD does not have extended abilities.

45.2.1.7.7 PMD transmit disable ability (1.8.8)

When read as a one, bit 1.8.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.8.8 indicates that the PMD is not able to perform the transmit disable function. If a PMD is able to perform the transmit disable function, then it is controlled using the PMD transmit disable register.

45.2.1.7.8 10GBASE-SR ability (1.8.7)

When read as a one, bit 1.8.7 indicates that the PMA/PMD is able to support a 10GBASE-SR PMA/PMD type. When read as a zero, bit 1.8.7 indicates that the PMA/PMD is not able to support a 10GBASE-SR PMA/PMD type.

45.2.1.7.9 10GBASE-LR ability (1.8.6)

When read as a one, bit 1.8.6 indicates that the PMA/PMD is able to support a 10GBASE-LR PMA/PMD type. When read as a zero, bit 1.8.6 indicates that the PMA/PMD is not able to support a 10GBASE-LR PMA/PMD type.

45.2.1.7.10 10GBASE-ER ability (1.8.5)

When read as a one, bit 1.8.5 indicates that the PMA/PMD is able to support a 10GBASE-ER PMA/PMD type. When read as a zero, bit 1.8.5 indicates that the PMA/PMD is not able to support a 10GBASE-ER PMA/PMD type.

45.2.1.7.11 10GBASE-LX4 ability (1.8.4)

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-LX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-LX4 PMA/PMD type.

45.2.1.7.12 10GBASE-SW ability (1.8.3)

When read as a one, bit 1.8.3 indicates that the PMA/PMD is able to support a 10GBASE-SW PMA/PMD type. When read as a zero, bit 1.8.3 indicates that the PMA/PMD is not able to support a 10GBASE-SW PMA/PMD type.

45.2.1.7.13 10GBASE-LW ability (1.8.2)

When read as a one, bit 1.8.2 indicates that the PMA/PMD is able to support a 10GBASE-LW PMA/PMD type. When read as a zero, bit 1.8.2 indicates that the PMA/PMD is not able to support a 10GBASE-LW PMA/PMD type.

45.2.1.7.14 10GBASE-EW ability (1.8.1)

When read as a one, bit 1.8.1 indicates that the PMA/PMD is able to support a 10GBASE-EW PMA/PMD type. When read as a zero, bit 1.8.1 indicates that the PMA/PMD is not able to support a 10GBASE-EW PMA/PMD type.

45.2.1.7.15 PMA loopback ability (1.8.0)

When read as a one, bit 1.8.0 indicates that the PMA is able to perform the loopback function. When read as a zero, bit 1.8.0 indicates that the PMA is not able to perform the loopback function. If a PMA is able to perform the loopback function, then it is controlled using the PMA loopback bit 1.0.0.

45.2.1.8 10G PMD transmit disable register (Register 1.9)

Change transmit disable function description by deleting "four lane electrical" to be more specific "10GBASE-CX4".

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–10. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for serial PMDs is described in 52.4.7. The transmit disable function for wide wavelength division multiplexing (WWDM) PMDs is described in 53.4.7. The transmit disable function for 10GBASE-CX4 ~~four-lane electrical~~ PMDs is described in 54.5.6.

Table 45–10—10G PMD transmit disable register bit definitions

Bit(s)	Name	Description	R/W[a]
1.9.15:5	Reserved	Value always 0, writes ignored	R/W
1.9.4	PMD transmit disable 3	1 = Disable output on transmit lane 3 0 = Enable output on transmit lane 3	R/W
1.9.3	PMD transmit disable 2	1 = Disable output on transmit lane 2 0 = Enable output on transmit lane 2	R/W
1.9.2	PMD transmit disable 1	1 = Disable output on transmit lane 1 0 = Enable output on transmit lane 1	R/W
1.9.1	PMD transmit disable 0	1 = Disable output on transmit lane 0 0 = Enable output on transmit lane 0	R/W
1.9.0	Global PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[a]R/W = Read/Write

Editors Comment: What do we want to do with transmit disable? Currently not defined in section 55.

45.2.1.8.1 PMD transmit disable 3 (1.9.4)

When bit 1.9.4 is set to a one, the PMD shall disable output on lane 3 of the transmit path. When bit 1.9.4 is set to a zero, the PMD shall enable output on lane 3 of the transmit path.

The default value for bit 1.9.4 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.2 PMD transmit disable 2 (1.9.3)

When bit 1.9.3 is set to a one, the PMD shall disable output on lane 2 of the transmit path. When bit 1.9.3 is set to a zero, the PMD shall enable output on lane 2 of the transmit path.

The default value for bit 1.9.3 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.3 PMD transmit disable 1 (1.9.2)

When bit 1.9.2 is set to a one, the PMD shall disable output on lane 1 of the transmit path. When bit 1.9.2 is set to a zero, the PMD shall enable output on lane 1 of the transmit path.

The default value for bit 1.9.2 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.4 PMD transmit disable 0 (1.9.1)

When bit 1.9.1 is set to a one, the PMD shall disable output on lane 0 of the transmit path. When bit 1.9.1 is set to a zero, the PMD shall enable output on lane 0 of the transmit path.

The default value for bit 1.9.1 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.5 Global PMD transmit disable (1.9.0)

When bit 1.9.0 is set to a one, the PMD shall disable output on the transmit path. When bit 1.9.0 is set to a zero, the PMD shall enable output on the transmit path.

For single wavelength PMD types, transmission will be disabled when this bit is set to one. When this bit is set to zero, transmission is enabled.

For multiple wavelength or lane PMD types, transmission will be disabled on all lanes when this bit is set to one. When this bit is set to zero, the lanes are individually controlled by their corresponding transmit disable bits 1.9.4:1.

The default value for bit 1.9.0 is zero.

45.2.1.9 10G PMD receive signal detect register (Register 1.10)

The assignment of bits in the 10G PMD receive signal detect register is shown in Table 45–11. The 10G PMD receive signal detect register is mandatory. PMD types that use only a single wavelength indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bits 1.10.4:1. PMD types that use multiple wavelengths or lanes indicate the status of each lane in bits 1.10.4:1 and the logical AND of those bits in bit 1.10.0.

Table 45–11—10G PMD receive signal detect register bit definitions

Bit(s)	Name	Description	R/W[a]
1.10.15:5	Reserved	Value always 0, writes ignored	RO
1.10.4	PMD receive signal detect 3	1 = Signal detected on receive lane 3 0 = Signal not detected on receive lane 3	RO
1.10.3	PMD receive signal detect 2	1 = Signal detected on receive lane 2 0 = Signal not detected on receive lane 2	RO
1.10.2	PMD receive signal detect 1	1 = Signal detected on receive lane 1 0 = Signal not detected on receive lane 1	RO
1.10.1	PMD receive signal detect 0	1 = Signal detected on receive lane 0 0 = Signal not detected on receive lane 0	RO
1.10.0	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO

[a]RO = Read Only

45.2.1.9.1 PMD receive signal detect 3 (1.10.4)

When bit 1.10.4 is read as a one, a signal has been detected on lane 3 of the PMD receive path. When bit 1.10.4 is read as a zero, a signal has not been detected on lane 3 of the PMD receive path.

45.2.1.9.2 PMD receive signal detect 2 (1.10.3)

When bit 1.10.3 is read as a one, a signal has been detected on lane 2 of the PMD receive path. When bit 1.10.3 is read as a zero, a signal has not been detected on lane 2 of the PMD receive path.

45.2.1.9.3 PMD receive signal detect 1 (1.10.2)

When bit 1.10.2 is read as a one, a signal has been detected on lane 1 of the PMD receive path. When bit 1.10.2 is read as a zero, a signal has not been detected on lane 1 of the PMD receive path.

45.2.1.9.4 PMD receive signal detect 0 (1.10.1)

When bit 1.10.1 is read as a one, a signal has been detected on lane 0 of the PMD receive path. When bit 1.10.1 is read as a zero, a signal has not been detected on lane 0 of the PMD receive path.

45.2.1.9.5 Global PMD receive signal detect (1.10.0)

When bit 1.10.0 is read as a one, a signal has been detected on all the PMD receive paths. When bit 1.10.0 is read as a zero, a signal has not been detected on at least one of the PMD receive paths.

Single wavelength PMD types indicate the status of their receive path signal using this bit.

Multiple wavelength or multiple lane PMD types indicate the global status of the lane-by-lane signal detect indications using this bit. This bit is read as a one when all the lane signal detect indications are one; otherwise, this bit is read as a zero.

45.2.1.10 10G PMA/PMD extended ability register (Register 1.11)

Change table by renumbering column 1 row 2 from "1" to "2" and inserting row 3 with associated text.

The assignment of bits in the 10G PMA/PMD extended ability register is shown in Table 45–12. All of the bits in the 10G PMA/PMD extended ability register are read only; a write to the 10G PMA/PMD extended ability register shall have no effect.

Table 45–12—10G PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15:2~~1~~	Reserved	Ignore on read	RO
1.11.1	10GBASE-T ability	1 = PMA/PMD is able to perform 10GBASE-T 0 = PMA/PMD is not able to perform 10GBASE-T	RO
1.11.0	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

[a]RO = Read Only

Insert paragraphs 45.2.1.10.1 and 45.2.1.10.2

45.2.1.10.1 10GBASE-T ability (1.11.1)

When read as a one, bit 1.11.1 indicates that the PMA/PMD is able to support a 10GBASE-T PMA/PMD type. When read as a zero, bit 1.11.1 indicates that the PMA/PMD is not able to support a 10GBASE-T PMA/PMD type.

Editors note: section 45.2.1.10.2 was omitted in the origianal draft and while not directly part of the 802.3an working group was added for completeness and consistancy in style.

45.2.1.10.2 10GBASE-CX4 ability (1.11.0)

When read as a one, bit 1.11.0 indicates that the PMA/PMD is able to support a 10GBASE-CX4 PMA/PMD type. When read as a zero, bit 1.11.0 indicates that the PMA/PMD is not able to support a 10GBASE-CX4 PMA/PMD type.

45.2.1.11 PMA/PMD package identifier (Registers 1.14 and 1.15)

Registers 1.14 and 1.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PMA/PMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.1.12 10P/2B PMA/PMD control register (Register 1.30)

The assignment of bits in the 10P/2B PMA control register is shown in Table 45–13.

Table 45–13—10P/2B PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.30.15	PMA/PMD link control	1 = begin initialization, enable link (-R default) 0 = force link down (-O default)	R/W
1.30.14	STFU	Silence the far unit 1 = send silence command 0 = silence command inactive (default)	R/W
1.30.13:8	Silence time	Silence time = 10 × (value of bits + 1) seconds	R/W
1.30.7	Port sub-type select	1 = port operates as an -O sub-type 0 = port operates as a -R sub-type	R/W
1.30.6	Handshake cleardown	1 = send cleardown command 0 = idle (default)	R/W,SC
1.30.5	Ignore incoming hand-shake	1 = PMA/PMD does not respond to handshake tones 0 = PMA/PMD responds to handshake tones	R/W
1.30.4:0	PMA/PMD type selection	3:4 2 1 0 0 0 0 0 = 10PASS-TS PMA/PMD type 0 0 0 1 = 2BASE-TL PMA/PMD type 0 0 1 0 = 2BASE-TL or 10PASS-TS (-R only) 0 0 1 1 = 2BASE-TL preferred, or 10PASS-TS (-O only) 0 1 0 0 = 10PASS-TS preferred, or 2BASE-TL (-O only) all other values are reserved	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.12.1 PMA/PMD link control (1.30.15)

The STA may enable the PMA/PMD link and initiate link initialization by writing this bit to a one. While link is initializing or up, this bit shall remain a one and writing a one to this bit shall be ignored. The STA may force the link down by writing a zero to this bit. While this bit is set to zero, the PHY shall not send G.994.1 handshake tones. For -O sub-types, upon link drop or MMD reset, the PMA/PMD shall set these bits to zero. For -R sub-types, upon link drop or MMD reset, the PMA/PMD shall set these bits to one.

45.2.1.12.2 STFU (1.30.14)

When this bit is set to a one, the PMA/PMD sends a message to the link partner instructing it to be silent for the silence time (see 45.2.1.12.3). Writing to this bit is valid only when the PMA/PMD link status bits in the PMA/PMD status register (see 45.2.1.13.4) are set to “link is down (ready)”. Writes are otherwise ignored.

This bit clears to zero when the silence command is sent, or upon the execution of an MMD reset.

45.2.1.12.3 Silence time (1.30.13:8)

The value of these bits sets the silence time conveyed in a STFU operation (see 45.2.1.12.2). The silence time is encoded according to the following formula, where x is the decimal value of the bits:

$$\text{time} = 10 \times (x + 1) \text{ seconds}$$

45.2.1.12.4 Port sub-type select (1.30.7)

This register bit selects the port sub-type for PMA/PMD operation. The bit defaults to a supported mode. The PHY shall ignore writes that select an unsupported mode (see 45.2.1.12).

Changing this bit alters the fundamental operation of the PMA/PMD, therefore, writes to change this bit shall be ignored if the link is up or initializing (see 45.2.1.13.4).

45.2.1.12.5 Handshake cleardown (1.30.6)

Setting this bit to a one shall cause the PMA/PMD to issue a G.994.1 cleardown command to the link partner (see 61.4.3). The PMA/PMD shall clear this bit to zero after the cleardown command has been sent or upon MMD reset. If the PMA/PMD link is not in the “link down (ready)” state (see 45.2.1.13.4), writes to this register shall be ignored.

45.2.1.12.6 Ignore incoming handshake (1.30.5)

When set to a one, the PMA/PMD shall not respond to received handshake tones (see 61.4.3). When set to a zero, the PMA/PMD shall respond to received handshake tones normally, according to 61.4.3 and G.994.1. Upon MMD reset, this bit shall be cleared to zero.

45.2.1.12.7 PMA/PMD type selection (1.30.4:0)

The PMA/PMD type of a 10P/2B PHY may be selected using bits 4 through 0. A PHY shall ignore writes to the type selection bits that select PMA/PMD types it has not advertised in the speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable port types are applied consistently across all the MMDs on a particular PHY.

A value of 0010 may be set in -R sub-type PMA/PMDs that have both 2BASE-TL and 10PASS-TS capability set in the PMA/PMD speed ability register. The PMA/PMD type of the -R is set upon link initialization by the -O.

Values of 0011 and 0100 may be set in -O sub-type PMA/PMDs that have both 2BASE-TL and 10PASS-TS capabilities set in the PMA/PMD speed ability register. These values indicate whether the -R is set to 10PASS-TS or 2BASE-TL respectively. If the -R is not capable of the “preferred” mode, the -R is set to 10PASS-TS or 2BASE-TL respectively.

The selection is advertised during link initialization G.994 handshake.

The PMA/PMD type selection defaults to a supported ability.

45.2.1.13 10P/2B PMA/PMD status register (Register 1.31)

The assignment of bits in the 10P/2B PMA/PMD status register is shown in Table 45–14.

Table 45–14—10P/2B PMA/PMD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.31.15:5	Data rate	Current operating bit rate of the PMD n = the value of the bits Data rate = 64n kb/s	RO
1.31.4	CO supported	1 = -O sub-type operation supported 0 = -O sub-type operation not supported	RO
1.31.3	CPE supported	1 = -R sub-type operation supported 0 = -R sub-type operation not supported	RO
1.31.2:0	PMA/PMD link status	2 1 0 0 0 0 = link is Down (not ready) 1 0 0 = link is Down (ready) 0 0 1 = link is Initializing 0 1 0 = link is Up, 10PASS-TS 0 1 1 = link is Up, 2BASE-TL all other values reserved	RO

[a]RO = Read Only

45.2.1.13.1 Data rate (1.31.15:5)

These bits indicate the current bit rate of an operational PMA/PMD link. These bits shall be set to all zeros when the link is down or initializing.

45.2.1.13.2 CO supported (1.31.4)

This bit indicates that the PMA/PMD supports operation as a -O sub-type. This bit is set to a one when the capability is supported and zero otherwise. This bit reflects the signal PMA_PMD_type in 61.3.2.1.

45.2.1.13.3 CPE supported (1.31.3)

This bit indicates that the PMA/PMD supports operation as a -R sub-type. This bit is set to a one when the capability is supported and zero otherwise. This bit reflects the signal PMA_PMD_type in 61.3.2.1.

45.2.1.13.4 PMA/PMD link status (1.31.2:0)

The overall state of the PMA/PMD link is reflected in bits 2:0. After the PMA/PMD is linked to the remote PHY, the PHY shall set these bits to indicate the PMA/PMD port type that is linked (010 for 10PASS-TS and 011 for 2BASE-TL). The corresponding signal, PMA_received_synchronized, is defined in 61.3.2.1.

While the link is initializing, these bits shall be set to 001.

When read as 000, these bits shall indicate that PMA/PMD link is down and the PMA/PMD is not detecting handshake tones from a link partner. This state is known as “not ready”.

When read as 100, these bits shall indicate that the PMA/PMD link is down and the PMA/PMD is detecting handshake tones from a link partner. This state is known as “ready”.

45.2.1.14 Link Partner PMA/PMD control register (Register 1.32)

The 10PASS-TS-O and 2BASE-TL-O PMA/PMDs allow access to certain register values of their link partner via the local MDIO interface. A summary of link partner parameters that may be sent or retrieved is provided in Table 45–15.

Table 45–15—Link partner PMA/PMD registers and PMA/PMD register duals

	Register type	Link partner register	Local register counterpart	
	PHY sub-type	-O	-O	-R
Link partner register name		**Address and access type[a]**		
10P/2B link partner RX SNR margin		1.38 RO	1.37 RO	1.37 RO
10P/2B link partner line attenuation		1.40 RO	1.39 RO	1.39 RO
10P/2B link partner line quality thresholds		1.42 R/W	1.41 R/W	n/a
10P link partner FEC correctable errors		1.45 RO	1.43 RO	1.43 RO
10P link partner FEC uncorrectable errors		1.46 RO	1.44 RO	1.44 RO
10P link partner electrical length		1.48 RO	1.47 RO	1.47 RO
2B link partner code violation errors		1.90 RO	1.89 RO	1.89 RO
2B link partner errored seconds		1.92 RO	1.91 RO	1.91 RO
2B link partner severely errored seconds		1.94 RO	1.93 RO	1.93 RO
2B link partner LOSW		1.96 RO	1.95 RO	1.95 RO
2B link partner unavailable seconds		1.98 RO	1.97 RO	1.97 RO
2B link partner state defects register		1.100 RO	1.99 RO	1.99 RO

[a]R/W = Read/Write, RO = read only, n/a = undefined

The Link partner PMA/PMD control register allows the -O STA to control the transmission and retrieval of parameters from its -R link partner.

The -R STA may read values exchanged by the -O STA in the local register counterpart to the link partner register. For example, the -O 10P link partner electrical length register will be populated with the contents of the -R 10P electrical length register upon a successful “Get link partner parameters” command. Similarly, the -R 10P/2B line quality thresholds register will contain the values sent by the -O in the 10P/2B link partner line quality thresholds register, after a successful “Send link partner parameters” command.

The link partner registers listed in Table 45–15 have the same behaviour upon being read or reset as their local register counterparts.

This register is defined for -O port sub-types only.

Bit definitions for the Link partner PMA/PMD control register are found in Table 45–16.

Table 45–16—Link partner PMA/PMD control register bit definitions

Bits(s)	Name	Description	R/W[a]
1.32.15	Get link partner parameters	1 = get link partner parameters 0 = operation complete, ready	R/W, SC
1.32.14	Reserved	Value always 0, writes ignored	R/W
1.32.13	Send link partner parameters	1 = send link partner parameters 0 = operation complete, ready	R/W, SC
1.32.12:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.14.1 Get link partner parameters (1.32.15)

When this bit is set to a one, the -O PHY updates its link partner registers shown in Table 45–15 with values from the link partner. While the operation is in progress, the PHY shall keep the bit set as one. If the "Get link partner parameters" operation does not complete within 10 seconds, its result shall be marked as "failed" (see 45.2.1.14) and the operation marked as "complete". After completion of the operation or upon reset, the PHY shall reset the bit to zero. A write to this bit when link is down shall cause the result to be marked as "failed" and the operation marked as "complete".

45.2.1.14.2 Send link partner parameters (1.32.13)

When this bit is set to a one, the -O PHY sends the contents of the 2B link partner line quality thresholds register (see 45.2.1.21) to the link partner. While the operation is in progress, the PHY shall keep the bit set as one. The "Send Link partner parameters" operation must complete within 10 seconds, or its result shall be marked as "failed" (see 45.2.1.14) and the operation marked as "complete". After completion of the operation or upon reset, the PHY shall reset the bit to zero. A write to this bit when link is down shall cause the result to be marked as "failed" and the operation marked as "complete".

45.2.1.15 Link partner PMA/PMD status register (Register 1.33)

The Link partner PMA/PMD status register reflects the result of the operations that are performed using the Link Partner PMA/PMD control register (1.32).

This register is defined for -O port sub-types only.

Bit definitions for the Link partner PMA/PMD status register are found in Table 45–17.

Table 45–17—Link Partner PMA/PMD status register bit definitions

Bits(s)	Name	Description	R/W[a]
1.33.15	Reserved	Value always 0, writes ignored	RO
1.33.14	Get link partner result	1 = operation failed 0 = operation successful	RO, LH
1.33.13	Reserved	Value always 0, writes ignored	RO
1.33.12	Send link partner result	1 = operation failed 0 = operation successful	RO, LH
1.33.11:0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read Only, LH = Latches High

45.2.1.15.1 Get link partner result (1.33.14)

After a "Get link partner parameters" operation terminates, this bit reflects the result of the operation. If the operation did not complete successfully, the PHY shall set this bit to a one. Upon being read or a reset, the PHY shall set the bit to zero.

The definition of an unsuccessful "Get link partner parameters" operation is unspecified and left to the implementation.

45.2.1.15.2 Send link partner result (1.33.12)

After a "Send link partner parameters" operation terminates, this bit reflects the result of the operation. If the operation did not complete successfully, the PHY shall set this bit to a one. Upon being read or a reset, the PHY resets the bit to zero.

The definition of an unsuccessful "Send link partner parameters" operation is unspecified and left to the implementation.

45.2.1.16 10P/2B PMA/PMD link loss register (Register 1.36)

The 10P/2B PMA/PMD link loss register is a 16 bit counter that contains the number of times the PMA/PMD link is lost. Link is considered lost when the PMA_receive_synchronized signal (see 61.3.2.1) transitions from up to down. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PMA/PMD link loss register is shown in Table 45–18.

Table 45–18—10P/2B PMA/PMD link loss register bit definitions

Bits(s)	Name	Description	R/W[a]
1.36.15:0	Link lost events	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.1.17 10P/2B RX SNR margin register (Register 1.37)

For further information on 2BASE-TL SNR margin, see 63.3. For 10PASS-TS SNR margin, see 62.3.

The bit definitions for the 10P/2B RX SNR margin register are found in Table 45–19.

Table 45–19—10P/2B RX SNR margin register bit definition

Bit(s)	Name	Description	R/W[a]
1.37.15:8	Reserved	Value always 0, writes ignored	R/W
1.37.7:0	RX SNR margin	Value of SNR margin in dB	RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.18 10P/2B link partner RX SNR margin register (Register 1.38)

The 10P/2B link partner RX SNR margin register provides access to the link partner's receive SNR margin. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–19.

45.2.1.19 10P/2B line attenuation register (Register 1.39)

This register reports the line attenuation as measured by the PMA/PMD. For more information, see the reference documents in 63.3 and 62.3.

The bit definitions for the 10P/2B line attenuation register are found in Table 45–20.

Table 45–20—10P/2B line attenuation register bit definitions

Bits(s)	Name	Description	R/W[a]
1.39.15:0	Line attenuation	The value of the line attenuation in dB, as perceived by the local PMD.	RO

[a]RO = Read Only

45.2.1.20 10P/2B link partner line attenuation register (Register 1.40)

The 10P/2B link partner line attenuation register provides access to the link partner's perceived line attenuation margin. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–20.

45.2.1.21 10P/2B line quality thresholds register (Register 1.41)

The 10P/2B line quality thresholds register sets the target environment for the 10PASS-TS/2BASE-TL connection. The line quality is defined by the SNR margin and line attenuation values.

Bit definitions for the 10P/2B line quality threshold register are found in Table 45–21.

Table 45–21— 10P/2B line quality thresholds register bit definition

Bit(s)	Name	Description	R/W[a]
1.41.15:8	Loop attenuation threshold	Attenuation threshold in dB	O: R/W R: RO
1.41.7:4	SNR margin threshold	SNR margin threshold in dB	O: R/W R: RO
1.41.3:0	Reserved	Value always 0, writes ignored	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.21.1 Loop attenuation threshold (1.41.15:8)

These bits set the loop attenuation threshold for 2BASE-TL PMA/PMDs. Writing to these bits on a 10PASS-TS PMA/PMD have no effect. The threshold value is in units of dB. For more information on the loop attenuation threshold, see 63.2.2.3.

45.2.1.21.2 SNR margin threshold (1.41.7:4)

These bits set the SNR margin threshold for 10PASS-TS and 2BASE-TL PMA/PMDs. The threshold is expressed in units of dB. For more information of the SNR margin threshold, see 63.2.2.3 for 2BASE-TL and Section 10 of the document referenced in 62.1.3 for 10PASS-TS.

45.2.1.22 2B link partner line quality thresholds register (Register 1.42)

The 2B link partner line quality thresholds register allows the -O STA to set its -R link partner's line quality thresholds. The contents of this register are transmitted to the -R when the STA activates the "Send link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.2).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–21.

45.2.1.23 10P FEC correctable errors counter (Register 1.43)

The 10P FEC correctable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and corrected. For more information on 10PASS-TS FEC, see 62.2.4.2. These bits shall be reset to all zeroes upon execution of the MMD reset and upon being read. The assignment of bits in the 10P FEC correctable error counter is shown in Table 45–22.

Table 45–22—10P FEC correctable errors counter register bit definitions

Bits(s)	Name	Description	R/W[a]
1.43.15:0	Correctable codewords [15:0]	The bytes of the counter	RO

[a]RO = Read Only

45.2.1.24 10P FEC uncorrectable errors counter (Register 1.44)

The 10P FEC uncorrectable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and are uncorrectable. For more information on 10PASS-TS FEC, see 62.2.4.2. These bits shall be reset to all zeroes upon execution of the MMD reset and upon being read. The assignment of bits in the 10P FEC uncorrectable error counter is shown in Table 45–23.

Table 45–23—10P FEC uncorrectable errors counter bit definitions

Bits(s)	Name	Description	R/W[a]
1.44.15:0	Uncorrectable codewords [15:0]	The bytes of the counter	RO

[a]RO = Read Only

45.2.1.25 10P link partner FEC correctable errors register (Register 1.45)

The 10P link partner FEC correctable errors register provides the -O STA with a snapshot of the -R link partner's FEC correctable errors counter. Because this register is not a counter, its value will increment only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–22 and 45.2.1.23.

45.2.1.26 10P link partner FEC uncorrectable errors register (Register 1.46)

The 10P link partner FEC uncorrectable errors register provides the -O STA a snapshot of the -R link partner's FEC uncorrectable errors counter. Because this register is not a counter, its value will increment only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–23 and 45.2.1.24.

45.2.1.27 10P electrical length register (Register 1.47)

The bit definitions for the 10P electrical length register are found in Table 45–24.

Table 45–24—10P electrical length register bit definitions

Bits(s)	Name	Description	R/W[a]
1.47.15:0	Electrical length	The electrical length of the medium (in meters), as perceived at the local PMD	RO

[a]RO = Read Only

45.2.1.27.1 Electrical length (1.47.15:0)

After the link is established, these bits contain the measured electrical length (in meters) of the medium as measured by the PMD. If the link is down or the PMD is unable to determine the electrical length, these bits shall be set to all ones (see 62.3.2).

45.2.1.28 10P link partner electrical length register (Register 1.48)

The 10P link partner electrical length register provides access to the link partner's electrical length measurement. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–24 and 45.2.1.27.1.

45.2.1.29 10P PMA/PMD general configuration register (Register 1.49)

The 10P PMA/PMD general configuration register is defined for -O port types only.

The 10P PMA/PMD general configuration register bit definitions are found in Table 45–25.

Table 45–25—10P PMA/PMD general configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.49.15:8	Reserved	Value always 0, writes ignored	R/W
1.49.7:0	TX window length	Transmit window length	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.29.1 TX window length (1.49.7:0)

Bits 7:0 control the PMD transmit window length within the cyclic prefix and suffix in units of number of samples, as defined in 62.3.2.

45.2.1.30 10P PSD configuration register (Register 1.50)

This register is defined for -O port sub-types only.

The 10P PSD configuration register bit definitions may be found in Table 45–26.

Table 45–26—10P PSD configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.50.15:9	Reserved	Value always 0, writes ignored	R/W
1.50.8	PBO disable	1 = PBO disabled 0 = PBO normal operation	O: R/W R: undefined
1.50.7:0	Reserved	Value always 0, writes ignored	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.30.1 PBO disable (1.50.8)

Setting this bit to a one disables UPBO for performance testing purposes. Refer to 62.3.4.4.

45.2.1.31 10P downstream data rate configuration (Registers 1.51, 1.52)

These registers are defined for -O port sub-types only.

The bit definitions for the 10P downstream data rate configuration registers are found in Table 45–27.

Table 45–27—10P downstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.51.15:0	Minimum downstream data rate	Sets the minimum required downstream payload data rate M = value of bits Data rate = M × 64000 b/s	O: R/W R: undefined
1.52.15:0	Maximum downstream data rate	Sets the maximum downstream payload data rate M = value of bits Data rate = M × 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.32 10P downstream Reed-Solomon configuration (Register 1.53)

This register is defined for -O port sub-types only.

The bit definitions for 10P downstream Reed-Solomon configuration are found in Table 45–28.

Table 45–28—10P downstream Reed-Solomon configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.53.15:1	Reserved	Value always 0, writes ignored	O: R/W R: undefined
1.53.0	RS codeword length	1 = codeword length of 144 0 = codeword length of 240	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.32.1 RS codeword length (1.53.0)

This bit selects the Reed-Solomon forward error correction codeword length used in the downstream direction. For more information, see 62.2.4.2.

45.2.1.33 10P upstream data rate configuration (Registers 1.54, 1.55)

These registers are defined for -O port sub-types only.

The bit definitions for 10P upstream data rate configuration are found in Table 45–29.

45.2.1.34 10P upstream 10P upstream Reed-Solomon configuration register (Register 1.56)

This register is defined for -O port sub-types only.

The bit definitions for the 10P upstream Reed-Solomon configuration are found in Table 45–30.

Table 45–29—10P upstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.54.15:0	Minimum upstream data rate	Sets the required upstream payload data rate M = value of bits Data rate = M × 64000 b/s	O: R/W R: undefined
1.55.15:0	Maximum upstream data rate	Sets the maximum upstream payload data rate M = value of bits Data rate = M × 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

Table 45–30—10P upstream Reed-Solomon configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.56.15:1	Reserved	Value always 0, writes ignored	O: R/W R: undefined
1.56.0	RS codeword length	1 = codeword length = 144 0 = codeword length = 240	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.34.1 RS codeword length (1.56.0)

This bit selects the Reed-Solomon forward error correction codeword length used in the upstream direction. For more information, see 62.2.4.2.

45.2.1.35 10P tone group registers (Registers 1.57, 1.58)

10PASS-TS operates by modulating 4096 individual tones across the transmission spectrum. Each tone can be assigned a PSD level, desired SNR margin and transmission direction (downstream or upstream). To reduce the complexity of addressing individual tones, tones are addressed by group. The STA sets the lower and upper tones in a group, sets the parameters for that group, and issues a command to activate those parameters for that group. See 62.3.4.7 for details on the mechanism that transfers tone information across the link to and from the -R link partner.

This register allows the STA to specify the range of tones to control. The bit definitions for the 10P tone group register are defined in Table 45–31.

Table 45–31—10P tone group register bit definitions

Bit(s)	Name	Description	R/W[a]
1.57.15:0	Lower tone	The number of the lower frequency tone in the group. Valid when ≤ the Upper tone.	R/W
1.58.15:0	Upper tone	The number of the higher frequency tone in the group. Valid when ≥ the Lower tone.	R/W

[a]R/W = Read/Write

45.2.1.36 10P tone control parameters (Registers 1.59, 1.60, 1.61, 1.62, 1.63)

These registers allow the STA to specify parameters for the tones selected in the 10P tone group registers. These values do not take effect until the corresponding activation commands are issued in the 10P tone control action register. The bit definitions for the 10P tone control parameters are shown in Table 45–32.

These registers are defined for -O port sub-types only.

Table 45–32—10P tone control parameters register bit definitions

Bit(s)	Name	Description	R/W[a]
1.59.15	Tone active	1 = selected tones are active 0 = selected tones are disabled	R/W
1.59.14	Tone direction	1 = selected tones assigned to upstream communication 0 = selected tones assigned to downstream communication	R/W
1.59.13:5	Max SNR margin	Assigns the maximum SNR margin the PMD may achieve M = value of bits Max SNR Margin = M/4 dB	R/W
1.59.4:0	Reserved	Value always 0, writes ignored	R/W
1.60:15:9	Reserved	Value always 0, writes ignored	R/W
1.60.8:0	Target SNR margin	Assigns the target SNR margin for the selected tones M = value of bits Target SNR Margin = M/4 dB	R/W
1.61:15:9	Reserved	Value always 0, writes ignored	R/W
1.61.8:0	Min SNR margin	Assigns the minimum SNR margin for the selected tones M = value of bits Min SNR Margin = M/4 dB	R/W
1.62.15:9	Reserved	Value always 0, writes ignored	R/W
1.62.8:0	PSD level	Assigns a TX PSD level for the selected tones in dBm/Hz P = value of bits (2's complement) PSD Level = P/4 - 100 dBm/Hz	R/W
1.63.15:9	Reserved	Value always 0, writes ignored	R/W
1.63.8:0	USPBO reference	Assigns the level of the USPBO reference at the points represented by the selected tones P = value of bits (2's complement) PSD Level = P/4 - 100 dBm/Hz	R/W

[a]R/W = Read/Write

45.2.1.36.1 Tone active (1.59.15)

These bits are used to control the activity of the selected tones. When the "Change tone activity" command is issued (1.64.4), the selected tones will be either activated or deactivated based on the value set in these bits.

45.2.1.36.2 Tone direction (1.59.14)

These bits are used to control the direction of the selected tones. When the "Change tone direction" command is issued (1.64.3), the selected tones will adopt the direction set in these bits.

45.2.1.36.3 Max SNR Margin (1.59.13:5)

These bits control the maximum SNR margin for the selected tones. When the "Change SNR margin" command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to maximum SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.36.4 Target SNR margin (1.60.8:0)

These bits control the target SNR margin for the selected tones. When the "Change SNR margin" command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to target SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.36.5 Minimum SNR margin (1.61.8:0)

These bits control the minimum SNR margin for the selected tones. When the "Change SNR margin" command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to minimum SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.36.6 PSD level (1.62.8:0)

These bits control the transmit PSD level of the selected tones. When the "Change PSD level" command is issued (1.64.1), the PMA/PMD will set the PSD level of the selected tones to according to this formula, where x is the value of bits 8:0:

$$power = \frac{x}{4} - 100\frac{dBm}{Hz} \quad (45–1)$$

45.2.1.36.7 USPBO reference (1.63.8:0)

These bits control the reference level for the upstream power back-off function of the PMA/PMD. When the "Change USPBO reference PSD" command (1.64.0) is issued, the portion of the USPBO reference curve that corresponds to the selected tones is changed to the value specified by these bits. The USPBO reference level is specified according to this formula, where x is the value of bits 8:0:

$$power = \frac{x}{4} - 100\frac{dBm}{Hz} \quad (45–2)$$

45.2.1.37 10P tone control action register (Register 1.64)

The operations in this register apply to the tones selected in the 10P tone group registers (1.57, 1.58).

This register is defined for -O port sub-types only.

The bit definitions for the 10P tone control action register are shown in Table 45–33T

Table 45–33—10P tone control action register bit definitions

Bit(s)	Name	Description	R/W[a]
1.64.15:6	Reserved	Value always 0, writes ignored	R/W
1.64.5	Refresh tone status	1 = refresh selected tones for the 10P tone status registers 0 = ready, operation complete	R/W, SC
1.64.4	Change tone activity	1 = activate tone active setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.3	Change tone direction	1 = activate tone direction setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.2	Change SNR margin	1 = activate min, max and target SNR margin settings as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.1	Change PSD level	1 = activate PSD level setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.0	Change UPBO reference PSD	1 = activate UPBO reference PSD settings as in tone control parameter register 0 = ready, operation complete	R/W, SC

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.37.1 Refresh tone status (1.64.5)

When this bit is set to a one, the tone status information from the local and link partner is gathered so that it may be read using the 10P tone status registers (1.65, 1.66 and 1.67). While the tones are being refreshed, this bit shall remain set as one. This bit shall be reset to zero when the refresh operation is over or upon reset.

NOTE—Refreshing a large number of tones may take a long time to complete.

45.2.1.37.2 Change tone activity (1.64.4)

When this bit is set to a one, the selected tones are enabled or disabled according to the assignment in the tone active bit of the 10P tone control parameters register (1.59.15). While the tones are being activated/deactivated, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.3 Change tone direction (1.64.3)

When this bit is set to a one, the transmission direction of selected tones is changed according to the assignment in the tone direction bit of the 10P tone control parameters register (1.59.14). While the tones are being assigned, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.4 Change SNR margin (1.64.2)

When this bit is set to a one, the SNR margin parameters for the selected tones are loaded according the assignment in the Minimum, Target and Maximum SNR margin bits of the 10P tone control parameters register (1.59.13:5, 1.60.8:0, 1.61.8:0). While the parameters are being loaded, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.5 Change PSD level (1.64.1)

When this bit is set to a one, the PSD level for the selected tones is set according to the value in the PSD level bits of the 10P tone control parameters register (1.62.8:0). While the PSD is being set, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.37.6 Change USPBO reference PSD (1.64.0)

When this bit is set to a one, the upstream power back-off reference PSD level for the selected tones is set according to the value in the USPBO PSD reference bits of the 10P tone control parameters register (1.63.8:0). While the reference PSD is being set, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.38 10P tone status registers (Registers 1.65, 1.66, 1.67)

The 10P tone status registers allow the STA to query the status of any individual tone in the link. The values read in the 10P tone status register correspond to the tone whose number is set in the "Lower tone" of the 10P tone group registers (see 45.2.1.35).

The status of some tones is read from the link partner. Because the constant update of these values would be a strain on channel resources, these values are only updated for selected tones when the "Refresh tone table" command is issued in the 10P tone control action register (1.64).

The 10P tone status registers bit definitions are given in Table 45–34.

Table 45–34—10P tone status registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.65.15	Refresh status	1 = tone entry has been refreshed 0 = tone entry has not been refreshed since last read	RO
1.65.14	Active	1 = tone is disabled 0 = tone is active	RO
1.65.13	Direction	1 = tone is assigned to upstream communication 0 = tone is assigned to downstream communication	RO
1.65.12:8	Reserved	Value always 0, writes ignored	RO
1.65.7:0	RX PSD	PSD of the tone at the receiver in dBm/Hz	RO
1.66.15:8	TX PSD	PSD of the tone at the transmitter in dBm/Hz	RO
1.66.7:3	Bit load	The number of bits currently loaded on the tone	RO
1.66.2:0	Reserved	Value always 0, writes ignored	RO
1.67.15:10	Reserved	Value always 0, writes ignored	RO
1.67.9:0	SNR margin	Current SNR margin for the tone R = value of bits SNR Margin = R/4 dB	RO

[a]RO = Read Only

45.2.1.38.1 Refresh status (1.65.15)

This bit set to a one indicates that the values for this tone table have not been read since the last "Refresh tone status" command is issued in the 10P tone control action register (1.64). Upon reading this bit or upon reset, the bit shall be reset to zero.

45.2.1.38.2 Active (1.65.14)

When read as a one, this bit indicates that the selected tone is disabled (i.e. powered off and not carrying data).

45.2.1.38.3 Direction (1.65.13)

When read as a one, this bit indicates that the selected tone is assigned to upstream communication. When read as a zero, the tone is assigned to downstream communication.

45.2.1.38.4 RX PSD (1.65.7:0)

These bits report the PSD of the selected tone as perceived at the receiver in units of dBm/Hz.

45.2.1.38.5 TX PSD (1.66.15:8)

These bits report the PSD of the selected tone as output by the transmitter in units of dBm/Hz.

45.2.1.38.6 RX PSD (1.66.7:3)

These bits report the number of bits encoded on the selected tone.

45.2.1.38.7 SNR Margin (1.67.9:0)

These bits report the current SNR margin for the selected tone, as perceived by the receiver, in units of dB. The value of the SNR margin is obtained by dividing the decimal value of bits 9:0 by 4.

45.2.1.39 10P outgoing indicator bits status register (Register 1.68)

The 10P outgoing indicator bits status register conveys the current state of the indicator bits being sent to the link partner. (See 62.3.4.7) The bit definitions for the 10P indicator bits status register are shown in Table 45–35.

Table 45–35—10P outgoing indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.68.15:9	Reserved	Value always 0, writes ignored	RO
1.68.8	LoM	1 = received signal below SNR margin threshold 0 = normal state	RO
1.68.7	lpr	1 = power supply voltage invalid 0 = normal state	RO
1.68.6	po	1 = PMA/PMD is being powered off 0 = normal state	RO
1.68.5	Rdi	1 = severely errored frames have been received 0 = normal state	RO
1.68.4	los	1 = signal power is lower than the threshold 0 = normal state	RO
1.68.3	fec-f	1 = reserved condition 0 = normal state	RO
1.68.2	be-f	1 = reserved condition 0 = normal state	RO
1.68.1	fec-s	1 = corrected errors have been detected in the received FEC block of slow data 0 = normal state	RO
1.68.0	be-s	1 = non-corrected errors have been detected in the received block of slow data 0 = normal state	RO

[a]RO = Read Only

NOTE—These bit refer to “slow” data. 10PASS-TS uses the slow data channel as referenced in T1.424. The name is kept here to simplify a comparison between the two documents

45.2.1.39.1 LoM (1.68.8)

When read as a one, this bit indicates that the PMA/PMD is receiving a signal whose SNR margin is below the set threshold (see 45.2.1.21). The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.2 lpr (1.68.7)

When read as a one, this bit indicates that the PMA/PMD is not receiving sufficient power supply input for proper operation. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.3 po (1.68.6)

When read as a one, this bit indicates that the PMA/PMD has been instructed to power off. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.4 Rdi (1.68.5)

When read as a one, this bit indicates that the PMA/PMD has received PMA/PMD frames containing severe errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.5 los (1.68.4)

When read as a one, this bit indicates that the PMA/PMD is not receiving a valid signal. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.6 fec-f (1.68.3)

This bit is reserved and shall read as zero for 10PASS-TS.

45.2.1.39.7 be-f (1.68.2)

This bit is reserved and shall read as zero for 10PASS-TS.

45.2.1.39.8 fec-s (1.68.1)

When read as a one, this bit indicates that the PMA/PMD is receiving FEC blocks with one or more correctable errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.39.9 be-s (1.68.0)

When read as a one, this bit indicates that the PMA/PMD is receiving FEC blocks with one or more uncorrectable errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40 10P incoming indicator bits status register (Register 1.69)

The 10P indicator bits status register conveys the current state of the indicator bits being received from the link partner's PMA (see 62.3.4.7). The bit definitions for the 10P incoming indicator bits status register are shown in Table 45–35.

Table 45–36—10P incoming indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.69.15:9	Reserved	Value always 0, writes ignored	RO
1.69.8	LoM	1 = received signal below SNR margin threshold 0 = normal state	RO
1.69.7	Flpr	1 = power supply voltage invalid 0 = normal state	RO
1.69.6	Fpo	1 = PMA/PMD is being powered off 0 = normal state	RO
1.69.5	Rdi	1 = severely errored frames have been received 0 = normal state	RO
1.69.4	Flos	1 = signal power is lower than the threshold 0 = normal state	RO
1.69.3:2	Reserved	Value always 0	RO
1.69.1	Ffec-s	1 = corrected errors have been detected in the received FEC block of slow data 0 = normal state	RO
1.69.0	Febe-s	1 = non-corrected errors have been detected in the received block of slow data 0 = normal state	RO

[a]RO = Read Only

NOTE —These bit refer to "slow" data. 10PASS-TS uses the slow data channel as referenced in T1.424. The name is kept here to simplify a comparison between the two documents.

45.2.1.40.1 LoM (1.69.8)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving a signal whose SNR margin is below the set threshold (see 45.2.1.21). The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.2 Flpr (1.69.7)

When read as a one, this bit indicates that the link partner PMA/PMD is not receiving sufficient power supply input for proper operation. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.3 Fpo (1.69.6)

When read as a one, this bit indicates that the link partner PMA/PMD has been instructed to power off. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.4 Rdi (1.69.5)

When read as a one, this bit indicates that the link partner PMA/PMD has received PMA/PMD frames containing severe errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.5 Flos (1.69.4)

When read as a one, this bit indicates that the link partner PMA/PMD has is not receiving a valid signal. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.6 Ffec-s (1.69.1)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving FEC blocks with one or more correctable errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.40.7 Febe-s (1.69.0)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving FEC blocks with one or more uncorrectable errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.41 10P cyclic extension configuration register (Register 1.70)

The 10P cyclic extension configuration register controls the length of the cyclic extension for the 10P PMD. For more information, see 62.3.4.2. The value of the cyclic extension is equal to the decimal value set in bits 15:0. Values of decimal 10, 20 and 40 are valid. Writes to set any other values shall be ignored. Upon reset, the PMD shall set these bits to a decimal value of 20.

The bit definitions for this register are shown in Table 45–37.

Table 45–37—10P cyclic extension configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.70.15:0	Cyclic extension	The value of the cyclic extension	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.42 10P attainable downstream data rate register (Register 1.71)

The 10P attainable downstream data rate register reports the data rate that the -R link partner measures to be the highest data rate for downstream transmission. The data rate is encoded as 1 kb/s times the decimal value of the register bits 15:0. The value of the register bits are not valid until after link is “up” (see 45.2.1.13.4).

The bit definitions for this register are found in Table 45–38.

Table 45–38—10P attainable downstream data rate register bit definitions

Bit(s)	Name	Description	R/W[a]
1.71.15:0	Attainable downstream data rate	Data rate in 1 kb/s increments	RO

[a]RO = Read Only

45.2.1.43 2B general parameter register (Register 1.80)

The 2B general parameter register controls various parameters for the operation of the 2BASE-TL PMA/PMD.

This register is read only for -R ports which may be read so the STA may know the mode selected by the -O port. The selected parameters on the -O are sent to the -R link partner on link initialization. For more information on how these parameters are passed across the physical link using G.994.1 signalling (see 61B.3.2).

The bit definitions for the 2B general parameter register are found in Table 45–39.

Table 45–39— 2B general parameter register bit definition

Bit(s)	Name	Description	R/W[a]
1.80.15	Reserved	Value always 0, writes ignored	R/W
1.80.14:10	PMMS target margin	margin = 14:10 - 10dB	R/W
1.80.9	Line probing control	1 = use line probing 0 = do not use line probing (default)	R/W
1.80.8	Noise environment	1 = current condition 0 = worst case (default)	R/W
1.80.7:2	Reserved	Value always 0, writes ignored	R/W
1.80.1:0	Region	Selects the regional annex to operate under 00 = Annex A 01 = Annex B 10 = Annex C 11 = reserved, writes ignored	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.43.1 PMMS target margin (1.80.14:10)

The PMMS target margin specified in bits 14:10 specifies the noise margin that the PMMS procedure tries to attain. The margin is expressed in dB as the decimal value of bits 14:10 minus 10dB. The margin specified is measured either against either worst case or current line conditions, based on the value set in 1.80.8.

The PMMS margin value is transferred during 2BASE-TL initialization via the worst case PMMS margin bits in Table 61B–57 and Table 61B–43, or the current condition PMMS margin bits in Table 61B–48 and Table 61B–44.

45.2.1.43.2 Line probing control (1.80.9)

When set to a one, this bit tells the PMA/PMD to perform line probing the next time link is initialized. When set to a zero, the PMA/PMD does not use line probing. Line probing causes the PMA/PMD to select probe duration and the link data rate. For more information, see the documents referenced in 63.3.

45.2.1.43.3 Noise environment (1.80.8)

This bit controls the reference noise used during line probing. When set to a one, the noise environment is based on the current line conditions. When set to a zero, the noise environment is based on worst case models. For more information, see the documents referenced in 63.3.

45.2.1.43.4 Region (1.80.1:0)

These bits select the regional annex that is used for the operation of the 2BASE-TL PMA/PMD. These annexes refer to clauses in documents referenced by the 2BASE-TL PMA/PMD specification. These are not annexes in IEEE Std 802.3-2002 or its amendments. For details on each annex, see the document referenced in 63.1.3.

45.2.1.44 2B PMD parameters registers (Registers 1.81 through 1.88)

The 2B PMD parameters registers set the transmission parameters for an individual 2BASE-TL PMA/PMD link. When the link is initialized, these parameters are used by the link partner PMA/PMDs in an attempt to achieve specified settings.

These registers allow one to specify a single fixed data rate or up to four data rate ranges at the -O PMA/PMD. An additional set of four data ranges are found in the 2B extended PMD parameters registers (1.102 through 1.109). Bit descriptions for the 2B extended PMD parameters registers are found in 45.2.1.58. Together these sets allow up to eight data rate ranges to be specified.

If at least one data rate range is specified with different Minimum and Maximum data rates, the link is trained with the highest attainable rate. If line probing is enabled, the highest rate is determined by the result of line probing and the “Data rate step” value is ignored. If line probing is disabled, the minimum and maximum rate, “Data rate step” and “Power” values are used to determine the highest attainable rate.

In the case of a single fixed rate specified (Minimum data rate1 equals Maximum data rate1, Data rate step[1:8] set to zero, Minimum/Maximum data rate[2:8] set to zero), the link is trained at the specified rate.

When multiple ranges are specified, the PMD selects the first attainable range, starting sequentially from the first range.

Since writing to this register does not have an immediate effect, reading this register returns the desired parameters, which are not necessarily the current operating parameters.

For more information on how these parameters are passed across the physical link using G.994.1 signalling (see 61B.3.2).

The bit definitions for the 2B PMD parameters register are found in Table 45–40.

Table 45–40— 2B PMD parameters registers bit definition

Bit(s)	Name	Description	R/W[a]
1.81.15	Reserved	Value always 0, writes ignored	R/W
1.81.14:8	Min data rate1	Min data rate of the first range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.81.7	Reserved	Value always 0, writes ignored	R/W
1.81.6:0	Max data rate1	Max data rate of the first range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.82.15:14	Reserved	Value always 0, writes ignored	R/W
1.82.13:7	Data rate step1	Data rate step of the first range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.82.6:2	Power1	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.82.1:0	Constellation1	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.83.15	Reserved	Value always 0, writes ignored	R/W
1.83.14:8	Min data rate2	Min data rate of the second range n = value of the bits, n valid 3 to 89 Data Rate =64n kb/s	O: R/W R: RO
1.83.7	Reserved	Value always 0, writes ignored	R/W
1.83.6:0	Max data rate2	Max data rate of the second range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.84.15:14	Reserved	Value always 0, writes ignored	R/W
1.84.13:7	Data rate step2	Data rate step of the second range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.84.6:2	Power2	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.84.1:0	Constellation2	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.85.15	Reserved	Value always 0, writes ignored	R/W
1.85.14:8	Min data rate3	Min data rate of the third range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.85.7	Reserved	Value always 0, writes ignored	R/W

Table 45–40— 2B PMD parameters registers bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.85.6:0	Max data rate3	Max data rate of the third range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.86.15:14	Reserved	Value always 0, writes ignored	R/W
1.86.13:7	Data rate step3	Data rate step of the third range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.86.6:2	Power3	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.86.1:0	Constellation3	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.87.15	Reserved	Value always 0, writes ignored	R/W
1.87.14:8	Min data rate4	Min data rate of the fourth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.87.7	Reserved	Value always 0, writes ignored	R/W
1.87.6:0	Max data rate4	Max data rate of the fourth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.88.15:14	Reserved	Value always 0, writes ignored	R/W
1.88.13:7	Data rate step4	Data rate step of the fourth range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.88.6:2	Power4	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.88.1:0	Constellation4	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.44.1 Minimum data rate (1.81 through 87.14:8)

Bits 14:8 in registers 1.81 through 1.87 set the minimum data rate for each of the four ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 14:8 by 64.

45.2.1.44.2 Max data rate (1.81 through 87.6:0)

Bits 6:0 in registers 1.81 through 1.87 set the maximum data rate for each of the four ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 6:0 by 64.

45.2.1.44.3 Data rate step (1.82 through 88.13:7)

Bits 13:7 in registers 1.82 through 1.88 set the granularity used by the PMA/PMD when determining the line rate. Valid values for these bits are decimal 1 through 86, writes to set an invalid value shall be ignored. The data rate step is expressed in units of kb/s and is derived by multiplying the decimal value of bits 13:7 by 64.

45.2.1.44.4 Power (1.82 through 88.6:2)

Bits 6:2 in registers 1.82 through 1.88 set the allowed power level for each data rate range. The power levels set in these bits override those of the annex selected in the 2B general parameter register (1.80). The power level is expressed in units of dBm and is derived by the following equation, where x equals the value of bits 6:2.

$$power = \left(5 + \frac{x}{2}\right) \text{ dBm} \qquad (45–3)$$

45.2.1.44.5 Constellation (1.82 through 88.1:0)

Bits 1:0 in registers 1.82 through 1.88 set the allowed constellation for each data rate range. Setting a value of 10 or 01 restricts the constellation to 16- or 32-TCPAM respectively. When set to a value of 00, the PMD automatically determines the constellation during initialization. Attempts to set a value of 11 shall be ignored.

45.2.1.45 2B code violation errors counter (Register 1.89)

The 2B code violation errors counter is a 16-bit counter that contains the number of the 2BASE-TL CRC anomalies. See 63.2.2.3 for more information. These bits shall be set to all zeros upon an MMD reset and upon being read.

Bit definitions for the 2B code violation errors counter are found in Table 45–41.

Table 45–41—2B code violation errors counter bit definitions

Bits(s)	Name	Description	R/W[a]
1.89.15:0	Code violations [15:0]	The bytes of the counter	RO

[a]RO = Read Only

45.2.1.46 2B link partner code violations register (Register 1.90)

The 2B link partner code violations register provides the -O STA with a snapshot of the -R link partner's 2B code violations counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–41.

45.2.1.47 2B errored seconds counter (Register 1.91)

This 8-bit counter contains the number of errored seconds (see 63.2.2.3) These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B errored seconds counter are found in Table 45–42.

Table 45–42—2B errored seconds counter bit definitions

Bits(s)	Name	Description	R/W[a]
1.91.15:8	Reserved	Value always 0, writes ignored	RO
1.91.7:0	Errored seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.48 2B link partner errored seconds register (Register 1.92)

The 2B link partner errored seconds register provides the -O STA with a snapshot of the -R link partner's 2B errored seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–42.

45.2.1.49 2B severely errored seconds counter (Register 1.93)

This 8-bit counter contains the number severely errored seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B severely errored seconds register are found in Table 45–43.

Table 45–43—2B severely errored counter register bit definitions

Bits(s)	Name	Description	R/W[a]
1.93.15:8	Reserved	Value always 0, writes ignored	RO
1.93.7:0	Severely errored seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.50 2B link partner severely errored seconds register (Register 1.94)

The 2B link partner severely errored seconds register provides the -O STA with a snapshot of the -R link partner's 2B severely errored seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–43.

45.2.1.51 2B LOSW counter (Register 1.95)

This 8-bit counter contains the number of loss of sync seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B LOSW counter are found in Table 45–44.

Table 45–44—2B LOSW counter bit definitions

Bits(s)	Name	Description	R/W[a]
1.95.15:8	Reserved	Value always 0, writes ignored	RO
1.95.7:0	loss of sync seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.52 2B link partner LOSW register (Register 1.96)

The 2B link partner LOSW register provides the -O STA with a snapshot of the -R link partner's 2B LOSW counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–44.

45.2.1.53 2B unavailable seconds counter (Register 1.97)

This 8-bit counter contains the number of unavailable seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B unavailable seconds counter are found in Table 45–45.

Table 45–45—2B unavailable seconds counter bit definitions

Bits(s)	Name	Description	R/W[a]
1.97.15:8	Reserved	Value always 0, writes ignored	RO
1.97.7:0	unavailable seconds [7:0]	The byte of the counter	RO

[a]RO = Read Only

45.2.1.54 2B link partner unavailable seconds register (Register 1.98)

The 2B link partner unavailable seconds register provides the -O STA with a snapshot of the -R link partner's 2B unavailable seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–45.

45.2.1.55 2B state defects register (Register 1.99)

The 2B state defects register is used to communicate defect states from the 2BASE-TL PMD (see 63.2.2.3). The thresholds for these defects are set using the 2B line quality threshold register (see 45.2.1.21). The register bits are cleared to zero when read by the STA or upon MMD reset. On a -R PMA/PMD, these bits are also cleared to zero upon the successful reception of a "Get link partner parameters" command (see 45.2.1.13.1).

Bit definitions for the 2B state defects register are found in Table 45–46.

Table 45–46—2B state defects register bit definitions

Bits(s)	Name	Description	R/W[a]
1.99.15	Segment defect	1 = segment defect detected 0 = normal condition	RO, LH
1.99.14	SNR margin defect	1 = SNR margin defect detected 0 = normal condition	RO, LH
1.99.13	Loop attenuation defect	1 = loop attenuation defect detected 0 = normal condition	RO, LH
1.99.12	Loss of sync word	1 = loss of sync word detected 0 = normal condition	RO, LH
1.99.11:0	Reserved	Value always 0, writes ignored	R/W

[a]RO = Read Only, LH = Latching High, R/W = Read/Write

45.2.1.55.1 Segment defect (1.99.15)

When read as a one, this bit indicates that the local PMA/PMD has detected a segment defect.

45.2.1.55.2 SNR margin defect (1.99.14)

When read as a one, this bit indicates that the local PMA/PMD has received a signal whose SNR is below the set threshold (see 45.2.1.21).

45.2.1.55.3 Loop attenuation defect (1.99.13)

When read as a one, this bit indicates that the PMA/PMD has detected that the loop attenuation is below the set threshold (see 45.2.1.21).

45.2.1.55.4 Loss of sync word (1.99.12)

When read as a one, this bit indicates that the PMA/PMD has lost PMA/PMD frame sync.

45.2.1.56 2B link partner state defects register (Register 1.100)

The 2B link partner state defects register provides the -O STA with a snapshot of the -R link partner's 2B state defects register. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.13) and the command completes successfully (see 45.2.1.15.1).

This register is defined for -O port sub-types only.

The bit definitions for this register are found in Table 45–46.

45.2.1.57 2B negotiated constellation register (Register 1.101)

The bit definitions for this register are shown in Table 45–47.

Table 45–47—2B register bit definition

Bit(s)	Name	Description	R/W[a]
1.101.15:2	Reserved	Value always 0, writes ignored	R/W
1.101.1:0	Negotiated constellation	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = undetermined	RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.57.1 Negotiated constellation (1.101.1:0)

These bits report the resulting constellation that was obtained after initialization. For more information on configuring 2BASE-TL PMA/PMD link initialization, see the 2B PMD parameter registers (see 45.2.1.44). When read as 10 or 01, the constellation has been set as either 16- or 32-TCPAM respectively. When read as 00, the local PMD has not arrived at a constellation with its link partner (as may be the case while link is down or initializing, after reset or upon a failed initialization).

45.2.1.58 2B extended PMD parameters registers (Registers 1.102 through 1.109)

The 2B extended PMD parameters registers define four additional data range sets to be used in conjunction with the 2B PMD parameters registers when additional PMD configuration detail is desired. For a complete description of the use of these registers, see 45.2.1.44.

Bit definitions for these registers can be found in Table 45–48

Table 45–48— 2B extended PMD parameters registers bit definition

Bit(s)	Name	Description	R/W[a]
1.102.15	Reserved	Value always 0, writes ignored	R/W
1.102.14:8	Min data rate5	Min data rate of the fifth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.102.7	Reserved	Value always 0, writes ignored	R/W
1.102.6:0	Max data rate5	Max data rate of the fifth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.103.15:14	Reserved	Value always 0, writes ignored	R/W
1.103.13:7	Data rate step5	Data rate step of the fifth range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.103.6:2	Power5	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.103.1:0	Constellation5	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.104.15	Reserved	Value always 0, writes ignored	R/W
1.104.14:8	Min data rate6	Min data rate of the sixth range n = value of the bits, n valid 3 to 89 Data Rate =64n kb/s	O: R/W R: RO
1.104.7	Reserved	Value always 0, writes ignored	R/W
1.104.6:0	Max data rate6	Max data rate of the sixth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.105.15:14	Reserved	Value always 0, writes ignored	R/W
1.105.13:7	Data rate step6	Data rate step of the sixth range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.105.6:2	Power6	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.105.1:0	Constellation6	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.106.15	Reserved	Value always 0, writes ignored	R/W
1.106.14:8	Min data rate7	Min data rate of the seventh range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.106.7	Reserved	Value always 0, writes ignored	R/W

Table 45–48— 2B extended PMD parameters registers bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.106.6:0	Max data rate7	Max data rate of the seventh range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.107.15:14	Reserved	Value always 0, writes ignored	R/W
1.107.13:7	Data rate step7	Data rate step of the seventh range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.107.6:2	Power7	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.107.1:0	Constellation7	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.108.15	Reserved	Value always 0, writes ignored	R/W
1.108.14:8	Min data rate8	Min data rate of the eighth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.108.7	Reserved	Value always 0, writes ignored	R/W
1.108.6:0	Max data rate8	Max data rate of the eighth range n = value of the bits, n valid 3 to 89 Data Rate = 64n kb/s	O: R/W R: RO
1.109.15:14	Reserved	Value always 0, writes ignored	R/W
1.109.13:7	Data rate step8	Data rate step of the eighth range n = value of the bits, n valid 1 to 86 Data Rate = 64n kb/s	O: R/W R: RO
1.109.6:2	Power8	x = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5x) dBm	O: R/W R: RO
1.109.1:0	Constellation8	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.1.58.1 Minimum data rate (1.102 through 108.14:8)

Bits 14:8 in registers 1.102 through 1.108 set the minimum data rate for each of the four extended ranges. Valid values for these bits are decimal 3 through 89. writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 14:8 by 64.

45.2.1.58.2 Max data rate (1.102 through 108.6:0)

Bits 6:0 in registers 1.102 through 1.108 set the maximum data rate for each of the four extended ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 6:0 by 64.

45.2.1.58.3 Data rate step (1.103 through 109.13:7)

Bits 13:7 in registers 1.102 through 1.109 set the granularity used by the PMA/PMD when determining the line rate. Valid values for these bits are decimal 1 through 86, writes to set an invalid value shall be ignored. The data rate step is expressed in units of kb/s and is derived by multiplying the decimal value of bits 13:7 by 64.

45.2.1.58.4 Power (1.103 through 109.6:2)

Bits 6:2 in registers 1.103 through 1.109 set the allowed power level for each extended data rate range. The power levels set in these bits override those of the annex selected in the 2B general parameter register (1.80). The power level is expressed in units of dBm and is derived by the following equation, where x equals the value of bits 6:2.

$$\text{power} = \left(5 + \frac{x}{2}\right) \text{ dBm} \qquad (45\text{–}4)$$

45.2.1.58.5 Constellation (1.103 through 109.1:0)

Bits 1:0 in registers 1.103 through 1.109 set the allowed constellation for each extended data rate range. Setting a value of 10 or 01 restricts the constellation to 16- or 32-TCPAM respectively. When set to a value of 00, the PMD automatically determines the constellation during initialization. Attempts to set a value of 11 shall be ignored.

Insert sections 45.2.1.59 through 45.2.1.61 including all sub sections and tables.

45.2.1.59 10GBASE-T status (Register 1.129)

45.2.1.59.1 The assignments of bit in the 10GBASE-T status regiser is shown in Table 45–49

45.2.1.59.2 LP information valid (1.129.0)

Editor comment: this bit needs to get cleared on loss of link, phy reset, or other condition(s) TBD.

When read as a logic one, bit 1.129.0 indicates that the startup protocol defined in TBD (55.?.) has been completed, and that the contents of bits 1.130.12:8 and 1.131.15:8 which are set during the startup protocol are valid. When read as a logic zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of bits 1.130.12:8 and 1.131.15:8 which are established during the startup protocol and invalid. A 10GBASE-T PMA shall return a value of zero in bit 1.129.0 if TBD. .

Table 45–49—10GBASE-T status register bit definitions

Bits(s)	Name	Description	R/W[a]
1.129.15:1	Reserved	Value always 0, writes ignored	RO
1.129.0	LP information valid	1 = Link partner information is valid 0 = Link partner information is invalid	RO

[a]RO = Read Only

45.2.1.60 10GBASE-T THP setting (Register 1.130)

The THP setting register will reflect the THP setting selected during the startup process and will only be valid if bit 1.129.0 is set to one. The startup process and all THP settings are defined in TBD (55.???). As described in TBD, only one THP setting may be selected at any time. The assignment of bits for the precoder setting are shown in Table 45–50..

Table 45–50—10GBASE-T THP setting register bit definitions

Bit(s)	Name	Description	R/W[a]
1.130.15:13	Reserved	Value always 0, writes ignored	RO
1.130.12	Link Partner THP 4 setting	1 = Link partner THP setting four is selected 0 = Link partner setting four is not selected	RO
1.130.11	Link Partner THP 3 setting	1 = Link partner setting four is selected 0 = Link partner setting four is not selected	RO
1.130.10	Link Partner THP 2 setting	1 = Link partner setting four is selected 0 = Link partner setting four is not selected	RO
1.130.9	Link Partner THP 1 setting	1 = Link partner setting four is selected 0 = Link partner setting four is not selected	RO
1.130.8	Link Partner THP 0 bypass	1 = Link partner setting four is selected 0 = Link partner setting four is not selected	RO
1.130.7:5	Reserved	Value always 0, writes ignored	RO
1.130.4	THP 4 setting	1 = PMA THP setting four is selected 0 = PMA THP setting four is not selected	RO
1.130.3	THP 3 setting	1 = PMA THP setting four is selected 0 = PMA THP setting four is not selected	RO
1.130.2	THP 2 setting	1 = PMA THP setting four is selected 0 = PMA THP setting four is not selected	RO
1.130.1	THP 1 setting	1 = PMA THP setting four is selected 0 = PMA THP setting four is not selected	RO
1.130.0	THP 0 bypass	1 = PMA THP setting four is selected 0 = PMA THP setting four is not selected	RO

[a]RO = Read Only

45.2.1.60.1 Link partner THP 4 setting (1.130.12)

When read as a one, bit 1.130.12 indicates that the 10GBASE-T PMA link partner will operate with THP setting 4. When read as a zero, bit 1.130.12 indicates that the 10GBASE-T PMA link partner will not operate with THP setting 4.

45.2.1.60.2 Link partner THP 3 setting (1.130.11)

When read as a one, bit 1.130.11 indicates that the 10GBASE-T PMA link partner will operate with THP setting 3. When read as a zero, bit 1.130.11 indicates that the 10GBASE-T PMA link partner will not able to operate with THP setting 3.

45.2.1.60.3 Link partner THP 2 setting (1.130.10)

IWhen read as a one, bit 1.130.10 indicates that the 10GBASE-T PMA link partner will to operate with THP setting 2. When read as a zero, bit 1.130.10 indicates that the 10GBASE-T PMA link partner will not able to operate with THP setting 2.

45.2.1.60.4 Link partner THP 1 setting (1.130.9)

When read as a one, bit 1.130.9 indicates that the 10GBASE-T PMA link partner will operate with THP setting 1. When read as a zero, bit 1.130.9 indicates that the 10GBASE-T PMA link partner will not able to operate with THP setting 1.

45.2.1.60.5 Link partner THP 0 bypass setting (1.130.8)

When read as a one, bit 1.130.8 indicates that the 10GBASE-T PMA link partner will operate in THP bypass mode. When read as a zero, bit 1.130.8 indicates that the 10GBASE-T PMA link partner will not able to operate in THP bypass mode.

45.2.1.60.6 If THP 4 setting (1.130.4)

When read as a one, bit 1.130.4 indicates that the 10GBASE-T PMA will operate with THP setting 4. When read as a zero, bit 1.130.4 indicates that the 10GBASE-T PMA will not operate with THP setting 4.

45.2.1.60.7 THP 3 setting (1.130.3)

When read as a one, bit 1.130.3 indicates that the 10GBASE-T PMA will operate with THP setting 3. When read as a zero, bit 1.130.3 indicates that the 10GBASE-T PMA will not operate with THP setting 3.

45.2.1.60.8 THP 2 setting (1.130.2)

When read as a one, bit 1.130.2 indicates that the 10GBASE-T PMA will operate with THP setting 2. When read as a zero, bit 1.130.2 indicates that the 10GBASE-T PMA will not operate with THP setting 2.

45.2.1.60.9 THP 1 setting (1.130.1)

When read as a one, bit 1.130.1 indicates that the 10GBASE-T PMA will operate with THP setting 1. When read as a zero, bit 1.130.1 indicates that the 10GBASE-T PMA will not operate with THP setting 1.

45.2.1.60.10 THP 0 bypass (1.130.0)

When read as a one, bit 1.130.0 indicates that the 10GBASE-T PMA will bypass THP. When read as a zero, bit 1.130.0 indicates that the 10GBASE-T PMA will not bypass THP.

45.2.1.61 10GBASE-T TX power level setting (Register 1.133)

The TX power level setting register will reflect the TX power level selected during the startup negotiation process. The startup negotiation process and all TX power level settings are defined in TBD (55.???). As described in TBD, only one TX power level setting may be selected at any time. If bit 1.129.0 is set to zero bits 1.131.15:8 will not indicate the TX power level setting of the link partner. The assignment of bits for the precoder setting are shown in Table .

Table 45–51—10GBASE-T TX power level setting register bit definitations

Bits(s)	Name	Description	R/W[a]
1.131.15	Link partner TX power level 7	1 = Link partner is operating with TX power level setting seven 0 = Link partner is not operating with TX power level setting seven	RO
1.131.14	Link partner TX power level 6	1 = Link partner is operating with TX power level setting six 0 = Link partner is not operating with TX power level setting six	RO
1.131.13	Link partner TX power level 5	1 = Link partner is operating with TX power level setting five 0 = Link partner is not operating with TX power level setting five	RO
1.131.12	Link partner TX power level 4	1 = Link partner is operating with TX power level setting four 0 = Link partner is not operating with TX power level setting four	RO
1.131.11	Link partner TX power level 3	1 = Link partner is operating with TX power level setting three 0 = Link partner is not operating with TX power level setting three	RO
1.131.10	Link partner TX power level 2	1 = Link partner is operating with TX power level setting two 0 = Link partner is not operating with TX power level setting two	RO
1.131.9	Link partner TX power level 1	1 = Link partner is operating with TX power level setting one 0 = Link partner is not operating with TX power level setting one	RO
1.131.8	Link partner TX power level 0	1 = Link partner is operating with TX power level setting 0 0 = Link partner is not operating with TX power level setting 0	RO
1.131.7	TX power level 7	1 = PMA is operating with TX power level setting seven 0 = PMA is not operating with TX power level setting seven	RO
1.131.6	TX power level 6	1 = PMA is operating with TX power level setting six 0 = PMA is not operating with TX power level setting six	RO
1.131.5	TX power level 5	1 = PMA is operating with TX power level setting five 0 = PMA is not operating with TX power level setting five	RO
1.131.4	TX power level 4	1 = PMA is operating with TX power level setting four 0 = PMA is not operating with TX power level setting four	RO
1.131.3	TX power level 3	1 = PMA is operating with TX power level setting three 0 = PMA is not operating with TX power level setting three	RO
1.131.2	TX power level 2	1 = PMA is operating with TX power level setting two 0 = PMA is not operating with TX power level setting two	RO
1.131.1	TX power level 1	1 = PMA is operating with TX power level setting one 0 = PMA is not operating with TX power level setting one	RO
1.131.0	TX power level 0	1 = PMA is operating with TX power level setting 0 0 = PMA is not operating with TX power level setting 0	RO

[a]RO = Read Only

45.2.1.61.1 Link partner TX power level 7 setting (1.131.15)

If bit 1.129.0 is set to one and bit 1.131.15 is set to one then bit 1.131.15 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 7. If bit 1.129.0 is set to one and bit 1.131.15 is set to zero then bit 1.131.15 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 7.

45.2.1.61.2 Link partner TX power level 6 setting (1.131.14)

If bit 1.129.0 is set to one and bit 1.131.14 is set to one then bit 1.131.14 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 6. If bit 1.129.0 is set to one and bit 1.131.14 is set to zero then bit 1.131.14 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 6.

45.2.1.61.3 Link partner TX power level 5 setting (1.131.13)

If bit 1.129.0 is set to one and bit 1.131.13 is set to one then bit 1.131.13 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 5. If bit 1.129.0 is set to one and bit 1.131.13 is set to zero then bit 1.131.13 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 5.

45.2.1.61.4 Link partner TX power level 4 setting (1.131.12)

If bit 1.129.0 is set to one and bit 1.131.12 is set to one then bit 1.131.12 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 4. If bit 1.129.0 is set to one and bit 1.131.12 is set to zero then bit 1.131.12 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 4.

45.2.1.61.5 Link partner TX power level 3 setting (1.131.11)

If bit 1.129.0 is set to one and bit 1.131.11 is set to one then bit 1.131.11 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 3. If bit 1.129.0 is set to one and bit 1.131.11 is set to zero then bit 1.131.11 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 3.

45.2.1.61.6 Link partner TX power level 2 setting (1.131.10)

If bit 1.129.0 is set to one and bit 1.131.10 is set to one then bit 1.131.10 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 2. If bit 1.129.0 is set to one and bit 1.131.10 is set to zero then bit 1.131.10 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 2.

45.2.1.61.7 Link partner TX power level 1 setting (1.131.9)

If bit 1.129.0 is set to one and bit 1.131.9 is set to one then bit 1.131.9 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level setting 1. If bit 1.129.0 is set to one and bit 1.131.9 is set to zero then bit 1.131.9 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level setting 1.

45.2.1.61.8 Link partner TX power level 0 setting (1.131.8)

If bit 1.129.0 is set to one and bit 1.131.8 is set to one then bit 1.131.8 indicates that the 10GBASE-T PMA link partner has the ability to operate with TX power level 0. If bit 1.129.0 is set to one and bit 1.131.8 is set to zero then bit 1.131.8 indicates that the 10GBASE-T PMA link partner is not able to operate with TX power level 0.

45.2.1.61.9 TX power level 7 setting (1.131.7)

When read as a one, bit 1.131.7 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 7. When read as a zero, bit 1.131.7 indicates that the 10GBASE-T PMA is not able to support TX power level setting 7.

45.2.1.61.10 TX power level 6 setting (1.131.6)

When read as a one, bit 1.131.6 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 6. When read as a zero, bit 1.131.6 indicates that the 10GBASE-T PMA is not able to support TX power level setting 6.

45.2.1.61.11 TX power level 5 setting (1.131.5)

When read as a one, bit 1.131.5 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 5. When read as a zero, bit 1.131.5 indicates that the 10GBASE-T PMA is not able to support TX power level setting 5.

45.2.1.61.12 TX power level 4 setting (1.131.4)

When read as a one, bit 1.131.4 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 4. When read as a zero, bit 1.131.4 indicates that the 10GBASE-T PMA is not able to support TX power level setting 4.

45.2.1.61.13 TX power level 3 setting (1.131.3)

When read as a one, bit 1.131.3 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 3. When read as a zero, bit 1.131.3 indicates that the 10GBASE-T PMA is not able to support TX power level setting 3.

45.2.1.61.14 TX power level 2 setting (1.131.2)

When read as a one, bit 1.131.2 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 2. When read as a zero, bit 1.131.2 indicates that the 10GBASE-T PMA is not able to support TX power level setting 2.

45.2.1.61.15 TX power level 1 setting (1.131.1)

When read as a one, bit 1.131.1 indicates that the 10GBASE-T PMA has the ability to support TX power level setting 1. When read as a zero, bit 1.131.1 indicates that the 10GBASE-T PMA is not able to support TX power level setting 1.

45.2.1.61.16 TX power level 0 setting (1.131.0)

When read as a one, bit 1.131.0 indicates that the 10GBASE-T PMA has the ability to support TX power level zero. When read as a zero, bit 1.131.0 indicates that the 10GBASE-T PMA is not able to support TX power level zero.

45.2.2 WIS registers

The assignment of registers in the WIS is shown in Table 45–52. For the WIS octet fields, bit 8 of the corresponding field in the WIS frame maps to the lowest numbered bit of the field in the register.

45.2.2.1 WIS control 1 register (Register 2.0)

The assignment of bits in the WIS control 1 register is shown in Table 45–53. The default value for each bit of the WIS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–52—WIS registers

Register address	Register name
2.0	WIS control 1
2.1	WIS status 1
2.2, 2.3	WIS device identifier
2.4	WIS speed ability
2.5, 2.6	WIS devices in package
2.7	10G WIS control 2
2.8	10G WIS status 2
2.9	10G WIS test-pattern error counter
2.10 through 2.13	Reserved
2.14, 2.15	WIS package identifier
2.16 through 2.32	Reserved
2.33	10G WIS status 3
2.34 through 2.36	Reserved
2.37	10G WIS far end path block error count
2.38	Reserved
2.39 through 2.46	10G WIS J1 transmit
2.47 through 2.54	10G WIS J1 receive
2.55, 2.56	10G WIS far end line BIP errors
2.57, 2.58	10G WIS line BIP errors
2.59	10G WIS path block error count
2.60	10G WIS section BIP error count
2.61 through 2.63	Reserved
2.64 through 2.71	10G WIS J0 transmit
2.72 through 2.79	10G WIS J0 receive
2.80 through 2.32 767	Reserved
2.32 768 through 2.65 535	Vendor specific

Table 45–53— WIS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.0.15	Reset	1 = WIS reset 0 = Normal operation	R/W SC
2.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
2.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.12	Reserved	Value always 0, writes ignored	R/W
2.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
2.0.10:7	Reserved	Value always 0, writes ignored	R/W
2.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
2.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.2.1.1 Reset (2.0.15)

Resetting a WIS is accomplished by setting bit 2.0.15 to a one. This action shall set all WIS registers to their default states. As a consequence, this action may change the internal state of the WIS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a WIS shall return a value of one in bit 2.0.15 when a reset is in progress and a value of zero otherwise. A WIS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 2.0.15. During a reset, a WIS shall respond to reads from register bits 2.0.15 and 2.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.2.1.2 Loopback (2.0.14)

The WIS shall be placed in a Loopback mode of operation when bit 2.0.14 is set to a one. When bit 2.0.14 is set to a one, the WIS shall ignore all data presented to it by the PMA sublayer. When bit 2.0.14 is set to a one, the WIS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the detailed behavior of the WIS during loopback is specified in 50.3.9

The default value of bit 2.0.14 is zero.

NOTE—The signal path through the WIS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the WIS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.2.1.3 Low power (2.0.11)

A WIS may be placed into a low-power mode by setting bit 2.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the WIS. The behavior of the WIS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 2.0.11 is zero.

45.2.2.1.4 Speed selection (2.0.13, 2.0.6, and 2.0.5:2)

Speed selection bits 2.0.13 and 2.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the WIS may be selected using bits 5 through 2. The speed abilities of the WIS are advertised in the WIS speed ability register. A WIS may ignore writes to the WIS speed selection bits that select speeds it has not advertised in the WIS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The WIS speed selection defaults to a supported ability.

45.2.2.2 WIS status 1 register (Register 2.1)

The assignment of bits in the WIS status 1 register is shown in Table 45–54. All the bits in the WIS status 1 register are read only; a write to the WIS status 1 register shall have no effect.

Table 45–54—WIS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.1.15:8	Reserved	Ignore when read	RO
2.1.7	Fault	1 = Fault condition 0 = No fault condition	RO/LH
2.1.6:3	Reserved	Ignore when read	RO
2.1.2	Link status	1 = WIS link up 0 = WIS link down	RO/LL
2.1.1	Low-power ability	1 = WIS supports low-power mode 0 = WIS does not support low-power mode	RO
2.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High, LL = Latching Low

45.2.2.2.1 Fault (2.1.7)

When read as a one, bit 2.1.7 indicates that the WIS has detected a fault condition. When read as a zero, bit 2.1.7 indicates that the WIS has not detected a fault condition. The fault bit shall be implemented with latching high behavior.

The default value of bit 2.1.7 is zero.

45.2.2.2.2 Link status (2.1.2)

When read as a one, bit 2.1.2 indicates that the WIS receive link is up. When read as a zero, bit 2.1.2 indicates that the WIS receive link is down. The link status bit shall be implemented with latching low behavior.

45.2.2.2.3 Low-power ability (2.1.1)

When read as a one, bit 2.1.1 indicates that the WIS supports the low-power feature. When read as a zero, bit 2.1.1 indicates that the WIS does not support the low-power feature. If a WIS supports the low-power feature, then it is controlled using the low-power bit in the WIS control register.

45.2.2.3 WIS device identifier (Registers 2.2 and 2.3)

Registers 2.2 and 2.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of WIS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS device identifier.

The format of the WIS device identifier is specified in 22.2.4.3.1.

45.2.2.4 WIS speed ability (Register 2.4)

The assignment of bits in the WIS speed ability register is shown in Table 45–55.

Table 45–55— WIS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
2.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
2.4.0	10G capable	1 = WIS is capable of operating at 10 Gb/s 0 = WIS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.2.4.1 10G capable (2.4.0)

When read as a one, bit 2.4.0 indicates that the WIS is able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate). When read as a zero, bit 2.4.0 indicates that the WIS is not able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate).

45.2.2.5 WIS devices in package (Registers 2.5 and 2.6)

The WIS devices in package registers are defined in Table 45–7.

45.2.2.6 10G WIS control 2 register (Register 2.7)

The assignment of bits in the 10G WIS control 2 register is shown in Table 45–56. The default value for each bit of the 10G WIS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–56—10G WIS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.7.15:6	Reserved	Value always 0, writes ignored	R/W
2.7.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
2.7.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
2.7.3	Test-pattern selection	1 = Select square wave test pattern 0 = Select mixed-frequency test pattern	R/W
2.7.2	Receive test-pattern enable	1 = Enable test-pattern mode on the receive path 0 = Disable test-pattern mode on the receive path	R/W
2.7.1	Transmit test-pattern enable	1 = Enable test-pattern mode on the transmit path 0 = Disable test-pattern mode on the transmit path	R/W
2.7.0	PCS type selection	1 = Select 10GBASE-W PCS type 0 = Select 10GBASE-R PCS type	R/W

[a]R/W = Read/Write

45.2.2.6.1 PRBS31 receive test-pattern enable (2.7.5)

If the WIS supports the optional PRBS31 (see 49.2.8) pattern testing advertised in bit 2.8.1 and the mandatory receive test-pattern enable bit (2.7.2) is not one, setting bit 2.7.5 to a one shall set the receive path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2

45.2.2.6.2 PRBS31 transmit test-pattern enable (2.7.4)

If the WIS supports the optional PRBS31 pattern testing advertised in bit 2.8.1 and the mandatory transmit test-pattern enable bit (2.7.1) is not one, then setting bit 2.7.4 to a one shall set the transmit path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2

45.2.2.6.3 Test-pattern selection (2.7.3)

Bit 2.7.3 controls the type of pattern sent by the transmitter when in test-pattern mode. Setting bit 2.7.3 to a one shall select the square wave test pattern. Setting bit 2.7.3 to a zero shall select the mixed-frequency test pattern. The details of the test patterns are specified in Clause 50.

45.2.2.6.4 Receive test-pattern enable (2.7.2)

Setting bit 2.7.2 to a one shall set the receive path of the WIS into the test-pattern mode. Setting bit 2.7.2 to a zero shall disable the test-pattern mode on the receive path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50.

45.2.2.6.5 Transmit test-pattern enable (2.7.1)

Setting bit 2.7.1 to a one shall set the transmit path of the WIS into the test-pattern mode. Setting bit 2.7.1 to a zero shall disable the test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50.

45.2.2.6.6 PCS type selection (2.7.0)

Setting bit 2.7.0 to a one shall enable the 10GBASE-W logic and set the speed of the WIS-PMA interface to 9.95328 Gb/s. Setting bit 2.7.0 to a zero shall disable the 10GBASE-W logic, set the speed of the PCS-PMA interface to 10.3125 Gb/s and bypass the data around the 10GBASE-W logic. A WIS that is only capable of supporting 10GBASE-W operation and is unable to support 10GBASE-R operation shall ignore values written to this bit and shall return a value of one when read. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.2.7 10G WIS status 2 register (Register 2.8)

The assignment of bits in the 10G WIS status 2 register is shown in Table 45–57. All the bits in the 10G WIS status 2 register are read only; a write to the 10G WIS status 2 register shall have no effect.

Table 45–57—10G WIS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
2.8.13:2	Reserved	Ignore when read	RO
2.8.1	PRBS31 pattern testing ability	1 = WIS is able to support PRBS31 pattern testing 0 = WIS is not able to support PRBS31 pattern testing	RO
2.8.0	10GBASE-R ability	1 = WIS is able to support 10GBASE-R port types 0 = WIS is not able to support 10GBASE-R port types	RO

[a]RO = Read Only

45.2.2.7.1 Device present (2.8.15:14)

When read as <10>, bits 2.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 2.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.2.7.2 PRBS31 pattern testing ability (2.8.1)

When read as a one, bit 2.8.1 indicates that the WIS is able to support PRBS31 pattern testing. When read as a zero, bit 2.8.1 indicates that the WIS is not able to support PRBS31 pattern testing. If the WIS is able to support PRBS31 pattern testing, then the pattern generation and checking is controlled using bits 2.7.5:4.

45.2.2.7.3 10GBASE-R ability (2.8.0)

When read as a one, bit 2.8.0 indicates that the WIS is able to bypass the WIS logic and adjust the XSBI interface speed to support 10GBASE-R port types. When read as a zero, bit 2.8.0 indicates that the WIS is not able to bypass the WIS logic and cannot support 10GBASE-R port types.

45.2.2.8 10G WIS test-pattern error counter register (Register 2.9)

The assignment of bits in the 10G WIS test-pattern error counter register is shown in Table 45–58. This register is only required when the PRBS31 pattern generation capability is supported.

Table 45–58—10G WIS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
2.9.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read Only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the WIS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.8.

45.2.2.9 WIS package identifier (Registers 2.14 and 2.15)

Registers 2.14 and 2.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the WIS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the WIS package identifier is specified in 22.2.4.3.1.

45.2.2.10 10G WIS status 3 register (Register 2.33)

The assignment of bits in the 10G WIS status 3 register is shown in Table 45–59. All the bits in the 10G WIS status 3 register are read only; a write to the 10G WIS status 3 register shall have no effect.

Table 45–59—10G WIS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.33.15:12	Reserved	Ignore when read	RO
2.33.11	SEF	Severely errored frame	RO/LH
2.33.10	Far end PLM-P/LCD-P	1 = Far end path label mismatch / Loss of code-group delineation 0 = No far end path label mismatch / Loss of code-group delineation	RO/LH
2.33.9	Far end AIS-P/LOP-P	1 = Far end path alarm indication signal / Path loss of pointer 0 = No far end path alarm indication signal / Path loss of pointer	RO/LH
2.33.8	Reserved	Ignore when read	RO
2.33.7	LOF	1 = Loss of frame flag raised 0 = Loss of frame flag lowered	RO/LH
2.33.6	LOS	1 = Loss of signal flag raised 0 = Loss of signal flag lowered	RO/LH
2.33.5	RDI-L	1 = Line remote defect flag raised 0 = Line remote defect flag lowered	RO/LH
2.33.4	AIS-L	1 = Line alarm indication flag raised 0 = Line alarm indication flag lowered	RO/LH
2.33.3	LCD-P	1 = Path loss of code-group delineation flag raised 0 = Path loss of code-group delineation flag lowered	RO/LH
2.33.2	PLM-P	1 = Path label mismatch flag raised 0 = Path label mismatch flag lowered	RO/LH
2.33.1	AIS-P	1 = Path alarm indication signal raised 0 = Path alarm indication signal lowered	RO/LH
2.33.0	LOP-P	1 = Loss of pointer flag raised 0 = Loss of pointer flag lowered	RO/LH

[a]RO = Read Only, LH = Latching High

45.2.2.10.1 SEF (2.33.11)

When read as a one, bit 2.33.11 indicates that the SEF flag has been raised by the WIS. When read as a zero, bit 2.33.11 indicates that the SEF flag is lowered. The SEF bit shall be implemented with latching high behavior.

The SEF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.2 Far end PLM-P/LCD-P (2.33.10)

When read as a one, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag is lowered. The far end PLM-P/LCD-P bit shall be implemented with latching high behavior.

The far end path label mismatch/loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.3 Far end AIS-P/LOP-P (2.33.9)

When read as a one, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag has been raised by the WIS. When read as a zero, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag is lowered. The far end AIS-P/LOP-P bit shall be implemented with latching high behavior.

The far end path alarm indication signal/path loss of pointer functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.4 LOF (2.33.7)

When read as a one, bit 2.33.7 indicates that the loss of frame flag has been raised. When read as a zero, bit 2.33.7 indicates that the loss of frame flag is lowered. The LOF bit shall be implemented with latching high behavior.

The LOF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.5 LOS (2.33.6)

When read as a one, bit 2.33.6 indicates that the loss of signal flag has been raised. When read as a zero, bit 2.33.6 indicates that the loss of signal flag is lowered. The LOS bit shall be implemented with latching high behavior.

The LOS functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.6 RDI-L (2.33.5)

When read as a one, bit 2.33.5 indicates that the line remote defect flag has been raised. When read as a zero, bit 2.33.5 indicates that the line remote defect flag is lowered. The RDI-L bit shall be implemented with latching high behavior.

The RDI-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.7 AIS-L (2.33.4)

When read as a one, bit 2.33.4 indicates that the line alarm indication flag has been raised. When read as a zero, bit 2.33.4 indicates that the line alarm indication flag is lowered. The AIS-L bit shall be implemented with latching high behavior.

The AIS-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.8 LCD-P (2.33.3)

When read as a one, bit 2.33.3 indicates that the loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.3 indicates that the loss of code-group delineation flag is lowered. The LCD-P bit shall be implemented with latching high behavior.

The loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.9 PLM-P (2.33.2)

When read as a one, bit 2.33.2 indicates that the path label mismatch flag has been raised. When read as a zero, bit 2.33.2 indicates that the path label mismatch flag is lowered. The PLM-P bit shall be implemented with latching high behavior.

The PLM-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.10 AIS-P (2.33.1)

When read as a one, bit 2.33.1 indicates that the path alarm indication signal has been raised. When read as a zero, bit 2.33.1 indicates that the path alarm indication signal is lowered. The AIS-P bit shall be implemented with latching high behavior.

The path alarm indication signal functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.11 LOP-P (2.33.0)

When read as a one, bit 2.33.0 indicates that the loss of pointer flag has been raised. When read as a zero, bit 2.33.0 indicates that the loss of pointer flag is lowered. The LOP-P bit shall be implemented with latching high behavior.

The LOP-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.11 10G WIS far end path block error count (Register 2.37)

The assignment of bits in the 10G WIS far end path block error count register is shown in Table 45–60.

Table 45–60—10G WIS far end path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.37.15:0	Far end path block error count	Far end path block error count	RO

[a]RO = Read Only,

The 10G WIS far end path block error count is incremented by one whenever a far end path block error, defined in Annex 50A, is detected as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.12 10G WIS J1 transmit (Registers 2.39 through 2.46)

The assignment of octets in the 10G WIS J1 transmit registers is shown in Table 45–61.

Table 45–61—10G WIS J1 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.46.15:8	J1 transmit 15	Transmitted path trace octet 15	R/W
2.46.7:0	J1 transmit 14	Transmitted path trace octet 14	R/W
2.45.15:8	J1 transmit 13	Transmitted path trace octet 13	R/W
2.45.7:0	J1 transmit 12	Transmitted path trace octet 12	R/W
2.44.15:8	J1 transmit 11	Transmitted path trace octet 11	R/W
2.44.7:0	J1 transmit 10	Transmitted path trace octet 10	R/W
2.43.15:8	J1 transmit 9	Transmitted path trace octet 9	R/W
2.43.7:0	J1 transmit 8	Transmitted path trace octet 8	R/W
2.42.15:8	J1 transmit 7	Transmitted path trace octet 7	R/W
2.42.7:0	J1 transmit 6	Transmitted path trace octet 6	R/W
2.41.15:8	J1 transmit 5	Transmitted path trace octet 5	R/W
2.41.7:0	J1 transmit 4	Transmitted path trace octet 4	R/W
2.40.15:8	J1 transmit 3	Transmitted path trace octet 3	R/W
2.40.7:0	J1 transmit 2	Transmitted path trace octet 2	R/W
2.39.15:8	J1 transmit 1	Transmitted path trace octet 1	R/W
2.39.7:0	J1 transmit 0	Transmitted path trace octet 0	R/W

[a]R/W = Read/Write

The first transmitted path trace octet is J1 transmit 15, which contains the delineation octet. The default value for the J1 transmit 15 octet is 137 (hexadecimal 89). The last transmitted path trace octet is J1 transmit 0. The default value for the J1 transmit 0 through 14 octets is 0. The transmitted path trace is described in 50.3.2.1.

45.2.2.13 10G WIS J1 receive (Registers 2.47 through 2.54)

The assignment of octets in the 10G WIS J1 receive registers is shown in Table 45–62.

Table 45–62—10G WIS J1 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.54.15:8	J1 receive 15	Received path trace octet 15	RO
2.54.7:0	J1 receive 14	Received path trace octet 14	RO
2.53.15:8	J1 receive 13	Received path trace octet 13	RO
2.53.7:0	J1 receive 12	Received path trace octet 12	RO
2.52.15:8	J1 receive 11	Received path trace octet 11	RO
2.52.7:0	J1 receive 10	Received path trace octet 10	RO
2.51.15:8	J1 receive 9	Received path trace octet 9	RO
2.51.7:0	J1 receive 8	Received path trace octet 8	RO
2.50.15:8	J1 receive 7	Received path trace octet 7	RO
2.50.7:0	J1 receive 6	Received path trace octet 6	RO
2.49.15:8	J1 receive 5	Received path trace octet 5	RO
2.49.7:0	J1 receive 4	Received path trace octet 4	RO
2.48.15:8	J1 receive 3	Received path trace octet 3	RO
2.48.7:0	J1 receive 2	Received path trace octet 2	RO
2.47.15:8	J1 receive 1	Received path trace octet 1	RO
2.47.7:0	J1 receive 0	Received path trace octet 0	RO

[a]RO = Read Only

The first received path trace octet is J1 receive 15. The last received path trace octet is J1 receive 0. The received path trace is described in 50.3.2.4.

45.2.2.14 10G WIS far end line BIP errors (Registers 2.55 and 2.56)

The assignment of octets in the 10G WIS far end line BIP errors registers is shown in Table 45–63.

Table 45–63—10G WIS far end line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.56.15:0	WIS far end line BIP errors 0	Least significant word of the WIS far end line BIP errors counter	RO
2.55.15:0	WIS far end line BIP errors 1	Most significant word of the WIS far end line BIP errors counter	RO

[a]RO = Read Only

The 10G WIS far end line BIP Errors register pair reflects the contents of the far end line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of far end line BIP errors reported by the far end, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.55) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.55 and the least significant 16 bits appearing in 2.56, the value being latched before the contents of 2.55 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.56 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

NOTE—These counters do not follow the behaviour described in 45.2 for 32-bit counters.

45.2.2.15 10G WIS line BIP errors (Registers 2.57 and 2.58)

The assignment of octets in the 10G WIS line BIP errors registers is shown in Table 45–64.

Table 45–64—10G WIS line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.58.15:0	WIS line BIP errors 0	Least significant word of the WIS line BIP errors counter	RO
2.57.15:0	WIS line BIP errors 1	Most significant word of the WIS line BIP errors counter	RO

[a]RO = Read Only

The 10G WIS line BIP errors register pair reflects the contents of the line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of line BIP errors detected on the incoming data stream, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.57) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.57 and the least significant 16 bits appearing in 2.58, the value being latched before the contents of 2.57 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.58 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

NOTE—These counters do not follow the behaviour described in 45.2 for 32-bit counters.

45.2.2.16 10G WIS path block error count (Register 2.59)

The assignment of bits in the 10G WIS path block error count register is shown in Table 45–65.

Table 45–65—10G WIS path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.59.15:0	Path block error count	Path block error counter	RO

[a]RO = Read Only

45.2.2.16.1 Path block error count (2.59.15:0)

The path block error count is incremented by one whenever a B3 parity error (defined in Annex 50A) is detected, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.17 10G WIS section BIP error count (Register 2.60)

The assignment of bits in the 10G WIS section BIP error count register is shown in Table 45–66.

Table 45–66—10G WIS section BIP error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.60.15:0	Section BIP error count	Section BIP error count	RO

[a]RO = Read Only

45.2.2.17.1 Section BIP error count (2.60.15:0)

The section BIP error count is incremented by the number of section BIP errors detected within each WIS frame, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.18 10G WIS J0 transmit (Registers 2.64 through 2.71)

The assignment of octets in the 10G WIS J0 transmit registers is shown in Table 45–67.

Table 45–67—10G WIS J0 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.71.15:8	J0 transmit 15	Transmitted section trace octet 15	R/W
2.71.7:0	J0 transmit 14	Transmitted section trace octet 14	R/W
2.70.15:8	J0 transmit 13	Transmitted section trace octet 13	R/W
2.70.7:0	J0 transmit 12	Transmitted section trace octet 12	R/W
2.69.15:8	J0 transmit 11	Transmitted section trace octet 11	R/W
2.69.7:0	J0 transmit 10	Transmitted section trace octet 10	R/W
2.68.15:8	J0 transmit 9	Transmitted section trace octet 9	R/W
2.68.7:0	J0 transmit 8	Transmitted section trace octet 8	R/W
2.67.15:8	J0 transmit 7	Transmitted section trace octet 7	R/W
2.67.7:0	J0 transmit 6	Transmitted section trace octet 6	R/W
2.66.15:8	J0 transmit 5	Transmitted section trace octet 5	R/W
2.66.7:0	J0 transmit 4	Transmitted section trace octet 4	R/W
2.65.15:8	J0 transmit 3	Transmitted section trace octet 3	R/W
2.65.7:0	J0 transmit 2	Transmitted section trace octet 2	R/W
2.64.15:8	J0 transmit 1	Transmitted section trace octet 1	R/W
2.64.7:0	J0 transmit 0	Transmitted section trace octet 0	R/W

[a]R/W = Read/Write

The J0 transmit octets allow a receiver to verify its continued connection to the WIS transmitter. The first transmitted section trace octet is J0 transmit 15, which contains the delineation octet. The default value for the J0 transmit 15 octet is 137 (hexadecimal 89). The last transmitted section trace octet is J0 transmit 0. The default value for the J0 transmit 0 through 14 octets is 0. The transmitted section trace is described in 50.3.2.3.

45.2.2.19 10G WIS J0 receive (Registers 2.72 through 2.79)

The assignment of octets in the 10G WIS J0 receive registers is shown in Table 45–68.

The first received section trace octet is J0 receive 15. The last received section trace octet is J0 receive 0. The J0 receive octets allow a WIS receiver to verify its continued connection to the intended transmitter. The received section trace is described in 50.3.2.4.

Table 45–68— 10G WIS J0 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.79.15:8	J0 receive 15	Received section trace octet 15	RO
2.79.7:0	J0 receive 14	Received section trace octet 14	RO
2.78.15:8	J0 receive 13	Received section trace octet 13	RO
2.78.7:0	J0 receive 12	Received section trace octet 12	RO
2.77.15:8	J0 receive 11	Received section trace octet 11	RO
2.77.7:0	J0 receive 10	Received section trace octet 10	RO
2.76.15:8	J0 receive 9	Received section trace octet 9	RO
2.76.7:0	J0 receive 8	Received section trace octet 8	RO
2.75.15:8	J0 receive 7	Received section trace octet 7	RO
2.75.7:0	J0 receive 6	Received section trace octet 6	RO
2.74.15:8	J0 receive 5	Received section trace octet 5	RO
2.74.7:0	J0 receive 4	Received section trace octet 4	RO
2.73.15:8	J0 receive 3	Received section trace octet 3	RO
2.73.7:0	J0 receive 2	Received section trace octet 2	RO
2.72.15:8	J0 receive 1	Received section trace octet 1	RO
2.72.7:0	J0 receive 0	Received section trace octet 0	RO

[a]RO = Read Only

45.2.3 PCS registers

The assignment of registers in the PCS is shown in Table 45–69.

Table 45–69—PCS registers

Register address	Register name
3.0	PCS control 1
3.1	PCS status 1
3.2, 3.3	PCS device identifier
3.4	PCS speed ability
3.5, 3.6	PCS devices in package
3.7	10G PCS control 2
3.8	10G PCS status 2
3.9 through 3.13	Reserved
3.14, 3.15	PCS package identifier
3.16 through 3.23	Reserved
3.24	10GBASE-X PCS status
3.25	10GBASE-X PCS test control
3.26 through 3.31	Reserved
3.32	10GBASE-R PCS status 1
3.33	10GBASE-R PCS status 2
3.34 through 3.37	10GBASE-R PCS test pattern seed A
3.38 through 3.41	10GBASE-R PCS test pattern seed B
3.42	10GBASE-R PCS test pattern control
3.43	10GBASE-R PCS test pattern error counter
3.44 through 3.59	Reserved
3.60	10P/2B capability
3.61	10P/2B PCS control register
3.62, 3.63	10P/2B PME available
3.64, 3.65	10P/2B PME aggregate
3.66	10P/2B PAF RX error counter
3.67	10P/2B PAF small fragment counter
3.68	10P/2B PAF large fragments counter
3.69	10P/2B PAF overflow counter
3.70	10P/2B PAF bad fragment counter
3.71	10P/2B PAF lost fragment counter
3.72	10P/2B PAF lost start of fragment counter
3.73	10P/2B PAF lost end of fragment counter
3.74 through 3.79	Reserved
3.80	10GBASE-T PCS control
3.81	10GBASE-T PCS status 1
3.82	10GBASE-T PCS status 2

Table 45–69—PCS registers

Register address	Register name
3.83	10GBASE-T PRBS31 error counter
3.84 through 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

Change table 45-71 by changing "3.74 through 3.32 767" to "3.74 through 3.79". Insert new rows and associated information for 3.80, 3.81, 3.82, and 3.83. Insert new row for "3.84 through 3.32 767".

45.2.3.1 PCS control 1 register (Register 3.0)

The assignment of bits in the PCS control 1 register is shown in Table 45–70. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–70—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
3.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.12	Reserved	Value always 0, writes ignored	R/W
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10:7	Reserved	Value always 0, writes ignored	R/W
3.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.3.1.1 Reset (3.0.15)

Resetting a PCS is accomplished by setting bit 3.0.15 to a one. This action shall set all PCS registers to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PCS shall return a value of one in bit 3.0.15 when a reset is in progress and a value of zero otherwise. A PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 3.0.15. During a reset, a PCS shall respond to reads from register bits 3.0.15 and 3.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.3.1.2 Loopback (3.0.14)

change paragraph to include 10GBASE-T in loopback function.

When 10GBASE-T or ~~The~~ 10GBASE-R mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), the PCS shall be placed in a Loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the ~~10GBASE-R~~ PCS shall accept data on the transmit path and return it on the receive path. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. The specific behavior for the 10GBASE-T PCS during loopback is specified in TBD (55.2). For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

The default value of bit 3.0.14 is zero.

NOTE—The signal path through the PCS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PCS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.3.1.3 Low power (3.0.11)

A PCS may be placed into a low-power mode by setting bit 3.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PCS. The behavior of the PCS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 3.0.11 is zero.

45.2.3.1.4 Speed selection (3.0.13, 3.0.6, 3.0.5:2)

Speed selection bits 3.0.13 and 3.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PCS may be selected using bits 5 through 2. The speed abilities of the PCS are advertised in the PCS speed ability register. A PCS may ignore writes to the PCS speed selection bits that select speeds it has not advertised in the PCS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PCS speed selection defaults to a supported ability.

The speed selection bits 3.0.5:2, when set to 0001, select the use of the 10PASS-TS and 2BASE-TL PCS.

45.2.3.2 PCS status 1 register (Register 3.1)

The assignment of bits in the PCS status 1 register is shown in Table 45–71. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

45.2.3.2.1 Fault (3.1.7)

When read as a one, bit 3.1.7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the PCS has not detected a fault condition. For 10 Gb/s operation, bit 3.1.7 is read as a one when either of the fault bits (3.8.11, 3.8.10) located in register

Table 45–71—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:8	Reserved	Ignore when read	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6:3	Reserved	Ignore when read	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

3.8 are read as a one. For 10BASE-TS or 2BASE-TL operation, this bit shall become a one when any 10P/2B PCS registers indicate a fault (see 45.2.3.17 and 45.2.3.21 through 45.2.4.5).

45.2.3.2.2 PCS receive link status (3.1.2)

add description for 10GBASE-T.

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10GBASE-R or 10GBASE-W mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.24.12. When a 10GBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.80.12. The receive link status bit shall be implemented with latching low behavior.

45.2.3.2.3 Low-power ability (3.1.1)

When read as a one, bit 3.1.1 indicates that the PCS supports the low-power feature. When read as a zero, bit 3.1.1 indicates that the PCS does not support the low-power feature. If a PCS supports the low-power feature then it is controlled using the low-power bit 3.0.11.

45.2.3.3 PCS device identifier (Registers 3.2 and 3.3)

Registers 3.2 and 3.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PCS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS device identifier.

The format of the PCS device identifier is specified in 22.2.4.3.1.

45.2.3.4 PCS speed ability (Register 3.4)

The assignment of bits in the PCS speed ability register is shown in Table 45–72.

Table 45–72—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
3.4.1	10PASS-TS/2BASE-TL capable	1 = PCS is capable of operating as the 10P/2B PCS 0 = PCS is not capable of operating as the 10P/2B PCS	RO
3.4.0	10G capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.3.4.1 10G capable (3.4.0)

When read as a one, bit 3.4.0 indicates that the PCS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 3.4.0 indicates that the PCS is not able to operate at a data rate of 10 Gb/s.

45.2.3.4.2 10PASS-TS/2BASE-TL capable

When read as a one, this bit indicates that the PCS is able to operate as the 10PASS-TS/2BASE-TL PCS, as specified in Clause 61.

45.2.3.5 PCS devices in package (Registers 3.5 and 3.6)

The PCS devices in package registers are defined in Table 45–2.

45.2.3.6 10G PCS control 2 register (Register 3.7)

The assignment of bits in the 10G PCS control 2 register is shown in Table 45–73. The default value for each bit of the 10G PCS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–73—10G PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:2	Reserved	Value always 0, writes ignored	R/W
3.7.1:0	PCS type selection	1 0 1 1 = Select 10GBASE-T PCS type~~Reserved~~ 1 0 = Select 10GBASE-W PCS type 0 1 = Select 10GBASE-X PCS type 0 0 = Select 10GBASE-R PCS type	R/W

[a]R/W = Read/Write

Change table 45-75 by deleting reserved and adding 10GBASE-T

45.2.3.6.1 PCS type selection (3.7.1:0)

Change section 45.2.3.6.1 by replacing "2" with "3". Change table 45-76 by add 3.8.3 and associated text inlcuding changing number in previous row.

The PCS type shall be selected using bits 1 through 0. The PCS type abilities of the 10G PCS are advertised in bits 3.8.~~2~~3:0. A 10G PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.7 10G PCS status 2 register (Register 3.8)

The assignment of bits in the 10G PCS status 2 register is shown in Table 45–74. All the bits in the 10G PCS status 2 register are read only; a write to the 10G PCS status 2 register shall have no effect.

Table 45–74—10G PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
3.8.13:12	Reserved	Ignore when read	RO
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO/LH
3.8.9:~~3~~4	Reserved	Ignore when read	RO
3.8.3	10GBASE-T capable	1 = PCS is able to support 10GBASE-T PCS type 0 = PCS is not able to support 10GBASE-T PCS type	RO
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO

[a]RO = Read Only, LH = Latching High

45.2.3.7.1 Device present (3.8.15:14)

When read as <10>, bits 3.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 3.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.3.7.2 Transmit fault (3.8.11)

When read as a one, bit 3.8.11 indicates that the PCS has detected a fault condition on the transmit path. When read as a zero, bit 3.8.11 indicates that the PCS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.11 is zero.

45.2.3.7.3 Receive fault (3.8.10)

When read as a one, bit 3.8.10 indicates that the PCS has detected a fault condition on the receive path. When read as a zero, bit 3.8.10 indicates that the PCS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.10 is zero.

Add definition for bit 3.8.3

45.2.3.7.4 10GBASE-T capable (3.8.3)

When read as a one, bit 3.8.3 indicates that the PCS is able to support the 10GBASE-T PCS type. When read as a zero, bit 3.8.3 indicates that the PCS is not able to support the 10GBASE-T PCS type

45.2.3.7.5 10GBASE-W capable (3.8.2)

When read as a one, bit 3.8.2 indicates that the 64B/66B PCS is able to support operation in a 10GBASE-W PHY (that is, supports operation with a WIS). When read as a zero, bit 3.8.2 indicates that the 64B/66B PCS is not able to support operation with a WIS in a 10GBASE-W PHY.

NOTE—This bit does not indicate that the PCS is performing the functionality contained in the WIS. This bit indicates whether the 64B/66B PCS would be able to support a WIS if it were to be attached.

45.2.3.7.6 10GBASE-X capable (3.8.1)

When read as a one, bit 3.8.1 indicates that the PCS is able to support the 10GBASE-X PCS type. When read as a zero, bit 3.8.1 indicates that the PCS is not able to support the 10GBASE-X PCS type.

45.2.3.7.7 10GBASE-R capable (3.8.0)

When read as a one, bit 3.8.0 indicates that the PCS is able to support operation in a 10GBASE-R PHY. When read as a zero, bit 3.8.0 indicates that the PCS is not able to support operation in a 10GBASE-R PHY.

45.2.3.8 PCS package identifier (Registers 3.14 and 3.15)

Registers 3.14 and 3.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PCS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.3.9 10GBASE-X PCS status register (Register 3.24)

The assignment of bits in the 10GBASE-X PCS status register is shown in Table 45–75. All the bits in the 10GBASE-X PCS status register are read only; a write to the 10GBASE-X PCS status register shall have no effect. A PCS device that does not implement 10GBASE-X shall return a zero for all bits in the 10GBASE-X PCS status register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–75—10GBASE-X PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.24.15:13	Reserved	Ignore when read	RO
3.24.12	10GBASE-X lane alignment status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO
3.24.11	Pattern testing ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO
3.24.10:4	Reserved	Ignore when read	RO
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.3.9.1 10GBASE-X receive lane alignment status (3.24.12)

When read as a one, bit 3.24.12 indicates that the 10GBASE-X PCS has synchronized and aligned all four receive lanes. When read as a zero, bit 3.24.12 indicates that the 10GBASE-X PCS has not synchronized and aligned all four receive lanes.

45.2.3.9.2 Pattern testing ability (3.24.11)

When read as a one, bit 3.24.11 indicates that the 10GBASE-X PCS is able to generate test patterns. When read as a zero, bit 3.24.11 indicates that the 10GBASE-X PCS is not able to generate test patterns. If the 10GBASE-X PCS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 3.25.

45.2.3.9.3 Lane 3 sync (3.24.3)

When read as a one, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is synchronized. When read as a zero, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is not synchronized.

45.2.3.9.4 Lane 2 sync (3.24.2)

When read as a one, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is synchronized. When read as a zero, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is not synchronized.

45.2.3.9.5 Lane 1 sync (3.24.1)

When read as a one, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is synchronized. When read as a zero, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is not synchronized.

45.2.3.9.6 Lane 0 sync (3.24.0)

When read as a one, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is synchronized. When read as a zero, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is not synchronized.

45.2.3.10 10GBASE-X PCS test control register (Register 3.25)

The assignment of bits in the 10GBASE-X PCS test control register is shown in Table 45–76. The default value for each bit of the 10GBASE-X PCS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–76—10GBASE-X PCS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.25.15:3	Reserved	Value always 0, writes ignored	R/W
3.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
3.25.1:0	Test pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.3.10.1 Transmit test-pattern enable (3.25.2)

When bit 3.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 3.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10GBASE-X PCS to generate test patterns is advertised by the pattern testing ability bit in register 3.24. A 10GBASE-X PCS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 3.25.2 is zero.

45.2.3.10.2 Test pattern select (3.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 3.25.2 is selected using bits 3.25.1:0. When bits 3.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.3.11 10GBASE-R PCS status 1 register (Register 3.32)

The assignment of bits in the 10GBASE-R PCS status 1 register is shown in Table 45–77. All the bits in the 10GBASE-R PCS status 1 register are read only; a write to the 10GBASE-R PCS status 1 register shall have no effect. A PCS device that does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.32 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

Table 45–77—10GBASE-R PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.32.15:13	Reserved	Ignore when read	RO
3.32.12	10GBASE-R receive link status	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
3.32.11:3	Reserved	Ignore when read	RO
3.32.2	PRBS31 pattern testing ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO
3.32.1	10GBASE-R PCS high BER	1 = 10GBASE-R PCS reporting a high BER 0 = 10GBASE-R PCS not reporting a high BER	RO
3.32.0	10GBASE-R PCS block lock	1 = 10GBASE-R PCS locked to received blocks 0 = 10GBASE-R PCS not locked to received blocks	RO

[a]RO = Read Only

45.2.3.11.1 10GBASE-R receive link status (3.32.12)

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the state of the PCS_status variable defined in 49.2.14.1.

45.2.3.11.2 PRBS31 pattern testing ability (3.32.2)

When read as a one, bit 3.32.2 indicates that the PCS is able to support PRBS31 pattern testing. When read as a zero, bit 3.32.2 indicates that the PCS is not able to support PRBS31 pattern testing. If the PCS is able to support PRBS31 pattern testing then the pattern generation and checking is controlled using bits 3.42.5:4.

45.2.3.11.3 10GBASE-R PCS high BER (3.32.1)

When read as a one, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_ber variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

45.2.3.11.4 10GBASE-R PCS block lock (3.32.0)

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver has not got block lock. This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

45.2.3.12 10GBASE-R PCS status 2 register (Register 3.33)

The assignment of bits in the 10GBASE-R PCS status 2 register is shown in Table 45–78. All the bits in the 10GBASE-R PCS status 2 register are read only; a write to the 10GBASE-R PCS status 2 register shall have no effect. A PCS device which does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.33 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

Table 45–78—10GBASE-R PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.33.15	Latched block lock	1 = 10GBASE-R PCS has block lock 0 = 10GBASE-R PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = 10GBASE-R PCS has reported a high BER 0 = 10GBASE-R PCS has not reported a high BER	RO/LH
3.33.13:8	BER	BER counter	RO/NR
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR

[a]RO = Read Only, LL = Latching Low, LH = Latching High, NR = Non Roll-over

45.2.3.12.1 Latched block lock (3.33.15)

When read as a one, bit 3.33.15 indicates that the 10GBASE-R PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 10GBASE-R PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10GBASE-R PCS block lock status bit (3.32.0).

45.2.3.12.2 Latched high BER (3.33.14)

When read as a one, bit 3.33.14 indicates that the 10GBASE-R PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 10GBASE-R PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 10GBASE-R PCS high BER status bit (3.32.1).

45.2.3.12.3 BER(3.33.13:8)

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2. These bits shall be reset to all zeros when the BER count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.12.4 Errored blocks (3.33.7:0)

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.13 10GBASE-R PCS test pattern seed A (Registers 3.34 through 3.37)

The assignment of bits in the 10GBASE-R PCS test pattern seed A registers is shown in Table 45–79. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

Table 45–79—10GBASE-R PCS test pattern seed A 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.37.15:10	Reserved	Value always 0, writes ignored	R/W
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48-57	R/W
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32-47	R/W
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16-31	R/W
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0-15	R/W

[a]R/W = Read/Write

The A seed for the pseudo random test pattern is held in registers 3.34 through 3.37. The test-pattern methodology is described in 49.2.8.

45.2.3.14 10GBASE-R PCS test pattern seed B (Registers 3.38 through 3.41)

The assignment of bits in the 10GBASE-R PCS test pattern seed B registers is shown in Table 45–80. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

The B seed for the pseudo random test pattern is held in registers 3.38 through 3.41. The test-pattern methodology is described in 49.2.8.

Table 45–80—10GBASE-R PCS test pattern seed B 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.41.15:10	Reserved	Value always 0, writes ignored	R/W
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48-57	R/W
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32-47	R/W
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16-31	R/W
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0-15	R/W

[a]R/W = Read/Write

45.2.3.15 10GBASE-R PCS test-pattern control register (Register 3.42)

The assignment of bits in the 10GBASE-R PCS test-pattern control register is shown in Table 45–81. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. The test-pattern methodology is described in 49.2.8.

Table 45–81—10GBASE-R PCS test-pattern control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.42.15:6	Reserved	Value always 0, writes ignored	R/W
3.42.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
3.42.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
3.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
3.42.2	Receive test-pattern enable	1 = Enable receive test-pattern testing 0 = Disable receive test-pattern testing	R/W
3.42.1	Test-pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	R/W
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	R/W

[a]R/W = Read/Write

45.2.3.15.1 PRBS31 receive test-pattern enable (3.42.5)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory receive test-pattern enable bit (3.42.2) is not one, setting bit 3.42.5 to a one shall set the receive path of the PCS into

the PRBS31 test-pattern mode. The number of errors received during a PRBS31 pattern test are recorded in register 3.43. Setting bit 3.42.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

45.2.3.15.2 PRBS31 transmit test-pattern enable (3.42.4)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory transmit test-pattern enable bit (3.42.3) is not one, then setting bit 3.42.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode. Setting bit 3.42.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

45.2.3.15.3 Transmit test-pattern enable (3.42.3)

When bit 3.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 3.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 3.42.3 is zero.

45.2.3.15.4 Receive test-pattern enable (3.42.2)

When bit 3.42.2 is set to a one, pattern testing is enabled on the receive path. When bit 3.42.2 is set to a zero, pattern testing is disabled on the receive path.

The default value for bit 3.42.2 is zero.

45.2.3.15.5 Test-pattern select (3.42.1)

When bit 3.42.1 is set to a one, the square wave test pattern is used for pattern testing. When bit 3.42.1 is set to a zero, the pseudo random test pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

45.2.3.15.6 Data pattern select (3.42.0)

When bit 3.42.0 is set to a one, the zeros data pattern is used for pattern testing. When bit 3.42.0 is set to a zero, the LF data pattern is used for pattern testing.

The default value for bit 3.42.0 is zero.

45.2.3.16 10GBASE-R PCS test-pattern error counter register (Register 3.43)

The assignment of bits in the 10GBASE-R PCS test-pattern error counter register is shown in Table 45–82. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode, or may function as defined for 10GBASE-R.

Table 45–82—10GBASE-R PCS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.43.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read Only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.12. This counter will count either block errors or bit errors dependent on the test mode (see 49.2.12).

45.2.3.17 10P/2B capability register (3.60)

The 10P/2B capability register reports which functions are supported by the PCS. This register is present at the PCS layer for each PHY. The bit definitions of the 10P/2B capability register are shown in Table 45–83.

Table 45–83—10P/2B capability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.60.15:13	Reserved	Value always 0, writes ignored	RO
3.60.12	PAF available	1 = PAF supported 0 = PAF not supported	RO
3.60.11	Remote PAF supported	1 = link partner supports PAF 0 = link partner does not support PAF	RO
3.60.10:0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read Only

45.2.3.17.1 PAF available (3.60.12)

This bit indicates that the PHY supports the PME aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit reflects the signal PAF_available in 61.2.3.

45.2.3.17.2 Remote PAF supported (3.60.11)

This bit indicates that the remote, link-partner PHY supports the PME aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit does not accurately report the capability of the remote PCS until a remote discovery operation has been completed by the -O PHY. In this case, this bit is set if the “Ethernet bonding” NPar(2) bit is set in the capabilities exchange message received from the other device. See 61.4.7, which discusses use of G.994.1 to access remote registers.

45.2.3.18 10P/2B PCS control register (Register 3.61)

The assignment of bits in the 10P/2B PCS control register is shown in Table 45–84.

45.2.3.18.1 MII receive during transmit (3.61.15)

This register bit is used to tell the PHY-MAC rate matching function if the MAC is capable of receiving frames from the PHY while the MAC is transmitting (i.e. sending frames to the PHY). The variable tx_rx_simultaneously for the PHY-MAC Rate-Matching function takes on the value of this bit as defined in 61.2.3.

Table 45–84—10B/2B PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.61.15	MII receive during transmit	1 = MII can TX/RX simultaneously 0 = MII cannot TX/RX simultaneously (default)	R/W
3.61.14	TX_EN and CRS infer a collision	1 = MII uses TX_EN and CRS to infer a collision 0 = MII uses COL to indicate a collision (default)	R/W
3.61.13:1	Reserved	Value always 0, writes ignored	R/W
3.61.0	PAF enable	1 = use PAF 0 = do not use PAF	O: R/W R: RO

[a]R/W = Read/Write, RO = Read Only

45.2.3.18.2 TX_EN and CRS infer a collision (3.61.14)

This bit is set by the STA to tell the MAC-PHY rate matching function that the MAC-PHY interface does not have a separate collision signal but instead infers a collision when TX_EN and CRS are asserted simultaneously. The variable crs_and_tx_en_infer_col in the PHY-MAC Rate-Matching function takes on the value of this bit as in 61.2.3. This bit will default to a supported mode, and writes to unsupported modes will be ignored.

45.2.3.18.3 PAF enable (3.61.0)

Setting this bit to a one shall activate the PME aggregation function of the PCS when the link is established. Writes to this bit while link is up or initializing (see 45.2.1.12) or if the PAF is not supported shall be ignored. When link is established, handshake indicates the use of PAF to the -R PHY. This bit reflects the signal PAF_enable in 61.2.3.4.

45.2.3.19 10P/2B PME available (Registers 3.62 and 3.63)

The 10P/2B PME available registers are used to indicate which PMEs in the aggregation group are available to be attached to the queried PCS. A PME is marked as unavailable if the PME does not support PME aggregation or if the PME is currently marked to be aggregated with another PMD. For a device that does not support aggregation of multiple PMEs, a single bit of this register shall be set to one and all other bits cleared to zero.

These registers may be writable for -R ports. For PMEs that may be accessed through more than one MII, the availability is limited such that no PME may be mapped to more than one MII prior to enabling the links. In this case, the reset state of the 10P/2B PME available registers shall reflect the capabilities of the device, the management entity should reset appropriate bits to meet the restriction described.

If the -R device is not capable of aggregating PMEs to multiple MIIs then these registers may be read only.

The 10P/2B PME available register shall be available per PCS. For example, a package implementing four PMEs and one MII would have only one set of 10P/2B PME available registers, addressed by a read or write to 3.62 and 3.63 on any of those PHYs.

For more information, see 61.2.2.8.3.

The assignment of bits in the 10P/2B PME Available registers is shown in Table 45–85

Table 45–85—10P/2B PME available register bit definitions

Bit(s)	Name	Description	R/W[a]
3.62.15:0	PME [p = 31:16] available	For each bit in the sequence: 1 = PME[p] is available for aggregating 0 = PME[p] is unavailable	O: RO R: R/W
3.63.15:0	PME [p = 15:0] available	For each bit in the sequence: 1 = PME[p] is available for aggregating 0 = PME[p] is unavailable	O: RO R: R/W

[a]RO = Read Only, R/W = Read/Write

45.2.3.20 10P/2B PME aggregate registers (Registers 3.64 and 3.65)

The 10P/2B PME aggregate registers are used to select PMEs for aggregation. Attempts to activate aggregation with an unavailable PME (see 45.2.3.19) are ignored. The PCS shall use PME aggregation if one or more bits are set to a one and if PME aggregation is supported.

The 10P/2B PME aggregate register shall be available per PCS. For example, a package implementing four PMEs and one MII would have only one set of 10P/2B PME aggregate registers, accessed by a read or write to 3.64, 3.65 on any of those PHYs.

Upon MMD reset, these registers shall be reset to all zeros.

For more information, see 61.2.2.8.3.

The assignment of bits for the 10P/2B PME aggregate registers are shown in Table 45–86**.**

Table 45–86—10P/2B PME aggregate register bit definitions

Bit(s)	Name	Description	R/W[a]
3.64.15:0	Aggregate with PME [p = 31:16]	For each bit in the sequence: 1 = activate aggregation with PME[p] 0 = deactivate aggregation with PME[p]	R/W
3.65.15:0	Aggregate with PME [p = 15:0]	For each bit in the sequence: 1 = activate aggregation with PME[p] 0 = deactivate aggregation with PME[p]	R/W

[a]R/W = Read/Write

45.2.3.21 10P/2B PAF RX error register (Register 3.66)

The 10P/2B PAF RX error register is a 16 bit counter that contains the number of fragments that have been received across the gamma interface with RxErr asserted. The corresponding signal, TC_PAF_RxErrorReceived, is defined in 61.2.3. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be reset to all zeroes when the 10P/2B PAF RX error register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF RX error register is shown in Table 45–87.

Table 45–87—10P/2B PAF RX error register bit definitions

Bits(s)	Name	Description	R/W[a]
3.66.15:0	PAF RX errors[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.22 10P/2B PAF small fragments register (Register 3.67)

The 10P/2B PAF small fragments register is a 16 bit counter that contains the number of small fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_FragmentTooSmall, is defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF small fragment register is shown in Table 45–88.

Table 45–88—10P/2B PAF small fragments register bit definitions

Bits(s)	Name	Description	R/W[a]
3.67.15:0	PAF small fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.23 10P/2B PAF large fragments register (Register 3.68)

The 10P/2B PAF large fragments register is a 16 bit counter that contains the number of large fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_FragmentTooLarge, is defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF large fragments register is shown in Table 45–89.

Table 45–89—10P/2B PAF large fragments register bit definitions

Bits(s)	Name	Description	R/W[a]
3.68.15:0	PAF large fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.24 10P/2B PAF overflow register (Register 3.69)

The 10P/2B PAF overflow register is a 16 bit counter that contains the number of fragments that have been received across the gamma interface which would have caused the receive buffer to overflow. The corresponding signal, TC_PAF_Overflow, is defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF overflow register is shown in Table 45–90.

Table 45–90—10P/2B PAF overflow register bit definitions

Bits(s)	Name	Description	R/W[a]
3.69.15:0	PAF overflow fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.25 10P/2B PAF bad fragment register (Register 3.70)

The 10P/2B PAF bad fragment register is a 16 bit counter that contains the number of bad fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_BadFragmentReceived, is defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF bad fragment register is shown in Table 45–91.

Table 45–91—P10P/2B AF bad fragment register bit definitions

Bits(s)	Name	Description	R/W[a]
3.70.15:0	PAF bad fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.26 10P/2B PAF lost fragment register (Register 3.71)

The 10P/2B PAF lost fragment register is a 16 bit counter that contains the number of gaps in the sequence of fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_LostFragment, is defined in 61.2.3.

These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost fragment register is shown in Table 45–92.

Table 45–92—10P/2B PAF lost fragment register bit definitions

Bits(s)	Name	Description	R/W[a]
3.71.15:0	PAF lost fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.27 10P/2B PAF lost start of fragment register (Register 3.72)

The 10P/2B PAF lost start of fragment register is a 16-bit counter that contains the number of missing start of fragment indicators expected by the frame assembly function. The corresponding signal, TC_PAF_LostStart, is defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost start of fragment register is shown in Table 45–93.

Table 45–93—10P/2B PAF lost start of fragment register bit definitions

Bits(s)	Name	Description	R/W[a]
3.72.15:0	PAF lost starts of fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.3.28 10P/2B PAF lost end of fragment register (Register 3.73)

The 10P/2B PAF lost end of fragment register is a 16 bit counter that contains the number of missing end of fragment indicators expected by the frame assembly function. The corresponding signal, TC_PAF_LostEnd, is defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost end of fragment register is shown in Table 45–94.

Table 45–94—10P/2B PAF lost end of fragment register bit definitions

Bits(s)	Name	Description	R/W[a]
3.73.15:0	PAF lost ends of fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

Add registers and bit definitations for 3.80 through 3.83

45.2.3.29 10GBASE-T PCS control register (Register 3.80)

The assignment of bits in the 10GBASE-T PCS control register is shown in Table 45–95. The test-pattern methodology is described in TBD (55.3.??).

45.2.3.29.1 PRBS31 Receive test-pattern enable (3.80.5)

Editors Comment: Test-pattern modes and capability have yet to be clearly defined. Removal, change and addition of additional test modes and potentially corresponding counter registers will be determine based on comment.

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.81.2 then setting bit 3.80.5 to a one shall set the receive path of the PCS into the PRBS31 test-pattern mode. The number of errors received during a PRBS31 pattern test are recorded in register 3.83. Setting bit 3.80.5 to a zero shall disable the

Table 45–95—10GBASE-T PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.15:6	Reserved	Value always 0, writes ignored	R/W
3.80.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
3.80.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
3.80.3:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write

PRBS31 test-pattern mode on the receive path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause TBD (55.3.??).

45.2.3.29.2 PRBS31 transmit test-pattern enable (3.80.4)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.81.2 then setting bit 3.80.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode. Setting bit 3.80.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause TBD (55.3.??)

45.2.3.30 10GBASE-T PCS status 1 register (Register 3.81)

Editors Comment: Test-pattern modes and capability have yet to be clearly defined. Removal, change and addition of additional test modes and potentially corresponding counter registers will be determine based on comments.

The assignment of bits in the 10GBASE-T PCS status 1 register is shown in Table 45–96. All the bits in the 10GBASE-T PCS status 1 register are read only; a write to the 10GBASE-R PCS status 1 register shall have no effect. A PCS device that does not implement 10GBASE-T shall return a zero for all bits in the 10GBASE-T PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.81 are undefined when the 10GBASE-T PCS is operating in PRBS31 test-pattern mode.

45.2.3.30.1 10GBASE-T receive link status (3.81.12)

When read as a one, bit 3.81.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.81.12 indicates that the PCS is not fully operational. This bit is a reflection of the state of the PCS_Status variable defined in TBD (55.3.13.1).

45.2.3.30.2 PRBS31 pattern testing ability (3.81.2)

When read as a one, bit 3.81.2 indicates that the PCS is able to support PRBS31 pattern testing. When read as a zero, bit 3.81.2 indicates that the PCS is not able to support PRBS31 pattern testing. If the PCS is able to support PRBS31 pattern testing then the pattern generation and checking is controlled using bits TBD.

Editors Comment: Test-pattern modes and capability have yet to be clearly defined. Removal, change and addition of additional test modes and potentially corresponding counter registers will be determine based on comments.

Table 45–96—10GBASE-T PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.81.15:13	Reserved	Ignore when read	RO
3.81.12	10GBASE-T receive link status	1 = 10GBASE-T PCS receive link up 0 = 10GBASE-T PCS receive link down	RO
3.81.11:4	Reserved	Ignore when read	RO
3.81.2	PRBS31 ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO
3.81.1	10GBASE-T PCS high BER status	1 = 10GBASE-T PCS reporting a high BER 0 = 10GBASE-T PCS not reporting a high BER	RO
3.81.0	10GBASE-T PCS lock status	1 = 10GBASE-T PCS locked to received blocks 0 = 10GBASE-T PCS not locked to received blocks	RO

[a]RO = Read Only

45.2.3.30.3 10GBASE-T PCS high BER status (3.81.1)

When read as a one, bit 3.81.1 indicates that the 64B/65B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.81.1 indicates that the 64B/65B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_lber variable in the 64B/65B state machine and is defined in TBD (55.3.13.1).

45.2.3.30.4 10GBASE-T PCS lock status (3.81.0)

PCS lock status is the logical AND of the sync_status variable in the LDPC state machine, defined in TBD (55.3.2), and the block_lock variable in the 64B/65B state machine, defined in TBD (55.3.13.1). When read as a one, bit 3.81.0 indicates that the PCS receiver has lock. When read as a zero, bit 3.81.0 indicates that the receiver does not have lock.

45.2.3.31 10GBASE-T PCS status 2 register (Register 3.82)

The assignment of bits in the 10GBASE-T PCS status 2 register is shown in Table 45–97. All the bits in the 10GBASE-T PCS status 2 register are read only; a write to the 10GBASE-T PCS status 2 register shall have no effect. A PCS device which does not implement 10GBASE-T shall return a zero for all bits in the 10GBASE-T PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port

type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.82 are undefined when the 10GBASE-T PCS is operating in PRBS31 test-pattern mode.

Table 45–97—10GBASE-T PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15	PCS lock	1 = 10GBASE-T PCS has lock 0 = 10GBASE-T PCS does not have lock	RO/LL
3.82.14	High BER	1 = 10GBASE-T PCS has reported a high BER 0 = 10GBASE-T PCS has not reported a high BER	RO/LH
3.82.13:8	BER counter	BER counter	RO/NR
3.82.7:0	Errored blocks	Errored blocks counter	RO/NR

[a]RO = Read Only, LL = Latching Low, LH = Latching High, NR = Non Roll-over

45.2.3.31.1 PCS lock (3.82.15)

When read as a one, bit 3.82.15 indicates that the 10GBASE-T PCS has maintained PCS lock since the last read of the the 10GBASE-T PCS status 2 register. When read as a zero, bit 3.82.15 indicates that the 10GBASE-T PCS has lost PCS lock. This bit is a latching low version of the 10GBASE-T PCS lock status bit (3.81.0). The PCS lock bit will be reset to logic high upon read of the 10GBASE-T PCS status 2 register.

45.2.3.31.2 High BER (3.82.14)

When read as a one, bit 3.82.14 indicates that the 10GBASE-T PCS has detected a high BER. When read as a zero, bit 3.82.14 indicates that the 10GBASE-T PCS has not detected a high BER. This bit is a latching high version of the 10GBASE-R PCS high BER status bit (3.81.1). The High BER bit will be reset to logic low upon read of the 10GBASE-T PCS status 2 register

45.2.3.31.3 BER counter (3.82.13:8)

Editors Note: The resolution of the BER counter is still TBD. The size here will be adjusted accordingly.

The BER counter is a six bit count as defined by the lber_count variable in TBD (55.3.13.2). These bits shall be reset to all zeros when the BER count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.31.4 Errored blocks (3.82.7:0)

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in TBD (55.3.13.2). These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.32 10GBASE-T PCS PRBS31 error counter register (Register 3.83)

Editors Comment: Test-pattern modes and capability have yet to be clearly defined. Removal, change and addition of additional test modes and potentially corresponding counter registers will be determine based on comment.

The assignment of bits in the 10GBASE-T PCS PRBS31 error counter register is shown in Table 45–98.

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in TBD (55.3.??).

Table 45–98—10GBASE-T PCS PRBS31 error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.83.15:0	PRBS31 error counter	Error counter	RO

[a]RO = Read Only

45.2.4 PHY XS registers

The assignment of registers in the PHY XS is shown in Table 45–99.

Table 45–99—PHY XS registers

Register address	Register name
4.0	PHY XS control 1
4.1	PHY XS status 1
4.2, 4.3	PHY XS device identifier
4.4	PHY XS speed ability
4.5, 4.6	PHY XS devices in package
4.7	Reserved
4.8	PHY XS status 2
4.9 through 4.13	Reserved
4.14, 4.15	PHY XS package identifier
4.16 through 4.23	Reserved
4.24	10G PHY XGXS lane status
4.25	10G PHY XGXS test control
4.26 through 4.32 767	Reserved
4.32 768 through 4.65 535	Vendor specific

45.2.4.1 PHY XS control 1 register (Register 4.0)

The assignment of bits in the PHY XS control 1 register is shown in Table 45–100. The default value for each bit of the PHY XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–100—PHY XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.0.15	Reset	1 = PHY XS reset 0 = Normal operation	R/W SC
4.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
4.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.12	Reserved	Value always 0, writes ignored	R/W
4.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
4.0.10:7	Reserved	Value always 0, writes ignored	R/W
4.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
4.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.4.1.1 Reset (4.0.15)

Resetting a PHY XS is accomplished by setting bit 4.0.15 to a one. This action shall set all PHY XS registers to their default states. As a consequence, this action may change the internal state of the PHY XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PHY XS shall return a value of one in bit 4.0.15 when a reset is in progress and a value of zero otherwise. A PHY XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 4.0.15. During a reset, a PHY XS shall respond to reads from register bits 4.0.15 and 4.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.4.1.2 Loopback (4.0.14)

The PHY XS shall be placed in a Loopback mode of operation when bit 4.0.14 is set to a one. When bit 4.0.14 is set to a one, the PHY XS shall accept data on the receive path and return it on the transmit path. The direction of the loopback path for the PHY XS is opposite to all other MMD loopbacks.

The loopback function is optional. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PHY XS that is unable to perform the loopback function shall ignore writes to this bit and return a value of zero when read. For 10 Gb/s operation,

the loopback functionality is detailed in 48.3.3 and the loopback ability bit is specified in the 10G PHY XGXS Lane status register.

The default value of bit 4.0.14 is zero.

NOTE—The signal path through the PHY XS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY XS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.4.1.3 Low power (4.0.11)

A PHY XS may be placed into a low-power mode by setting bit 4.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PHY XS. The behavior of the PHY XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 4.0.11 is zero.

45.2.4.1.4 Speed selection (4.0.13, 4.0.6, 4.0.5:2)

Speed selection bits 4.0.13 and 4.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PHY XS may be selected using bits 5 through 2. The speed abilities of the PHY XS are advertised in the PHY XS speed ability register. A PHY XS may ignore writes to the PHY XS speed selection bits that select speeds it has not advertised in the PHY XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PHY XS speed selection defaults to a supported ability.

45.2.4.2 PHY XS status 1 register (Register 4.1)

The assignment of bits in the PHY XS status 1 register is shown in Table 45–101. All the bits in the PHY XS status 1 register are read only; a write to the PHY XS status 1 register shall have no effect.

45.2.4.2.1 Fault (4.1.7)

When read as a one, bit 4.1.7 indicates that the PHY XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 4.1.7 indicates that the PHY XS has not detected a fault condition. Bit 4.1.7 is set to a one when either of the fault bits (4.8.11, 4.8.10) located in register 4.8 are set to a one.

45.2.4.2.2 PHY XS transmit link status (4.1.2)

When read as a one, bit 4.1.2 indicates that the PHY XS transmit link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS transmit link is not aligned. The transmit link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, bit 4.1.2 is a latching low version of bit 4.24.12.

Table 45–101—PHY XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.1.15:8	Reserved	Ignore when read	RO
4.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
4.1.6:3	Reserved	Ignore when read	RO
4.1.2	PHY XS transmit link status	1 = The PHY XS transmit link is up 0 = The PHY XS transmit link is down	RO/LL
4.1.1	Low-power ability	1 = PHY XS supports low-power mode 0 = PHY XS does not support low-power mode	RO
4.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.4.2.3 Low-power ability (4.1.1)

When read as a one, bit 4.1.1 indicates that the PHY XS supports the low-power feature. When read as a zero, bit 4.1.1 indicates that the PHY XS does not support the low-power feature. If a PHY XS supports the low-power feature then it is controlled using the low-power bit in the PHY XS control register.

45.2.4.3 PHY XS device identifier (Registers 4.2 and 4.3)

Registers 4.2 and 4.3 provide a 32-bit value, which may constitute a unique identifier for a PHY XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS device identifier.

The format of the PHY XS device identifier is specified in 22.2.4.3.1.

45.2.4.4 PHY XS speed ability (Register 4.4)

The assignment of bits in the PHY XS speed ability register is shown in Table 45–102.

Table 45–102—PHY XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
4.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
4.4.0	10G capable	1 = PHY XS is capable of operating at 10 Gb/s 0 = PHY XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.4.4.1 10G capable (4.4.0)

When read as a one, bit 4.4.0 indicates that the PHY XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 4.4.0 indicates that the PHY-XS is not able to operate at a data rate of 10 Gb/s.

45.2.4.5 PHY XS devices in package (Registers 4.5 and 4.6)

The PHY XS devices in package registers are defined in Table 45–2.

45.2.4.6 PHY XS status 2 register (Register 4.8)

The assignment of bits in the PHY XS status 2 register is shown in Table 45–103. All the bits in the PHY XS status 2 register are read only; a write to the PHY XS status 2 register shall have no effect.

Table 45–103—PHY XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
4.8.13:12	Reserved	Ignore when read	RO
4.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
4.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
4.8.9:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High

45.2.4.6.1 Device present (4.8.15:14)

When read as <10>, bits 4.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 4.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.4.6.2 Transmit fault (4.8.11)

When read as a one, bit 4.8.11 indicates that the PHY XS has detected a fault condition on the transmit path. When read as a zero, bit 4.8.11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value for bit 4.8.11 is zero.

45.2.4.6.3 Receive fault (4.8.10)

When read as a one, bit 4.8.10 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 4.8.10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 4.8.10 is zero.

45.2.4.7 PHY XS package identifier (Registers 4.14 and 4.15)

Registers 4.14 and 4.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PHY XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the PHY XS package identifier is specified in 22.2.4.3.1.

45.2.4.8 10G PHY XGXS lane status register (Register 4.24)

The assignment of bits in the 10G PHY XGXS lane status register is shown in Table 45–104. All the bits in the 10G PHY XGXS lane status register are read only; a write to the 10G PHY XGXS lane status register shall have no effect.

45.2.4.8.1 PHY XGXS transmit lane alignment status (4.24.12)

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four transmit lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four transmit lanes.

45.2.4.8.2 Pattern testing ability (4.24.11)

When read as a one, bit 4.24.11 indicates that the 10G PHY XGXS is able to generate test patterns. When read as a zero, bit 4.24.11 indicates that the 10G PHY XGXS is not able to generate test patterns. If the 10G PHY XGXS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 4.25.

45.2.4.8.3 PHY XS loopback ability (4.24.10)

When read as a one, bit 4.24.10 indicates that the PHY XGXS is able to perform the loopback function. When read as a zero, bit 4.24.10 indicates that the PHY XGXS is not able to perform the loopback function. If a 10G PHY XGXS is able to perform the loopback function, then it is controlled using the PHY XGXS loopback bit 4.0.14.

45.2.4.8.4 Lane 3 sync (4.24.3)

When read as a one, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is synchronized. When read as a zero, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is not synchronized.

Table 45–104—10G PHY XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
4.24.15:13	Reserved	Ignore when read	RO
4.24.12	PHY XGXS lane alignment status	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	RO
4.24.11	Pattern testing ability	1 = PHY XGXS is able to generate test patterns 0 = PHY XGXS is not able to generate test patterns	RO
4.24.10	PHY XGXS loopback ability	1 = PHY XGXS has the ability to perform a loopback function 0 = PHY XGXS does not have the ability to perform a loopback function	RO
4.24.9:4	Reserved	Ignore when read	RO
4.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
4.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
4.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
4.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.4.8.5 Lane 2 sync (4.24.2)

When read as a one, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is synchronized. When read as a zero, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is not synchronized.

45.2.4.8.6 Lane 1 sync (4.24.1)

When read as a one, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is synchronized. When read as a zero, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is not synchronized.

45.2.4.8.7 Lane 0 sync (4.24.0)

When read as a one, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is synchronized. When read as a zero, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is not synchronized.

45.2.4.9 10G PHY XGXS test control register (Register 4.25)

The assignment of bits in the 10G PHY XGXS test control register is shown in Table 45–105. The default value for each bit of the 10G PHY XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–105—10G PHY XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
4.25.15:3	Reserved	Value always 0, writes ignored	R/W
4.25.2	Receive test-pattern enable	1 = Receive test pattern enabled 0 = Receive test pattern not enabled	R/W
4.25.1:0	Test-pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.4.9.1 10G PHY XGXS test-pattern enable (4.25.2)

When bit 4.25.2 is set to a one, pattern testing is enabled on the receive path. When bit 4.25.2 is set to a zero, pattern testing is disabled on the receive path. Pattern testing is optional, and the ability of the 10G PHY XGXS to generate test patterns is advertised by the pattern testing ability bit in register 4.24. A 10G PHY XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 4.25.2 is zero.

45.2.4.9.2 10G PHY XGXS test-pattern select (4.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 4.25.2 is selected using bits 4.25.1:0. When bits 4.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.5 DTE XS registers

The assignment of registers in the DTE XS is shown in Table 45–106.

45.2.5.1 DTE XS control 1 register (Register 5.0)

The assignment of bits in the DTE XS control 1 register is shown in Table 45–107. The default value for each bit of the DTE XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.5.1.1 Reset (5.0.15)

Resetting a DTE XS is accomplished by setting bit 5.0.15 to a one. This action shall set all DTE XS registers to their default states. As a consequence, this action may change the internal state of the DTE XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a DTE XS shall return a value of one in bit 5.0.15 when a reset is in progress and a value of zero otherwise. A DTE XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 5.0.15. During a reset, a DTE XS shall respond to reads to register bits 5.0.15 and 5.8.15:14. All other register bits should be ignored.

Table 45–106—DTE XS registers

Register address	Register name
5.0	DTE XS control 1
5.1	DTE XS status 1
5.2, 5.3	DTE XS device identifier
5.4	DTE XS speed ability
5.5, 5.6	DTE XS devices in package
5.7	Reserved
5.8	DTE XS status 2
5.9 through 5.13	Reserved
5.14, 5.15	DTE XS package identifier
5.16 through 5.23	Reserved
5.24	10G DTE XGXS lane status
5.25	10G DTE XGXS test control
5.26 through 5.32 767	Reserved
5.32 768 through 5.65 535	Vendor specific

NOTE—This operation may interrupt data communication.

45.2.5.1.2 Loopback (5.0.14)

The DTE XS shall be placed in a Loopback mode of operation when bit 5.0.14 is set to a one. When bit 5.0.14 is set to a one, the DTE XS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the specific behavior of a DTE XS during loopback is specified in 48.3.3.

The default value of bit 5.0.14 is zero.

NOTE—The signal path through the DTE XS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the DTE XS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.5.1.3 Low power (5.0.11)

A DTE XS may be placed into a low-power mode by setting bit 5.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the DTE XS. The behavior of the DTE XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 5.0.11 is zero.

Table 45–107—DTE XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.0.15	Reset	1 = DTE XS reset 0 = Normal operation	R/W SC
5.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
5.0.13	Speed selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	R/W
5.0.12	Reserved	Value always 0, writes ignored	R/W
5.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
5.0.10:7	Reserved	Value always 0, writes ignored	R/W
5.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
5.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
5.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.5.1.4 Speed selection (5.0.13, 5.0.6, 5.0.5:2)

Speed selection bits 5.0.13 and 5.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the DTE XS may be selected using bits 5 through 2. The speed abilities of the DTE XS are advertised in the DTE XS speed ability register. A DTE XS may ignore writes to the DTE XS speed selection bits that select speeds it has not advertised in the DTE XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The DTE XS speed selection defaults to a supported ability.

45.2.5.2 DTE XS status 1 register (Register 5.1)

The assignment of bits in the DTE XS status 1 register is shown in Table 45–108. All the bits in the DTE XS status 1 register are read only; a write to the DTE XS status 1 register shall have no effect.

Table 45–108—DTE XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.1.15:8	Reserved	Ignore when read	RO
5.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
5.1.6:3	Reserved	Ignore when read	RO
5.1.2	DTE XS receive link status	1 = The DTE XS receive link is up 0 = The DTE XS receive link is down	RO/LL
5.1.1	Low-power ability	1 = DTE XS supports low-power mode 0 = DTE XS does not support low-power mode	RO
5.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.5.2.1 Fault (5.1.7)

When read as a one, bit 5.1.7 indicates that the DTE XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 5.1.7 indicates that the DTE XS has not detected a fault condition. Bit 5.1.7 is set to a one when either of the fault bits (5.8.11, 5.8.10) located in register 5.8 are set to a one.

45.2.5.2.2 DTE XS receive link status (5.1.2)

When read as a one, bit 5.1.2 indicates that the DTE XS receive link is aligned. When read as a zero, bit 5.1.2 indicates that the DTE XS receive link is not aligned. The receive link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, this bit is a latching low version of bit 5.24.12.

45.2.5.2.3 Low-power ability (5.1.1)

When read as a one, bit 5.1.1 indicates that the DTE XS supports the low-power feature. When read as a zero, bit 5.1.1 indicates that the DTE XS does not support the low-power feature. If a DTE XS supports the low-power feature then it is controlled using the low-power bit in the DTE XS control register.

45.2.5.3 DTE XS device identifier (Registers 5.2 and 5.3)

Registers 5.2 and 5.3 provide a 32-bit value, which may constitute a unique identifier for a DTE XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS device identifier.

The format of the DTE XS device identifier is specified in 22.2.4.3.1

45.2.5.4 DTE XS speed ability (Register 5.4)

The assignment of bits in the DTE XS speed ability register is shown in Table 45–109.

Table 45–109— DTE XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
5.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
5.4.0	10G capable	1 = DTE XS is capable of operating at 10 Gb/s 0 = DTE XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.5.4.1 10G capable (5.4.0)

When read as a one, bit 5.4.0 indicates that the DTE XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 5.4.0 indicates that the DTE XS is not able to operate at a data rate of 10 Gb/s.

45.2.5.5 DTE XS devices in package (Registers 5.5 and 5.6)

The DTE XS devices in package registers are defined in Table 45–2.

45.2.5.6 DTE XS status 2 register (Register 5.8)

The assignment of bits in the DTE XS status 2 register is shown in Table 45–110. All the bits in the DTE XS status 2 register are read only; a write to the DTE XS status 2 register shall have no effect.

Table 45–110—DTE XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
5.8.13:12	Reserved	Ignore when read	RO
5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
5.8.9:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High

45.2.5.6.1 Device present (5.8.15:14)

When read as <10>, bits 5.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 5.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.5.6.2 Transmit fault (5.8.11)

When read as a one, bit 5.8.11 indicates that the DTE XS has detected a fault condition on the transmit path. When read as a zero, bit 5.8.11 indicates that the DTE XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.11 is zero.

45.2.5.6.3 Receive fault (5.8.10)

When read as a one, bit 5.8.10 indicates that the DTE XS has detected a fault condition on the receive path. When read as a zero, bit 5.8.10 indicates that the DTE XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.10 is zero.

45.2.5.7 DTE XS package identifier (Registers 5.14 and 5.15)

Registers 5.14 and 5.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the DTE XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the DTE XS package identifier is specified in 22.2.4.3.1.

45.2.5.8 10G DTE XGXS lane status register (Register 5.24)

The assignment of bits in the 10G DTE XGXS lane status register is shown in Table 45–111. All the bits in the 10G DTE XGXS lane status register are read only; a write to the 10G DTE XGXS lane status register shall have no effect.

45.2.5.8.1 DTE XGXS receive lane alignment status (5.24.12)

When read as a one, bit 5.24.12 indicates that the DTE XGXS has synchronized and aligned all four receive lanes. When read as a zero, bit 5.24.12 indicates that the DTE XGXS has not synchronized and aligned all four receive lanes.

45.2.5.8.2 Pattern testing ability (5.24.11)

When read as a one, bit 5.24.11 indicates that the 10G DTE XGXS is able to generate test patterns. When read as a zero, bit 5.24.11 indicates that the 10G DTE XGXS is not able to generate test patterns. If the 10G DTE XGXS is able to generate test patterns then the functionality is controlled using the transmit test-pattern enable bit in register 5.25.

45.2.5.8.3 Lane 3 sync (5.24.3)

When read as a one, bit 5.24.3 indicates that the XGXS receive lane 3 is synchronized. When read as a zero, bit 5.24.3 indicates that the XGXS receive lane 3 is not synchronized.

Table 45–111—10G DTE XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
5.24.15:13	Reserved	Ignore when read	RO
5.24.12	DTE XGXS lane alignment status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO
5.24.11	Pattern testing ability	1 = DTE XGXS is able to generate test patterns 0 = DTE XGXS is not able to generate test patterns	RO
5.24.10:4	Reserved	Ignore when read	RO
5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.5.8.4 Lane 2 sync (5.24.2)

When read as a one, bit 5.24.2 indicates that the XGXS receive lane 2 is synchronized. When read as a zero, bit 5.24.2 indicates that the XGXS receive lane 2 is not synchronized.

45.2.5.8.5 Lane 1 sync (5.24.1)

When read as a one, bit 5.24.1 indicates that the XGXS receive lane 1 is synchronized. When read as a zero, bit 5.24.1 indicates that the XGXS receive lane 1 is not synchronized.

45.2.5.8.6 Lane 0 sync (5.24.0)

When read as a one, bit 5.24.0 indicates that the XGXS receive lane 0 is synchronized. When read as a zero, bit 5.24.0 indicates that the XGXS receive lane 0 is not synchronized.

45.2.5.9 10G DTE XGXS test control register (Register 5.25)

The assignment of bits in the 10G DTE XGXS test control register is shown in Table 45–112. The default value for each bit of the 10G DTE XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.5.9.1 10G DTE XGXS test-pattern enable (5.25.2)

When bit 5.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 5.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10G DTE XGXS to generate test patterns is advertised by the pattern testing ability bit in register 5.24. A 10G

Table 45–112—10G DTE XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
5.25.15:3	Reserved	Value always 0, writes ignored	R/W
5.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
5.25.1:0	Test-pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

DTE XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 5.25.2 is zero.

45.2.5.9.2 10G DTE XGXS test-pattern select (5.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 5.25.2 is selected using bits 5.25.1:0. When bits 5.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.6 TC registers

The assignment of registers in the TC MMD is shown in Table 45–113.

Table 45–113—TC registers

Register address	Register name
6.0	TC control
6.1	Reserved
6.2, 6.3	TC device identifier
6.4	TC speed ability
6.5, 6.6	TC devices in package
6.7 through 6.13	Reserved
6.14, 6.15	TC package identifier

Table 45–113—TC registers

Register address	Register name
6.16	10P/2B aggregation discovery control[a]
6.17	10P/2B aggregation and discovery status[a]
6.18, 6.19, 6.20	10P/2B aggregation discovery code[a]
6.21	10P/2B link partner PME aggregate control[a]
6.22, 6.23	10P/2B link partner PME aggregate data[a]
6.24	10P/2B TC CRC error counter
6.25, 6.26	10P/2B TPS-TC coding violations counter
6.27	10P/2B TC indications
6.28 through 6.32 767	Reserved
6.32 768 through 6.65 535	Vendor specific

[a]Register is defined only for -O port types and is reserved for -R ports

45.2.6.1 TC control register (Register 6.0)

The assignment of bits in the TC control register is shown in Table 45–114. The default value for each bit of the TC control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–114—TC control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.0.15	Reset	1 = TC reset 0 = Normal operation	R/W SC
6.0.14	Reserved	Value always 0, writes ignored	R/W
6.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
6.0.12:7	Reserved	Value always 0, writes ignored	R/W
6.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
6.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = Reserved	R/W
6.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.6.1.1 Reset (6.0.15)

Resetting a TC is accomplished by setting bit 6.0.15 to a one. This action shall set all TC registers to their default states. As a consequence, this action may change the internal state of the TC and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a TC shall return a value of one in bit 6.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A TC is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 6.0.15. During a reset, a TC shall respond to reads from register bit 6.0.15.

NOTE—This operation may interrupt data communication. The data path of a TC, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset.

45.2.6.1.2 Speed selection (6.0.13, 6.0.6, 6.0.5:2)

Speed selection bits 6.0.13 and 6.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The operating mode of the TC may be selected using bits 5 through 2. The abilities of the TC are advertised in the TC speed ability register. A TC may ignore writes to the TC speed selection bits that select speeds it has not advertised in the TC speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The speed selection bits 6.0.5:2, when set to 0001, select the use of the 10PASS-TS and 2BASE-TL TC.

The TC speed selection defaults to a supported ability.

45.2.6.2 TC device identifier (Registers 6.2 and 6.3)

Registers 6.2 and 6.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of TC. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A TC may return a value of zero in each of the 32 bits of the TC device identifier.

The format of the TC device identifier is specified in 22.2.4.3.1.

45.2.6.3 TC speed ability (Register 6.4)

The assignment of bits in the TC speed ability register is shown in Table 45–115.

Table 45–115—TC speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
6.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
6.4.1	10PASS-TS/2BASE-TL capable	1 = TC is capable of operating as the 10P/2B TC 0 = TC is not capable of operating as the 10P/2B TC	RO
6.4.0	Reserved	Value always 0, writes ignored	RO

[a]RO = Read Only

45.2.6.3.1 10PASS-TS/2BASE-TL capable (6.4.1)

When read as a one, this bit indicates that the TC is able to operate as the 10PASS-TS/2BASE-TL TC, as specified in Clause 61.

45.2.6.4 TC devices in package registers (Registers 6.5, 6.6)

The TC devices in package registers are defined in Table 45–2.

45.2.6.5 TC package identifier registers (Registers 6.14, 6.15)

Registers 6.14 and 6.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the TC MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A TC may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.6.6 10P/2B aggregation discovery control register (Register 6.16)

The 10P/2B aggregation discovery control register allows the STA of an -O port to determine the aggregation capabilities of an -R link-partner.

The 10P/2B aggregation discovery control register shall be implemented as a unique register for each TC MMD in a package. For example, a package implementing four PHYs would have four independent instances of the 10P/2B aggregation discovery control register, accessed by a read or write to each PHY.

For information on the encoding of this function on the physical link, see 61.4.7.

This register is defined for -O port sub-types only. The register bit definitions for the 10P/2B aggregation discovery control register are shown in Table 45–116.

Table 45–116—10P/2B aggregation discovery control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.16.15:2	Reserved	Value always 0, writes ignored	R/W
6.16.1:0	Discovery operation	01 = Ready (default) 00 = Set if clear 11 = Clear if same 10 = Get	R/W

[a]R/W = Read/Write

45.2.6.6.1 Discovery operation (6.16.1:0)

The Discovery operation bits are used to query and manipulate the remote discovery register. The remote discover register is not a Clause 45 object, but a variable of the PME Aggregation PCS function on -R ports. The Discovery operation makes use of G.994.1 handshaking messages, therefore valid only when the link status is down (i.e., neither Initializing nor Up). Attempts to perform an operation while the link is Initializing or Up shall be ignored.

The default state of these bits is “Ready.” The bits shall indicate “Ready” any time the PME aggregation function is capable of performing an operation on the remote discovery register. If PAF is not supported, the discovery operation bits shall indicate “Ready” and ignore writes. These bits shall return to the “Ready” state upon MMD Reset.

If the STA sets the bits to "Get," the PME aggregation function queries the remote discovery register and returns its contents to the aggregation discovery code register.

If the STA sets the bits to "Set if clear," the PME aggregation function passes a message to the -R PCS instructing it to set the remote discovery register to the contents of the aggregation discovery code register, but only if the remote discovery register is all zeroes.

If the STA sets the bits to "Clear if same," the PME aggregation function passes a message to the -R PCS instructing it to clear the remote discovery register, but only if the contents of the remote discovery register currently match the contents of the aggregation discovery code register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate "Ready". If the operation does not complete within a 255 second time-out, the discovery operation result bit (6.17.0) will be set to "1" (operation unsuccessful), and the discovery operation bits will be set to "Ready".

45.2.6.7 10P/2B aggregation and discovery status register (Register 6.17)

The 10P/2B aggregation and discovery status register is defined for -O port sub-types only.

The assignment of bits in the 10P/2B aggregation and discovery status register is shown in Table 45–117.

Table 45–117—10P/2B aggregation and discovery status register bit definitions

Bit(s)	Name	Description	R/W[a]
6.17.15:2	Reserved	Value always 0, writes ignored	R/W
6.17.1	Link partner aggregate operation result	1 = operation unsuccessful 0 = operation completed successfully (default)	RO, LH
6.17.0	Discovery operation result	1 = operation unsuccessful 0 = discovery operation completed successfully (default)	RO, LH

[a]R/W = Read/Write, RO = Read Only, LH = Latches High

45.2.6.7.1 Link partner aggregate operation result (6.17.1)

When a link partner aggregate operation is complete, the PHY sets this bit to indicate the result of the operation. A "1" indicates that the operation could not be completed. This may be for a variety of reasons:

a) PMA/PMD link status is initializing or up.
b) the link partner is not present or not responding.

If PAF is not supported, this bit shall remain set to zero.

45.2.6.7.2 Discovery operation result (6.17.0)

When a discovery operation is complete, the PHY sets this bit to indicate the result of the operation. A "1" indicates that the operation could not be completed. This may be for a variety of reasons:

a) PMA/PMD link status is initializing or up
b) a "Set if clear" operation was requested but the remote discovery register was not clear
c) a "Clear if same" operation was requested but the remote discovery register did not match the aggregation discovery code register
d) the link partner is not present or not responding

If PAF is not supported, this bit shall read as zero.

45.2.6.8 10P/2B aggregation discovery code (Registers 6.18, 6.19, 6.20)

The 10P/2B aggregation discovery code registers store the value of the remote_discovery_register exchanged with the -R link partner.

This register is defined for -O port sub-types only.

These registers shall be implemented as unique registers for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the 10P/2B aggregation discovery code registers, accessed by a read or write to each PHY.

For information on the encoding of this function on the physical link, please see 61.4.7.

The assignment of bits for the 10P/2B aggregation discovery code registers are shown in Table 45–118.

Table 45–118—10P/2B aggregation discovery code bit definitions

Bit(s)	Name	Description	R/W[a]
6.18.15:0	Code [47:32]	The two most significant octets of the aggregation discovery code	R/W
6.19.15:0	Code [31:16]	The two middle octets of the aggregation discovery code	R/W
6.20.15:0	Code [15:0]	The two least significant octets of the aggregation discovery code	R/W

[a]R/W = Read/Write

45.2.6.9 10P/2B link partner PME aggregate control register (Register 6.21)

The 10P/2B link partner PME aggregate control register allows the STA of an -O port to read and write the remote PME_Aggregate_register (see 61.2.2.8.3).

The 10P/2B link partner PME aggregate control register shall be implemented as a unique register for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the 10P/2B link partner PME aggregate control register, accessed by a read or write to each PHY.

This register is defined for -O port sub-types only.

The register bit definitions for the 10P/2B link partner PME aggregate control register are shown in Table 45–119.

Table 45–119—10P/2B link partner PME aggregate control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.21.15:2	Reserved	Value always 0, writes ignored	R/W
6.21.1:0	Link partner aggregate operation	01 = Ready (default) 00 = Set 11 = invalid 10 = Get	R/W

[a]R/W = Read/Write

45.2.6.9.1 Link partner aggregate operation (1.21.1:0)

The Link partner aggregate operation bits are used to query and manipulate the remote PME_Aggregate_register. This operation makes use of G.994.1 handshaking messages and therefore must be performed only when the link status is down (i.e., neither Initializing nor Up). Attempts to perform an operation while the link is Initializing or Up shall be ignored.

The default state of these bits is "Ready." The bits shall indicate "Ready" any time the PME aggregation function is capable of performing an operation on the remote PME_Aggregate_register. If PAF is not supported, the link partner aggregate operation bits shall indicate "Ready" ignore writes. These bits shall return to the "Ready" state upon MMD Reset.

If the STA sets the bits to "Get," the PME aggregation function queries the remote PME_Aggregate_register and returns its contents to the 10P/2B link partner PME aggregate data register (see 45.2.6.10).

If the STA sets the bits to "Set," the PME aggregation function passes a message to the -R PCS instructing it to set the bit location in the remote PME_Aggregate_register corresponding to the TC on which the message was received to the contents of bit 0 of the 10P/2B link partner PME aggregate data register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate "Ready".

45.2.6.10 10P/2B link partner PME aggregate data (Registers 6.22, 6.23)

The 10P/2B link partner PME aggregate data registers store the data for the link partner aggregate operation. This register either contains the result of a "Get" operation, the data sent in a "Set" operation, or all zeros following an MMD reset.

These registers are defined for -O port sub-types only.

These registers shall be implemented as unique registers for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the registers, accessed by a read or write to each PHY.

The assignment of bits for the 10P/2B link partner PME aggregate data registers are shown in Table 45–120.

Table 45–120—10P/2B link partner PME aggregate data registers bit definitions

Bit(s)	Name	Description	R/W[a]
6.22.15:0	Data[31:16]	The two most significant octets of the link partner PME aggregate data	R/W
6.23.15:0	Data[15:0]	The two least significant octets of the link partner PME aggregate data	R/W

[a]R/W = Read/Write

45.2.6.11 10P/2B TC CRC error register (Register 6.24)

The 10P/2B TC CRC error register is a 16 bit counter that contains the number of TC frames received with the TC_CRC_error primitive asserted, defined in 61.2.3. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B TC CRC error register are shown in Table 45–121.

Table 45–121—10P/2B TC CRC error register bit definitions

Bits(s)	Name	Description	R/W[a]
6.24.15:0	CRC errors[15:0]	The bytes of the counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.6.12 10P/2B TPS-TC coding violations counter (Registers 6.25, 6.26)

The 10P/2B TPS-TC coding violations counter is a 32-bit counter that contains the number of 64/64-octet encapsulation errors, defined in 61.3.3.1. This counter increments for each 64/65-octet received with the TC_coding_error signal asserted. These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B TPS-TC coding violations counter are shown in Table 45–122.

Table 45–122—10P/2B TPS-TC coding violations counter bit definitions

Bits(s)	Name	Description	R/W[a]
6.25.15:0	Coding violations[31:16]	The high order bytes of the counter	RO, MW
6.26.15:0	Coding violations[15:0]	The low order bytes of the counter	RO, MW

[a]RO = Read Only, MW = Multi-word

45.2.6.13 10P/2B TC indications register (Register 6.27)

The 10P/2B TC indications register reflects the state of the TC sync detect state machine and the state of the link partner TC sync detect state machine (if present) (see 61.3.3.5). The assignment of bits in the 10P/2B TC indications register is shown in Table 45–123.

Table 45–123—10P/2B TC indications register bit definitions

Bit(s)	Name	Description	R/W[a]
6.27.15:9	Reserved	Value always 0	RO
6.27.8	Local TC synchronized	1 = TC_synchronized is TRUE 0 = TC_synchronized is FALSE	RO
6.27.7:1	Reserved	Value always 0	RO
6.27.0	Remote TC synchronized	1 = remote_TC_out_of_sync is FALSE 0 = remote_TC_out_of_sync is TRUE	RO

[a]RO = Read Only

45.2.6.13.1 Local TC synchronized (6.27.8)

This bit is read as a one when the TC_synchronized variable in the TC sync detect state machine is TRUE (see 61.2.3.3.8). In all other cases, this bit is read as zero.

45.2.6.13.2 Remote TC synchronized (6.27.0)

This bit is read as a one when the remote_TC_out_of_sync variable in the link partner TC sync detect state machine is FALSE (see 61.2.3.3.8). In all other cases, this bit is read as zero.

45.2.7 Clause 22 extension registers

As new management features are added to 10, 100 and 1000 Mb/s PHYs, more register space is required beyond that defined in Clause 22. The Clause 22 extension MMD provides this space. This MMD is defined only for 10, 100, 1000 Mb/s PHYs. Since these PHYs do not segment their management by their sublayers, all management extensions to these PHYs will appear in the Clause 22 extension MMD.

The assignment of registers in the Clause 22 extension MMD is shown in Table 45–124.

Table 45–124—Clause 22 extension registers

Register address	Register name
29.0 through 29.4	Reserved
29.5, 29.6	Clause 22 extension devices in package
29.7	FEC capability
29.8	FEC control
29.9	FEC buffer head coding violation counter
29.10	FEC corrected blocks counter
29.11	FEC uncorrected blocks counter
29.12 through 29.32 767	Reserved

45.2.7.1 Clause 22 extension devices in package registers (Registers 29.5, 29.6)

The Clause 22 extension devices in package registers are defined in Table 45–7.

45.2.7.2 FEC capability register (Register 29.7)

The assignment of bits in the FEC capability register is shown in.Table 45–125.

Table 45–125—FEC capability register bit definitions

Bits(s)	Name	Description	R/W[a]
29.7.15:1	Reserved	Value always 0, writes ignored	RO
29.7.0	FEC capable	1 = FEC supported 0 = FEC unsupported	RO

[a]RO = Read Only

45.2.7.2.1 FEC capable (29.7.0)

When read as a one, this bit indicates that the PHY supports forward error correction. When read as a zero, the PHY does not support forward error correction.

45.2.7.3 FEC control register (Register 29.8)

The assignment of bits in the FEC control register is shown in Table 45–126.

Table 45–126—FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
29.8.15:1	Reserved	Value always 0, writes ignored	R/W
29.8.0	FEC enable	1 = FEC enabled 0 = FEC disabled	R/W

[a]R/W = Read/Write

45.2.7.3.1 FEC enable (29.8.0)

When written as a one, this bit enables the PHY's forward error correction. When written as a zero, FEC is disabled. This bit shall be set to zero upon execution of a PHY reset.

45.2.7.4 FEC buffer head coding violation counter (Register 29.9)

The assignment of bits in the FEC buffer head coding violation counter register is shown in Table 45–127. See 65.2.3.6.1 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–127—FEC buffer head coding violation counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.9.15:0	FEC buffer head coding violation counter	Error counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.7.5 FEC corrected blocks counter (Register 29.10)

The assignment of bits in the FEC corrected blocks counter register is shown in Table 45–128. See 65.2.3.6.2 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–128—FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.10.15:0	FEC corrected blocks counter	Error counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.7.6 FEC uncorrected blocks counter (Register 29.11)

The assignment of bits in the FEC uncorrected blocks counter register is shown in Table 1–0a. See 65.2.3.6.3 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 1–0a—FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.11.15:0	FEC uncorrected blocks counter	Error counter	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.8 Vendor specific MMD 1 registers

The assignment of registers in the vendor specific MMD 1 is shown in Table 45–129. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

Table 45–129—Vendor specific MMD 1 registers

Register address	Register name
30.0, 30.1	Vendor specific
30.2, 30.3	Vendor specific MMD 1 device identifier
30.4 through 30.7	Vendor specific
30.8	Vendor specific MMD 1 status register
30.9 through 30.13	Vendor specific
30.14, 30.15	Vendor specific MMD 1 package identifier
30.16 through 30.65 535	Vendor specific

45.2.8.1 Vendor specific MMD 1 device identifier (Registers 30.2 and 30.3)

Registers 30.2 and 30.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 1 device identifier.

The format of the vendor specific MMD 1 device identifier is specified in 22.2.4.3.1.

45.2.8.2 Vendor specific MMD 1 status register (Register 30.8)

The assignment of bits in the vendor specific MMD 1 status register is shown in Table 45–130. All the bits in the vendor specific MMD 1 status register are read only; a write to the vendor specific MMD 1 status register shall have no effect.

Table 45–130—Vendor specific MMD 1 status register bit definitions

Bit(s)	Name	Description	R/W[a]
30.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
30.8.13:0	Reserved	Ignore when read	RO

[a]RO = Read Only

45.2.8.2.1 Device present (30.8.15:14)

When read as <10>, bits 30.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 30.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.8.3 Vendor specific MMD 1 package identifier (Registers 30.14 and 30.15)

Registers 30.14 and 30.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD 1 is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD 1 may return a value of zero in each of the 32 bits of the vendor specific MMD 1 package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 1 package identifier is specified in 22.2.4.3.1.

45.2.9 Vendor specific MMD 2 registers

The assignment of registers in the vendor specific MMD 2 is shown in Table 45–131. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

45.2.9.1 Vendor specific MMD 2 device identifier (Registers 31.2 and 31.3)

Registers 31.2 and 31.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number,

Table 45–131—Vendor specific MMD 2 registers

Register address	Register name
31.0, 31.1	Vendor specific
31.2, 31.3	Vendor specific MMD 2 device identifier
31.4 through 31.7	Vendor specific
31.8	Vendor specific MMD 2 status register
31.9 through 31.13	Vendor specific
31.14, 30.15	Vendor specific MMD 2 package identifier
31.16 through 31.65 535	Vendor specific

plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 2 device identifier.

The format of the vendor specific MMD 2 device identifier is specified in 22.2.4.3.1.

45.2.9.2 Vendor specific MMD 2 status register (Register 31.8)

The assignment of bits in the vendor specific MMD 2 status register is shown in Table 45–132. All the bits in the vendor specific MMD 2 status register are read only; a write to the vendor specific MMD status register shall have no effect.

Table 45–132—Vendor specific MMD 2 status register bit definitions

Bit(s)	Name	Description	R/W[a]
31.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
31.8.13:0	Reserved	Ignore when read	RO

[a]RO = Read Only

45.2.9.2.1 Device present (31.8.15:14)

When read as <10>, bits 31.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 31.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.9.3 Vendor specific MMD 2 package identifier (Registers 31.14 and 31.15)

Registers 31.14 and 31.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 2 package identifier is specified in 22.2.4.3.1.

45.3 Management frame structure

The MDIO interface frame structure is compatible with the one defined in 22.2.4.5 such that the two systems can co-exist on the same MDIO bus. The electrical specification for the MDIO interface is incompatible to that defined in 22.2.4.5; therefore, if the two systems are to co-exist on the same bus, a voltage translation device is required (see Annex 45A). The extensions that are used for MDIO indirect register accesses are specified in Table 45–133.

Table 45–133—Extensions to Management Frame Format for Indirect Access

	Management frame fields							
Frame	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**ADDRESS / DATA**	**IDLE**
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

Each MMD shall implement a sixteen bit address register that stores the address of the register to be accessed by data transaction frames. The address register shall be overwritten by address frames. At power up or device reset, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames shall access the register whose address is stored in the address register. Write and read frames shall not modify the contents of the address register.

Upon receiving a post-read-increment-address frame and having completed the read operation, the MMD shall increment the address register by one. For the case where the MMD's address register contains 65 535, the MMD shall not increment the address register.

Implementations that incorporate several MMDs within a single component shall implement separate address registers so that the MMD's address registers operate independently of one another.

45.3.1 IDLE (idle condition)

The idle condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the MMD's pull-up resistor will pull the MDIO line to a one.

45.3.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC to provide the MMD with a pattern that it can use to establish synchronization. An MMD shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

45.3.3 ST (start of frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 shall be ignored by the devices specified in Clause

45.3.4 OP (operation code)

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read-increment-address operation.

45.3.5 PRTAD (port address)

The port address is five bits, allowing 32 unique port addresses. The first port address bit to be transmitted and received is the MSB of the address. A station management entity must have a priori knowledge of the appropriate port address for each port to which it is attached, whether connected to a single port or to multiple ports.

45.3.6 DEVAD (device address)

The device address is five bits, allowing 32 unique MMDs per port. The first device address bit transmitted and received is the MSB of the address.

45.3.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the device address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, both the STA and the MMD shall remain in a high-impedance state for the first bit time of the turnaround. The MMD shall drive a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–13 shows the behavior of the MDIO signal during the turnaround field of a read or post-read-increment-address transaction.

45.3.8 ADDRESS / DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register.

For a read or post-read-increment-address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

45.4 Electrical interface

45.4.1 Electrical specification

The electrical characteristics of the MDIO interface are shown in Table 45–134. The MDIO uses signal levels that are compatible with devices operating at a nominal supply voltage of 1.2V.

NOTE—It is possible to implement the MDIO electrical interface using open drain buffers and a weak resistive pull up to a V_{DD} of 1.2V.

Table 45–134—MDIO electrical interface characteristics

Symbol	Parameter	Condition	Min.	Max.
V_{IH}	Input high voltage		0.84V	1.5V
V_{IL}	Input low voltage		–0.3V	0.36V
V_{OH}	Output high voltage	I_{OH} = -100uA	1.0V	1.5V
V_{OL}	Output low voltage	I_{OL} = 100uA	–0.3V	0.2V
I_{OH}[a]	Output high current	V_I = 1.0V		–4mA
I_{OL}	Output low current	V_I = 0.2V	+4mA	
C_i	Input capacitance			10pF
C_L	Bus loading			470pF

[a]I_{OH} parameter is not applicable to open drain drivers.

45.4.2 Timing specification

MDIO is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the MMD. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 45–3, measured at the MMD.

When the MDIO signal is sourced by the MMD, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the MMD, as measured at the STA, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 45–4.

The timing specification for the MDC signal is given in 22.2.2.11.

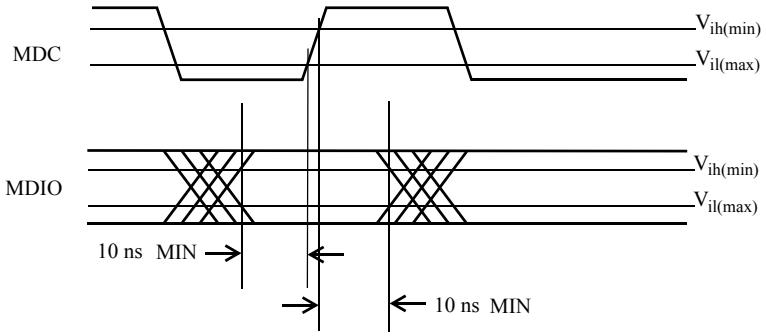


Figure 45–3—MDIO sourced by STA

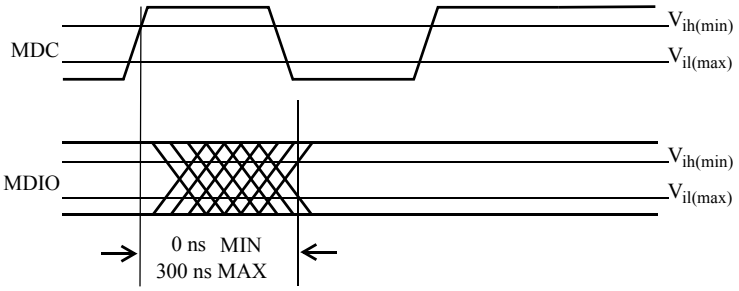


Figure 45–4—MDIO sourced by MMD

45.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 45, MDIO interface[2]

45.5.3 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 45, MDIO interface, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

45.5.4 Identification

45.5.4.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

45.5.4.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Implementation of PMA/PMD MMD	45.2.1		O	Yes [ ] No [ ]
*WIS	Implementation of WIS MMD	45.2.2		O	Yes [ ] No [ ]
*PCS	Implementation of PCS MMD	45.2.3		O	Yes [ ] No [ ]
*PX	Implementation of PHY XS MMD	45.2.4		O	Yes [ ] No [ ]
*DX	Implementation of DTE XS MMD	45.2.5		O	Yes [ ] No [ ]
*VSA	Implementation of Vendor Specific MMD 1	45.2.8		O	Yes [ ] No [ ]
*VSB	Implementation of Vendor Specific MMD 2	45.2.9		O	Yes [ ] No [ ]
*TC	Implementation of the TC MMD	45.2.6		10P*2B:M	Yes [ ] No [ ]
*CTT	Implementation of the Clause 22 extension MMD	45.2.7		O	Yes [ ] No [ ]

45.5.5 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.5.1 MDIO signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	MDIO uses three-state drivers	45.4.1		M	Yes [ ]

45.5.5.2 PMA/PMD MMD options

Item	Feature	Subclause	Value/Comment	Status	Support
*ALB	Implementation of PMA loop-back function	45.2.1.1.4		PMA:O	Yes [ ] No [ ] N/A [ ]
*PLF	Implementation of fault detection	45.2.1.7		PMA:O	Yes [ ] No [ ] N/A [ ]
*PTD	Implementation of transmit disable function	45.2.1.8		PMA:O	Yes [ ] No [ ] N/A [ ]
*10P	Implementation of the 10PASS-TS PMA/PMD	45.2.1.4		O	Yes [ ] No [ ]
*2B	Implementation of the 2BASE-TL PMA/PMD	45.2.1.4		O	Yes [ ] No [ ]

45.5.5.3 PMA/PMD management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MM1	Device responds to all register addresses for that device	45.2		PMA:M	Yes [ ] N/A [ ]
MM2	Writes to undefined and read-only registers have no effect	45.2		PMA:M	Yes [ ] N/A [ ]
MM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		PMA:M	Yes [ ] N/A [ ]
MM4	Reserved and unsupported bits return a value of zero	45.2		PMA:M	Yes [ ] N/A [ ]
MM5	Latching low bits remain low until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM7	Latching high bits remain high until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM9	Action on reset	45.2.1.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PMA:M	Yes [ ] N/A [ ]
MM10	Return 1 until reset completed	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM11	Control and management interfaces are restored to operation within 0.5 s of reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM12	Responds to reads of bit 15 and 1.8.15:14 during reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM13	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.1.1.2		PMA:M	Yes [ ] N/A [ ]
MM14	Speed selection bits 13 and 6 are written as one	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM15	Invalid writes to speed selection bits are ignored	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM16	PMA is set into Loopback mode when bit 0 is set to a one	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM17	PMA transmit data is returned on receive path when in loopback	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]
MM18	PMA ignores writes to this bit if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM19	PMA returns a value of zero when read if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM20	Writes to status 1 register have no effect	45.2.1.2		PMA:M	Yes [ ] N/A [ ]
MM21	Receive link status implemented with latching low behavior	45.2.1.2.2		PMA:M	Yes [ ] N/A [ ]
MM22	Unique identifier is composed of OUI, model number and revision	45.2.1.3		PMA:M	Yes [ ] N/A [ ]
MM23	10G PMA/PMD type is selected using bits 2:0	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM24	10G PMA/PMD ignores writes to type selection bits that select types that it has not advertised	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM25	Writes to the status 2 register have no effect	45.2.1.7		PMA:M	Yes [ ] N/A [ ]
MM26	PMA/PMD returns a value of zero for transmit fault if it is unable to detect a transmit fault	45.2.1.7.4		PMA:M	Yes [ ] N/A [ ]
MM27	Transmit fault is implemented using latching high behavior	45.2.1.7.4		PMA*PLF:M	Yes [ ] N/A [ ]
MM28	PMA/PMD returns a value of zero for receive fault if it is unable to detect a receive fault	45.2.1.7.5		PMA*!PLF:M	Yes [ ] N/A [ ]
MM29	Receive fault is implemented using latching high behavior	45.2.1.7.5		PMA*PLF:M	Yes [ ] N/A [ ]
MM30	Writes to register 9 are ignored by device that does not implement transmit disable	45.2.1.8		PMA*!PTD:M	Yes [ ] N/A [ ]
MM31	Single wavelength device uses bit 1.9.0 for transmit disable	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM32	Single wavelength device ignores writes to bits 1 – 4 and returns a value of zero for them	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM33	Setting bit 4 to a one disables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM34	Setting bit 4 to a zero enables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM35	Setting bit 3 to a one disables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM36	Setting bit 3 to a zero enables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM37	Setting bit 2 to a one disables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM38	Setting bit 2 to a zero enables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM39	Setting bit 1 to a one disables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM40	Setting bit 1 to a zero enables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM41	Setting bit 0 to a one disables transmission	45.2.1.8.5		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM42	Setting bit 0 to a zero enables transmission	45.2.1.8.5	Only if all lane transmit disables are zero	PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM43a	Writes to the extended ability register have no effect	45.2.1.10		PMA:M	Yes [ ] N/A [ ]
MM43b	Unique identifier is composed of OUI, model number and revision	45.2.1.11		PMA:M	Yes [ ] N/A [ ]
MM46	Bit indicates link down while initializing	45.2.1.2.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM47	Bit remains a one and writing a one is ignored when link is up or initializing	45.2.1.11.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM48	Bit set to zero upon reset or upon link down	45.2.1.11.1	-O sub-types only	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM49	Bit set to one upon reset or upon link down	45.2.1.11.1	-R sub-types only	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM50	Handshake tones not sent while bit is set to zero	45.2.1.11.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM51	Writes to set unsupported modes or when link is not down are ignored	45.2.1.12.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM52	Setting bit to one to one issues a cleardown command	45.2.1.12.5		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM53	MMD clears bit to zero when cleardown command is issued or on reset	45.2.1.12.5		PMA*10P*2B:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM54	Writes ignored if link is not in "Link down (ready)" state	45.2.1.12.5	link state described in 45.2.1.13.4	PMA*10P*2B: M	Yes [ ] N/A [ ]
MM55	PMA/PMD does not respond to handshake tones while bit is set to one	45.2.1.12.6		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM56	PMA/PMD responds to hand-shake tones properly when bit is set to zero	45.2.1.12.6		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM57	Bit set to zero upon MMD reset	45.2.1.12.6		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM58	Writes to set unsupported modes are ignored	45.2.1.12.7		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM59	Bits zero when link is down or initializing	45.2.1.12.1		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM60	Bits set indicate linked port type or link status	45.2.1.13.4		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM61	Bits indicate 001 while link is initializing	45.2.1.13.4		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM62	Bits indicate 000 when link is down and handshake tones are not detected	45.2.1.13.4		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM63	Bits indicate 100 when link is down and handshake tones are detected	45.2.1.13.4		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM64	Bit held as one during opera-tion, clears to zero after	45.2.1.13.1		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM65	Result = failed after 10 second timeout	45.2.1.13.1		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM66	Writes to one while link is down are marked completed and failed	45.2.1.13.1		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM67	Bit held as one during opera-tion, clears to zero after	45.2.1.13.2		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM68	Result = failed after 10 second timeout	45.2.1.13.2		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM69	Writes to one while link is down are marked completed and failed	45.2.1.13.2		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM70	Bit set to result of the "Get" operation	45.2.1.15.1		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM71	Bit set to zero on read or reset	45.2.1.15.1		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM72	Bit set to result of the "Send "operation	45.2.1.15.2		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM73	Bits are reset to zero when read or on reset	45.2.1.16		PMA*10P*2B: M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM74	Bits are held to all ones upon counter overflow	45.2.1.16		PMA*10P*2B: M	Yes [ ] N/A [ ]
MM75	Bits are reset to zero when read or reset	45.2.1.23		PMA*10P:M	Yes [ ] N/A [ ]
MM76	Bits are reset to zero when read or reset	45.2.1.24		PMA*10P:M	Yes [ ] N/A [ ]
MM77	Bits are held at all ones when PHY cannot determine value	45.2.1.27.1	ex: While link is down	PMA*10P:M	Yes [ ] N/A [ ]
MM78	Bit remain as one while tones are being refreshed	45.2.1.37.1		PMA*10P:M	Yes [ ] N/A [ ]
MM79	Bit set to zero when operation completes or upon reset	45.2.1.37.1		PMA*10P:M	Yes [ ] N/A [ ]
MM80	Bit remain as one while tones are being activated/deactivated	45.2.1.37.2		PMA*10P:M	Yes [ ] N/A [ ]
MM81	Bit set to zero when operation completes or upon reset	45.2.1.37.2		PMA*10P:M	Yes [ ] N/A [ ]
MM82	Bit remain as one while tone direction is being changed	45.2.1.37.3		PMA*10P:M	Yes [ ] N/A [ ]
MM83	Bit set to zero when operation completes or upon reset	45.2.1.37.3		PMA*10P:M	Yes [ ] N/A [ ]
MM84	Bit remain as one while SNR margins parameters are loaded	45.2.1.37.4		PMA*10P:M	Yes [ ] N/A [ ]
MM85	Bit set to zero when operation completes or upon reset	45.2.1.37.4		PMA*10P:M	Yes [ ] N/A [ ]
MM86	Bit remain as one while PSD level is set	45.2.1.37.5		PMA*10P:M	Yes [ ] N/A [ ]
MM87	Bit set to zero when operation completes or upon reset	45.2.1.37.5		PMA*10P:M	Yes [ ] N/A [ ]
MM88	Bit remain as one while reference PSD level is set	45.2.1.37.6		PMA*10P:M	Yes [ ] N/A [ ]
MM89	Bit set to zero when operation completes or upon reset	45.2.1.37.6		PMA*10P:M	Yes [ ] N/A [ ]
MM90	Bits are reset to zero when read or upon reset	45.2.1.38.1		PMA*10P:M	Yes [ ] N/A [ ]
MM91	Bits read as zero	45.2.1.39.6		PMA*10P:M	Yes [ ] N/A [ ]
MM92	Bits read as zero	45.2.1.39.7		PMA*10P:M	Yes [ ] N/A [ ]
MM93	Writes to an invalid value are ignored	45.2.1.41	Valid values are decimal 10, 20, or 40	PMA*10P:M	Yes [ ] N/A [ ]
MM94	Bits set to default value on MMD reset	45.2.1.41	Default value is decimal 20	PMA*10P:M	Yes [ ] N/A [ ]
MM95	Writes to set an invalid value are ignored	45.2.1.44.1	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM96	Writes to set an invalid value are ignored	45.2.1.44.2	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM97	Writes to set an invalid value are ignored	45.2.1.44.3	Valid values are decimal 1through 86	PMA*10P:M	Yes [ ] N/A [ ]
MM98	Writes to set an invalid value are ignored	45.2.1.44.5	Invalid value is 11	PMA*10P:M	Yes [ ] N/A [ ]
MM99	Bits set to zero when read or reset	45.2.1.45		PMA*2B:M	Yes [ ] N/A [ ]
MM100	Bits set to zero when read or reset	45.2.1.47		PMA*2B:M	Yes [ ] N/A [ ]
MM101	Bits set to zero when read or reset	45.2.1.49		PMA*2B:M	Yes [ ] N/A [ ]
MM102	Bits set to zero when read or reset	45.2.1.51		PMA*2B:M	Yes [ ] N/A [ ]
MM103	Bits set to zero when read or reset	45.2.1.53		PMA*2B:M	Yes [ ] N/A [ ]
MM104	Writes to set an invalid value are ignored	45.2.1.58.1	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM105	Writes to set an invalid value are ignored	45.2.1.58.2	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM106	Writes to set an invalid value are ignored	45.2.1.58.3	Valid values are decimal 1through 86	PMA*10P:M	Yes [ ] N/A [ ]
MM107	Writes to set an invalid value are ignored	45.2.1.58.5	Invalid value is 11	PMA*10P:M	Yes [ ] N/A [ ]

45.5.5.4 WIS options

Item	Feature	Subclause	Value/Comment	Status	Support
*WPT	Implementation of PRBS31 pattern testing	45.2.2		WIS:O	Yes [ ] No [ ] N/A [ ]

45.5.5.5 WIS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
WM1	Device responds to all register addresses for that device	45.2		WIS:M	Yes [ ] N/A [ ]
WM2	Writes to undefined and read-only registers have no effect	45.2		WIS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
WM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		WIS:M	Yes [ ] N/A [ ]
WM4	Reserved and unsupported bits return a value of zero	45.2		WIS:M	Yes [ ] N/A [ ]
WM5	Latching low bits remain low until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM7	Latching high bits remain high until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM9	Action on reset	45.2.2.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	WIS:M	Yes [ ] N/A [ ]
WM10	Return 1 until reset completed	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM11	Reset completes within 0.5 s	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM12	Responds to reads of bits 2.0.15 and 2.8.15:14 during reset	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM13	Loopback mode	45.2.2.1.2	Whenever bit 2.0.14 is set to a one	WIS:M	Yes [ ] N/A [ ]
WM14	Data received from PMA ignored during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM15	Transmit data returned on receive path during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.2.1.3		WIS:M	Yes [ ] N/A [ ]
WM17	Speed selection bits 13 and 6 are written as one	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM18	Invalid writes to speed selection bits are ignored	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM19	Writes to status 1 register have no effect	45.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM20	Fault bit implemented using latching high behavior	45.2.2.2.1		WIS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
WM21	Link status bit implemented using latching low behavior	45.2.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM22	Unique identifier is composed of OUI, model number and revision	45.2.2.3		WIS:M	Yes [ ] N/A [ ]
WM23	Setting bit 2.7.5 to a one enables PRBS31 receive pattern testing if bit 2.8.1 is a one and bit 2.7.2 is not a one	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM24	Setting bit 2.7.5 to a zero disables PRBS31 receive pattern testing	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM25	Setting bit 2.7.4 to a one enables PRBS31 transmit pattern testing if bit 2.8.1 is a one and bit 2.7.1 is not a one	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM26	Setting bit 2.7.4 to a zero disables PRBS31 transmit pattern testing	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM27	Setting bit 3 to one selects the square wave test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM28	Setting bit 3 to zero selects the pseudo random test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM29	Setting bit 2 to one enables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM30	Setting bit 2 to zero disables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM31	Setting bit 1 to one enables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM32	Setting bit 1 to zero disables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM33	Setting bit 0 to a one enables 10GBASE-W logic and sets interface speed	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM34	Setting bit 0 to a zero disables 10GBASE-W logic, sets interface speed. and bypasses data	45.2.2.6.6		WIS:O	Yes [ ] N/A [ ]
WM35	Writes to bit are ignored by WIS not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM36	Bit returns one when read if WIS is not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM37	Writes to status 2 register have no effect	45.2.2.7		WIS:M	Yes [ ] N/A [ ]
WM38	Counter is reset to all zeros when read or reset	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
WM39	Counter is held at all ones at overflow	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]
WM40	Unique identifier is composed of OUI, model number and revision	45.2.2.9		WIS:M	Yes [ ] N/A [ ]
WM41	Writes to Status 3 register have no effect	45.2.2.10		WIS:M	Yes [ ] N/A [ ]
WM42	SEF bit implemented using latching high behavior	45.2.2.10.1		WIS:M	Yes [ ] N/A [ ]
WM43	Far end PLM-P/LCD-P bit implemented using latching high behavior	45.2.2.10.2		WIS:M	Yes [ ] N/A [ ]
WM44	Far end AIS-P/LOP-P bit implemented using latching high behavior	45.2.2.10.3		WIS:M	Yes [ ] N/A [ ]
WM45	LOF bit implemented using latching high behavior	45.2.2.10.4		WIS:M	Yes [ ] N/A [ ]
WM46	LOS bit implemented using latching high behavior	45.2.2.10.5		WIS:M	Yes [ ] N/A [ ]
WM47	RDI-L bit implemented using latching high behavior	45.2.2.10.6		WIS:M	Yes [ ] N/A [ ]
WM48	AIS-L bit implemented using latching high behavior	45.2.2.10.7		WIS:M	Yes [ ] N/A [ ]
WM49	LCD-P bit implemented using latching high behavior	45.2.2.10.8		WIS:M	Yes [ ] N/A [ ]
WM50	PLM-P bit implemented using latching high behavior	45.2.2.10.9		WIS:M	Yes [ ] N/A [ ]
WM51	AIS-P bit implemented using latching high behavior	45.2.2.10.10		WIS:M	Yes [ ] N/A [ ]
WM52	LOP-P bit implemented using latching high behavior	45.2.2.10.11		WIS:M	Yes [ ] N/A [ ]

45.5.5.6 PCS options

Item	Feature	Subclause	Value/Comment	Status	Support
*CR	Implementation of 10GBASE-R PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*CX	Implementation of 10GBASE-X PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*CT	Implementation of 10GBASE-T PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*XP	Implementation of 10GBASE-X pattern testing	45.2.3		PCS* CX:O	Yes [ ] No [ ] N/A [ ]
*PPT	Implementation of PRBS31 pattern testing	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*EPC	Implementation of the 10BASE-TS/2BASE-TL PCS	45.2.3.17		PCS:O	Yes [ ] No [ ] N/A [ ]
*PAF	Implementation of the PME aggregation function	45.2.3.17		PCS*EPC:O	Yes [ ] No [ ] N/A [ ]

Add row for *CT and all associated text.

Add "or 10GBASE-T" to row item RM15 & RM16. Add row items RM77-92 and all associated text with those rows.

45.5.5.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Device responds to all register addresses for that device	45.2		PCS:M	Yes [ ] N/A [ ]
RM2	Writes to undefined and read-only registers have no effect	45.2		PCS:M	Yes [ ] N/A [ ]
RM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PCS:M	Yes [ ] N/A [ ]
RM4	Reserved and unsupported bits return a value of zero	45.2		PCS:M	Yes [ ] N/A [ ]
RM5	Latching low bits remain low until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM7	Latching high bits remain high until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM9	Action on reset	45.2.3.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PCS:M	Yes [ ] N/A [ ]
RM10	Return 1 until reset completed	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM11	Reset completes within 0.5 s	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM12	Device responds to reads of register bits 3.0.15 and 3.5.15:14 during reset	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM13	Loopback mode	45.2.3.1.2	Whenever bit 3.0.14 is set to a one	PCS:M	Yes [ ] N/A [ ]
RM14	Transmit data is returned on the receive path during loopback	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM15	Writes to loopback bit are ignored when operating at 10 Gb/s with port type selections other than 10GBASE-R or 10GBASE-T	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM16	Loopback bit returns zero when operating at 10 Gb/s with port type selections other than 10GBASE-R or 10GBASE-T	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM17	Device responds to transactions necessary to exit low-power mode while in low- power state	45.2.3.1.3		PCS:M	Yes [ ] N/A [ ]
RM18	Speed selection bits 13 and 6 are written as one	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM19	Invalid writes to speed selection bits are ignored	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM20	Writes to PCS status 1 register have no effect	45.2.3.2		PCS:M	Yes [ ] N/A [ ]
RM21	Receive link status implemented using latching low behavior	45.2.3.2.2		PCS:M	Yes [ ] N/A [ ]
RM22	Unique identifier is composed of OUI, model number and revision	45.2.3.3		PCS:M	Yes [ ] N/A [ ]
RM23	PCS type is selected using bits 1 through 0	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM24	Writes to the type selection bits that select types that have not been advertised are ignored	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM25	Writes to PCS status 2 register have no effect	45.2.3.7		PCS:M	Yes [ ] N/A [ ]
RM26	Transmit fault implemented with latching high behavior	45.2.3.7.2		PCS:M	Yes [ ] N/A [ ]
RM27	Receive fault implemented with latching high behavior	45.2.3.7.3		PCS:M	Yes [ ] N/A [ ]
RM28	Unique identifier is composed of OUI, model number and revision	45.2.3.8		PCS:M	Yes [ ] N/A [ ]
RM29	Writes to 10GBASE-X PCS status register have no effect	45.2.3.9		PCS* CX:M	Yes [ ] N/A [ ]
RM30	Register returns zero if the PCS does not implement the 10GBASE-X port type	45.2.3.9		PCS* !CX:M	Yes [ ] N/A [ ]
RM31	Writes to bit are ignored and reads return a value of zero	45.2.3.10.1		PCS* PX:M	Yes [ ] N/A [ ]
RM32	Setting the bits to <10> selects the mixed frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM33	Setting the bits to <01> selects the low-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM34	Setting the bits to <00> selects the high-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM35	Writes to 10GBASE-R PCS status 1 register have no effect	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM36	Reads from 10GBASE-R PCS status 1 register return zero for PCS that does not support 10GBASE-R	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM37	Writes to 10GBASE-R PCS status 2 register have no effect	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM38	Reads from 10GBASE-R PCS status 2 register return zero for PCS that does not support 10GBASE-R	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM39	Latched block lock implemented with latching low behavior	45.2.3.12.1		PCS* CR:M	Yes [ ] N/A [ ]
RM40	Latched high BER implemented with latching high behavior	45.2.3.12.2		PCS* CR:M	Yes [ ] N/A [ ]
RM41	BER counter clears to zero on read or reset	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM42	BER counter holds at all ones at overflow	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM43	Errored blocks counter implemented as a non roll over counter	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM44	Errored blocks counter clears to zero on read	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM45	Setting bit 3.42.5 to a one enables PRBS31 receive pattern testing if bit 3.32.2 is a one and bit 3.42.2 is not a one	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM46	Setting bit 3.42.5 to a zero disables PRBS31 receive pattern testing	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM47	Setting bit 3.42.4 to a one enables PRBS31 transmit pattern testing if bit 3.32.2 is a one and bit 3.42.3 is not a one	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM48	Setting bit 3.42.4 to a zero disables PRBS31 transmit pattern testing	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM49	Test-pattern error counter clears to zero on read or reset	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]
RM50	Test-pattern error counter holds at all ones at overflow	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]
RM51	Bit indicates fault when any PCS register indicates fault	45.2.3.2.1	If sub-type is supported	PCS*EPC:O	Yes [ ] No [ ] N/A [ ]
RM52	Writes to bit 15 are ignored	45.2.3.17	If sub-type is unsupported	PCS*EPC:O	Yes [ ] No [ ] N/A [ ]
RM53	Writing this bit to a one activates the PAF when link is established	45.2.3.18.3		PCS*PAF:M	Yes [ ] N/A [ ]
RM54	Writes to bit are ignored while link is active or initializing or if PAF is not supported	45.2.3.18.3		PCS*PAF:M	Yes [ ] N/A [ ]
RM55	Bits indicate device capabilities upon reset	45.2.3.19		PCS*PAF:M	Yes [ ] N/A [ ]
RM56	Writes to the register through any PCS MMD in the same package effect the register equally	45.2.3.19		PCS*PAF:M	Yes [ ] N/A [ ]
RM57	Single bit set to one and all others cleared to zero when device does not support aggregation of multiple PMEs	45.2.3.19		PCS:M	Yes [ ] N/A [ ]
RM58	PME aggregation used if one or more bits set	45.2.3.20		PCS*PAF:M	Yes [ ] N/A [ ]
RM59	Registers set to all zeros upon reset	45.2.3.20		PCS*PAF:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM60	Writes to the register through any PCS MMD in the same package effect the register equally	45.2.3.20		PCS*PAF:M	Yes [ ] N/A [ ]
RM61	Bits reset to zero when read of upon MMD reset	45.2.3.21		PCS*PAF:M	Yes [ ] N/A [ ]
RM62	Bits held to one upon overflow	45.2.3.21		PCS*PAF:M	Yes [ ] N/A [ ]
RM63	Bits reset to zero when read of upon MMD reset	45.2.3.22		PCS*PAF:M	Yes [ ] N/A [ ]
RM64	Bits held to one upon overflow	45.2.3.22		PCS*PAF:M	Yes [ ] N/A [ ]
RM65	Bits reset to zero when read of upon MMD reset	45.2.3.23		PCS*PAF:M	Yes [ ] N/A [ ]
RM66	Bits held to one upon overflow	45.2.3.23		PCS*PAF:M	Yes [ ] N/A [ ]
RM67	Bits reset to zero when read of upon MMD reset	45.2.3.24		PCS*PAF:M	Yes [ ] N/A [ ]
RM68	Bits held to one upon overflow	45.2.3.24		PCS*PAF:M	Yes [ ] N/A [ ]
RM69	Bits reset to zero when read of upon MMD reset	45.2.3.25		PCS*PAF:M	Yes [ ] N/A [ ]
RM70	Bits held to one upon overflow	45.2.3.25		PCS*PAF:M	Yes [ ] N/A [ ]
RM71	Bits reset to zero when read of upon MMD reset	45.2.3.26		PCS*PAF:M	Yes [ ] N/A [ ]
RM72	Bits held to one upon overflow	45.2.3.26		PCS*PAF:M	Yes [ ] N/A [ ]
RM73	Bits reset to zero when read of upon MMD reset	45.2.3.27		PCS*PAF:M	Yes [ ] N/A [ ]
RM74	Bits held to one upon overflow	45.2.3.27		PCS*PAF:M	Yes [ ] N/A [ ]
RM75	Bits reset to zero when read of upon MMD reset	45.2.3.28		PCS*PAF:M	Yes [ ] N/A [ ]
RM76	Bits held to one upon overflow	45.2.3.28		PCS*PAF:M	Yes [ ] N/A [ ]
RM77	Writes to 10GBASE-T PCS status 1 register have no effect	45.2.3.30		PCS* CT:M	Yes [ ] N/A [ ]
RM78	Reads from 10GBASE-T PCS status 1 register return zero for PCS that does not support 10GBASE-T	45.2.3.30		PCS* CT:M	Yes [ ] N/A [ ]
RM79	Writes to 10GBASE-T PCS status 2 register have no effect	45.2.3.31		PCS* CT:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM80	Reads from 10GBASE-T PCS status 2 register return zero for PCS that does not support 10GBASE-T	45.2.3.31		PCS* CT:M	Yes [ ] N/A [ ]
RM81	PCS lock implemented with latching low behavior	45.2.3.31.1		PCS* CT:M	Yes [ ] N/A [ ]
RM82	High BER implemented with latching high behavior	45.2.3.31.2		PCS* CT:M	Yes [ ] N/A [ ]
RM83	BER counter clears to zero on read or reset	45.2.3.31.3		PCS* CT:M	Yes [ ] N/A [ ]
RM84	BER counter holds at all ones at overflow	45.2.3.31.3		PCS* CT:M	Yes [ ] N/A [ ]
RM85	Errored blocks counter implemented as a non roll over counter	45.2.3.31.4		PCS* CT:M	Yes [ ] N/A [ ]
RM86	Errored blocks counter clears to zero on read	45.2.3.31.4		PCS* CT:M	Yes [ ] N/A [ ]
RM87	Setting bit 3.80.5 to a one enables PRBS31 receive pattern testing if bit 3.81.2 is a one	45.2.3.29.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM88	Setting bit 3.80.5 to a zero disables PRBS31 receive pattern testing	45.2.3.29.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM89	Setting bit 3.80.4 to a one enables PRBS31 transmit pattern testing if bit 3.81.2 is a one	45.2.3.29.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM90	Setting bit 3.80.4 to a zero disables PRBS31 transmit pattern testing	45.2.3.29.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM91	PRBS31 error counter clears to zero on read or reset	45.2.3.32		PCS* CT:M	Yes [ ] N/A [ ]
RM92	PRBS31 error counter holds at all ones at overflow	45.2.3.32		PCS* CT:M	Yes [ ] N/A [ ]

45.5.5.8 PHY XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*PL	Implementation of loopback	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]
*PT	Implementation of pattern testing	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]

45.5.5.9 PHY XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Device responds to all register addresses for that device	45.2		PX:M	Yes [ ] N/A [ ]
PM2	Writes to undefined and read-only registers have no effect	45.2		PX:M	Yes [ ] N/A [ ]
PM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PX:M	Yes [ ] N/A [ ]
PM4	Reserved and unsupported bits return a value of zero	45.2		PX:M	Yes [ ] N/A [ ]
PM5	Latching low bits remain low until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM7	Latching high bits remain high until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM9	Action on reset	45.2.4.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PX:M	Yes [ ] N/A [ ]
PM10	Return 1 until reset completed	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM11	Reset completes within 0.5 s	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM12	Device responds to reads of bits 4.0.15 and 4.8.15:14 during reset	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM13	Loopback mode	45.2.4.1.2	Whenever bit 4.0.14 is set to a one	PX*PL:M	Yes [ ] N/A [ ]
PM14	Receive data is returned on transmit path during loopback	45.2.4.1.2		PX*PL:M	Yes [ ] N/A [ ]
PM15	Writes to loopback bit are ignored and reads return zero	45.2.4.1.2		PX*!PL:M	Yes [ ] N/A [ ]
PM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.4.1.3		PX:M	Yes [ ] N/A [ ]
PM17	Speed selection bits 13 and 6 are written as one	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PM18	Invalid writes to speed selection bits are ignored	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]
PM19	Writes to status 1 register have no effect	45.2.4.2		PX:M	Yes [ ] N/A [ ]
PM20	Transmit link status implemented using latching low behavior	45.2.4.2.2		PX:M	Yes [ ] N/A [ ]
PM21	Unique identifier is composed of OUI, model number and revision	45.2.4.3		PX:M	Yes [ ] N/A [ ]
PM22	Writes to status 2 register have no effect	45.2.4.6		PX:M	Yes [ ] N/A [ ]
PM23	Transmit fault implemented with latching high behavior	45.2.4.6.2		PX:M	Yes [ ] N/A [ ]
PM24	Receive fault implemented with latching high behavior	45.2.4.6.3		PX:M	Yes [ ] N/A [ ]
PM25	Unique identifier is composed of OUI, model number and revision	45.2.4.7		PX:M	Yes [ ] N/A [ ]
PM26	Writes to 10G PHY XGXS Lane status register have no effect	45.2.4.8		PX:M	Yes [ ] N/A [ ]
PM27	Writes to bit are ignored and reads return a value of zero	45.2.4.9.1		PX*!PT:M	Yes [ ] N/A [ ]
PM28	Setting the bits to <10> selects the mixed frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM29	Setting the bits to <01> selects the low-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM30	Setting the bits to <00> selects the high-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]

45.5.5.10 DTE XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*DT	Implementation of pattern testing	45.2.5		DX:O	Yes [ ] No [ ] N/A [ ]

45.5.5.11 DTE XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
DM1	Device responds to all register addresses for that device	45.2		DX:M	Yes [ ] N/A [ ]
DM2	Writes to undefined and read-only registers have no effect	45.2		DX:M	Yes [ ] N/A [ ]
DM3	Operation is not affected by writes to reserved and unsupported bits	45.2		DX:M	Yes [ ] N/A [ ]
DM4	Reserved and unsupported bits return a value of zero	45.2		DX:M	Yes [ ] N/A [ ]
DM5	Latching low bits remain low until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM7	Latching high bits remain high until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM9	Action on reset	45.2.5.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	DX:M	Yes [ ] N/A [ ]
DM10	Return 1 until reset completed	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM11	Reset completes within 0.5 s	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM12	Device responds to reads of bits 5.0.15 and 5.8.15:14 during reset	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM13	Loopback mode	45.2.5.1.2	Whenever bit 5.0.14 is set to a one	DX:M	Yes [ ] N/A [ ]
DM14	Transmit data is returned on receive path during loopback	45.2.5.1.2		DX:M	Yes [ ] N/A [ ]
DM15	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.5.1.3		DX:M	Yes [ ] N/A [ ]
DM16	Speed selection bits 13 and 6 are written as one	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM17	Invalid writes to speed selection bits are ignored	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM18	Writes to status 1 register have no effect	45.2.5.2		DX:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
DM19	Receive link status implemented using latching low behavior	45.2.5.2.2		DX:M	Yes [ ] N/A [ ]
DM20	Unique identifier is composed of OUI, model number and revision	45.2.5.3		DX:M	Yes [ ] N/A [ ]
DM21	Writes to status 2 register have no effect	45.2.5.6		DX:M	Yes [ ] N/A [ ]
DM22	Transmit fault implemented with latching high behavior	45.2.5.6.2		DX:M	Yes [ ] N/A [ ]
DM23	Receive fault implemented with latching high behavior	45.2.5.6.3		DX:M	Yes [ ] N/A [ ]
DM24	Unique identifier is composed of OUI, model number and revision	45.2.5.7		DX:M	Yes [ ] N/A [ ]
DM25	Writes to 10G DTE XGXS Lane status register have no effect	45.2.5.8		DX:M	Yes [ ] N/A [ ]
DM26	Writes to bit are ignored and reads return a value of zero	45.2.5.9.1		DX*!DT:M	Yes [ ] N/A [ ]
DM27	Setting the bits to <10> selects the mixed frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM28	Setting the bits to <01> selects the low-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM29	Setting the bits to <00> selects the high-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]

45.5.5.12 Vendor specific MMD 1 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSA1	Device responds to all register addresses for that device	45.2		VSA:M	Yes [ ] N/A [ ]
VSA2	Writes to undefined and read-only registers have no effect	45.2		VSA:M	Yes [ ] N/A [ ]
VSA3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSA:M	Yes [ ] N/A [ ]
VSA4	Reserved and unsupported bits return a value of zero	45.2		VSA:M	Yes [ ] N/A [ ]
VSA5	Unique identifier is composed of OUI, model number and revision	45.2.8.1		VSA:M	Yes [ ] N/A [ ]
VSA6	Writes to status register have no effect	45.2.8.2		VSA:M	Yes [ ] N/A [ ]
VSA7	Unique identifier is composed of OUI, model number and revision	45.2.8.3		VSA:M	Yes [ ] N/A [ ]

45.5.5.13 Vendor specific MMD 2 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSB1	Device responds to all register addresses for that device	45.2		VSB:M	Yes [ ] N/A [ ]
VSB2	Writes to undefined and read-only registers have no effect	45.2		VSB:M	Yes [ ] N/A [ ]
VSB3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSB:M	Yes [ ] N/A [ ]
VSB4	Reserved and unsupported bits return a value of zero	45.2		VSB:M	Yes [ ] N/A [ ]
VSB5	Unique identifier is composed of OUI, model number and revision	45.2.9.1		VSB:M	Yes [ ] N/A [ ]
VSB6	Writes to status register have no effect	45.2.9.2		VSB:M	Yes [ ] N/A [ ]
VSB7	Unique identifier is composed of OUI, model number and revision	45.2.9.3		VSB:M	Yes [ ] N/A [ ]

45.5.5.14 Management frame structure

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Device has implemented sixteen bit address register	45.3		M	Yes [ ]
MF2	Address register is overwritten by address frames	45.3		M	Yes [ ]
MF3	Write, read, and post-read-increment-address frames access the register whose address is held in the address register	45.3		M	Yes [ ]
MF4	Write and read frames do not modify the address register	45.3		M	Yes [ ]
MF5	Post-read-increment-address frames increment the address register by one unless the address register contains 65 535	45.3		M	Yes [ ]
MF6	Components containing several MMDs implement separate address registers	45.3		M	Yes [ ]
MF7	Tri state drivers are disabled during idle	45.3.1		M	Yes [ ]
MF8	STA sources 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF9	MMD observes 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF10	Frames containing ST=<01> sequence are ignored	45.3.3		M	Yes [ ]
MF11	STA tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF12	MMD tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF13	MMD tri state driver drives a zero bit during second bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF14	STA tri state driver drives a one bit followed by a zero bit for the TA during write or address frames	45.3.7		M	Yes [ ]
MF15	First bit transmitted and received is bit 15	45.3.8		M	Yes [ ]

45.5.5.15 TC management functions

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Device responds to all register addresses for that device	45.2		TC:M	Yes [ ] N/A [ ]
TC2	Writes to undefined and read only register have no effect	45.2		TC:M	Yes [ ] N/A [ ]
TC3	Operation is not affected by writes to reserved and unsupported bits	45.2		TC:M	Yes [ ] N/A [ ]
TC4	Reserved and unsupported bits return a value of zero	45.2		TC:M	Yes [ ] N/A [ ]
TC5	Setting bit to a one sets all TC registers to their default states	45.2.1.1.1		TC:M	Yes [ ] N/A [ ]
TC6	Bit reads one while reset is in progress otherwise reads zero	45.2.1.1.1		TC:M	Yes [ ] N/A [ ]
TC7	Control and management interface is restored within 0.5s from setting bit to a one	45.2.1.1.1		TC:M	Yes [ ] N/A [ ]
TC8	During reset, TC responds to reads from bit	45.2.1.1.1		TC:M	Yes [ ] N/A [ ]
TC9	Writes that would select an unsupported ability are ignored	45.2.1.1.3		TC:M	Yes [ ] N/A [ ]
TC10	Identifier composed properly	45.2.6.2		TC:M	Yes [ ] N/A [ ]
TC11	Identifier composed properly	45.2.6.5		TC:M	Yes [ ] N/A [ ]
TC12	Register is unique across all PCS MMDs in a package	45.2.6.6		TC:M	Yes [ ] N/A [ ]
TC13	Operation ignored when link is up or initializing	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC14	Bits indicate “Ready” when PAF is capable	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC15	Writes ignored and “Ready” indicated if PAF is unsupported	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC16	Bits indicate “Ready” when operation is complete or upon reset	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC17	Bits read as zero if PAF is unsupported	45.2.6.7.1		TC:M	Yes [ ] N/A [ ]
TC18	Bits read as zero if PAF is unsupported	45.2.6.7.2		TC:M	Yes [ ] N/A [ ]
TC19	Register is unique across all PCS MMDs in a package	45.2.6.8		TC:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC20	Register is unique across all PCS MMDs in a package	45.2.6.9		TC:M	Yes [ ] N/A [ ]
TC21	Operation ignored when link is up or initializing	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC22	Bits indicate “Ready” when PAF is capable	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC23	Writes ignored and “Ready” indicated if PAF is unsupported	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC24	Bits indicate “Ready” when operation is complete or on reset	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC25	Register is unique across all PCS MMDs in a package	45.2.6.10		TC:M	Yes [ ] N/A [ ]
TC26	Bits reset to zero when read or reset	45.2.6.11		TC:M	Yes [ ] N/A [ ]
TC27	Bits held to one upon overflow	45.2.6.11		TC:M	Yes [ ] N/A [ ]
TC28	Bits reset to zero when read or reset	45.2.6.12		TC:M	Yes [ ] N/A [ ]
TC29	Bits held to one upon overflow	45.2.6.12		TC:M	Yes [ ] N/A [ ]

45.5.5.16 Clause 22 extension options

Item	Feature	Subclause	Value/Comment	Status	Support
*FEC	Implementation of PHY FEC	65.4.4.6		CTT:O	Yes [ ] No [ ] N/A [ ]

45.5.5.17 Clause 22 extension management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CT1	Device responds to all register addresses for that device	45.2		CTT:M	Yes [ ] N/A [ ]
CT2	Writes to undefined and read only register have no effect	45.2		CTT:M	Yes [ ] N/A [ ]
CT3	Operation is not affected by writes to reserved and unsupported bits	45.2		CTT:M	Yes [ ] N/A [ ]
CT4	Reserved and unsupported bits return a value of zero	45.2		CTT:M	Yes [ ] N/A [ ]
CT5	Bits set to zero upon PHY reset	45.2.7.3.1		CTT*FEC:M	Yes [ ] N/A [ ]
CT6	Bits reset to all zeroes when the register is read by the management function or upon PHY reset.	45.2.7.4		CTT*FEC:M	Yes [ ] N/A [ ]
CT7	Bits held at all ones in the case of overflow	45.2.7.4		CTT*FEC:M	Yes [ ] N/A [ ]
CT8	Bits reset to all zeroes when the register is read by the management function or upon PHY reset.	45.2.7.5		CTT*FEC:M	Yes [ ] N/A [ ]
CT9	Bits held at all ones in the case of overflow	45.2.7.5		CTT*FEC:M	Yes [ ] N/A [ ]
CT10	Bits reset to all zeroes when the register is read by the management function or upon PHY reset.	45.2.7.6		CTT*FEC:M	Yes [ ] N/A [ ]
CT11	Bits held at all ones in the case of overflow	45.2.7.6		CTT*FEC:M	Yes [ ] N/A [ ]

45.5.5.18 Signal timing characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	MDIO setup and hold time	45.4.2	Setup min = 10 ns; Hold min = 10 ns per	M	Yes [ ]
ST2	MDIO clock to output delay	45.4.2	Min = 0 ns; Max = 300 ns per	M	Yes [ ]
ST3	MDC min high/low time	45.4.2	160 ns	M	Yes [ ]
ST4	MDC min period	45.4.2	400 ns	M	Yes [ ]

45.5.5.19 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	V_{OH}	45.4.1	≥ 1.0V (I_{OH} = –100 uA) ≤ 1.5V (I_{OH} = –100 uA)	M	Yes [ ]
EC2	V_{OL}	45.4.1	≥ –0.3V (I_{OL} = 100 uA) ≤ 0.2 V (I_{OL} = 100 uA)	M	Yes [ ]
EC3	V_{IH}	45.4.1	0.84 V ≤ V_{IH} ≤ 1.5 V	M	Yes [ ]
EC4	V_{IL}	45.4.1	–0.3 ≤ V_{IL} ≤ 0.36 V	M	Yes [ ]
EC5	Input capacitance for MDIO	45.4.1	≤ 10pF	M	Yes [ ]
EC6	Bus loading	45.4.1	≤ 470pF	M	Yes [ ]
EC7	I_{OH}	45.4.1	≤ –4mA at V_I = 1.0V	M	Yes [ ]
EC8	I_{OL}	45.4.1	≥ +4mA at V_I = 0.2V	M	Yes [ ]

55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.1 Overview

The 10GBASE-T PHY is one of the 10 Gigabit Ethernet family of high-speed CSMA/CD network specifications. The 10GBASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium specifications are intended for users who want 10 Gb/s performance over balanced twisted-pair structured cabling systems. 10GBASE-T signaling requires four pairs of balanced cabling, as specified in ISO/IEC 11801 Edition 2 with appropriate augmentation as specified in 55.7.

This clause defines the type 10GBASE-T PCS, type 10GBASE-T PMA sublayer, and type 10GBASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer define a 10GBASE-T Physical layer (PHY). Functional, electrical and mechanical specifications for the type 10GBASE-T PCS, PMA, and MDI are provided in this document. This clause also specifies the baseband medium used with 10GBASE-T.

55.1.1 Objectives

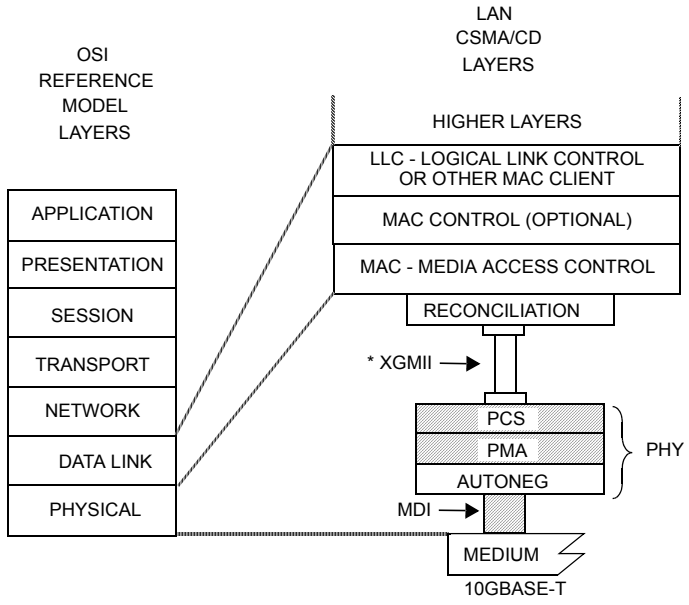
The following are the objectives of 10GBASE-T:

a) Support full duplex operation only
b) Support star-wired local area networks using point-to-point links and structured cabling topologies.
c) Support a speed of 10.000 Gb/s at the MAC/PLS service interface.
d) Support copper medium from ISO/IEC 11801:2002, with appropriate augmentation as specified in Clause 55.7
e) Support operation over 4-connector structured 4-pair, twisted copper cabling for all supported distances and Classes.
f) Define a single 10Gb/s PHY that would support links of:
    1) 100 m on four pair Class F balanced copper cabling
    2) At least 55 m to 100 m on four pair Class E balanced copper cabling
g) Preserve the 802.3/Ethernet frame format at the MAC Client service Interface.
h) Preserve minimum and maximum frame size of the current 802.3 Standard.
i) Support Auto-Negotiation (Clause 28).
j) Meet CISPR/FCC Class A EMC limits.
k) Support a Bit Error Rate of less than or equal to 10^{-12} on all supported distances and Classes

Editor's Note: When the extrapolation of the Class E specifications specified in Clause 55.7 is incorporated into the appropriate TIA/ISO/IEC specifications, we will pull in references to these in here. Frequency extrapolation of the Class E specification is already available in the TR-42 Draft Technical Report entitled "Assessment of installed class E and class F cabling performance beyond their maximum specified frequencies.

55.1.2 Relationship of 10GBASE-T to other standards

Relations between the 10GBASE-T PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 55–1. The PHY sub-layers (shown shaded) in Figure 55–1 connect one Clause 4 Media Access Control (MAC) layer to the medium.



MDI = MEDIUM DEPENDENT INTERFACE
XGMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE

*XGMII is optional.

Figure 55–1—Type 10GBASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

55.1.3 Operation of 10GBASE-T

The 10GBASE-T PHY employs full duplex baseband transmission over four pairs of balanced cabling. The aggregate data rate of 10 Gb/s is achieved by transmission at a data rate of 2500 Mb/s over each wire pair, as shown in Figure 55–2. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signaling with a modulation rate of 800 Msymbols/s is used on each of the wire pairs. The transmitted symbols are selected from a four-dimensional 16-level symbol constellation. Each four-dimensional symbol can be viewed as a 4-tuple (A_n, B_n, C_n, D_n) of one-dimensional symbols taken from the set {-15, -13, -11, -9, -7, -5, -3, -1, 1, 3, 5, 7, 9, 11, 13, 15}. 10GBASE-T uses a continuous signaling system; in the absence of data, control symbols are transmitted. Data and Control symbols are embedded in a framing scheme which runs continuously after startup of the link. The 128 2D values of a DoubleSquare (DSQ128) Modulation are employed for transmission over each wire pair. The modulation symbol rate of 800 Msymbols/s results in a symbol period of 1.25 ns.

A 10GBASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see TBD). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented, the SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter

operations, i.e., it performs loop timing, as illustrated in Figure 55–3. If loop timing is not implemented, the SLAVE PHY clocking is identical to the MASTER PHY clocking. In a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

The PCS and PMA subclauses of this document are summarized in 55.1.3.1 and 55.1.3.2. Figure 55–3 shows the functional block diagram.

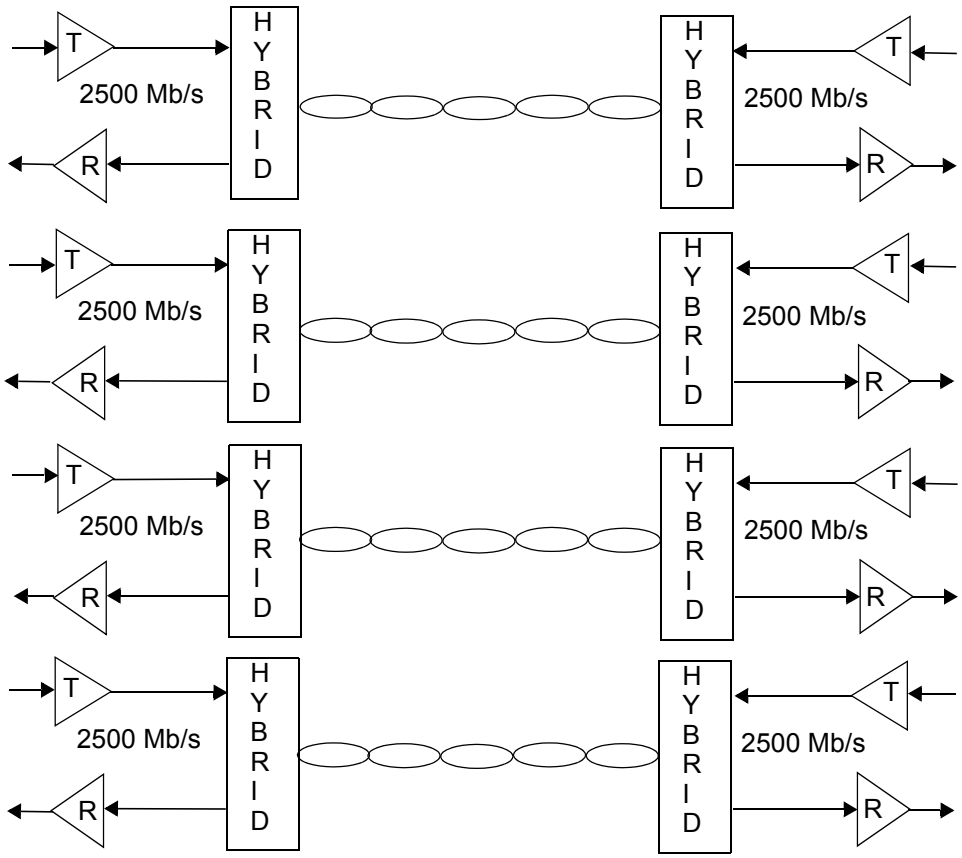


Figure 55–2—10GBASE-T topology

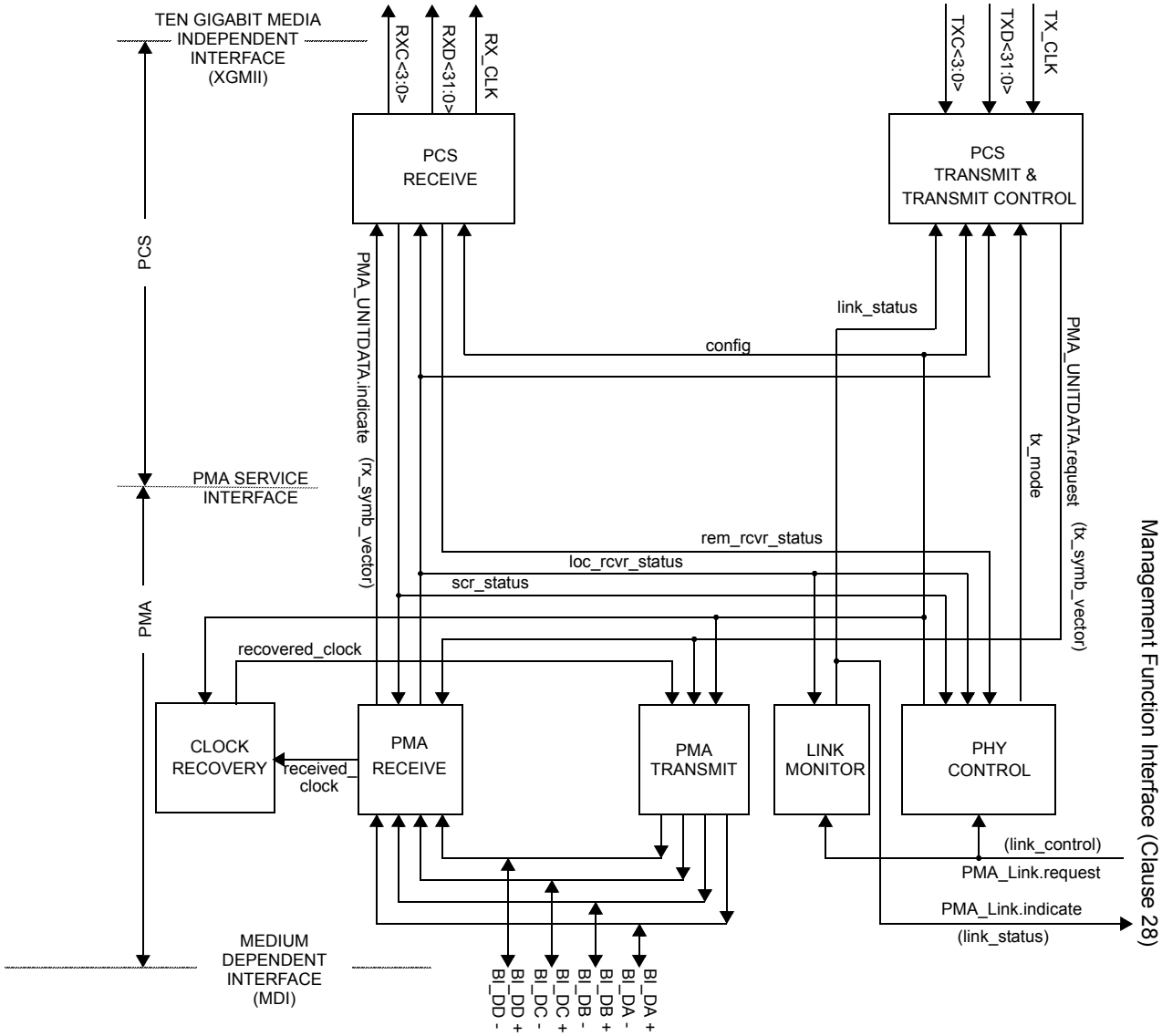


Figure 55–3—Functional block diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

55.1.3.1 Physical Coding Sublayer (PCS)

The 10GBASE-T PCS couples a Ten Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 10GBASE-T Physical Medium Attachment (PMA) sublayer.

In the transmit direction, in normal mode, the PCS takes eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the XGMII start of packet boundary as indicated by the XGMII transmit control signals (TXCn = 1). The resulting 65-bit blocks are taken in groups of 50 blocks and CRC-7 check bits are added to form a CRC-checked Ethernet data payload of 50x65+7 = 3257 bits. An auxiliary channel bit and a sync bit is added to form an LDPC transmit frame. Of the resulting 3259 bits, 1723 bits are encoded using a systematic LDPC(1723,2048) encoder, which adds 325 LDPC check bits.

The 2048 bits of the resulting LDPC codewords are divided into 512 coded 4-bit labels. Each coded 4-bit label determines one subset out of the sixteen subsets of a 2D DSQ128 symbol constellation. The 8 2D symbols in each subset are maximally spaced in a Euclidean distance sense.

The remaining 1536 bits, among them the sync bit, are left uncoded. The 1536 uncoded bits are divided into 512 uncoded 3-bit labels. Each uncoded 3-bit label selects one 2D symbol in a DSQ128 subset selected by a coded 4-bit label. In this way, a block of 512 2D DSQ128 symbols is obtained. Each DSQ128 symbol constitutes a constrained pair of two 1D PAM16 symbols which are denoted 1DSQ128. Thus a LDPC frame finally comprises of 1024 1DSQ128 symbols or equivalently 256 4D 1DSQ128

A continuous stream of four dimensional 1DSQ128 symbols is passed on the PMA via PMA_UNITDATA.request signal. The PMA transmit block operates continuously this stream of four dimensional symbols. Details of the mapping are covered in 55.3.

In the receive direction, in normal mode, the PCS processes code-groups received from the remote PHY via the PMA in 256 4D symbol blocks and maps them to the XGMII service interface in the receive path. In this receive processing scheme, symbol clock synchronization is done by the PMA receive function.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

The PCS functions and state diagrams are specified in 55.3. The signals provided by the PCS at the XGMII conform to the interface requirements of Clause 46. The PCS Service Interfaces to the XGMII and the PMA are abstract message-passing interfaces specified in 55.2.

55.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the balanced cabling physical medium via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at 800 Msymbols/s over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four transmitters to generate continuous time analog signals on each of the four pairs BI_DA, BI_DB, BI_DC and BI_DD, as described in 55.4.3.1. In normal mode, each four dimensional symbol received from the PCS transmit function undergoes multiple stages of processing. First the symbol goes through a Tomlinson Harashima Precoder (THP) which maps the 1DSQ128 input in each dimension of the four dimensional symbol into a quasi-continuous discrete time value in the range (-16, 16]. This THP processed four dimensional symbol stream is then passed on to four digital to analog converters (DACs). Each DAC outputs may be further processed with continuous time filters to roll off the high frequency spectral response to limit high frequency emissions and are then applied to the four balanced pairs via the MDI port.

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC and BI_DD, as described in 55.4.3.2. The receivers are responsible for acquiring symbol timing and, when operating in normal mode, for cancelling echo, near end cross talk, far end cross talk and equalizing the signal. The 4-D symbols are provided to the PCS receive function via the PMA_UNITDATA.indicate message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the start-up functions required for successful 10GBASE-T operation. It determines whether the PHY operates in a normal state, enabling data transmission over the link segment, or whether the PHY sends special PAM2 code-groups that are used in the training mode. The latter occurs when either one or both of the PHYs that share a link segment are not operating reliably.

PMA functions and state diagrams are specified in 55.4. PMA electrical specifications are given in 55.5.

55.1.4 Signaling

10GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including

a) Forward Error Correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to four dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.

The PHY operates in two basic modes, normal mode or training mode. In normal mode, PCS generates a continuous stream of four dimensional symbols that are transmitted via the PMA at one of eight power levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See the PCS reference diagram in 55.2.)

55.1.5 Inter-sublayer interfaces

All implementations of the balanced cabling link are compatible at the MDI. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. When the PHY is incorporated within the physical bounds of a single-port device or a multiport device, implementation of the XGMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

55.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementor.

55.2 10GBASE-T Service Primitives and Interfaces

10GBASE-T transfers data and control information across the following four service interfaces:

a) Ten Gigabit Media Independent Interface (XGMII)
b) Management Function Interface
c) PMA Service Interface
d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Management Function Interface is specified in Clause 45. The PMA Service Interface is defined in 55.2.2 and the MDI is defined in 55.8.

55.2.1 Management Function Interface

10GBASE-T uses the following service primitives to exchange status indications and control signals across the Management Function Interface as specified in Clause 28:

Editor's note: These primitives have been taken from Clause 40 (1000BASE-T). Are these valid for 10GBASE-T? If we need changes to these, please provide comments.

PMA_LINK.request (link_control)

PMA_LINK.indicate (link_status)

55.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

55.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

55.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

55.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 55.4.2.5.

55.2.1.2 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation algorithm about the status of the underlying link.

55.2.1.2.1 Semantics of the primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY(PB)	The Link Monitor function indicates that a 10GBASE-T link is intact and ready to be established.
OK(PB)	The Link Monitor function indicates that a valid 10GBASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

PB is a parameter that can take any value from 1 to 8 and indicates the power backoff levels of Ptxmax, Ptxmax-2dB, Ptxmax-4dB, Ptxmax-6dB, Ptxmax-8dB, Ptxmax-10dB, Ptxmax-12dB or Ptxmax-14dB respectively. Ptx is the nominal maximum transmit power

55.2.1.2.2 When generated

The PMA generates this primitive continuously to indicate the value of link_status in compliance with the state diagram given in Figure 55–19.

55.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is TBD.

55.2.2 PMA Service Interface

10GBASE-T uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

Editor's note: These primitives have been taken from Clause 40. Are these valid for 10GBASE-T? If we need changes to these, please provide comments.

PMA_TXMODE.indicate (tx_mode)

PMA_CONFIG.indicate (config)

PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indicate (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_RXSTATUS.indicate (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

PMA_RESET.indicate (TBD)

The use of these primitives is illustrated in Figure 55–4.

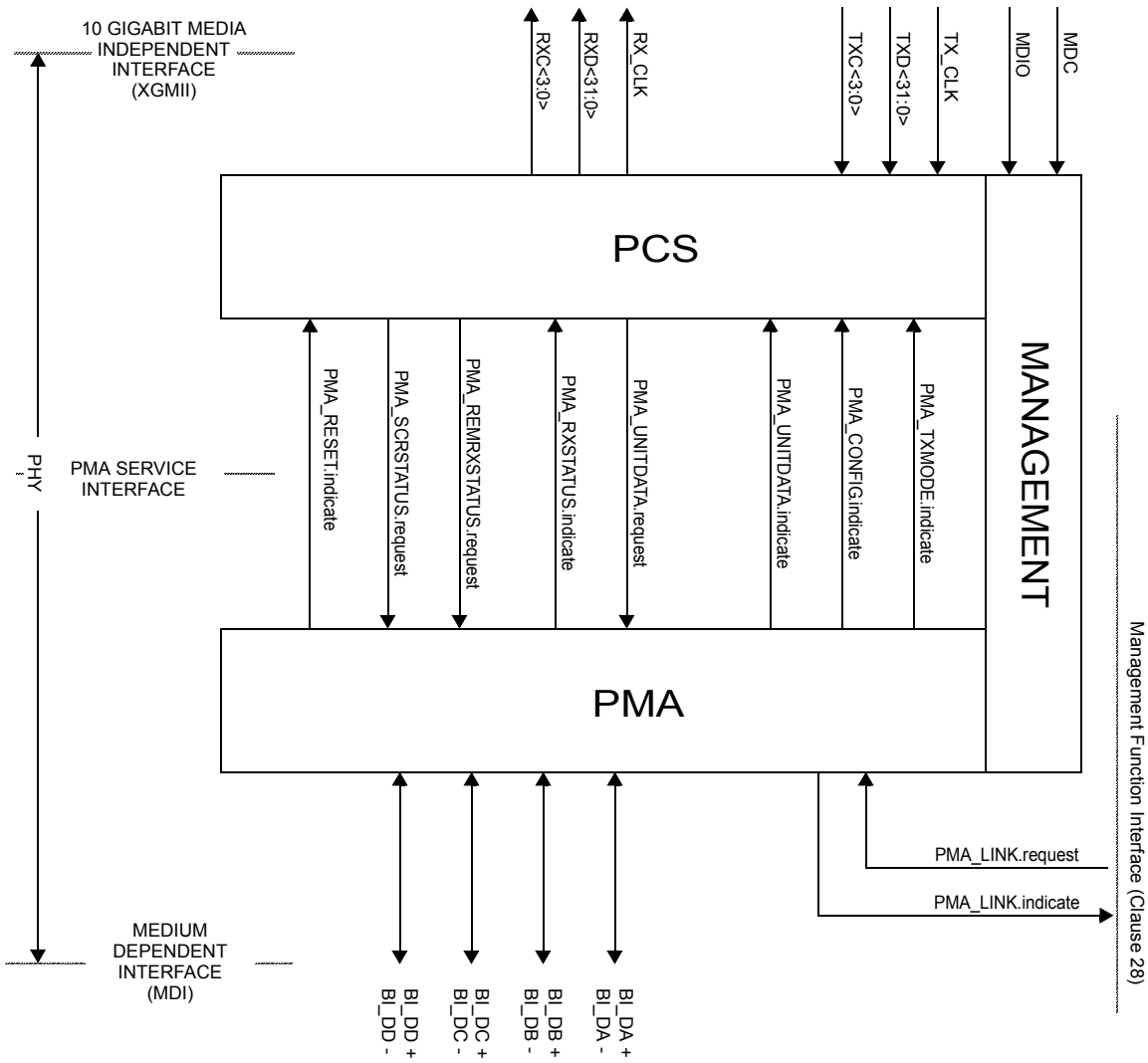


Figure 55–4—10GBASE-T service interfaces

55.2.3 PMA_TXMODE.indicate

The transmitter in a 10GBASE-T link normally sends over the four pairs, four dimensional symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

55.2.3.1 Semantics of the primitive

PMA_TXMODE.indicate (tx_mode)

PMA_TXMODE.indicate specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of four dimensional symbols representing an XGMII data stream in normal mode.

SEND_T This value is continuously asserted in case transmission of sequences of code-groups representing the startup mode is to take place.

SEND_Z This value is continuously asserted in case transmission of zeros is required.

55.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indicate messages continuously.

55.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 55.3.2.2.

55.2.4 PMA_CONFIG.indicate

Each PHY in a 10GBASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (55.6.1). The result of this negotiation is provided to the PMA.

55.2.4.1 Semantics of the primitive

PMA_CONFIG.indicate (config)

PMA_CONFIG.indicate specifies to PCS and PMA Transmit via the parameter config whether the PHY must operate as a MASTER PHY or as a SLAVE PHY and the power backoff level at which the transmitter shall operate. The parameter config can take on one of the following two values of the form:

MASTER(PB) This value is continuously asserted when the PHY must operate as a MASTER PHY.

SLAVE(PB) This value is continuously asserted when the PHY must operate as a SLAVE PHY.

PB can take any value from 1 to 8 to indicate the power backoff mode.

55.2.4.2 When generated

PMA generates PMA_CONFIG.indicate messages continuously.

55.2.4.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

55.2.5 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 55.3.2.2 to represent XGMII data and control streams or other sequences.

55.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. Each symbol may take on one of the values in the set {-15,-13,-11,-9, -7, -5, -3, -1, 1, 3, 5, 7, 9, 11,13,15}.

The symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

55.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_4D) synchronously with every transmit clock cycle.

55.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with the Tomlinson Harashima Precoder (THP), the transmit filter and other specified PMA transmit processing. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD for cancelling the echo and Near End Cross Talk (NEXT).

55.2.6 PMA_UNITDATA.indicate

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

55.2.6.1 Semantics of the primitive

PMA_UNITDATA.indicate (rx_symb_vector)

During reception the PMA_UNITDATA.indicate simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symb_vector parameter takes on the form:

SYMB_4D A vector of the four 1-D symbols that is the receiver's best estimate of the symbols that were sent by the remote transmitter across the four pairs.

55.2.6.2 When generated

The PMA generates PMA_UNITDATA.indicate(SYMB_4D) messages synchronously every 4 symbols received at the MDI. The nominal rate of the PMA_UNITDATA.indicate primitive is 800 MHz, as governed by the recovered clock.

55.2.6.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

55.2.7 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

Editor's note: Do we need to create a similar primitive to communicate status of PCS descrambler?

55.2.7.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The training mode descrambler has achieved synchronization.
NOT_OK	The training mode descrambler is not synchronized.

55.2.7.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

55.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.4.2.3, 55.4.2.4, and 55.4.6.1.

55.2.8 PMA_RXSTATUS.indicate

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams.

55.2.8.1 Semantics of the primitive

PMA_RXSTATUS.indicate (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

55.2.8.2 When generated

PMA Receive generates PMA_RXSTATUS.indicate messages continuously on the basis of signals received at the MDI.

55.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–18 and in subclauses 55.2 and 55.4.6.2.

55.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementor. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS receive decoding is achieved.

55.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

55.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis on signals received at the MDI.

55.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–18.

55.2.10 PMA_RESET.indicate

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indicate primitive can take on one of two values:

TRUE	Reset is enabled.
FALSE	Reset is not enabled.

55.2.10.1 When generated

The PMA Reset function is executed as described in 55.4.2.1.

55.2.10.2 Effect of receipt

The effect of receipt of this primitive is specified in 55.4.2.1.

55.3 Physical Coding Sublayer (PCS)

Editor's note: Clause 49 (PCS for 64/66B, type 10GBASE-R) has been used as the starting point for most of the PCS for this draft of 10GBASE-T in addition to some sections of Clause 40 (1000BASE-T).

55.3.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-T PCS to transfer information to and from a PCS client. The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

55.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 55–5, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 55–5. Management is specified in Clause 30.

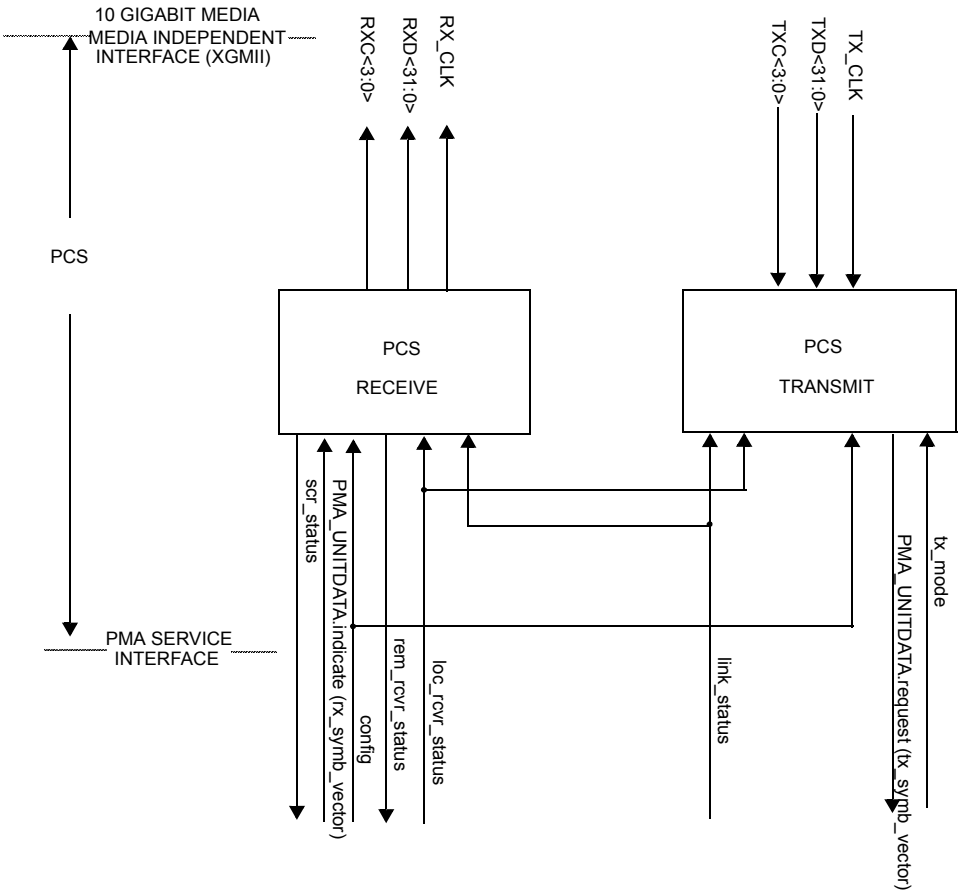


Figure 55–5—PCS reference diagram

55.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see TBD).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

55.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 55–14.

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 64B/65B is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates 65B blocks based upon the TXD <31:0> and TXC <3:0> signals on the XGMII. The subsequent functions of the PCS Transmit process then pack the resulting blocks, and split the bits into the uncoded set and the coded set which is processed by a Low Density Parity Check (LDPC) and then joint mapped into a transmit LDPC frame of DSQ (Double Square) symbols. Transmit data-units are sent to the PMA or service interface via the PMA_UNITDATA.request primitive, respectively.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_SIGNAL.indicate(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the sync_status flag to indicate whether the PCS has obtained synchronization.

When the PCS Synchronization process has obtained synchronization, the LDPC Frame Error Rate (LFER) monitor process monitors the signal quality asserting hi_lfer if excessive LDPC frame errors are detected (LDPC parity error or CRC7 error). When sync_status is asserted and hi_lfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is 1.25 ns. If a PMA_TXMODE.indicate message has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

Editor's note: Clause 49 transports idle as 64B/65B control payload. Should we preserve a PMA idle mode with binary level PAM for PMA training?

If a PMA_TXMODE.indicate message has the value SEND_T, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values {-9, 9} are transmitted in this case. This value keeps the power in the training mode the same as the power in normal mode. Training mode encoding also takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner.

In the normal mode of operation, the PMA_TXMODE.indicate message has the value SEND_N, and the PCS Transmit function uses a 65B-LDPC coding technique to generate at each symbol period code-groups that represent data or control. During transmission, the 65B bits are scrambled by the PCS using a PCS scrambler, a 7 CRC check bit, an auxiliary channel bit and a sync bit is added, then data frames are encoded into a code-group of four dimensional symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a LDPC frame encoder.

55.3.3 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an LDPC frame, and vice versa, using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 55.3.4.

55.3.4 65B-LDPC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encoding defined by the transmission code ensure that sufficient information is present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any LDPC frame errors that may occur during transmission and reception of information. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 55–6 for transmit and Figure 55–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 55.3.4.3 for information on how blocks containing control characters are mapped.

55.3.4.1 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/ and /T/ are labeled C_0 to C_7. The control character for ordered_set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

Two consecutive XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfers.

Contents of block type fields, data octets and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1e is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<64:0> and RxB<64:0> respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the

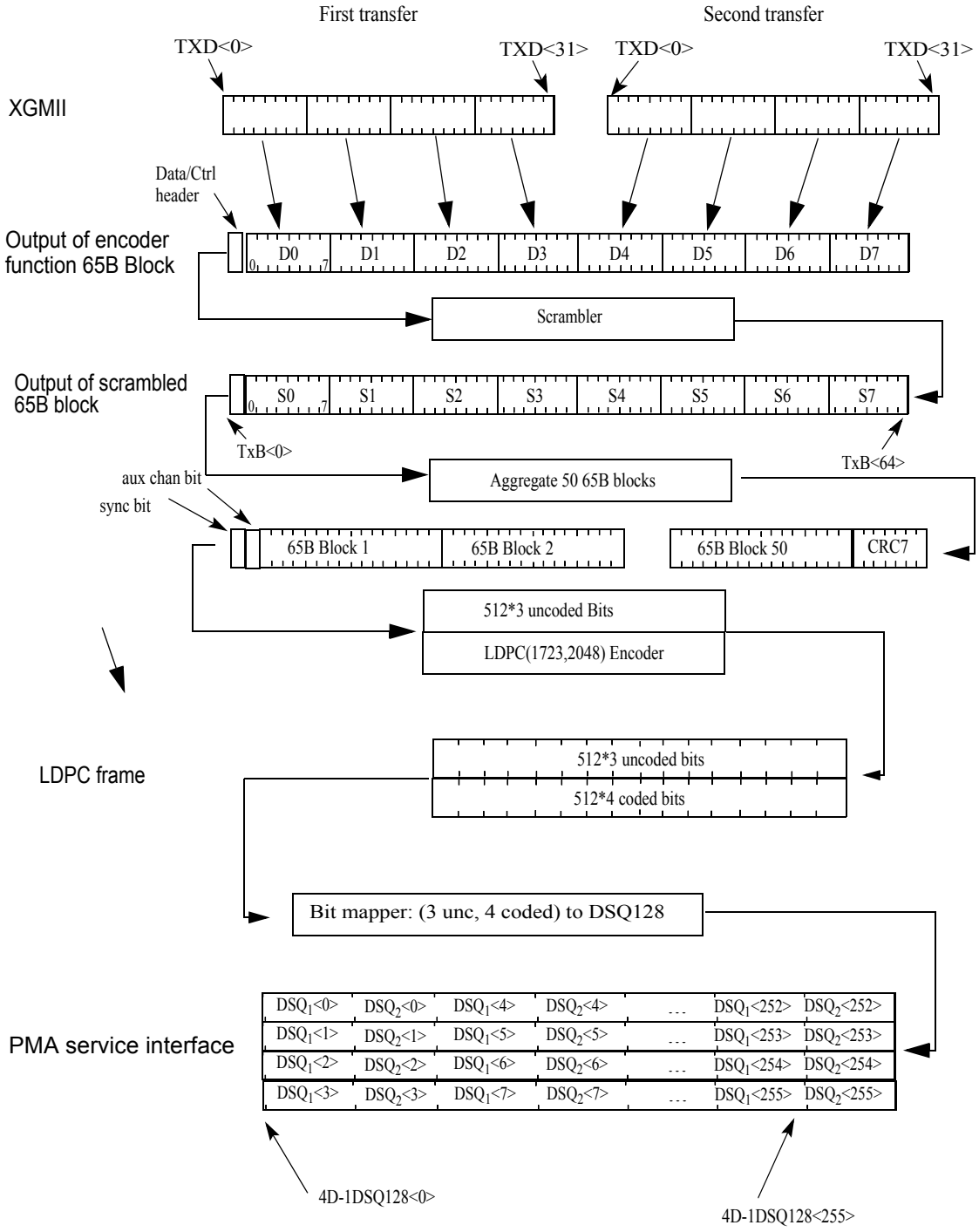


Figure 55–6—PCS Transmit Bit Ordering. Note: scr based partially on C49

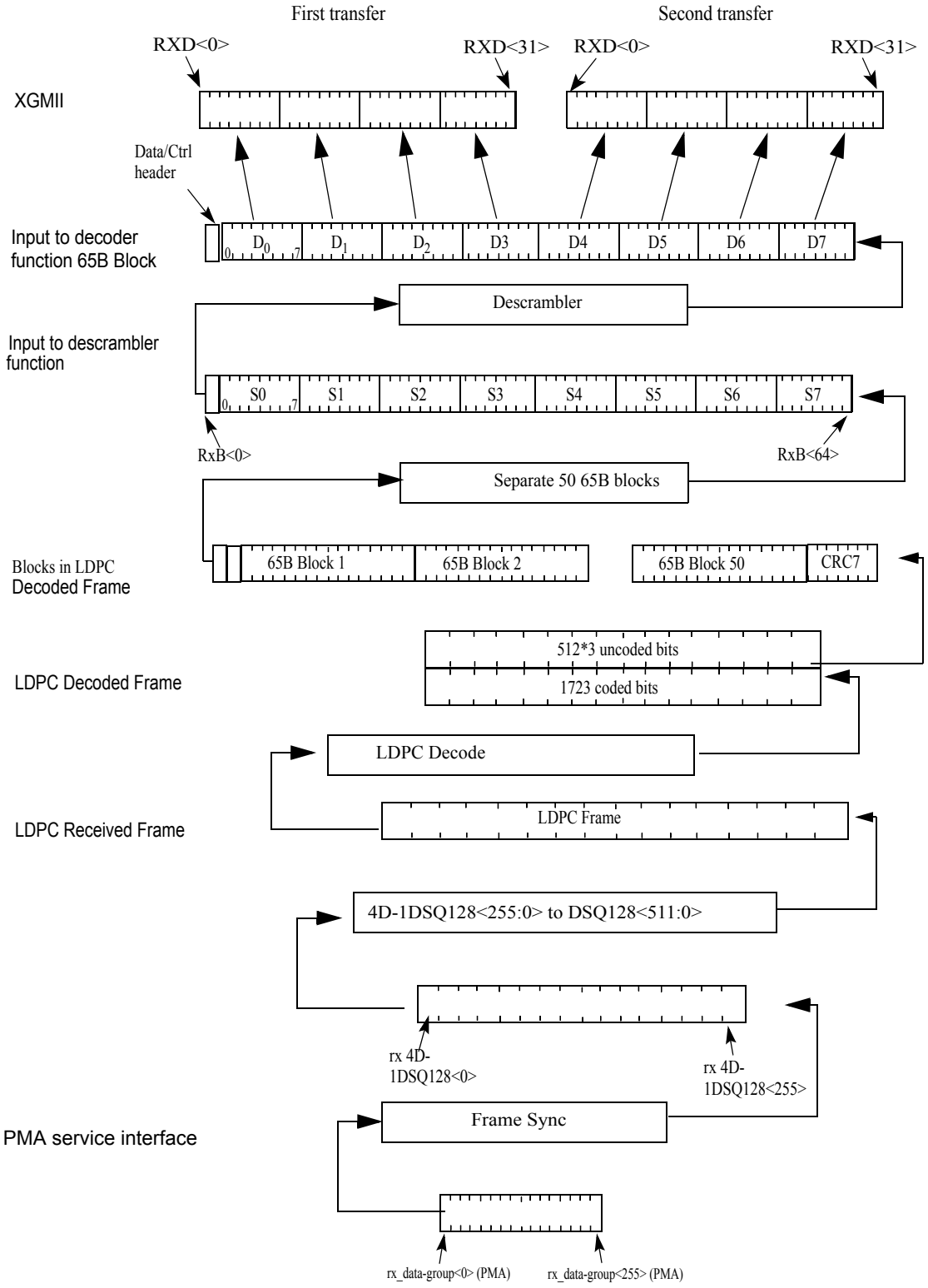


Figure 55–7—PCS Receive Bit Ordering

data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

55.3.4.2 Transmission order

Block bit transmission order is illustrated in Figure 55–6, Figure 55–8 and Figure 55–7. Note that these figures show the mapping from XGMII to 64B/65B block for a block containing eight data characters.

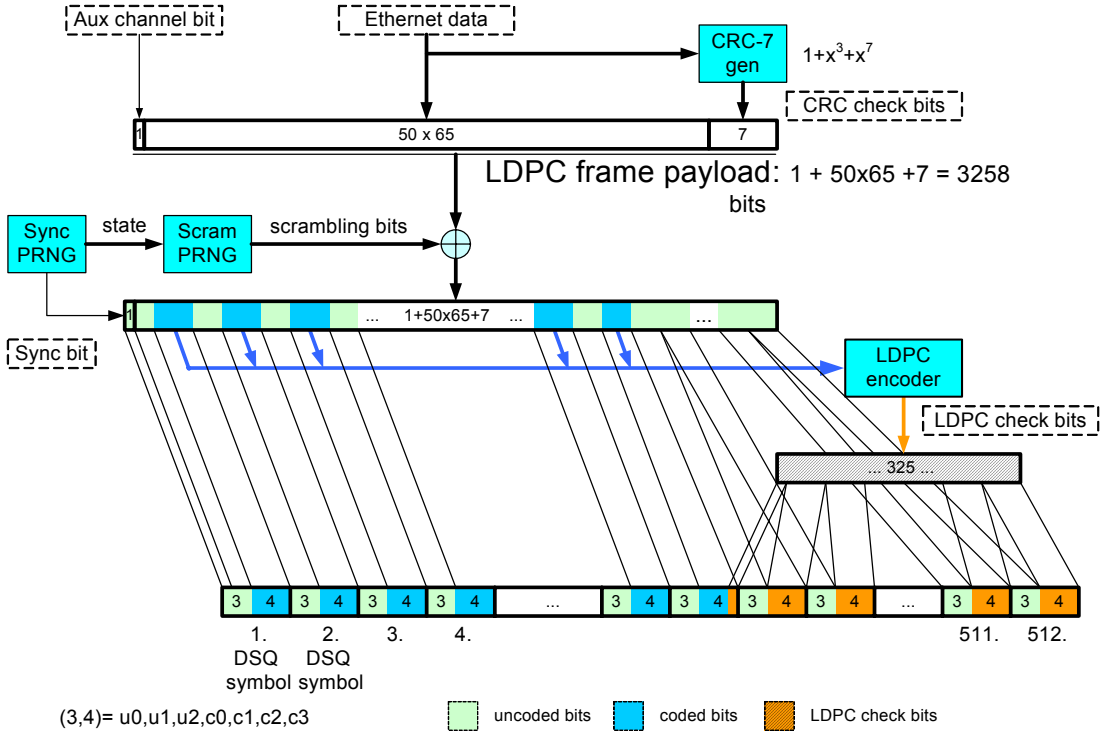


Figure 55–8—PCS Detailed Transmit Bit Ordering

55.3.4.3 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code or a 4-bit O Code. Each control block contains eight characters.

The format of the blocks is as shown in Figure 55–9. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown in normal hexadecimal. For example the block type field 0x1e is sent as 01111000 representing bits 1 through 8 of the 65 bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[3] are reserved.

55.3.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-T PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-T PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-T PCS encodes the ordered_set control codes using a combination of the block type field and a 4-bit O code for each ordered_set. The 10GBASE-T PCS encodes each of the other control characters into a 7-bit C code).

The control characters and their mappings to 10GBASE-T control codes and XGMII control codes are specified in Table 55–1. All XGMII and 10GBASE-T control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

55.3.4.5 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 10 Gigabit Ethernet uses one kind of ordered_set: the sequence ordered_set (see 46.3.4). The sequence ordered_set control character is denoted /Q/. An additional ordered_set, the signal ordered_set, has been reserved and it begins with another control code. The 4-bit O field encodes the control code. See Table 55–1 for the mappings.

55.3.4.6 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 55–1.
c) Any O code contains a value not in Table 55–1.
d) The set of eight XGMII characters does not have a corresponding block format in Figure 55–9.

55.3.4.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall

[3]The block type field values have been chosen to have a 4-bit Hamming distance between them. The only unused value which maintains the Hamming distance is 0x00.

Input Data	data ctrl bit	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\,C_1\,C_2\,C_3/O_4\,D_5\,D_6\,D_7$	1	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\,C_1\,C_2\,C_3/S_4\,D_5\,D_6\,D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/S_4\,D_5\,D_6\,D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/O_4\,D_5\,D_6\,D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/C_4\,C_5\,C_6\,C_7$	1	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	1	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	1	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	1	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	1	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	1	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 55–9—64B/65B Block Formats

occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

55.3.4.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<0:7> and RXD<0:7>). Receipt of an /S/ on any other octet of TxD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

55.3.4.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

55.3.4.10 ordered_set (/O/)

The ordered_set control characters (/O/) indicate the start of an ordered_set. There are two kinds of ordered sets: the sequence ordered_set and the signal ordered_set (which is reserved). When it is necessary to designate the control character for the sequence ordered_set specifically, /Q/ will be used. /O/ is only valid on the

Table 55–1—Control Codes

Control Character	Notation	XGMII Control Code	10GBASE-T Control Code	10GBASE-T O Code	8B/10B Code[a]
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
start	/S/	0xfb	Encoded by block type field		K27.7
terminate	/T/	0xfd	Encoded by block type field		K29.7
error	/E/	0xfe	0x1e		K30.7
Sequence ordered_set	/Q/	0x9c	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/[b]	0x1c	0x2d		K28.0
reserved1		0x3c	0x33		K28.1
reserved2	/A/	0x7c	0x4b		K28.3
reserved3	/K/	0xbc	0x55		K28.5
reserved4		0xdc	0x66		K28.6
reserved5		0xf7	0x78		K23.7
Signal ordered_set[c]	/Fsig/	0x5c	Encoded by block type field plus O code	0xF	K28.2

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.
[b]The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.
[c]Reserved for INCITS T11 Fibre Channel use.

first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered_set.

Sequence ordered_sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered_sets are not deleted for clock compensation.

55.3.4.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. It is also sent when invalid blocks are received. The /E/ allows physical sublayers such as the XGXS and PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 55.3.15.2.3 for further information.

55.3.5 Transmit process

The transmit process generates blocks based upon the TXD<31:0> and TXC<3:0> signals received from the XGMII. Two XGMII data transfers are encoded into each block. It takes 256 PMA_UNITDATA transfers to send an LDPC frame of data. Therefore, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 25:64, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process will need to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the transmit process state machine. The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

55.3.6 PCS Scrambler.

Editor's note: The PCS scrambler for draft 1.1 was taken from Clause 49. From ungerboeck_1_1104.pdf a new scrambler was proposed. Both are listed here and in Fig 55-10. Please provide comments.

The payload of the PCS frame is scrambled. The scrambler shall produce the same result as the implementation shown in Figure 55–10. This implements the scrambler polynomial:[4]

$$G(x) = 1 + x^{39} + x^{58} \quad (55–1)$$

The initial values of the sync polynomial shall be set differently for master and slave. The master initial value shall be 0xTBD and the initial slave value shall be 0xTBD. In no case shall the scrambler state be initialized to all zeros. The scrambler is run continuously on all payload bits.

Editor's note: Novel proposed scrambler

The payload of the PCS frame is scrambled using a 2-level side stream scrambling scheme shown in Figure 55-10 (Novel scrambler). The outer scrambler (sync PRNG)

$$G(x) = 1 + x^{5} + x^{23} \quad (55–2)$$

is clocked once per PCS frame to generate a single frame sync bit. For any given PCS frame, the state of the outer scrambler is used as the seed for the inner side stream scrambler (scram PRNG)

$$S(x) = 1 + x^{18} + x^{23} \quad (55–3)$$

The inner scrambler is clocked 3258 times per frame to generate the payload scrambling sequence.

In no case shall the sync polynomial state be initialized to all zeros. MASTER vs. SLAVE??? Reverse the polynomials???

[4]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (55–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

END New proposed scrambler

.

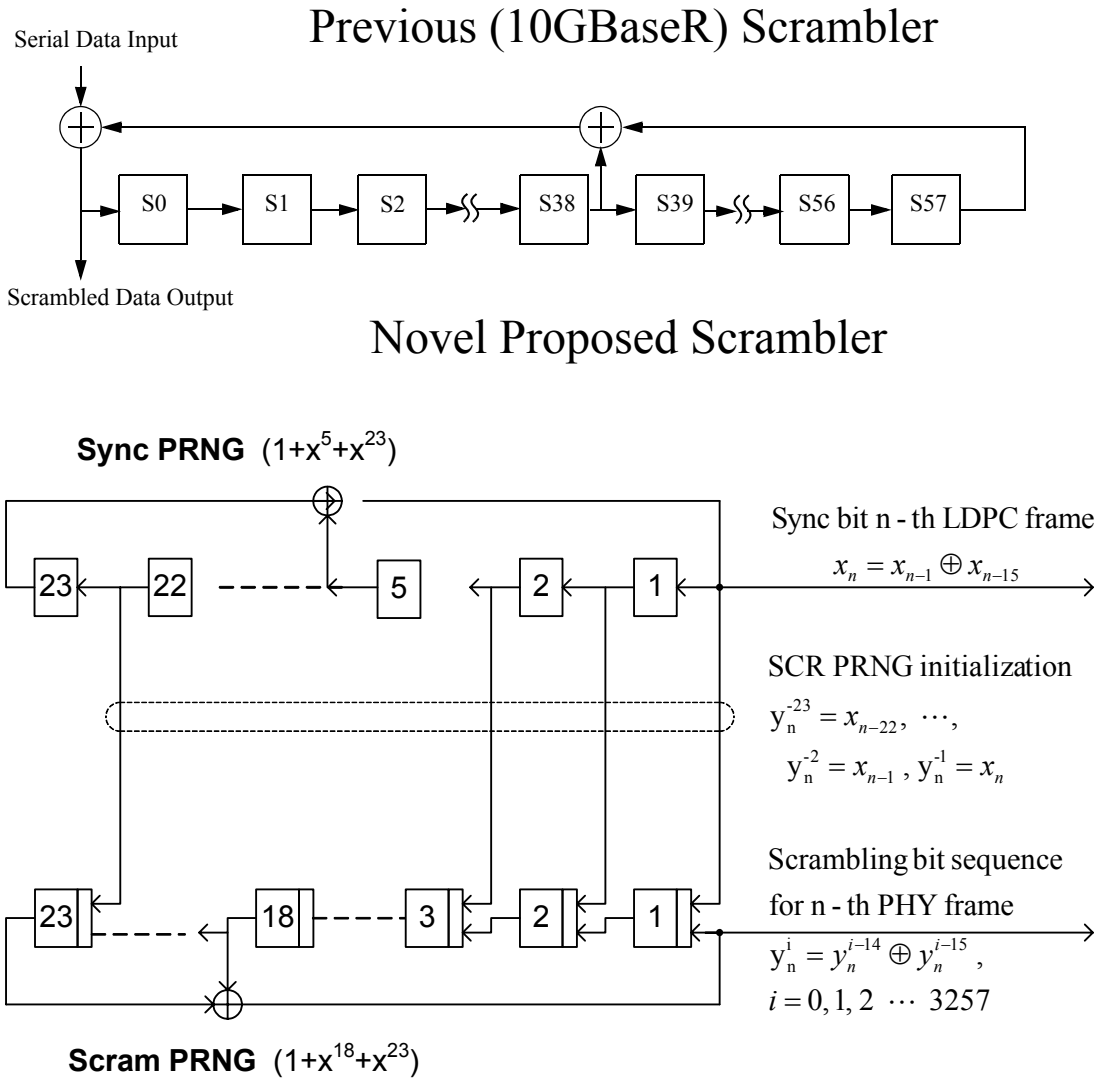


Figure 55–10—Scrambler Alternatives

55.3.7 DSQ128 bit mapping

Double Square 128 (DSQ128) refers to a two dimensional constellation with 128 possible 2D values. Each value has two components denoted $DSQ128_1$ and $DSQ128_2$ respectively. When referring to either component of the 2D DSQ128 we will use the notation 1DSQ128. The combined 2D symbol can carry log2(128) or 7 bits. The DSQ128 can be constructed by pruning the 256 values of a 2D-PAM16 where every other point in 2D is discarded (like the black or white squares in a checkerboard). The 1DSQ128 components $DSQ128_1$ and $DSQ128_2$ can each take any of the values from the set {-15, -13, -11, -9, -7, -5, -3, -1, 1, 3, 5, 7, 9, 11, 13, 15}. The mapping from 7 bits where u_0 u_1 u_2 denote the 3 uncoded bits and c_0 c_1 c_2 c_3 denote

the 4 coded bits to the DSQ128 is described by the following 3 steps (the bits from the scrambler output shall be read lsb first):

Editors Note: Need to replace the steps below for a 128 point DSQ constellation with 7 bit labels next to each symbol

Step 1:

$x_{13} = !u_0 \,\&\, u_2$

$x_{12} = u_0 \text{ XOR } u_2$

$x_{11} = c_0$

$x_{10} = c_0 \text{ XOR } c_1$

$x_{23} = (u_1 \,\&\, u_2) \text{ OR } (u_0 \,\&\, !u_1)$

$x_{22} = u_1 \text{ XOR } u_2$

$x_{21} = c_2$

$x_{20} = c_2 \text{ XOR } c_3$

Then,

$x_1 = 8x_{13}+4x_{12}+2x_{11}+x_{10}$

$x_2 = 8x_{23}+4x_{22}+2x_{21}+x_{20}$

Step 2:

$y_1 = (x_1 + x_2) \bmod 16$

$y_2 = (-x_1 + x_2) \bmod 16$

Step 3:

$DSQ128_1 = 2y_1 - 15$

$DSQ128_2 = 2y_2 - 15$

55.3.8 DSQ128 to 4D-1DSQ128

The DSQ mapper generates 512 DSQ128 2D symbols per LDPC frame that must be mapped onto 256 4D symbols prior to sending to the PMA via PMA_UNITDATA.request. The mapping of DSQ128 to 4D-1DSQ128 is illustrated in Figure 55–6. As shown in the figure, the two 1DSQ128 components of each DSQ128 symbol are mapped onto two consecutive time periods on the same wire pair

55.3.9 65B-LDPC Framer

The 65B-LDPC adapts between the 65-bit width of the 65B blocks and the 4D-1DSQ128 width of the PMA. When the transmit channel is operating in normal mode, the 65B-LDPC sends four 1DSQ128 of transmit data at a time via PMA_UNITDATA.request primitives. The UNITDATA.request primitives are fully packed with bits.

55.3.10 Test-pattern generators

Editor's note: I was asked to include some type of Test Mode and added the corresponding section from. Clause 49 (PCS for 64/66B, type 10GBASE-R) as the starting template. Please comment.

When the transmit channel is operating in test-pattern mode, it sends TBD bits of test pattern at a time via PMA_UNITDATA.request primitives.

There are TBD types of required transmit test patterns: square wave and pseudo-random. The square wave pattern is intended to aid in conducting certain transmitter tests. It is not intended for receiver tests and the receiver is not expected to receive this test pattern. The pseudo-random test-pattern mode is suitable for receiver tests and for certain transmitter tests. There is also an optional PRBS31 test pattern, which may be used for some transmit and receiver tests. When this option is supported, both the PRBS31 test-pattern generator and the PRBS31 test-pattern checker shall be provided. See Clause TBD for recommendations on the appropriate pattern for tests.

When square wave pattern is selected, the PCS will send a repeating pattern of n ones followed by n zeros where n may be any number between TBD1 and TBD2 inclusive. The value of n is an implementation choice.

When pseudo-random pattern is selected, the test pattern is generated by the scrambler using the seeds loaded through the MDIO registers and the selected data pattern. The scrambler is loaded with a seed or its inverse at the start of a block every TBD blocks. The seeds are loaded in the following pattern:

Seed A
Seed A Invert
Seed B
Seed B Invert

Invert indicates that the seed is inverted for that load. Either TBD zeros or the 64-bit encoding for two Local Fault ordered_sets can be selected as the data pattern. After loading Seed A or Seed B, the scrambler input shall be driven with the data pattern. After loading Seed A Invert or Seed B Invert, the scrambler input shall be driven with the inverse of the data pattern. While in pseudo-random test-pattern mode, the data/ctrl headers will be the control header. Thus the pseudo-random test pattern is a series of blocks with the control header and a pseudo-random payload. The characteristics of the pseudo-random test pattern can be varied by varying the seed values and data input.

When the optional PRBS31 mode is selected, the PRBS31 pattern generator sends TBD bits of PRBS31 test pattern at a time via PMA_UNITDATA.request primitives. The PRBS31 test pattern is the output of a Pseudo-Random Bit Sequence of order 31 (PRBS31) generator. The PRBS31 pattern generator shall produce the same result as the implementation shown in Fig TBD. This implements the inverted version of the bit stream produced by the polynomial

55.3.11 Frame and Block synchronization

When the receive channel is operating in normal mode, the frame and block synchronization function receives data via 4D-1DSQ128 PMA_UNITDATA.request primitives. It shall form a 4D 1DSQ128 stream from the primitives by concatenating requests with the 1DSQ128s of each primitive in order from rx_data-group<0> to rx_data-group<255> (see Figure 55–7). It obtains lock to the LDPC frames during the PAM2 training pattern using synchronization bits provided on pair A. The 65-bit blocks are extracted based on their location in the LDPC frame.

55.3.12 PCS Descrambler

Editor's note: The PCS descrambler for draft 1.1 was taken from Clause 49. From ungerboeck_1_1104.pdf a new scrambler was proposed. The corresponding descrambler would follow from the Novel Scrambler in Fig 55-10. Please provide comments.

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementation shown in Figure 55–11.

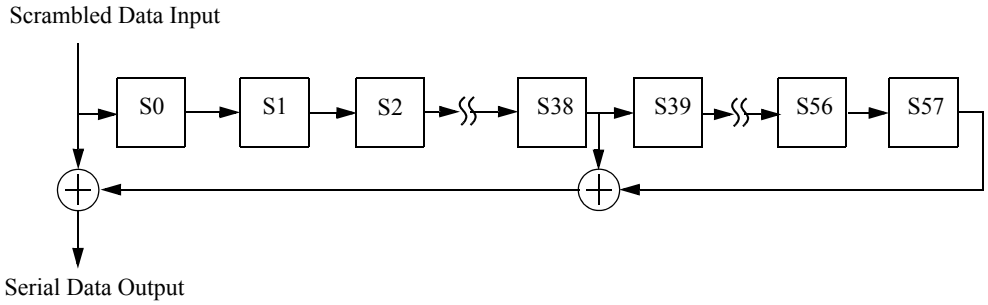


Figure 55–11—Descrambler

55.3.13 PCS Receive function

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed. During training mode, PCS Receive checks the received framing and signals the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The received 65B-LDPC frames are decoded into blocks of 65-bits to obtain the signals RXD<31:0> and RXC<3:0> for transmission to the XGMII. Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized to a 25:64 ratio, the receive process will insert idles, delete idles, or delete sequence ordered sets to adapt between rates.

The receive process decodes blocks as specified in the receive state machine shown in Figure 55–15.

55.3.14 PMA Training Side-stream scrambler polynomials

Editor's note: For PMA training the side-stream scrambler from 1000BASE-T has been used. The motion from Nov. meeting did not specify the duration of the training Please provide comments.

The PCS Transmit function employs side-stream scrambling for 2-level PAM PMA training. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indicate message assumes the value of SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 55–12. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are initialized with the values $seed_m[32:0]$ for the MASTER scrambler and $seed_s[32:0]$ for the SLAVE scrambler. Moreover after every TBD1 symbol periods, the MASTER and SLAVE scramblers shall be initialized with the values $seed_M[32:0]$ and $seed_S[32:0]$ respectively to generate a periodically repeating pattern with repetition period TBDperiodic. The initial values of the scrambler state $seed_M[32:0]$ and $seed_S[32:0]$ is left to the implementor and shall be communicated with the link partner during autoneg. In no case shall the scrambler state be initialized to all zeros.

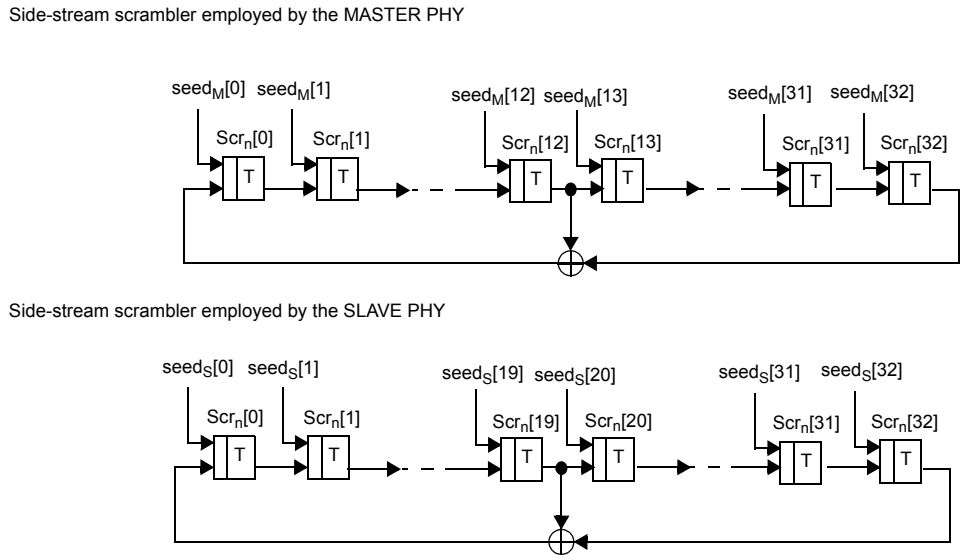


Figure 55–12—A realization of side-stream scramblers by linear feedback shift registers

55.3.14.1 Generation of bits $Sy_n[3:0]$

PMA Training signal encoding rules are based on the generation, at time n, of the four bits $Sy_n[3:0]$. These four bits are generated in a systematic fashion using the bits in $Scr_n[0:32]$, and an auxiliary generating polynomial, g(x). These four bits are mutually uncorrelated. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These four bits are derived from elements of the same maximum-length shift register sequence of length $2^{33}–1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits $Sy_n[3:0]$. The auxiliary generating polynomial is

$g(x) = x^3 \wedge x^8$

where ^ denotes the XOR logic operator.

The four bits $Sy_n[3:0]$ are generated using the bit $Scr_n[0]$ and g(x) as in the following equations:

$Sy_n[0] = Scr_n[0]$

$Sy_n[1] = g(Sy_n[0]) = Scr_n[3] \wedge Scr_n[8]$

$Sy_n[2] = g(Sy_n[1]) = Scr_n[6] \wedge Scr_n[16]$

$Sy_n[3] = g(Sy_n[2]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24]$

By construction, the four bits $Sy_n[3:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33}–1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

55.3.14.2 Generation of 4-D symbols TA_n, TB_n, TC_n, TD_n

The four-bit word Syn[3:0] is mapped to a 4-D symbol (TA_n, TB_n, TC_n, TD_n) according to following equations:

$Sz_n[0] = !Sy_n[0]$ *for* $n=k*256$, $k=0, 1, 2, \ldots$ *and* $n<TBDtraining$

$= Sy_n[0]$ *elseif* $n<TBDtraining$

$= IF_n$ *else*

TA_n= 9 *if* $(Sz_n[0]=0)$

-9 *else*

TB_n= 9 *if* $(Sy_n[1]=0)$

-9 *else*

TC_n= 9 *if* $(Sy_n[2]=0)$

-9 *else*

TD_n= 9 *if (Sy_n[3]=0)*

-9 *else*

Notice that from time *0<=n<TBDtrain* pair A is generated from the scrambler Scr_n[0], with the values negated every 256 symbols. For time *TBDtrain<=n<TBDperiod* pair A transmits the InfoField which communicates to the remote transceiver three transmitter settings of THP and Power Backoff. The transmit setting indicate the specific THP and Power Backoff used by the local transmitter, the future setting for the local transmitter and desired remote transmitter. Since there are FIR THP, 4 IIR THP and 1 bypass THP alternatives, specifying the THP setting requires 4 bits. The InfoField contains 3 bits to indicate each of the 8 the Power Backoff setting, TBD1 bits to indicate when the future setting becomes effective, TBD2 bits to indicate the local receiver decision point SNR, and one bit to indicate the value of loc_rec_status, followed by a CRC14 check for reliability. Thus a total number of bits is (4+3)*3 + TBD + 1 + 14 = 36 + TBD.

55.3.14.3 Decoding of code-groups

TBD.

55.3.14.4 Training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

55.3.15 Detailed functions and state diagrams

55.3.15.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

55.3.15.2 State diagram parameters

55.3.15.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /E/ in all the eight character locations.

IFRAME_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /I/ in all the eight character locations

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing two Local Fault ordered_sets. The Local Fault ordered_set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing two Local Fault ordered sets.

55.3.15.2.2 Variables

config
: The config parameter set by PMA and passed to the PCS via the PMA_CONFIG.indicate primitive. Values: MASTER, SLAVE

lfer_test_lf
: Boolean variable that is set true when a new LDPC frame is available for testing and false when LFER_TEST_LF state is entered. A new LDPC frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next LDPC frame

block_lock
: Boolean variable that is set true when receiver acquires block delineation

hi_lfer
: Boolean variable which is asserted true when the lfer_cnt exceeds TBD indicating a bit error ratio >TBD

reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>
: Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 55–9. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
: Vector containing two successive XGMII transfers. RXC<0> through RXC<3> for the first transfer are placed in rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are placed in rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are placed in rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

lf_valid
: Boolean indication that is set true if received LDPC frame is valid.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indicate(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the Block Lock State Machine has been completed indicating that the next candidate frame sync position can be tested.

test_lf
: Boolean variable that is set true when a new LDPC frame is available for testing and false when TEST_LF state is entered. A new LDPC frame is available for testing when the Block Sync process has accumulated enough bits from the PMA to evaluate the LDPC frame of the next block

tx_coded<64:0>
: Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 55–9. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<0> through TXC<3> for the first transfer are placed in tx_raw<0> through tx_raw<3>, respectively. TXC<0> through TXC<3> for the second transfer are placed in tx_raw<4> through tx_raw<7>, respectively. TXD<0> through TXD<31> for the first transfer are placed in tx_raw<8> through tx_raw<39>, respectively. TXD<0> through TXD<31> for the second transfer are placed in tx_raw<40> through tx_raw<71>, respectively.

55.3.15.2.3 Functions

DECODE(rx_symb_vector<255:0>)

In the PCS Receive process, this function takes as its argument 256 values of rx_symb_vector<255:0> from the PMA and decodes the 65B-LDPC bit vector returning 50 vectors rx_raw<71:0> which is sent to the XGMII. The DECODE function shall decode the block as specified in 55.3.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 256 values of tx_symb_vector. The ENCODE function shall encode the block as specified in 55.3.4.

R_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 65-bit rx_coded vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains a sync header of 1 and one of the following:

a) A block type field of 0x1e and eight valid control characters other than /E/;

b) A block type field of 0x2d or 0x4b, a valid O code, and four valid control characters;

c) A block type field of 0x55 and two valid O codes.

S; The vector contains a sync header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;

b) A block type field of 0x66 and a valid O code;

c) A block type field of 0x78.

T; The vector contains a sync header of 1, a block type field of 0x87, 0x99, 0xaa, 0xb4, 0xcc, 0xd2, 0xe1 or 0xff and all control characters are valid.

D; The vector contains a sync header of 0.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-R control code specified in Table 55–1. A valid O code is one containing an O code specified in Table 55–1.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP

Causes the next candidate 65B-LDPC frame sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible symbol positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains one of the following:

a) eight valid control characters other than /O/, /S/, /T/ and /E/;

b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;

c) two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 55–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 55–1.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT
Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

55.3.15.2.4 Counters

lfer_cnt
Count up to a maximum of TBD of the number of invalid LDPC frames within the current TBD μs period.

lf_cnt
Count of the number of LDPC frames checked within the current TBD LDPC frame window.

lf_invalid_cnt
Count of the number of invalid LDPC frames within the current TBD LDPC frame window.

55.3.15.2.5 Timers

symb_timer
Continuous timer: The condition symb_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.
Duration: TBD ns nominal. (See clock tolerance in 55.5.8.2.)

Symb-timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

55.3.15.3 Messages

PMA_UNITDATA.indicate (rx_symb_vector)
A signal sent by PMA Receive indicating that a vector of four symbols is available in rx_symb_vector. (See 55.2.6.)

PMA_UNITDATA.request (tx_symb_vector)
A signal sent to PMA Transmit indicating that a vector of four 1DSQ128 symbols is available in tx_symb_vector. (See 55.2.5.)

PUDI
Alias for PMA_UNITDATA.indicate (rx_symb_vector).

PUDR
Alias for PMA_UNITDATA.request (tx_symb_vector).

STD
: Alias for symb_timer_done.

55.3.15.4 State diagrams

The Lock state machine shown in Figure 55–13 determines when the PCS has obtained lock to the received data stream. The LFER Monitor state machine shown in Figure 55–13 monitors the received signal for high LDPC frame error ratio.

The Transmit state machine shown in Figure 55–14 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the Transmit state machine sends Local Fault ordered sets when reset is asserted, the scrambler and 65B-LDPC may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the PMA service interface.

The Receive state machine shown in Figure 55–15 controls the decoding of received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of Lock, LFER Monitor, Transmit and Receive as specified in these state machines.

55.3.16 PCS Management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

55.3.16.1 Status

PCS_status:
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_lfer is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_lfer:
: Indicates the state of the hi_lfer variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

55.3.16.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

lfer_count:
: TBD-bit counter that counts each time LFER_BAD_LF state is entered. This counter is reflected in MDIO register bits 3.33.13:8. Note that this counter counts a maximum of TBD counts per TBD μs since the LFER_BAD_LF can be entered a maximum of TBD times per TBD μs window.

errored_block_count:
: TBD-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0.

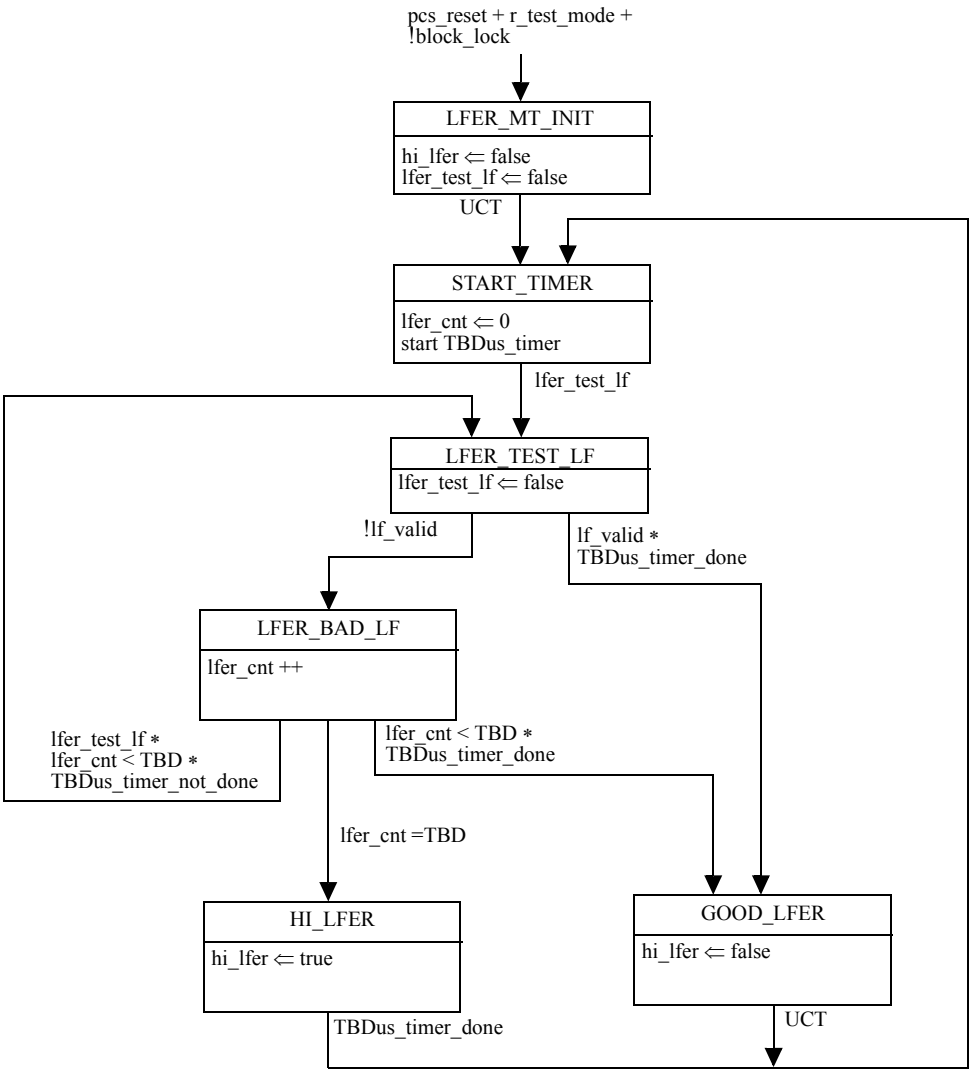


Figure 55–13—LFER monitor state machine

55.3.16.3 Loopback

Editor's note: PCS for 1000BASE-T does not appear to include loop back modes. This can be useful. Please comment.

The PCS shall be placed in Loopback mode when the Loopback bit in MDIO register TBD is set to a logic one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of TBD 1DSQ128 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

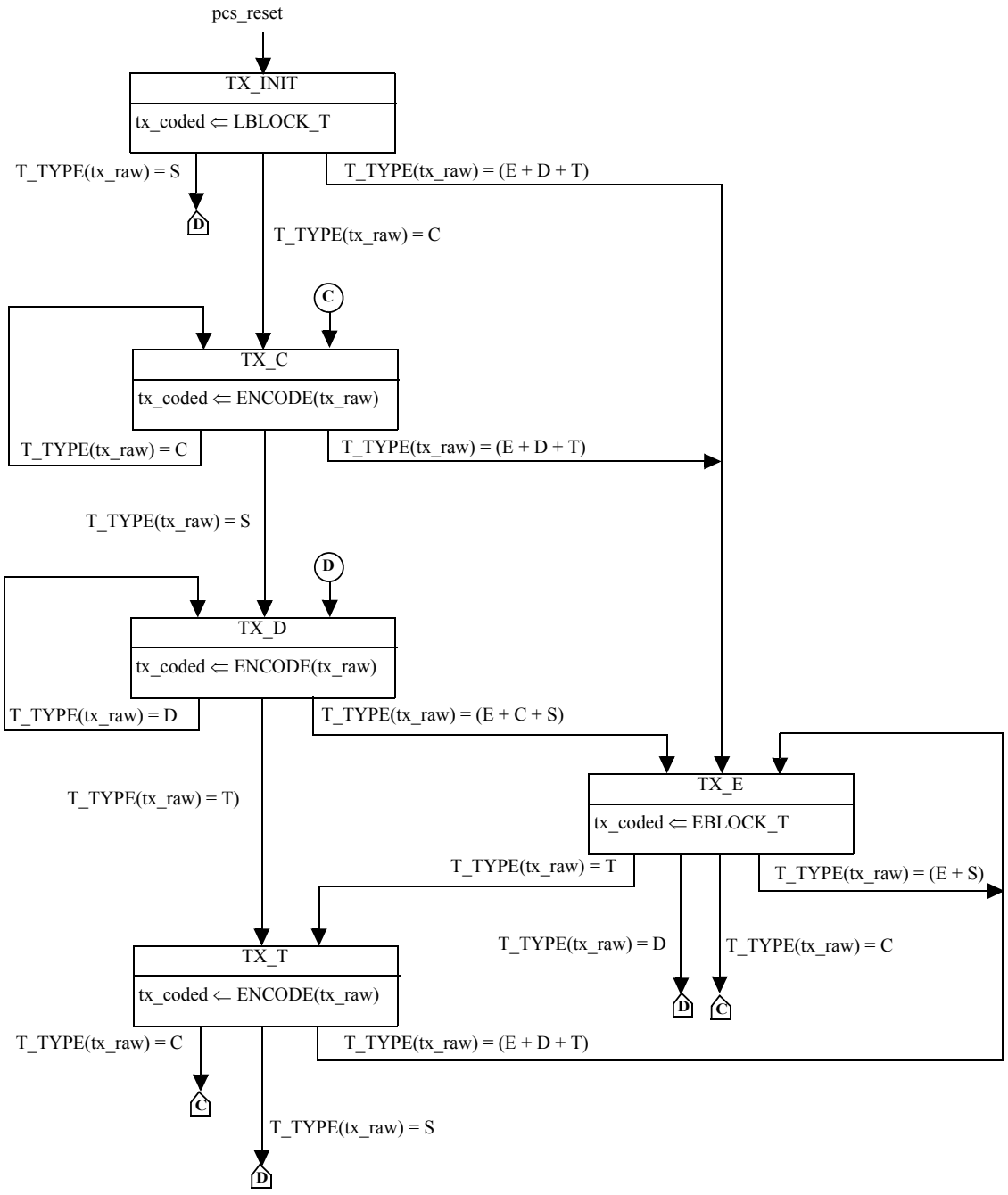


Figure 55–14—PCS Transmit state machine

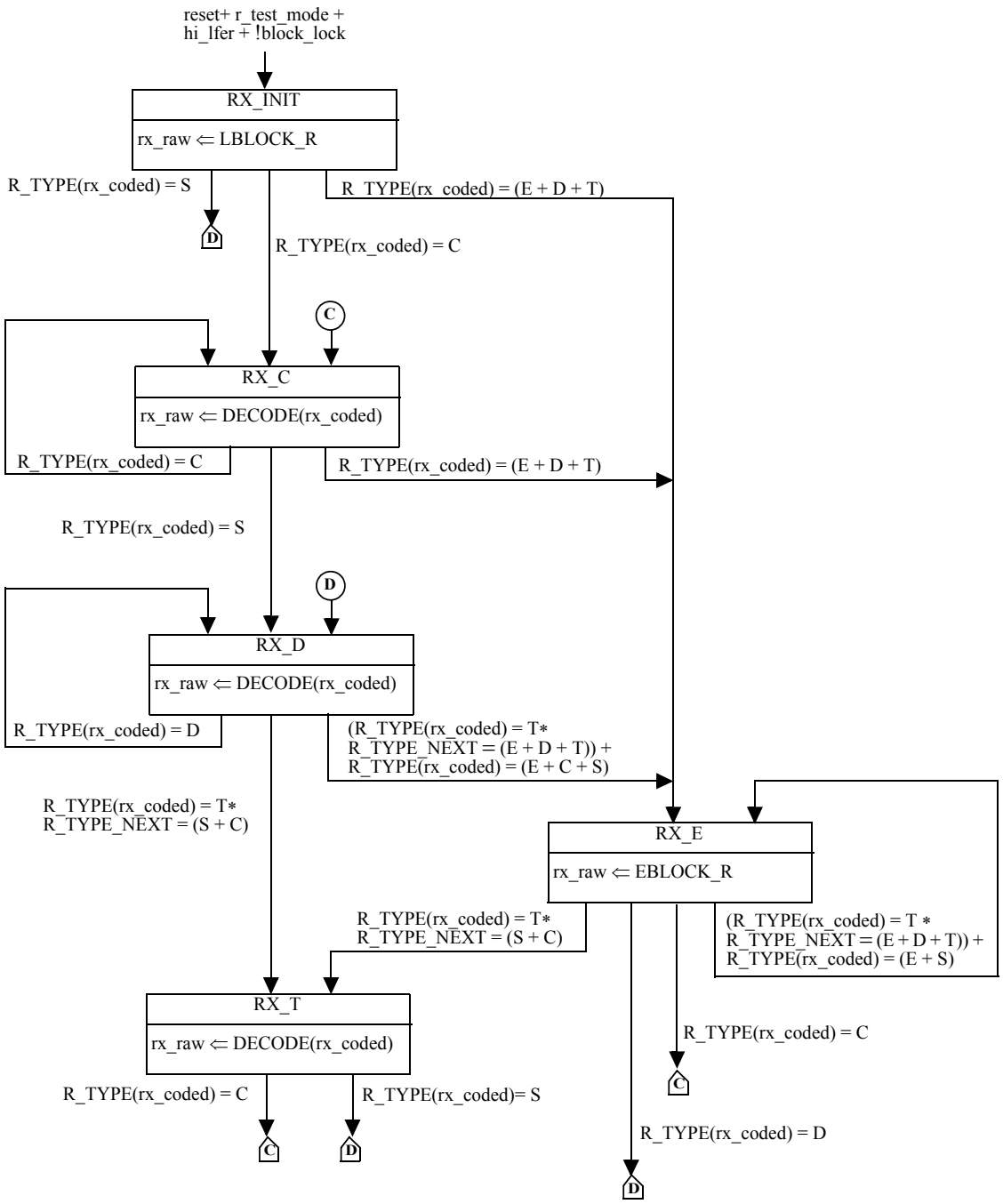


Figure 55–15—PCS Receive state machine

55.4 Physical Medium Attachment (PMA) sublayer

Editor's note: Clause 40 has been used as the starting point for most of the PMA for this initial draft of 10GBASE-T. Please provide comments.

55.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 55.2.2 to the 10GBASE-T baseband medium, specified in 55.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 55.8.

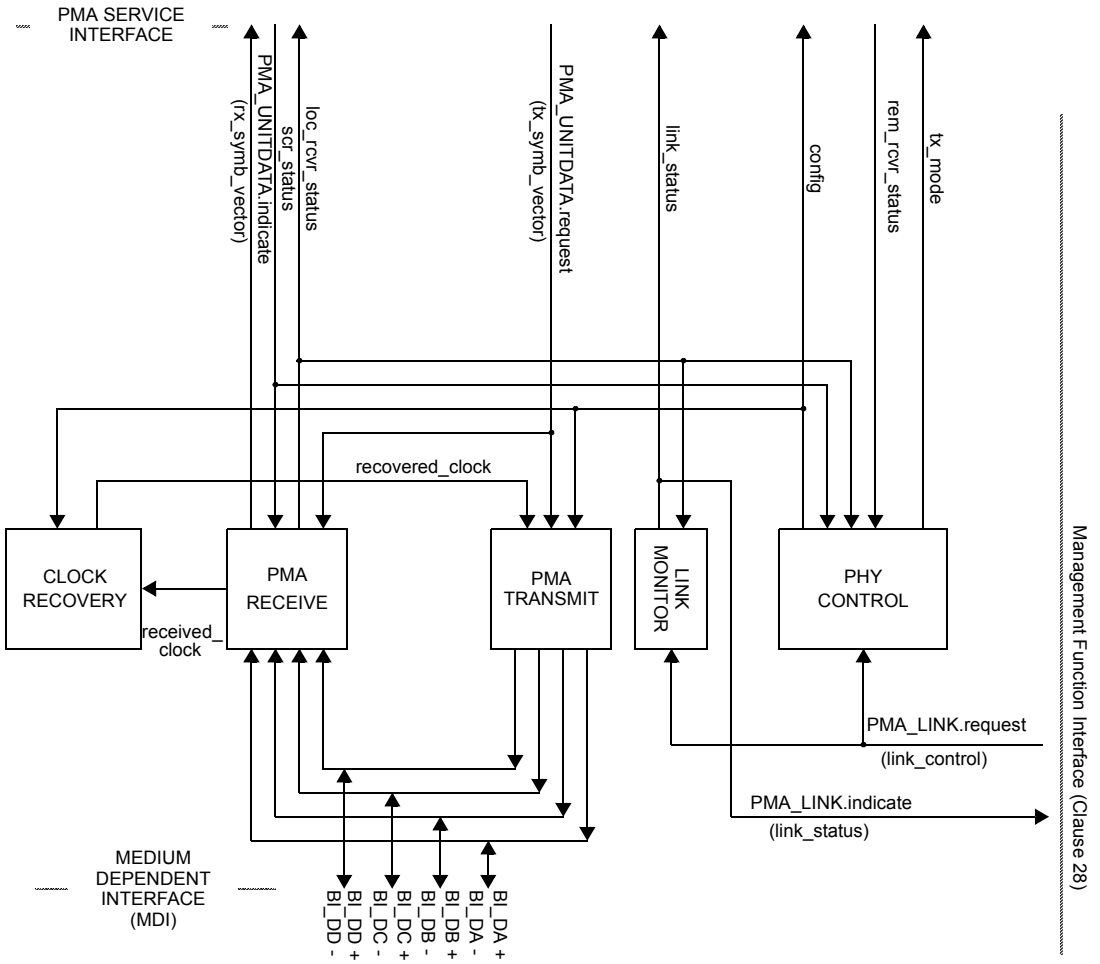


Figure 55–16—PMA reference diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

55.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 55–16, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 55–16. The management interface and its functions are specified in Clause 22 CHANGE LINK TO C45.

Editor's note: Should we include references to Clause 28 and Clause 30 in addition to Clause 22?

55.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see Clause 46.TBD)
b) The receipt of a request for reset from the management entity

PMA Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

55.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively after processing with the THP, TBD transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 55.4.3.1, and shall comply with the electrical specifications given in 55.5.

When the PMA_CONFIG.indicate parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 55.5.5. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented and the PMA_CONFIG.indicate parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 55.4.2.6 while meeting the jitter requirements of 55.5.5. If loop timing is not implemented, the SLAVE PHY clocking is identical to the MASTER PHY clocking.

55.4.2.3 PMA Receive function

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 55.4.3.2. The PMA shall translate the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DB into the PMA_UNITDATA.indicate parameter rx_symb_vector with equivalent LFER of less than $3.2*10^{-9}$ over a channel meeting the requirements of 55.7.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

55.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 55–18 (TBD).

During Auto-Negotiation PHY Control is in the DISABLE 10GBASE-T TRANSMITTER state and the transmitters are disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the SLAVE SILENT state for the SLAVE. Upon entering this state, the maxwait timer is started and PHY Control forces transmission of zeros by setting tx_mode=SEND_Z. In MASTER mode, PHY Control transitions immediately to the PMA TRAINING Init state. In SLAVE mode, PHY Control transitions to the TRAINING Init state only after the SLAVE PHY acquires timing, converges its equalizers, and acquires its descrambler state, and sets scr_status=OK**.** Upon entering the PMA TRAINING Init state, the minwait_timer is started and PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T.

The final choice of THP and Power Backoff settings and convergence of the adaptive filter parameters is completed in the PMA TRAINING Update state. After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter Info Fields (IF) and loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status and remIF. When the minwait_timer expires and the condition loc_rcvr_status=OK and rem_rcvr_status is satisfied, PHY Control transitions into PCS training.

The normal mode of operation corresponds to the SEND PCS DATA state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 55.3.2.1.

55.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 55–19.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 10GBASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

55.4.2.6 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the LDPC FER indicated in 55.4.2.3 is achieved. The received clock signal must be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

55.4.3 MDI

Communication through the MDI is summarized in 55.4.3.1 and 55.4.3.2.

55.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is 1DSQ128. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$b_i = (a_i + \sum_{k=1}^{\infty} b_{i-k}\alpha_k) mod 16$$

$$s(t) = \sum_{k=0}^{\infty} b_k h_1(t - kT)$$

where ‘x mod16’ of a real number x, is defined as a value between the interval (-16, 16] such that ‘x mod16 = x + 32m’, for some integer m. In the above equation, a_i represents the 1DSQ128 symbol from the set {-15, -13, -11, -9, -7, -5, -3, -1, 1, 3, 5, 7, 9, 11, 13, 15} to be transmitted at time iT, α_k denotes the THP coefficients, and $h_1(t)$ denotes the system symbol response at the MDI. The THP coefficients shall be selected from a predetermined set of 4 IIR THP coefficients or 4 FIR THP coefficient or the option of bypassing the THP altogether. Each of the THP filters (plus bypass) shall be optimized to a decreasing length of cable (from max length to 0m length). The THP filter coefficients shall be fixed after startup. This symbol response shall comply with the electrical specifications given in 55.5.

55.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{k=0}^{\infty} a_{k,agmt} h_2(t - kT) + w(t)$$

In this equation $a_{k,agmt}$ represents the augmented DSQ128 constellation elements by the transmit mod16 function, $h_2(t)$ denotes the impulse response of the overall channel between the transmit symbol source and the receive MDI and $w(t)$ is a term that represents the contribution of various noise sources. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD shall be processed within the PMA Receive function to yield the received symbols rx_symb_vector.

55.4.4 Automatic MDI/MDI-X Configuration

Automatic MDI/MDI-X Configuration is intended to eliminate the need for crossover cables between similar devices. Implementation of an automatic MDI/MDI-X configuration is required for 10GBASE-T

devices. The automatic configuration method used shall comply with the following specifications. The assignment of pin-outs for a 10GBASE-T crossover function cable is shown in Table 55–9 in 55.8.

55.4.4.1 Description of Automatic MDI/MDI-X state machine

The Automatic MDI/MDI-X state machine facilitates switching the BI_DA(C)+ and BI_DA(C)– with the BI_DB(D)+ and BI_DB(D)– signals respectively prior to the auto-negotiation mode of operation so that fast link pulses can be transmitted and received in compliance with Clause 28 Auto-Negotiation specifications. The correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. This algorithm uses an 11-bit Linear Feedback Shift Register (LFSR) to create a pseudo-random sequence that each end of the link uses to determine its proposed configuration. Upon making the selection to either MDI or MDI-X, the node waits for a specified amount of time while evaluating its receive channel to determine whether the other end of the link is sending link pulses or PHY-dependent data. If link pulses or PHY-dependent data are detected, it remains in that configuration. If link pulses or PHY-dependent data are not detected, it increments its LFSR and makes a decision to switch based on the value of the next bit. The state machine does not move from one state to another while link pulses are being transmitted.

55.4.4.2 Pseudo-random sequence generator

One possible implementation of the pseudo-random sequence generator using a linear-feedback shift register is shown in Figure 55–17. The bits stored in the shift register delay line at time n are denoted by S[10:0]. At each sample period, the shift register is advanced by one bit and one new bit represented by S[0] is generated. Switch control is determined by S[10].

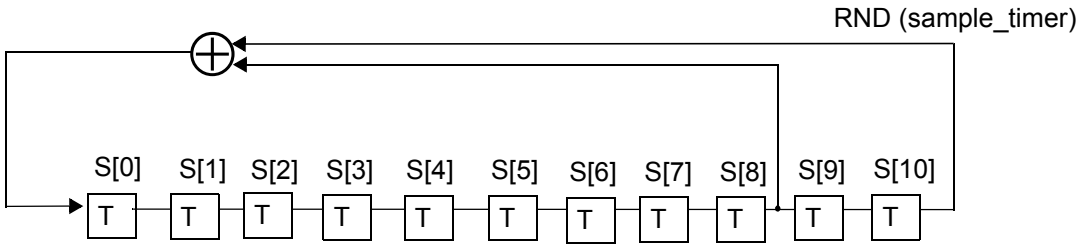


Figure 55–17—Automatic MDI/MDI-X linear-feedback shift register

55.4.5 State variables

55.4.5.1 State diagram variables

config

The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indicate primitive.

Values: MASTER or SLAVE

link_control

This variable is defined in 28.2.6.2.

Link_Det

This variable indicates linkpulse = true or link_status = READY has occurred at the receiver since the last time sample_timer has been started.

Values: TRUE: linkpulse = true or link_status = READY has occurred since the last time sample_timer has been started.

FALSE: otherwise

55.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop timer” is asserted.

A_timer

An asynchronous (to the Auto-Crossover State Machine) free-running timer that provides for a relatively arbitrary reset of the state machine to its initial state. This timer is used to reduce the probability of a lock-up condition where both nodes have the same identical seed initialization at the same point in time.

Values: The condition A_timer_done becomes true upon timer expiration.

Duration: This timer shall have a period of TBD ± TBD%.

Initialization of A_timer is implementation specific.

maxwait_timer

A timer used to limit the amount of time during which a receiver dwells in the SLAVE SILENT and TRAINING states. The timer shall expire TBD ± TBD ms if config = MASTER or TBD ± TBD ms if config = SLAVE. This timer is used jointly in the PHY Control and Link Monitor stage diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 55–18.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the PMA TRAINING, SEND IDLE, or DATA states. The timer shall expire TBD ± TBDμs after being started.

sample_timer

This timer provides a long enough sampling window to ensure detection of Link Pulses or link_status, if they exist at the receiver.

Values: The condition sample_timer_done becomes true upon timer expiration.

Duration: This timer shall have a period of TBD ± TBD ms.

stabilize_timer

A timer used to control the minimum time that loc_rcvr_status must be OK before a transition to Link Up can occur. The timer shall expire TBD ± TBD μs after being started.

55.4.6 State Diagrams

55.4.6.1 PHY Control state diagram

Editor’s note: Clause 40 has been used as the starting point for this initial PHY Control state diagram with some additional outline THP/PBO states based on Info Field exchanges. The THP/PBO effect in the PHY start-up requires additional input for the Task Force. Please provide comments.

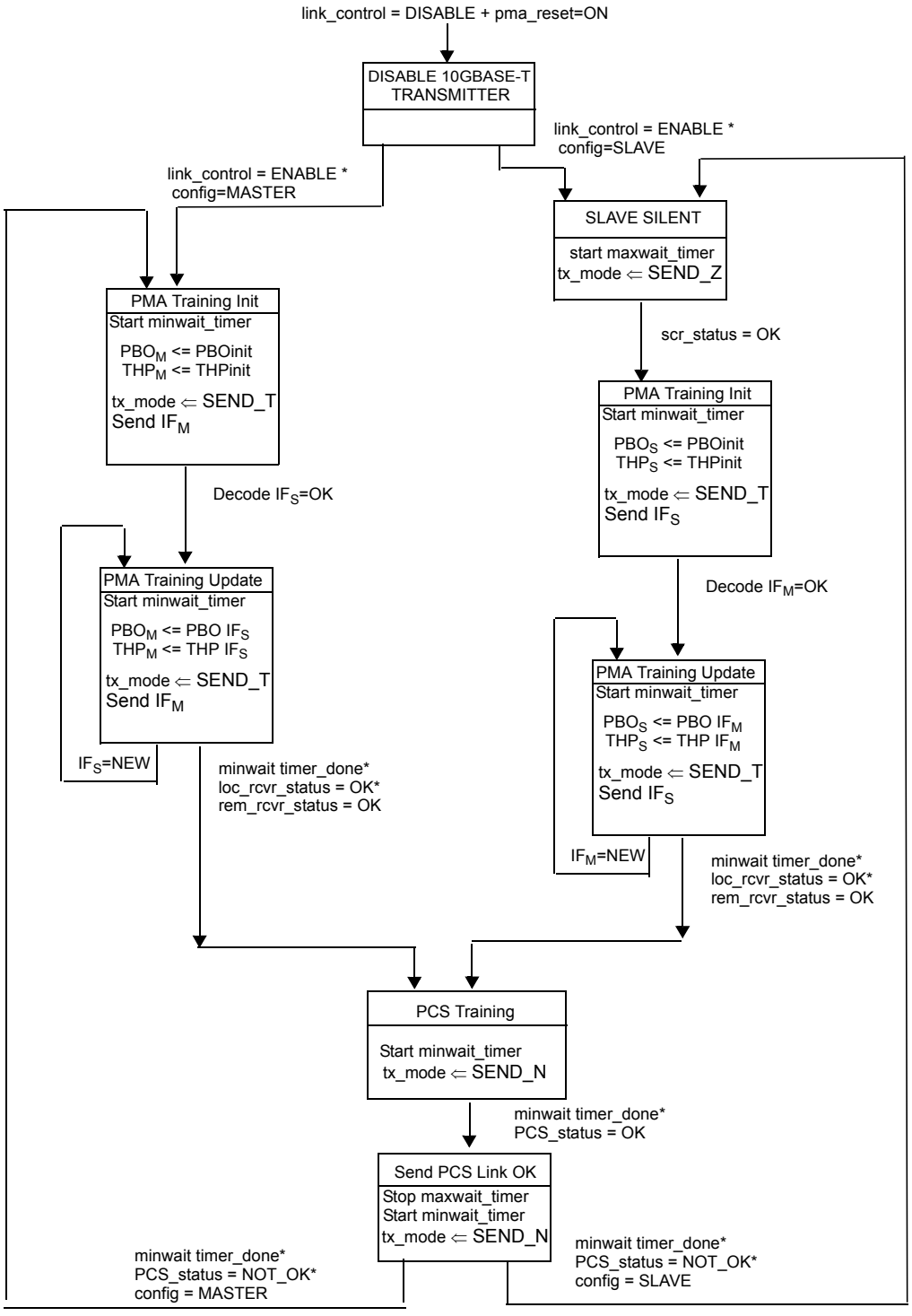
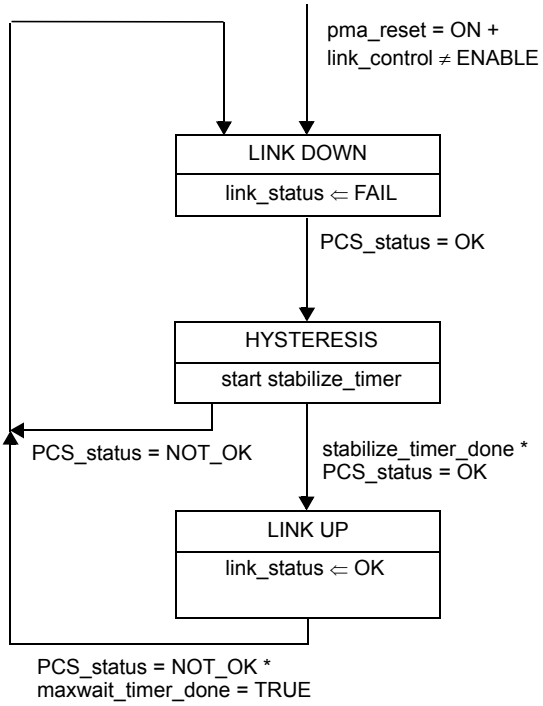


Figure 55–18—PHY Control state diagram

55.4.6.2 Link Monitor state diagram



NOTES
1—maxwait_timer is started in PHY Control state diagram (see Figure 55–18).
2—The variables link_control and link_status are designated as link_control_(10GigT) and link_status_(10GigT), respectively, by the Auto-Negotiation Arbitration state diagram (TBD Figure 28–16).

Figure 55–19—Link Monitor state diagram

55.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

Common-mode tests use the common-mode return point as a reference.

55.5.1 Isolation requirement

Editor's note: Text in Clause 55.5.1 is copied from the 1000BASE-T standard, section 40.6.1.1 with updates to some of the references. This text is unapproved

The PHY shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950-1: 2001.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950-1: 2001.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950-1: 2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

55.5.1.1 Test channel

Editor's note: Un-approved text based on 1000BASE-T standard. Editor's x_1, x_2, x and y as well as the Attenuation numbers in the table specifying the test channel are TBD

To perform the transmitter MASTER-SLAVE timing jitter tests described in this clause, a test channel is required to ensure that jitter is measured under conditions of poor signal to echo ratio. This test channel shall be constructed by combining 100 Ω and 120 Ω cable segments that both meet or exceed ISO/IEC 11801 augmented by link segment specified in 55.7 for each pair, as shown in Figure 55–20, with the lengths and additional restrictions on parameters described in Table 55–2. The ends of the test channel shall be terminated with connectors meeting or exceeding ISO/IEC 11801:2001 Class E specifications. The return loss of the resulting test channel shall meet the return loss requirements of 55.7.2.3 and the crosstalk requirements of 55.7.3.2.2.

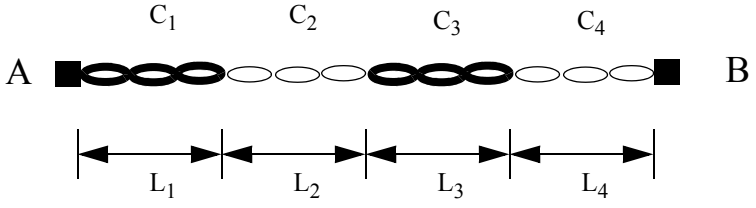


Figure 55–20—Test channel topology for each cable pair

Table 55–2—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at TBD freq)
1	$L_1=x_1$	120 ± 5Ω	TBD
2	$L_2=x$	100 ± 5Ω	TBD
3	$L_3=x_2$	120 ± 5Ω	TBD
4	$L_4=y$	100 ± 5Ω	TBD

55.5.2 Test modes

Editor's Note: Method for test mode 4 and test mode 5 was approved. Remaining text is un-approved text and is based on framework in 1000BASE-T standard.

Note: F_s equals 800 ± TBD and is the symbol rate in MHz. Later in the text, when a specific tolerance on the symbol rate is not specified, it is assumed to be this.

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, and transmitted jitter.

For a PHY with an MDIO management interface, these modes shall be enabled by setting ***TBD*** bits (10GBASE-T Control Register) of the MDIO Management register set as shown in Table 55–3. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a MDIO shall provide a means to enable these modes for conformance testing.

Table 55–3—MDIO management register settings for test modes

Bit 1 TBD	Bit 2 TBD	Bit 3 TBD	Mode
0	0	0	Normal operation
0	0	1	Test mode 1—Transmit voltage at MDI test
0	1	0	Test mode 2—Transmit jitter test in MASTER mode
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode
1	0	0	Test mode 4—Transmit distortion test
1	0	1	Test mode 5 - Normal operation with no power back-off. This is for the PSD mask and power level test
1	1	0	Test mode 6 - Transmitter droop test mode.
1	1	1	Reserved, operations not identified.

When test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 55.4.3.1 continually from all four transmitters, with the THP turned off:

{{TBD +16 followed by TBD -16 symbols}.

This sequence is repeated continually without breaks between the repetitions when the test mode is enabled. The transmitter shall time the transmitted symbols from a F_s clock in the MASTER timing mode.

When test mode 2 is enabled, the PHY shall transmit, with THP turned off, the data symbol sequence, {+16, –16} repeatedly on all channels. The transmitter shall time the transmitted symbols from an F_s clock in the MASTER timing mode.

When test mode 3 is enabled, the PHY shall transmit the data symbol sequence {+16, -16} repeatedly on all channels. The transmitter shall time the transmitted symbols from an F_s clock in the SLAVE timing mode. A typical transmitter output for transmitter test modes 2 & 3 in is shown in Figure 55–21.

Editor's note: The waveform shown in Figure 55–21 assumes a peak-to-peak output swing of 2V differential. This is illustrative waveforms and can be adjusted once both the parameters are finalized by the task force.

When test mode 4 is enabled, the PHY shall transmit, with the THP turned off, transmitted symbols, timed from an F_s clock in the MASTER timing mode, defined as follows:

Symbols corresponding to a single frequency tone, with frequencies of TBD.

*Editor's Note: Recommended frequencies are (800MHz/1024)*13, (800MHz/1024)*23, (800MHz/1024)*53, (800MHz/1024)*101, (800MHz/1024)*167*.

Symbols corresponding to dual frequency tones in the pairs of TBD.

*Editor's Note: Recommended frequencies are: [(800MHz/1024)*179, (800MHz/1024)*181], [(800MHz/1024)*277, (800MHz/1024)*281], [(800MHz/1024)*397, (800MHz/1024)*401], [(800MHz/1024)*499, (800MHz/1024)*503].*

The peak to peak symbols used in this test, for both single and dual frequency tones correspond to ± 16.

Editor's Note: As written, this deviates from the 1000BASE-T approach because time domain distortion tests based on a scrambled sequence will be hard/marginal to measure with currently available test equipment. This is because of the higher speed and the lower distortion specifications. This issue was discussed in detail in http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf *at the July 2004 meeting.*

When test mode 5 is enabled, the PHY shall transmit as in normal operation but with the power backoff disabled. Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level.

Test mode 6 is for testing transmitter droop. When test mode 6 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 55.4.3.1 continually from all four transmitters, with the THP turned off:

{{TBD +16 followed by TBD -16 symbols}.

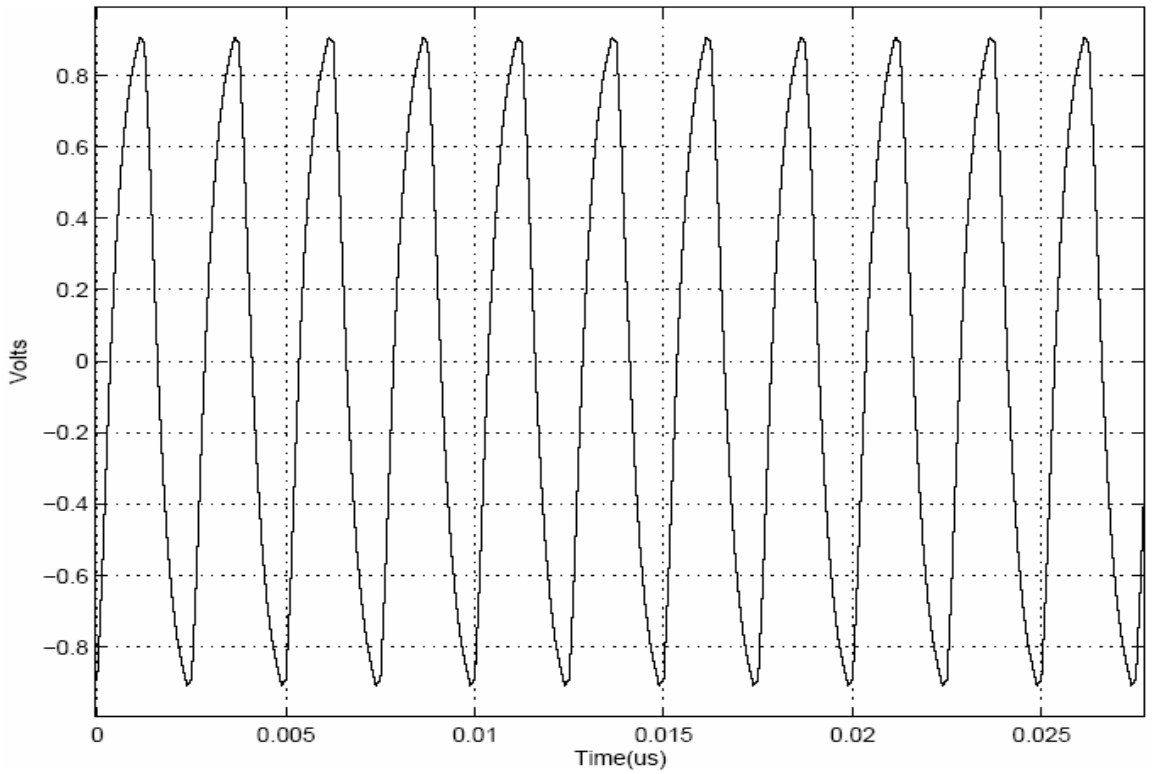


Figure 55–21—Informative: Example of transmitter test modes 2 & 3 waveform

55.5.2.1 Test Fixtures

The following fixtures (illustrated by Figure 55–22, Figure 55–23 and Figure 55–24), or their functional equivalents, shall be used for measuring the transmitter specifications described in 55.5.3.

Editor's note: The next three figures have been changed from the 1000BASE-T test setups in places where deemed necessary. These test setups are unapproved. Figure 55–23 includes a power summer or Balun device to couple the 100 Ω differential output of the transmitter to the 50 Ω single-ended input typically found in a Spectrum Analyzer input. Comments/alternate proposals are welcome.

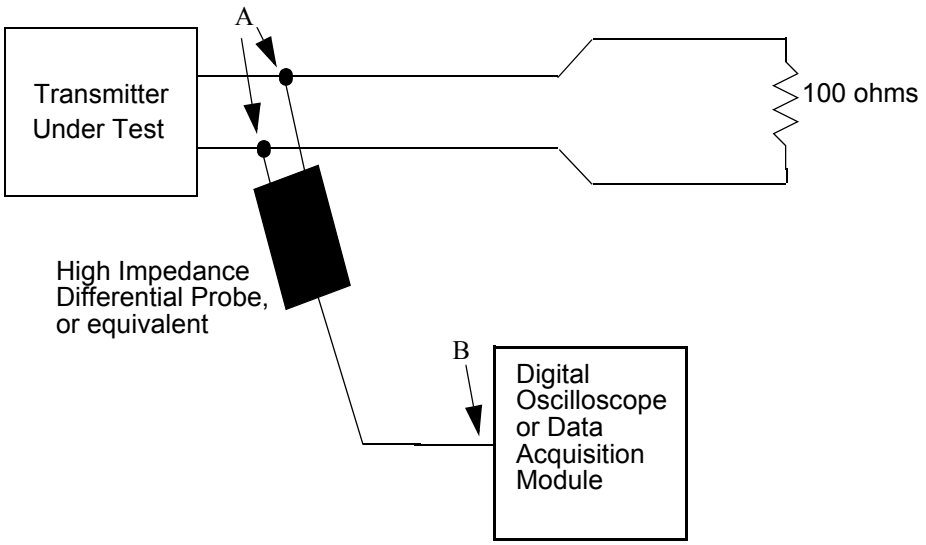


Figure 55–22—Transmitter test fixture 1 for peak to peak voltage measurement and Transmitter droop measurement

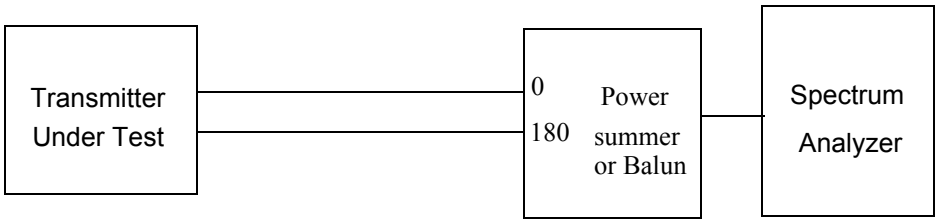


Figure 55–23—Transmitter test fixture 2 for linearity measurement, power spectral density measurement and transmit power level measurement

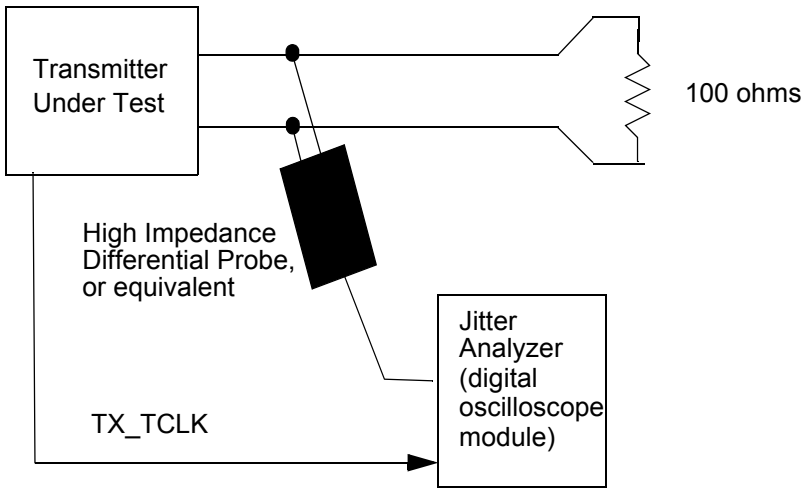


Figure 55–24—Transmitter test fixture 3 for transmitter jitter measurement

To allow for measurement of transmitted jitter in test mode 2 and 3, for both master and slave modes, the PHY shall provide access to the F_s rate symbol clock, TX_TCLK, that times the transmitted symbols (see 55.4.2.2). The PHY shall provide a means to enable this clock output if it is not normally enabled.

55.5.3 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 55.4.2.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

55.5.3.1 Peak differential output voltage

Editor's note: We must narrow down the voltage range as the range could cut into the ANEXT margin. The method of measuring the peak to peak value must be specified.

The peak to peak value of the waveform in Test 1 should be TBD in the range (2V to 2.5V) ± TBD%. This measurement is to be made for each pair while operating in test mode 1 by observing the differential signal output directly at the MDI using transmitter test fixture 1.

Editor's note: See http://www.ieee802.org/3/an/public/jul04/motions_1_0704.pdf

Material relevant to the motion is discussed in the following presentations:

http://www.ieee802.org/3/an/public/may04/gupta_1_0504.pdf

http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf

55.5.3.2 Maximum output droop

Editor's note: This is unapproved text

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and the negative droop over a period of 0.08 μsec measured after a settling time of TBD *(Editor recommends 10)* nsec after the zero crossing shall be less than TBD % *(Editor recommends 5.5%)* of the initial value.

Editor's Note: This test can be replaced by a test for the corner frequency of the transformer. The Editor's recommendation is based on the transformer high pass pole being at 100kHz with a 10% margin. For a discussion, see the presentation:

http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf

55.5.4 Transmitter linearity.

Editor's note: The general method was approved though the waveform must be approved by the Task Force and the number must be approved too.

When in test mode 4 and observing the spectrum of the differential signal output at the MDI using transmitter test fixture 2, for each pair, with no intervening cable, the transmitter linearity mask to be defined as follows.

The SFDR of the transmitter when subject to single tone inputs producing output with peak to peak transmit amplitude shall be:

better than X_{nonlin} dB in the frequency range, f ε (0.1, f_1] MHz, f_1 is in MHz

and better than [X_{nonlin}-$X_{nlslope}$*log10(f/f_1)] dB, for f ε (f_1, 800/6] MHz.

The Signal to Intermodulation distortion ratio of the transmitter, for dual tone inputs, producing output with peak to peak transmit amplitude, shall be better than:

[X_{nonlin} +2.5- $X_{nlslope}$*log10(f/f_1)] dB for f ε (800/6, 800/2]MHz

The specification on transmit linearity, is provided for the interoperability of the far end device. As a normative specification, the parameter X_{nonlin} = TBD *(Editor recommends 65)* dB, parameter f_1= TBD *(Editor recommends 25MHz)*, and parameter $X_{nlslope}$ = TBD *(Editor recommends 20dB)*. The recommended specification is X_{nonlin} = TBD dB and parameter $X_{nlslope}$ = TBD *(Editor recommends 0dB)*.

Editor's note: The above specification assumes a frequency domain approach to measuring transmitter nonlinearity. The rationale for taking the frequency domain approach was explained in section 55.5.2. Alternate proposals to this methodology/numbers chosen above are welcome.

The "normative" and "recommended" specification is provided in accordance with the motion in the IEEE July meeting.

http://www.ieee802.org/3/an/public/jul04/motions_1_0704.pdf

The recommended specification on transmitter linearity will enable the local receiver to achieve the echo cancellation required to meet its BER performance requirements without need for non-linear cancellers and external hybrids. If the transceiver uses other techniques to suppress the impact of local transmitter nonlinearity and can meet its performance requirements in their presence, compliance with the recommended linearity requirement is not required.

55.5.5 Transmitter timing jitter

Editor's note: This is unapproved text. Methodology borrowed from 1000BASE-T. Please suggest alternatives if you want it changed. The parameters J_1, J_2, J_{1filt}, J_{2filt}, bw1, bw2 are TBD.

When in test mode 2 or test mode 3, the peak-to-peak jitter J_{txout} of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX_TCLK is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be less than J_1. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be less than J_{1filt}.

$$H_{jf1}(f) = \frac{jf}{jf + bw1} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 55.5.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be less than J_2 after the receiver is properly receiving the data. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be no more than J_{2filt} greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$.

$$H_{jf2}(f) = \frac{jf}{jf + bw2} \qquad f \text{ in Hz}$$

For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least 10^6 clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

55.5.6 Transmitter power spectral density (PSD) and power level

In test mode 4, the the transmit power shall be in the range (TBD dBm, TBD dBm) and the power spectral density of the transmitter, measured using the test fixture shown in Figure 55–23 shall be below the mask specified in Figure 55–25 which corresponds to:

$$\text{PSD Mask (f)} = \begin{cases} -78\,\text{dBm/Hz} & 1 \le f \le 330 \\ -78 - \left(\frac{f-330}{40}\right)\text{dBm/Hz} & 330 < f \le 1850 \\ -116\,\text{dBm/Hz} & 1850 < f \le 3000 \end{cases} \qquad f \text{ is in MHz}$$

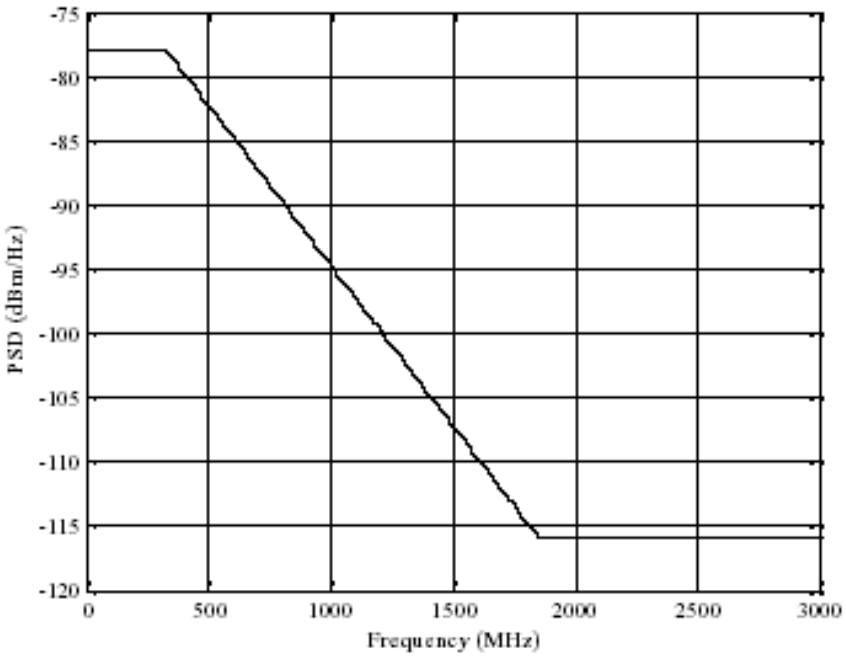


Figure 55–25—Transmitter power spectral density mask

55.5.7 Transmit clock frequency

The symbol transmission rate on each pair of the master PHY shall be F_s which is 800MHz ±TBD%

55.5.8 Receiver electrical specifications

The PMA shall provide the Receive function specified in 55.4.2.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall be within the limits specified in 55.7.

55.5.8.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 55.5.3 and have passed through a link specified in 55.7 are received with a BER less than 10^{-12} and sent to the PCS after link reset completion. This specification shall be satisfied by an LDPC frame error rate less than $3.2x10^{-9}$.

55.5.8.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a symbol rate within the range 800MHz ± TBD %.

55.5.9 Common-mode noise rejection

Editor's Note: This is un-approved text. The 2.8V number comes from the 1000BASE-T standard.

This specification is provided to limit the sensitivity of the PMA receiver to common-mode noise from the cabling system. Common-mode noise generally results when the cabling system is subjected to electromagnetic fields.

The common mode signal that the transceiver shall be subject to, while maintaining link performance, with a LDPC frame error rate less than $3.2x10^{-9}$, should be <= 2.8V for f ε (1,f_1] MHz, and <= 2.8*f_1/f for f ε (f_1, 500) MHz, f_1 in MHz.

Editor's note: Methodology to be agreed upon. Parameter f_1 TBD. Initial recommendation of f_1=80MHz. An appropriate test set-up TBD to realize and test the above specification up to 500MHz, similar to 1000BASE-T standard.

55.5.9.1 Alien Crosstalk noise rejection

While receiving data from a transmitter specified in 55.5.3 through a link segment specified in 55.7 connected to all MDI duplex channels, a receiver shall operate with an LDPC frame error rate of less than $3.2x10^{-9}$ with four noise sources at the specified levels representing alien NEXT, one connected to each of the four pairs. The noise sources shall be connected to each of the MDI inputs using Category 6 balanced cable of a maximum length of 0.5m. The noise source shall meet the ANEXT specifications in 55.7.3.4.

Editor's note: Please suggest specific ways to generate the ANEXT noise source. Some methods to generate the noise source to model ANEXT were discussed in the presentation:

http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf

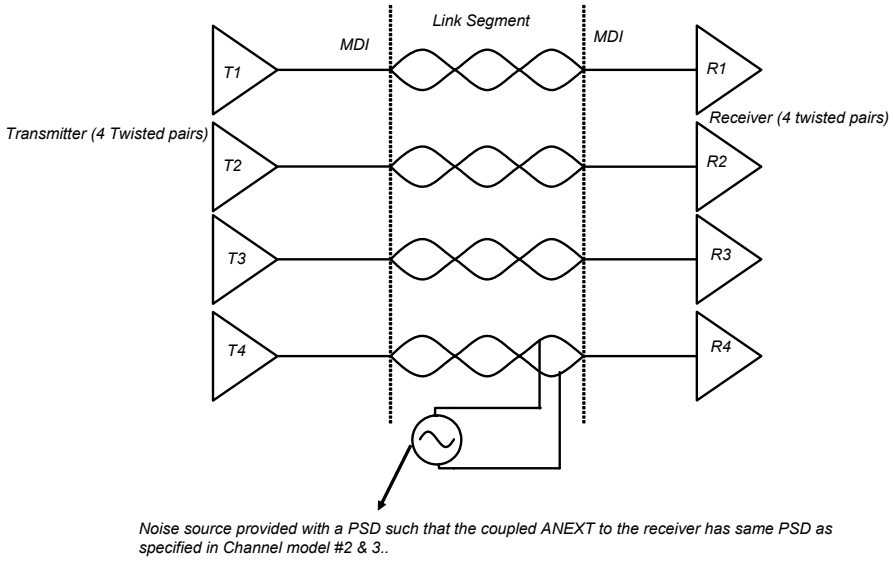


Figure 55–26—ANEXT noise rejection test

55.6 Management interface

10GBASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

55.6.1 Support for Auto-Negotiation

All 10GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE. All 10GBASE-T PHYs shall provide support for extended Next Pages as defined in 28.2.3.4.2#CrossRef# and shall support optimized FLP Burst to FLP burst timing as defined in 28.2.1.1.1 #CrossRef#.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for the following two primary purposes for 10GBASE-T:

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

This relationship is necessary for establishing the timing control of each PHY. The 10GBASE-T MASTER PHY is clocked from a local source. The SLAVE PHY uses loop timing where the clock is recovered from the received data stream.

55.6.1.1 10GBASE-T use of registers during Auto-Negotiation

A 10GBASE-T PHY shall use the management register definitions and values specified in Table 55–4 #CrossRef#.

Table 55–4—10GBASE-T Registers

Register	Bit	Name	Description	Type [a]
0	0.15:0	MII control register	Defined in 28.2.4.1.1	RO
1	1.15:0	MII status register	Defined in 28.2.4.1.2	RO
4	4.15:0	Auto-Negotiation advertisement register	The Selector Field (4.4:0) is set to the appropriate code as specified in Annex 28A. The Technology Ability Field bits 4.12:5 are set to the appropriate code as specified in Annexes 28B and 28D. Bit 4.15 is set to logical one to indicate the desired exchange of Next Pages describing the gigabit extended capabilities.	R/W
5	5.15:0	Auto-Negotiation link partner ability register	Defined in 28.2.4.1.4. 10GBASE-T implementations do not use this register to store Auto-Negotiation Link Partner Next Page data.	RO
6	6.15:0	Auto-Negotiation expansion register	Defined in 28.2.4.1.5	RO
7	7.15:0	Auto-Negotiation Next Page transmit register	Defined in 28.2.4.1.6	R/W
8	8.15:0	Auto-Negotiation link partner Next Page register	Defined in 28.2.4.1.8	RO
TBD	TBD	Test mode bits	TBD	R/W

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

Table 55–4—10GBASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
TBD	TBD	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual configuration value 0=Disable MASTER-SLAVE Manual configuration value Default bit value is 0.	R/W
TBD	TBD	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when TBD is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when TBD is set to logical one. Default bit value is 0.	R/W
TBD	TBD	Port type	Bit TBD is to be used to indicate the preference to operate as MASTER (multiport device) or as SLAVE (single-port device) if the MASTER-SLAVE Manual Configuration Enable bit, TBD, is not set. Usage of this bit is described in TBD. 1=Multiport device 0=single-port device	R/W
TBD	TBD	10GBASE-T Full Duplex	1 = Advertise PHY is 10GBASE-T full duplex capable. 0 = Advertise PHY is not 10GBASE-T full duplex capable.	R/W
TBD	TBD	Reserved	Write as 0, ignore on read.	R/W
TBD	TBD	MASTER-SLAVE configuration fault	Configuration fault, as well as the criteria and method of fault detection, is PHY specific. The MASTER-SLAVE Configuration Fault bit will be cleared each time register TBD is read via the management interface and will be cleared by a 10GBASE-T PMA reset. This bit will self clear on Auto-Negotiation enable or Auto-Negotiation complete.This bit will be set if the number of failed MASTER-SLAVE resolutions reaches TBD. For l0GBASE-T, the fault condition will occur when both PHYs are forced to be MASTERs or SLAVEs at the same time using bits TBD and TBD. Bit TBD should be set via the MASTER-SLAVE Configuration Resolution function described in TBD. 1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC
TBD	TBD	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO
TBD	TBD	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status=OK) 0 = Local Receiver not OK (loc_rcvr_status=NOT_OK) Defined by the value of loc_rcvr_status as per TBD.	RO
TBD	TBD	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status=OK) 0 = Remote Receiver not OK (rem_rcvr_status=NOT_OK) Defined by the value of rem_rcvr_status as per TBD.	RO
TBD	TBD	LP 10GBASE-T FD	1 = Link Partner is capable of 10GBASE-T full duplex 0 = Link Partner is not capable of 10GBASE-T full duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

Table 55–4—10GBASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
TBD	TBD	Reserved	Reserved	RO
TBD	TBD	Idle Error Count	Bits TBD indicate the Idle Error count, where TBD is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and are to be held at all ones in case of overflow (see TBD).	RO/SC
TBD	TBD	Extended status register	See 22.2.4.4	RO

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

55.6.1.2 10GBASE-T Auto-Negotiation page use

10GBASE-T PHYs shall exchange a 10GBASE-T and 1000BASE-T formatted extended Next Page, as specified in Table 55-7 #CrossRef#, immediately following the exchange of the Base Page

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 10GBASE-T message page exchange.

Table 55–5—10GBASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
BASE PAGE		
D15	1 (to indicate that Next Pages follow)	
D14:D13	As specified in 28.2.1.2	Management register 4
D12	1 (to indicate extended Next Pages follow)	Management register 4
D11:D0	As specified in 28.2.1.2	Management register 4
Extended Next Page (Message Code Field and Flags Field)		
M10:M0	9	
T	As specified in 28.2.3.4.7	
Ack2	0	
MP	1 (to indicate this is the	
Ack	As specified in 28.2.3.4.4	
NP	As specified in 28.2.3.4.3	
Extended Next Page (Unformatted Message Code Field)		
U31:U20	Reserved transmit as 0	
U19		
U18		
U17	Loop Timing (1 = support of Loop Timing and 0 = no support)	Register TBD

Table 55–5—10GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Bit definition	Register location
U16	10GBASE-T (1 = support of 10GBASE-T and 0 = no support)	GMII register TBD (MASTER-SLAVE Control register)
U15	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	GMII register TBD (MASTER-SLAVE Control register)
U14	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	GMII register TBD (MASTER-SLAVE Control register)
U13	Port type bit (1 = multiport device and 0 = single-port device)	GMII register TBD (MASTER-SLAVE Control register)
U12	10GBASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE.) This bit is ignored if TBD =0.	GMII register TBD (MASTER-SLAVE Control register)
U11	10GBASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit TBD.	GMII register TBD (MASTER-SLAVE Control register)
U10	MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value(10:0)
U9	MASTER-SLAVE Seed Bit 9 (SB9)	
U8	MASTER-SLAVE Seed Bit 8 (SB8)	
U7	MASTER-SLAVE Seed Bit 7 (SB7)	
U6	MASTER-SLAVE Seed Bit 6 (SB6)	
U5	MASTER-SLAVE Seed Bit 5 (SB5)	
U4	MASTER-SLAVE Seed Bit 4 (SB4)	
U3	MASTER-SLAVE Seed Bit 3 (SB3)	
U2	MASTER-SLAVE Seed Bit 2 (SB2)	
U1	MASTER-SLAVE Seed Bit 1 (SB1)	
U0	MASTER-SLAVE Seed Bit 0 (SB0)	

55.6.1.3 Sending Next Pages

Implementors who do not wish to send additional Next Pages (i.e., Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28 and the Next Pages defined in 50.6.1.2 #CrossRef#. Implementors who wish to send additional Next Pages are advised to consult Annex 40C.

55.6.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using TBD with the 10GBASE-T Technology Ability Next Page bit values specified in TBD and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–13.)

The following four equations are used to determine these relationships:

manual_MASTER = U0 * U1
manual_SLAVE = U0 * !U1

single-port device = !U0 * !U2,
multiport device = !U0 * U2

where

U0 is bit 0 of unformatted page 1,
U1 is bit 1 of unformatted page 1, and
U2 is bit 2 of unformatted page 1 (see Table 55–5).

A 10GBASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies may result in contention. The resolution function of TBD is defined to handle any relationship conflicts.

In the instance when both link partners support the optional Loop Timing mode, as designated by bit U17, the resolution shown inTable 55–6 shall be used. When only one link partner supports Loop Timing, the device that supports Loop Timing shall be forced to SLAVE and the other device shall be forced to MASTER.

Table 55–6—10GBASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

The rationale for the hierarchy illustrated in Table 55–6 is straightforward. A 10GBASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_10GigT=FAIL (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementor. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to $2^{11}-2$. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 10.15 shall be set to logical zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit TBD) and the MASTER-SLAVE Config Value bit (control register bit TBD) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Configuration fault condition, thus the MASTER-SLAVE Configuration fault bit (status register bit TBD) shall be set to logical one. The MASTER-SLAVE Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_1GigT shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–16) when the highest common denominator (HCD) technology is 10GBASE-T. The resulting MASTER-SLAVE value is used by the 10GBASE-T PHY control (TBD).

If MASTER-SLAVE Manual Configuration is disabled (bit TBD is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit TBD of the 10GBASE-T Status Register is set to logical zero and bit TBD is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 10GBASE-T returns control to Auto_Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–16) and passes the value MASTER or SLAVE to PMA_CONFIG.indicate (see TBD.)
b) *Unsuccessful:* link_status_10GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–16.)
c) *Fault detected:* (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit TBD of the 10GBASE-T Status Register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER SLAVE relationship via the seed method have failed. When a fault is detected, link_status_10GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 10GBASE-T is selected as the highest common denominator; otherwise, it is assumed to have passed this condition

55.7 10GBASE-T link segment characteristics

10GBASE-T is designed to operate over ISO/IEC 11801 Class E or Class F 4-pair balanced cabling that meets the additional requirements specified in this subclause. Each of the four pairs supports an effective data rate of 2500 Mb/s in each direction simultaneously. The term "link segment" used in this clause refers to four duplex channels. Specifications for a link segment apply equally to each of the four duplex channels. All implementations of the balanced cabling link segment specification shall be compatible at the MDI.

55.7.1 Cabling system characteristics

The cabling system used to support 10GBASE-T requires 4 pairs of ISO/IEC 11801 Class E or Class F balanced cabling with a nominal impedance of 100 Ω.

Additionally:

a) 10GBASE-T uses a star topology with Class E or Class F balanced cabling used to connect PHY entities.
b) 10GBASE-T is an ISO/IEC 11801 Class E and Class F application with the additional transmission requirements specified in this subclause.

55.7.2 10GBASE-T link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a 10GBASE-T link segment consisting of at least 55 to 100 meters of Class E and a 10GBASE-T link segment consisting of 100 meters of Class F respectively will provide a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, nominal impedance, NEXT loss, ELFEXT loss, and return loss. In addition, the requirements for the alien crosstalk coupled "between" link segments is specified.

Link segment testing shall be conducted using source and load impedances of 100 Ω.

The link segment transmission parameters of insertion loss and ELFEXT loss specified are ISO/IEC 11801 Class E specifications extended by extrapolating the formulas to a frequency up to 500 MHz. The link segment transmission parameters of NEXT loss, MDNEXT loss and Return Loss specified are ISO/IEC 11801 Class E specifications extended beyond 250 MHz by utilizing the equations referenced in TIA TR42 D1.1a TSB-155.

55.7.2.1 Insertion loss

The insertion loss of each duplex channel shall be less than

$$1.05\left(1.82\times\sqrt{f}+0.0169\times f+\frac{0.25}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f} \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 500 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

55.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 500 MHz.

55.7.2.3 Return loss

Each link segment duplex channel shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 500 MHz. The reference impedance shall be 100 Ω.

$$\text{Return\_Loss}(f) = \begin{Bmatrix} 19 & 1 \le f < 10 \\ 24 - 5\log 10(f) & 10 \le f < 40 \\ 32 - 10\log 10(f) & 40 \le f < 400 \\ 6 & 400 \le f \le 500 \end{Bmatrix} \quad \text{(dB)}$$

where f is the frequency in MHz.

55.7.3 Coupling parameters

55.7.3.1 Coupling parameters between duplex channels

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. In addition, each duplex channel can be disturbed by more than one duplex channel. To ensure the total NEXT loss and FEXT loss coupled into a duplex channel is limited, multiple disturber Near-End Crosstalk (MDNEXT) and multiple disturber ELFEXT (MDELFEXT) loss is specified.

55.7.3.1.1 Near-End Crosstalk (NEXT)

55.7.3.1.1.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the bit error rate objective specified in 55.1. The NEXT loss between any two duplex channels of a link segment shall be at least

$$-20 \times \log 10\left(10^{\frac{74.3 - 15\log 10(f)}{-20}} + 2 \times 10^{\frac{94 - 20\log 10(f)}{-20}}\right) \quad \text{(dB)}$$

where f is the frequency $(1 \le f < 330)$ in MHz.

The NEXT loss between any two duplex channels of a link segment shall be at least

$$31 - 50 \times \log 10\left(\frac{f}{330}\right) \quad \text{(dB)}$$

where f is the frequency $(330 \le f \le 500)$ in MHz.

55.7.3.1.1.2 Multiple Disturber Near-End Crosstalk (MDNEXT) loss

Since four duplex channels are used to transfer data between PMDs, the NEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels.

To ensure the total NEXT coupled into a duplex channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses. The Power Sum loss between a duplex channel and the three adjacent disturbers shall be greater than

$$-20 \times \log 10\left(10^{\frac{72.3 - 15\log 10(f)}{-20}} + 2 \times 10^{\frac{90 - 20\log 10(f)}{-20}}\right) \quad \text{(dB)}$$

where f is the frequency $1 \le f < 330$ in MHz and

$$28 - 42 \times \log 10\left(\frac{f}{330}\right) \quad \text{(dB)}$$

where f is the frequency $(330 \le f \le 500)$ in MHz.

55.7.3.1.1.3 Multiple-Disturber Power Sum Near-End Crosstalk (PS NEXT) loss

PS NEXT loss is determined by summing the power of the three individual pair-to-pair differential NEXT loss values over the frequency range 1 MHz to 500 MHz. as follows:

$$-10 \times \log 10 \sum_{i=1}^{n} 10^{\frac{-NL(f)i}{10}} \quad \text{(dB)}$$

where

NL(f)i is the magnitude in dB of NEXT loss at frequency f of pair combination i

i is the 1, 2, or 3 (pair-to-pair combination)

n is the number of pair-to-pair combinations

55.7.3.1.2 Far-End Crosstalk (FEXT)

55.7.3.1.2.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in 55.1.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end.

Editor's Note: For 1000BASE-T the error rate is specified as symbol error rate, frame error rate and bit error rate. For 10GBASE-T D1.0, as a starting point, the BER objective of 10^-12 specified in 55.1 will be utilized throughout subclause 55.7.

FEXT loss is defined as

$$\text{FEXT\_Loss(f)} = 20 \times \log 10\left(\frac{V_{pds(f)}}{V_{pcn(f)}}\right) \qquad \text{(dB)}$$

and ELFEXT_Loss is defined as

$$\text{ELFEXT\_Loss(f)} = 20 \times \log 10\left(\frac{V_{pds(f)}}{V_{pcn(f)}}\right) - \text{SLS\_Loss(f)} \qquad (dB)$$

where

*V*pds	is the peak voltage of disturbing signal (near-end transmitter)
*V*pcn	is the peak crosstalk noise at far end of disturbed channel
SLS_Loss	is the insertion loss of disturbed channel in dB

The worst pair ELFEXT loss between any two duplex channels shall be greater than

$$-20 \times \log 10\left(10^{\frac{67.8 - 20\log 10(f)}{-20}} + 4 \times 10^{\frac{83.1 - 20\log 10(f)}{-20}}\right) \qquad \text{(dB)}$$

where *f* is the frequency over the range of 1 MHz to 500 MHz.

55.7.3.1.2.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses. The Power Sum loss between a duplex channel and the three adjacent disturbers shall be greater than

$$-20 \times \log 10\left(10^{\frac{64.8 - 20\log 10(f)}{-20}} + 4 \times 10^{\frac{80.1 - 20\log 10(f)}{-20}}\right) \quad \text{(dB)}$$

where *f* is the frequency over the range of 1 MHz to 500 MHz.

55.7.3.1.2.3 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PS ELFEXT) loss

PS ELFEXT loss is determined by summing the power of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 1 MHz to 500 MHz as follows:

$$\text{PSELFEXT\_Loss(f)} = -10 \times \log_{10} \sum_{i=1}^{i=n} 10^{\frac{-EL(f)i}{10}}$$

where

EL(*f*)i is the magnitude of ELFEXT loss at frequency *f* of pair combination i
i is the 1, 2, or 3 (pair-to-pair combination)
n is the number of pair-to-pair combinations

55.7.3.2 Coupling parameters between link segments

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise.To ensure the total Alien NEXT loss and Alien FEXT loss coupled between link segments is limited, multiple disturber Alien Near-End Crosstalk (MD ANEXT) and multiple disturber Alien FEXT (MDAFEXT) loss is specified. In addition, to ensure the reliable operation of the link segment, a minimum alien crosstalk to insertion loss ratio is specified.

Editor's Note: Text needs to be added to clearly identify the alien crosstalk dependencies.

55.7.3.2.1 Multiple Disturber Alien Near-End Crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error rate objective specified in 55.1. To ensure the total Alien NEXT coupled into a duplex channel is limited, multiple disturber Alien NEXT loss is specified as the power sum of the individual Alien NEXT disturbers.

55.7.3.2.1.1 Multiple-Disturber Power Sum Near-End Crosstalk (PS ANEXT) loss

ANEXT loss is determined by summing the power of the individual pair-to-pair differential Alien NEXT loss values over the frequency range 1 MHz to 500 MHz. as follows:

$$-10 \times \log 10 \sum_{i=1}^{n} 10^{\frac{-AN(f)i}{10}} \quad \text{(dB)}$$

where

AN(f)i is the magnitude in dB of ANEXT loss at frequency f of pair combination i

i is the pair-to-pair combination (1 to n)

n is the number of pair-to-pair combinations between link segments

The Power Sum ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is defined by the equations:

$$PSANEXT \geq \begin{cases} X1 - 10\log 10(\frac{f}{100}) \ \ (dB) & 1 \leq f \leq 100 \\ X1 - 15\log 10(\frac{f}{100}) \ \ (dB) & 100 < f \leq 500 \end{cases}$$

where f is the frequency in MHz and X1 = the intercept at f=100 MHz.

The intercept is referred to as the PS ANEXT constant. The PS ANEXT constant is determined in 55.7.3.2.2 constrained by the ratio of the PS ANEXT to the insertion loss.

55.7.3.2.2 PS ANEXT loss to insertion loss ratio requirements

To ensure reliable operation, a minimum insertion loss to alien crosstalk ratio must be maintained. The PS ANEXT loss requirement of 55.7.3.2.2.1 can be relaxed based on a reduction in the maximum insertion loss specified in 55.7.2.1. The insertion loss reduction can be achieved by scaling the length of a link segment consisting of Class E cabling or using a link segment consisting of Class F cabling or using a link segment consisting of Augmented Category 6 (Augmented Class E) cabling.

The adjusted PS ANEXT loss requirement is determined by first calculating the PS ANEXT_constant and utilizing the constant in the PS ANEXT limit line model.

The PS ANEXT_constant is defined by the following equation:

$$\text{PSANEXT\_constant} = 62 - (\text{CE\_IL\_250}MHz - \text{SCE\_IL\_250}MHz) \times \frac{15}{15.6} \quad \text{(dB)}$$

where

CE_IL_250 MHz is the Class E insertion loss at 250 MHz

SCE_IL_250 MHz is the scaled Class E insertion loss at 250 MHz

For the purpose of calculating the scaled Class E insertion loss at 250 MHz, the cable insertion loss is assumed to scale linearly with length.Insertion Loss Scaling

The Scaled Class E IL is defined by the following equation:

$$\text{Scaled\_Class\_E\_IL} = \frac{\text{Length\_m}}{100} \times 1.05\left(1.82 \times \sqrt{f} + 0.0169 \times f + \frac{0.25}{\sqrt{f}}\right) + 4 \times 0.02 \times \sqrt{f}\ (\text{dB})$$

where Length_m is in meters

.Table 1 lists the calculated PS ANEXT_constants for the cabling types and distances.

Table 1—PS ANEXT Constants for cabling types and distances

Cabling	Distance	PS ANEXT_ constant	Insertion Loss
Class E	100 meters	62	55.7.2.1
Class E	55 meters	47	55.7.3.2.6
Class F	100 meters	60	55.7.3.2.4
Augmented Category 6	100 meters	60	55.7.3.2.5

Note: The PS ANEXT constants in Table 1 are for certification of the channel. For simulating PHY performance to estimate system margin, the PS ANEXT constants must be increased by 2.5 dB. This represents the difference between the limit line, which is used for channel certification, and the average value of PS ANEXT which will be lower than the limit line.

Editors Note: Alien crosstalk is not adequately specified in the ISO/IEC 11801 or TIA cabling standards. The PS ANEXT limits provided below for Class E, Class F, and augmented Category 6 are the minimum requirements for 100 meter operation and are not intended to represent the PS ANEXT performance limits of the cabling (i.e., the PS ANEXT performance of the cabling may be better than the minimum requirements specified in 10GBASE-T). Both TIA and ISO/IEC have initiated projects in support 10GBASE-T. TR42 has initiated Project SP-3-4426-AD10 to develop augmented Category 6 cabling. The resulting requirements will be presented in a new revision or addendum to the TIA-568-B standard.

55.7.3.2.2.1 PS ANEXT for a Class E Channel

For a link segment consisting of a 100 meter Class E channel with the maximum insertion loss of 55.7.3.1 the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT \geq \begin{cases} 62 - 10\log 10\left(\frac{f}{100}\right) \quad (dB) & 1 \leq f \leq 100 \\ 62 - 15\log 10\left(\frac{f}{100}\right) \quad (dB) & 100 < f \leq 500 \end{cases}$$

55.7.3.2.2.2 PS ANEXT for a Class F Channel

For a link segment consisting of a 100 meter Class F channel the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT \geq \left\{ \begin{array}{ll} 60 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ 60 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{array} \right\}$$

where f is the frequency in MHz.

The PS ANEXT for a Class F channel specified in 55.7.3.2.1.3 assumes the maximum insertion loss of a Class F channel in 55.7.3.2.5

55.7.3.2.2.3 PS ANEXT for an Augmented Category 6 (Augmented Class E) Channel

For a link segment consisting of a 100 meter Augmented Category 6 (Augmented Class E) channel the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT \geq \left\{ \begin{array}{ll} 60 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ 60 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{array} \right\}$$

The PS ANEXT for an Augmented Category 6 (Augmented Class E) Channel specified in 55.7.3.2.1.4 assumes the maximum insertion loss of an Augmented Category 6 (Augmented Class E) channel in 55.7.3.2.6.

55.7.3.2.2.4 PS ANEXT for a Category 6 channel of 55 meters

For a Category 6 channel of 55 meters with worst case insertion loss of 55.7.3.2.7 the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT > \left\{ \begin{array}{ll} 47 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ 47 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{array} \right\}$$

where f is the frequency in MHz.

Editor's note: PSAFEXT limits need to be added with reference to test methods.

55.7.3.2.3 Multiple Disturber Alien Far-End Crosstalk (MDAFEXT) loss (ffs)

55.7.3.2.3.1 Multiple -Disturber Power Sum Alien Far-End Crosstalk (PS AFEXT) loss (ffs)

55.7.3.2.4 Insertion Loss for a Class F Channel

The PS ANEXT for a Class F Channel assumes the maximum insertion loss of a Class F channel.

The insertion loss of a Class F duplex channel shall be less than

$$1.05\left(1.8 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 4 \times 0.02 \times \sqrt{f} \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 500 MHz. This includes the attenuation of the balanced cabling pairs, including the cords and connecting hardware losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

NOTE— The Class F insertion loss is an improvement of 2.1 dB at 250 MHz over the Class E insertion loss specifications resulting in a 2 dB relaxation in the Class F PS ANEXT requirement.

55.7.3.2.5 Insertion Loss for an Augmented Category 6 (Augmented Class E) Channel

The insertion loss of an Augmented Category 6 (Augmented Class E) Channel shall be less than

$$1.05\left(1.8\times\sqrt{f}+0.01\times f+\frac{0.2}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f}\qquad\text{(dB)}$$

at all frequencies from 1 MHz to 500 MHz. This includes the attenuation of the balanced cabling pairs, including the cords and connecting hardware losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

55.7.3.2.6 Insertion Loss of a Category 6 channel of 55 meters

ISO/IEC 11801 classes for balanced cabling refer to cabling channel distances of 100 meters. For cabling channels less than 100 meters the Category of the components comprising the channel applies (e.g., Category 6 components provide Class E balanced cabling performance).

The insertion loss of a Category 6 channel of 55 meters is defined by the following equation:

$$\text{Scaled\_Class\_E\_IL}(55m)=\frac{55}{100}\times 1.05\left(1.82\times\sqrt{f}+0.0169\times f+\frac{0.25}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f}\,(\text{dB})$$

55.7.4 Delay

In order to simultaneously send data over four duplex channels in parallel, the propagation delay of each duplex channel as well as the difference in delay between any two of the four channels are specified. This ensures the 10 Gb/s data that is divided across four channels can be properly reassembled at the far-end receiver.

55.7.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 500 MHz.

55.7.4.2 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 2 MHz to 500 MHz. It is a further

functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns within the above requirement.

55.7.5 Noise environment

Editor's Note: The noise environment (55.7.5) sub clause is extracted from 1000BASE-T specification with minor changes. This text will likely evolve to reflect the 10GBASE-T noise environment assumptions.

The 10GBASE-T noise environment consists of noise from many sources. The primary noise sources that impact the objective BER are NEXT and echo interference, which are reduced to a small residual noise using cancellers. The remaining noise sources, which are secondary sources, are discussed in the following list. The 10GBASE-T noise environment consists of the following:

a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bi-directional transmission of data and by impedance mismatches in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.

b) Near-End Crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver will experience NEXT interference from three adjacent transmitters. NEXT cancellers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor.

c) Far-End Crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be cancelled in the same way as echo and NEXT interference although the symbols from the remote transmitters are not immediately available.

d) Inter-Symbol Interference (ISI) noise. ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same channel.

e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and non-linear channel characteristics.

f) Noise coupled between link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise.Since the transmitted symbols from the alien NEXT noise source are not available to the cancellation processor (they are in another cable), it is very difficult to cancel the alien NEXT noise. To ensure robust operation the alien NEXT noise must meet the specification of 55.7.5.

g) The background noise for 10GBASE-T is expected not to exceed -150 dBm/Hz.. A background noise limit of -150 dBm/Hz was assumed in the 10GBASE-T Matlab simulation models.

55.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 55.4.4 for a description of the automatic MDI/MDI-X configuration.

55.8.1 MDI connectors

Eight-pin connectors meeting the requirements of subclause 3 and Figures 1 through 4 of IEC 60603-7: 1995 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 55–29 and Figure 55–30. The assignment of PMA signals to connector contacts for PHYs is shown in Table 55–9. The PHY shall be capable of reversing the polarity of the contacts for any PMA signal to correct for a mis-wired channel between any two PHY entities within the link segment.

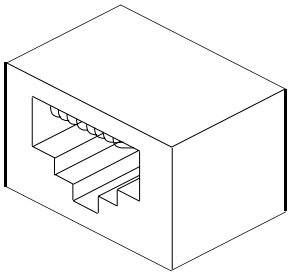


Figure 55–29—MDI connector

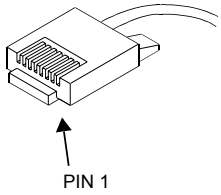


Figure 55–30—Balanced cabling connector

Table 55–9—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

55.8.2 Crossover function

It is a functional requirement that a crossover function be implemented in every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers

of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or else-where in the link segment. The MDI connector for a 10GBASE-T PHY shall be marked with the graphical symbol X. The crossover function specified here is not compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a single-port device to a multiport device, it is recommended that the crossover be implemented in the PHY local to the multiport device. It is recommended that the crossover be visible to an installer from one of the PHYs. It is further recommended that, in networks in which the topology identifies either a central backbone segment or a central device, the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

Editor's note: The MDI crossover function has been made mandatory rather than optional.

55.8.3 MDI electrical specifications

The MDI connector (jack) when mated with a specified balanced cabling connector (plug) shall meet the electrical requirements for Category 6 connecting hardware for use with 100-ohm Category 6 cable as specified in ANSI/TIA/EIA-568-B.2:2002 and ISO/IEC 11801:2002.

The mated MDI/balanced cabling connector pair shall have a FEXT loss not less than $43.1 - 20\log_{10}(f/100)$ (where f is the frequency over the range 1 MHz to 500 MHz) between all contact pair combinations shown in Table 55–9.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5), when released from power-down mode, or when external power is first applied to the PHY.

55.8.3.1 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω ± TBD% is attenuated, relative to the incident signal, at least 16 dB over the frequency range of 1.0 MHz to 40 MHz and at least $16 - 10\log_{10}(f/40)$ dB over the frequency range 40 MHz to 500 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data or control symbols.

55.8.3.2 MDI impedance balance

Impedance balance is a measurement of the impedance-to-ground difference between the two MDI contacts used by a duplex link channel and is referred to as common-mode-to-differential-mode impedance balance. Over the frequency range 1.0 MHz to 500.0 MHz, the common-mode-to-differential-mode impedance balance of each channel of the MDI shall exceed:

$$45 - 4\log_{10}\left(\frac{f}{50}\right) \quad \text{dB}$$

where f is the frequency in MHz when the transmitter is transmitting random or pseudo random data. Test-mode 4 may be used to generate an appropriate transmitter output. The balance is defined as:

$$20\log_{10}\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 55–31 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.

NOTES

1—Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

2—The imbalance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

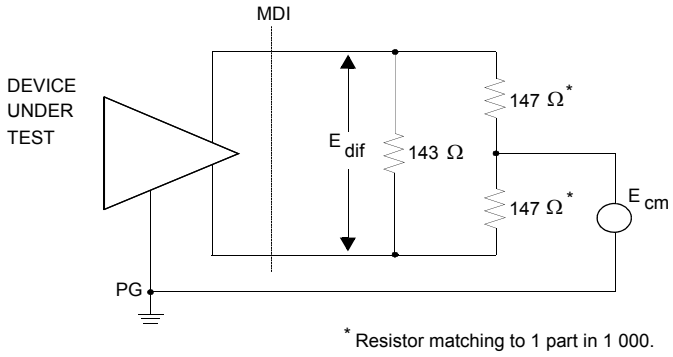


Figure 55–31—MDI impedance balance test circuit

Editor's note: The impedance balance equation was obtained by processing the data provided by Pulse on the magnetics. Other factors contributing to the imbalance may require us to modify the above requirement. Please provide feedback on the feasibility of the above proposal.

55.8.3.3 MDI common-mode output voltage

The magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 55–32, shall be less than 15 mV peak-to-peak when transmitting data.

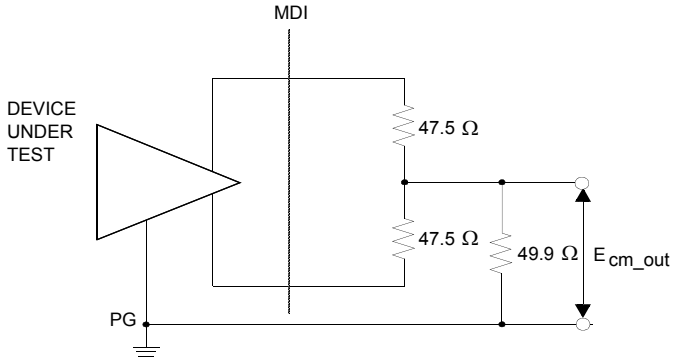


Figure 55–32—Common-mode output voltage test circuit

Editor's note: 1000BASE-T specified 50 mV as the maximum permissible common-mode output voltage. That number has been reduced to 15 mV to because reducing it should make it easier to pass EMI. We need feedback from the Task Force on whether this value is feasible from an implementation point of view from both the PHY vendors and the magnetics manufacturers.

NOTE—The imbalance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

55.8.3.4 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

A powered MDI will not disrupt 10GBASE-T and vice versa.

Each wire pair shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 55–33). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

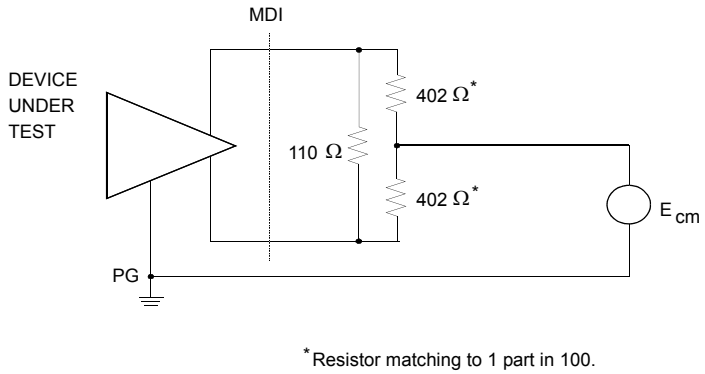


Figure 55–33—MDI fault tolerance test circuit

55.9 Environmental specifications

55.9.1 General safety

All equipment meeting this standard shall conform to IEC 60950-1: 2001.

55.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational

system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

Editor's note: References have been updated; the frequency range of interest is now from 1MHz to 500MHz. The equations have been updated to reflect this and the formulae have been adjusted.

55.9.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

55.9.4 Telephone voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10GBASE-T. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard. The following maximums generally apply.

a) Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.
a) Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10GBASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltage shall not result in any safety hazard.

55.9.5 Electromagnetic emissions

A system integrating the 10GBASE-T shall comply with applicable local and national codes for the limitation of electromagnetic interference.

55.9.6 Temperature and humidity

A system integrating the 10GBASE-T is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

55.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Gb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 10GBASE-T)
d) Any applicable safety warnings

55.11 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI.

55.11.1 MDI to XGMII delay constraints

Every 10GBASE-T PHY associated with a XGMII shall comply with the bit delay constraints specified in Table 55–10 for full duplex operation. These constraints apply for all 10GBASE-T PHYs.

Table 55–10—MDI to XGMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
XGMII ⇔ MDI ⇔XGMII	SFD coming in on XGMII on one PHY and coming out of the XGMII on the other PHY with two PHYs connected back to back with 10m cable	—	TBD	TBD	TBD
XGMII ⇔ MDI	TBD	—	TBD	TBD	TBD

Editor's note: Delay is measureable easily on two PHYs connected back to back however this delay will vary depending on timing of arrival of the SFD on the XGMII relative to start of LDPC code. Delay from XGMII to MDI will be hard to measure because all symbols are encoded and buried inside LDPC code words. It may make sense to have an optional flag put in which is detectable on the MDI port solely to enable easy detection of delays while testing.

55.12 Protocol implementation conformance statement (PICS) proforma for Clause 55—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 10GBASE-T[5]

The supplier of a protocol implementation that is claimed to conform to this clause shall complete the Protocol Implementation Conformance Statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so it can be used for its intended purpose and may further publish the completed PICS.

55.12.1 Identification

55.12.1.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTES 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

55.12.1.2 Protocol summary

Identification of protocol specification	IEEE Std 802.an:?, Clause 55, Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer, and baseband medium, type 10GBASE-T
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21—The answer Yes means that the implementation does not conform to the standard)	
Date of Statement	

55.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*XGMII	PHY associated with XGMII	TBD	O	Yes [ ] No [ ]	

55.12.3 Clause conventions

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	The values of all components in test circuits shall be	TBD	M	Yes [ ]	Accurate to within ±1% unless otherwise stated.

55.12.4 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	The PCS shall	TBD	M	Yes [ ]	

55.12.4.1 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function shall	TBD	M	Yes [ ]	

55.12.4.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	TBD	M	Yes [ ]	

55.12.5 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	TBD	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity or from PHY Control.
PMF2	PMA Transmit shall	TBD	M	Yes [ ]	
PMF3	The four transmitters shall be driven by the same transmit clock, TX_TCLK	TBD	M	Yes [ ]	
PMF4	PMA Transmit shall	TBD	M	Yes [ ]	Follow the mathematical description given in TBD.
PMF5	PMA Transmit shall comply with	TBD	M	Yes [ ]	The electrical specifications given in TBD.
PMF6	When the PMA_CONFIG.indicate parameter config is MASTER, the PMA Transmit function shall	TBD	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of TBD.
PMF7	When the PMA_CONFIG.indicate parameter config is SLAVE, the PMA Transmit function shall	TBD	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock of TBD while meeting the jitter requirements of TBD.

55.12.6 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	All 10GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.	TBD	M	Yes [ ]	

55.12.6.1 10GBASE-T Specific Auto-Negotiation Requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	10GBASE-T PHYs shall	TBD	M	Yes [ ]	TBD
AN2	The MASTER-SLAVE relationship shall be determined during Auto-Negotiation	TBD	M	Yes [ ]	TBD

55.12.7 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME3	The PHY shall provide electrical isolation between	TBD	M	Yes [ ]	The port device circuits including frame ground, and all MDI leads.

55.12.8 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	All implementations of the balanced cabling link shall	TBD	M	Yes [ ]	Be compatible at the MDI.

55.12.9 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	TBD	M	Yes [ ]	8-Way connector as per IEC TBD.