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(Draft Amendment of IEEE Std 802.3-2008)

IEEE *Draft* P802.3az™/D3.2

Draft Standard for Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—
Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment:
Media Access Control parameters, Physical Layers and management parameters for Energy-Efficient Ethernet

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2008 and includes a new clause, Clause 78, which provides an overview of changes required to enable energy efficient operation of several existing physical layers. Changes to the specifications of these physical layers are also included in this draft. Draft D3.2 is prepared by the IEEE 802.3az Energy Efficient Task Force for sponsor ballot recirculation. This draft reflects changes made in response to the comment resolutions and motions from the task force meeting held in July 2010 and expires 6 months after the date of publication or when the next version is published, whichever comes first.

IEEE Standards Activities Department
445 Hoes Lane
Piscataway, NJ 08854, USA

Abstract: This amendment to IEEE Std 802.3–2008 specifies changes to several existing physical layers to enable energy efficient operation of Ethernet. Changes to 10BASE-T include a reduction in transmit voltage requirements. Changes to 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KX4 and 10GBASE-KR include the definition of a Low Power Idle (LPI) mode and mechanisms to communicate and manage the entry and exit into and out of LPI and the operation of this mode. New LLDP TLVs are defined for negotiating system level energy efficiency parameters.
Keywords: 802.3az, 10BASE-T, 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, Backplane Ethernet, Energy Efficient Ethernet (EEE), Low Power Idle Mode (LPI), TLV, LLDP

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

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Introduction

Editor's Note (to be removed prior to publication):

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

One exceptions to IEEE style that is consciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecutively with arabic page numbers.

This introduction is not part of IEEE Std 802.3az-2010, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements, Part 3: CSMA/CD Access Method and Physical Layer Specifications, Amendment: Energy Efficient Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE 802.3az-20XX).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x™ specified full duplex operation and a flow control protocol, IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in, and are superseded by, IEEE Std 802.3-2008 and are not maintained as separate documents.

At the date of IEEE Std 802.3az-20XX publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2008

Section One -- Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two -- Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three -- Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four -- Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five -- Includes Clause 56 through Clause 74 and Annex 57A through Annex 74A. Clause 56 through Clause 67 and associated annexes specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

IEEE Std 802.3av™-2009

This amendment includes changes to IEEE Std 802.3-2008 and adds Clause 75 through Clause 77 and Annex 75A through Annex 76A. This amendment adds new Physical Layers for 10 Gb/s operation on point-to-multipoint passive optical networks.

IEEE Std 802.3bc™-2009

This amendment includes changes to IEEE Std 802.3-2008 and adds Clause 79. This amendment moves the Ethernet Organizationally Specific Type, Length, Value (TLV) information elements that were specified in IEEE Std 802.1AB to IEEE Std 802.3.

IEEE Std 802.3at™-2009

This amendment includes changes to IEEE Std 802.3-2008. This amendment augments the capabilities of IEEE Std 802.3-2008 with higher power levels and improved power management information.

IEEE Std 802.3-2008™/Cor 1–2009

This corrigendum corrects the PAUSE reaction timing delay value for the 10GBASE-T PHY type.

IEEE Std 802.3ba™-2010

This amendment includes changes to IEEE Std 802.3-2008 and adds Clause 80 through Clause 88 and Annex 83A through Annex 83C, Annex 85A and Annex 86A. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 40 Gb/s and 100 Gb/s.

IEEE Std 802.3az™-20XX

This amendment includes changes to IEEE Std 802.3-2008 and adds Clause 78. This amendment adds changes required to enable energy efficient operation of several existing Physical Layers.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Portions of this standard can be downloaded from the Internet. Materials include PICS tables, data tables, and code. URLs are listed in the text in the appropriate sections.

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Wael William Diab, *Working Group Vice-Chair*

Steven B. Carlson, *Working Group Executive Secretary*
Adam Healey, *Working Group Secretary*
Bradley Booth, *Working Group Treasurer*

Michael Bennett, *IEEE P802.3az Energy-efficient Ethernet Task Force Chair*
Sanjay Kasturia, *IEEE P802.3az Energy-efficient Ethernet Task Force Editor-in-Chief*

IEEE P802.3az Energy-efficient Ethernet Clause Editors

Hugh Barrass
Mandeep Chadha
Joseph Chou
Wael Diab
Adam Healey
David Koenen
Gavin Parnaby
Velu Pillai
Dimitry Taich
Anoop Vetteth

Ghani Abbas
John Abbott
Akira Agata
Arne Alping
Yehuda Alush
Peter Anslow
Vittal Balasubramanian
Thananya Baldwin
Jaya Bandyopadhyay
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Kathryn M. Cush
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j

List of special symbols

Note: a new symbol indicating a rightward assignment operator has been added to the table below:

For the benefit of those who have received this document by electronic means, what follows is a list of special symbols and operators. If any of these symbols or operators fail to print out correctly on your machine, the editors apologize, and hope that this table will at least help you to sort out the meaning of the resulting funny-shaped blobs and strokes.

Special symbols and operators

Printed character	Meaning	Keystrokes	Character code	Font
∗	Boolean AND	*	ALT-042	Symbol
+	Boolean OR, arithmetic addition	+	ALT-043	Symbol
^	Boolean XOR	^	ALT-094	Times New Roman
!	Boolean NOT	!	ALT-033	Symbol
×	Multiplication	Ctrl-q 4	ALT-0180	Symbol
<	Less than	<	ALT-060	Symbol
≤	Less than or equal to	Ctrl-q #	ALT-0163	Symbol
>	Greater than	>	ALT-062	Symbol
≥	Greater than or equal to	Ctrl-q 3	ALT-0179	Symbol
=	Equal to	=	ALT-061	Symbol
≠	Not equal to	Ctrl-q 9	ALT-0185	Symbol
⇐	Assignment operator	Ctrl-q \	ALT-0220	Symbol
⇒	Assignment operator			Symbol
∈	Indicates membership	Ctrl-q Shift-n	ALT-0206	Symbol
∉	Indicates nonmembership	Ctrl-q Shift-o	ALT-0207	Symbol
±	Plus or minus (a tolerance)	Ctrl-q 1	ALT-0177	Symbol
°	Degrees	Ctrl-q 0	ALT-0176	Symbol
∑	Summation	Esc ^ Shift-a	ALT-0229	Symbol
√	Square root	Ctrl-q Shift-v	ALT-0214	Symbol
—	Big dash (em dash)	Ctrl-q Shift-q	ALT-0151	Times New Roman
–	Little dash (en dash), subtraction	Ctrl-q Shift-p	ALT-0150	Times New Roman
|	Vertical bar	|	ALT-0124	Times New Roman
†	Dagger	Ctrl-q Space	ALT-0134	Times New Roman
‡	Double dagger	Ctrl-q ‘	ALT-0135	Times New Roman
α	Lower case alpha	a	ALT-097	Symbol
β	Lower case beta	b	ALT-098	Symbol
γ	Lower case gamma	g	ALT-103	Symbol
δ	Lower case delta	d	ALT-100	Symbol
ε	Lower case epsilon	e	ALT-101	Symbol
λ	Lambda	l	ALT-0108	Symbol
μ	Micro	Ctrl-q 5	ALT-0181	Times New Roman
Ω	Omega	W	ALT-087	Symbol
Π	Upper case Pi	Shift-p		Symbol

Revisions to IEEE Std 802.3-2008

EDITORIAL NOTES - Unless otherwise indicated in the editing instructions, this supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3az.

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross-references that do not point to text in this amendment may be shown in Dark Blue and have no active link.

1. Introduction

1.4 Definitions

Insert the following definition(s) in alphanumeric order:

10BASE-Te	IEEE 802.3 Physical Layer specification for an Energy Efficient version of 10BASE-T for a 10 Mb/s CSMA/CD local area network over two pairs of Category 5 or better balanced cabling. (See IEEE 802.3, Clause 14.)
Low Power Idle Mode	An optional mode intended to save power that may be enabled during periods of low link utilization in which either side of a link may disable portions of device or system functionality.

1.5 Abbreviations

Insert the following abbreviations in alphanumeric order:

EEE	Energy Efficient Ethernet
LPI	Low Power Idle

Change the clause heading as shown below:

14.Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T including type 10BASE-Te

14.1 Scope

14.1.1 Overview

Change the first paragraph of 14.1.1 as shown below and insert a NOTE as shown below after the first paragraph:

Clause 14 defines the functional, electrical, and mechanical characteristics of the type 10BASE-T MAU and one specific medium for use with that MAU. This clause also specifies the functional, electrical, and mechanical characteristics of the Energy Efficient version of 10BASE-T, the type 10BASE-Te MAU, and one specific medium for use with that MAU. The relationship of this clause to the entire ~~ISO/IEC 8802-3~~IEEE Std 802.3 LAN International Standard is shown in Figure 14–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

NOTE—Support for both 10BASE-T and 10BASE-Te signal levels in a single device is not required.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Clause 1 through Clause 7 and Clause 9 of this standard.

14.1.1.1 Medium Attachment Unit (MAU)

Insert items (i) and (j) into the list of general characteristics as shown below:

The MAU has the following general characteristics:

a) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Clause 14.
b) Supports message traffic at a data rate of 10 Mb/s.
c) Provides for operating over 0 m to at least 100 m of twisted pair without the use of a repeater.
d) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.
e) Supports network configurations using the CSMA/CD access method defined in this standard with baseband signaling.
f) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.
h) Allows for either half duplex operation, full duplex operation, or both.
i) Provides for operation with reduced peak differential voltage on the TD circuit for type 10BASE-Te. A 10BASE-Te MAU interoperates with a 10BASE-T MAU if the minimum cabling requirements of a 10BASE-Te MAU are met.
j) All references to 10BASE-T include 10BASE-Te unless otherwise stated.

14.1.1.3 Twisted-pair media

Change the first paragraph of 14.1.1.3 as shown below:

The medium for 10BASE-T is twisted-pair wire. The performance specifications of the 10BASE-T except 10BASE-Te simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter [26 AWG to 22 AWG] unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

Insert the following paragraphs in 14.1.1.3 after the first paragraph:

The medium for 10BASE-Te is twisted-pair wire. The performance specifications of the 10BASE-Te simplex link segment (either pure 10BASE-Te or mixed 10BASE-T, 10BASE-Te) is a channel meeting or exceeding the requirements of the Class D channel specified by ISO/IEC 11801:1995. These channel requirements can also be met by the Category 5 channel specified by ANSI/TIA/EIA-568-B:2001.

NOTE—ISO/IEC 11801:2002 provides a specification for media that exceeds the minimum requirements of this standard.

14.3.1 MAU-to-MDI interface characteristics

14.3.1.2 Transmitter specifications.

The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this subclause.

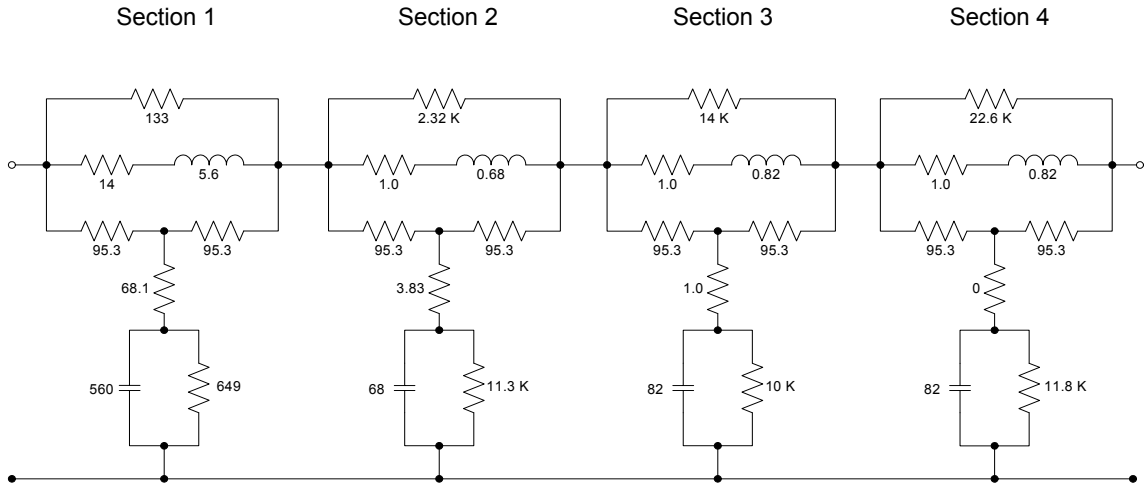
Where a load is not specified, the transmitter shall meet requirements of this subclause when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

Change the third paragraph onwards of 14.3.1.2 to read as shown below:

Some tests in this subclause require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Figure 14–7 for a type 10BASE-T MAU that is not a type 10BASE-Te MAU and according to Figure 14–7a for a type 10BASE-Te MAU with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to section 1 and the signal measured across a load connected to section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit. Also, the value of the resistor that is in series with the inductors includes the series resistance of the inductor itself. The actual value of the resistor that is used is computed by subtracting the series resistance of the inductor from the resistor value shown in the figure.

~~The~ For a type 10BASE-T MAU that is not a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.

Insert the following paragraph and Figure 14–7a showing new twisted-pair model after Figure 14.7 (which shows the existing twisted-pair model).

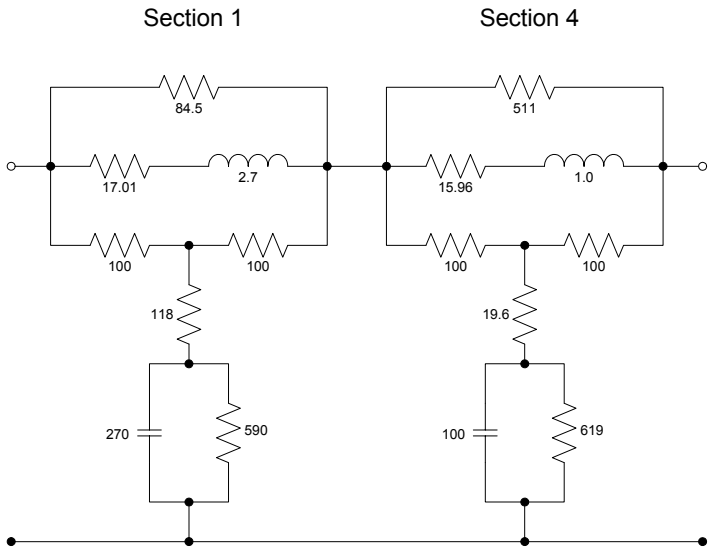


NOTE: Care must be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

Figure 14–7—Twisted-pair model for 10BASE-T

For a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 6.8 dB and 7.4 dB at 10 MHz, and between 4.75 dB and 5.25 dB at 5 MHz.



NOTE: Care must be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

Figure 14–7a—Twisted-pair model for 10BASE-Te

14.3.1.2.1 Differential output voltage

Some of the text and figures of this subclause describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

Change the second and third paragraphs of 14.3.1.2.1 (Differential output voltage) to read as shown below:

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences for a type 10BASE-T MAU that is not a type 10BASE-Te MAU. For a type 10BASE-Te MAU, the peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 1.54 V and 1.96 V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal V_o, is defined at the output of the twisted-pair model as shown in Figure 14–8. The specific twisted-pair model used in Figure 14–8 shall be the equivalent circuit shown in Figure 14–7 for 10BASE-T except 10BASE-Te and shall be the equivalent circuit shown in Figure 14–7a for 10BASE-Te. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Figure 14–9 for all data sequences. Voltage and time coordinates for inflection points on Figure 14–9 are given in Table 14–1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Figure 14–9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in B.4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

Change the fifth, sixth and seventh paragraphs of 14.3.1.2.1 (Differential output voltage) to read as shown below:

The TP_IDL shall always start with a positive waveform when a waveform conforming to Figure 14–12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14–10. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Figure 14–10 shall be met when measured across each of the test loads defined in Figure 14–11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8 for 10BASE-T except 10BASE-Te and Figure 14–7a and Figure 14–8 for 10BASE-Te.

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Figure 14–12. Once the differential output voltage has become more negative than –50 mV, it shall remain less than +50 mV. The template requirements of Figure 14–12 shall be met when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8 for 10BASE-T except 10BASE-Te and Figure 14–7a and Figure 14–8 for 10BASE-Te.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the tem-

plate requirements of Figure 14–12 when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8 for 10BASE-T except 10BASE-Te and Figure 14–7a and Figure 14–8 for 10BASE-Te.

14.4 Characteristics of the simplex link segment

Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

14.4.1 Overview

Change the first paragraph of 14.4.1 as shown below:

The medium for 10BASE-T is twisted-pair wiring. ~~Since a~~A significant number of 10BASE-T networks are ~~expected to be~~ installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

Insert paragraph as shown after the first paragraqh of 14.4.1

The medium for 10BASE-Te is twisted pair wire. The requirements of the 10BASE-Te simplex link segment (either pure 10BASE-Te or mixed 10BASE-T, 10BASE-Te) are equivalent to the requirements of the Class D channel specified by ISO/IEC 11801:1995. This requirement can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-B:2001.

14.4.2.1 Insertion loss

Change the first paragraph of 14.4.2.1 to read as shown below

The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 and 10 MHz for a 10BASE-T MAU that is not a 10BASE-Te MAU. For a 10BASE-Te MAU, the insertion loss of a simplex link segment shall be no more than 8.5 dB at all frequencies between 5.0 MHz and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE—Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

14.5.2 Crossover function

Change the last sentence of the first paragraph of 14.5.2 to read as shown below

Additionally, the MDI connector for a MAU that implements ~~the~~ a fixed crossover function shall be marked with the graphical symbol “X”. Internal and external crossover functions are shown in Figure 14–22.

14.8 MAU labeling

Change the list by modifying items (c) and (d) and inserting item (e) as shown below:

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s,
b) Power level in terms of maximum current drain (for external MAUs),
c) Any applicable safety warnings, ~~and~~
d) Duplex capabilities~~.~~, and
e) Which of the two specifications is implemented, i.e., 10BASE-T or 10BASE-Te (not both).

See also 14.5.2.

Change section 14.10 header to read as shown below:

14.10 Protocol implementation conformance statement (PICS) proforma for Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T and type 10BASE-Te[1]

14.10.3 Identification of the protocol

Change text in first row of the table as shown below:

IEEE Std 802.3-2008,Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T except type 10BASE-Te	Y [ ]	N [ ]

Insert following text in table after first row:

IEEE Std 802.3-2008,Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-Te	Y [ ]	N [ ]

14.10.4.5.12 Transmitter specification

Change TS1 to read as shown below. Change table by inserting TS2 and renumbering subsequent entries in the PICS:.

	Parameter	Subclause	Req	Imp	Value/Comment
TS1	Peak differential output voltage on TD circuit for a type 10BASE-T MAU that is not a type 10BASE-Te MAU	14.3.1.2.1	C~~M~~		Conditional on whether it is a type 10BASE-T MAU that is not a type 10BASE-Te MAU. 2.2 to 2.8 V
TS2	Peak differential output voltage on TD circuit for a type 10BASE-Te MAU	14.3.1.2.1	C		Conditional on whether it is a type 10BASE-Te MAU. 1.54 to 1.96 V

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

14.10.4.7.1 10BASE-T link segment characteristics

Change LS4 to read as shown below. Change table by inserting LS5 and renumbering subsequent entries in the PICS:

	Parameter	Subclause	Req	Imp	Value/Comment
LS4	Insertion loss, 5.0 to 10 MHz for a type 10BASE-T MAU that is not a type 10BASE-Te MAU	14.4.2.1	C		Conditional on whether it is a type 10BASE-T MAU that is not a type 10BASE-Te MAU. ≤ 11.5 dB
LS5	Insertion loss, 5.0 to 10 MHz for a type 10BASE-Te MAU	14.4.2.1	C		Conditional on whether it is a type 10BASE-Te MAU. ≤ 8.5 dB

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

Change 22.2.1 for LPI function:

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2. The mapping is changed if EEE capability is supported (see 78.3), as described in 22.6a. EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the station management entity (STA).

Editors' Notes: *To be removed prior to publication.*
Figure 22-3 is changed to correct an error in 802.3-2008/2005.

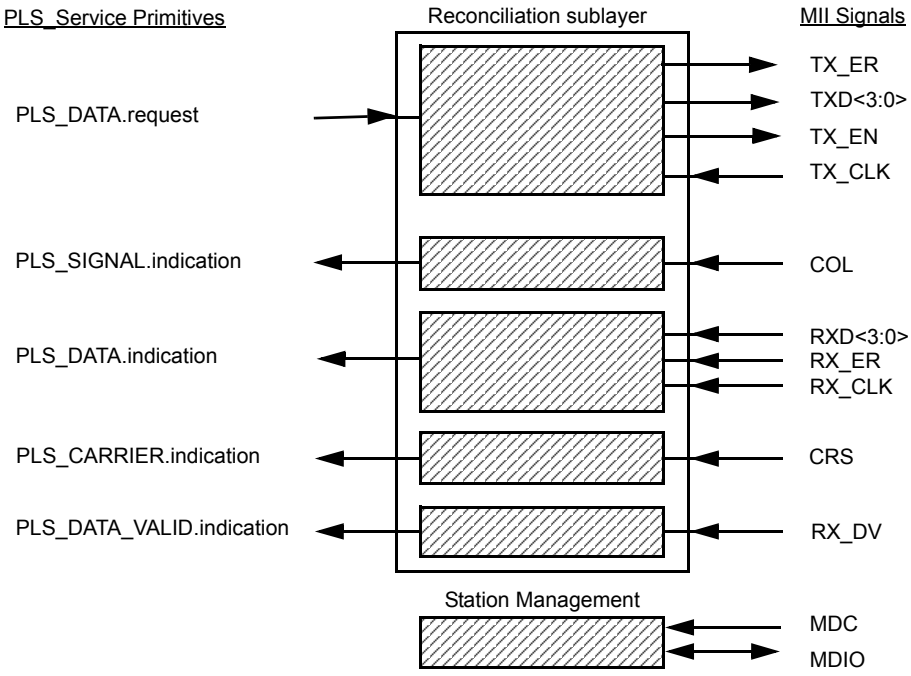


Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

Change 22.2.1.3 for PLS_CARRIER.indication:

22.2.1.3 Mapping of PLS_CARRIER.indication

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the MII signal CRS.

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signal CRS, and the LPI assert function if the EEE capability supported (see 22.6a.2).

22.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

Editors' Notes: *To be removed prior to publication.*
The following change to the base clause.is the subject of change request #1205
See revision item
http://ieee802.org/3/maint/requests/maint_1205.pdf
and revision history (look at item 1205)
http://ieee802.org/3/maint/requests/revision_history.html

~~While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.~~ Any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the receiveDataValid variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC processBitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

For EEE capability, CARRIER_STATUS is overridden according to the behavior of the LPI transmit state diagram (see Figure 22–21). The signal CRS has no effect on CARRIER_STATUS while in states LPI_ASSERTED and LPI_WAIT. A transition to the LPI_ASSERTED state in the transmit LPI state diagram shall cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and a transition to the LPI_DEASSERTED state in the transmit LPI state diagram shall cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

Change the final paragraph of 22.2.2.2 and NOTE as follows:

22.2.2.2 RX_CLK (receive clock)

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-

assertion of RX_DV at the end of a frame or while the PHY is asserting LPI, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period. For EEE capability, RX_CLK may be stopped by the PHY during LPI when the Clock stop enable bit is asserted (see 22.2.2.8a and 45.2.3.1.3a).

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5 and 22.2.2.8a.

Change 22.2.2.4 for TXD definition:

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN and TX_ER are both ~~is~~ de-asserted, TXD<3:0> shall have no effect upon the PHY.

For EEE capability, the RS shall use the combination of TX_EN de-asserted, TX_ER asserted and TXD<3:0> equal to 0001 shown in Table 22–1 as a request to enter, or remain in a low power state. Other values of TXD<3:0> with this combination of TX_EN and TX_ER shall have no effect upon the PHY.

Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
~~0~~	~~1~~	~~0000 through 1111~~	~~Reserved~~
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Insert 22.2.2.5a after 22.2.2.5 for transmit LPI transition:

22.2.2.5a Transmit direction LPI transition

When the transmit LPI state diagram is in state LPI_ASSERTED, the LPI client requests the PHY to transition to the LPI state by de-asserting TX_EN, asserting TX_ER and setting TXD<3:0> to 0001. The LPI client maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The LPI client requests the PHY to transition out of the LPI state by de-asserting TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the resolved wake up time specified for the PHY.

Figure 22–6a shows the behavior of TX_EN, TX_ER and TXD<3:0> during the transition into and out of the LPI state.

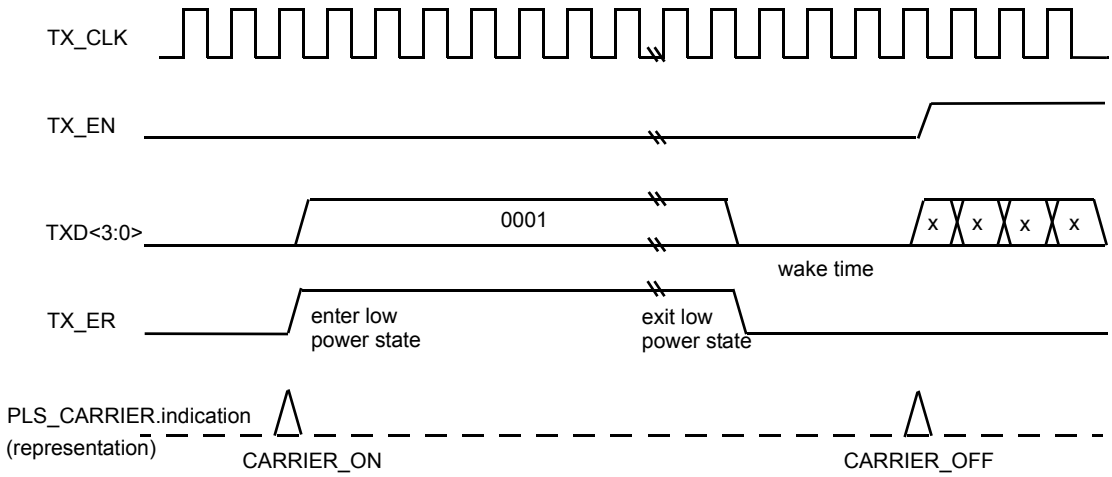


Figure 22–6a—LPI transition

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Insert the following between the second and third paragraphs of 22.2.2.7:

22.2.2.6 RXD (receive data)

For EEE capability, the PHY indicates that it is receiving LPI by asserting the RX_ER signal and driving the value 0001 onto RXD<3:0> while RX_DV is de-asserted.

Change Table 22-2, insert new row and change as follows:

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
~~0~~	~~1~~	~~0001 through 1101~~	~~Reserved~~
0	1	0001	Assert LPI
0	1	0010 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

Insert 22.2.2.8a after 22.2.2.8 for receive LPI transition:

22.2.2.8a Receive direction LPI transition

When the PHY receives signals from the link partner to indicate transition into the low power state, it indicates this to the LPI client by asserting RX_ER and setting RXD<3:0> to 0001 while keeping RX_DV de-asserted. The PHY maintains these signals in this state while it remains in the low power state. When the PHY receives signals from the link partner to indicate transition out of the low power state it indicates this to the LPI client by de-asserting RX_ER and returning to a normal inter-frame state.

While the PHY device is indicating LPI, it may halt the RX_CLK at any time more than 9 clock cycles after the start of the low power state as shown in (Figure 22–9a) if and only if the Clock stop enable bit is asserted (see 45.2.3.1.3a). The PHY may restart RX_CLK at any time while it is asserting LPI, but shall restart RX_CLK so that at least one positive transition occurs before it de-asserts LPI.

Figure 22–9a shows the behavior of RX_ER, RX_DV and RXD<3:0> during LPI transitions.

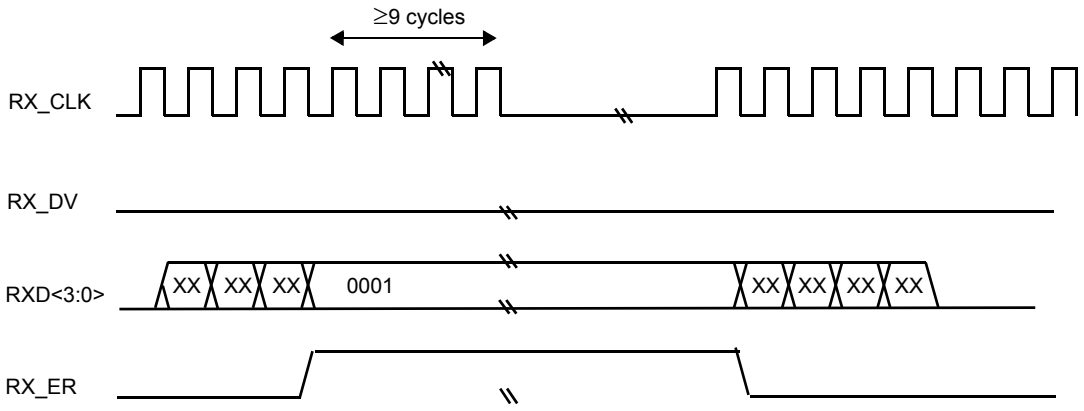


Figure 22–9a—LPI transitions (receiver)

Insert a new section, 22.6a before 22.7 for LPI assertion and detection:

22.6a LPI Assertion and Detection

Certain PHYs support Energy Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the LPI client to signal to the PHY and to the link partner that an interruption in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication. LPI signaling on the MII is specified only for 100 Mb/s operation.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the MII signals as shown in Figure 22–20a.

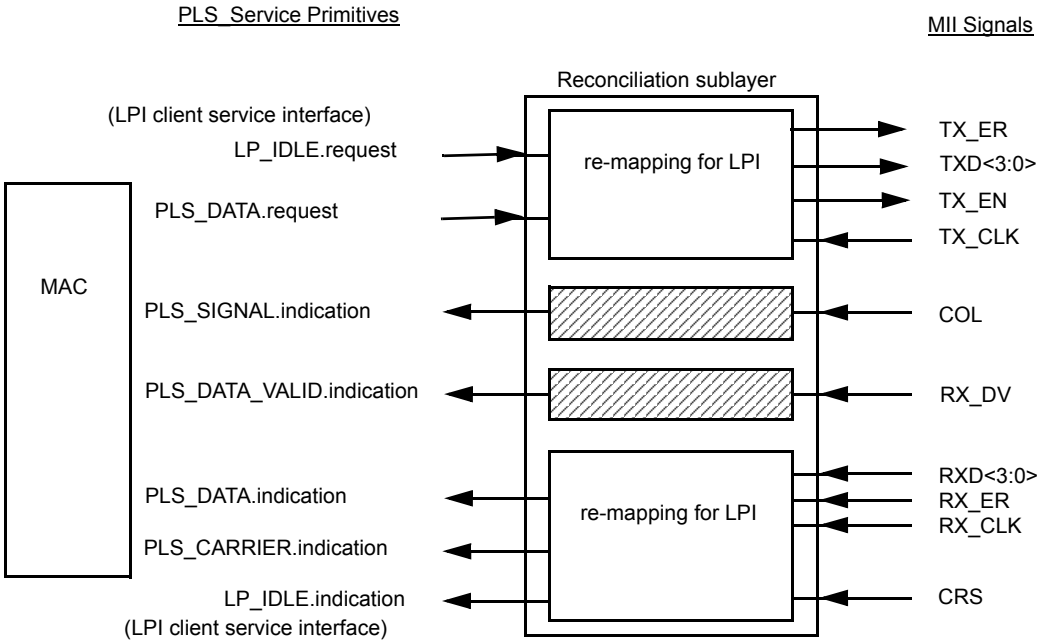


Figure 22–20a—LPI assertion and detection mechanism

The definition of TX_EN, TX_ER and TXD<3:0> is derived from the state of PLS_DATA.request (22.2.1.1), except when it is overridden by an assertion of LP_IDLE.request. Similarly, RX_ER and RXD<3:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected. CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire. The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

22.6a.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or de-assertion of LPI from the link partner.

Values:DEASSERT: The link partner is operating with normal inter-frame behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT initiates the signaling of LPI to the link partner. DE-ASSERT stops the signaling of LPI to the link

partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or if LPI_REQUEST=ASSERT within 1 second of the change of link_status to OK.

22.6a.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been de-asserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state diagram and the rules mapping CARRIER_SENSE.indication defined in 22.2.1.3. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 22–21.

22.6a.2.1 Conventions

The notation used in the state diagram follows the conventions of 21.5.

22.6a.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

power_on
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
Values:FALSE: The device is completely powered (default).
TRUE: The device has not been completely powered.

rs_reset
: Used by management to control the resetting of the RS.
Values:FALSE: Do not reset the RS (default).
TRUE: Reset the RS.

tw_timer
: A timer that counts the time since the de-assertion of LPI. The terminal count of the timer shall be the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 and 78.4. The minimum value of $T_{w\_sys\_tx}$ shall be 30 μs for 100BASE-TX. Signal tw_timer_done is asserted on reaching its terminal count.

22.6a.2.3 State Diagram

22.6a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the de-assertion of LPI. Buffering and queue management should be designed to accommodate this.

22.6a.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the MII. The receive system should be aware that data frames may arrive at the MII following the de-assertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

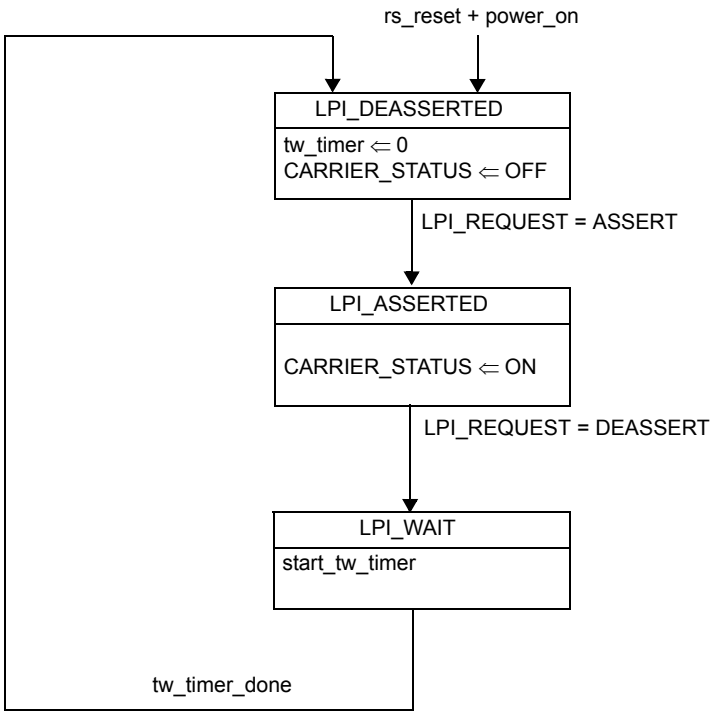


Figure 22–21—Transmit LPI State Diagram

22.7 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[1]

Insert the following row into table 22.7.2.3:

22.7.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*LPI	Implementation of LPI	22.6a	O		

Insert new subclause 22.7.3.2a after 22.7.3.2:

22.7.3.2a LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
L1	Transitions to LPI_ASSERTED and LPI_DEASSERTED reflected in CARRIER_STATUS	22.2.1.3.3	LPI:M		
L2	RX_CLK max high/low time while the PHY is asserting LPI	22.2.2.2	LPI:M		Max 2 times the nominal period
L3	Assertion of LPI as defined in Table 22–1	22.2.2.4	LPI:M		
L4	RX_CLK stoppable during LPI	22.2.2.8a	LPI:O		At least 9 cycles after LPI assertion
L5	RX_CLK restart before LPI deasserted	22.2.2.8a	LPI:O		At least 1 positive edge before LPI de-assertion
L6	Behavior matches the transmit LPI state diagram	22.6a.2	LPI:M		
L7	Terminal count for tw_timer	22.6a.2.2	LPI:M		Based on resolved $T_{w\_sys\_tx}$
L8	RS continues to indicate IDLE on PLS_DATA.indicate	22.6a.3.1	LPI:M		

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.1 Overview

24.1.1 Scope

Insert the following paragraph after the second paragraph:

The 100BASE-X may support the capability of Energy Efficient Ethernet (EEE) as described in Clause 78. When a transmitting station of a link with this capability detects low link utilization, it can request the local PHY transmitter to enter the Low Power Idle (LPI) mode and send appropriate symbols over the link. Upon receiving and decoding those symbols, the link partner's receiver can enter the LPI mode. The transmit and receive paths can enter and exit low power states independently. Energy is conserved by deactivating the corresponding functional blocks of individual path. Only 100BASE-TX supports this optional capability.

24.1.2 Objectives

Change 24.1.2 by inserting item (g) after item (f) in the lettered list, and change item (d) and (e)(1) per 802.3 maintenance requests #1206 and #1207.

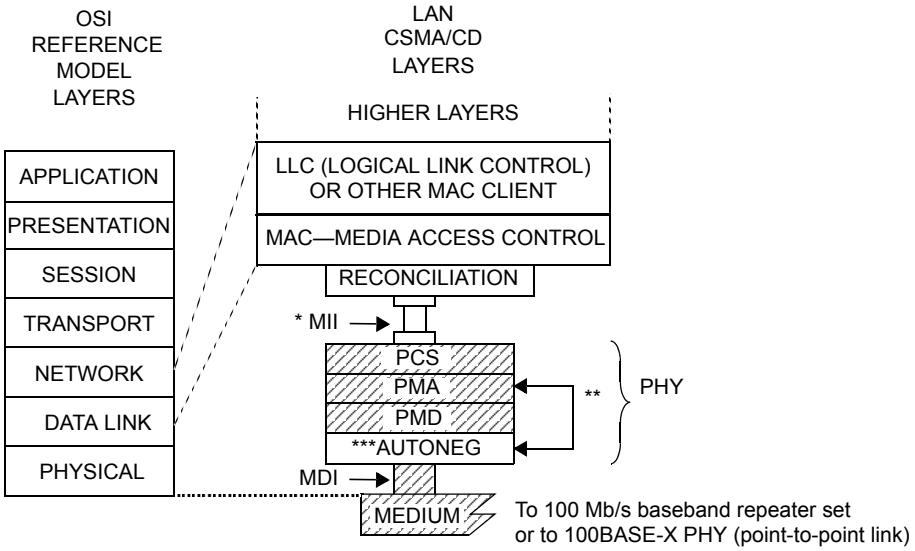
The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC in the half duplex and the full duplex modes of operation.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 UTP[5], 150 Ω STP or optical fiber, compliant with ISO/IEC 11801.
e) Allow for a nominal network extent of 200–400 m, including
   1) Unshielded[5] twisted-pair links of 100 m;
   2) Two repeater networks of approximately 200 m span;
   3) One repeater network of approximately 300 m span (using fiber); and
   4) DTE/DTE links of approximately 400 m (half duplex mode using fiber) and 2 km (full duplex mode using multimode fiber).
f) Preserve full duplex behavior of underlying PMD channels.
g) Optionally support Energy Efficient Ethernet through the function of Low Power Idle (see Clause 78), available only for 100BASE-TX.

[5]ISO/IEC 11801 makes no distinction between shielded or unshielded twisted-pair cables, referring to both as balanced cables.

24.1.3 Relationship of 100BASE-X to other standards

Replace Figure 24-1 with the new Figure 24–1 as shown below:



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is mandatory for EEE capability and optional otherwise.

Figure 24–1—Type 100BASE-X PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

24.1.4 Summary of 100BASE-X sublayers

24.1.4.1 Physical Coding Sublayer (PCS)

Change the second paragraph by inserting item (e) after item (d) in the list of services as shown below:

The 100BASE-X PCS realizes all services required by the MII, including:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B);
b) Generating Carrier Sense and Collision Detect indications;
c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA~~, and~~;
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA~~,~~and
e) Optionally, interpreting and generating MII data signals to enable or disable the LPI mode.

24.1.4.2 Physical Medium Attachment (PMA) sublayer

Change 24.1.4.2 by inserting item (e) after item (d) in the lettered list and renumber the items as shown below:

d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication; ~~and~~

e) Optionally, receiving and processing LPI control signals from the PCS; and

f) Recovery of clock from the NRZI data supplied by the PMD.

Insert 24.1.4.4 after 24.1.4.3.

24.1.4.4 Auto-Negotiation

Auto-Negotiation shall be implemented for EEE capability. See Clause 28.

24.1.6 Functional block diagram

Change 24.1.6 as shown below:

Figure 24–4 provides a functional block diagram of the 100BASE-X PHY. Signals or functions shown with dashed lines are optional.

Replace Figure 24-4 with the new Figure 24–4 as shown below:

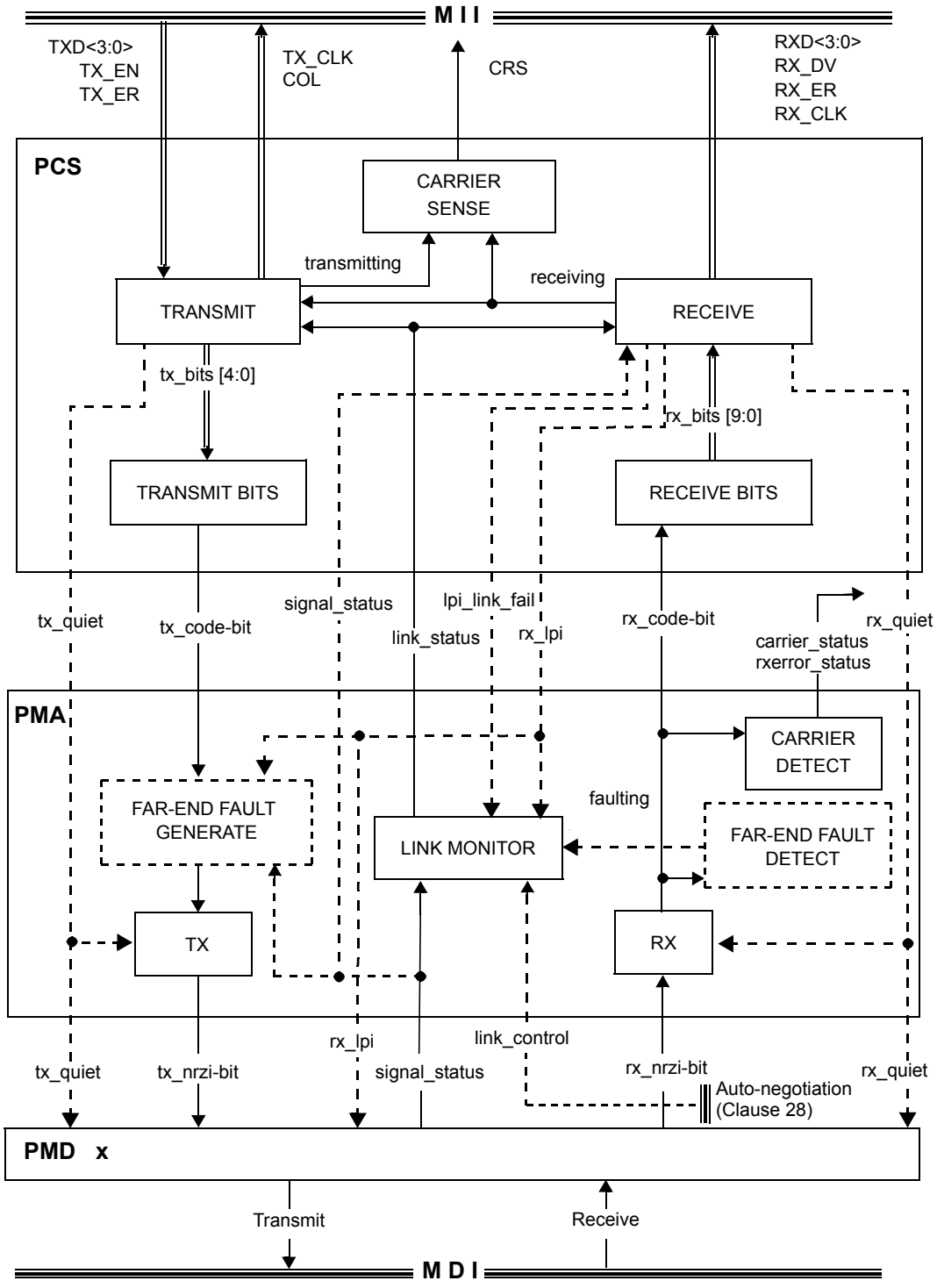


Figure 24–4—Functional block diagram

24.2 Physical Coding Sublayer (PCS)

24.2.2 Functional requirements

Change the existing 3rd and 4th paragraph of 24.2.2 by removing some space characters and inserting two new paragraphs after the 3rd and 4th paragraph respectively as shown below:

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates ~~RXD <3:0>~~RXD<3:0>, RX_DV and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

Upon receiving proper code-groups via rx_code_bits from the link partner as described in 24.2.2.1.5, the Receive process may support the LPI function by deactivating all or part of receive functional blocks of the PCS, PMA, and PMD to conserve energy during the low link utilization period, and generate commands through the MII as described in 22.2.2.7. By interacting with the Link Monitor of the PMA, a link failure detection mechanism is included to differentiate two conditions of link failure due to signal off: the loss of channel signal during the normal operation and the loss of refresh signal in the LPI mode.

The Transmit process generates continuous code-groups based upon the ~~TXD <3:0>~~TXD<3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA.request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Transmit process may support the LPI function by deactivating all or part of transmit functional blocks of the PCS, PMA, and PMD to conserve energy during the low link utilization period upon receiving the proper command from MII as described in 22.2.2.4. In this mode, the Transmit process is periodically activated to transmit refresh signal through tx_code_bits in order to allow the remote receiver to keep track of the long term variation of channel characteristics and the clock drift between link partners.

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

24.2.2.1 Code-groups

Change the last paragraph of 24.2.2.1 as shown below:

The indicated code-group mapping is identical to ISO/IEC 9314-1:1989, with ~~four~~five exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.
e) The /P/ code-group is used to indicate LPI.

24.2.2.1.1 Data code-groups

Change Table 24–1 by inserting the new code-groups SLEEP below existing code-groups IDLE as shown below.

Table 24–1—4B/5B code-groups

PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
0 0 0 0 0	P	0 0 0 1	SLEEP; LPI code only for the EEE capability. Otherwise, Invalid code; refer to Table 22–1 and Table 22–2

Insert 24.2.2.1.5a after 24.2.2.1.5.

24.2.2.1.5a SLEEP code-groups (/P/)

The SLEEP code-group (/P/) is used to delineate the boundary of an LPI sequence and to deliver a refresh signal to maintain clock synchronization and verify the link status. The SLEEP code-groups are emitted from, and interpreted by, the PCS.

24.2.3 State variables

24.2.3.1 Constants

Insert the following text at the end of the list, right before 24.2.3.2 Variables:

The following constants are required only for the optional EEE capability.

SLEEP
: The SLEEP code-group (/P/) used by the LPI state delineator, as specified in 24.2.2.1.

TX_LP_IDLE
: A binary value 0001 of transmit nibble-wide Data signals (TXD), together with the de-assertion of TX_EN and the assertion of TX_ER on the MII, used to indicate "Assert LPI", as specified in 22.2.2.

RX_LP_IDLE
: A binary value 0001 of receive nibble-wide Data signals (RXD), together with the de-assertion of RX_DV and the assertion of RX_ER on the MII, used to indicate "Assert LPI", as specified in 22.2.2.

24.2.3.2 Variables

Insert the following text at the end of the list, right before 24.2.3.3 Functions:

The following variables are required only for the optional EEE capability.

lpi_link_fail

A Boolean set by the Receive process to control the transition to a Link Down state when in the LPI mode. Used by the Link Monitor process of the PMA as communicated through the PMA_LPILINKFAIL.request primitive.

Values: TRUE; Local receiver has detected a link failure status when in the LPI mode
FALSE; Local receiver is functioning normally when in the LPI mode

rx_lpi

A Boolean set by the Receive process to indicate the LPI mode. Used by the Link Monitor process of the PMA as communicated through the PMA_RXLPI.request primitive. This parameter is used to alter the signal detection time as shown in Table 25–3. It can also be used to halt the clock RXC of MII as described in Clause 22.

Values: TRUE; Local receiver is in the LPI mode
FALSE; Local receiver is in the normal mode

rx_quiet

A Boolean set by the Receive process to indicate a Quiet state of the receiver in the LPI mode as communicated through the PMD_RXQUIET.request primitive. Also may be used to control the power saving function of various receive blocks (PCS, PMA, and PMD).

Values: TRUE; The local receiver is in the Quiet state
FALSE; The local receiver is not in the Quiet state

tx_quiet

A Boolean set by the Transmit process to indicate a Quiet state of the transmitter in the LPI mode as communicated through the PMD_TXQUIET.request primitive. Also may be used to control the power saving function of various transmit blocks (PCS, PMA, and PMD).

Values: TRUE; The local transmitter is in the Quiet state
FALSE; The local transmitter is not in the Quiet state

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

24.2.3.4 Timers

Insert the following text at the end of the list, right before 24.2.3.5 Counters:

The following timers are required only for the optional EEE capability.

lpi_link_fail_timer

In the LPI mode, the receiver in Wake state is checking if valid symbols are properly received. This timer defines the maximum time allowed for the PHY between entry into the Wake state and subsequent entry into the Quiet, Sleep, or Idle states before assuming a link failure. The timer shall have a period between 90 μs and 110 μs.

lpi_rx_ti_timer

In the LPI mode, the receiver can move to the Idle state when it receives consecutive IDLE symbols. In order to distinguish the intended IDLE symbols sent by the link partner from ones falsely decoded during the transition from the Sleep state to the Quiet state before the signal status is de-asserted, this receiver timer counts the minimum duration of received IDLE symbols. During this period of time, the receiver stays in an intermediate state. The timer shall have a period

between 0.8 μs and 0.9 μs.

lpi_rx_tq_timer

In the LPI mode, this receiver timer counts the maximum duration the PHY stays in the Quiet state before it expects a Refresh signal. If the PHY fails to receive a valid Refresh signal or Wake signal before this timer expires, the receiver shall assume a link failure. The timer shall have a period between 24 ms and 26 ms.

lpi_rx_ts_timer

In the LPI mode, this receiver timer counts the maximum duration the PHY is allowed to stay in the Sleep state before assuming a link failure. The timer shall have a period between 240 μs and 260 μs.

lpi_rx_tw_timer

In the LPI mode, the receiver in the Quiet state is woken up by the receiving signal. This receiver timer counts the expected duration for the PHY to identify if valid SLEEP symbols for the Refresh state or valid IDLES for the Wake state have been properly received. If none of the SLEEP or IDLE symbols are received when the timer expires, the wake error counter as defined in MDIO manageable device (MMD) register 3.22 (see 45.2.3.9b) shall be incremented. The timer shall have a period that does not exceed 20.5 μs.

lpi_tx_tq_timer

In the LPI mode, this transmitter timer counts the duration the PHY remains in the Quiet state before it must wake to send a refresh signal. The timer shall have a period between 20 ms and 22 ms.

lpi_tx_ts_timer

In the LPI mode, this transmitter timer counts the duration the PHY is sending continuous SLEEP symbols in the Sleep state before going into the Quiet state. The timer shall have a period between 200 μs and 220 μs.

24.2.4 State diagrams

Editor's Note: *To be removed prior to publication*

The state diagram conventions described in 24.1.7 apply to all of the state diagrams in this clause.

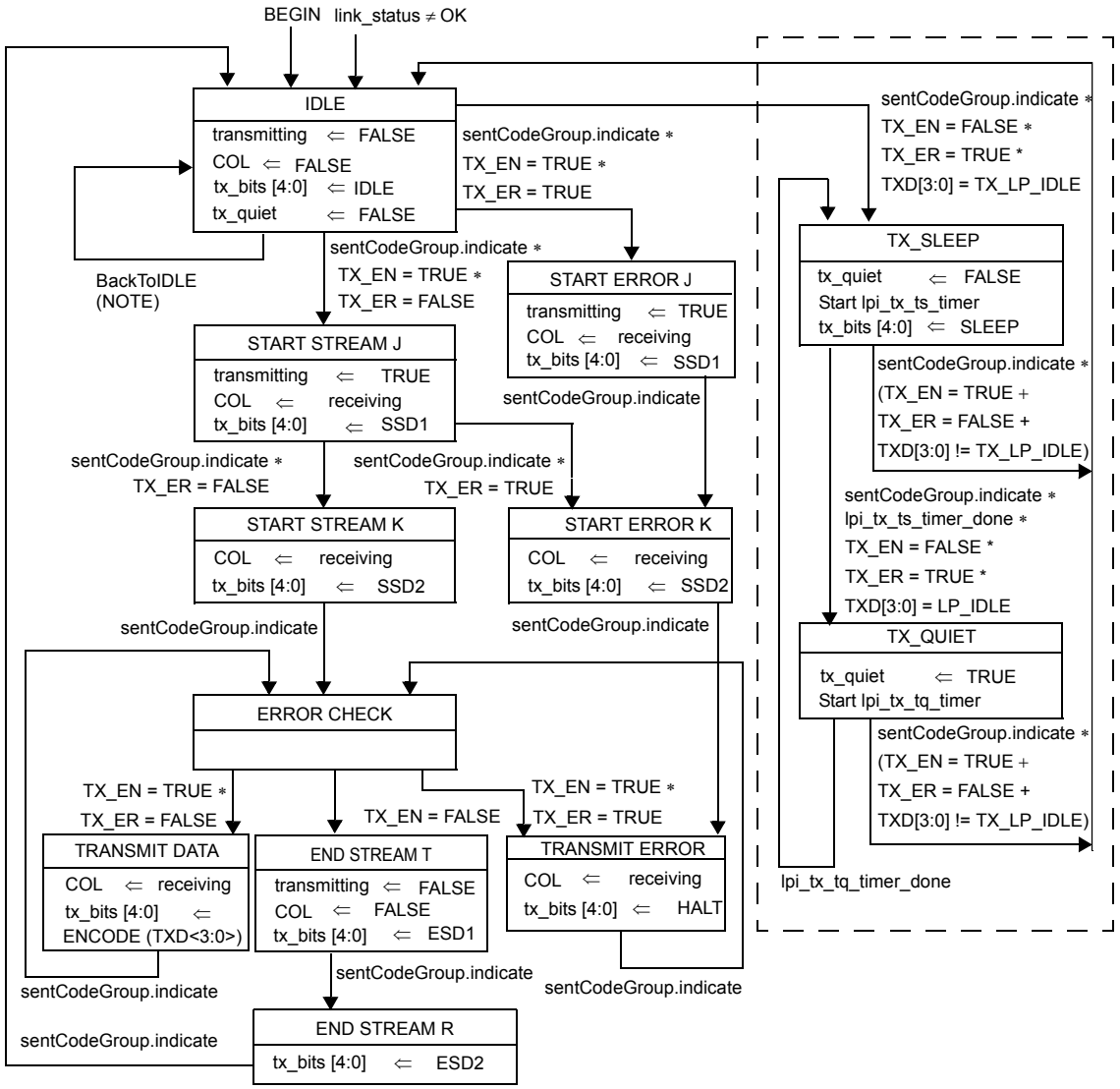
24.2.4.2 Transmit

Change the first paragraph in 24.2.4.2 as shown below:

The Transmit process sends code-groups to the PMA via tx_bits and the Transmit Bits process. When initially invoked, and between streams (delimited by TX_EN on the MII), except in the LPI mode for the optional EEE capability, the Transmit process sources continuous Idle code-groups (/I/) to the PMA. Upon the assertion of TX_EN by the MII, the Transmit process passes an SSD (/J/K/) to the PMA, ignoring the ~~TXD <3:0>~~ TXD<3:0> nibbles during these two code-group times. Following the SSD, each ~~TXD <3:0>~~ TXD<3:0> nibble is encoded into a five-bit code-group until TX_EN is de-asserted. If, while TX_EN is asserted, the TX_ER signal is asserted, the Transmit process passes Transmit Error code-groups (/H/) to the PMA. Following the de-assertion of TX_EN, an ESD (/T/R/) is generated, after which the transmission of Idle code-groups is resumed by the IDLE state.

If EEE Capability is supported, upon the assertion of LPI on the MII (A binary value 0001 of TXD, together with the de-assertion of TX_EN and the assertion of TX_ER, see 22.2.2), the Transmit process enters the LPI mode and starts to source SLEEP (/P/) code-groups to the PMA. In the LPI mode, the Transmit process is controlled by timers to switch between the TX_SLEEP and TX_QUIET states. The Transmit process returns to the IDLE state whenever the MII de-asserts LPI.

Replace the Transmit state diagram (Figure 24–8) with the new Figure 24–8:



NOTE ─ BackToIDLE represents the following branch condition:
If the EEE capability is supported,
sentCodeGroup.indicate * TX_EN = FALSE * (TX_E R= FALSE + (TX_ER = TRUE * TXD[3:0] ≠ TX_LP_IDLE))
Otherwise,
sentCodeGroup.indicate * TX_EN = FALSE

NOTE ─ States and state transitions shown within the dashed box are only required for the EEE capability

Figure 24–8—Transmit state diagram

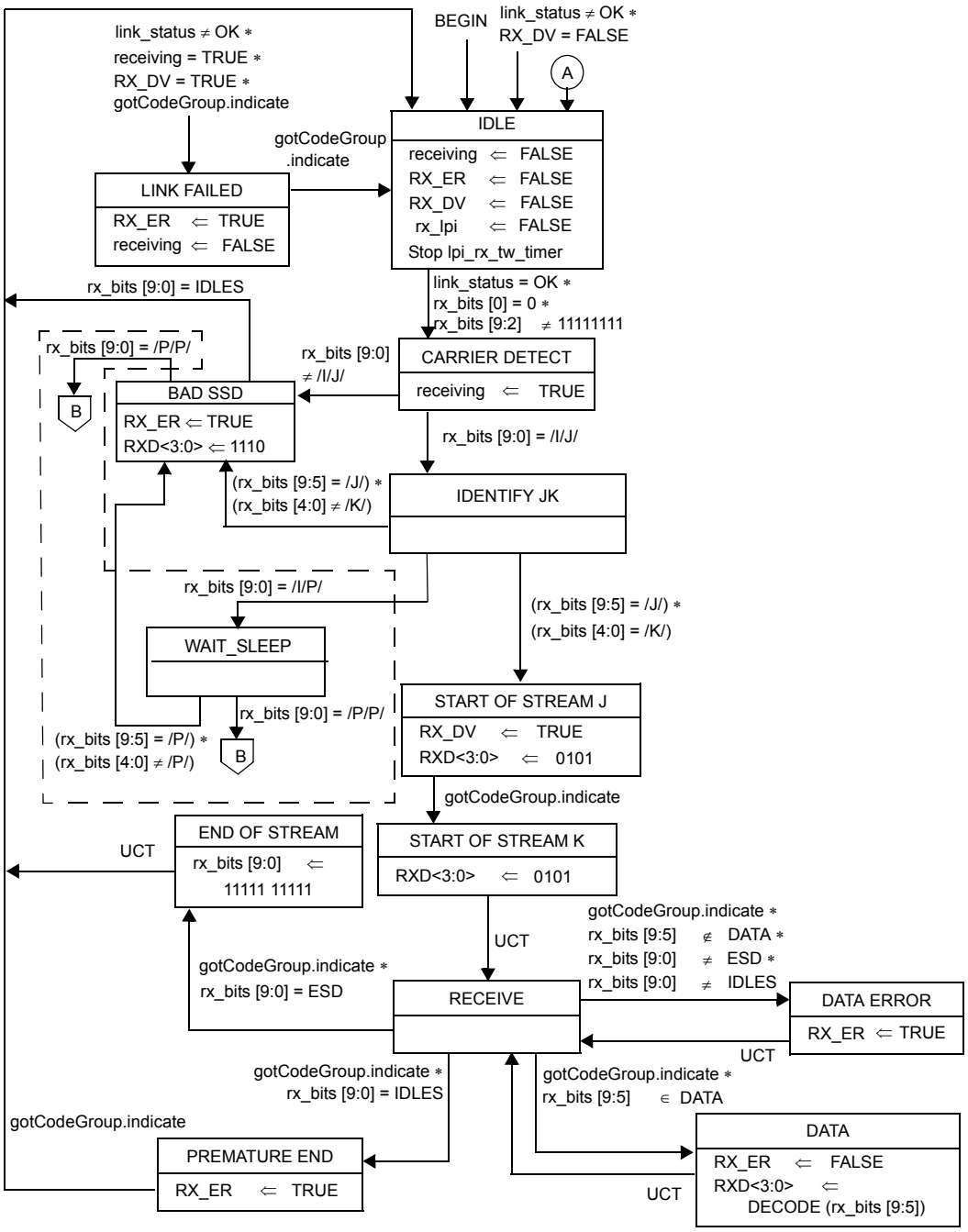
24.2.4.4 Receive

Change the first paragraph in 24.2.4.4 as shown below:

The Receive process state diagram can be viewed as comprising two sections: prealigned and aligned. In the prealigned states, IDLE, CARRIER DETECT, and ~~CONFIRM K~~ IDENTIFY JK, except for the detection of SLEEP code-groups when supporting the optional EEE capability, the Receive process is waiting for an indication of channel activity followed by ~~a~~ an SSD. After successful alignment, the incoming code-groups are decoded while waiting for stream termination.

If EEE Capability is supported, when the Receive process successfully aligns and decodes two consecutive SLEEP (/P/) code-groups, it enters the LPI mode and stays in LPI states until either the IDLE code-groups are received, where it leads the Receive process to the IDLE state, or a link failure condition in the LPI mode occurs, where it causes the Receive process to enter the RX_LPI_LINK_FAIL state and eventually move to the IDLE state.

Replace the Receive state diagram (Figure 24–11) with new figures Figure 24–11a and Figure 24–11b:



NOTE ─ States and state transitions shown within the dashed box are only required for the EEE capability

Figure 24–11a—Receive state diagram, part a

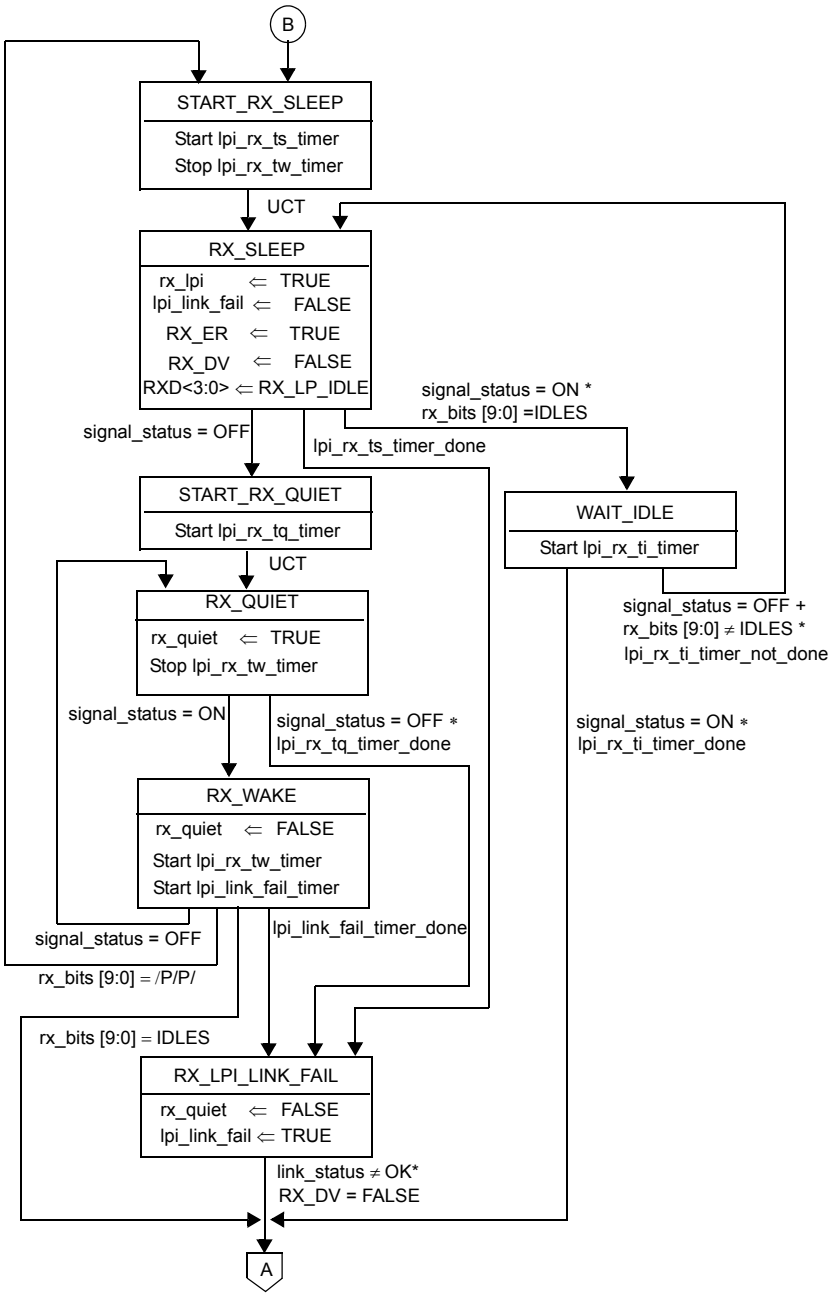


Figure 24–11b—Receive state diagram, part b (only required for the EEE capability)

24.3 Physical Medium Attachment (PMA) sublayer

24.3.1 Service Interface

Insert new primitives in 24.3.1 after the third paragraph before 24.3.1.1 as shown below:

PMA_LPILINKFAIL.request
PMA_RXLPI.request

Insert the following new primitive definitions following existing primitives after clause 24.3.1.7.3 as shown below:

24.3.1.8 PMA_LPILINKFAIL.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to control one of the link failure conditions of the Link Monitor in the PMA (see 24.2.4.4 and Figure 24–11b).

24.3.1.8.1 Semantics of the service primitive

PMA_LPILINKFAIL.request (lpi_link_fail)

The lpi_link_fail parameter takes on one of two values: TRUE or FALSE, indicating whether a link failure condition has been set (TRUE) or not (FALSE). The value of TRUE, when in the LPI mode, sets the link_status of the Link Monitor to FAIL (see 24.3.4.4 and Figure 24–15).

24.3.1.8.2 When generated

The PCS generates this primitive to indicate a link failure condition caused by the loss of Refresh signal when in the LPI mode.

24.3.1.8.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.9 PMA_RXLPI.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to indicate that the receiver is in the LPI mode (see 24.2.4.4 and Figure 24–11b).

24.3.1.9.1 Semantics of the service primitive

PMA_RXLPI.request (rx_lpi)

The rx_lpi parameter takes on one of two values: TRUE or FALSE, indicating whether the receiver is in the LPI mode (TRUE) or not (FALSE).

24.3.1.9.2 When generated

The PCS generates this primitive to indicate the LPI mode.

24.3.1.9.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as described in 24.3.4.4. Other use of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.2 Functional requirements

Insert item (e) after item (d) in the lettered list of 24.3.2 as shown below:

e) EEE capability, which disables the Far-End Fault function and modifies the link down condition with the PMA_RXLPI.request primitive.

24.3.2.1 Far-End fault

Change the sixth paragraph of 24.3.2.1 as shown below:

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF during the normal operation) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status. The Far-End Fault shall not be generated when in the LPI mode.

Insert 24.3.2.3 after 24.3.2.2 as shown below:

24.3.2.3 EEE capability

EEE capability, when communicated by the PMA_RXLPI.request primitive, affects the PMA in two ways. It disables the operation of the Far-End Fault processes to ignore the frequent on and off activity of signal_status. It receives link failure detection as communicated by the PMA_LPILINKFAIL.request primitive and changes the Link Monitor process to allow an exit from the LPI mode to a link down state. The EEE capability of the PMA is required only if the PCS supports EEE. If LPI is implemented, the operation of the PMA shall comply with the requirements in this subclause.

24.3.3 State variables

24.3.3.2 Variables

Insert the following text at the end of the list, right before 24.3.3.3 Functions:

The following variables are required only for the optional EEE capability.

lpi_link_fail

The lpi_link_fail parameter is communicated by the PMA_LPILINKFAIL.request primitive. In the LPI mode, this variable is generated by the Receive process of the PCS to control the transition to a Link Down state. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE; Local receiver has detected a link failure status when in an LPI state
FALSE; Local receiver is functioning normally when in an LPI state

rx_lpi

The rx_lpi parameter is communicated by the PMA_RXLPI.request primitive. This variable is generated by the Receive process of the PCS to indicate the LPI mode. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE; Local receiver is in the LPI mode
FALSE; Local receiver is in the normal operation mode

24.3.4 Process specifications and state diagrams

Editor's Note: *To be removed prior to publication*

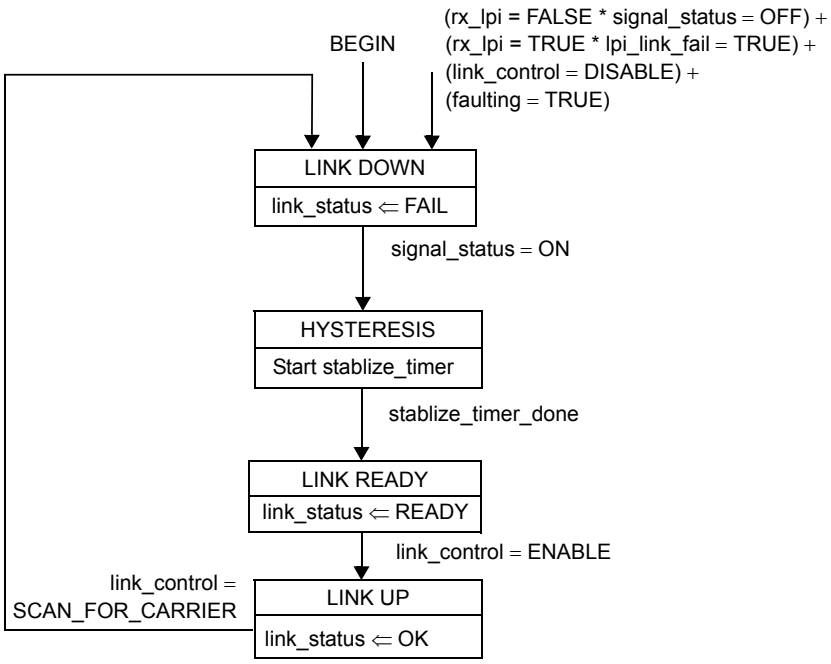
The state diagram conventions described in 24.1.7 apply to all of the state diagrams in this clause.

24.3.4.4 Link Monitor

Change the second paragraph of 24.3.4.4 as shown below:

The Link Monitor process monitors signal_status, setting link_status to FAIL whenever signal_status is OFF during the normal operation or when Auto-Negotiation sets link_control to DISABLE. If the EEE capability is supported, when the receiver is in the LPI mode, the assertion of lpi_link_fail shall set the link_status to FAIL and eventually brings the receiver out of the LPI mode. The link is deemed to be reliably operating when signal_status has been continuously ON for a period of time. This period is implementation dependent but not less than 330 µs or greater than 1000 µs. If so qualified, Link Monitor sets link_status to READY in order to synchronize with Auto-Negotiation, when implemented. Auto-Negotiation permits full operation by setting link_control to ENABLE. When Auto-Negotiation is not implemented, Link Monitor operates with link_control always set to ENABLE.

Replace the Link Monitor diagram (Figure 24–15) with the new Figure 24–15 as shown below.



NOTE – The variables link_control and link_status are designated as link_control_[TX] and link_status_[TX], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

NOTE – The variables rx_lpi and lpi_link_fail are only required for the EEE capability and should be treated as if the value of these two variables is FALSE otherwise.

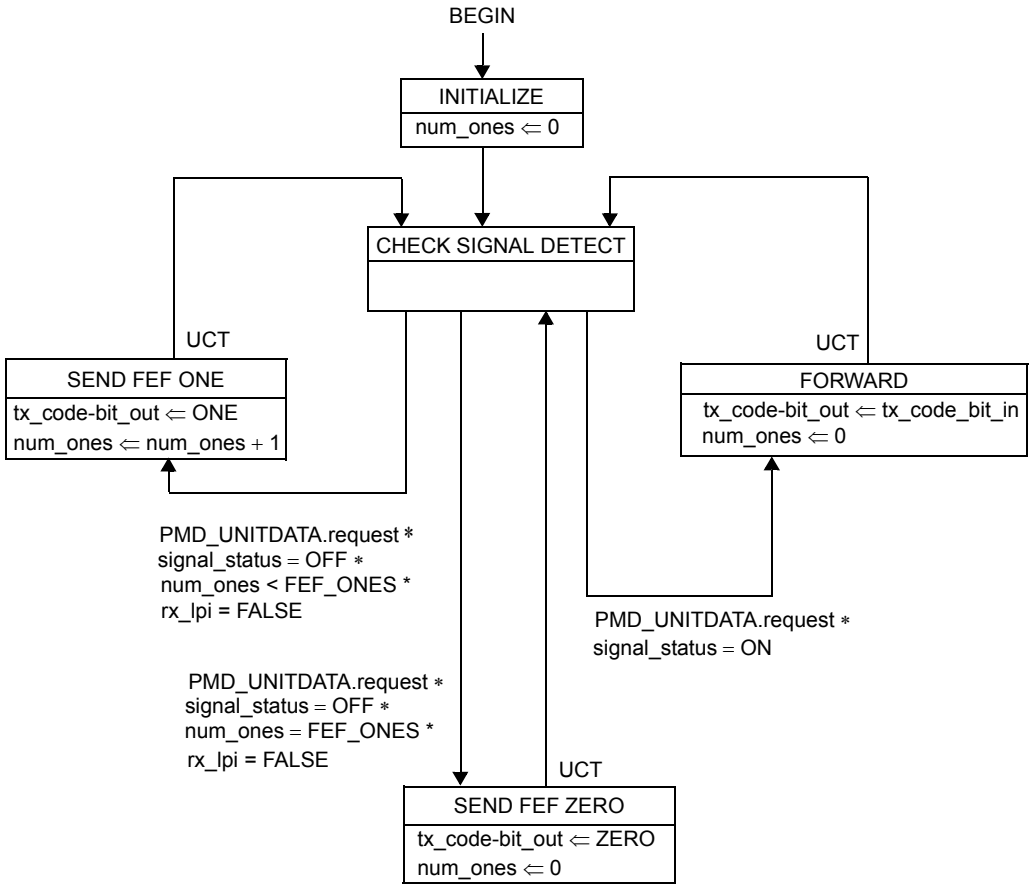
Figure 24–15—Link Monitor State Diagram

24.3.4.5 Far-End Fault Generation

Change the first paragraph of 24.3.4.5 Far-End Fault Generation as shown below:

Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON. When signal_status=OFF and not in the LPI mode, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted.

Replace the Far-End Fault diagram (Figure 24–16) with the new Figure 24–16 as shown below.



NOTE– The variable rx_lpi is only required for the EEE capability and should be treated as if the value of this variable is FALSE otherwise.

Figure 24–16—Far-End Fault Generation state diagram

24.4 Physical Medium Dependent (PMD) sublayer

24.4.1 PMD Service Interface

Change the first two paragraph of subclause 24.4.1 as shown by inserting a new exception item, and change the text containing the number of exceptions:

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3:1990 and ANSI X3.263-1995, with ~~two~~ three exceptions:

a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3:1990 and ANSI X3.263-1995.
b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.
c) 100BASE-X may support LPI for the EEE capability.

Insert the following text and primitives at the end of 24.4.1 right before 24.4.1.1 as shown below:

The following primitives are defined only for the optional EEE capability.

PMD_RXQUIET.request
PMD_TXQUIET.request

Insert the following new primitive definitions after 24.4.1.3.3 as shown below:

24.4.1.4 PMD_RXQUIET.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to indicate that the receiver is in the LPI mode and the line is in the Quiet state (see 24.2.4.4 and Figure 24–11b).

24.4.1.4.1 Semantics of the service primitive

PMD_RXQUIET.request(rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE, indicating whether the receiver is in the Quiet state (TRUE) or not (FALSE).

24.4.1.4.2 When generated

The PCS generates this primitive to indicate a Quiet state of the transmitter in the LPI mode.

24.4.1.4.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.4a.2. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.5 PMD_TXQUIET.request

This primitive is generated by the Transmit Process of the PCS only if EEE is supported to indicate that the transmitter is in the LPI mode and the line is in the Quiet state (see 24.2.4.2 and Figure 24–8).

24.4.1.5.1 Semantics of the service primitive

PMD_TXQUIETrequest(tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE, indicating whether the transmitter is in the Quiet state (TRUE) or not (FALSE).

24.4.1.5.2 When generated

The PCS generates this primitive to indicate a Quiet state of the transmitter in the LPI mode.

24.4.1.5.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.4a.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.8 Protocol implementation conformance statement (PICS) proforma for Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X[6]

24.8.2 Identification

24.8.2.3 Major capabilities/options

Insert the following rows after the item PMA in the table of 24.8.2.3:

Item	Feature	Subclause	Status	Support	Value/Comment
*LPC	PCS implementation of LPI	24.2	PCS:O		
*LPM	PMA implementation of LPI	24.3	LPC:M		

Replace the item *FEF in the table of 24.8.2.3 with the new item *FEF as shown below:

Item	Feature	Subclause	Status	Support	Value/Comment
*FEF	Implements Far-End Fault	24.3.2.1	NWC:X LPM:X		

Replace the item NWY in the table of 24.8.2.3 with the new item NWY as shown below:

Item	Feature	Subclause	Status	Support	Value/Comment
NWY	Supports Auto-Negotiation (Clause 28)	24.1.4.4	NWC:O LPC:M		See Clause 28

24.8.3 PICS proforma tables for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

Insert 24.8.3.5:

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

24.8.3.5 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
LF1	lpi_rx_ti_timer	24.2.3.4	LPC:M		The timer has a period between 0.8-0.9 μs.
LF2	lpi_rx_tq_timer	24.2.3.4	LPC:M		The timer has a period between 24-26 ms.
LF3	lpi_rx_ts_timer	24.2.3.4	LPC:M		The timer has a period between 240-260 μs.
LF4	lpi_rx_tw_timer	24.2.3.4	LPC:M		The timer has a period that does not exceed 20.5 μs.
LF5	LPI wake error counter	24.2.3.4	LPC:M		Increment the wake error counter for each transition of lpi_rx_tw_timer_done from false to true.
LF6	lpi_tx_tq_timer	24.2.3.4	LPC:M		The timer has a period between 20-22 ms.
LF7	link failure caused by lpi_rx_tq_timer	24.2.3.4	LPC:M		The receiver assumes a link failure if the PHY fails to receive a valid Refresh or Wake signal before the lpi_rx_tq_timer expires.
LF8	lpi_tx_ts_timer	24.2.3.4	LPC:M		The timer has a period between 200-220 μs.
LF9	lpi_link_fail_timer	24.2.3.4	LPC:M		The timer has a period between 90-110 μs.
LF11	lpi_link_fail	24.3.3.2	LPM:M		The PHY operates as if the value of this variable is FALSE in the absence of the optional EEE capability.
LF12	rx_lpi	24.3.3.2	LPM:M		The PHY operates as if the value of this variable is FALSE in the absence of the optional EEE capability.
LF13	link_status affected by lpi_link_fail	24.3.4.4	LPM:M		The assertion of lpi_link_fail sets the link_status to FAIL if the EEE is supported and the receiver is in the LPI mode,

25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.1 Overview

Insert 25.1.1 after 25.1 as shown below:

25.1.1 State diagram conventions

The body of this standard is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.

25.3 General exceptions

Change item (d) per 802.3 maintenance request #1210.

Insert item (e) following item (d) and change the original item (e) to item (f) as shown below:

d) The cable plant specifications for ~~untwisted shielded~~ unshielded twisted pair (UTP) of TP-PMD 11.1 are replaced by those specified in 25.4.7.

e) 100BASE-TX optionally supports Energy Efficient Ethernet (EEE), as described in Clause 78, with its Low Power Idle (LPI). Two new service primitives PMD_RXQUIET.request(rx_quiet) (see 24.4.1.4) and PMD_TXQUIET.request(tx_quiet) (see 24.4.1.5) are generated by the PCS to pass the energy saving requests.

f) There are minor terminology differences between this standard and TP-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 25–1

25.4 Specific requirements and exceptions

25.4.6 Change to 9.1.9, "Jitter"

Insert new paragraph shown below in 25.4.6 as the last paragraph:

In the LPI mode, jitter shall be measured using scrambled SLEEP code groups transmitted during the TX_SLEEP state (see PCS Transmit state diagram, Figure 24–8). Total transmit jitter with respect to a continuous unjittered reference shall not exceed 1.4 ns peak-to-peak with the exception that the jitter contributions from the clock transitions occurring during the TX_QUIET state and the first 5 μs of the TX_SLEEP state or the first 5 μs of the IDLE state following a TX_QUIET state are ignored. The jitter measurement time period shall be not less than 100 ms and not greater than 1 second.

Insert 25.4a after 25.4 as shown below:

25.4a EEE capability

Editor's Note: *To be removed prior to publication*

The state diagram conventions described in 25.1.1 apply to all of the state diagrams in this clause.

TP-PMD does not have an option to support EEE. In order to add this capability to existing TP-PMD specification, the TP-PMD 7.1.2, 7.2.2, 10.1.2, 10.1.3, and Table 4 are modified to incorporate the LPI function. This subclause only applies to the optional EEE capability. If LPI is implemented, the operation of the PMD shall comply with the requirements in this subclause.

25.4a.1 Change to TP-PMD 7.1.2 "Encoder"

The Encoder receives the scrambled NRZ data stream from the scrambler (see TP-PMD 7.1.1) and encodes the stream into MLT3 code for presentation to the driver (see TP-PMD 7.1.3). MLT3 coding is similar to NRZI coding, but three instead of two levels are transmitted. The Encoder can be deactivated when in the LPI mode. The PMD Encoder function of the 100BASE-TX with EEE capability is identical to that of the TP-PMD except that the output of the Encoder is set to a value ZERO_VOLTAGE when the transmitter is in the Quiet state of the LPI mode (TX_QUIET, see PCS Transmit state diagram, Figure 24–8).

The PMD in the LPI mode shall implement the Encoder state diagram as depicted in Figure 25–1.

25.4a.1.1 State variables

25.4a.1.1.1 Variables

encoder_input
: Indicates the value of each scrambled NRZ bit to be encoded.

  Values: ZERO; the NRZ bit from the scrambler has a logical value 0
  ONE; the NRZ bit from the scrambler has a logical value 1

encoder_output
: Indicates the value from the encoder for each MLT-3 encoded bit.

  Values: POSITIVE_VOLTAGE; the output indicates a positive value of voltage to TP-PMD driver
  ZERO_VOLTAGE; the output indicates a zero value of voltage to TP-PMD driver
  NEGATIVE_VOLTAGE; the output indicates a negative value of voltage to TP-PMD driver

link_status
: The link_status parameter as communicated by the PMA_LINK.indicate primitive.

  Values: FAIL; the receive channel is not intact
  READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
  OK; the receive channel is intact and enabled for reception

tx_quiet
: The tx_quiet parameter as communicated by the PMD_TXQUIET.request (tx_quiet) primitive. This variable is generated by the Transmit process of the PCS to control the power saving function of the local transmitter. It sets the Encoder state diagram to an initial state of ZERO_V.

  Values: TRUE; The local transmitter is in the Quiet state
  FALSE; The local transmitter is not in the Quiet state

le_flag

A Boolean set by the Encoder process to indicate whether the last non-zero value of encoder_output was POSITIVE_VOLTAGE. The flag le_flag is set upon entry to the PLUS_V state and is cleared upon entry to the MINUS_V state.

Values: ONE; The encoder is in the PLUS_V state
ZERO; The encoder is in the MINUS_V state

25.4a.1.1.2 Messages

gotNRZbit.indicate

A signal sent to the Encoder process by the scrambler after a scrambled NRZ text bit has been generated using recursive linear function by the scrambler from plaintext bit stream and is ready to transmit.

25.4a.1.2 State Diagram

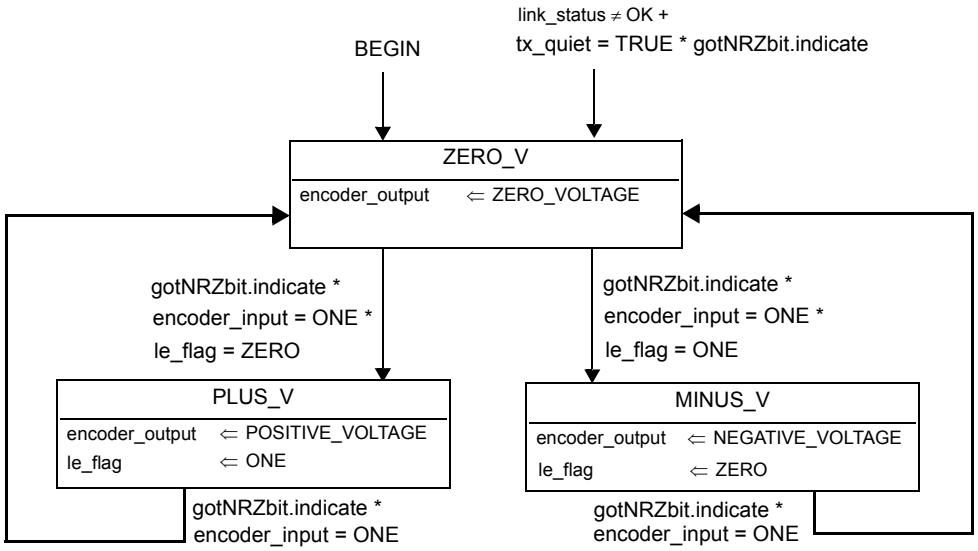


Figure 25–1—Encoder state diagram

25.4a.2 Change to TP-PMD 7.2.2 “Decoder”

The Decoder receives the MLT3 encoded bit stream from the receiver (see TP-PMD 7.2.1), and decodes it into a NRZ encoded bit stream for presentation to the descrambler (see TP-PMD 7.2.3). The Decoder can be deactivated when in the LPI mode. The PMD Decoder function of the 100BASE-TX with EEE capability is identical to that of the TP-PMD except that the output of the Decoder is set to a value ZERO when the receiver is in the Quiet state of the LPI mode (RX_QUIET, see PCS Receive state diagram, Figure 24–11b).

The PMD in the LPI mode shall implement the Decoder state diagram as depicted in Figure 25–2.

25.4a.2.1 State variables

25.4a.2.1.1 Variables

decoder_input
: Indicates the value of the MLT-3 encoded bit from the receiver.

  Values: ZERO; the MLT3 bit from the receiver has a logical value 0
  NONZERO; the MLT3 bit from the receiver has a non-zero logical value

decoder_output
: Indicates the value of the NRZ encoded bit.

  Values: ZERO; the output indicates a logical value of 0 to the descrambler
  ONE; the output indicates a logical value of 1 to the descrambler

link_status
: The link_status parameter as communicated by the PMA_LINK.indicate primitive.

  Values: FAIL; the receive channel is not intact
  READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
  OK; the receive channel is intact and enabled for reception

rx_quiet
: The rx_quiet parameter as communicated by the PMD_RXQUIET.request (rx_quiet) primitive. This variable is generated by the Receive process of the PCS to control the power saving function of local receiver. It sets the Decoder state diagram to an initial state of ZERO_VALUE.

  Values: TRUE; The local receiver is in the Quiet state
  FALSE; The local receiver is not in the Quiet state

prev_data
: Indicates whether the last value of decoder_input was ZERO or NONZERO.

  Values: ZERO; the last value of MLT3 bit of decoder_input has a logical value 0
  NONZERO; the last value of MLT3 bit of decoder_input has a non-zero logical value

25.4a.2.1.2 Messages

sentNRZbit.indicate
: A signal sent to the Decoder process by the descrambler after an NRZ bit from ciphertext bit stream has been processed using recursive linear function and is ready to process the next bit from Decoder.

25.4a.2.2 State Diagram

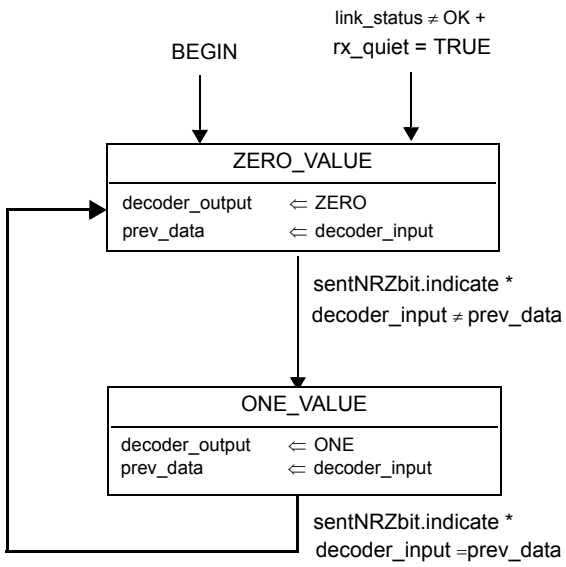


Figure 25–2—Decoder state diagram

25.4a.3 Changes to 10.1.1.1 "Signal_Detect assertion threshold"

The TP-PMD 10.1.1.1 is applicable to the normal operation. In the LPI mode, when rx_lpi as communicated by the PMA_RXLPI.request primitive is asserted, Signal_Detect shall be asserted per 25.4a.5 for any valid peak to peak signal, VSDA, of greater than 400 mV.

25.4a.4 Changes to 10.1.1.2 "Signal_Detect de-assertion threshold"

The TP-PMD 10.1.1.2 is applicable to the normal operation. In the LPI mode, when rx_lpi is de-asserted, Signal_Detect shall be de-asserted per 25.4a.6 for any valid peak to peak signal, VSDD, of smaller than 200 mV.

25.4a.5 Change to 10.1.2 "Signal_Detect timing requirements on assertion"

The TP-PMD 10.1.2 is applicable to the normal operation. In the LPI mode, when rx_lpi is asserted, Signal_Detect output shall be asserted within 5 µs under the same quality requirement of received signal as in normal operation. The new definition of conditional parameter AS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.4a.6 Change to 10.1.3 "Signal_Detect timing requirements on de-assertion"

The TP-PMD 10.1.3 is applicable to the normal operation. In the LPI mode, when rx_lpi is asserted, Signal_Detect output shall be de-asserted within 5 µs under the same quality requirement of received signal as in normal operation. The new definition of conditional parameter ANS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.4a.7 Changes to TP-PMD 10.2 "Transmitter"

For the optional EEE capability, when tx_quiet (as communicated by the PMD_TXQUIET.request primitive) is set to FALSE, the transmitter output shall deliver a signal that exceeds Signal_Detect assertion threshold within 2 μs. The scrambler shall continue to operate for the first 5 μs following tx_quiet = TRUE. Transmit functions may be deactivated after this period. The transmitter shall deliver a fully compliant signal when tx_quiet is set to FALSE less than 5 μs after being set to TRUE. If tx_quiet is set to FALSE more than 5 μs after being set to TRUE, then the transmitter shall deliver a fully compliant signal within 5 μs (see 25.4.6).

25.4a.8 Replace TP-PMD Table 4 "Signal_Detect summary" with Table 25-3

The requirement of signal detection time and threshold are different between the normal operation mode and the LPI mode. In order to share one Signal_Detect, the timing and threshold characteristics may be qualified by LPI signal rx_lpi as communicated by the PMA_RXLPI.request primitive.

Table 25–3—Signal_Detect summary

Characteristic	Minimum	Maximum	Units
Assert time Normal operation mode		1000	μs
De-assert time Normal operation mode		350	μs
Assert time LPI mode		5	μs
De-assert time LPI mode		5	μs
Assert threshold VSDA 100 ohm balanced cable Normal operation mode		1000	mV peak to peak
De-assert threshold VSDD 100 ohm balanced cable Normal operation mode	200		mV peak to peak
Assert threshold VSDA 150 ohm balanced shielded cable Normal operation mode		1225	mV peak to peak
De-assert threshold VSDD 150 ohm balanced shielded cable Normal operation mode	245		mV peak to peak
Assert threshold VSDA LPI mode		400	mV peak to peak
De-assert threshold VSDD LPI mode	200		mV peak to peak

25.5 Protocol implementation conformance statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[1]

25.5.3 Major capabilities/options

Insert the following row at the end of the table of Clause 25.5.3:

Item	Feature	Subclause	Status	Support	Value/Comment
*LPI	Implementation of LPI	25.4a	O		

Insert a new subclause 25.5.4.4 LPI Functions with the following table after 25.5.4.3:

25.5.4 PICS proforma tables for the Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.5.4.4 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
LP1	Jitter measurement in the LPI mode	25.4.6	LPI:M	Yes [ ]	1.4 ns peak to peak
LP2	Code-groups used to measure jitter in the LPI mode	25.4.6	LPI:M	Yes [ ]	Scrambled SLEEP code-groups
LP3	Jitter measurement time interval in the LPI mode	25.4.6	LPI:M	Yes [ ]	No less than 100 ms and no greater than 1 second
LP4	Encoder function in the LPI mode	25.4a.1	LPI:M	Yes [ ]	Comply with the state diagram shown in Figure 25-1
LP5	Decoder function in the LPI mode	25.4a.2	LPI:M	Yes [ ]	Comply with the state diagram shown in Figure 25-2
LP6	Signal_Detect assertion threshold in the LPI mode	25.4a.3	LPI:M	Yes [ ]	Minimum 400 mV peak to peak
LP7	Signal_Detect deassertion threshold in the LPI mode	25.4a.4	LPI:M	Yes [ ]	Maximum 200 mV peak to peak
LP8	Signal_Detect assertion time in the LPI mode	25.4a.5	LPI:M	Yes [ ]	Maximum 5 μs
LP9	Signal_Detect deassertion time in the LPI mode	25.4a.6	LPI:M	Yes [ ]	Maximum 5 μs
LP10	Scrambler and transmit functions deactivation time	25.4a.7	LPI:M	Yes [ ]	The scrambler and transmit functions continue to operate for the first 5 μs following tx_quiet = TRUE.

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Status	Support	Value/Comment
LP11	Transmitter output amplitude initial ramp up time	25.4a.7	LPI:M	Yes [ ]	The transmitter output delivers a signal that exceeds Signal_Detect assertion threshold within 2 μs when tx_quiet is set to TRUE.
LP12	Transmitter output recovery time after a short Quiet state	25.4a.7	LPI:M	Yes [ ]	The transmitter delivers a fully compliant signal promptly if tx_quiet is set to FALSE less than 5 μs after being set to TRUE.
LP13	Transmitter output recovery time after a long Quiet state	25.4a.7	LPI:M	Yes [ ]	The transmitter delivers a fully compliant signal within 5 μs if tx_quiet is set to FALSE more than 5 μs after being set to TRUE.

30. Management

Append the following into Table 30-1b (after aMaxFrameLength):

Table 30–1b—Capabilities

				DT
				Energy Efficient Ethernet (optional)
oMACEntity managed object class (con'd.)				
	aTransmitLPIMicroseconds	ATTRIBUTE	GET	
	aReceiveLPIMicroseconds	ATTRIBUTE	GET	
	aTransmitLPITransitions	ATTRIBUTE	GET	
	aReceiveLPITransitions	ATTRIBUTE	GET	
	aLDFastRetrainCount	ATTRIBUTE	GET	
	aLPFastRetrainCount	ATTRIBUTE	GET	

Insert the following objects after 30.3.1.1.37:

30.3.1.1 MAC entity attributes

30.3.1.1.38 aTransmitLPIMicroseconds

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 000 000 counts per second

BEHAVIOUR DEFINED AS:

A count reflecting the amount of time that the LPI_REQUEST parameter has the value ASSERT. The request is indicated to the PHY according to the requirements of the RS (see 22.7a, 35.4a, 46.4a.).;

30.3.1.1.39 aReceiveLPIMicroseconds

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 000 000 counts per second

BEHAVIOUR DEFINED AS:

A count reflecting the amount of time that the LPI_INDICATION parameter has the value ASSERT. The indication reflects the state of the PHY according to the requirements of the RS (see 22.7a, 35.4a, 46.4a.).;

30.3.1.1.40 aTransmitLPITransitions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 50 000 counts per second at 100 Mb/s; 90 000 counts per second at 1000 Mb/s; and 230 000 counts per second at 10 Gb/s

BEHAVIOUR DEFINED AS:

A count of occurrences of the transition from state LPI_DEASSERTED to state LPI_ASSERTED of the LPI transmit state diagram is the RS. The state transition corresponds to the assertion of the LPI_REQUEST parameter. The request is indicated to the PHY according to the requirements of the RS (see 22.7a, 35.4a, 46.4a.).;

30.3.1.1.41 aReceiveLPITransitions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 50 000 counts per second at 100 Mb/s; 90 000 counts per second at 1000 Mb/s; and 230 000 counts per second at 10 Gb/s

BEHAVIOUR DEFINED AS:

A count of occurrences of the transition from DEASSERT to ASSERT of the LPI_INDICATE parameter. The indication reflects the state of the PHY according to the requirements of the RS (see 22.7a, 35.4a, 46.4a.).;

30.3.1.1.42 aLDFastRetrainCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of 10GBASE-T fast retrains initiated by the local device. The indication reflects the state of the PHY event counter (see 45.2.1.76a.2 and 55.4.5.1.).;

30.3.1.1.43 aLPFastRetrainCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of 10GBASE-T fast retrains initiated by the link partner. The indication reflects the state of the PHY event counter (see 45.2.1.76a.2 and 55.4.5.1.).;

Append the following into Table 30-6 :

Table 30–6—LLDP Capabilities

				LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
oLldpXdot3Config managed object class (30.12.1)					
oLldpXdot3LocSystemsGroup managed object class (30.12.2)					
aLldpXdot3LocTxTwSys	ATTRIBUTE	GET		X	
aLldpXdot3LocTxTwSysEcho	ATTRIBUTE	GET		X	
aLldpXdot3LocRxTwSys	ATTRIBUTE	GET		X	
aLldpXdot3LocRxTwSysEcho	ATTRIBUTE	GET		X	
aLldpXdot3LocFbTwSys	ATTRIBUTE	GET		X	
aLldpXdot3TxDllReady	ATTRIBUTE	GET		X	
aLldpXdot3RxDllReady	ATTRIBUTE	GET		X	
aLldpXdot3LocDllEnabled	ATTRIBUTE	GET		X	
oLldpXdot3RemSystemsGroup managed object class (30.12.3)					
aLldpXdot3RemTxTwSys	ATTRIBUTE	GET			X
aLldpXdot3RemTxTwSysEcho	ATTRIBUTE	GET			X
aLldpXdot3RemRxTwSys	ATTRIBUTE	GET			X
aLldpXdot3RemRxTwSysEcho	ATTRIBUTE	GET			X
aLldpXdot3RemFbTwSys	ATTRIBUTE	GET			X

30.5 Layer management for medium attachment units (MAUs)

Insert new objects for LPI after 30.5.1.1.20:

30.5.1.1.21 aEEESupportList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of ENUMERATIONS that match the syntax of aMAUType

BEHAVIOUR DEFINED AS:

A read-only list of the possible PHY types for which the underlying system supports Energy Efficient Ethernet (EEE) as defined in Clause 78. If Clause 28 or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local

device;

30.12.2 LLDP Local System Group managed object class

30.12.2.1 LLDP Local System Group attributes

Insert new subclauses 30.12.2.1.22 through 30.12.2.1.29 after 30.12.2.1.21 for LPI:

30.12.2.1.22 aLldpXdot3LocTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemValue as defined in 78.4.2.3;

30.12.2.1.23 aLldpXdot3LocTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemValueEcho as defined in 78.4.2.3;

30.12.2.1.24 aLldpXdot3LocRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemValue as defined in 78.4.2.3;

30.12.2.1.25 aLldpXdot3LocRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable LocRxSystemValueEcho as defined in 78.4.2.3;

30.12.2.1.26 aLldpXdot3LocFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of the fallback $T_{w\_sys\_tx}$ that the local system is advertising to the remote system. This attribute maps to the variable LocFbSystemValue as defined in 78.4.2.3;

30.12.2.1.27 aLldpXdot3TxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE: Local system has not completed initialization of the EEE transmit Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.

TRUE: Local system has initialized the EEE transmit Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:

A GET operation returns the initialization status of the EEE transmit Data Link Layer management function on the local system.;

30.12.2.1.28 aLldpXdot3RxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE: Local system has not completed initialization of the EEE receive Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.

TRUE: Local system has initialized the EEE receive Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:

A GET operation returns the initialization status of the EEE receive Data Link Layer management function on the local system.;

30.12.2.1.29 aLldpXdot3LocDllEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE: Local system has not completed autonegotiation with a link partner that has indicated at least one EEE capability.

TRUE: Local system has completed autonegotiation with a link partner that has indicated at least one EEE capability.

BEHAVIOUR DEFINED AS:

A GET operation returns the status of the EEE capability negotiation on the local system.;

30.12.3 LLDP Remote System Group managed object class

30.12.3.1 LLDP Remote System Group attributes

Insert new subclauses 30.12.3.1.19 through 30.12.2.1.23 after 30.12.2.1.18 for LPI:

30.12.3.1.19 aLldpXdot3RemTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemValue as defined in 78.4.2.3;

30.12.3.1.20 aLldpXdot3RemTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemValueEcho as defined in 78.4.2.3;

30.12.3.1.21 aLldpXdot3RemRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemValue as defined in 78.4.2.3;

30.12.3.1.22 aLldpXdot3RemRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemValueEcho as defined in 78.4.2.3;

30.12.3.1.23 aLldpXdot3RemFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of fallback $T_{w\_sys\_tx}$ that the remote system is advertising. This attribute maps to the variable RemFbSystemValue as defined in 78.4.2.3;

35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

Insert item h) into 35.1.1 as follows:

35.1.1 Summary of major concepts

h) The GMII may also support Low Power Idle (LPI) signaling as defined for Energy Efficient Ethernet in Clause 78 for certain PHY types.

Change 35.2.1 for LPI function:

35.2.1 Mapping of GMII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The mapping is changed for EEE capability (see 78.3), as described in 35.3a.

An LPI_IDLE.request primitive with value ASSERT shall not be generated unless the attached link is operational (i.e. link_status = OK, according to the underlying PCS/PMA). The PHY shall not cause an LP_IDLE.request primitive with value ASSERT to be generated for at least one second following a link_status change to OK (see 78.1.2.1.2).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the station management entity (STA).

Change 35.2.2 to show LPI signaling:

35.2.2 GMII signal functional specifications

Insert NOTE in 35.2.2.1 for clock definitions:

NOTE—For EEE capability, GTX_CLK may be halted according to 35.2.2.5a.

Insert NOTE in 35.2.2.1 for clock definitions:

NOTE—For EEE capability, RX_CLK may be halted during periods of low utilization according to 35.2.2.8a.

Change 35.2.2.4 for TXD definition:

35.2.2.4 TXD (transmit data)

TXD is a bundle of eight data signals (TXD<7:0>) that are driven by the Reconciliation sublayer. TXD<7:0> shall transition synchronously with respect to the GTX_CLK. For each GTX_CLK period in which TX_EN is asserted and TX_ER is de-asserted, data are presented on TXD<7:0> to the PHY for transmission. TXD<0> is the least significant bit. While TX_EN and TX_ER are both de-asserted, TXD<7:0> shall have no effect upon the PHY.

While TX_EN is de-asserted and TX_ER is asserted, TXD<7:0> are used to request the PHY to generate LPI, Carrier Extend or Carrier Extend Error code-groups. The use of TXD<7:0> during the transmission of a frame with carrier extension is described in 35.2.2.5. Carrier extension shall only be signaled immediately

following the data portion of a frame. The use of TXD<7:0> to signal LPI transitions is described in 35.2.2.5a.

For EEE capability, the RS shall use the combination of TX_EN de-asserted, TX_ER asserted and TXD<7:0> equal to 0x01 as shown in Table 35–1 as a request to enter, or remain in the LPI state. Transition into and out of the LPI state is shown in Figure 35–6a.

Table 35–1 specifies the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

Table 35–1—Permissible encodings of TXD<7:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00	Reserved	—
0	1	01	Assert LPI	—
0	1	02 through 0E	Reserved	—
~~0~~	~~1~~	~~00 through 0E~~	~~Reserved~~	—
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter
NOTE—Values in TXD<7:0> column are in hexadecimal.				

Insert 35.2.2.5a after 35.2.2.5 for transmit LPI transition:

35.2.2.5a Transmit direction LPI transition

EEE capability and the LPI client are described in 78.1. The LPI client requests the PHY to transition to its low power state by asserting TX_ER and setting TXD<7:0> to 0x01. The LPI client maintains the same state for these signals for the entire time that the PHY is to remain in the low power state.

The LPI client may halt GTX_CLK at any time more than 9 clock cycles after the start of the LPI state as shown in Figure 35–6a if and only if the Clock stop capable bit is asserted (45.2.3.1.3a).

The LPI client requests the PHY to transition out of its low power state by de-asserting TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the wake up time specified for the PHY.

Figure 35–6a shows the behavior of TX_EN, TX_ER and TXD<7:0> during the transition into and out of the LPI state.

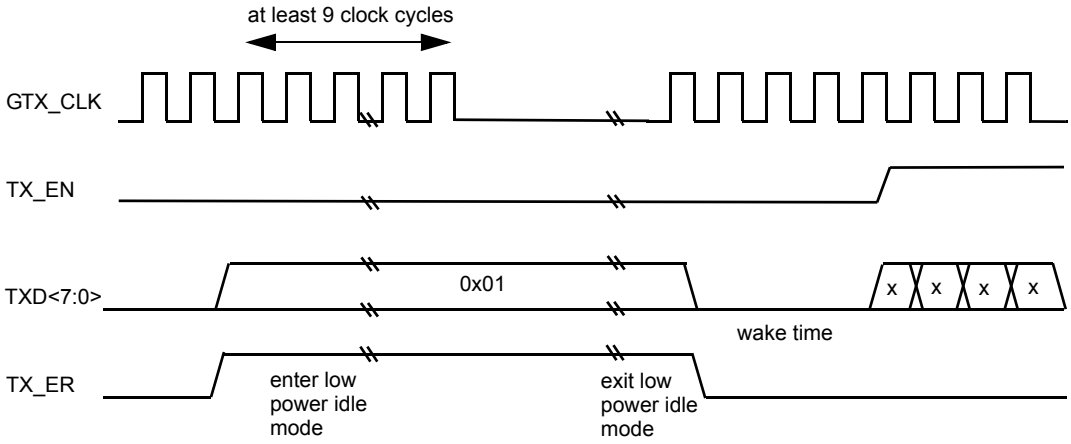


Figure 35–6a—LPI transition

Table 35–1 summarizes the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

Change 35.2.2.7 for RXD definition:

35.2.2.6 RXD (receive data)

RXD is a bundle of eight data signals (RXD<7:0>) that are driven by the PHY. RXD<7:0> shall transition synchronously with respect to RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD<7:0> transfer eight bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. Figure 35–8 shows the behavior of RXD<7:0> during frame reception.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the specific value listed in Table 35–2 onto RXD<7:0>. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication. LPI transitions are described in 35.2.2.8a.

While RX_DV is de-asserted, the PHY may indicate that it is receiving LPI by asserting the RX_ER signal while driving the value 0x01 onto RXD<7:0>.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the GMII.

In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<7:0> back to RXD<7:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD<7:0> shall not be looped back to RXD<7:0> unless the loopback mode of operation is selected.

While RX_DV is de-asserted and RX_ER is asserted, a specific RXD<7:0> value is used to transfer recovered Carrier Extend from the PHY to the Reconciliation sublayer. A Carrier Extend Error is indicated by another specific value of RXD<7:0>. Figure 35–7 shows the behavior of RX_DV during frame reception with carrier extension. Carrier extension shall only be signalled immediately following frame reception.

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–8 shows the behavior of RX_ER and RX_DV during burst reception.

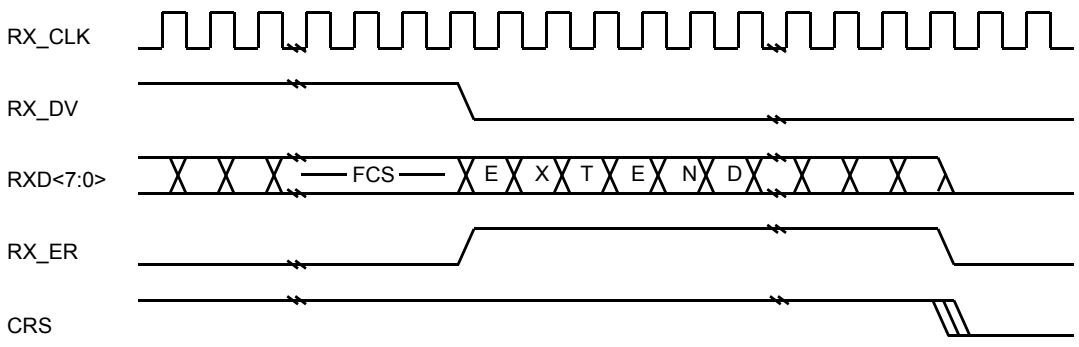


Figure 35–7—Frame reception with carrier extension

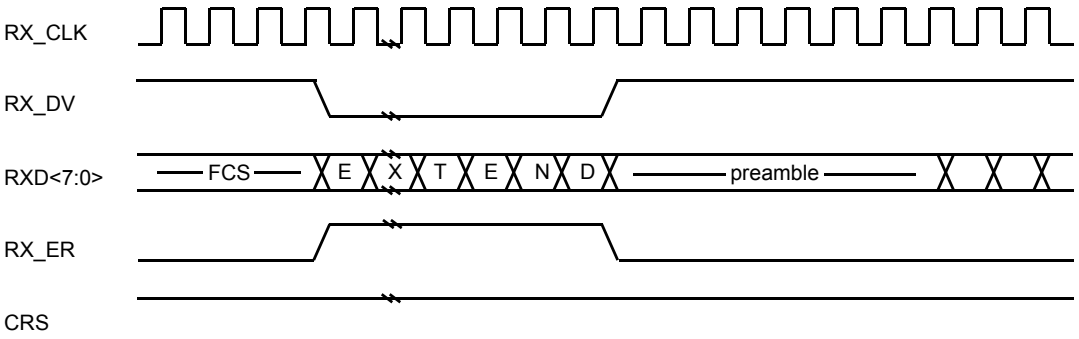


Figure 35–8—Burst reception

Table 35–2 specifies the permissible encoding of RXD<7:0>, RX_ER, and RX_DV, along with the specific indication that shall be interpreted by the RS.

Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01	Assert LPI	No applicable parameter

Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV *(continued)*

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
~~0~~	~~1~~	~~01 through 0D~~	~~Reserved~~	~~—~~
0	1	02 through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicable parameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE (eight bits)
NOTE—Values in RXD<7:0> column are in hexadecimal.				

Insert 35.2.2.8a after 35.2.2.8 for receive LPI transition:

35.2.2.8a Receive direction LPI transition

EEE capability and the LPI client are described in 78.1. When the PHY receives signals from the link partner indicating LPI, it signals this to the LPI client by asserting RX_ER and setting RXD<7:0> to 0x01 while keeping RX_DV de-asserted. The PHY maintains these signals in this state while it remains in the low power state. When the PHY receives signals from the link partner indicating its transition out of the low power state, it signals this to the LPI client by de-asserting RX_ER and returning to normal inter-frame encoding.

While the PHY device is indicating LPI the PHY device may halt the RX_CLK as shown in Figure 35–9a if and only if the Clock stop enable bit is asserted (see 45.2.3.1.3a). The PHY may restart RX_CLK at any time while it is asserting LPI, but shall restart RX_CLK so that at least one positive transition occurs before it de-asserts LPI.

Figure 35–9a shows the behavior of RX_ER, RX_DV and RXD<7:0> during LPI transitions.

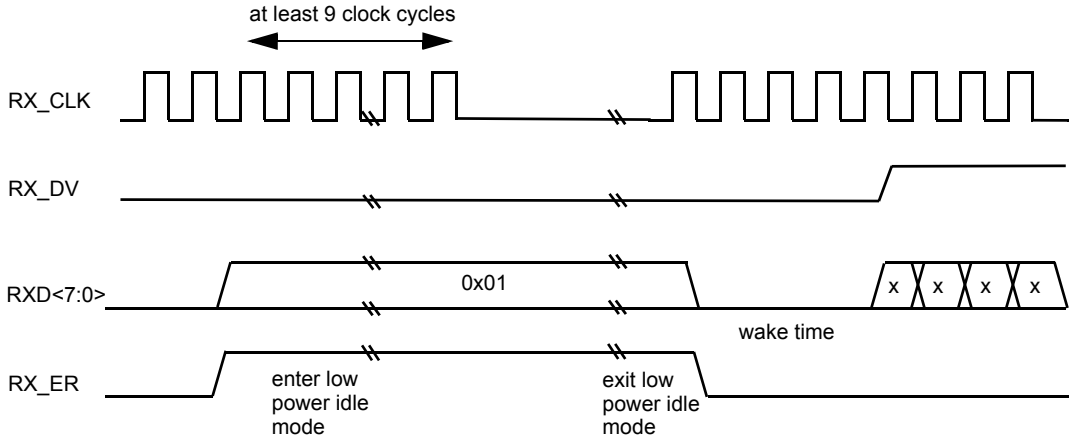


Figure 35–9a—LPI transitions (receive)

Insert a new section, 35.3a after 35.3:

35.3a LPI Assertion and Detection

Certain PHYs support Energy Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the LPI client to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the GMII signals as shown in Figure 35–21a.

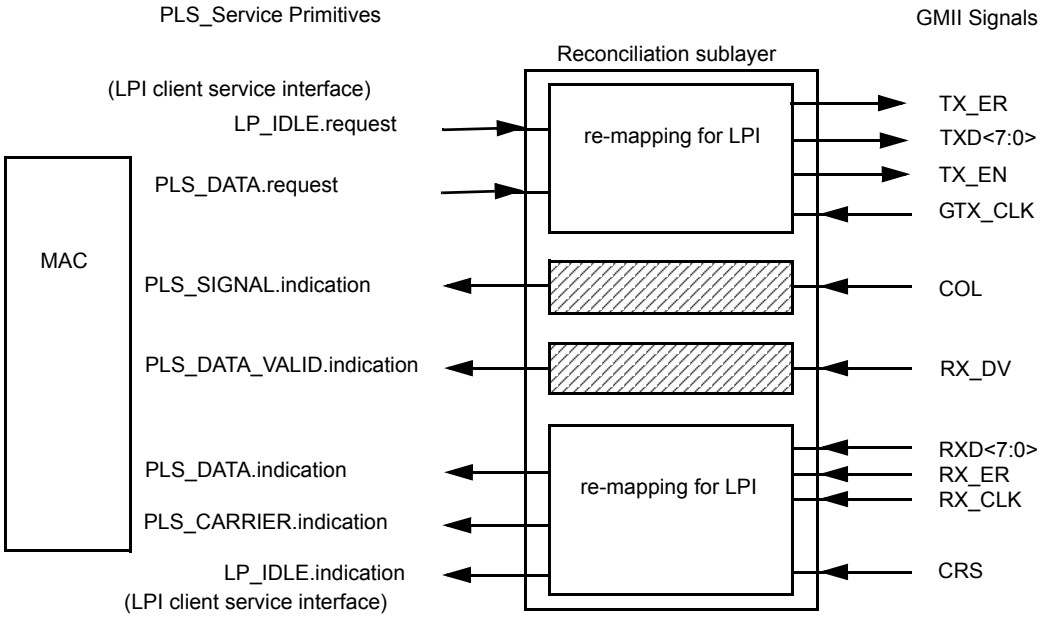


Figure 35–21a—LPI assertion and detection mechanism

The definition of TX_EN, TX_ER and TXD<7:0> is derived from the state of PLS_DATA.request (35.2.1.1), except when it is overridden by an assertion of LP_IDLE.request.

Similarly, RX_ER and RXD<7:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected

CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

35.3a.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or de-assertion of LPI from the link partner.

Values:DEASSERT: The link partner is operating with normal inter-frame behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT initiates the signaling of LPI to the link partner. DE-ASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or if LPI_REQUEST=ASSERT within 1 second of the change of link_status to OK.

35.3a.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been de-asserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state diagram and the rules mapping CARRIER_SENSE.indication defined in 35.2.1. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 35–22.

35.3a.2.1 Conventions

The notation used in the state diagram follows the conventions of 34.2.

35.3a.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
Values:FALSE: The device is completely powered (default).
TRUE: The device has not been completely powered.

rs_reset

Used by management to control the resetting of the RS.
Values:FALSE: Do not reset the RS (default).
TRUE: Reset the RS.

tw_timer

A timer that counts the time since the de-assertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 and 78.4. The minimum value of $T_{w\_sys\_tx}$ shall be 16.5 μs for 1000BASE-T and 13.26 μs for 1000BASE-KX. Signal tw_timer_done is asserted on reaching its terminal count.

35.3a.2.3 State Diagram

35.3a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the de-assertion of LPI. Buffering and queue management should be designed to accommodate this.

35.3a.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the GMII. The receive system should be aware that data frames may arrive at the GMII following the de-assertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

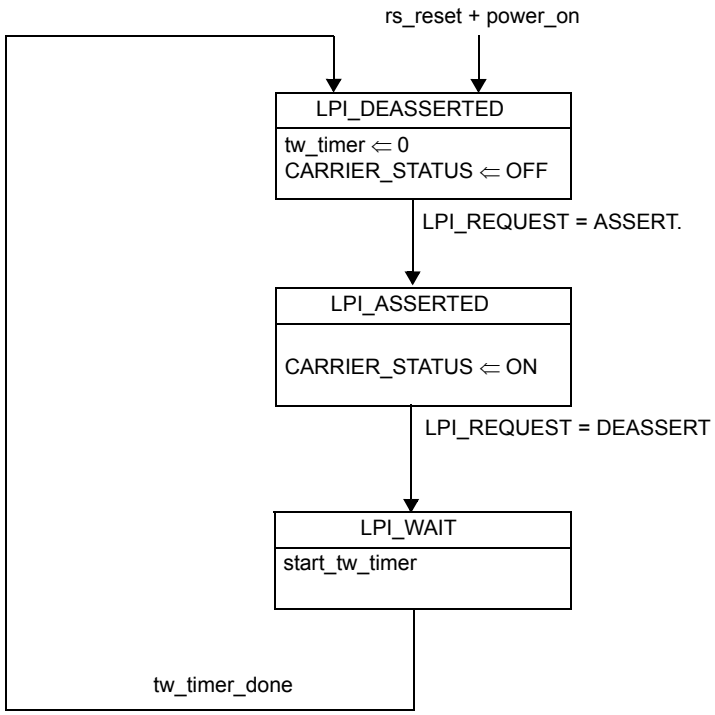


Figure 35–22—Transmit LPI State Diagram

35.5 Protocol implementation conformance statement (PICS) proforma for Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)[1]

Insert the following row into table 35.5.2.3:

35.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	35.2.2		O	Yes [ ] No [ ]

Insert the new subclause 35.5.3.3a after 35.5.3.3 for LPI functions:

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

35.5.3.3a LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	35.2.2.4	As defined in Table 35–1	LPI:M	Yes [ ]
L2	Assertion of LPI in Rx direction	35.2.2.6	As defined in Table 35–2	LPI:M	Yes [ ]
L3	GTX_CLK stoppable during LPI	35.2.2.5a	At least 9 cycles after LPI assertion	LPI:O	Yes [ ]
L4	RX_CLK stoppable during LPI	35.2.2.8a		LPI:O	Yes [ ]
L5	Terminal count for tw_timer	35.3a.2.2	Based on resolved $T_{w\_sys\_tx}$	LPI:M	Yes [ ]

36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

Change 36.2.4.7 for LPI signaling:

36.2.4.7 TXD (transmit data)

Eight ordered_sets, consisting of a single special code-group or combinations of special and data code-groups are specifically defined. Ordered_sets which include /K28.5/ provide the ability to obtain bit and code-group synchronization and establish ordered_set alignment (see 36.2.4.9 and 36.3.2.4). Ordered_sets provide for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. Table 36–3 lists the defined ordered_sets. Certain PHYs include an option (see 78.3) to transmit or receive /LI/, /LI1/ and /LI2/ to support Energy Efficient Ethernet (see Clause 78).

Insert rows into Table 36-3 below row /I2/ as follows:

Table 36–3—Defined ordered_sets

Code	TXD<7:0>	Number of Code-Groups	Encoding
/LI/	**LPI**		Correcting /LI1/, Preserving /LI2/
/LI1/	LPI 1	2	/K28.5/D6.5/
/LI2/	LPI 2	2	/K28.5/D26.4/

Insert 36.2.4.12a (after 36.2.4.12) to describe LPI signaling:

Editors' Note: *To be removed prior to publication.*
The state diagram conventions described in 36.1.7 apply to all of the state diagrams in this clause.

36.2.4.12a Low Power Idle (LPI)

LPI is transmitted in the same manner as IDLE. LPI ordered sets (\LI\) are transmitted continuously and repetitively whenever the GMII is indicating "Assert LPI". See 35.2.2.5a and 35.2.2.8a for corresponding GMII definitions.

Change the definition in 36.2.5.1.3 for "sync_status" and insert a note

sync_status

A parameter set by the PCS Synchronization process to reflect the status of the link as viewed by the receiver. The values of the parameter are defined for code_sync_status. The equation for this parameter is:

sync_status = code_sync_status + rx_lpi_active

~~Values: FAIL; The receiver is not synchronized to code-group boundaries.~~
~~OK; The receiver is synchronized to code-group boundaries.~~

NOTE: If EEE is not supported, the variable rx_lpi_active is always false and this variable is identical to code_sync_status controlled by the synchronization state diagram.

Insert new constants into 36.2.5.1.2, new variables into 36.2.5.1.3, new counters into 36.2.5.1.5, new messages into 36.2.5.1.6, and new timers into 36.2.5.1.7 to support state diagram changes. In each case, insert the new text at the end of the existing subclause

36.2.5.1.2 Constants

The following constant is used only for the EEE capability.

/LI/
The LP_IDLE ordered_set group, comprising either the /LI1/ or /LI2/ ordered_sets, as specified in 36.2.4.12a.

36.2.5.1.3 Variables

The following variables are used only for the EEE capability.

assert_lpidle
Alias used for the optional LPI function, consisting of the following terms:

(TX_EN=FALSE * TX_ER=TRUE * (TXD<7:0> =0x01))

code_sync_status
A parameter set by the PCS Synchronization process to reflect the status of the link as viewed by the receiver.

Values: FAIL; The receiver is not synchronized to code-group boundaries.
OK; The receiver is synchronized to code-group boundaries.

idle_d
Alias for the following terms:

SUDI(![/D21.5/] * ![/D2.2/])
that uses an alternate form to support the EEE capability:
SUDI(![/D21.5/] * ![/D2.2/] * ![/D6.5/] * ![/D26.4/])

rx_lpi_active
An boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

rx_quiet
A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise

tx_quiet
A boolean variable set to TRUE when the transmitter is in the TX_QUIET state and is set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 70.6.5

36.2.5.1.5 Counters

The following counter is used only for the EEE capability.

wake_error_counter

A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.8b)

36.2.5.1.6 Messages

The following messages are used only for the EEE capability.

PMD_RXQUIET.request(rx_quiet)

A signal sent by the PCS/PMA LPI receive state diagram to the PMD. Note that this message is ignored by devices that do not support EEE capability.

Values:TRUE: The receiver is in a quiet state and is not expecting incoming data.
FALSE: The receiver is ready to receive data.

PMD_TXQUIET.request(tx_quiet)

A signal sent by the PCS/PMA LPI transmit state diagram to the PMD. Note that this message is ignored by devices that do not support the optional LPI mechanism.

Values:TRUE: The transmitter is in a quiet state and may cease to transmit a signal on the medium.
FALSE: The transmitter is ready to transmit data.

36.2.5.1.7 Timers

The following timers are used only for the EEE capability.

rx_tq_timer

This timer is started when the PCS receiver enters the START_TQ_TIMER state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer

This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall not exceed the maximum value of T_{WR} in Table 36–3b. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer

This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the quiescent state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer

This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer

This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QI}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer

This timer is started when the PCS transmitter enters the TX_REFRESH state. The timer terminal count is set to T_{UI}. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

Change Figure 36–5 (New states and transitions are in dotted boxes) and Figure 36–6 in 36.2.5.2.1 as follows:

36.2.5.2.1 Transmit

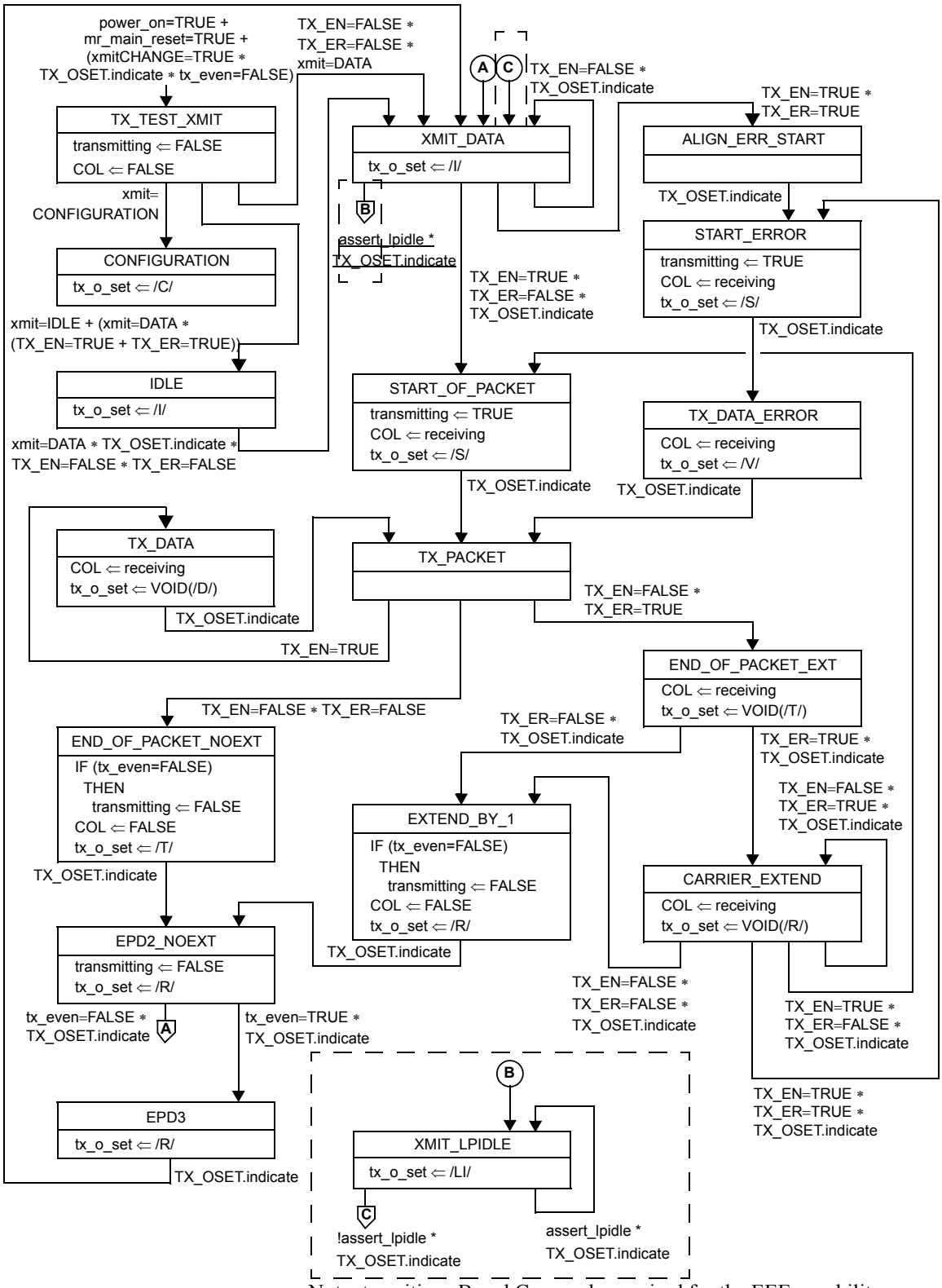


Figure 36–5—PCS transmit ordered_set state diagram

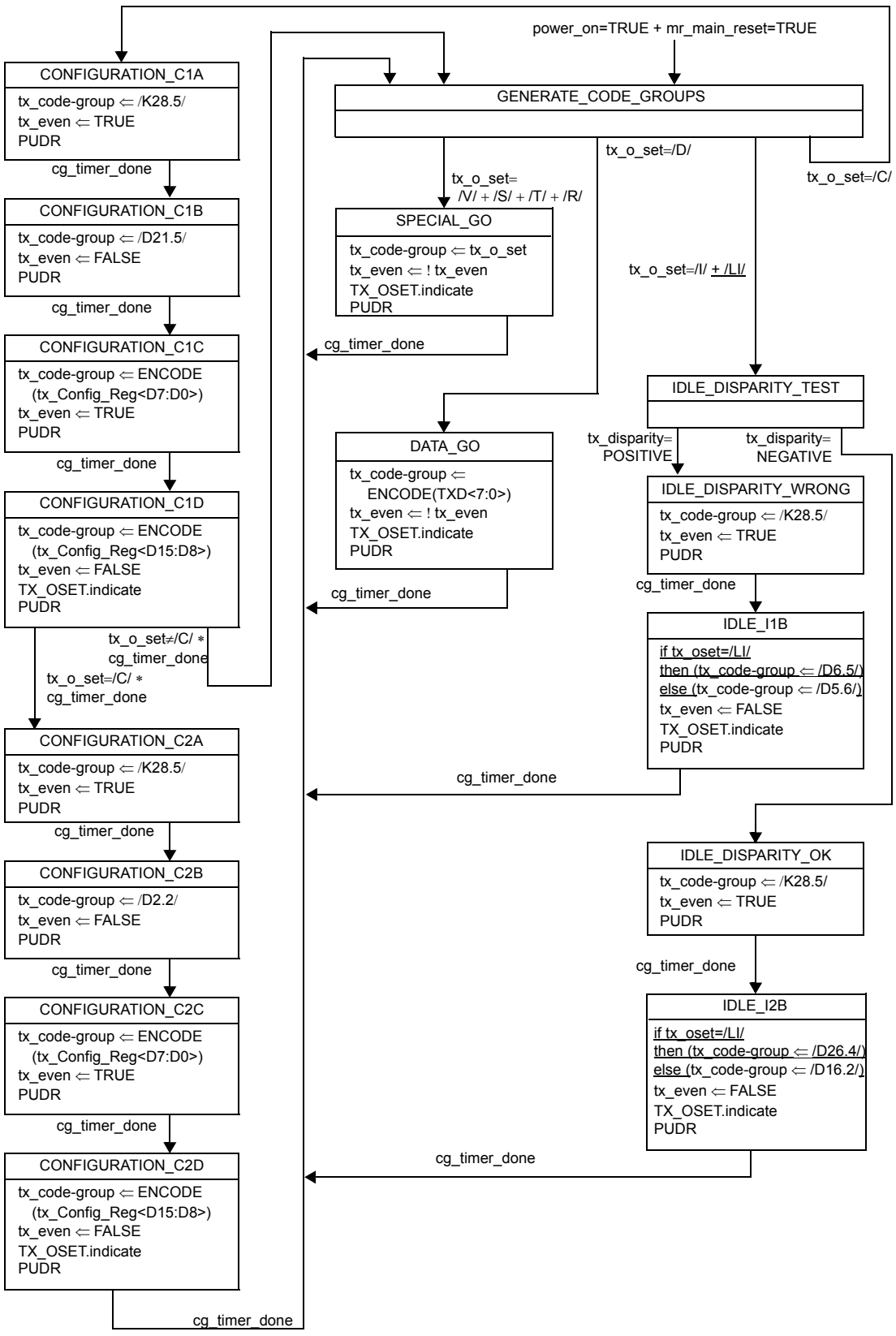
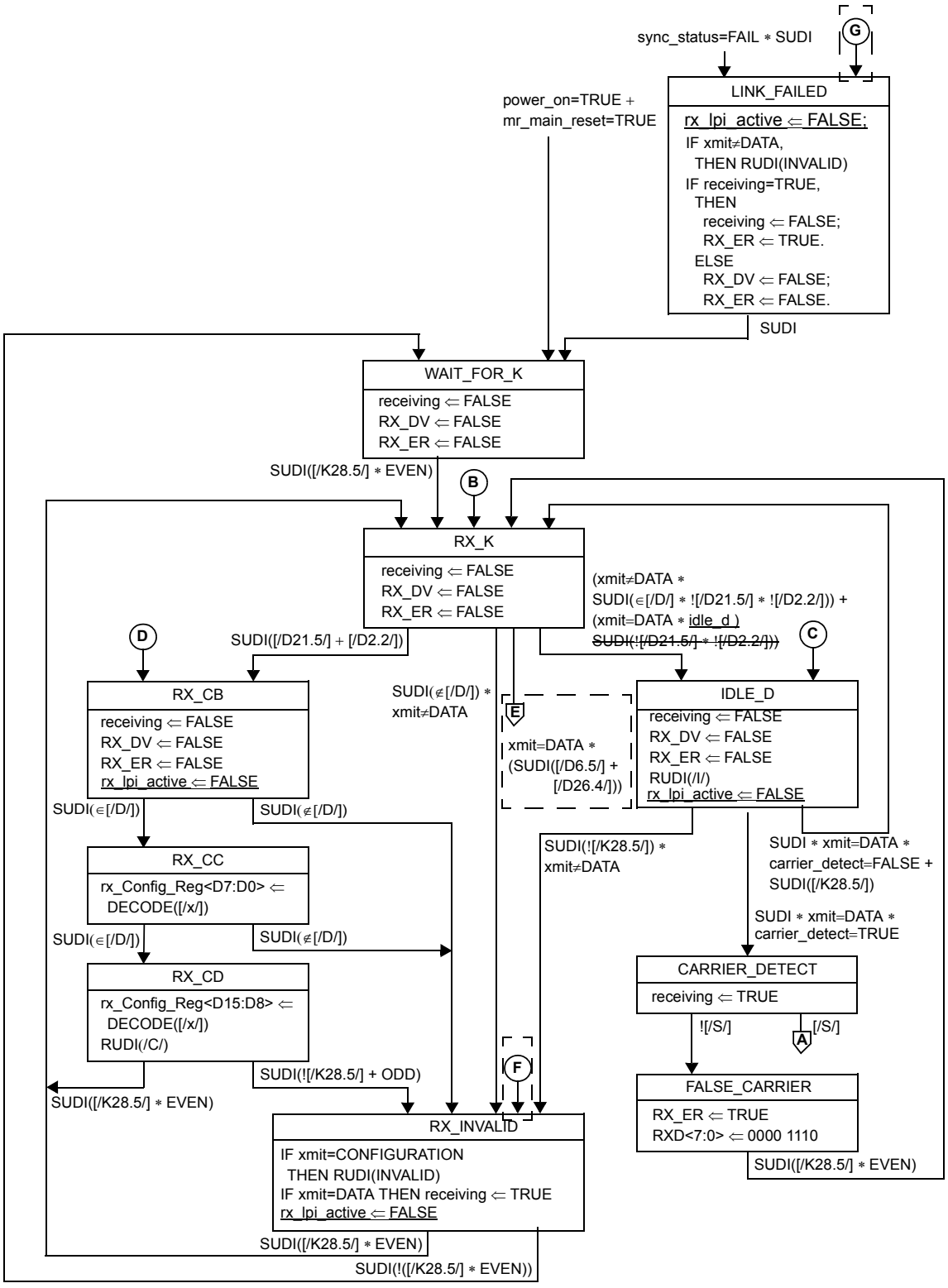


Figure 36–6—PCS transmit code-group state diagram

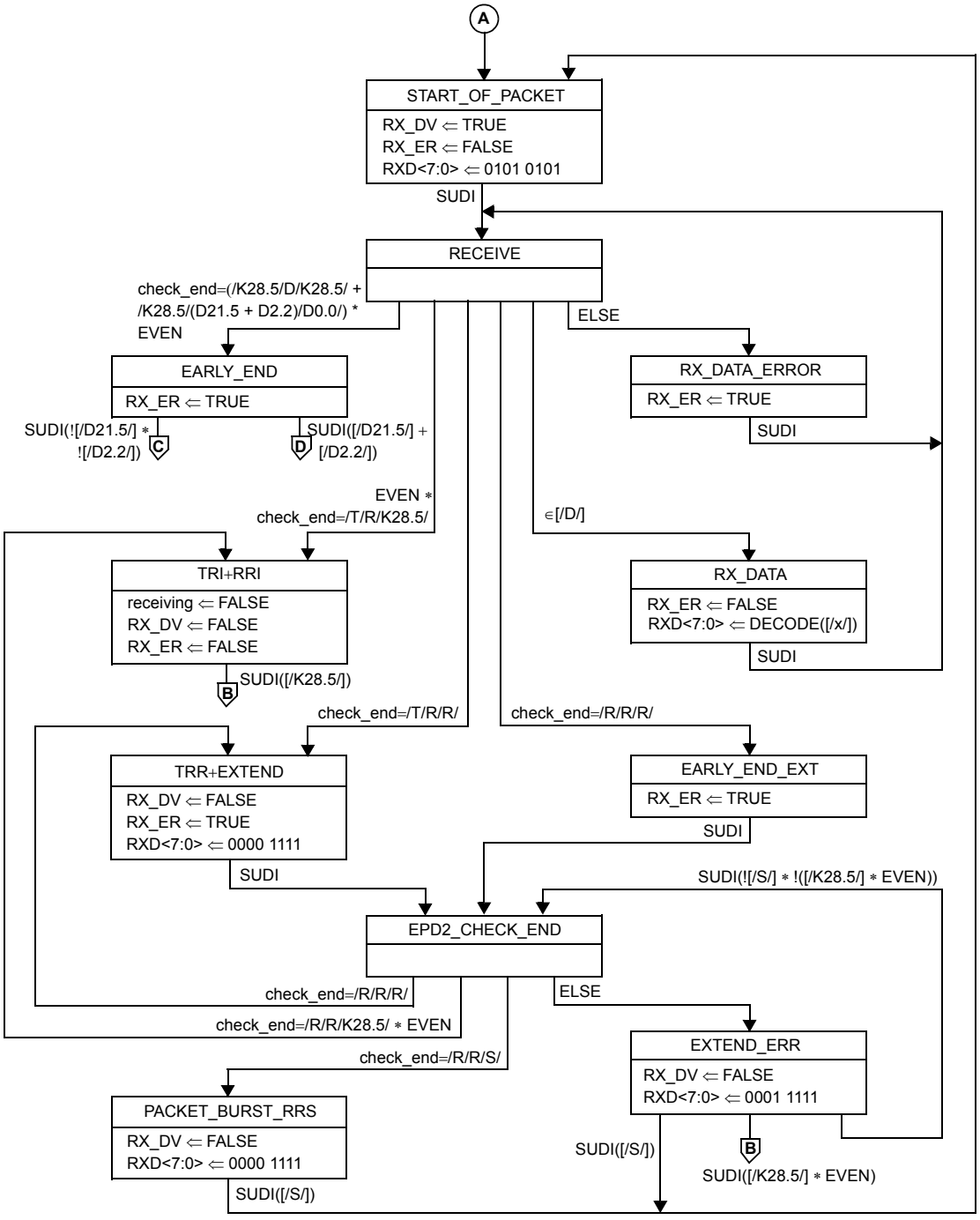
Change Figure 36–7a (New states and transitions are in dotted boxes) and Figure 36–7b and insert Figure 36–7c in 36.2.5.2.2 as follows:

36.2.5.2.2 Receive



NOTE—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7b and Figure 36–7c, and vice versa.

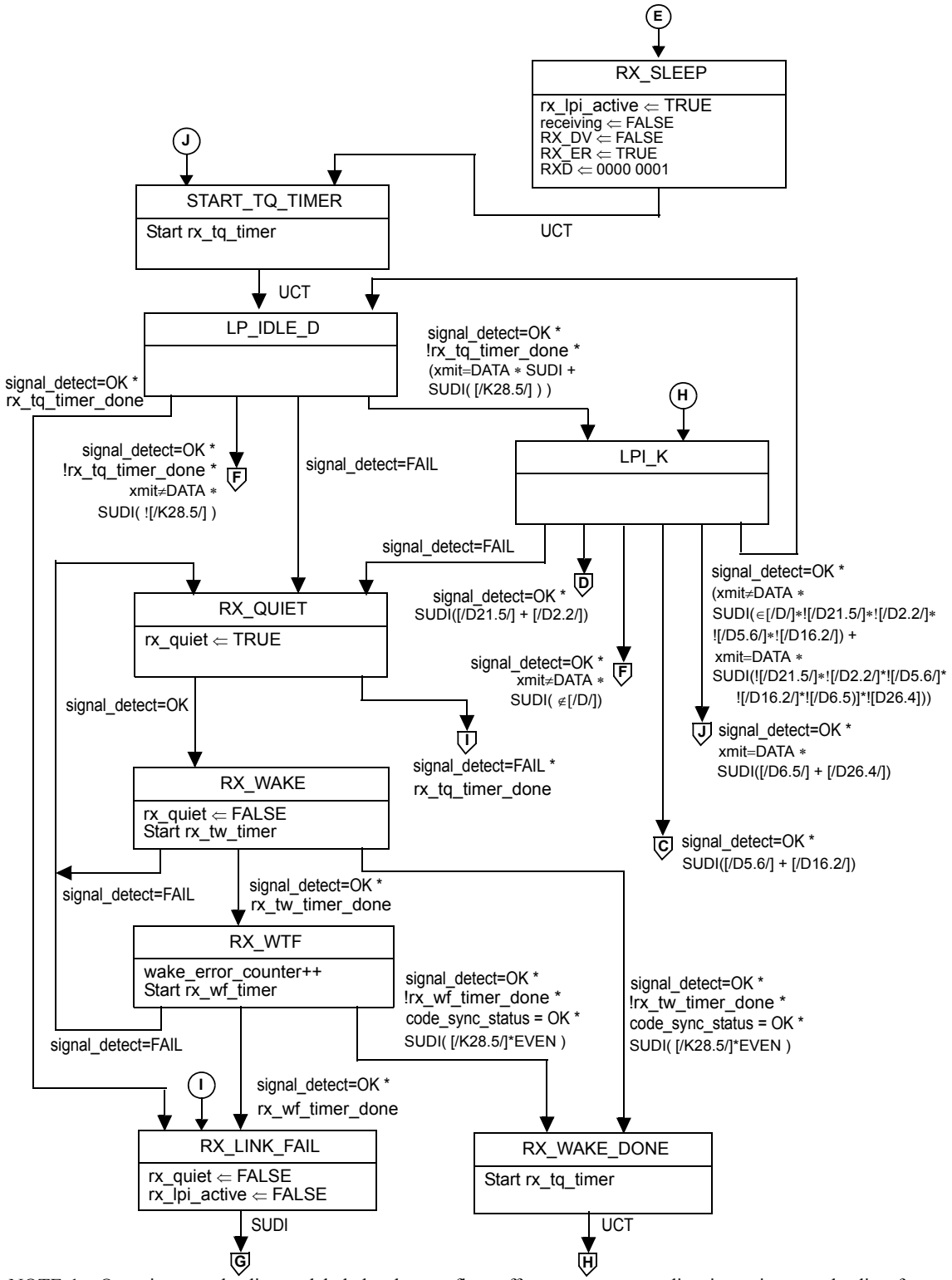
Figure 36–7a—PCS receive state diagram, part a



NOTE 1—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

NOTE 2—In the transition from RECEIVE to RX_DATA state the transition condition is a test against the code-group obtained from the SUDI that caused the transition to RECEIVE state.

Figure 36–7b—PCS receive state diagram, part b



NOTE 1—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

Figure 36–7c—PCS Receive state diagram, part c (only required for the optional EEE capability)

Insert the following paragraph between the third and fourth paragraphs of 36.2.5.2.6:

36.2.5.2.6 Synchronization

For EEE capability the relationship between sync_status and code_sync_status is given by Figure 36–7c, otherwise sync_status is identical to code_sync_status.

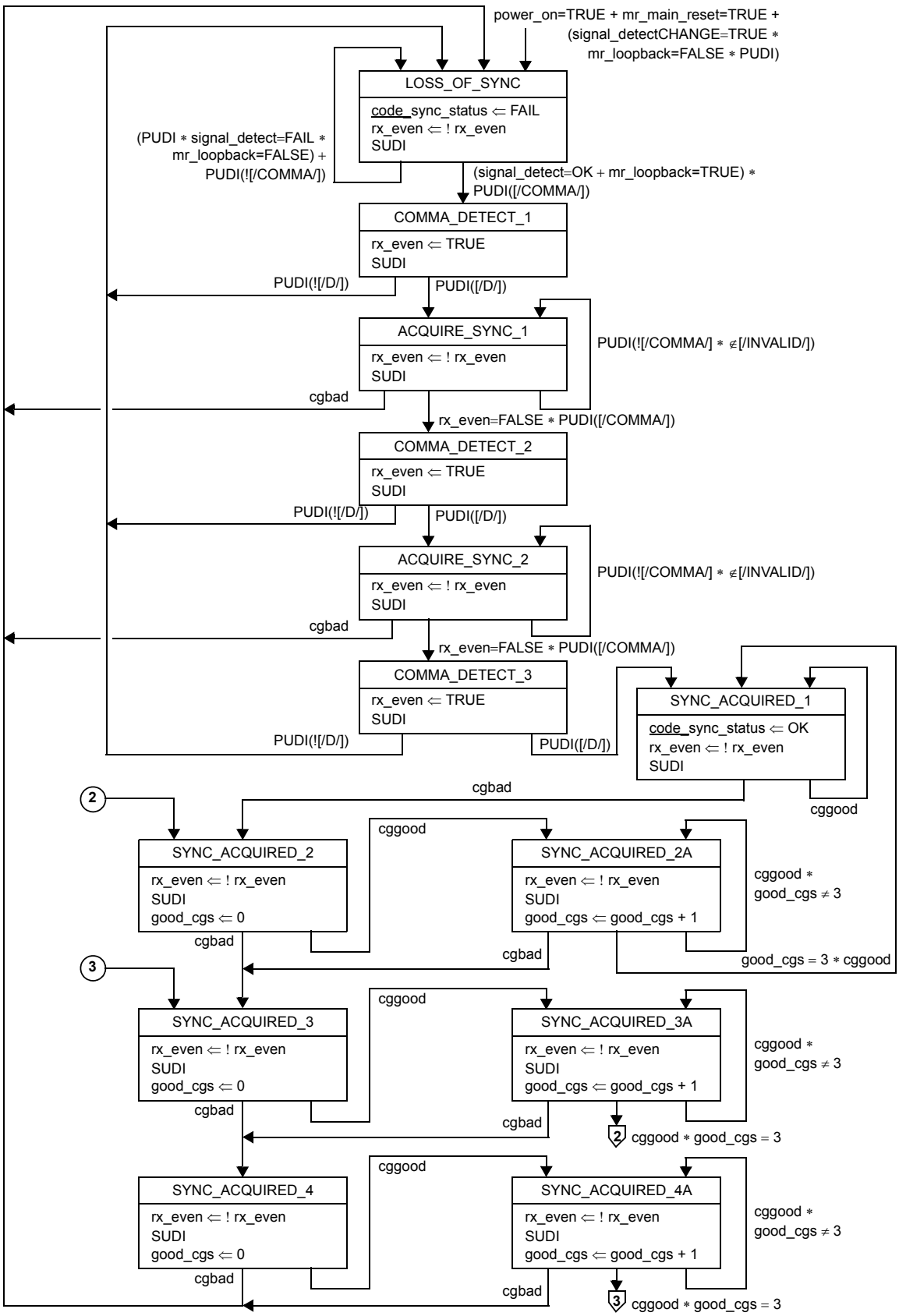


Figure 36–9—Synchronization state diagram

Insert 36.2.5.2.8 after 36.2.5.2.7 for LPI state diagram:

36.2.5.2.8 LPI state diagram

A PCS which supports the EEE capability shall implement the LPI transmit process as shown in Figures 36–9a. The transmit LPI state diagram controls tx_quiet which disables the transmitter when true.

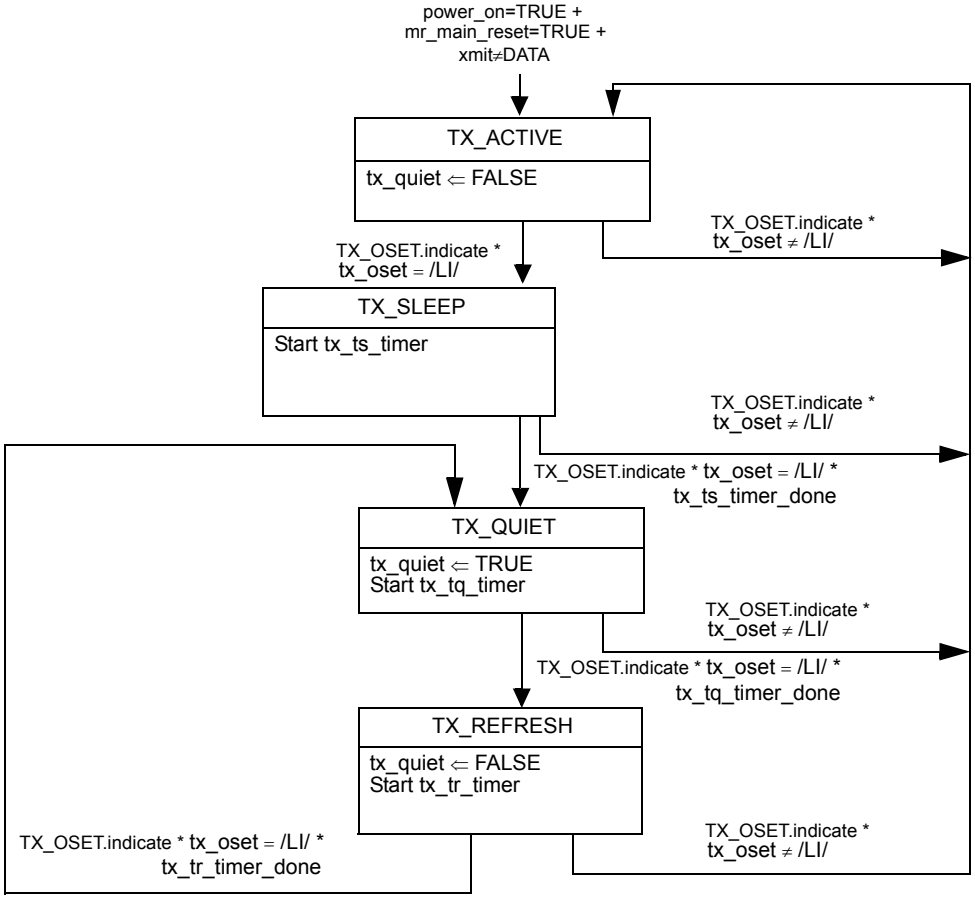


Figure 36–9a—LPI Transmit state diagram

The timer values for these state diagrams are shown in Table 36–3a for transmit and Table 36–3b for receive.

Table 36–3a—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_quiet is set to TRUE	19.9	20.1	μs
T_{QL}	Local Quiet Time from when tx_quiet is set to TRUE to entry into the TX_REFRESH state	2.5	2.6	ms
T_{UL}	Local Refresh Time from entry into the TX_REFRESH state to entry into the TX_QUIET state	19.9	20.1	μs

Table 36–3b—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect to be set to OK while in the LP_IDLE_D, LPI_K and RX_QUIET states before asserting a rx_fault	3	4	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (WTF).		11	μs
T_{WTF}	Wake time fault recovery time		1	ms

Insert 36.2.5.2.9 for LPI status:

36.2.5.2.9 LPI status and management

For EEE capability, the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variables shown in Table 36–3c.

Table 36–3c—MDIO status indications

MDIO status variable	Register name	Register address	Note
Tx LPI received	PCS status register 1	3.1.11	Latched version of 3.1.9
Rx LPI received	PCS status register 1	3.1.10	Latched version of 3.1.8
Tx LPI indication	PCS status register 1	3.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	PCS status register 1	3.1.8	TRUE when not in state RX_ACTIVE

36.7 Protocol implementation conformance statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X[1]

Insert the following row into table 36.7.3:

36.7.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	36.2.4.12a		O	Yes [ ] No [ ]

Insert the new subclause 36.7.4.9 after 46.7.4.8 for LPI functions:

36.7.4.9 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Transmit ordered set state diagram	36.2.5.2.1	Support additions to Figure 36–5 for LPI operation	LPI:M	Yes [ ] No [ ]
LP-02	Receive state diagram	36.2.5.2.2	Support additions to Figure 36–7a, Figure 36–7a for LPI operation	LPI:M	Yes [ ] No [ ]
LP-03	LPI transmit state diagram	36.2.5.2.8	Meets the requirements of Figure 36–9a	LPI:M	Yes [ ] No [ ]
LP-04	LPI receive state diagram	36.2.5.2.8	Meets the requirements of Figure 36–7c	LPI:M	Yes [ ] No [ ]
LP-03	LPI transmit timing	36.2.5.2.8	Meets the requirements of Table 36–3a	LPI:M	Yes [ ] No [ ]
LP-04	LPI receive timing	36.2.5.2.8	Meets the requirements of Table 36–3b	LPI:M	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

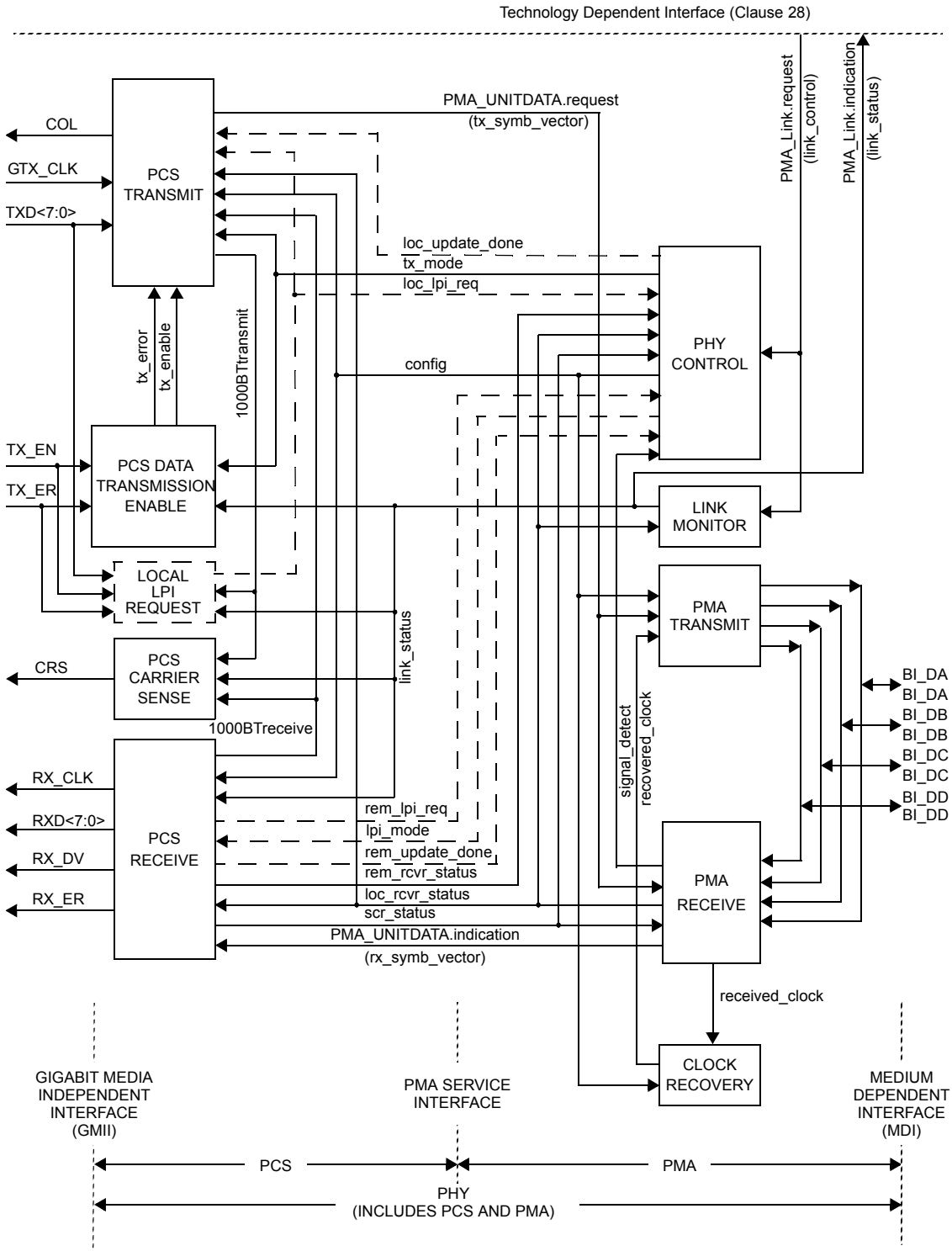
40.1.3 Operation of 1000BASE-T

Insert paragraph as shown before the last paragraph of 40.1.3:

A 1000BASE-T PHY with the optional Energy Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The "Assert LPI" request at the GMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as "Assert LPI" at the GMII. When LPI signaling is simultaneously transmitted and received, an Energy Efficient 1000BASE-T PHY ceases transmission and deactivates transmit and receive functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the GMII, the PHY re-activates transmit and receive functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

The conditions for supporting the optional EEE capability are defined in 78.3.

Replace the existing Functional block diagram figure (Figure 40–3) with the new Functional block diagram figure shown in Figure 40–3.



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 40–3—Functional block diagram

40.1.3.1 Physical Coding Sublayer (PCS)

Insert text shown below after the fourth paragraph is 40.1.3.1 as shown below:

When the PHY supports the optional EEE capability, Idle mode encoding also conveys to the remote PHY information of whether the local PHY is requesting entry into the LPI mode or not. Such requests are a direct translation of "Assert LPI" at the GMII. In addition, Idle mode encoding conveys to the remote PHY whether the local PHY has completed the update of its receiver state or not, as indicated by the PMA PHY Control function.

40.1.3.2 Physical Medium Attachment (PMA) sublayer

Insert the following text before the last paragraph of 40.1.3.2:

When the PHY supports the optional EEE capability, the PMA PHY Control function also coordinates transitions between the LPI mode and the normal operating mode.

40.1.4 Signaling

Insert new items j) and k) into the list of signaling scheme objectives as shown below and renumber subsequent items in list:

j) Optionally, ability to signal to the remote PHY a request to enter the LPI mode and to exit the LPI mode and return to normal operation.
k) Optionally, ability to signal to the remote PHY that the update of the local receiver state (e.g. timing recovery, adaptive filter coefficients) has completed.

Change the last paragraph of 40.1.4 as shown below:

The PHY ~~operates~~ may operate in ~~two~~ three basic modes, normal ~~mode~~mode, training mode, or ~~training~~an optional LPI mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA. In training mode, the PCS is directed to generate only idle code-groups for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. In LPI mode, the PCS is directed to generate only idle code groups encoded with LPI request and update status indications, or zeros as dictated by the PMA PHY Control function. (See the PCS reference diagram in 40.2.).

40.2.2 PMA Service Interface

Insert new items appended to the existing list of service primitives as shown below:

PMA_LPIMODE.indication(lpi_mode)

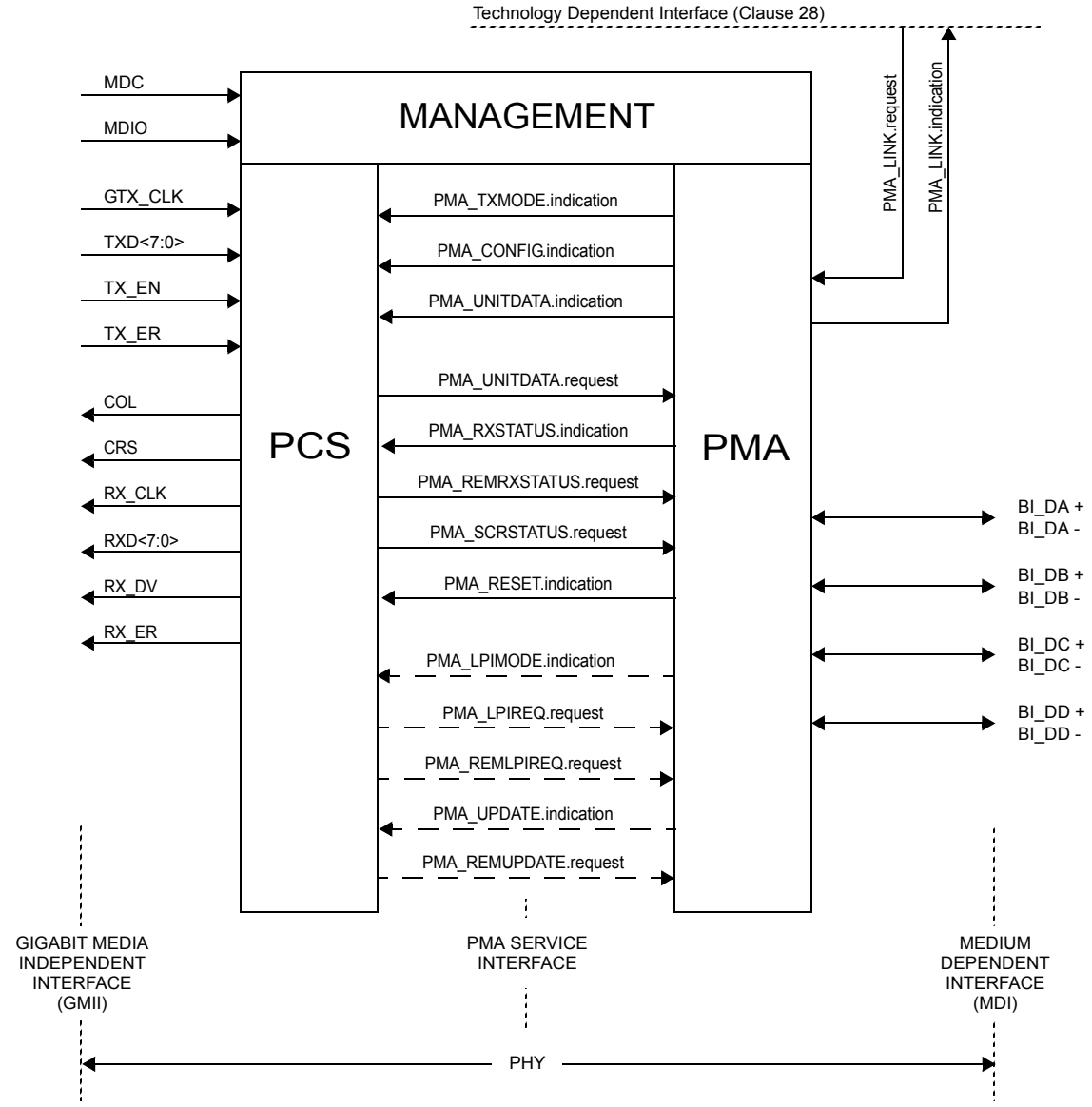
PMA_LPIREQ.request(loc_lpi_req)

PMA_REMLPIREQ.request(rem_lpi_req)

PMA_UPDATE.indication(loc_update_done)

PMA_REMUPDATE.request(rem_update_done)

Replace Figure 40–4 with the new Figure 40–4 shown below:



NOTE—Service interface primitives shown with dashed lines are only required for the EEE capability.

Figure 40–4—1000BASE-T service interfaces

Insert the following text after 40.2.10 PMA_RESET.indication:

40.2.11 PMA_LPIMODE.indication

This primitive is generated by the PMA to indicate that the PHY has entered the LPI mode of operation.

40.2.11.1 Semantics of the primitive

PMA_LPIMODE.indication(lpi_mode)

PMA_LPIMODE.indication specifies to the PCS Receive function, via the parameter lpi_mode, whether or not the PHY has entered LPI mode. The parameter lpi_mode can take on one of the following values of the form:

ON	This value is asserted with then PHY is operating in LPI mode.
OFF	This value is asserted during normal operation.

40.2.11.2 When generated

The PMA PHY Control function generates PMA_LPIMODE.indication messages continuously.

40.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Receive function as described in 40.3.1.4.

40.2.12 PMA_LPIREQ.request

This primitive is generated by the PCS to indicate a request to enter the LPI mode.

40.2.12.1 Semantics of the primitive

PMA_LPIREQ.request (loc_lpi_req)

PMA_LPIREQ.request specifies to the PMA PHY Control, via the parameter loc_lpi_req, whether or not the PHY is requested to enter the LPI mode. The parameter loc_lpi_req can take on one of the following values of the form:

TRUE	This value is continuously asserted when “Assert LPI” is present on the GMII. Note that “Assert LPI” at the GMII implies that no frame transmission is in progress hence 1000BTtransmit (see 40.3.3.1) will be set to FALSE by the PCS Transmit state diagram.
FALSE	This value is continuously asserted when “Assert LPI” is not present at the GMII.

40.2.12.2 When generated

The PCS Local LPI Request function generates PMA_LPIREQ.request messages continuously.

40.2.12.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.2.13 PMA_REMLPIREQ.request

This primitive is generated by the PCS to indicate a request to enter LPI mode as communicated by the remote PHY via its encoding of its loc_lpi_req parameter.

40.2.13.1 Semantics of the primitive

PMA_REMLPIREQ.request (rem_lpi_req)

PMA_REMLPIREQ.request specifies to the PMA PHY Control, via the parameter rem_lpi_req, whether or not the remote PHY is requesting entry into the LPI mode. The parameter rem_lpi_req can take on one of the follow values of the form:

TRUE	This value is continuously asserted when LPI is encoded in the received symbols.
FALSE	This value is continuously asserted when LPI is not encoded in the received symbols.

40.2.13.2 When generated

The PCS Receive function generates PMA_REMLPIREQ.request messages continuously on the basis of the signals received at the MDI.

40.2.13.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.2.14 PMA_UPDATE.indication

This primitive is generated by the PMA to indicate that the PHY has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients).

40.2.14.1 Semantics of the primitive

PMA_UPDATE.indication(loc_update_done)

PMA_UPDATE.indication specifies to the PCS Transmit functions, via the parameter loc_update_done, whether or not the PHY has completed the update of its receiver state. The parameter loc_update_done can take on one of the following values of the form:

TRUE	This value is asserted when the PHY has completed the current update.
FALSE	This value is asserted when the PHY is ready for the next update or when the current update is still in progress.

40.2.14.2 When generated

The PMA PHY Control function generates PMA_UPDATE.indication messages continuously.

40.2.14.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3 and 40.3.1.4.

40.2.15 PMA_REMUPDATE.request

This primitive is generated by the PCS to indicate that the remote PHY has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients).

40.2.15.1 Semantics of the primitive

PMA_REMUPDATE.request(rem_update_done)

PMA_REMUPDATE.indication specifies to the PMA PHY Control function, via the parameter rem_update_done, whether or not the remote PHY has completed the update of its receiver state. The parameter rem_update_done can take on one of the following values of the form:

TRUE	This value is asserted when the remote PHY has completed the current update.
FALSE	This value is asserted to when the remote PHY is ready for the next update or when the current update is still in progress.

40.2.15.2 When generated

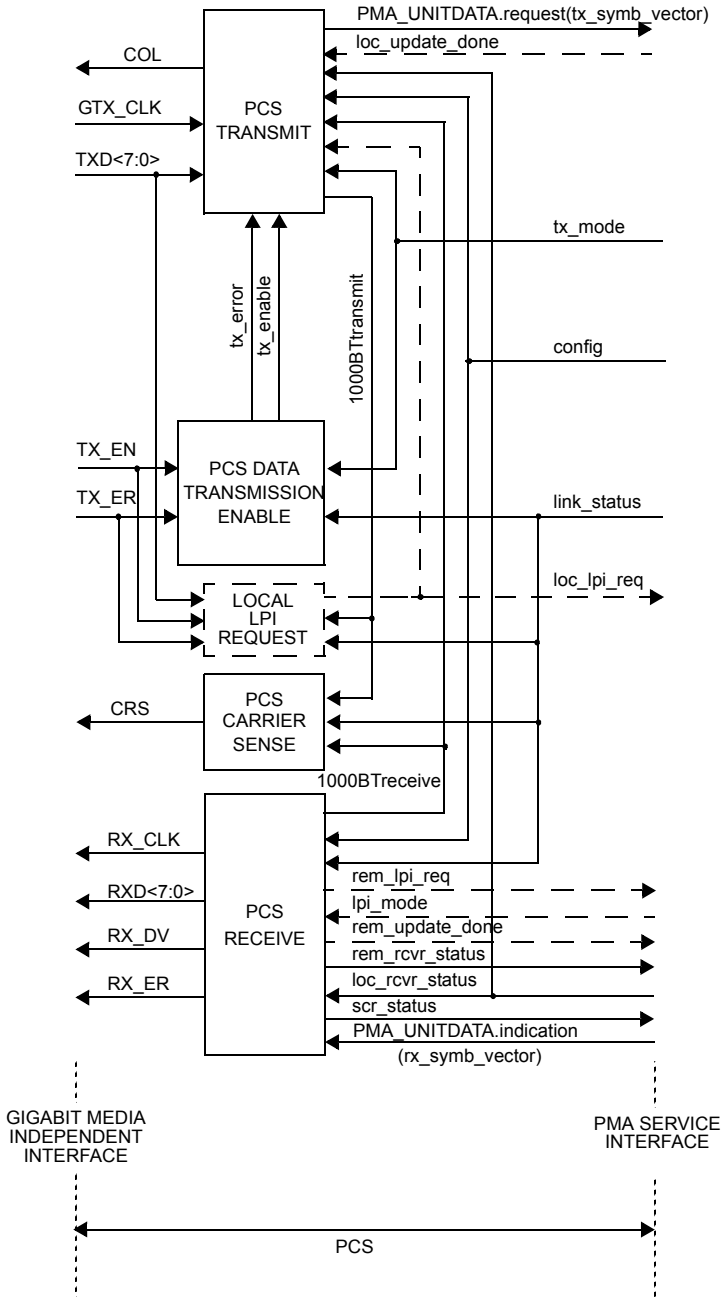
The PCS Receive function generates PMA_REMUDPATE.request messages continuously.

40.2.15.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.3 Physical Coding Sublayer (PCS)

Replace the existing PCS reference diagram, Figure 40–5 with the new Figure 40–5 shown below:



NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 40–5—PCS reference diagram

40.3.1.3 PCS Transmit function

Insert text between paragraphs five and six as shown below:

When the PHY supports the optional EEE capability, the LPI mode encoding also takes into account the value of the parameter loc_lpi_req. By this mechanism, the PHY indicates whether it requests to operate in LPI mode or return to the normal mode of operation. In addition, LPI mode encoding takes into account the

value of loc_update_done. By this mechanism, the PHY indicates whether it has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients) or not, as indicated by the PMA PHY Control function.

40.3.1.3.4 Generation of bits $Sd_n[8:0]$

Change the paragraph following the equation for $Sd_n[6]$ as shown below:

The bits Sd_n[5:4]~~[5:3]~~ are derived from the bits Sc_n[5:4]~~[5:3]~~ and the GMII data bits TXD_n[5:4]~~[5:3]~~ as

Replace the equation for $Sd_n[5:3]$ with the equation for $Sd_n[5:4]$ as shown below:

$$Sd_n[5:4] = \begin{cases} Sc_n[5:4] \wedge TXD_n[5:4] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[5:4] & \text{else} \end{cases}$$

Insert a new paragraph and equation for Sdn[3] following the equation for $Sd_n[5:4]$, formerly the equation for $Sd_n[5:3]$, as shown below:

The bit Sd_n[3] is used to scramble the GMII data bit TXD_n[3] during data mode and to encode loc_lpi_req otherwise. It is defined as

$$Sd_n[3] = \begin{cases} Sc_n[3] \wedge TXD_n[3] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[3] \wedge 1 & \text{else if } ((loc\_lpi\_req = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[3] & \text{else} \end{cases}$$

Replace the equation for $Sd_n[2]$ with the equation shown below:

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } ((loc\_rcvr\_status = \text{OK}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[2] & \text{else} \end{cases}$$

Change the paragraph following the equation for $Sd_n[2]$ as shown below:

The bits Sdn[1:0] are used to transmit carrier extension information during tx_mode=SEND_N and are thus dependent upon the bits cextn and cext_errn. In addition, bit Sd_n[1] is used to encode loc_update_done. These bits are dependent on the variable tx_errorn, which is defined in Figure 40–8. These bits are defined as

Replace the equations for $cext\_err_n$ and $Sd_n[1]$ with the equations shown below:

$$cext\_err_n = \begin{cases} tx\_error_n & \text{if } ((tx\_enable_n = 0) \text{ and } (TXD_n[7:0] \neq 0x0F) \text{ and } (loc\_lpi\_req = FALSE)) \\ 0 & \text{else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[1] \wedge 1 & \text{else if } ((loc\_update\_done = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[1] \wedge cext\_err_n & \text{else} \end{cases}$$

40.3.1.4 PCS Receive function

Insert the text below following the second paragraph:

When the PHY supports the optional EEE capability, the PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode to derive the values of the variables rem_lpi_req and rem_update_done.

Insert the text below as 40.3.1.6 following 40.3.1.5 PCS Carrier Sense function:

40.3.1.6 PCS Local LPI Request function

The PCS Local LPI Request function generates the signal loc_lpi_req, which indicates to the PMA PHY Control function whether or not the local PHY is requested to enter the LPI mode. When the PHY supports the optional EEE capability, the PCS shall conform to the Local LPI Request state diagram as depicted in Figure 40–8a including compliance with the associated state variables as specified in 40.3.3.

40.3.3 State variables

40.3.3.1 Variables

Change the following variable definition as shown:

1000BTtransmit
: A Boolean used by the PCS Transmit Process to indicate whether a frame transmission is in progress. Also ~~U~~used by the Carrier Sense and Local LPI Request processes.
Values: TRUE: The PCS is transmitting a stream
FALSE: The PCS is not transmitting a stream

Insert text following the existing list of variables as shown below:

The following state variables are only required for the optional EEE capability.

loc_lpi_req
: The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the LPI mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.
Values: TRUE or FALSE

lpi_mode
: The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered LPI mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. In the absence of the optional EEE capability, the PHY operates as if the value of this variable is OFF.
Values: ON or OFF

rem_lpi_req

The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into LPI mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE or FALSE

40.3.4 State diagrams

Editor's Note (to be removed prior to publication): The state diagram conventions described in 40.1.6 apply to all of the state diagrams in this clause.

Insert the PCS Local LPI Request state diagram (Figure 40-8a) after Figure 40-8 and renumber subsequent figures:

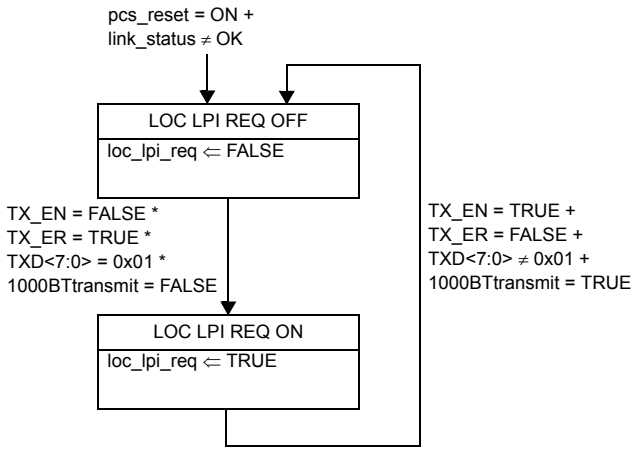


Figure 40–8a—PCS Local LPI Request state diagram (optional)

Replace existing PCS Receive state diagrams, part a (Figure 40-10a) with new PCS Receive state part a

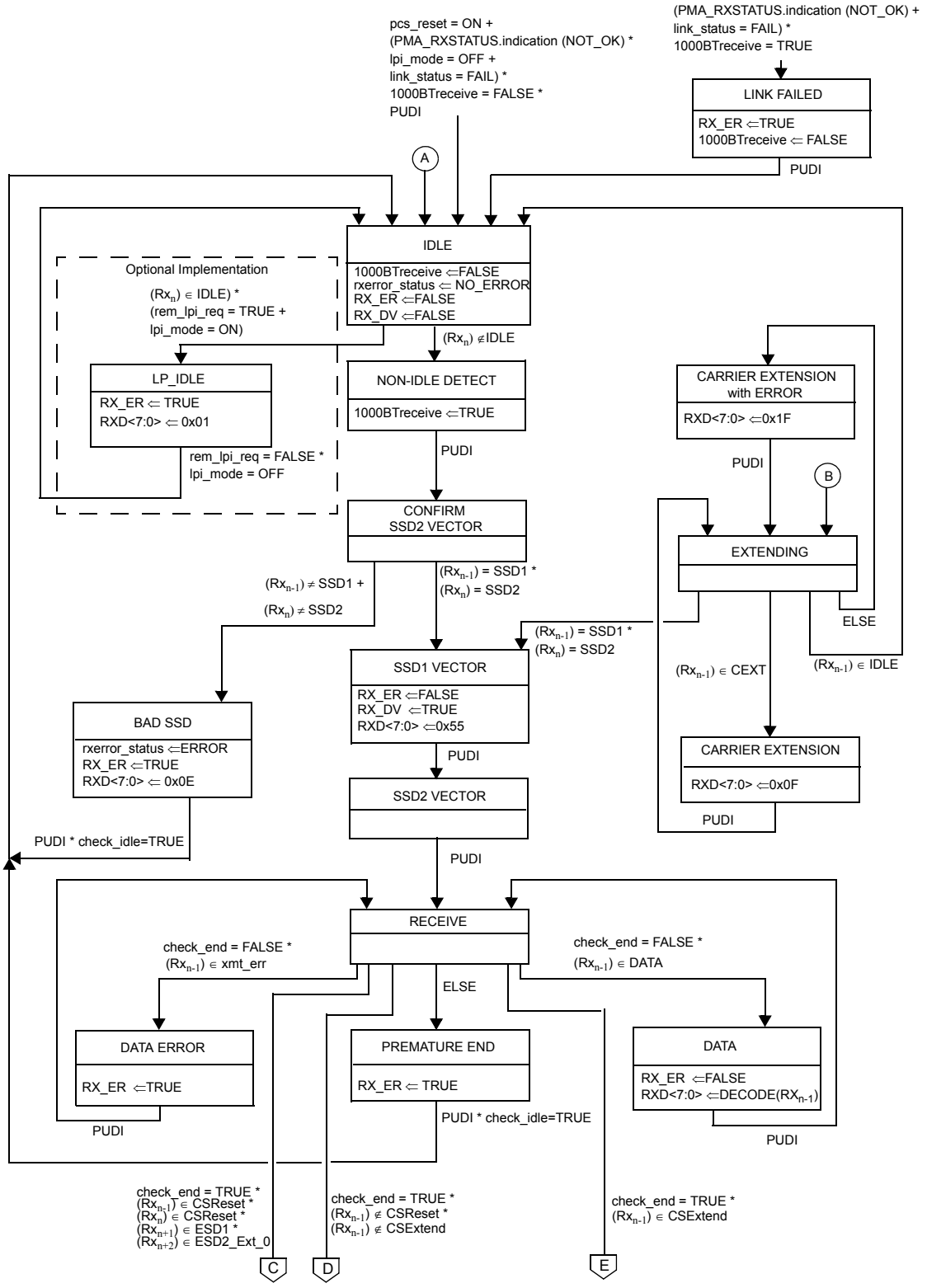
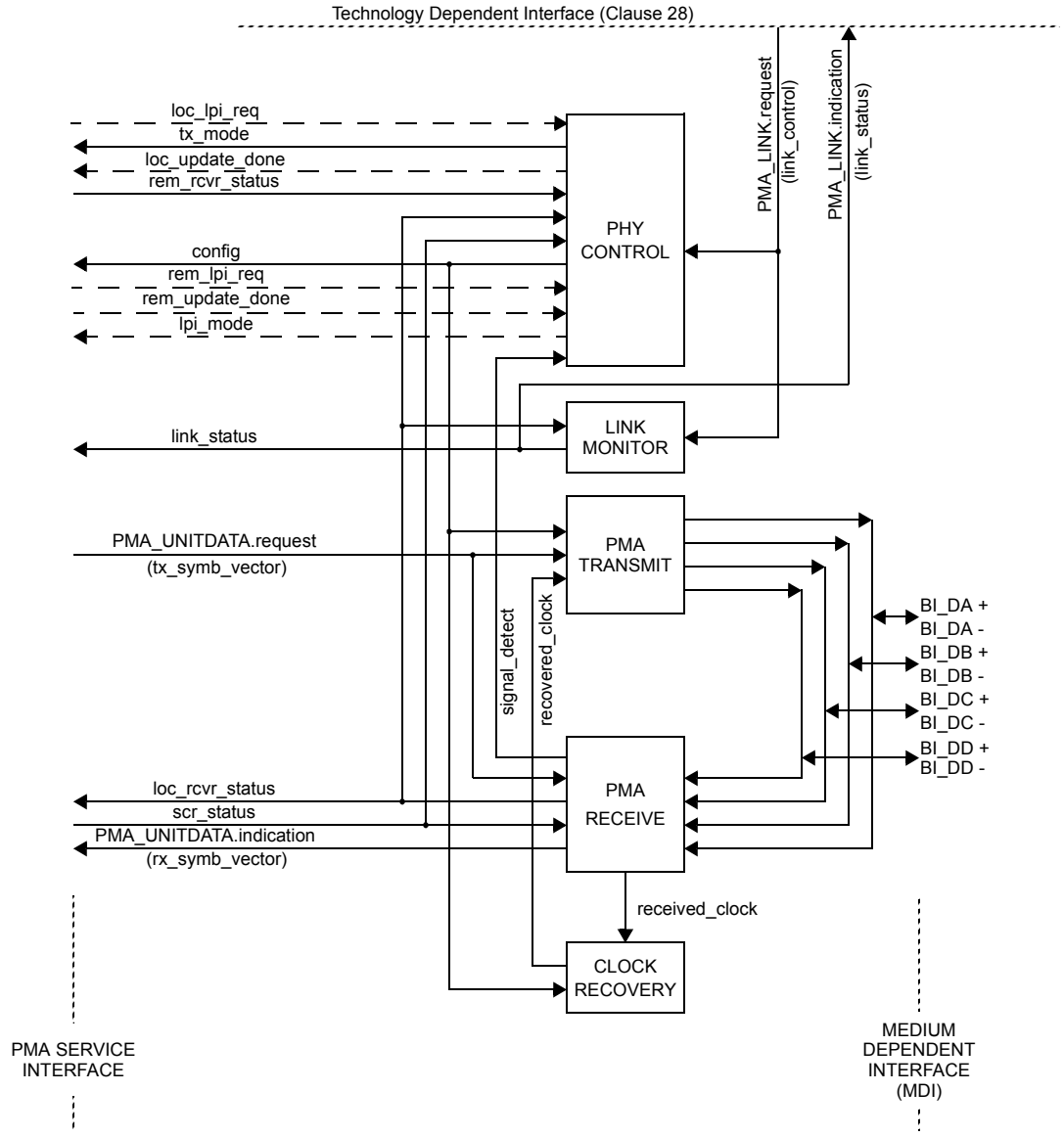


Figure 40–10a—PCS Receive state diagram, part a

40.4 Physical Medium Attachment (PMA) sublayer

40.4.2 PMA functions

Replace the existing PMA reference diagram (Figure 40-13) with the new PMA reference diagram Figure 40–13:



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 40–13—PMA reference diagram

40.4.2.4 PHY Control function

Change the last sentence in the first paragraph of 40.4.2.4 as shown below:

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 40–15a and Figure 40–15b~~Figure 40-15~~.

Insert the following text before the last paragraph of 40.4.2.4 as shown below:

When the PHY supports the optional EEE capability, PHY Control will transition to the LPI mode in response to concurrent requests for LPI mode from the local PHY (loc_lpi_req = TRUE) and remote PHY (rem_lpi_req = TRUE).

Upon activation of the LPI mode, the PHY Control asserts tx_mode = SEND_I for a period of time defined by lpi_update_timer which allows the remote PHY to prepare for cessation of transmission. When lpi_update_timer expires, PHY Control transitions to the POST_UPDATE state, signals to the remote PHY that is has completed the update by setting loc_update_done = TRUE, and starts the lpi_postupdate_timer. When lpi_postupdate_timer expires, PHY Control transitions to the WAIT_QUIET state. If there is a request to wake (loc_lpi_req = FALSE or rem_lpi_req = FALSE) while in the POST_UPDATE state, PHY Control will wait for confirmation that the remote PHY has completed the update (rem_update_done = TRUE) and is prepared for cessation of transmission before proceeding to the WAIT_QUIET state.

Upon entry into the WAIT_QUIET state, PHY Control asserts tx_mode = SEND_Z and transmission ceases. During the WAIT_QUIET and QUIET states, the PHY may deactivate transmit and receive functions in order to conserve energy. However, in the WAIT_QUIET state, the PHY shall be capable of correctly decoding rem_lpi_req. The PHY will remain in the QUIET state no longer than the time implied by lpi_quiet_timer.

When lpi_quiet_timer expires, the PHY initiates a wake sequence. The wake sequence begins with a transition to the WAKE state where the PHY will transmit (tx_mode = SEND_I) for the period lpi_waketx_timer and simultaneously start a parallel timer, lpi_wakemz_timer. Since it is likely that transmit circuits were deactivated while in the QUIET state, this transmission is not expected to be compliant 1000BASE-T signaling, but rather of sufficient quality and duration to be detected by the remote PHY receiver and initiate the wake sequence in the remote PHY.

Upon expiration of lpi_waketx_timer, the PHY will enter the WAKE_SILENT state and cease transmission (tx_mode = SEND_Z). The PHY will remain in the WAKE_SILENT state until lpi_wakemz_timer has expired, at which point it is assumed that the transmitter circuits have stabilized and compliant 1000BASE-T signaling can be transmitted. At this point the MASTER transitions to the WAKE_TRAINING state and transmits to the SLAVE PHY.

The remaining wake sequence is essentially an accelerated training mode sequence leading to entry into the UPDATE state.

Once scrambler synchronization is achieved, the incoming value of rem_lpi_req can be determined. If the LPI mode is no longer requested by either the local or remote PHY, then both PHYs return to the SEND IDLE OR DATA state and the normal mode of operation (tx_mode = SEND_N). If both PHYs continue to request the LPI mode, then both PHYs remain in the UPDATE state and continue to transmit for a time defined by lpi_update_timer. This time is intended to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If lpi_update_timer expires and both PHYs continue to request the LPI mode, then the PHY transitions to the POST_UPDATE state.

40.4.5 State variables

40.4.5.1 State diagram variables

Change definition of scr_status as shown:

scr_status
The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized. Note that when the PHY supports the optional EEE capability and signal_detect is FALSE, scr_status is set to NOT_OK.

Insert text following the existing list of variables as shown below:

The following state variables are only required for the optional EEE capability.

loc_lpi_req
The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the LPI mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. In the absence of the optional EEE capability, the PHY operates as if the value of this variable is FALSE.
Values: TRUE: "Assert LPI" is present at the GMII.
FALSE: "Assert LPI" is not present at the GMII.

loc_udpate_done
The loc_update_done variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has completed the update of its receiver state. It is passed to the PCS Transmit function via the PMA_UPDATE.indication primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.
Values: TRUE: The PHY has completed the current update.
FALSE: The PHY is ready for the next update or the current update is still in progress.

lpi_mode
The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered the LPI mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is OFF.
Values: ON: The PHY is operating in LPI mode.
OFF: The PHY is in normal operation.

rem_lpi_req
The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into LPI mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. In the absence of the optional EEE capability, the PHY operates as if the value of this variable is FALSE.
Values: TRUE: LPI is encoded in the received symbols.
FALSE: LPI is not encoded in the received symbols.

rem_update_done
The rem_update_done variable is generated by the PCS Receive function and indicates whether or not the remote PHY has completed the update of its receiver state. It is passed to the PMA PHY Control function via the PMA_REMUPDATE.request primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.
Values: TRUE: The remote PHY has completed the current update.

FALSE: The remote PHY is ready for the next update or the current update is still in progress.

signal_detect

The signal_detect variable is set by the PMA Receive function and indicates the presence of a signal at the MDI, as defined in 40.6.1.3.5.

Values: TRUE: There is a signal present at the MDI.
FALSE: There is no signal present at the MDI.

40.4.5.2 Timers

Insert text following the existing list of timers as shown below:

The following timers are only required for the optional EEE capability.

lpi_link_fail_timer

This timer defines the maximum time the PHY allows between entry into the WAKE state and subsequent entry into the UPDATE or SEND IDLE OR DATA states before forcing the link to restart.

Values: The condition lpi_link_fail_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 90 μs and 110 μs.

lpi_postupdate_timer

This timer defines the maximum time the PHY dwells in the POST_UPDATE state before proceeding to the WAIT_QUIET state.

Values: The condition lpi_postupdate_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 2.0 μs and 3.2 μs.

lpi_quiet_timer

This timer defines the maximum time the PHY remains quiet before initiating transmission to refresh the remote PHY.

Values: The condition lpi_quiet_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 20 ms and 24 ms.

lpi_waitwq_timer

This timer defines the maximum time the PHY dwells in the WAIT_QUIET state before forcing the link to restart.

Values: The condition lpi_waitwq_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 10 μs and 12 μs.

lpi_wake_timer

This timer defines the expected time for the PHY to transition from the LPI mode to normal operation.

Values: The condition lpi_wake_timer_done becomes true upon timer expiration. For each transition of lpi_wake_timer_done from false to true, the wake error counter (see 40.5.1.1) shall be incremented.
Duration: This timer shall have a period that does not exceed 16.5 μs.

lpi_waketx_timer

This timer defines the time the PHY transmits to ensure detection by the remote PHY receiver and trigger an exit from the low power state.

Values: The condition lpi_waketx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 1.2 µs and 1.4 µs.

lpi_wakemz_timer

This timer defines the time allowed for the PHY transmitter to achieve compliant operation following activation.

Values: The condition lpi_wakemz_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 4.25 µs and 5.00 µs.

lpi_update_timer

This timer defines the time the PHY transmits to facilitate a refresh of the remote PHY receiver.

Values: The condition lpi_update_timer_done becomes true upon timer expiration.
Duration: For a PHY configured as the MASTER, this timer shall have a period between 0.23 ms and 0.25 ms. For a PHY configured as the SLAVE, this timer shall have a period between 0.18 ms and 0.20 ms.

40.4.6 State Diagrams

40.4.6.1 PHY Control state diagram

Replace existing PHY Control state diagram (Figure 40-15) with new PHY Control state diagram, part a labeled Figure 40–15a

Also insert new PHY control state diagram (Phy Control state diagram, part b labeled Figure 40–15b) after Phy Control state diagram part a.

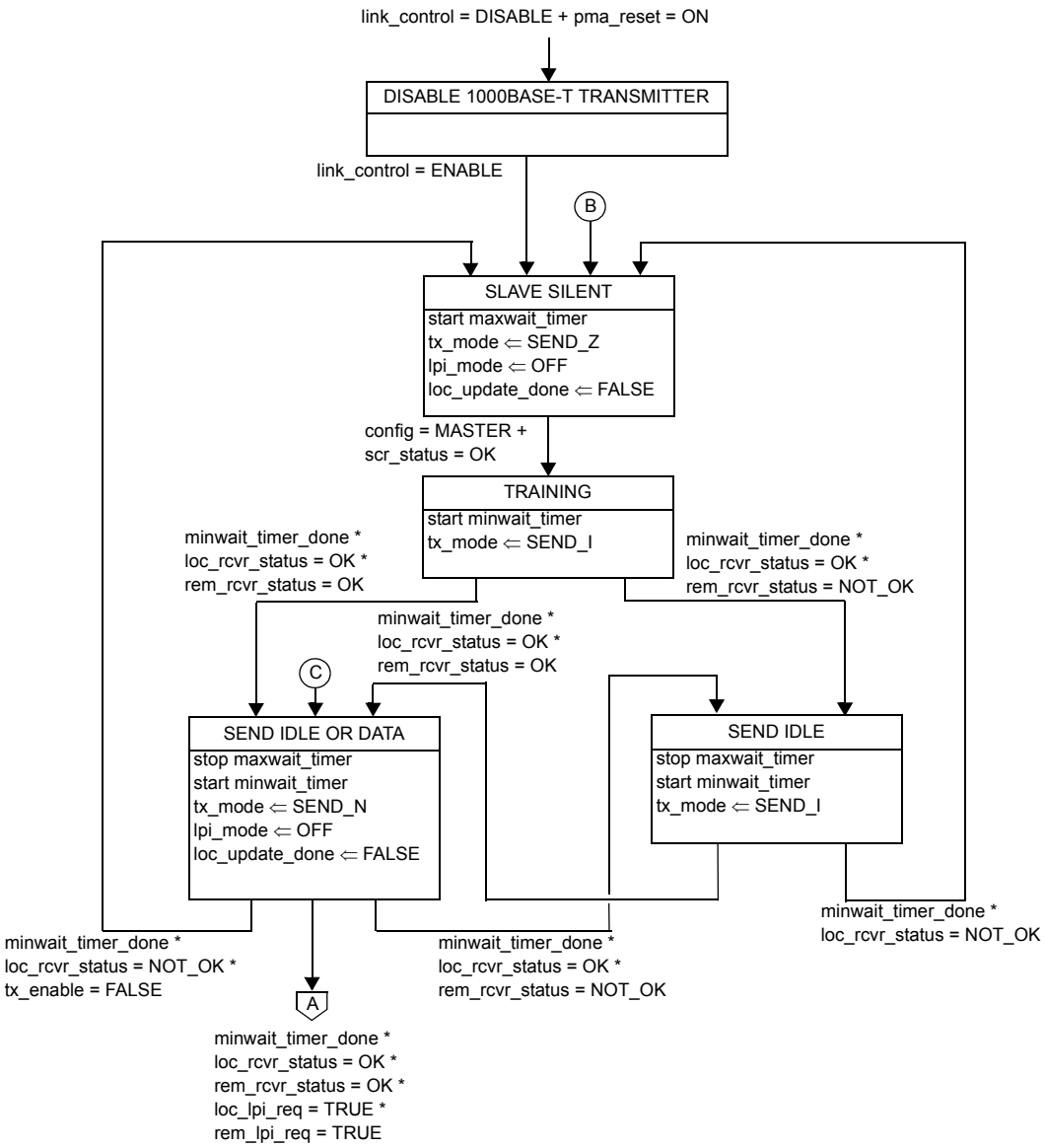


Figure 40–15a—PHY Control state diagram, part a

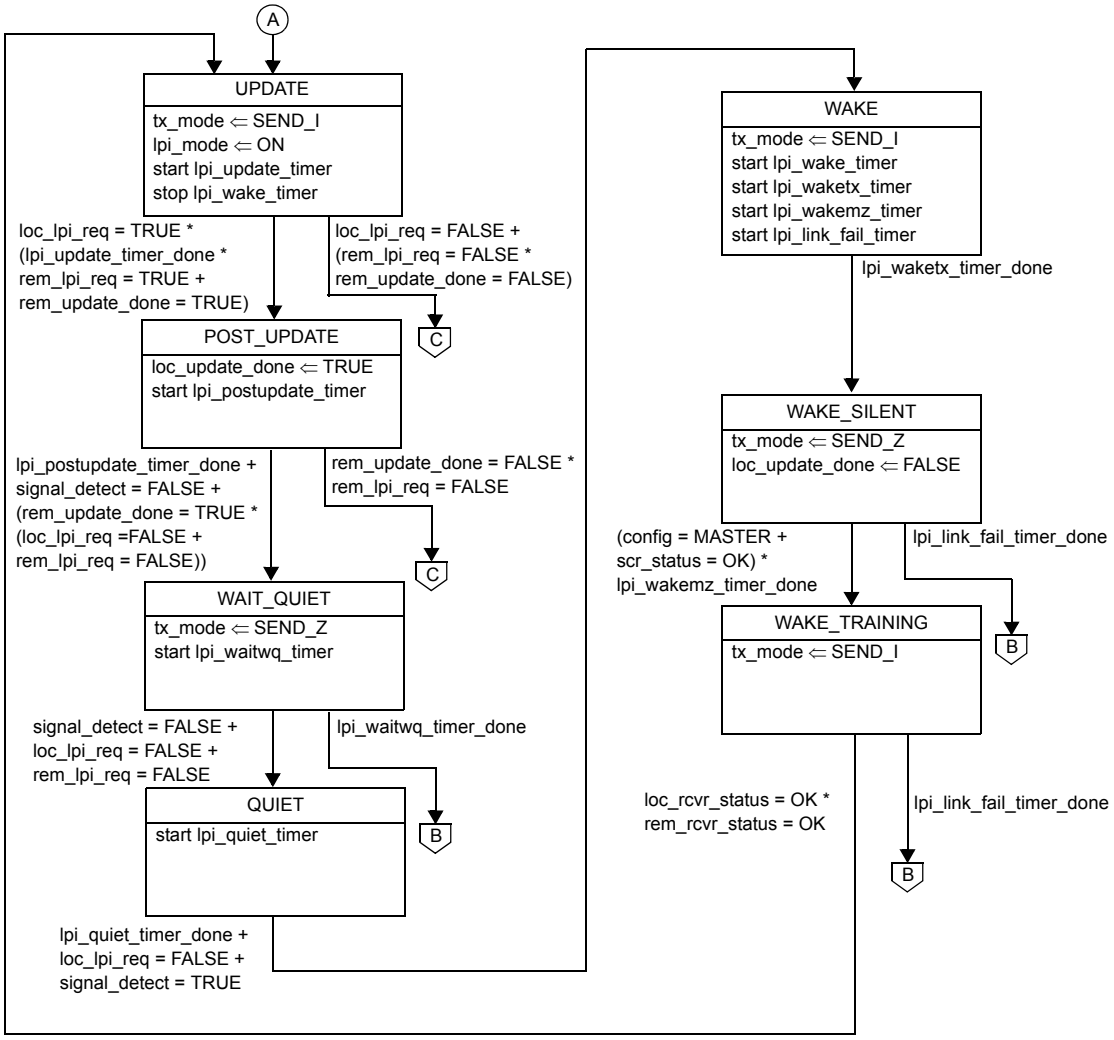
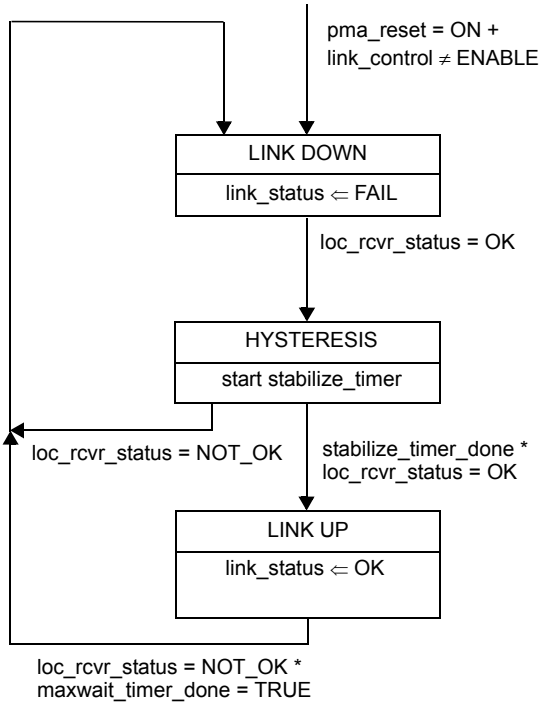


Figure 40–15b—PHY Control state diagram, part b (optional)

40.4.6.2 Link Monitor state diagram

Change Figure reference in NOTE 1 of the Link Monitor state diagram to point to new Phy Control state diagram part a (*Figure 40–15a****):***



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 40–15a).
NOTE 2—The variables link_control and link_status are designated as link_control_(1GigT) and link_status_(1GigT), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 40–16—Link Monitor state diagram

40.5 Management interface

40.5.1 Support for Auto-Negotiation

Insert the following below bullet item b):

c) To negotiate EEE capabilities as specified in 28C.12.

40.5.1.1 1000BASE-T use of registers during Auto-Negotiation

Insert rows in Table 40–3 following Register 15, "Extended status register," and note b as shown:

Table 40–3—1000BASE-T Registers

Register	Bit	Name	Description	Type[a]
3.0[b]	3.0.10	Clock stop enable	Defined in 45.2.3.1.3a. When the PHY supports the optional EEE capability, it may stop the derived GMII receive clock while it is signaling LPI in the receive direction. If this bit is set to 1 then the PHY may stop the receive GMII clock while it is signaling LPI otherwise it keeps the clock active.	R/W
3.1	3.1.11	Transmit LPI received	Defined in 45.2.3.2.1a.	RO/LH
3.1	3.1.10	Receive LPI received	Defined in 45.2.3.2.1b.	RO/LH
3.1	3.1.9	Transmit LPI indication	Defined in 45.2.3.2.1c.	RO
3.1	3.1.8	Receive LPI indication	Defined in 45.2.3.2.1d.	RO
3.1	3.1.6	Clock stop capable	Defined in 45.2.3.2.2a. When the PHY supports the optional EEE capability, this bit may be set to 1 to allow the MAC to stop the GMII clock while it is signaling LPI in the transmit direction. If this bit is 0, then the MAC keeps the clock active.	RO
3.20	3.20.2	1000BASE-T EEE supported	If the local device supports the optional EEE capability for 1000BASE-T, this bit is set to 1.	RO
3.22	3.22.15:0	EEE wake error counter	This counter is incremented for each transition of lpi_wake_timer_done from FALSE to TRUE (see 40.4.5.2).	RO, NR
7.60	7.60.2	1000BASE-T EEE advertisement	If the local device supports the optional EEE capability for 1000BASE-T and EEE is desired, this bit is set to 1	R/W
7.61	7.61.2	LP 1000BASE-T EEE advertisement	If the link partner supports the optional EEE capability for 1000BASE-T and EEE is desired, this bit is set to 1	RO

[b] This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

40.5.1.2 1000BASE-T Auto-Negotiation page use

Insert the paragraph as shown following the last paragraph of 40.5.1.2:

When the PHY supports the optional EEE capability, a 1000BASE-T PHY shall exchange an additional formatted next page and unformatted next page in sequence, without interruption, as specified in Table 40–4.

Insert rows in Table 40–4 following "PAGE 2 (Unformatted next page)" and note a as shown:

Table 40–4—1000BASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
PAGE 3 (Message page)		
M10:M0	10	
PAGE 4 (Unformatted next page)		
U10:U3	As specified in 45.2.7.13a.	
U2	1000BASE-T EEE (1 = EEE is supported for 1000BASE-T, 0 = EEE is not supported for 1000BASE-T)	Management register 7.60.2[a]
U1:U0	As specified in 45.2.7.13a.	

[a]This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

40.6 PMA electrical specifications

40.6.1.2.5 Transmitter timing jitter

Insert paragraph as shown following the last paragraph of 40.6.1.2.5:

When the PHY supports the optional EEE capability, the unfiltered jitter requirements shall also be satisfied during the LPI mode, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement. The PHY may turn off TX_TCLK during these states. For a MASTER PHY operating in the LPI mode, the unjittered reference shall be continuous.

Insert the following subclause after 40.6.1.2.6:

40.6.1.2.7 Transmitter operation following a transition from the QUIET to the WAKE state

When the PHY supports the optional EEE capability, it transmits Idle symbols while in the WAKE state (see the PHY Control state diagram, Figure 40–15b). This signal may be transmitted during reactivation of the PHY analog front-end and is not guaranteed or intended to be compliant.

The transmit levels of the Idle symbols transmitted during the WAKE state shall exceed 65% of the transmit levels of compliant Idle symbols for a period of at least 500 ns.

The PHY shall achieve compliant operation upon entry to the WAKE_TRAINING state (see the PHY Control state diagram, Figure 40–15b).

Insert the following subclause after 40.6.1.3.4:

40.6.1.3.5 Signal_detect

When the PHY supports the optional EEE capability, the PMA Receive function shall convey an indicator of signal presence, referred to as signal_detect, to the PMA PHY Control function. The value of signal_detect shall be set to TRUE within 0.5 μs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7. The value of signal_detect shall be set to FALSE within 0.5 μs of the receipt of a continuous sequence of zeros.

40.12 Protocol implementation conformance statement (PICS) proforma for Clause 40—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 1000BASE-T[1]

40.12.2 Major capabilities/options

Insert *EEE option into the table as follows;

Item	Feature	Subclause	Status	Support	Value/Comment
*EEE	EEE	40.1.3	O	Yes [ ] No [ ]	

40.12.4 Physical Coding Sublayer (PCS)

Insert PCT18 and PCT19 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PCT18	The PCS shall	40.3.1.6	EEE:M	Yes [ ]	Conform to the Local LPI Request state diagram as depicted in Figure 40–8a including compliance with the associated state variables specified in 40.3.3.
PCT19	In the absence of the optional EEE capability, the PHY shall	40.3.3.1	!EEE:M	Yes [ ]	Operate as if the value of loc_lpi_req is FALSE.

40.12.4.1 PCS receive functions

Insert PCR5 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PCR5	In the absence of the optional EEE capability, the PHY shall	40.3.3.1	!EEE:M	Yes [ ]	Operate as if the value of rem_lpi_req is FALSE.

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

40.12.5 Physical Medium Attachment (PMA)

Insert PMF24 through PMF37 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PMF24	PHY Control shall	40.4.2.4	EEE:M	Yes [ ]	Comply with the state diagram description given in Figure 40–15a and Figure 40–15b.
PMF25	In the WAIT_QUIET state, the PHY shall	40.4.2.4	EEE:M	Yes [ ]	Be capable of correctly decoding rem_lpi_req.
PMF26	In the absence of the optional EEE capability, the PHY shall	40.4.5.1	EEE:M	Yes [ ]	Operate as if the value of loc_update_done is FALSE.
PMF27	In the absence of the optional EEE capability, the PHY shall	40.4.5.1	EEE:M	Yes [ ]	Operate as if the value of lpi_mode is OFF.
PMF28	In the absence of the optional EEE capability, the PHY shall	40.4.5.1	EEE:M	Yes [ ]	Operate as if the value of rem_lpi_req is FALSE.
PMF29	lpi_link_fail_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 90 μs and 110 μs.
PMF30	lpi_postupdate_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 2.0 μs and 3.2 μs.
PMF31	lpi_quiet_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 20 ms and 24 ms.
PMF32	lpi_waitwq_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 10 μs and 12 μs.
PMF33	For each transition of lpi_wake_timer_done from false to true, the wake error counter shall	40.4.5.2	EEE:M	Yes [ ]	Be incremented.
PMF34	lpi_wake_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period that does not exceed 16.5 μs.
PMF35	lpi_waketx_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 1.2_μs and 1.4 μs.
PMF36	lpi_wakemz_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 4.25 μs and 5.00 μs.
PMF37	lpi_update_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 0.23 ms and 0.25 ms for a PHY configured as the MASTER and a period between 0.18 ms and 0.20 ms for a PHY configured as the SLAVE.

40.12.6 PMA Electrical Specifications

Insert PME71 through PME77 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PME71	The unfiltered jitter requirements shall	40.6	EEE:M	Yes [ ]	Be satisfied during the LPI mode, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement.
PME72	For a MASTER PHY operating in the LPI mode, the unjittered reference shall	40.6	EEE:M	Yes [ ]	Be continuous.
PME73	The transmit levels of the Idle symbols transmitted during the WAKE state shall	40.6.1.2.7	EEE:M	Yes [ ]	Exceed 65% of the transmit levels of compliant Idle symbols for a period of at least 500 ns.
PME74	The PHY shall	40.6.1.2.7	EEE:M	Yes [ ]	Achieve compliant operation upon entry to the WAKE_TRAINING state (see the PHY Control state diagram, Figure 40–15b).
PME75	PMA Receive function shall	40.6.1.3.5	EEE:M	Yes [ ]	Convey an indicator of signal presence, referred to as signal_detect, to the PMA PHY Control function.
PME76	The value of signal_detect shall	40.6.1.3.5	EEE:M	Yes [ ]	Be set to TRUE within 0.5 μs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7.
PME77	The value of signal_detect shall	40.6.1.3.5	EEE:M	Yes [ ]	Be set to FALSE within 0.5 μs of the receipt of a continuous sequence of zeros.

40.12.6.1 1000BASE-T Specific Auto-Negotiation Requirements

Insert AN15 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
AN15	When EEE is supported, a 1000BASE-T PHY shall	40.5.1.2	EEE:M	Yes [ ]	Exchange an additional formatted next page and unformatted next page in sequence, without interruption, as specified in Table 40–4.

45. Management Data Input/Output (MDIO) Interface

45.2.1 PMA/PMD registers

Change Table 45-3 to add the following row and change the reserved row accordingly:

Table 45–3—PMA/PMD registers

Register address	Register name
1.147	10GBASE-T fast retrain status and control register
1.1478 through 1.149	Reserved

Insert 45.2.1.76a after 45.2.1.76 (as renumbered by IEEE Std 802.3av^{TM}-2009):

45.2.1.76a 10GBASE-T fast retrain status and control register (Register 1.147)

Table 45–53a—10GBASE-T fast retrain status and control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.147.15:11	LP fast retrain count	Counts the number of fast retrains requested by the link partner	RO/NR
1.147.10:6	LD fast retrain count	Counts the number of fast retrains requested by the local device	RO/NR
1.147.5	Reserved	Ignore on read	RO
1.147.4	Fast retrain ability	1 = Fast retrain capability is supported 0 = Fast retrain capability is not supported	RO
1.147.3	Fast retrain negotiated	1 = Fast retrain capability was negotiated 0 = Fast retrain capability was not negotiated	RO
1.147.2:1	Fast retrain signal type	11 = Reserved 10 = PHY signals Link Interruption during fast retrain 01 = PHY signals Local Fault during fast retrain 00 = PHY signals IDLE during fast retrain	R/W
1.147.0	Fast retrain enable	1 = Fast retrain capability is enabled 0 = Fast retrain capability is disabled	R/W

[a] RO = Read only, R/W = Read/Write, NR = Non Roll-over

45.2.1.76a.1 LP fast retrain count (1.147.15:11)

These bits map to fr_rx_counter as defined in 55.4.5.1. The counter is a 5-bit count of the number of 10GBASE-T fast retrains requested by the link partner. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.76a.2 LD fast retrain count (1.147.10:6)

These bits map to fr_tx_counter as defined in 55.4.5.1. The counter is a 5-bit count of the number of 10GBASE-T fast retrains requested by the local device. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.76a.3 Fast retrain ability (1.147.4)

When read as a one, bit 1.147.4 indicates that the PHY supports fast retrain, as defined in 55.4.2.5.15. When read as a zero, bit 1.147.4 indicates that the PHY does not support fast retrain.

45.2.1.76a.4 Fast retrain negotiated (1.147.3)

When read as a one, bit 1.147.3 indicates that the PHY negotiated fast retrain, as defined in 55.4.2.5.15 during the most recent autonegotiation. When read as a zero, bit 1.147.3 indicates that the PHY did not negotiate fast retrain. See 45.2.7.10.5a.

45.2.1.76a.5 Fast retrain signal type (1.147.2:1)

For PHYs that support fast retrain, these bits map to fr_sigtype as defined in 55.3.5.2.2. When Fast retrain signal type is set to 00, the PMA sends IDLE characters on the receive path during fast retrain. When Fast retrain signal type is set to 01, the PMA sends Local Fault on the receive path during fast retrain. When Fast retrain signal type is set to 10, the PMA sends Link Interruption on the receive path during fast retrain.

45.2.1.76a.6 Fast retrain enable (1.147.0)

For PHYs that support fast retrain, this bit controls fr_enable as defined in 55.4.5.1. When PMA reset is executed, this bit is set to one.

Note: Setting this bit to zero while a link is up will cause the PHY to stop supporting fast retrain and the link will drop if the link partner initiates a fast retrain.

45.2.3 PCS registers

Change Table 45-83 (as renumbered by IEEE Std 802.3av^{TM}-2009) to add the following rows and change the reserved rows accordingly:

Table 45–83—PCS registers

Register address	Register name	Clause
3.16 through 3.~~23~~19	Reserved	
3.20	EEE capability register	45.2.3.8a
3.21	Reserved	
3.22	EEE wake error counter	45.2.3.8b

45.2.3.1 PCS control 1 register (Register 3.0)

Change Table 45-84 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new row and change as follows:

Table 45–84—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.10	Clock stop enable	1 = The PHY may stop the clock during LPI 0 = Clock not stoppable	R/W
3.0.~~10~~9:7	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self-clearing

Insert 45.2.3.1.3a after 45.2.3.1.3 as follows:

45.2.3.1.3a Clock stop enable (3.0.10)

If bit 3.0.10 is set to 1 then the PHY may stop the receive xMII clock while it is signaling LPI otherwise it shall keep the clock active. If the PHY does not support EEE capability or is not able to stop the receive clock then this bit has no effect (see 22.2.2.2, 35.2.2.8a, and 46.3.2.4).

45.2.3.2 PCS status 1 register (Register 3.1)

Change Table 45-85 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new rows and change as follows:.

Table 45–85—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:~~8~~12	Reserved	Ignore when read	RO
3.1.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.1.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.1.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.1.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.1.6	Clock stop capable	1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO
3.1.~~6~~5:3	Reserved	Ignore when read	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

Insert 45.2.3.2.a, b, c and d, before 45.2.3.2.1 and 45.2.3.2.2a before 45.2.3.2.3 as follows:

45.2.3.2.a Transmit LPI received (3.1.11)

When read as a one, bit 3.1.11 indicates that the transmit PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.1.11 indicates that the PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.2.b Receive LPI received (3.1.10)

When read as a one, bit 3.1.10 indicates that the receive PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.1.10 indicates that the PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.2.c Transmit LPI indication (3.1.9)

When read as a one, bit 3.1.9 indicates that the transmit PCS is currently receiving LPI signals. When read as a zero, bit 3.1.9 indicates that the PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.2.d Receive LPI indication (3.1.8)

When read as a one, bit 3.1.8 indicates that the receive PCS is currently receiving LPI signals. When read as a zero, bit 3.1.8 indicates that the PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.2.2a Clock stop capable (3.1.6)

If bit 3.1.6 is set to one then the RS may stop the transmit xMII clock while it is signaling LPI otherwise it shall keep the clock active. If the RS does not support EEE capability or is not able to stop the transmit clock then this bit has no effect (see 22.2.2.5a, 35.2.2.5a, and 46.3.2.4).

Insert 45.2.3.8a and b after 45.2.3.8 as follows:

45.2.3.8a EEE capability (Register 3.20)

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE capability register is shown in Table 45–88a.

Table 45–88a—EEE capability register (Register 3.20) bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15:7	Reserved	Ignore on read	RO
3.20.6	10GBASE-KR EEE	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	RO
3.20.5	10GBASE-KX4 EEE	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	RO
3.20.4	1000BASE-KX EEE	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	RO
3.20.3	10GBASE-T EEE	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	RO
3.20.2	1000BASE-T EEE	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	RO
3.20.1	100BASE-TX EEE	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	RO
3.20.0	Reserved	Ignore on read	RO

[a] RO = Read only

45.2.3.8a.1 10GBASE-KR EEE supported (3.20.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.1, this bit shall be set to one.

45.2.3.8a.2 10GBASE-KX4 EEE supported (3.20.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.2, this bit shall be set to one.

45.2.3.8a.3 1000BASE-KX EEE supported (3.20.4)

If the device supports EEE operation for 1000BASE-KX as defined in 70.1, this bit shall be set to one.

45.2.3.8a.4 10GBASE-T EEE supported (3.20.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3, this bit shall be set to one.

45.2.3.8a.5 1000BASE-T EEE supported (3.20.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.1.3, this bit shall be set to one.

45.2.3.8a.6 100BASE-TX EEE supported (3.20.1)

If the device supports EEE operation for 100BASE-TX as defined in 24.1.1, this bit shall be set to one.

45.2.3.8b EEE wake error counter (Register 3.22)

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and may occur during a refresh or a wakeup as defined by the PHY. This 16 bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PCS reset. This counter shall be held at all ones in the case of overflow.

45.2.4 PHY XS registers

Change Table 45-116 (as renumbered by IEEE Std 802.3av^{TM}-2009) to add the following rows and change the reserved rows accordingly:

Table 45–116—PHY XS registers

Register address	Register name
4.16 through 4.~~23~~19	Reserved
4.20	EEE capability register
4.21	Reserved
4.22	EEE wake error counter

45.2.4.1 PHY XS control 1 register (Register 4.0)

Change Table 45-117 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new row and change as follows:

Table 45–117—PHY XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.0.10	Clock stop enable	1 = The PHY XS may stop the clock during LPI 0 = Clock not stoppable	R/W
4.0.9	XAUI stop enable	1 = The PHY XS may stop XAUI signals during LPI 0 = XAUI not stoppable	R/W
4.0.~~10~~8:7	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self-clearing

Insert 45.2.4.1.3a and b after 45.2.4.1.3 as follows:

45.2.4.1.3a Clock stop enable (4.0.10)

If bit 4.0.10 is set to 1 then the PHY XS may stop the transmit direction xMII clock while it is signaling LPI otherwise it shall keep the clock active. If the PHY XS does not support EEE capability or is not able to stop the transmit clock then this bit has no effect (see 46.3.2.4).

45.2.4.1.3b XAUI stop enable (4.0.9)

If bit 4.0.9 is set to 1 then the PHY XS may stop signaling on the XAUI in the receive direction during LPI otherwise the PHY XS shall keep the XAUI signals active. If the PHY XS does not support EEE capability or is not able to stop the receive path XAUI signals then this bit has no effect.

45.2.4.2 PHY XS status 1 register (Register 4.1)

Change Table 45-118 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new rows and change as follows:.

Insert 45.2.4.2.a, b, c and d, before 45.2.4.2.1 and 45.2.4.2.2a before 45.2.4.2.3 as follows:

45.2.4.2.a Transmit LPI received (4.1.11)

When read as a one, bit 4.1.11 indicates that the transmit PHY XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 4.1.11 indicates that the PHY XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.4.2.b Receive LPI received (4.1.10)

When read as a one, bit 4.1.10 indicates that the receive PHY XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 4.1.10 indicates that the PHY XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

Table 45–118—PHY XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.1.15:~~8~~12	Reserved	Ignore when read	RO
4.1.11	Tx LPI received	1 = Tx PHY XS has received LPI 0 = LPI not received	RO/LH
4.1.10	Rx LPI received	1 = Rx PHY XS has received LPI 0 = LPI not received	RO/LH
4.1.9	Tx LPI indication	1 = Tx PHY XS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
4.1.8	Rx LPI indication	1 = Rx PHY XS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
4.1.6	Clock stop capable	1 = The attached PHY may stop the clock during LPI 0 = Clock not stoppable	RO
4.1.~~6~~5:3	Reserved	Ignore when read	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.4.2.c Transmit LPI indication (4.1.9)

When read as a one, bit 4.1.9 indicates that the transmit PHY XS is currently receiving LPI signals. When read as a zero, bit 4.1.9 indicates that the PHY XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.4.2.d Receive LPI indication (4.1.8)

When read as a one, bit 4.1.8 indicates that the receive PHY XS is currently receiving LPI signals. When read as a zero, bit 4.1.8 indicates that the PHY XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.4.2.2a Clock stop capable (4.1.6)

If bit 4.1.6 is set to one then the PHY XS is indicating that the attached PHY is permitted to stop the receive direction xMII clock while it is signaling LPI. If the bit is set to zero then the PHY XS is indicating that the attached PHY is not permitted to stop the receive xMII clock while it is signaling LPI. If the attached PHY does not support EEE capability or is not able to stop the receive direction xMII clock then this bit has no effect (see 46.3.2.4).

Insert 45.2.4.8a and b after 45.2.4.8 as follows:

45.2.4.8a EEE capability (Register 4.20)

This register is used to indicate the capability of the PHY XS to support EEE functions. The assignment of bits in the EEE capability register is shown in Table 45–122a.

Table 45–122a—EEE capability register (Register 4.20) bit definitions

Bit(s)	Name	Description	R/W[a]
4.20.15:5	Reserved	Ignore on read	RO
4.20.4	PHY XS EEE	1 = EEE is supported for PHY XS 0 = EEE is not supported for PHY XS	RO
4.20.3:1	Reserved	Ignore on read	RO
4.20.0	XAUI stop capable	1 = The DTE XS may stop XAUI signals during LPI 0 = XAUI signals not stoppable	RO

[a] RO = Read only

45.2.4.8a.1 PHY XS EEE supported (4.20.4)

If the device supports EEE operation for PHY XS as defined in 48.2, this bit shall be set to one.

45.2.4.8a.2 XAUI stop capable (4.20.0)

If bit 4.20.0 is set to one then the PHY XS is indicating that the attached DTE XS is permitted to stop transmitting XAUI signals during LPI. If the bit is set to zero then the PHY XS is indicating that the attached DTE XS is not permitted to stop transmitting XAUI signals during LPI. If the DTE XS does not support EEE capability or is not able to stop the the transmit direction XAUI then this bit has no effect.

45.2.4.8b EEE wake error counter (Register 4.22)

This register is used by PHY XS that support EEE to count wake time faults where the PHY XS fails to complete its normal wake sequence after a period of quiescence for XAUI transmit signals. The fault event to be counted may occur during a refresh or a wakeup. This 16 bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PHY XS reset. This counter shall be held at all ones in the case of overflow.

45.2.5 DTE XS registers

Change Table 45-123 (as renumbered by IEEE Std 802.3av™-2009) to add the following rows and change the reserved rows accordingly:

Table 45–123—DTE XS registers

Register address	Register name
5.16 through 5.~~23~~19	Reserved
5.20	EEE capability register
5.21	Reserved
5.22	EEE wake error counter

45.2.5.1 DTE XS control 1 register (Register 5.0)

Change Table 45-124 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new row and change as follows:

Table 45–124—DTE XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.0.10	Clock stop enable	1 = The DTE XS may stop the clock during LPI 0 = Clock not stoppable	R/W
5.0.9	XAUI stop enable	1 = The DTE XS may stop XAUI signals during LPI 0 = XAUI not stoppable	R/W
5.0.~~10~~8:7	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self-clearing

Insert 45.2.5.1.3a and b after 45.2.5.1.3 as follows:

45.2.5.1.3a Clock stop enable (5.0.10)

If bit 5.0.10 is set to 1 then the DTE XS may stop the receive xMII clock while it is signaling LPI otherwise it shall keep the clock active. If the DTE XS does not support EEE capability or is not able to stop the receive clock then this bit has no effect (see 46.3.2.4).

45.2.5.1.3b XAUI stop enable (5.0.9)

If bit 5.0.9 is set to 1 then the DTE XS may stop signaling on the XAUI in the transmit direction during LPI otherwise the DTE XS shall keep the XAUI signals active. If the DTE XS does not support EEE capability or is not able to stop the transmit path XAUI signals then this bit has no effect.

45.2.5.2 DTE XS status 1 register (Register 5.1)

Change Table 45-125 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new rows and change as follows:.

Insert 45.2.5.2.a, b, c and d, before 45.2.5.2.1 and 45.2.5.2.2a before 45.2.5.2.3 as follows:

45.2.5.2.a Transmit LPI received (5.1.11)

When read as a one, bit 5.1.11 indicates that the transmit DTE XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 5.1.11 indicates that the DTE XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.5.2.b Receive LPI received (5.1.10)

When read as a one, bit 5.1.10 indicates that the receive DTE XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 5.1.10 indicates that the DTE XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

Table 45–125—DTE XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.1.15:~~8~~12	Reserved	Ignore when read	RO
5.1.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
5.1.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
5.1.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
5.1.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
5.1.6	Clock stop capable	1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO
5.1.~~6~~5:3	Reserved	Ignore when read	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.5.2.c Transmit LPI indication (5.1.9)

When read as a one, bit 5.1.9 indicates that the transmit DTE XS is currently receiving LPI signals. When read as a zero, bit 5.1.9 indicates that the DTE XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.5.2.d Receive LPI indication (5.1.8)

When read as a one, bit 5.1.8 indicates that the receive DTE XS is currently receiving LPI signals. When read as a zero, bit 5.1.8 indicates that the DTE XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.5.2.2a Clock stop capable (5.1.6)

If bit 5.1.6 is set to one then the DTE XS is indicating that the attached RS is permitted to stop the transmit xMII clock while it is signaling LPI. If the bit is set to zero then the DTE XS is indicating that the attached RS is not permitted to stop the transmit xMII clock while it is signaling LPI. If the RS does not support EEE capability or is not able to stop the transmit direction xMII clock then this bit has no effect (see 46.3.2.4).

Insert 45.2.5.8a and b after 45.2.5.8 as follows:

45.2.5.8a EEE capability (Register 5.20)

This register is used to indicate the capability of the DTE XS to support EEE functions. The assignment of bits in the EEE capability register is shown in Table 45–122a.

Table 45–122a—EEE capability register (Register 5.20) bit definitions

Bit(s)	Name	Description	R/W[a]
5.20.15:5	Reserved	Ignore on read	RO
5.20.4	DTE XS EEE	1 = EEE is supported for DTE XS 0 = EEE is not supported for DTE XS	RO
5.20.3:1	Reserved	Ignore on read	RO
5.20.0	XAUI stop capable	1 = The PHY XS may stop XAUI signals during LPI 0 = XAUI signals not stoppable	RO

[a] RO = Read only

45.2.5.8a.1 PHY XS EEE supported (5.20.4)

If the device supports EEE operation for DTE XS as defined in 48.2, this bit shall be set to one.

45.2.5.8a.2 XAUI stop capable (5.20.0)

If bit 5.20.0 is set to one then the DTE XS is indicating that the attached PHY XS is permitted to stop signalling the XAUI in the receive direction during LPI. If the bit is set to zero then the DTE XS is indicating that the attached PHY XS is not permitted to stop signalling the XAUI in the receive direction during LPI. If the PHY XS does not support EEE capability or is not able to stop the receive direction XAUI then this bit has no effect.

45.2.5.8b EEE wake error counter (Register 5.22)

This register is used by DTE XS that support EEE to count wake time faults where the DTE XS fails to complete its normal wake sequence after a period of quiescence for XAUI receive signals. The fault event to be counted may occur during a refresh or a wakeup. This 16 bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the DTE XS reset. This counter shall be held at all ones in the case of overflow.

45.2.7 Auto-Negotiation registers

Change Table 45-141 (as renumbered by IEEE Std 802.3av^{TM}-2009) insert new rows and change as follows:

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Table 45–141— Auto-Negotiation MMD registers

Register address	Register name
~~7.49 through 7.32 767~~	~~Reserved~~
7.49 through 7.59	Reserved
7.60	EEE advertisement
7.61	EEE LP ability
7.62 through 7.32 767	Reserved

45.2.7.10 10GBASE-T AN control register (Register 7.32)

Change the reserved row of Table 45-148 (as renumbered by IEEE Std 802.3av^{TM}-2009) as follows:

Table 45–148—10GBASE-T AN control register

Bit(s)	Name	Description	R/W[a]
~~7.32.1~~	~~Reserved~~	~~Value always 0, writes ignored~~	~~RO~~
7.32.1	Fast retrain ability	1 = Advertise PHY as 10GBASE-T fast retrain capable 0 = Do not advertise PHY as 10GBASE-T fast retrain capable	R/W

[a] R/W = Read/Write, R/O = Read only

Insert 45.2.7.10.5a after 45.2.7.10.5 :

45.2.7.10.5a Fast retrain ability

Bit 7.32.1 is used to select whether or not Auto-Negotiation advertises the ability to support 10GBASE-T fast retrain. If bit 7.32.1 is set to one the PHY shall advertise fast retrain ability. If bit 7.32.1 is set to zero the PHY shall not advertise fast retrain ability.

45.2.7.11 10GBASE-T AN status register (Register 7.33)

Change the reserved row of Table 45-149 (as renumbered by IEEE Std 802.3av^{TM}-2009) as follows:

Table 45–149—10GBASE-T AN status register

Bit(s)	Name	Description	R/W[a]
7.33.8:~~0~~2	Reserved	Value always 0, writes ignored	RO
7.33.1	Fast retrain ability	1 = Link partner is capable of 10GBASE-T fast retrain 0 = Link partner is not capable of 10GBASE-T fast retrain	RO
7.33.0	Reserved	Value always 0, writes ignored	RO

[a] RO = Read only, SC = Self-clearing, LH = Latching high

Insert 45.2.7.11.8 after 45.2.7.11.7 :

45.2.7.11.8 Fast retrain ability

When read as a one, bit 7.33.1 is used to indicate that the link partner has the ability to support the fast retrain capability as specified in 55.4.2.5.15. When read as a zero, bit 7.33.1 indicates that the PHY lacks the ability to support the fast retrain capability.

Insert 45.2.7.13 and 45.2.7.14 after 45.2.7.12 for register definitions:

45.2.7.13 EEE advertisement (Register 7.60)

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code as defined in 28C.12 or sent in the unformatted next page following a EEE technology message code as defined in 73A.4 or sent as part of the 10GBASE-T extended next page as defined in 55.6.1. The assignment of bits in the EEE advertisement register and the correspondence with the bits in the next page messages are shown in Table 45–157a.

Bits 10:0 of register 7.60 map to bits U10 through U0 respectively of the unformatted next page following a EEE technology message code as defined in 28C.12. Bits 15:0 of register 7.60 map to bits U15 through U0 respectively of the unformatted next page following a EEE technology message code as defined in 73A.4. Devices using Clause 28 autonegotiation may ignore bits defined for Clause 73 autonegotiation and devices using Clause 73 autonegotiation may ignore bits defined for Clause 28 autonegotiation.

Table 45–157a—EEE advertisement register (Register 7.60) bit definitions

Bit(s)	Name	Description	Clause reference; next page bit number	R/W[a]
7.60.15:7	Reserved	Ignore on read		RO
7.60.6	10GBASE-KR EEE	1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	73.7.7.1; U6	R/W
7.60.5	10GBASE-KX4 EEE	1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	73.7.7.1; U5	R/W
7.60.4	1000BASE-KX EEE	1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	73.7.7.1; U4	R/W
7.60.3	10GBASE-T EEE	1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	28.2.3.4.1; U3 / 55.6.1; U24	R/W
7.60.2	1000BASE-T EEE	1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	28.2.3.4.1; U2 / 55.6.1; U23	R/W
7.60.1	100BASE-TX EEE	1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	28.2.3.4.1; U1 / 55.6.1; U22	R/W
7.60.0	Reserved	Ignore on read		RO

[a]R/W = Read/Write, RO = Read only

45.2.7.13.1 10GBASE-KR EEE supported (7.60.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.1, and EEE operation is desired, this bit shall be set to one.

45.2.7.13.2 10GBASE-KX4 EEE supported (7.60.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.2, and EEE operation is desired, this bit shall be set to one.

45.2.7.13.3 1000BASE-KX EEE supported (7.60.4)

If the device supports EEE operation for 1000BASE-KX as defined in 70.1, and EEE operation is desired, this bit shall be set to one.

45.2.7.13.4 10GBASE-T EEE supported (7.60.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3, and EEE operation is desired, this bit shall be set to one.

45.2.7.13.5 1000BASE-T EEE supported (7.60.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.2.11, and EEE operation is desired, this bit shall be set to one.

45.2.7.13.6 100BASE-TX EEE supported (7.60.1)

If the device supports EEE operation for 100BASE-TX as defined in 25.4a, and EEE operation is desired, this bit shall be set to one.

45.2.7.14 EEE link partner ability (Register 7.61)

All of the bits in the EEE LP ability register are read-only. A write to the EEE LP ability register shall have no effect. When the AN process has been completed, this register shall reflect the contents of the link part-

ner's EEE advertisement register. The assignment of bits in the EEE link partner ability register and the correspondence with the bits in the next page messages are shown in Table 45–157b.

Table 45–157b—EEE link partner ability (Register 7.61) bit definitions

Bit(s)	Name	Description	Clause reference; next page bit number	R/W[a]
7.61.15:7	Reserved	Ignore on read		RO
7.61.6	10GBASE-KR EEE	1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	73.7.7.1; U6	RO
7.61.5	10GBASE-KX4 EEE	1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for 10GBASE-KX4	73.7.7.1; U5	RO
7.61.4	1000BASE-KX EEE	1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	73.7.7.1; U4	RO
7.61.3	10GBASE-T EEE	1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	28.2.3.4.1; U3 / 55.6.1; U24	RO
7.61.2	1000BASE-T EEE	1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	28.2.3.4.1; U2 / 55.6.1; U23	RO
7.61.1	100BASE-TX EEE	1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	28.2.3.4.1; U1 / 55.6.1; U22	RO
7.61.0	Reserved	Ignore on read		RO

[a]R/W = Read/Write, RO = Read only

The definitions for the contents of the EEE LP ability register are given by the definitions for the contents on the link partner's EEE advertisement register, 7.60 (see 45.2.7.13).

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface[1]

Insert the following row into table 45.5.3.6:

45.5.3.6 PCS options

Item	Feature	Subclause	Value/Comment	Status	Support
*EEE	Implementation of EEE			O	Yes [ ] N/A [ ]

Insert the following rows into table 45.5.3.7:

45.5.3.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM30a	EEE capability indicated for each port type	45.2.3.8a		EEE:M	Yes [ ] N/A [ ]
RM30b	EEE wake error counter behavior as specified	45.2.3.9b		EEE:M	Yes [ ] N/A [ ]

Insert the following row into table 45.5.3.8:

45.5.3.8 Auto-negotiation options

Item	Feature	Subclause	Value/Comment	Status	Support
*EEE	Implementation of EEE			O	Yes [ ] N/A [ ]

Insert the following rows into table 45.5.3.9:

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.3.9 Auto-Negotiation management functions

Item	Feature	Subclause	Value/Comment	Status	Support
AM58	EEE capability in advertisement register for each port type	45.2.7.13		AN:EEE:M	Yes [ ] N/A [ ]
AM59	EEE LP advertisement register reflects link partner's capabilities	45.2.7.14		AN:EEE:M	Yes [ ] N/A [ ]
AM60	Writes to EEE LP advertisement register have no effect	45.2.7.14		AN:EEE:M	Yes [ ] N/A [ ]

46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

Change 46.1.1 for major concepts (Insert item h at he end of the list):

h) The XGMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy Efficient Ethernet (EEE) (see Clause 78).

Change 46.1.7 for LPI function:

46.1.7 Mapping of XGMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the XGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 10 Gb/s; therefore, PLSservice primitives supporting CSMA/CD operation are not mapped through the RS to the XGMII. The mapping is changed if EEE capability is supported (see 78.3). This behavior and restrictions are the same as described in 22.6a, with the details of the signaling described in 46.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e. link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 10 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

Change 46.1.7.3 for carrier indication definition:

46.1.7.3 Mapping of PLS_CARRIER.indication

10 Gb/s operation supports full duplex operation only. The RS never generates this primitive for PHYs that do not support EEE or Link Interruption.

For PHYs that support EEE capability, CARRIER_STATUS is set in response to LPI_REQUEST as shown in Figure 46–10a. For PHYs that support Link Interruption, CARRIER_STATUS may be set in response to link_fault. CARRIER_STATUS is set to CARRIER_ON if LPI_CARRIER_STATUS is TRUE or if link_fault is Link Interruption. CARRIER_STATUS is otherwise set to CARRIER_OFF. The deferral mechanism based upon the Link Interruption signal may be enabled or disabled by management.

Change 46.3 to show LPI signaling:

46.3 XGMII functional specifications

Insert NOTE in 46.3.1.1 for clock definitions:

NOTE—For EEE capability, TX_CLK may be halted according to 46.3.1.5.

Change NOTE in 46.3.2.1 for clock definitions:

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. For EEE capability, RX_CLK may be halted according to 46.3.2.4.

Insert the following at the end of 46.3.1.2:

46.3.1.2 TXC<3:0> (transmit control)

A PHY with EEE capability shall interpret the combination of TXC and TXD as shown in Table 46–3 as an assertion of LPI. Transition into and out of the LPI state is shown in Figure 46–7a.

Insert new row and change Table 46-3 as follows:

Table 46–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
~~1~~	~~00 through 06~~	~~Reserved~~	~~—~~
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to request LPI	No applicable parameter (Normal inter-frame)
NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).			

Insert 46.3.1.5 after 46.3.1.4 for transmit LPI transition:

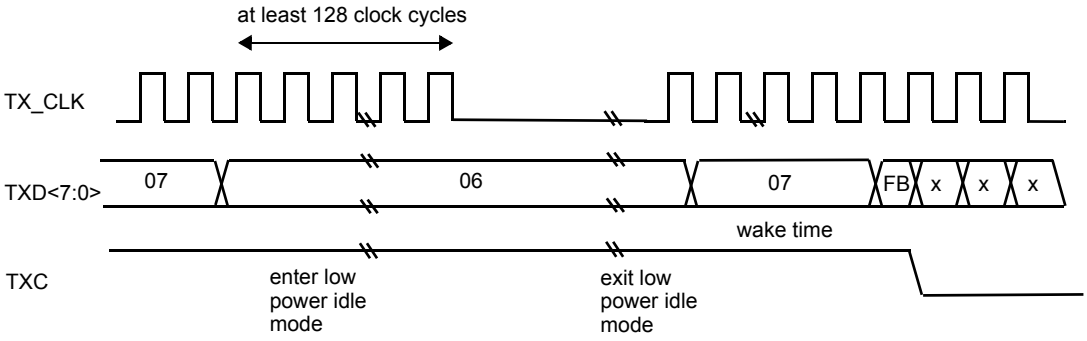
46.3.1.5 Transmit direction LPI transition

LPI operation and the LPI client are described in 78.1. The RS requests the PHY to transition to the LPI state by asserting TXC and setting TXD to 0x06 (in all lanes). The RS maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The RS may halt TX_CLK at any time more than 128 clock cycles after the start of the LPI state as shown in Figure 46–7a if the clock stop capable bit of the attached sublayer is asserted (see 45.2.3.2.a and 45.2.5.2.a). It is the responsibility of the management entity to ensure that the RS does not halt the TX_CLK if the attached device does not have its stop clock capable bit set. The RS shall restart TX_CLK so that at least one positive transition occurs before it deasserts LPI.

The RS asserts TXC and asserts IDLE on lanes 0-3 in order to make the PHY transition out of the LPI state. The RS should not present a start code for valid transmit data until after the wake up time specified for the PHY.

Figure 46–7a shows the behavior of TXC and TXD<7:0> during the transition into and out of the LPI state.



Note: TXC and TXD are shown for one lane, all 4 lanes behave identically during LPI

Figure 46–7a—LPI transition

Table 46–3 summarizes the permissible encodings of TXD<31:0>, TXC<3:0>.

Insert new row and change Table 46-4 in 46.3.2.2 as follows:

46.3.2.2 RXC<3:0> (receive control)

Table 46–4—Permissible lane encodings of RXD and RXC

RXC	RXD	Description	PLS_DATA.indication parameter
~~1~~	~~00 through 06~~	~~Reserved~~	~~—~~
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to indicate LP_IDLE is asserted	No applicable parameter (Normal inter-frame)
NOTE—Values in RXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).			

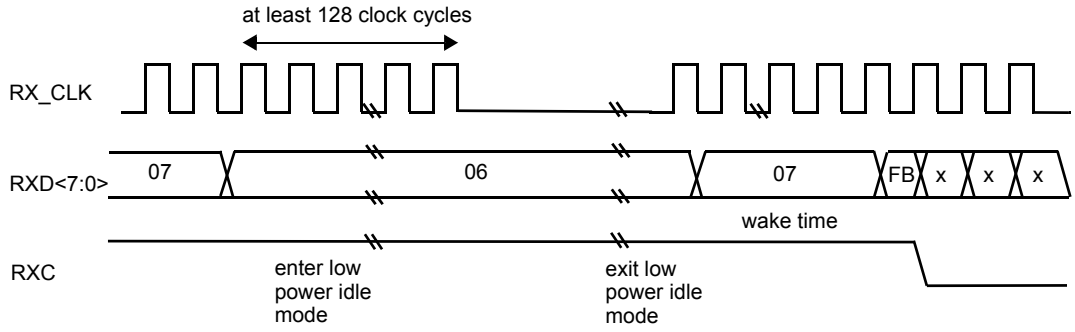
Insert 46.3.2.4 after 46.3.2.3 for receive LPI transition:

46.3.2.4 Receive direction LPI transition

LPI operation and the LPI client are described in 78.1. When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the RS by asserting RXC and setting RXD to 0x06 (in all lanes). The PHY maintains these signals in this state while it remains in the LPI state. When the PHY receives signals from the link partner to indicate transition out of the LPI state it indicates this to the RS by asserting RXC and asserting idle on lane 0-3 to return to a normal interframe state. The RS shall interpret the LPI coding as shown in Table 46–4.

The PHY or DTE XS may halt RX_CLK at any time more than 128 clock cycles after the start of the LPI state as shown in Figure 46–8a if the clock stop enable bit is asserted (see 45.2.3.1.3a and 45.2.5.1.3a). The PHY shall restart RX_CLK so that at least one positive transition occurs before it deasserts LPI.

Figure 46–8a shows the behavior of RXC and RXD<7:0> during LPI transitions.



Note: RXC and RXD are shown for one lane, all 4 lanes behave identically during LPI
Note: In some instances, LPI may be followed by characters other than IDLE during wake time

Figure 46–8a—LPI transition

Change 46.3.4 as follows:

46.3.4 Link fault signaling

Link fault signaling operates between the remote RS and the local RS. Faults detected between the remote RS and the local RS are received by the local RS as Local Fault. Only an RS originates Remote Fault signals.

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS stops sending MAC data or LPI, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). When Remote Fault or Link Interruption status is received by an RS, the RS stops sending MAC data or LPI, and continuously generates Idle control characters. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data or LPI.

Status is signaled in a four byte Sequence ordered_set as shown in Table 46–5. The PHY indicates Local Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x01 in lane 3. The RS indicates a Remote Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x02 in lane 3. Though most fault detection is on the receive data path of a PHY, in some specific sublayers, faults can be detected on the transmit side of the PHY. This is also indicated by the PHY with a Local Fault status.

For operation with links that may be temporarily interrupted, optional detection of a third fault condition, Link Interruption, is provided. Link Interruption is indicated by the PHY receive function by continuously sending the Link Interruption ordered_set as defined in Table 46-5.

Table 46–5—Sequence ordered_sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	0x00	0x00	0x03	Link Interruption
Sequence	≥ 0x00	≥ 0x00	≥ 0x03~~3~~4	Reserved
NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications				

The RS reports the fault status of the link. Local Fault indicates a fault detected on the receive data path between the remote RS and the local RS. Remote Fault indicates a fault on the transmit path between the local RS and the remote RS. The RS shall implement the link fault signaling state diagram (see Figure 46–10a).

Change 46.3.4.2 as follows:

46.3.4.2 Variables and counters

The link fault signaling state diagram uses the following variables and counters:

col_cnt
: A count of the number of columns received not containing a fault_sequence. This counter increments at RX_CLK rate (on both the rising and falling clock transitions) unless reset.

fault_sequence
: A new column received on RXC<3:0> and RXD<31:0> comprising a Sequence ordered_set of four bytes and consisting of a Sequence control character in lane 0 and a seq_type in lanes 1, 2, and 3 indicating either Local Fault, ~~or~~ Remote Fault or Link Interruption.

last_seq_type
: The seq_type of the previous Sequence ordered_set received
: Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.
Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3.

link_fault
: An indicator of the fault status.
: Values: OK; No fault.
Local Fault; fault detected by the PHY.
Remote Fault; fault detection signaled by the remote RS.
Link Interruption; link temporarily unavailable, signaled by the PHY.

reset
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
: Values: FALSE: The device is completely powered and has not been reset (default).
TRUE: The device has not been completely powered or has been reset.

seq_cnt

A count of the number of received Sequence ordered_sets of the same type.

seq_type

The value received in the current Sequence ordered_set

Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.
Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3.

Change the last two paragraphs of 46.3.4.3 as follows:

46.3.4.3 State Diagram

The variable link_fault is set to OK following any interval of 128 columns not containing a Remote Fault, ~~or~~ Local Fault or Link Interruption Sequence ordered_set.

The RS output onto TXC<3:0> and TXD<31:0> is controlled by the variable link_fault.

a) link_fault = OK
The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.
b) link_fault = Local Fault
The RS shall continuously generate Remote Fault Sequence ordered_sets.
c) link_fault = Remote Fault or link_fault = Link Interruption
The RS shall continuously generate Idle control characters.

Insert a new section, 46.3a before 46.4:

46.3a LPI Assertion and Detection

Certain PHYs support Energy Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the RS to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the XGMII signals as shown in Figure 46–9a.

The definition of TXC<3:0> and TXD<31:0> is derived from the state of PLS_DATA.request (46.1.7), except when it is overridden by an assertion of LP_IDLE.request.
Similarly, RXC<3:0> and RXD<31:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected
PLS_CARRIER.indication(CARRIER_STATUS) will be set to CARRIER_ON when the link is in LPI mode. See 46.1.7.3.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

46.3a.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or de-assertion of LPI from the link partner.

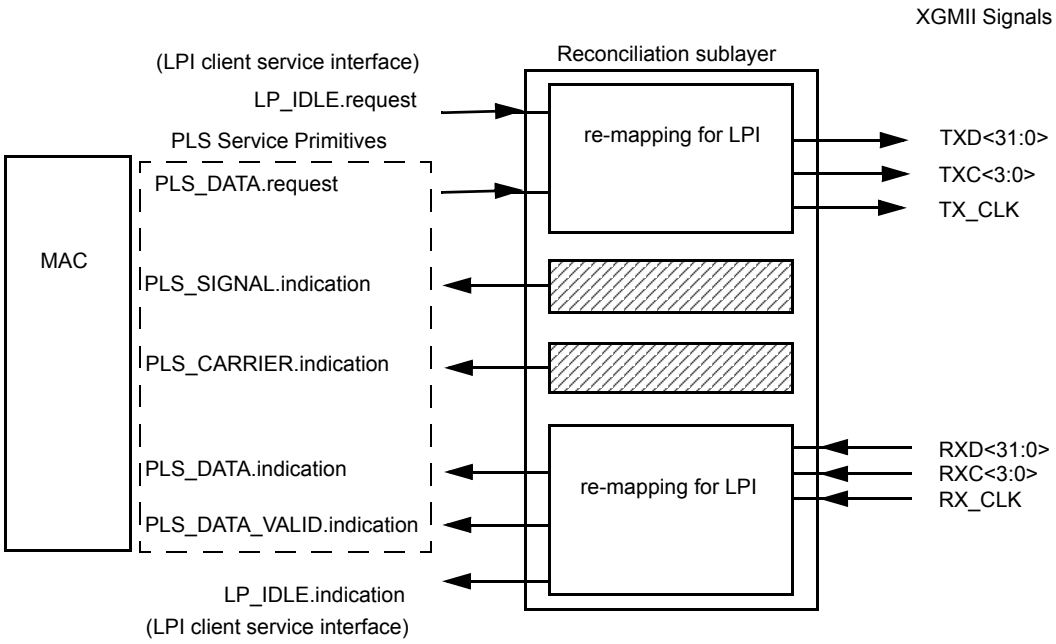


Figure 46–9a—LPI assertion and detection mechanism

Values:DEASSERT: The link partner is operating with normal inter-frame behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT initiates the signaling of LPI to the link partner. DE-ASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or within 1 second of the change of link_status to OK.

46.3a.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been de-asserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 46–10a.

Editors' Note: *To be removed prior to publication.*
The state diagram conventions described in 46.3.4.1 apply to all of the state diagrams in this clause.

46.3a.2.1 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

LPI_CARRIER_STATUS

The LPI_CARRIER_STATUS variable indicates how the CARRIER_STATUS parameter is con-

trolled by the LPI_REQUEST parameter. The LPI_CARRIER_STATUS is either TRUE or FALSE as determined by the Transmit LPI state diagram in Figure 46-10a.

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values:FALSE: The device is completely powered (default).

TRUE: The device has not been completely powered.

rs_reset

Used by management to control the resetting of the RS.

Values:FALSE: Do not reset the RS (default).

TRUE: Reset the RS.

tw_timer

A timer that counts, in microseconds, the time since the de-assertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2. If DTE XS XAUI stop enable bit is asserted (5.0.9), the terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 plus additional time equal to $T_{w\_sys\_tx}$ - $T_{w\_sys\_rx}$ for the XGXS as shown in Table 78-4.

The signal tw_timer_done is asserted when tw_timer reaches its terminal count.

46.3a.2.2 State Diagram

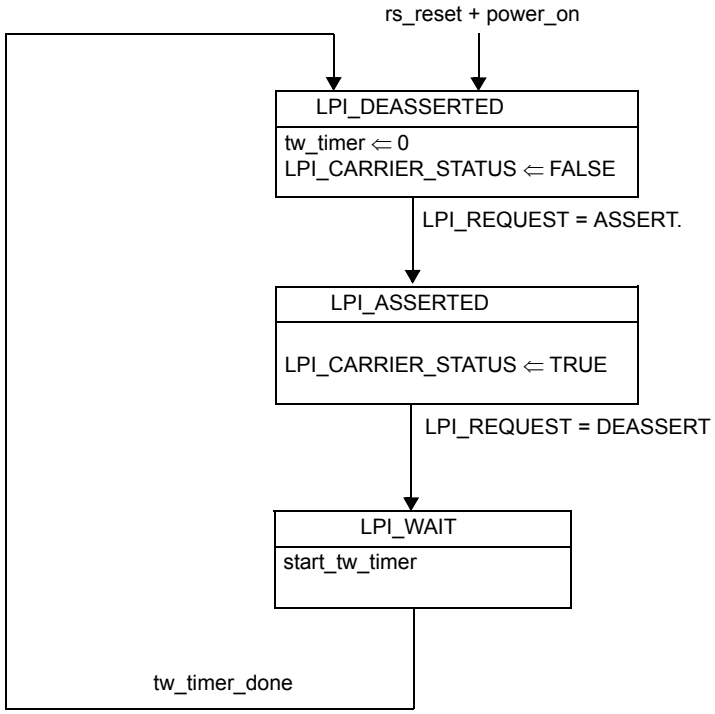


Figure 46–10a—Transmit LPI State Diagram

46.3a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the de-assertion of LPI. Buffering and queue management should be designed to accommodate this.

46.3a.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the XGMII. The receive system should be aware that data frames may arrive at the XGMII following the de-assertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

If the PHY XS XAUI stop enable bit (4.0.9) is asserted, the PHY XS may stop signaling on the XAUI in the receive direction to conserve energy. The receiver should negotiate an additional 9.5 μs for the remote Tw_sys (equal to Tw_sys_tx - Tw_sys_rx for the XGXS as shown in Table 78–4) before setting the PHY XS XAUI stop enable bit.

46.5 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[1]

Insert the following row into table 46.5.2.3:

46.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	46.1.7		O	Yes [ ] No [ ]

Insert the new subclause 46.5.3.3a after 46.5.3.3 for LPI functions:

46.5.3.3a LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	46.3.1.2	As defined in Table 46–3	LPI:M	Yes [ ] N/A [ ]
L2	Assertion of LPI in Rx direction	46.3.2.2	As defined in Table 46–4	LPI:M	Yes [ ] N/A [ ]
*L3	TX_CLK stoppable during LPI	46.3.1.5	At least 128 cycles after LPI assertion	LPI:O	Yes [ ] No [ ]
L4	TX_CLK restart before LPI deassert	46.3.1.5	At least 1 positive edge before LPI deassertion	L3:M	Yes [ ] N/A [ ]
L5	RX_CLK stoppable during LPI	46.3.2.4		LPI:O	Yes [ ] No [ ]

46.5.3.3b Link Interruption

Item	Feature	Subclause	Value/Comment	Status	Support
LINT	Detection of Link Interruption	46.3.4		O	Yes [ ] No [ ]
LINT1	CARRIER_STATUS response to Link Interruption	46.1.7.3	Set to CARRIER_ON if link_fault is Link Interruption	LINT:O	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

47. XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)

Insert the following after the second paragraph of 47.1

47.1 Overview

An XGMII Extender with the optional Energy Efficient Ethernet (EEE) capability (see 78.3) may enter a low power state to conserve energy during periods of low link utilization. The ability to support transition to a low power state is indicated by register 4.20.0 (for a PHY XS) or 5.20.0 (for a DTE XS). Transition to the low power state is enabled by register 4.0.9 (for a PHY XS) or 5.0.9 (for a DTE XS). The assertion of Low Power Idle (LPI) at the XGMII is encoded in the transmitted symbols. Detection of LPI encoding in the received symbols is indicated as LPI at the XGMII. When LPI is received on the transmit XGMII, an Energy Efficient XGMII Extender sends sleep symbols, then, if enabled, ceases transmission and deactivates XAUI transmit signals to conserve energy. When the receiver sees the sleep symbols it transitions to a quiet state. The XGMII Extender periodically transmits during the quiet period to allow the attached XGMII Extender to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame idle is asserted at the transmit XGMII, the XGMII Extender re-activates transmit functions and initiates transmission. This transmission will be detected by the attached XGMII Extender, causing it to also exit the low power state.

Add the following items to the list of characteristics in 47.1

i) Optionally extend LPI signaling to PHY for EEE
j) Optionally conserve energy during periods of low utilization

Insert the following after 47.1.4

47.1.5 Global signal detect function

Global signal detect is mandatory for EEE capability otherwise it is optional and its definition is beyond the scope of this standard. When global signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

For EEE capability, the global signal detect function shall control the PMA SIGNAL_DETECT parameter. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the XGXS is detecting electrical energy at the XAUI receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMA parameter rx_lane<3:0> is undefined.

47.1.6 Global transmit disable function

Global transmit disable is mandatory for EEE capability. The transmit disable function shall turn off all transmitter lanes after tx_mode changes to QUIET within a time and voltage level specified in 47.3.3.2. The transmit disable function shall turn on all transmitter lanes after tx_mode changes to DATA within a time and voltage level specified in 47.3.3.2.

Add the following at the end of 47.3.3.2

47.3.3.2 Amplitude and swing

For EEE capability, the transmitter lane's differential peak-to-peak output voltage shall be less than 30mV within 500ns of tx_quiet being asserted. Furthermore, the transmitter lane's differential peak-to-peak output voltage shall be greater than 800mV within 500ns of tx_quiet being de-asserted.

Change Table 47-3 in 47.3.4

47.3.4 Receiver characteristics

Receiver characteristics are summarized in Table 47–3 and detailed in the following subclauses.

Table 47–3—Receiver characteristics

Parameter	Value	Units
Baud rate tolerance	3.125 ±100	GBd ppm
Unit interval (UI) nominal	320	ps
Receiver coupling	AC	
EEE Signal Detect deactivation time (T_{SD}) from active to LPI quiet	750	ns
EEE Signal Detect activation time (T_{SA}) from LPI quiet to active	750	ns
Return loss[a] differential common-mode	 10 6	 dB dB
Jitter amplitude tolerance[b]	0.65	UI_{p-p}

[a]Relative to 100 Ω differential and 25 Ω common-mode. See 47.3.4.5 for input impedance details.
[b]See 47.3.4.6 for jitter tolerance details.

Add subclause 47.3.4.7 after current subclause 47.3.4.6

47.3.4.7 EEE receiver timing

For EEE capability, the receiver shall meet the timing requirements shown in Table 47–3 for Signal_Detect activation and deactivation.

47.6 Protocol implementation conformance statement (PICS) proforma for Clause 47, XGMII Extender (XGMII) and 10 Gigabit Attachment Unit Interface (XAUI)[1]

Insert the following row into table 48.6.3:

47.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	47.1		O	Yes [ ] No [ ]

Insert the new subclause 48.6.4.4 after 47.6.4.3 for LPI functions:

47.6.4.4 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Global signal detect	47.1.5	Meet the requirements of 47.1.5	LPI:M	Yes [ ] No [ ]
LP-02	Global transmit disable	47.1.6	Meet the requirements of 47.1.6	LPI:M	Yes [ ] No [ ]
LP-03	Transmit amplitude	47.3.3.2	Meet the requirements of 47.3.3.2	LPI:M	Yes [ ] No [ ]
LP-04	Signal detect timing	47.3.4	Meet the requirements of Table 47–3	LPI:M	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X

Add a paragraph at the end of 48.1.5

48.1.5 Allocation of functions

Certain PHYs support Energy Efficient Ethernet (EEE) (see Clause 78). PHYs that support EEE (see 78.3) use Low Power Idle (LPI) signaling to allow systems on both sides of the link to save power during periods of low link utilization. LPI signaling may optionally be used by XGXS to extend the EEE function to attached PHYs. Both PHY and DTE XGXS may optionally use LPI signaling to control the shutdown of signals on the XAUI to reduce power for PHY attachments.

Change 48.2.3 for LPI code groups

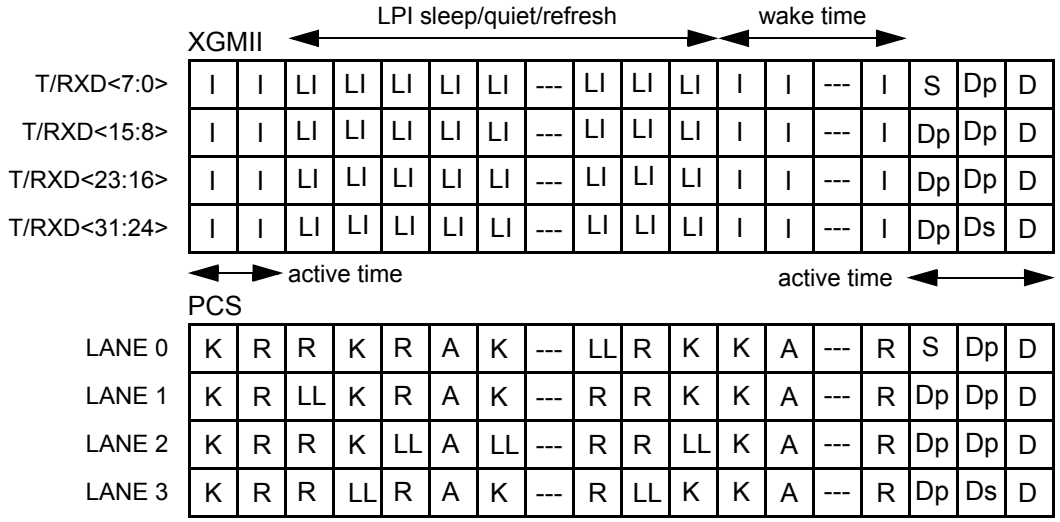
48.2.3 Use of code-groups

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 36.2.4. A 10GBASE-X PCS shall meet the requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. PCS lanes are independent of one another. All code-group rules specified in 36.2.4 are applicable to each lane. The mapping of XGMII characters to PCS code-groups is specified in Table 48–2. The mapping of PCS code-groups to XGMII characters is specified in Table 48–3. PHYs that support EEE are able to transmit and receive LPI characters.

Figure 48–3 illustrates the mapping of an example XGMII character stream into a PCS code-group stream. Figure 48-3a illustrates the mapping during LPI.

The relationship of code-group bit positions to XGMII, PCS and PMA constructs and PMD bit transmission order, exemplified for lane 0, is illustrated in Figure 48–4.

Insert Figure 48-3a as shown



Legend:
LI represents the data character containing the XGMII LPI pattern (06)
LL represents the LPI indication codegroup /D20.5/
Dp represents a data character containing the preamble pattern
Ds represents a data character containing the SFD pattern

Figure 48–3a—XGMII and PCS mapping example with optional LPI

In 48.2.4, insert row in Table 48-2 below "Normal data transmission;" insert row in Table 48-3 below "Normal data transmission;"and change rows in Link Status section of Table 48-4 all as follows:

48.2.4 Ordered_sets and special code-groups

.

Table 48–2—XGMII character to PCS code-group mapping

XGMII TXC	XGMII TXD	PCS code group	Description
1	06	K28.0 or K28.3 or K28.5 or D20.5[a]	Assert LPI
NOTE—Values in TXD column are in hexadecimal			

[a]Insertion of /D20.5/ is per the rules described in 48.2.4.2

Table 48–3—PCS code-group to XGMII character mapping

XGMII RXC	XGMII RXD	PCS code group	Description
1	06	K28.0 or K28.3 or K28.5 or D20.5[a]	Assert LPI
NOTE—Values in RXD column are in hexadecimal			

[a]Insertion of /D20.5/ is per the rules described in 48.2.4.2

Table 48–4—Defined ordered_sets and special code-groups

Code	Ordered_Set	Number of code-groups	Encoding
	Link Status		
||Q||	Sequence ordered_set	4	/K28.4/Dx.y/Dx.y/Dx.y/[a]
||LF||	Local Fault signal	4	/K28.4/D0.0/D0.0/D1.0/
||RF||	Remote Fault signal	4	/K28.4/D0.0/D0.0/D2.0/
||LINT||	Link Interruption signal	4	/K28.4/D0.0/D0.0/D3.0/
||Qrsvd||	Reserved	4	!||LF|| and !||RF|| and !||LINT||
[a]/Dx.y/ indicates any data code-group.			

Change 48.2.4.2 for LPI definitions

48.2.4.2 Idle (||I||) and Low Power Idle (||LPIDLE||)

Idle ordered_sets (||I||) are transmitted in full columns continuously and repetitively whenever the XGMII is idle (TXD<31:0>=0x07070707 and TXC<3:0>=0xF). ||I|| provides a continuous fill pattern to establish and maintain lane synchronization, perform lane-to-lane deskew and perform PHY clock rate compensation. ||I|| is emitted from, and interpreted by, the PCS.

A sequence of ||I|| ordered_sets consists of one or more consecutively transmitted ||K||, ||R|| or ||A|| ordered_sets, as defined in Table 48–4. Rules for ||I|| ordered_set sequencing shall be as follows:

a) ||I|| sequencing starts with the first column following a ||T||.
b) The first ||I|| following ||T|| alternates between ||A|| or ||K|| except if an ||A|| is to be sent and less than *r* [see item d)] columns have been sent since the last ||A||, a ||K|| is sent instead.
c) ||R|| is chosen as the second ||I|| following ||T||.
d) Each ||A|| is sent after *r* non-||A|| columns where *r* is a randomly distributed number between 16 and 31, inclusive. The corresponding minimum spacing of 16 non-||A|| columns between two ||A|| columns provides a theoretical 85-bit deskew capability.
e) When not sending an ||A||, either ||K|| or ||R|| is sent with a random uniform distribution between the two.
f) Whenever sync_status=OK, all ||I|| received during idle are translated to XGMII Idle control characters for transmission over the XGMII. All other !||I|| received during idle are mapped directly to XGMII data or control characters on a lane by lane basis, with the following exceptions for PHYs with EEE capability:

1) /D20.5/ (LPI) being detected in any lane and the rest of the lanes in the same column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE characters in all lanes.
2) ||A|| being detected and /D20.5/ (LPI) being detected in any lane of the previous column and the rest of the lanes in the previous column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE characters in all lanes.

The purpose of randomizing the ||I|| sequence is to reduce 10GBASE-X electromagnetic interference (EMI) during idle. The randomized ||I|| sequence produces no discrete spectrum. Both ||A|| spacing as well as ||K||, ||R||, or ||A|| selection shall be based on the generation of a random integer *r* generated by a PRBS based on one of the 7th order polynomials listed in Figure 48–5. ||A|| spacing is set to the next generated value of *r*. The rate of generation of *r* is once per column, 312.5 MHz ± 100 ppm. Once the ||A|| spacing count goes to zero (A_CNT=0), ||A|| is selected for transmission at the next opportunity during the Idle sequence. ||K|| and ||R|| selection follows the value of code_sel, which is continuously set according to the even or odd value of *r*. The method of generating the random integer *r* is left to the implementor. PCS Idle randomizer logic is illustrated in Figure 48-5.

||LPIDLE|| is coded in the same manner as ||I|| except that the /D20.5/ code group replaces one code group in each ||K|| or ||R|| (not ||A||) column with a random uniform distribution across the lanes. Insertion of /D20.5/ does not alter the distribution of ||A||, ||K|| or ||R||. Clock compensation may be performed during LPI according to the rules described in 48.2.4.2.3.

Insert the following at the end of 48.2.4.2.3

48.2.4.2.3 Skip ||R||

For EEE capability, a column containing three /R/ code groups and one /D20.5/ code group may be inserted or deleted in the same manner as four /R/ code groups.

Change the following constant definitions in 48.2.6.1.2 as follows:

48.2.6.1.2 Constants

||K||
: The column of four identical Idle Sync code-groups corresponding to the Idle Sync function specified in 48.2.4.2.1. For EEE capability, one lane of ||K|| is replaced by /D20.5/ during the assertion of LPI as defined in 48.2.4.2.

||R||
: The column of four identical Idle Skip code-groups corresponding to the Idle Skip function specified in 48.2.4.2.3. For EEE capability, one lane of ||R|| is replaced by /D20.5/ during the assertion of LPI as defined in 48.2.4.2.

Insert the following text into 48.2.6.1.2 at the end of the existing subclause

The following constants are used only for the EEE capability.

||LPIDLE||
: The column consisting of three /K/ characters and one of /D20.5/, or three /R/ characters and one /D20.5/, or a column of ||A|| preceded by a column containing three /K/ characters and one /D20.5/ or three /R/ characters and one /D20.5/ as specified in 48.2.4.2.

48.2.6.1.3 Variables

Insert a note in 48.2.6.1.3 below the definition for "align_status"

NOTE: For EEE capability, this variable is affected by the LPI receive state diagram. Without EEE capability this variable is identical to deskew_align_status controlled by the deskew state diagram

Insert new variables into 48.2.6.1.3, new timers into 48.2.6.1.5 and new messages into 48.2.6.1.6 for LPI state diagrams. In each case, insert the new text at the end of the existing subclause

The following variables are used only for the EEE capability.

deskew_align_status
: Variable used to by the deskew state diagram to reflect the status of the lane-to-lane code-group alignment.

  Values: FAIL; The deskew process is not complete.
  OK; All lanes are synchronized and aligned.

rx_lpi_active
: A boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and is not restricted by the LPI receive state diagram.

rx_quiet
: A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise. When this variable is TRUE it indicates that receive PCS and PMD may power-down nonessential functions.

tx_quiet
: A boolean variable set to TRUE when the transmitter is in the TX_QUIET state and is set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 71.6.6. When this variable is TRUE it indicates that transmit PCS and PMD may power-down nonessential functions.

48.2.6.1.5 Counters

The following counter is used only for the EEE capability.

wake_error_counter
: A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.8b)

48.2.6.1.6 Message

The following messages are used only for the EEE capability.

PMD_RXQUIET.request(rx_quiet)
: A signal sent by the PCS LPI receive state diagram to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data.

PMD_TXQUIET.request(tx_quiet)
: A signal sent by the PCS LPI transmit state diagram to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium.

Insert a new subclause 48.2.6.1.5a after 48.2.6.1.5

48.2.6.1.5a Timers

The following timers are used only for the EEE capability.

rx_tq_timer
: This timer is started when the PCS receiver enters the RX_SLEEP state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
: This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall be set to a value no larger than the maximum value given for T_{WR} in Table 48–10. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
: This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the QUIET state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
: This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

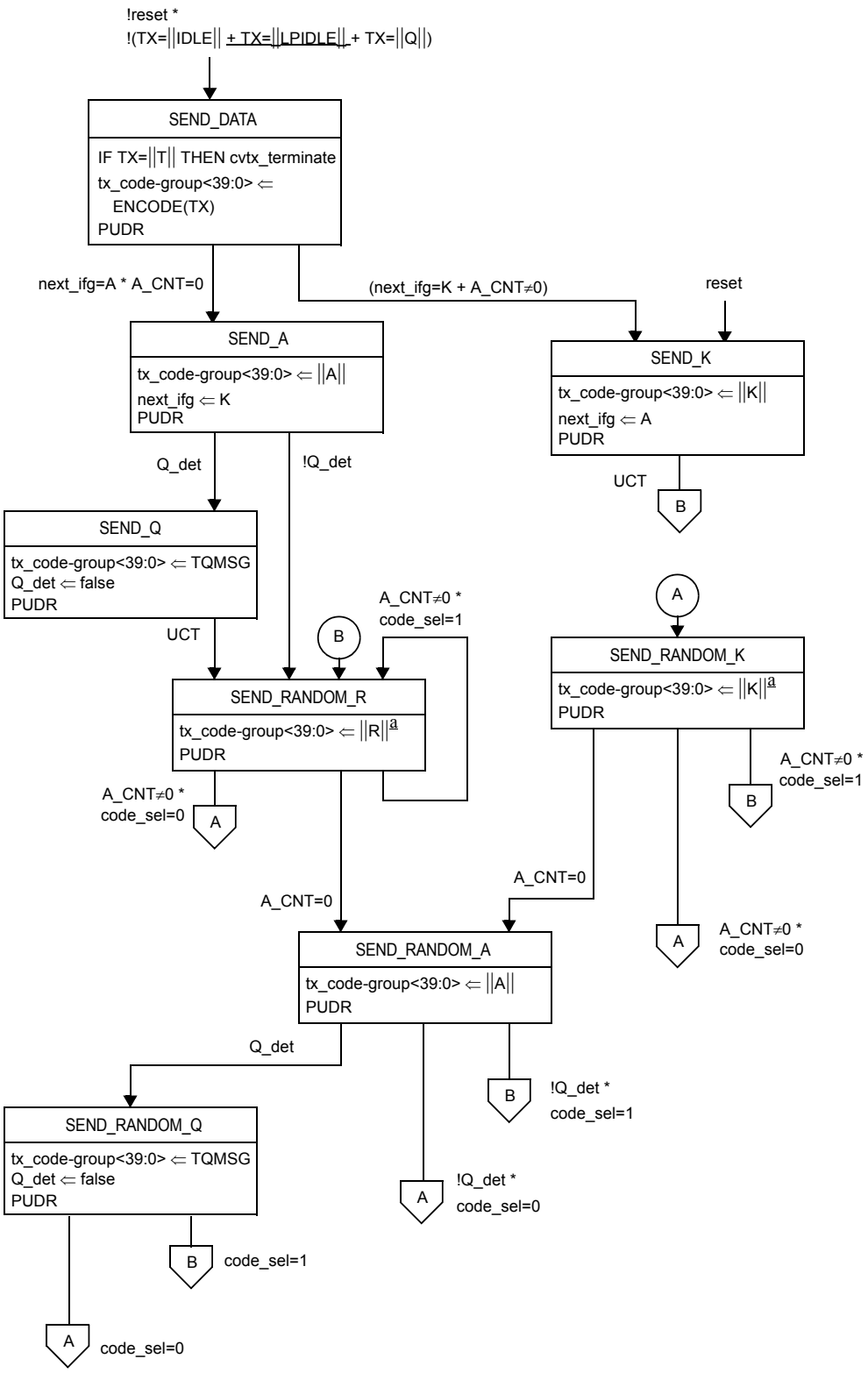
tx_tr_timer
: This timer is started when the PCS transmitter enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

48.2.6.2 State diagrams

Change Figure 48-6 for PCS transmit source state diagram; Figure 48-8 for synchronization and deskew; and Figure 48-9 for PCS receive state diagram

> ***Editors' Note:*** *To be removed prior to publication.*
> *The state diagram conventions described in 48.2.6 apply to all of the state diagrams in this clause.*

Change 48.2.6.2.2 and 48.6.2.3



[a] If TX=||LPIDLE|| one lane is replaced by /D20.5/ as defined in 48.2.4.2.

NOTE—The state diagram makes exactly one transition for each transmit code-group processed.

Figure 48–6—PCS transmit source state diagram

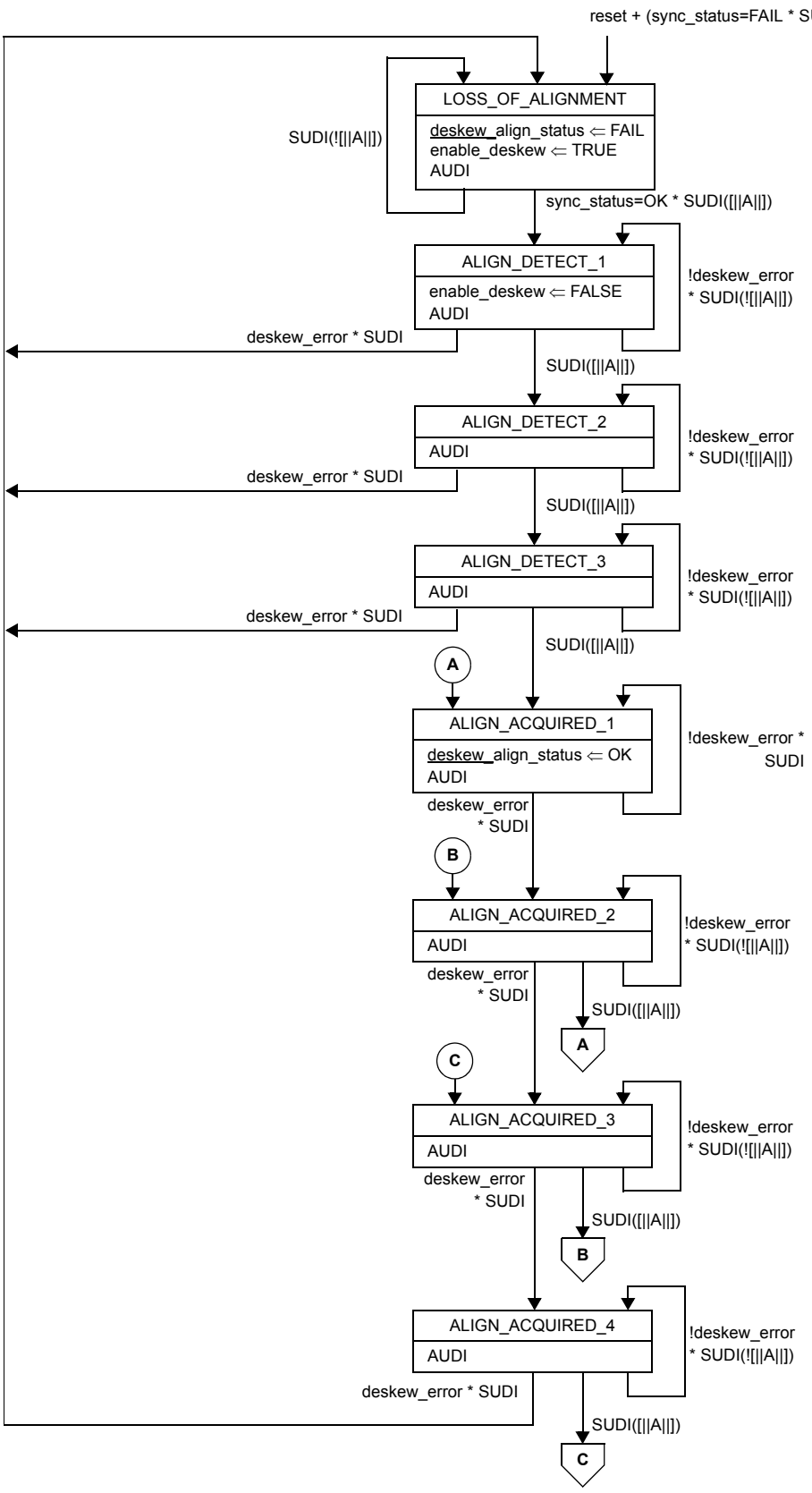


Figure 48–8—PCS deskew state diagram

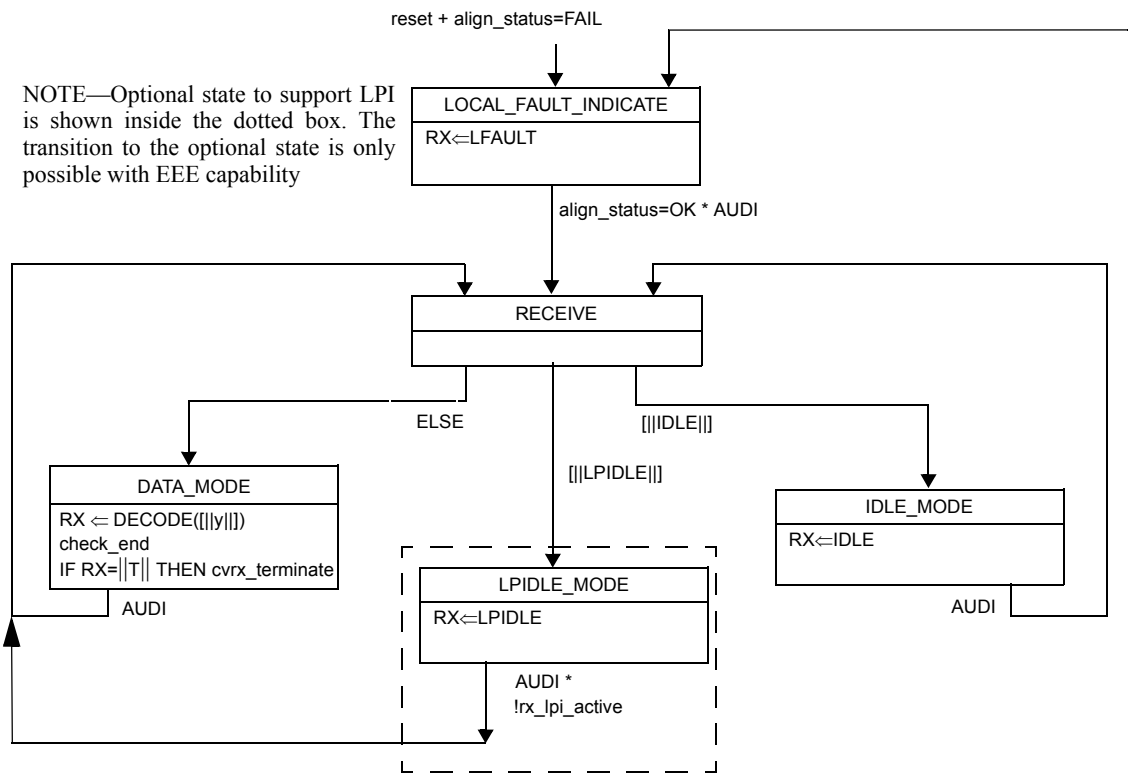


Figure 48–9—PCS receive state diagram

48.2.6.2.2 Synchronization

The PCS shall implement four Synchronization processes as depicted in Figure 48–7 including compliance with the associated state variables as specified in 48.2.6.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions. A Synchronization process operates independently on each lane, and synchronization is complete only when synchronization is acquired on all lanes. The synchronization process described in the following paragraphs applies to each lane.

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indication primitive and conveys received code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message.

When in the LOSS_OF_SYNC state, the PCS may attempt to realign its current code-group boundary to one which coincides with the code-group boundary defined by a comma (see 36.2.4.9). This process is referred to in this document as code-group alignment.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states. The Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis). Whenever any PMA lane is not operating dependably, as indicated by the setting of lane_sync_status <3:0>, the ~~align_status~~ deskew_align_status flag is set to FAIL

48.2.6.2.3 Deskew

The PCS shall implement the Deskew process as depicted in Figure 48–8 including compliance with the associated state variables as specified in 48.2.6.1. The Deskew process is responsible for determining whether the underlying receive channel is capable of presenting coherent data to the XGMII. The Deskew process asserts the deskew_align_status ~~align_status~~ flag to indicate that the PCS has successfully deskewed and aligned code-groups on all lanes. The Deskew process attempts deskew and alignment whenever the deskew_align_status ~~align_status~~ flag is de-asserted. The Deskew process is otherwise idle. For the EEE capability the relationship between align_status and deskew_align_status is given by Figure 48–9b, the LPI receive state diagram, otherwise align_status is identical to deskew_align_status. Whenever the align_status flag is set to FAIL the condition is indicated as a link_status=FAIL condition in the status register bit 4.1.2 or 5.1.2.

Once alignment is acquired, the Deskew process tests received columns and employs multiple sub-states, effecting hysteresis, to move between the ALIGN_ACQUIRED_1 and LOSS_OF_ALIGNMENT states. These states monitor the link for continued alignment, tolerate alignment inconsistencies due to a reasonably low BER, and restart the Deskew process if alignment can not be reliably maintained.

Change the first paragraph of 48.2.6.2.4:

48.2.6.2.4 Receive

The PCS shall implement its Receive process as depicted in Figure 48–9, including compliance with the associated state variables as specified in 48.2.6.1 and including the optional EEE capability.

Insert 48.2.6.2.5 after 48.2.6.2.4 for LPI state diagrams:

48.2.6.2.5 LPI state diagrams

A PCS which supports the EEE capability shall implement the LPI transmit and receive processes as shown in Figures 48–9a and 48–9b. The transmit LPI state diagram controls tx_quiet which disables the transmitter when TRUE. The receive LPI state diagram controls align_status during LPI and synchronizes the receive state diagram with the end of the LPI.

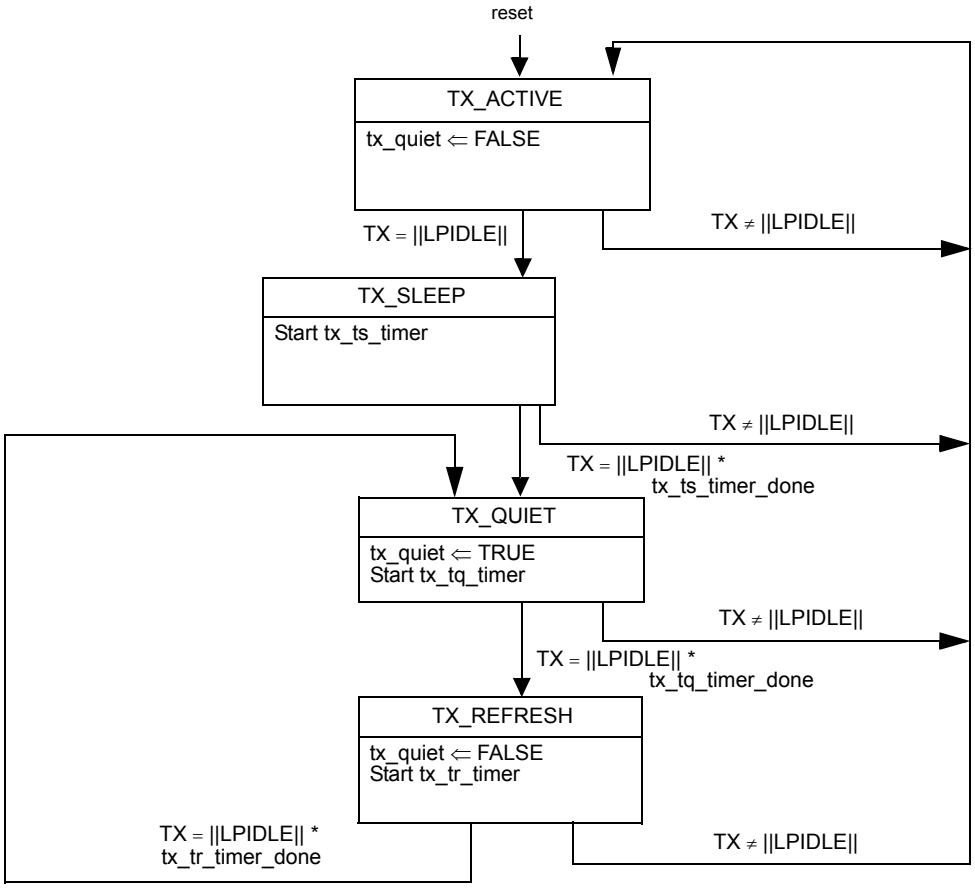


Figure 48–9a—LPI Transmit state diagram

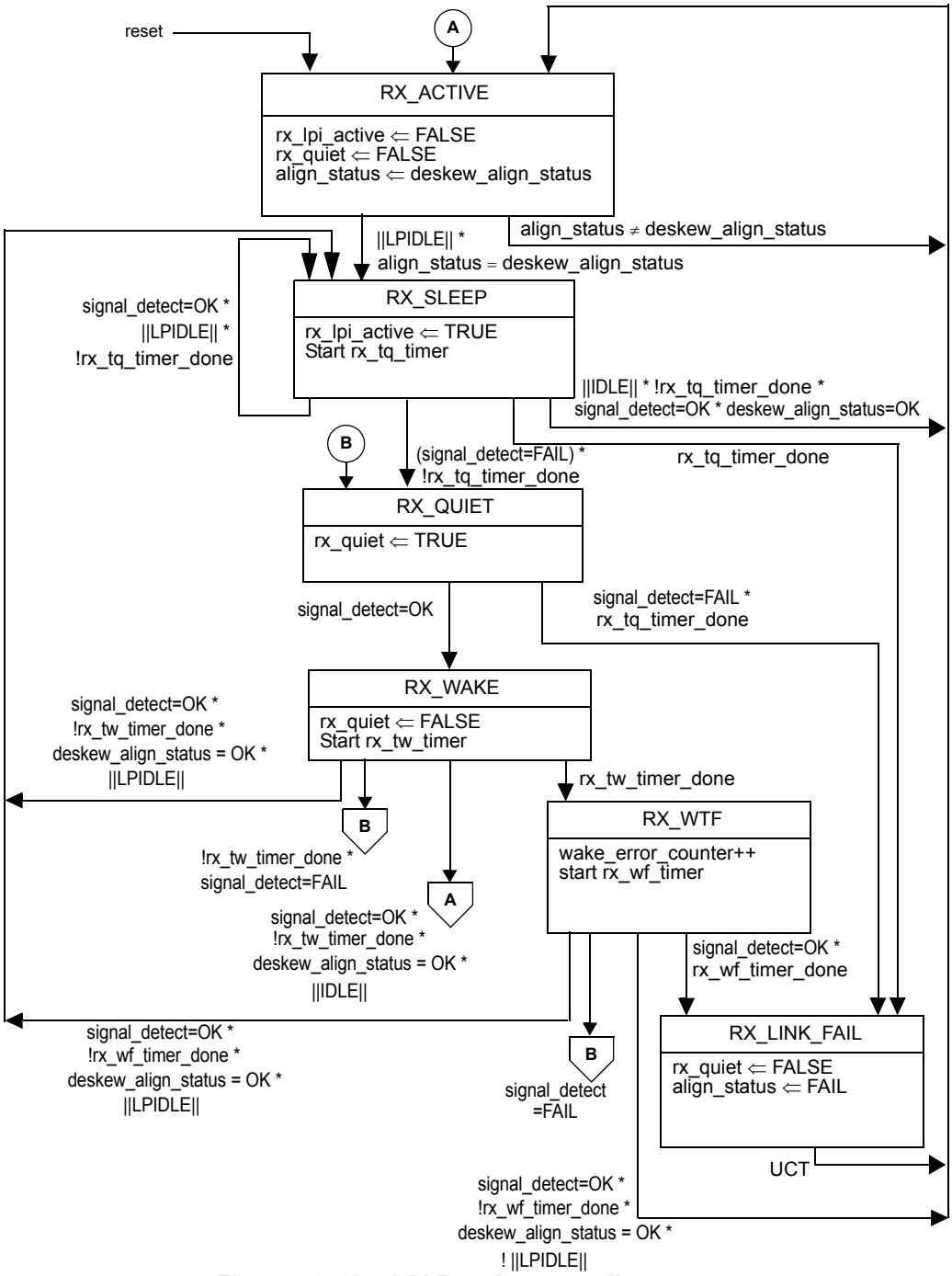


Figure 48–9b—LPI Receive state diagram

The LPI functions shall use timer values for these state diagrams as shown in Table 48–9 for transmit and Table 48–10 for receive.

Table 48–9—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_quiet is set to TRUE	19.9	20.1	µs
T_{QL}	Local Quiet Time from when tx_quiet is set to TRUE to entry into the TX_REFRESH state	2.5	2.6	ms
T_{UL}	Local Refresh Time from entry into the TX_REFRESH state to entry into the TX_QUIET state	19.9	20.1	µs

Table 48–10—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect to be set to OK while in the RX_SLEEP and RX_QUIET states before asserting rx_fault	3	4	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault.		9	µs
T_{WTF}	Wake time fault recovery time		1	ms

Insert 48.2.6.2.6 for LPI status:

48.2.6.2.6 LPI status and management

For EEE capability, the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variable shown in Table 48–11.

Table 48–11—MDIO status indications

MDIO status variable	Register name	Register address	Note
Tx LPI received	PCS status register 1	3.1.11	Latched version of 3.1.9
Rx LPI received	PCS status register 1	3.1.10	Latched version of 3.1.8
Tx LPI indication	PCS status register 1	3.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	PCS status register 1	3.1.8	TRUE when not in state RX_ACTIVE
Tx LPI received	PHY XS status register 1	4.1.11	Latched version of 4.1.9
Rx LPI received	PHY XS status register 1	4.1.10	Latched version of 4.1.8
Tx LPI indication	PHY XS status register 1	4.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	PHY XS status register 1	4.1.8	TRUE when not in state RX_ACTIVE
Tx LPI received	DTE XS status register 1	5.1.11	Latched version of 5.1.9
Rx LPI received	DTE XS status register 1	5.1.10	Latched version of 5.1.8
Tx LPI indication	DTE XS status register 1	5.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	DTE XS status register 1	5.1.8	TRUE when not in state RX_ACTIVE

48.7 Protocol implementation conformance statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X[1]

Insert the following row into table 48.7.3:

48.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	48.2.3		O	Yes [ ] No [ ]

Insert the new subclause 48.7.4.5 after 48.7.4.4 for LPI functions:

48.7.4.5 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Receive state diagrams	48.2.6.2	Support additions to Figure 48–9 for LPI operation	LPI:M	Yes [ ] No [ ]
LP-01	LPI transmit state diagrams	48.2.6.2.5	Meet the requirements of Figure 48–9a	LPI:M	Yes [ ] No [ ]
LP-01	LPI receive state diagrams	48.2.6.2.5	Meet the requirements of Figure 48–9b	LPI:M	Yes [ ] No [ ]
LP-01	LPI transmit timing	48.2.6.2.5	Meet the requirements of Table 48–9	LPI:M	Yes [ ] No [ ]
LP-01	LPI receive timing	48.2.6.2.5	Meet the requirements of Table 48–10	LPI:M	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

49. Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R

Change 49.1.5 and 49.1.6 for sublayer interfaces and block diagram:

49.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-R. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. The PCS service interface is the XGMII that is defined in Clause 46. The XGMII has an optional physical instantiation. An optional physical instantiation of the PMA service interface has also been defined (see Clause 51). It is called XSBI (10 Gigabit Sixteen Bit Interface). Figure 49–4 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-R.

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XGMII or the PCS may connect to an XGXS sublayer. The XGXS and the Reconciliation Sublayer provide the same service interface to the PCS. The lower interface of the PCS may connect to the WIS to support a WAN PMD or to the PMA sublayer to support a 10GBASE-R LAN PMD. The WIS and PMA interfaces are functionally equivalent except for data rate. When the PCS is connected directly to a LAN PMA, the nominal rate of the PMA service interface is 644.53 Mtransfers/s, which provides capacity for the MAC data rate of 10 Gb/s. When the PCS is connected to a WAN PMA, the nominal rate of the WIS service interface is 599.04 Mtransfers/s and the MAC uses IFS stretch mode to ensure that there will be enough idle time that the PCS can delete idles to adjust to the lower rate. Since the data rates are different, WIS and PMA interface connections pose somewhat different constraints. The PCS shall support connection to either a WIS or to a PMA and may optionally support both.

If the optional Energy Efficient Ethernet (EEE) capability is supported (see Clause 78, 78.3) then the interface with the PMA sublayer (or FEC sublayer) includes rx_mode and tx_mode to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver. If the PHY includes an FEC sublayer the interface includes rx_lpi_active to indicate that the LPI receive state diagram is not in RX_ACTIVE state.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

49.1.6 Functional block diagram

Figure 49–4 provides a functional block diagram of the 10GBASE-R PHY.

Editors' Note: *To be removed prior to publication.*
The state diagram conventions described in 49.2.13.1 apply to all of the state diagrams in this clause.

Change 49.2.4.4 for LPI function:

49.2.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-R PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-R PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-R PCS encodes the ordered_set control codes using a combination of the block type field and a 4-bit O code for each ordered_set. The 10GBASE-R PCS encodes each of the other control characters into a 7-bit C code.

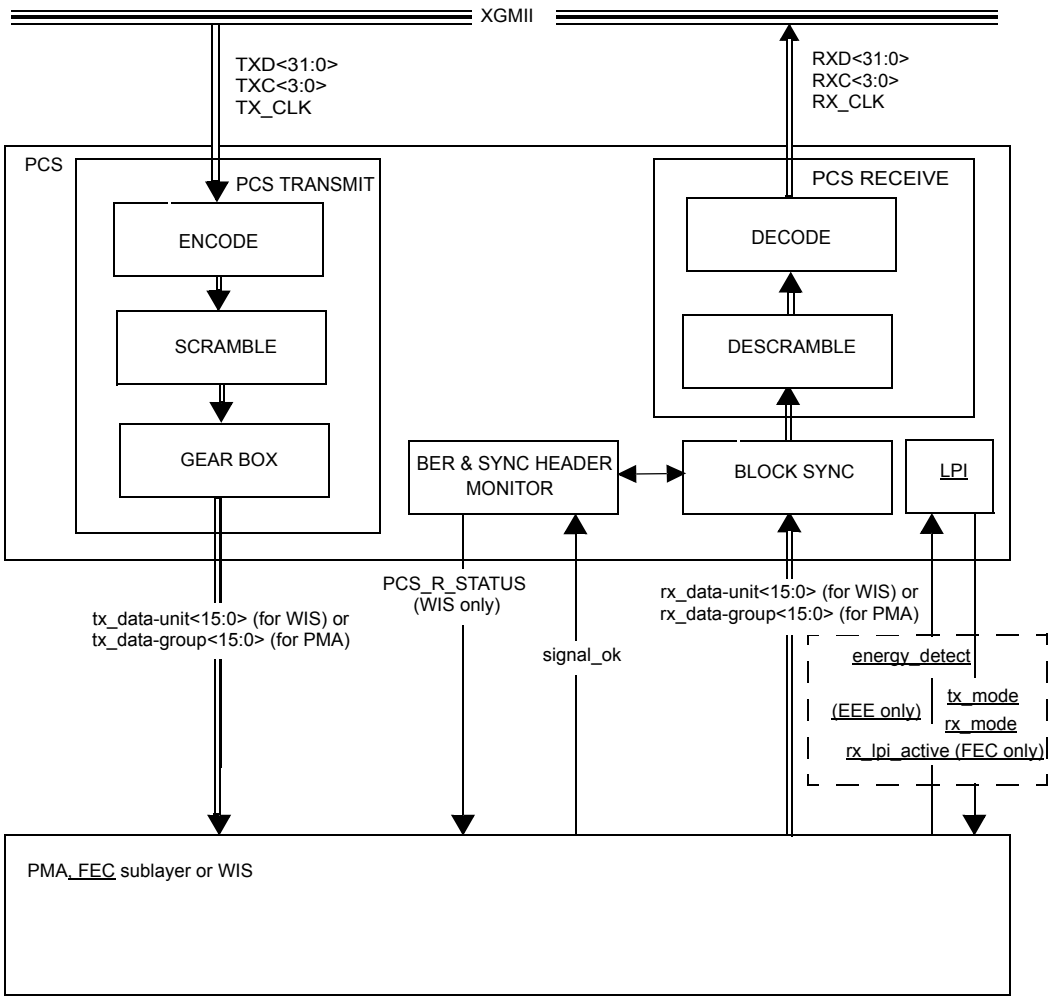


Figure 49–4—Functional block diagram

The control characters and their mappings to 10GBASE-R control codes and XGMII control codes are specified in Table 49–1. All XGMII and 10GBASE-R control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received. The ability to transmit or receive Low Power Idle (LPI) is required for PHYs that support EEE (see Clause 78). If EEE is not supported LPI shall not be transmitted and shall be treated as an error if received.

49.2.4.5 Ordered sets

Change Table 49-1 for LPI encoding, insert row:

Change 49.2.4.7 for LPI definitions

49.2.4.7 Idle /I/ and Low Power Idle /LI/

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall

Table 49–1—Control codes

Control character	Notation	XGMII control code	10GBASE-R control code	10GBASE-R O code	8B/10B code[a]
Idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
LPI	/LI/	0x06	0x06		K28.0 with D20.5 in one row or K28.3 or K28.5 with D20.5 in one row[b]
Start	/S/	0xfb	Encoded by block type field		K27.7

[a]For information only.The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48
[b]See 48.2.4.2

occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

To communicate LPI, LPI control character /LI/ is sent continuously in place of /I/. LPI control characters are transmitted when LPI control characters are received from the XGMII. LPI characters may be added or deleted by the PCS to adapt between clock rates in a similar manner to idle control characters. /LI/ insertion and deletion shall occur in groups of 4. /LI/s may only be added following other LPI characters.

Change 49.2.6 for scrambler bypass

49.2.6 Scrambler

The payload of the block is scrambled with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 49–5. This implements the scrambler polynomial:[1]

$$'(x) = 1 + x^{39} + x^{58} \quad (49–1)$$

There is no requirement on the initial value for the scrambler. The scrambler is run continuously on all payload bits. The sync header bits bypass the scrambler.

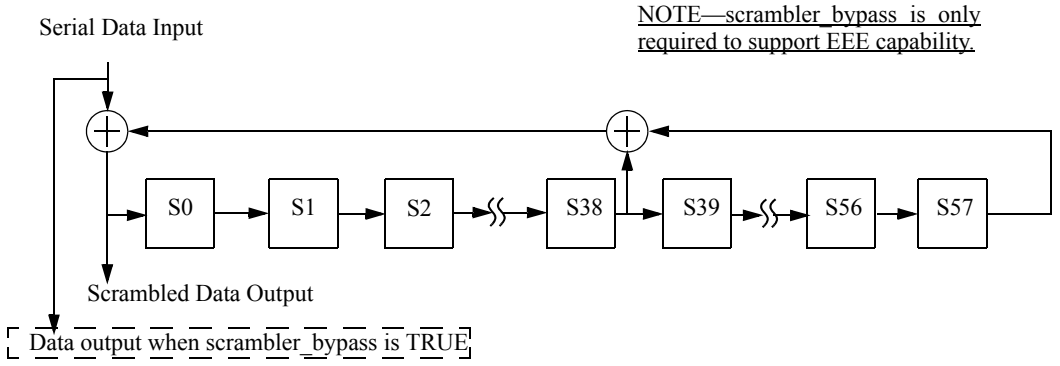


Figure 49–5—Scrambler

[1]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (49–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

To aid block synchronization in the receiver for EEE capability when Clause 74 FEC is in use, when scrambler_bypass is TRUE the PCS shall pass the unscrambled data from the scrambler input rather than the scrambled data from the scrambler output. The scrambler shall continue to advance normally.

Change 49.2.9 and Fig 49-12 for LPI override of synchronization

49.2.9 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 16-bit PMA_UNITDATA.request or WIS_UNITDATA.request primitives. It shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state diagram shown in Figure 49–12.

If EEE is not supported then block_lock is identical to rx_block_lock. Otherwise the relationship between block_lock and rx_block_lock is given by Figure 49–15 the LPI receive state diagram.

Change Figure 49–13 for BER monitor

Insert a note in 49.2.13.2.2 below the definition for "block_lock"

NOTE: If the EEE capability is supported, then this variable is affected by the LPI receive state diagram. If the EEE capability is not supported then this variable is identical to rx_block_lock controlled by the lock state diagram.

Insert new variables into 49.2.13.2.2, insert the new text at the end of the existing subclause.

49.2.13.2.2 Variables

The following variables are used only for the EEE capability.

energy_detect
: A Boolean variable sent from the PMD that is set to TRUE when signal energy is detected at the receiver and is set to FALSE otherwise

rx_block_lock
: Variable used by the lock state diagram to reflect the status of the code-group delineation. This variable is set TRUE when the receiver acquires block delineation.

rx_lpi_active
: A Boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

rx_mode
: A variable set to QUIET while the receiver is in the RX_QUIET state and is set to DATA otherwise

tx_mode
: A variable set to QUIET when the transmitter is in the TX_QUIET state, set to ALERT when the transmitter is in the TX_ALERT state and set to DATA otherwise. When set to QUIET, the PMD disables the transmitter as described in 72.6.5. When set to ALERT, the PMD transmits a repeating pattern of eight ones and eight zeroes as described in 72.6.2. When set to DATA the PMD passes data as normal.

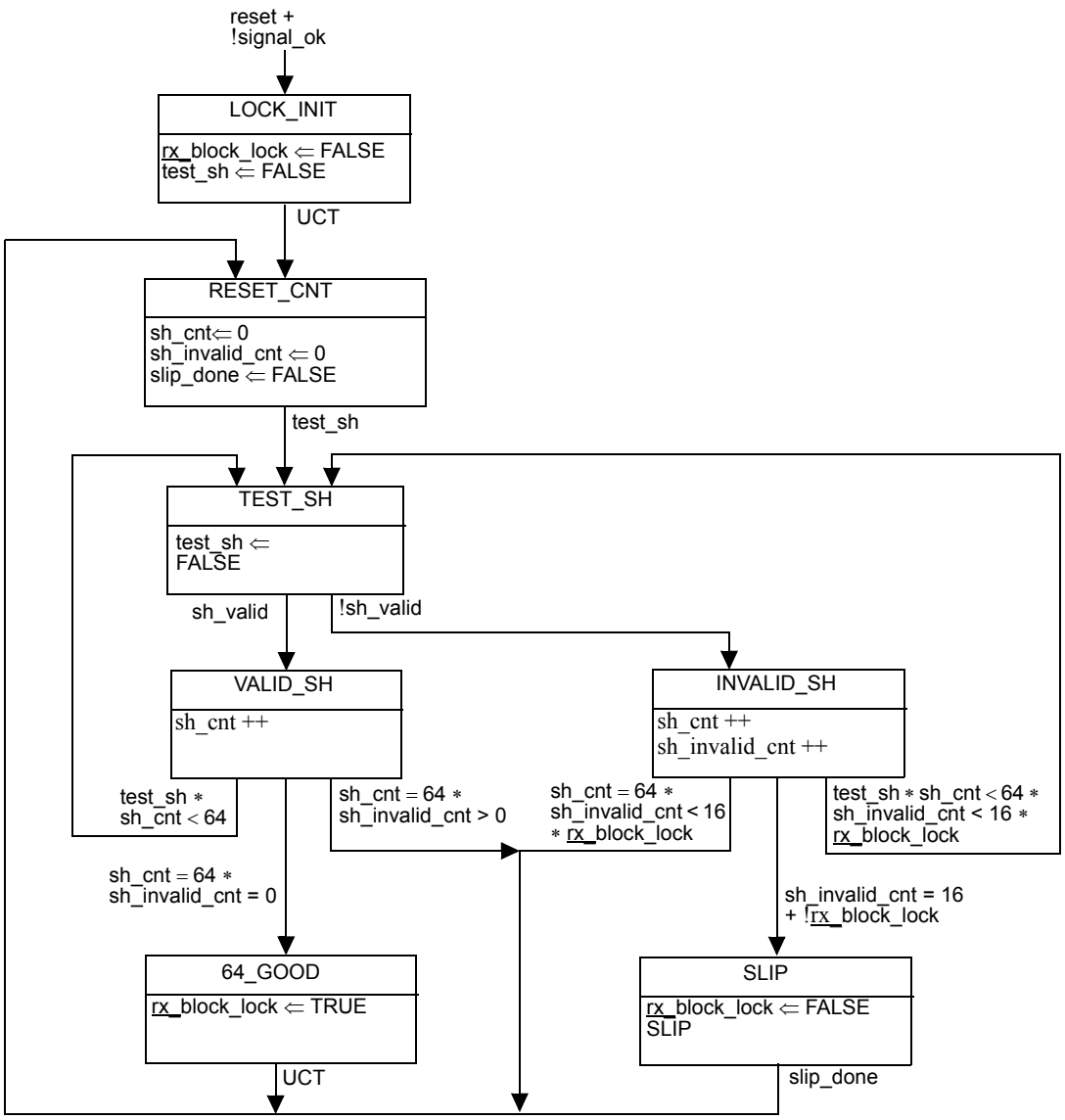


Figure 49–12—Lock state diagram

scrambler_bypass

This Boolean variable is used to bypass the Tx PCS scrambler in order to assist rapid synchronization following low power idle. When set to TRUE, the PCS will pass the unscrambled data from the scrambler input rather than the scrambled data from the scrambler output. The scrambler will continue to operate normally shifting input data into the delay line. When scrambler_bypass is set to FALSE the PCS will pass scrambled data from the scrambler output.

scr_bypass_enable

A Boolean variable used to indicate to the transmit LPI state diagram that the scrambler bypass option is required. The PHY shall set scr_bypass_enable = TRUE if Clause 74 FEC is in use. The PHY shall set scr_bypass_enable = FALSE if this FEC is not in use.

Change 49.2.13.2.3 function definitions for LPI block types

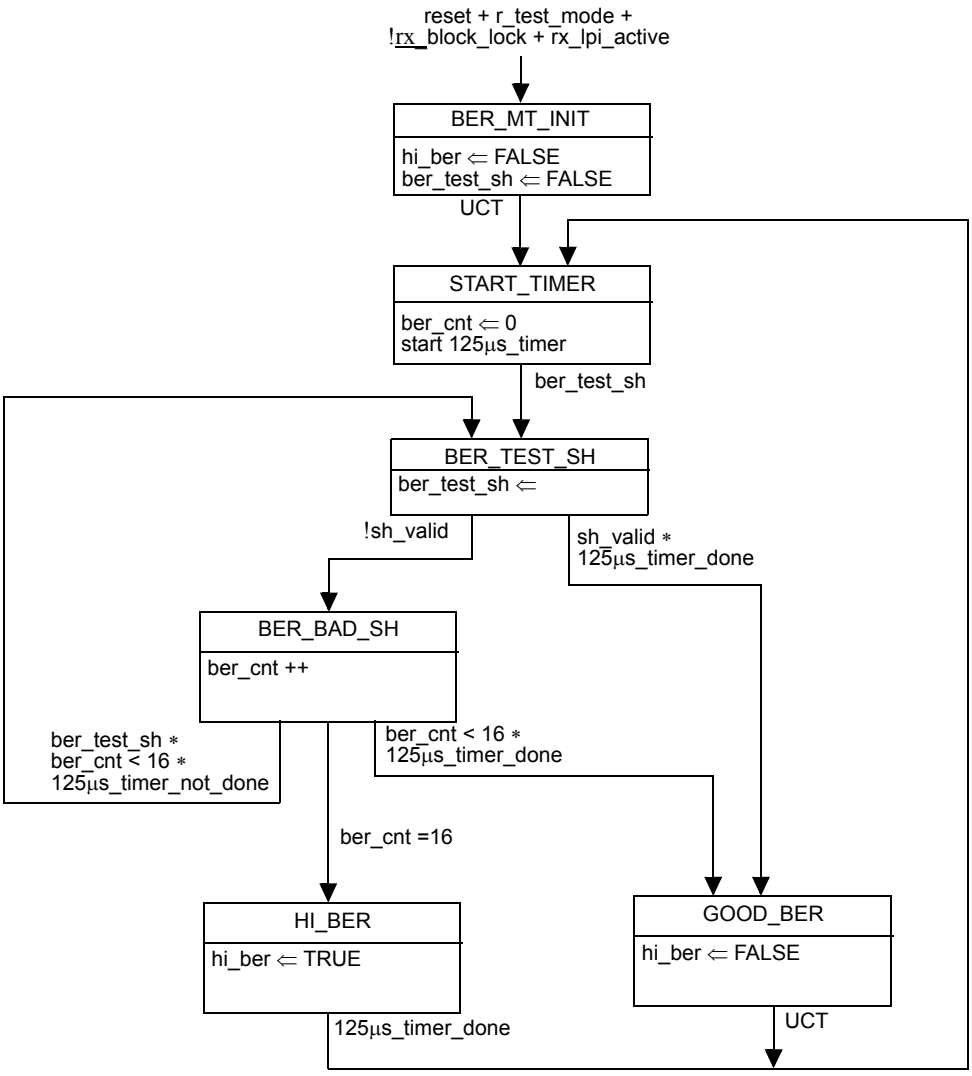


Figure 49–13—BER monitor state diagram

49.2.13.2.3 Functions

DECODE(rx_coded<65:0>)

Decodes the 66-bit vector returning rx_raw<71:0> which is sent to the XGMII. The DECODE function shall decode the block as specified in 49.2.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<63:0> is sent to the scrambler. The two high order sync bits bypass the scrambler. The ENCODE function shall encode the block as specified in 49.2.4.

R_BLOCK_TYPE = {C, S, T, D, E, LI}

This function classifies each 66-bit rx_coded vector as belonging to one of the ~~five~~ following types depending on its contents.

Values: C; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x1e and eight valid control characters other than /E/ and, if the EEE capability is supported, zero or four of the characters are /LI/;
b) A block type field of 0x2d or 0x4b, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.
LI; For EEE capability, the LI type is supported where the vector contains a sync header of 10, a block type field of 0x1e and eight control characters of 0x06 (/LI/).
S; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.
T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xaa, 0xb4, 0xcc, 0xd2, 0xe1 or 0xff and all control characters are valid.
D; The vector contains a sync header of 01.
E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-R control code specified in Table 49–1. A valid O code is one containing an O code specified in Table 49–1.
Note: A PCS that does not support EEE, classifies vectors containing one or more /LI/ control characters as type E.

R_TYPE(rx_coded<65:0>)
Returns the R_BLOCK_TYPE of the rx_coded<65:0> bit vector.

R_TYPE_NEXT
Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP
Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E, LI}
This function classifies each 72-bit tx_raw vector as belonging to one of the ~~five~~ following types depending on its contents.

Values: C; The vector contains one of the following:
a) eight valid control characters other than /O/, /S/, /T/, /E/ and, if the EEE capability is supported, zero or four of the characters are /LI/;
b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;
c) two valid ordered sets.
LI; For EEE capability, this vector contains eight /LI/ characters.
S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 49–1. A valid ordered_set con-

sists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 49–1.
Note: A PCS that does not support EEE, classifies vectors containing one or more /LI/ control characters as type E.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

Insert new counters into 49.2.13.2.4, new timers into 49.2.13.2.5 in support of the LPI state diagrams. In each case, insert the new text at the end of the existing subclause.

49.2.13.2.4 Counters

The following counter is used only for the EEE capability.

wake_error_counter
A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.8b)

49.2.13.2.5 Timers

The following timers are used only for the EEE capability.

one_us_timer
A timer used to count approximately 1 μs intervals. The timer terminal count is set to T_{1U}. When the timer reaches terminal count it will set the one_us_timer_done = TRUE.

rx_tq_timer
This timer is started when the PCS receiver enters the RX_SLEEP state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall be set to a value no larger than the maximum value given for T_{WR} in Table 49–3. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the QUIET state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SI}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QI}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tw_timer

This timer is started when the PCS transmitter enters the TX_WAKE state. The timer terminal count is set to T_{WL}. When the timer reaches terminal count it will set the tx_tw_timer_done = TRUE.

Change Figure 49-14 for LPI transmit state diagram and 49-15 for LPI receive state diagram; change the final paragraph of 49.2.13.3:

49.2.13.3 State diagrams

The PCS shall perform the functions of Lock, BER Monitor, Transmit and Receive as specified in these state diagrams, including the optional EEE capability if implemented.

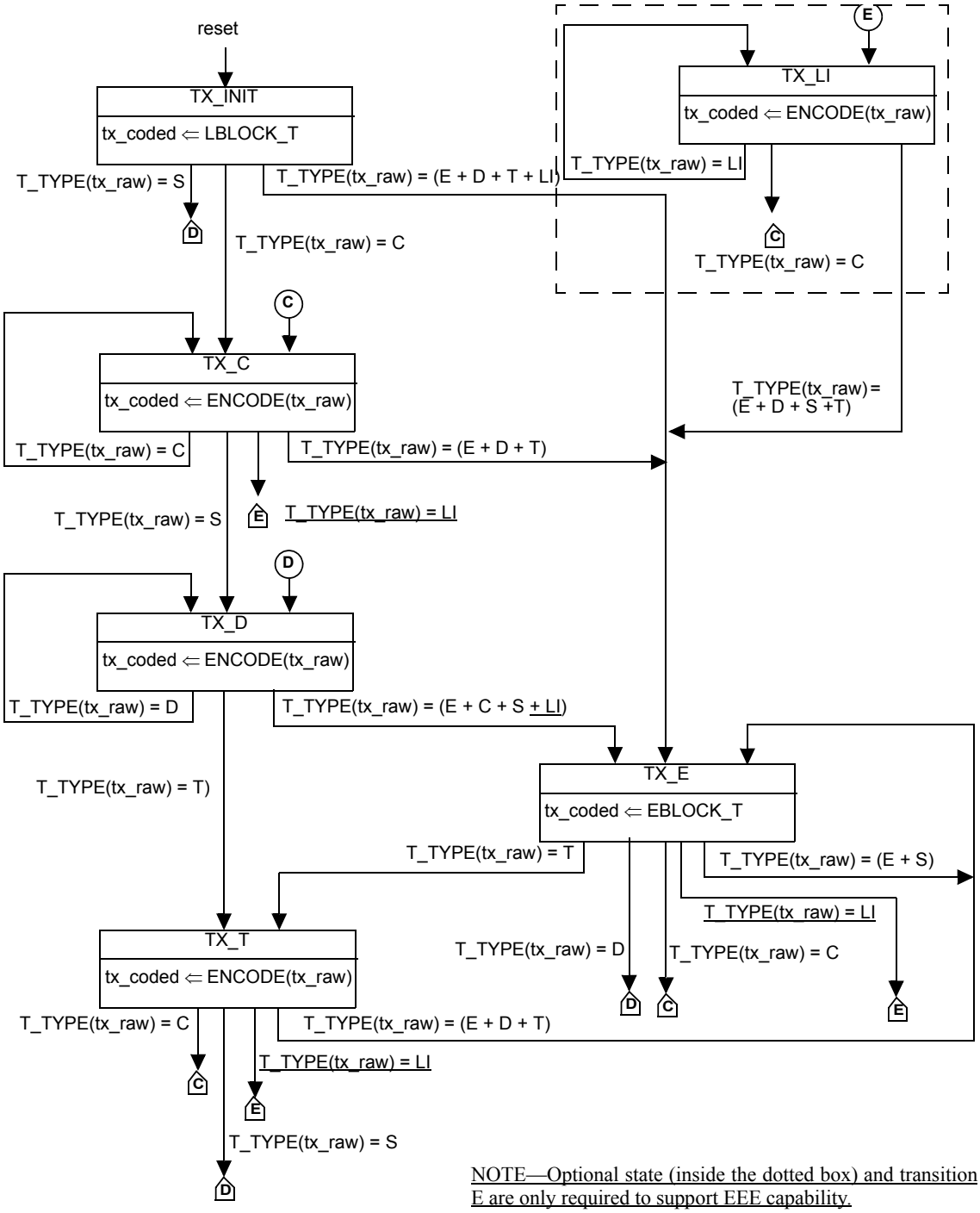


Figure 49–14—Transmit state diagram

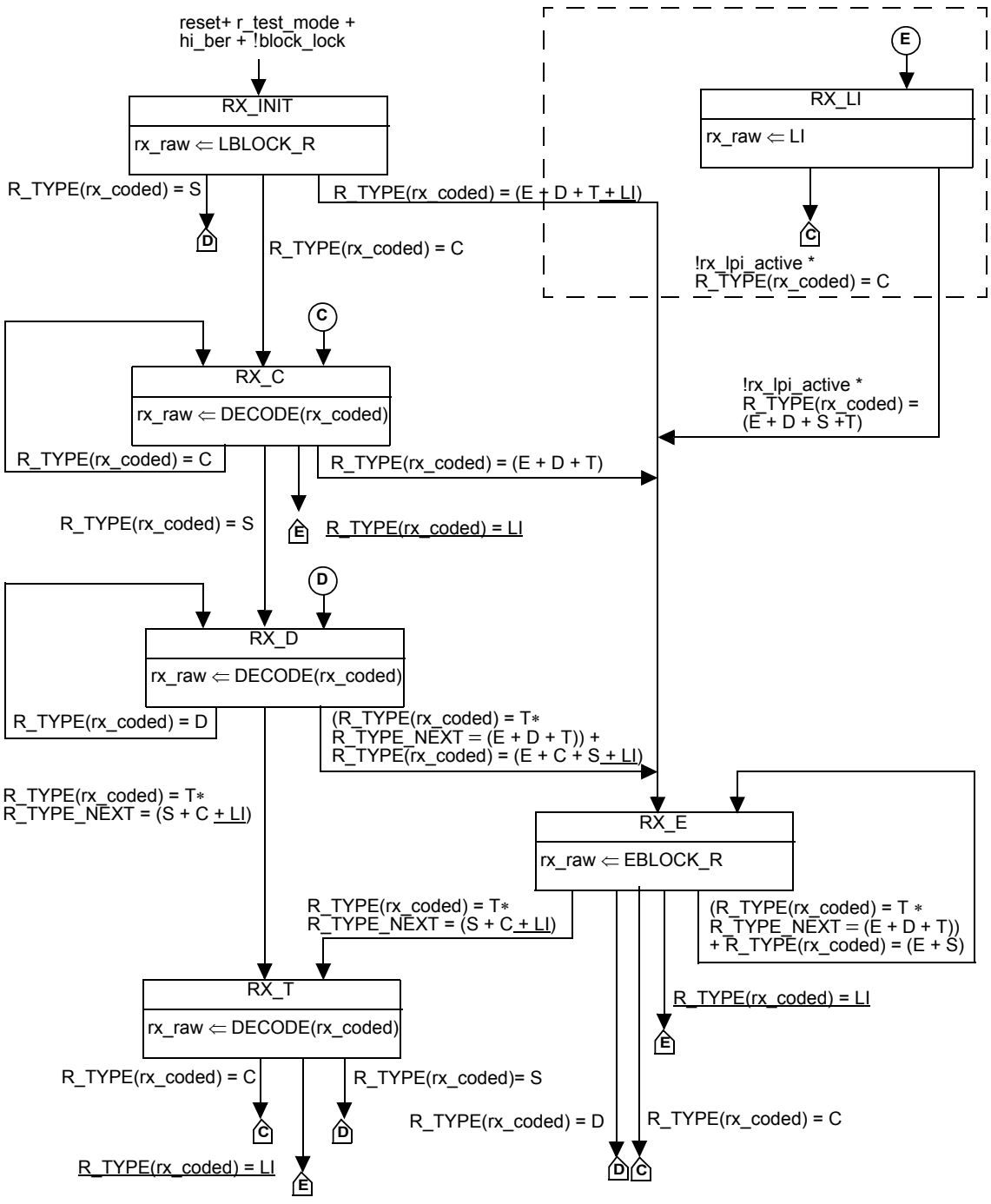


Figure 49–15—Receive state diagram

Insert 49.2.13.3.1 at the end of 49.2.13.3

49.2.13.3.1 LPI state diagrams

A PCS which supports the EEE capability shall implement the LPI transmit and receive processes as shown in figures 49–16 and 49–17. The transmit LPI state diagram controls tx_mode which disables the transmitter when it is set to QUIET. The receive LPI state diagram controls block_lock during LPI and signals the end of LPI to the receive state diagram.

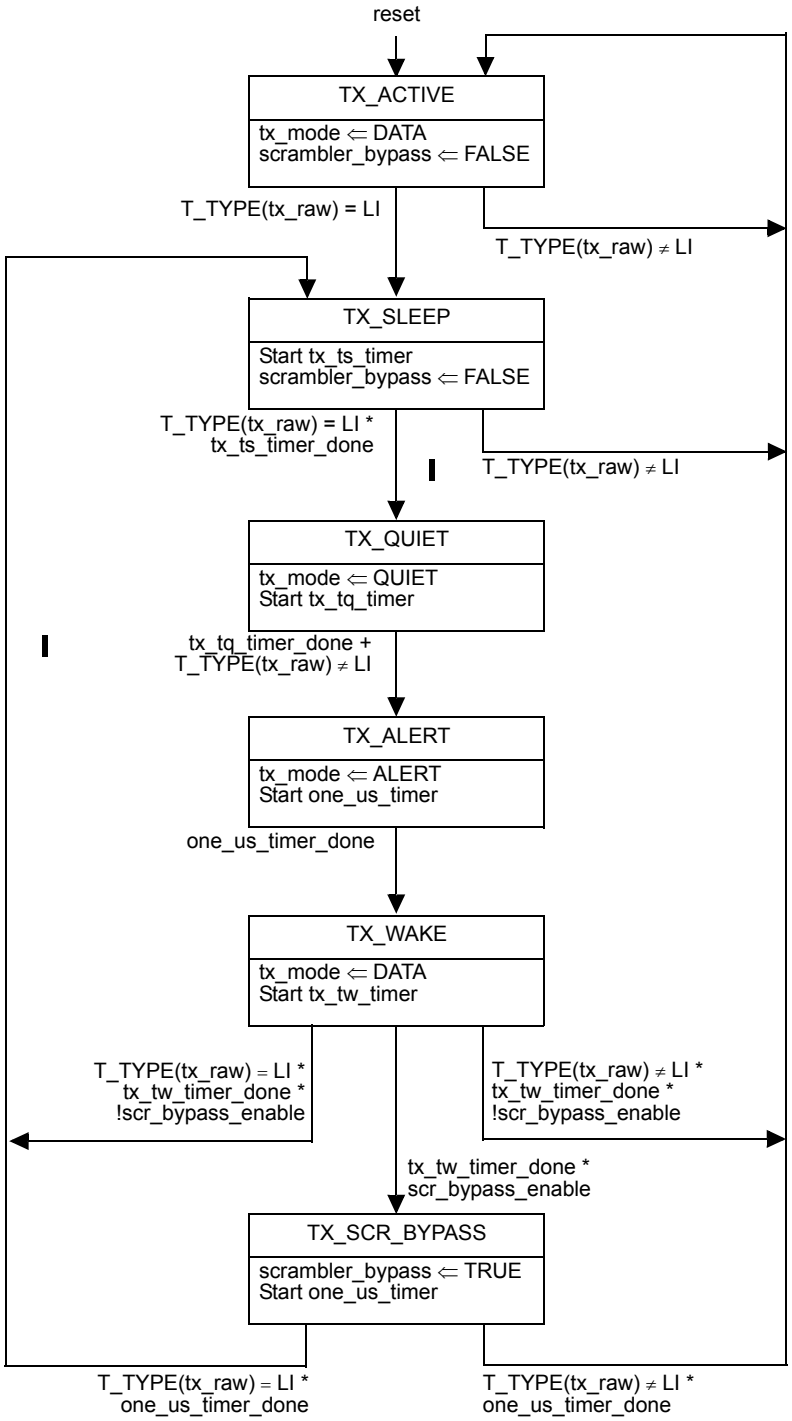


Figure 49–16—LPI Transmit state diagram

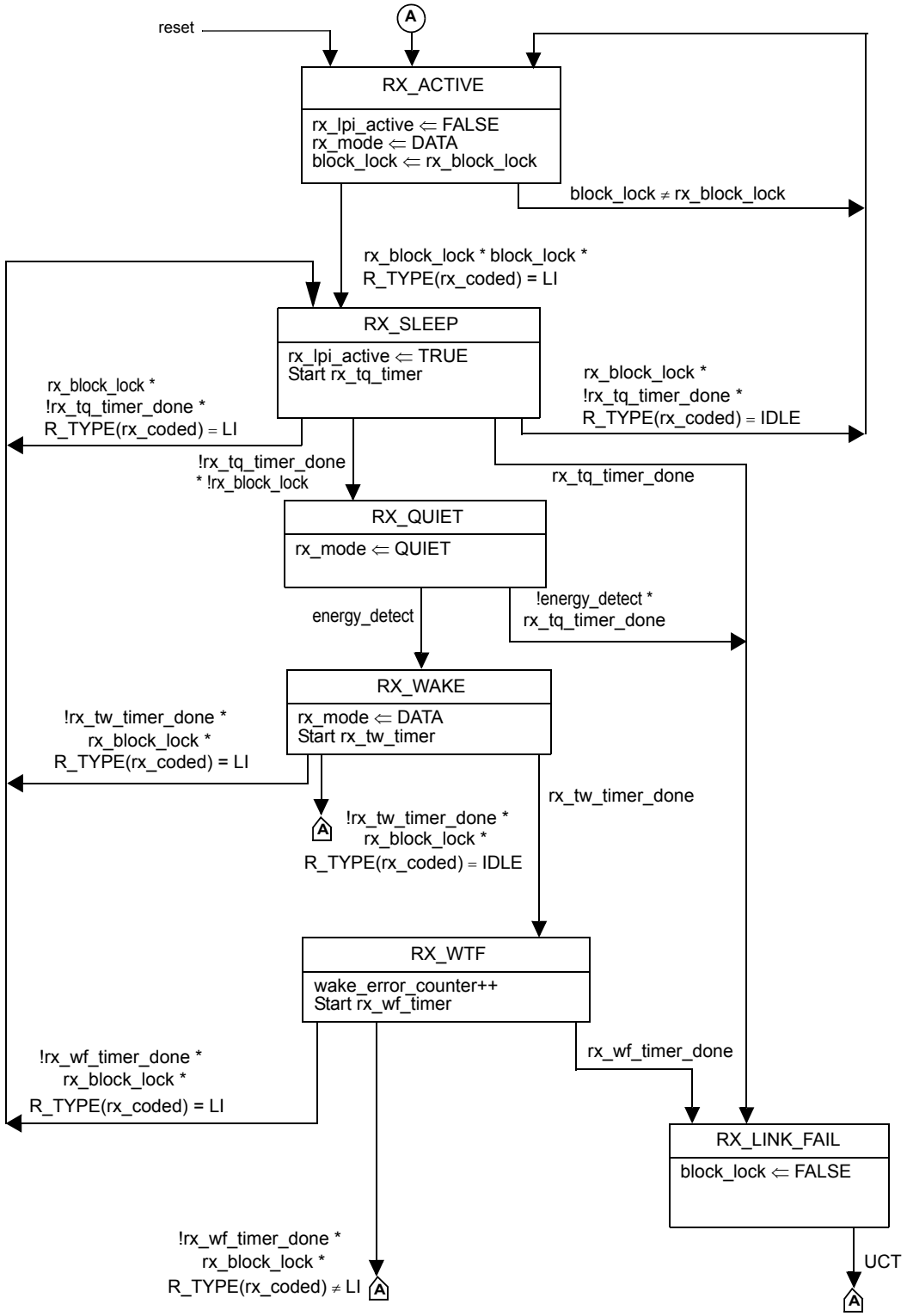


Figure 49–17—LPI Receive state diagram

Following a period of LPI, the receiver is required to achieve block synchronization within the wakeup time specified (See Figure 49–17). The implementation of the block synchronization state diagram should use techniques to ensure that block lock is achieved with minimal numbers of slip attempts. When the Clause 74 FEC is enabled, the receiver may use the knowledge that the link partner's transmitter will bypass the scrambler as part of the wake sequence. The idle sequence following this event will form a fixed pattern for the duration of the wake period.

The LPI functions shall use timer values for these state diagrams as shown in Table 49–2 for transmit and Table 49–3 for receive.

Table 49–2—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to QUIET	4.9	5.1	µs
T_{QL}	Local Quiet Time from when tx_mode is set to QUIET to entry into the TX_ALERT state	1.7	1.8	ms
T_{WL}	Time spent in the TX_WAKE state	10.9	11.1	µs
T_{1U}	Time spent in the TX_ALERT and TX_SCR_BYPASS states	1.1	1.3	µs

Table 49–3—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for energy_detect to be set to TRUE while in the RX_SLEEP and RX_QUIET states before asserting receive fault	2	3	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault. (when scr_bypass_enable = FALSE)		11.5	µs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault. (when scr_bypass_enable = TRUE)		13.7	µs
T_{WTF}	Wake time fault recovery time		10	ms

Change 49.2.14.1 for LPI status:

49.2.14.1 Status

PCS_status:

Indicates whether the PCS is in a fully operational state. It is only TRUE if block_lock is TRUE and hi_ber is FALSE. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_ber:

Indicates the state of the hi_ber variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LPI indication:

For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the LPI receive state diagram is in any state other than RX_ACTIVE. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

Tx LPI indication:

For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the LPI transmit state diagram is in any state other than TX_ACTIVE. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

49.3 Protocol implementation conformance statement (PICS) proforma for Clause 49, Physical Coding Sublayer (PCS) type 10GBASE-R[2]

Insert the following row into table 49.3.3:

49.3.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	49.2.4.4		O	Yes [ ] No [ ]

Insert the new subclause 49.3.6.6 after 49.3.6.5 for LPI functions:

49.3.6.6 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Insertion and deletion of LPIs in groups of 4	49.2.4.7		LPI:M	Yes [ ] No [ ]
LP-02	Unscrambled data transmitted when scrambler_bypass = TRUE	49.2.6		LPI:M	Yes [ ] No [ ]
LP-03	Scrambler continues to operate as normal when scrambler_bypass = TRUE	49.2.6		LPI:M	Yes [ ] No [ ]
LP-04	scr_bypass_enable = TRUE when FEC is in use	49.2.13.2.2		LPI:M	Yes [ ] No [ ]
LP-05	Transmit state diagrams	49.2.13.3	Support additions to Figure 49–14 for LPI operation	LPI:M	Yes [ ] No [ ]
LP-06	Receive state diagrams	49.2.13.3	Support additions to Figure 49–15 for LPI operation	LPI:M	Yes [ ] No [ ]
LP-07	LPI transmit state diagrams	49.2.13.3.1	Meets the requirements of Figure 49–16	LPI:M	Yes [ ] No [ ]
LP-08	LPI receive state diagrams	49.2.13.3.1	Meets the requirements of Figure 49–17	LPI:M	Yes [ ] No [ ]
LP-09	LPI transmit timing	49.2.13.3.1	Meets the requirements of Table 49–2	LPI:M	Yes [ ] No [ ]
LP-10	LPI receive timing	49.2.13.3.1	Meets the requirements of Table 49–3	LPI:M	Yes [ ] No [ ]

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

51. Physical Medium Attachment (PMA) sublayer, type Serial

Change Figure 51–3 for EEE signals across XSBI.

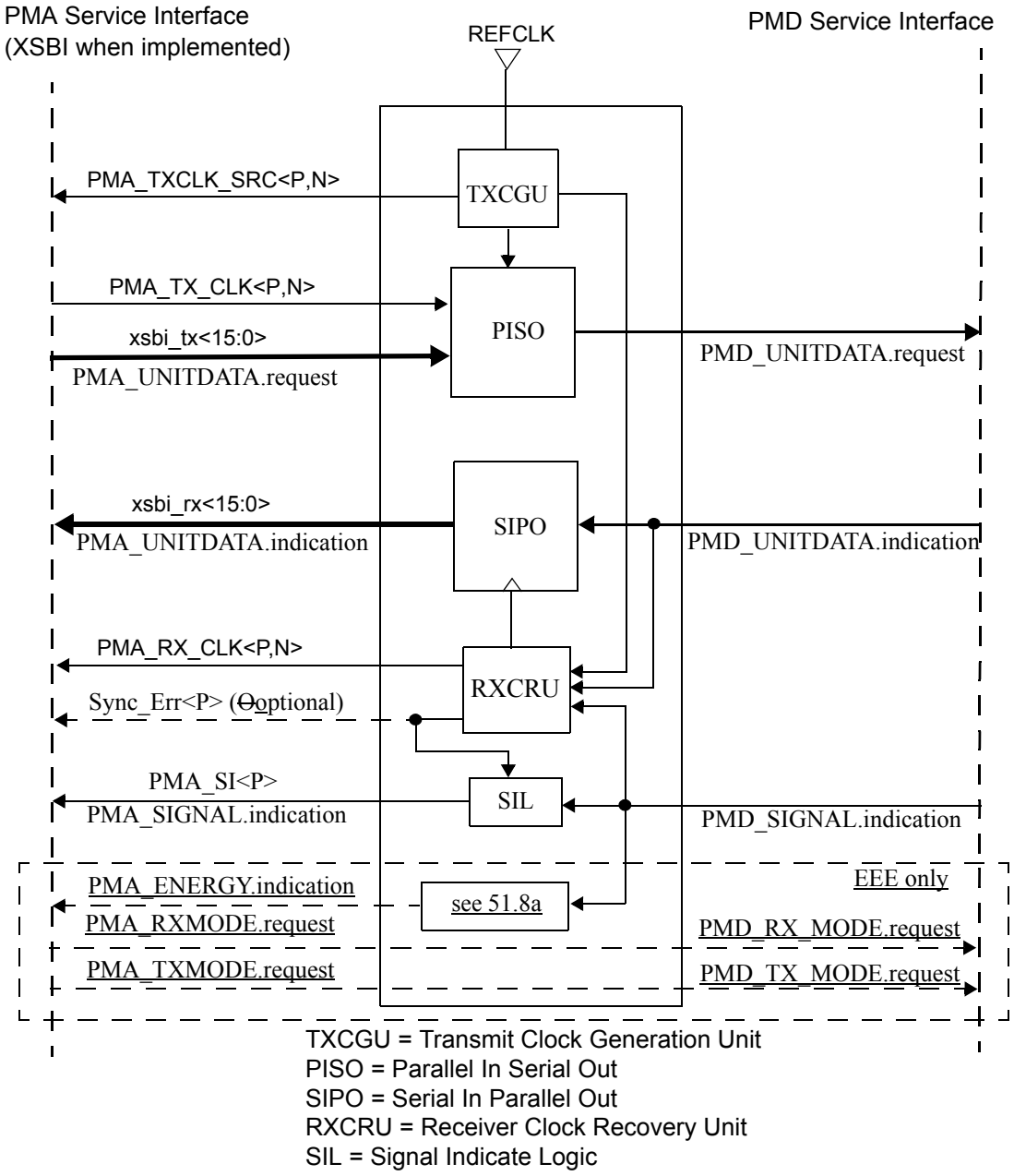


Figure 51–3—XSBI reference diagram

Insert primitives into 51.2 and add subclauses 51.2.4 through 51.2.6 after 51.2.3

51.2 PMA Service Interface

PMA_RXMODE.request(rx_mode)

PMA_TXMODE.request(tx_mode)

PMA_ENERGY.indication(energy_detect)

51.2.4 PMA_RXMODE.request

This primitive is generated by the PCS Receive Process for EEE capability (see 78.3) to indicate when the PMA and PMD receive functions may go into a low power mode, see 49.3.6.6. Without EEE capability, the primitive is never invoked and the PMA behaves as if rx_mode = DATA.

51.2.4.1 Semantics of the service primitive

PMA_RXMODE.request(rx_mode)

The rx_mode parameter takes on one of two values: QUIET or DATA.

51.2.4.2 When generated

The PCS generates this primitive to indicate the low power mode of the receive path.

51.2.4.3 Effect of receipt

When received the PMA receive is configured appropriately for the indicated state and the value is propagated to PMD_RX_MODE.request(rx_mode). When rx_mode is DATA the PMA operates normally. When rx_mode is QUIET, the PMA may go into a low power mode.

51.2.5 PMA_TXMODE.request

This primitive is generated by the PCS Transmit Process for EEE capability to invoke the appropriate PMA and PMD transmit EEE states, see 49.2.13.3.1. Without EEE capability, the primitive is never invoked and the PMA behaves as if tx_mode = DATA.

51.2.5.1 Semantics of the service primitive

PMA_TXMODE.request(tx_mode)

The tx_mode parameter takes on one of three values: QUIET, ALERT or DATA.

51.2.5.2 When generated

The PCS generates this primitive to indicate the low power mode of the transmit path.

51.2.5.3 Effect of receipt

When received the PMA transmit is configured appropriately for the indicated state and the value is propagated to PMD_TX_MODE.request(tx_mode). When tx_mode is DATA the PMA operates normally. When tx_mode is QUIET, the PMA may go into a low power mode. When tx_mode is ALERT, the PMA operation is not defined.

51.2.6 PMA_ENERGY.indicate

This primitive is sent by the PMA to its client to indicate the status of the receive process for EEE capability. PMA_ENERGY.indication is generated by the PMA receive process to propagate the energy detection indication from the PMD to the PMA client.

51.2.6.1 Semantics of the service primitive

PMA_ENERGY.indication(energy_detect)

The energy_detect parameter is boolean and reflects the state of the PMD_SIGNAL.indication(SIGNAL_OK) received from the PMD.

51.2.6.2 When generated

The PMA generates this primitive whenever there is a change in the value of the SIGNAL_OK parameter.

51.2.6.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

Insert new optional signals into 51.4.2

51.4.2 Optional Signals

energy_detect
: If the optional Energy Efficient Ethernet (EEE) function is supported (see Clause 78) then the XSBI interface includes energy_detect as described in 51.2.

rx_quiet
: If the optional EEE function is supported (see Clause 78) then the XSBI interface includes rx_quiet as described in 51.2.

tx_quiet
: If the optional EEE function is supported (see Clause 78) then the XSBI interface includes tx_quiet as described in 51.2.

51.10 Protocol implementation conformance statement (PICS) proforma for Clause 51, Physical Medium Attachment (PMA) sublayer, type Serial[1]

Insert the following row at the end of the table in 51.10.3:

51.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	51.2		O	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.1 Overview

Insert the following text after the last paragraph of 55.1:

This clause also specifies 10GBASE-T Low Power Idle (LPI) as part of Energy Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78. 10GBASE-T PHYs may optionally support a fast retrain mechanism.

55.1.1 Objectives

Insert the following objective to the end of the list as follows:

l) Support a EEE capability as part of Energy Efficient Ethernet (Clause 78)

55.1.3 Operation of 10GBASE-T

Insert the following text before the last paragraph of 55.1.3

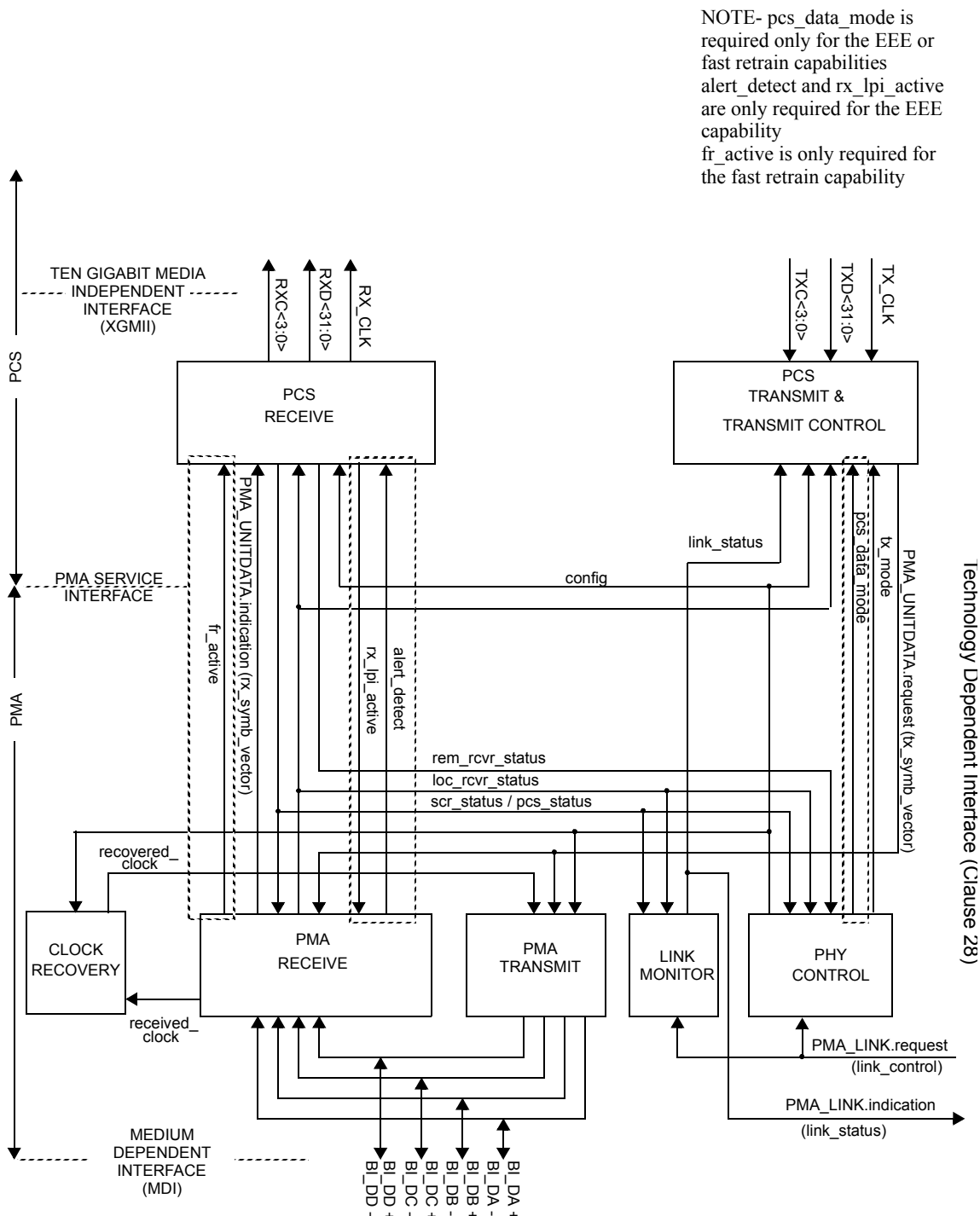
10GBASE-T PHYs optionally provide support for LPI as part of EEE (see Clause 78). This extension allows PHYs to enter an LPI mode when either the local or link partner system requests low power operation. The transmit and receive functions may enter and leave the LPI mode independently so that both symmetric and asymmetric operation is supported. While the PHY is in the LPI mode the PHY periodically transmits a refresh signal to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. An easily detectable alert signal is transmitted to signal an end to the LPI mode. The alert signal is followed by a wake signal to enable a rapid transition back to the normal operational mode.

10GBASE-T PHYs may optionally support a fast retrain mechanism. This function allows PHYs to quickly recover from link degradation without a normal two second retrain.

Change the last paragraph of 55.1.3 by inserting the sentence as shown below:

The PCS and PMA subclauses of this document are summarized in 55.1.3.1 and 55.1.3.2. The EEE capability is summarized in 55.1.3.3. Figure 55–3 shows the functional block diagram.

Replace Figure 55-3 with the figure shown below



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

Figure 55–3—Functional block diagram

55.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA sublayer may also support a fast retrain function. The fast retrain function is specified in 55.4.2.5.15.

Insert 55.1.3.3 after 55.1.3.2 as shown below:

55.1.3.3 EEE capability

A 10GBASE-T PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 10GBASE-T PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after reaching PCS data mode. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full-duplex link is in a period of low utilization. No data frames are lost or corrupted during the transition to or from the LPI mode.

In the transmit direction the transition to the LPI transmit mode begins when the PCS transmit function detects an LPI control character in all four lanes of two consecutive transfers of TXD[31:0] that will be mapped into a single 64B/65B block. Following this event a sleep signal is transmitted by the PMA. The sleep signal is composed of LDPC frames that contain only LP_IDLE 64B/65B blocks. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep frames the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. The LPI mode begins with quiet signaling or with a full refresh period. Partial refreshes (defined as a refresh signal shorter than 4 LDPC frames) that immediately follow the transition to the LPI mode are replaced with quiet signaling. The quiet-refresh cycle continues until the PCS function detects IDLE characters on the XGMII. These characters signal to the PHY that the LPI transmit mode should end. The PMA Transmit function in the PHY then sends an alert message to the link partner. The alert signal begins on a LDPC frame boundary, but has no fixed relationship to the quiet/refresh cycle. The alert signal wakes the link partner from sleep. The alert signal is followed by a wake signal, composed of LDPC frames containing only IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the LPI mode is triggered when the PCS Receive function detects LPI control characters within received LDPC frames. This indicates that the link partner is about to enter the LPI transmit mode. Following these frames the link partner ceases transmission and begins quiet-refresh signaling. During the quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the normal operational mode. The alert signal is detected in the PMA and signals that normal data frames will follow. The alert signal is followed by a wake signal that allows the local receiver time to prepare for the normal operational mode. The wake signal is composed of repeated IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

Support for the EEE capability is advertised during Auto-Negotiation. Transitions to and from the LPI transmit mode are controlled via XGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep, alert and wake signaling.

The PCS 64B/65B Transmit state diagram in Figure 55–15 and Figure 55–15a includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 55–16 and Figure 55–16a includes additional states for EEE. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 55–16b.

55.1.4 Signaling

Change the list of objectives by inserting item l as shown below:

10GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to four-dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four-dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation

Insert the following text at the end of the last paragraph in 55.1.4 as shown below:

PHYs may also support the EEE capability as described in 55.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

Insert the following text at the end of the last paragraph in 55.2.2 as shown below:

EEE capable PHYs additionally support the following service primitives:

PMA_ALERTDETECT.indication (alert_detect)

PCS_RX_LPI_STATUS.request (rx_lpi_active)

PMA_PCSDATAMODE.indication (pcs_data_mode)

Fast retrain capable PHYs additionally support the following service primitive:

PMA_FR_ACTIVE.indication (fr_active)

Replace the existing Figure 55-4 with the figure shown below.

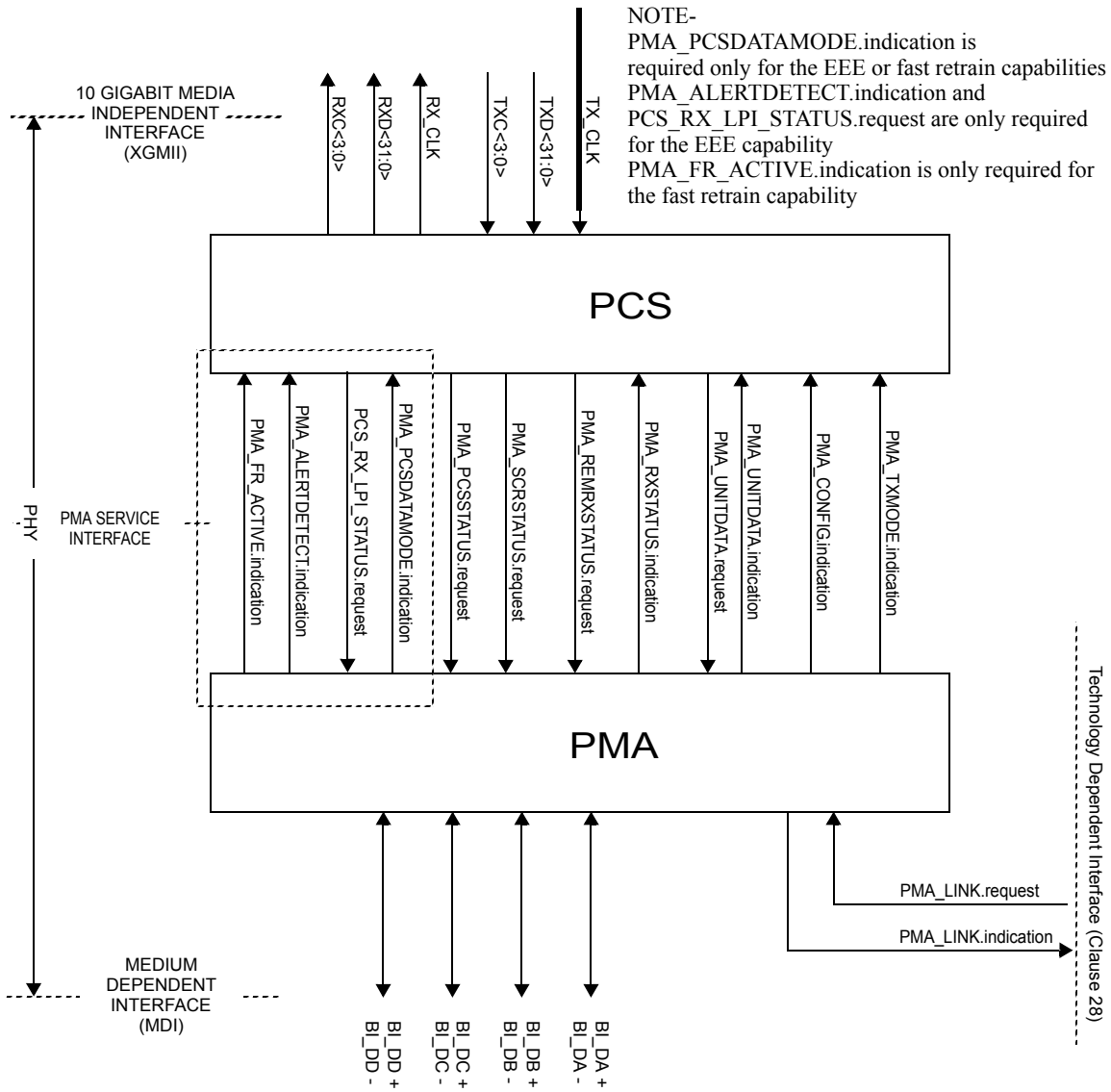


Figure 55–4—10GBASE-T service interfaces

55.2 10GBASE-T service primitives and interfaces

55.2.2.3.1 Semantics of the primitive

Change the tx_sym_vector parameter options in 55.2.2.3.1 as shown below:

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. For EEE capable PHYs, the vector also requests the PMA to send the ALERT signal during LPI. The tx_symb_vector parameter takes on the form:

SYMB_4D	A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. In normal operation each symbol may take on one of the values in the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The symbols may additionally take the value 0 when zeros are to be transmitted in the two cases: i) when PMA_TXMODE.indication is SEND_Z during PMA training ii) after data mode is reached, the transmit function is in the LPI transmit mode and lpi_tx_mode is QUIET
ALERT	A vector used to indicate that the PMA should transmit the alert sequence. ALERT will be asserted for a time equal to 4 LDPC frames.

Insert 55.2.2.9, 55.2.2.10, 55.2.2.11 and 55.2.2.12 after section 55.2.2.8 as shown below:

55.2.2.9 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is TRUE. The parameter alert_detect conveys to the PCS receive function information regarding the detection of the LPI alert signal by the PMA receive function. The criterion for setting the parameter alert_detect is left to the implementor.

55.2.2.9.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of two values of the form:

TRUE	The alert signal has been reliably detected at the local receiver
FALSE	The alert signal at the local receiver has not been detected.

55.2.2.9.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

55.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Clause 55.3.2.3, Figure 55–16 and Figure 55–16a.

55.2.2.10 PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode. The parameter is generated by the Receive 64B/65B state diagram in Figure 55-16.

55.2.2.10.1 Semantics of the primitive

PCS_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

TRUE	The receive function is in the LPI receive mode
FALSE	The receive function is not in the LPI receive mode

55.2.2.10.2 When generated

The PCS generates PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as determined by the receive state diagram in Figure 55-16.

55.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.3.2.3 and Figure 55–27a.

55.2.2.11 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

55.2.2.11.1 Semantics of the primitive

PMA_PCSDATAMODE.indication (pcs_data_mode)

55.2.2.11.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

55.2.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 55.3.2.2.

55.2.2.12 PMA_FR_ACTIVE.indication

This primitive indicates whether or not the PMA is currently performing a fast retrain. The fr_active variable is generated by the PMA PHY Control function. It is passed to the PCS Receive Control function via the PMA_FR_ACTIVE.indication primitive. This primitive is only supported by PHYs with the fast retrain capability.

55.2.2.12.1 Semantics of the primitive

PMA_FR_ACTIVE.indication (fr_active)

55.2.2.12.2 When generated

The PMA PHY Control function generates PMA_FR_ACTIVE.indication messages continuously.

55.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–16.

55.3 Physical Coding Sublayer (PCS)

55.3.2 PCS Functions

Replace the existing Figure 55-5 with the figure shown below.

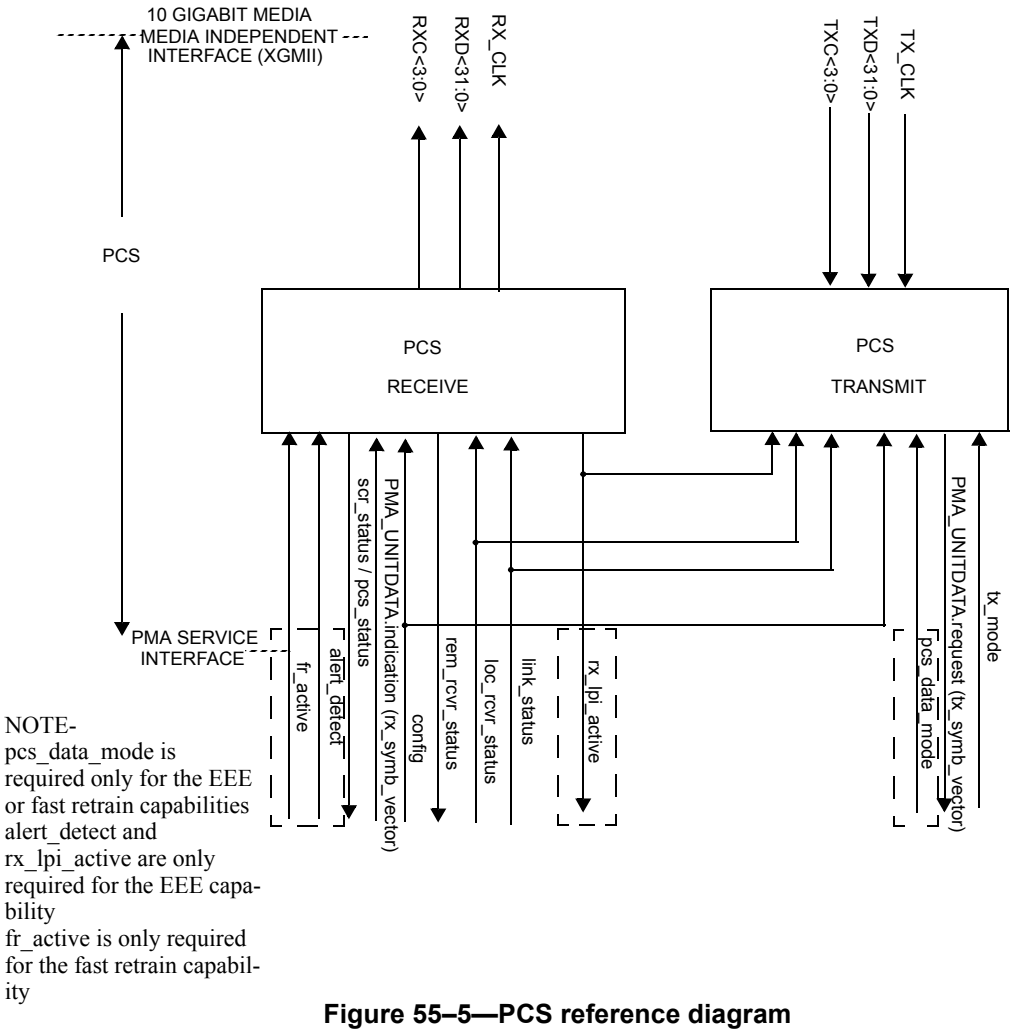


Figure 55–5—PCS reference diagram

55.3.2.2 PCS Transmit function

Insert the following text after the first paragraph in 55.3.2.2

Dashed rectangles in Figure 55–15 and Figure 55–15a are used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

Insert the following text after the last paragraph in 55.3.2.2

After reaching the normal mode of operation, EEE capable PHYs may enter the LPI transmit mode under the control of the MAC via the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 55.3.2.2.21

55.3.2.2.1 Use of blocks

Change text in 55.2.2.9.4 as shown below:

The PCS maps XGMII signals into 65-bit blocks inserted into an LDPC frame, and vice versa, using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. During the LPI mode, LDPC frame boundaries delimit sleep, wake, refresh, quiet and alert cycles. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 55.3.2.2.6.

55.3.2.2.9 Idle (/I/)

Remove the existing Control Codes table (55-1) and footnotes and replace them with the table and table footnotes shown below.

Table 55–1—Control Codes

Control character	Notation	XGMII Control codes	10GBASE-T Control codes	10GBASE-T O code	8B/10B code[a]
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5 without D20.5[b]
LPI	/LI/	0x06	0x06		K28.0 or K28.3 or K28.5 with D20.5[b]
start	/S/	0xFB	Encoded by block type field		K27.7
terminate	/T/	0xFD	Encoded by block type field		K29.7
error	/E/	0xFE	0x1E		K30.7
Sequence ordered_set	/Q/	0x9C	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/[c]	0x1C	0x2D		K28.0
reserved1		0x3C	0x33		K28.1
reserved2	/A/	0x7C	0x4B		K28.3
reserved3	/K/	0xBC	0x55		K28.5
reserved4		0xDC	0x66		K28.6
reserved5		0xF7	0x78		K23.7
Signal ordered_set[d]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF	K28.2

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.
[b]Use of idle and LPI ordered sets per 48.2.4.2
[c]The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.
[d]Reserved for INCITS T11 Fibre Channel use.

Insert 55.3.3.3.9a LPI (/LI/) as shown:

55.3.2.2.9a LPI (/LI/)

Low power idle (LPI) control characters (/LI/) on the XGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. EEE compliant PHYs respond to the LPI XGMII control characters using the procedure outlined in 55.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of 4. /LI/s may be added following low power idle characters. They shall not be added while data is being received.

If EEE is not supported, then /LI/ is not a valid control character.

Insert text shown as a new subclause 55.3.2.2.21 after the existing subclause 55.3.2.2.20:

55.3.2.2.21 EEE capability

The optional 10GBASE-T EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low.

EEE compliant PHYs shall implement the EEE transmit state diagram, shown in Figure 55–16b, within the PCS.

When PCS_Reset is asserted or pcs_data_mode is not asserted the state diagram enters the TX_NORMAL state.

When a complete 64B/65B block of LPI characters is generated by the PCS transmit function, the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the LPI transmit mode. If the sleep signal begins on an LDPC frame boundary, then it contains 9 full LDPC frames each composed entirely of 64B/65B LDPC-encoded LP_IDLE blocks. If the sleep signal does not begin on an LDPC frame boundary, then it contains one LDPC frame partially composed of LP_IDLE blocks followed by 9 LDPC frames fully composed of LP_IDLE blocks.

Following the transmission of the sleep signal, quiet/refresh signaling begins, as described in 55.3.4a.

After the sleep signal is transmitted LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit Function exits the LPI transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive as described below:

When the PHY is not in the PCS_Data state the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value NORMAL and the PMA asserts SEND_N the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive as described in 55.3.2.2.

When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH_A and the PMA asserts SEND_N the PCS passes the PMA training signal to the PMA on pair A, to allow both the local and remote PHY to refresh adaptive filters and timing loops. The PCS passes zeros to all other pairs in this condition. REFRESH_B, REFRESH_C and REFRESH_D operate in a analogous manner for the other pairs.

When the lpi_tx_mode variable takes the value ALERT and the PMA asserts SEND_N the PCS passes the ALERT vector to the PMA.

The quiet-refresh cycle is repeated until codewords other than LP_IDLE are detected at the XGMII. These codewords indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request message is set to the value ALERT. The alert signal is not synchronized with respect to the refresh/quiet cycle but shall be synchronized so that the alert signal from the PMA begins on a LDPC frame boundary.

The PHY will also transition back to the normal operation mode if an error condition occurs. This error condition is defined as the detection of any characters other than LPI or IDLE at the XGMII.

After the alert signal the PCS completes the transition from LPI mode to normal mode by sending a wake signal containing lpi_wake_time LDPC frames composed of IDLE 64B/65B blocks.

lpi_wake_time is a fixed parameter that is defined as 9 LDPC frames as shown in Table 55–1a below. The maximum PHY wake time when wake is requested before sleep has been completely transmitted is 7.36 μs (lpi_wake_timer=T_{w_phy} as defined by Clause 78). The maximum PHY wake time when wake is requested after sleep has been completely transmitted is 4.48 μs.

Table 55–1a—LPI wake time

lpi_wake_time	lpi_wake_timer when wake starts before sleep signal is complete		lpi_wake_timer when wake starts after sleep signal is complete	
(frames)	(frames)	(μs)	(frames)	(μs)
9	23	7.36	14	4.48

55.3.2.3 PCS Receive function

Insert the following text after the existing text in 55.3.2.3:

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 55.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting 9 LDPC frames composed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive XGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses LDPC frame counters to maintain synchronization with the remote PHY, and receives periodic refresh signals that are used to update coefficients so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in subclause 55.3.4a. The quiet/refresh cycle continues until the PMA asserts alert_detect to indicate that the alert signal has been reliably detected. After the alert signal the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the XGMII for 9 LDPC frame periods and then resumes normal operation.

Insert the following subclause after the existing 55.3.4.3 subclause:

55.3.4a LPI signaling

PHYs with the EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates 64B/65B blocks composed entirely of LPI control characters, as described in 55.3.2.2.21. The transmit function of the link partner signals the transition using the sleep signal. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle. The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 124 LDPC frame periods. The quiet period is defined in 55.3.4a.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 4 LDPC frame periods. The refresh period is defined in 55.3.4a.3. A cycle composed of one quiet period and one refresh period is known as a single pair LPI cycle and lasts for a time lpi_qr_time equal to 128 LDPC frame periods. The time taken to complete a quiet-refresh cycle for all four pairs is known as a complete LPI cycle.

lpi_offset, lpi_quiet_time, lpi_refresh_time, lpi_qr_time and lpi_allpairs_qr_time are timing parameters that are integer multiples of the LDPC frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 that is used to ensure refresh signals are appropriately offset by the link partners.

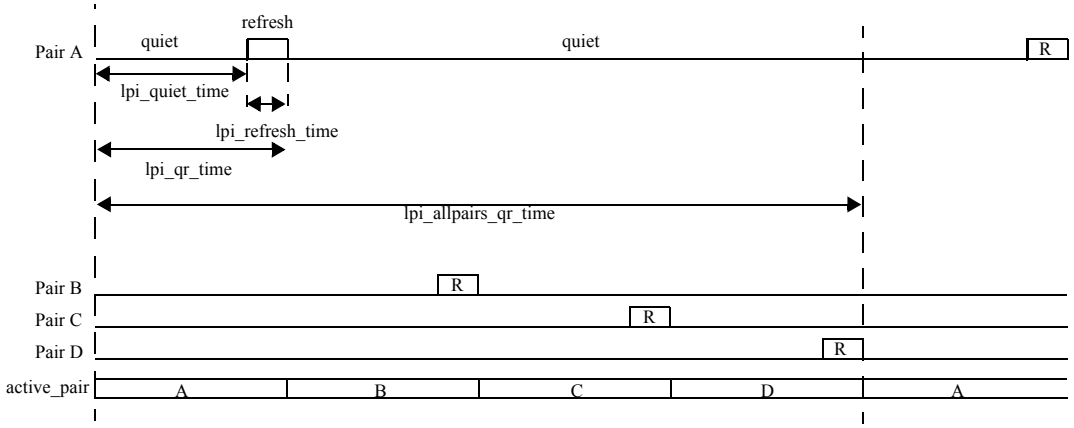


Figure 55–13a—Timing periods for LPI signals

PHYs begin the transition from the LPI receive mode when the alert signal is detected by the PMA as defined in 55.4.2.4.

55.3.4a.1 LPI Synchronization

To maximize power savings, maintain link integrity and ensure interoperability, EEE capable PHYs must synchronize refresh intervals during the LPI mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting LDPC frames from the transition to PCS_Test. An EEE capable PHY shall support loop timing and loop timing shall be enabled on the slave PHY.

In initial training, normal retraining, and fast retraining, with or without the EEE capability being supported, the master and slave signal when they will transition to PCS_Test using the transition counter following the procedure described in 55.4.2.5.14.

A EEE capable PHY in slave mode is responsible for synchronizing its PMA training frame to the master's PMA training frame during the transition to PMA_Training_Init_S. The slave shall ensure that its PMA training frames are synchronized to the master's PMA training frames within 1 LDPC frame, measured at the slave MDI on pair A. In addition, the slave shall initialize its transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master PHY's transition to PCS_Test, measured at the slave PHY's MDI on pair A. This mechanism ensures that the refresh offset is bounded to a small value at both MDI interfaces, thus ensuring there is no overlap of master and slave signals when both transmit and receive are in the LPI mode.

Following the transition to PCS_Test, the PCS counts transmitted and received LDPC frames, and uses these counters to generate refresh and pair control signals for the transmit and receive functions. The transmitted LDPC frame count is named tx_ldpc_frame_cnt. The received LDPC frame count is named rx_ldpc_frame_cnt.

The master and slave shall derive the active pair and refresh_active signals from the LDPC frame counters as shown in Table-55–1b and Table 55–1c.

Table 55–1b—Synchronization logic derived from slave signal LDPC frame count

Slave-side Variable	Master-side Variable	for master u=rx_ldpc_frame_cnt for slave u=tx_ldpc_frame_cnt
tx_refresh_active=true	rx_refresh_active=true	lpi_offset - lpi_refresh_time ≤ mod(u,lpi_qr_time) < lpi_offset
tx_lpi_full_refresh=true	N/A	lpi_offset - lpi_refresh_time = mod(u,lpi_qr_time)
tx_active_pair=PAIR_A	rx_active_pair=PAIR_A	lpi_offset + lpi_qr_time ≤ u < lpi_offset + 2 x lpi_qr_time
tx_active_pair=PAIR_B	rx_active_pair=PAIR_B	lpi_offset + 2 x lpi_qr_time ≤ u < lpi_offset + 3 x lpi_qr_time
tx_active_pair=PAIR_C	rx_active_pair=PAIR_C	lpi_offset + 3 x lpi_qr_time ≤ u < 4 x lpi_qr_time OR 0 ≤ u < lpi_offset
tx_active_pair=PAIR_D	rx_active_pair=PAIR_D	lpi_offset ≤ u < lpi_offset + lpi_qr_time

55.3.4a.2 Quiet period signaling

During the quiet period the transmitters on all four pairs should be turned off. Average launch power (as measured from 28 LDPC frames after a refresh period to 28 LDPC frames before the next refresh period on the same lane) for each Transmitter shall be less than -41dBm. This requirement does not apply to the periods when the alert signal is transmitted as defined in 55.4.2.2.1.

55.3.4a.3 Refresh period signaling

During the LPI mode 10GBASE-T PHYs use staggered, out-of-phase refresh signaling to maximize power savings. 2-level PAM refresh symbols are generated using the PMA side-stream scrambler polynomials described in 55.3.4 and exactly as is shown in Figure 55-13 with the exception that the InfoField consists of

Table 55–1c—Synchronization logic derived from master signal LDPC frame count

Slave-side Variable	Master-side Variable	for master v=tx_ldpc_frame_cnt for slave v=rx_ldpc_frame_cnt
rx_refresh_active=true	tx_refresh_active=true	lpi_quiet_time ≤ mod(v,lpi_qr_time)
N/A	tx_lpi_full_refresh=true	lpi_quiet_time = mod(v,lpi_qr_time)
rx_active_pair=PAIR_A	tx_active_pair=PAIR_A	0 ≤ v < lpi_qr_time
rx_active_pair=PAIR_B	tx_active_pair=PAIR_B	lpi_qr_time ≤ v < 2 x lpi_qr_time
rx_active_pair=PAIR_C	tx_active_pair=PAIR_C	2 x lpi_qr_time ≤ v < 3 x lpi_qr_time
rx_active_pair=PAIR_D	tx_active_pair=PAIR_D	3 x lpi_qr_time ≤ v < 4 x lpi_qr_time

a sequence of 128 zeros. The training sequence without periodic re-initialization described in 55.3.4 shall be used during the LPI mode, with the scramblers free-running from PCS Reset. If scrambler reinitialization is used for normal training, it shall be disabled and the scramblers shall begin free-running when the PHY Control state diagram enters the PCS_Test state.

Refresh signals shall be sent using the THP filter as described in 55.4.3.1. At the start of each refresh signal the THP feedback delay line shall be initialized with zeros.

While a transmit function is in the LPI transmit mode only one of the transmit pairs will be active during a refresh period. tx_symb_vector for all transmit pairs that are not active shall be set to zero.

When tx_symb_vector has the value ALERT and the PHY is the master the transmitter on pair A shall be active and all other pairs shall be quiet. When tx_symb_vector has the value ALERT and the PHY is slave the transmitter on pair C shall be active and all other pairs shall be quiet. If lpi_tx_mode=REFRESH_A on a MASTER PHY or lpi_tx_mode=REFRESH_C on a SLAVE PHY, and tx_symb_vector has the value ALERT then the alert signalling shall be transmitted in place of the refresh signalling where the signals overlap.

55.3.5 Detailed functions and state diagrams

55.3.5.2.1 Constants

Insert the following constant definitions after all existing constant definitions in the existing 55.3.5.2.1:

LPBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing /LI/ in all the eight character locations.

LPBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /LI/ in all the eight character locations.

IBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /I/ in all the eight character locations.

UBLOCK_R<71:0>

72 bit vector to be sent to the XGMII containing two Link Interruption ordered_sets. The Link Interruption ordered_set is defined in 46.3.4.

55.3.5.2.2 Variables

Insert the following variable definitions after all existing variable definitions in the existing 55.3.5.2.2:

The following variables are required for PHYs that support the EEE capability:

tx_lpi_active

A boolean variable that is set true when the PHY transmit function is operating in the LPI transmit mode and during transitions to and from the LPI transmit mode (i.e. at any time when the PHY is transmitting sleep, alert, wake or quiet-refresh signaling). It is set false otherwise.

tx_lpi_qr_active

A boolean variable that is set true during the LPI transmit mode, when the PHY is transmitting quiet-refresh signaling. Set false otherwise.

rx_lpi_active

A boolean variable that is set true when the PHY receive function is operating in the LPI receive mode and set false otherwise. The LPI receive mode begins when the sleep signal is detected and lasts until the alert signal is detected.When the EEE capability is not supported, rx_lpi_active is set false.

tx_lpi_req

A boolean variable that is set true when the LPI client indicates that it is requesting operation in the LPI transmit mode via the XGMII and set false otherwise.

alert_detect

Indicates that an alert signal from the link partner has been received at the MDI as indicated by PMA_ALERTDETECT.indication(alert_detect).

tx_lpi_alert_active

A boolean variable that is set true when the PHY is transmitting ALERT signaling. Set false otherwise.

rx_lpi_wake

A boolean variable that is set true when the PHY receiver is in the WAKE state and sending IDLE to the XGMII. Set false otherwise. When the EEE capability is not supported, rx_lpi_wake is set false.

tx_active_pair

A variable indicating the transmit active pair during the LPI transmit mode. The variable may take the values PAIR_A, PAIR_B, PAIR_C, PAIR_D. This variable is defined in 55.3.4a.1.

lpi_tx_mode

A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb_vector) interface.

lpi_tx_mode controls tx_symb_vector only when tx_mode is set to SEND_N.

The variable is set to NORMAL when (!tx_lpi_qr_active * !tx_lpi_alert_active), indicating that the PCS is in the normal mode of operation and will encode code-groups as described in Figures 55-15 and 55-15a

The variable is set to REFRESH_A when (tx_lpi_qr_active * (tx_active_pair==PAIR_A) * tx_refresh active).

The variable is set to REFRESH_B when (tx_lpi_qr_active * (tx_active_pair==PAIR_B) * tx_refresh active).

The variable is set to REFRESH_C when (tx_lpi_qr_active * (tx_active_pair==PAIR_C) *

tx_refresh active).

The variable is set to REFRESH_D when (tx_lpi_qr_active * (tx_active_pair==PAIR_D) * tx_refresh active).

The variable is set to QUIET when (tx_lpi_qr_active * (!tx _refresh_active + tx_lpi_initial_quiet))

The variable is set to ALERT when (tx_lpi_alert_active)

tx_refresh_active
A boolean value. This variable is set true following the logic described in 55.3.4a.1.

tx_lpi_full_refresh
A boolean value. This variable is set true following the logic described in 55.3.4a.1.

tx_lpi_initial_quiet
A boolean value. This variable is set true when the transmit function enters the LPI transmit mode and a partial refresh will be replaced by quiet signaling.

ldpc_frame_done
A boolean value. This variable is set true when the final symbol of each LDPC frame is transmitted and is set false otherwise.

The following variable is only required for PHYs that support the fast retrain capability.

fr_sigtype
If fast retrain is supported, this variable is set based on the value in 1.147.2:1 as follows:
00 IBLOCK_R
01 LBLOCK_R
10 UBLOCK_R
11 Reserved

55.3.5.2.3 Timers

Insert 4 additional timers after the existing timer definitions in 55.3.5.2.3:
The following timers are required for PHYs that support the EEE capability:

lpi_tx_sleep_timer
This timer defines the time the local transmitter sends the sleep signal to the link partner
Values: The condition lpi_tx_sleep_timer_done becomes true upon timer expiration
Duration: This timer shall have a period equal to 9 LDPC frame periods

lpi_tx_alert_timer
This timer defines the time the local transmitter transmits the alert signal.
Values: The condition lpi_tx_alert_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 4 LDPC frame periods.

lpi_tx_wake_timer:
This timer defines the time the local transmitter transmits the wake signal.
Values: The condition lpi_tx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

lpi_rx_wake_timer:
This timer defines the time the receiver sends IDLE blocks to the XGMII after the alert signal is detected.
Values: The condition lpi_rx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

55.3.5.2.4 Functions

Change the text in subclause 55.3.5.2.4 as shown below:

R_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this~~This~~ function classifies each 65 bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 65 bit rx_coded vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and eight valid control characters other than /E/ and /LI/.

b) A block type field of 0x2D or 0x4B, a valid O code, and four valid control characters;

c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;

b) A block type field of 0x66 and a valid O code;

c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

I; If the optional EEE capability is supported then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1e, and eight control characters of /I/.

LI: If the optional EEE capability is supported then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1e, and eight control characters of /LI/.

LII: If the optional EEE capability is supported then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:

a) four control characters of /LI/ followed by four control characters of /I/;

b) four control characters of /I/ followed by four control characters of /LI/

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-T control code specified in Table 55–1. A valid O code is one containing an O code specified in Table 55–1.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this~~This~~ function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) eight valid control characters other than /O/, /S/, /T/, ~~and~~/E/ and /LI/;

b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;

c) two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

I; If the optional EEE capability is supported then the I type is a special case of the C type where the vector contains eight control characters of /I/.

LI: If the optional EEE capability is supported then the LI type occurs when the vector contains eight control characters of /LI/.

LII: If the optional EEE capability is supported then the LII type occurs when the vector contains one of the following:

a) four control characters of /LI/ followed by four control characters of /I/;
b) four control characters of /I/ followed by four control characters of /LI/

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 55–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 55–1.

55.3.5.2.5 .Counters

Insert the following text after the existing text in subclause 55.3.5.2.5:

The following counters are required for PHYs that support the EEE capability:

tx_ldpc_frame_cnt

An integer value that counts transmit LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the transmit direction after normal training or fast retraining. It is incremented after the last symbol of each transmitted LDPC frame. tx_ldpc_frame_cnt is reset to 0 when tx_ldpc_frame_cnt = lpi_qr_time x 4.

rx_ldpc_frame_cnt

An integer value that counts receive LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the receive direction after normal training or fast retraining. It is incremented after the last symbol of each received LDPC frame. rx_ldpc_frame_cnt is reset to 0 when rx_ldpc_frame_cnt = lpi_qr_time x 4.

lpi_rxw_err_cnt

An integer value that counts the number of receive wake on error conditions. lpi_rxw_err_cnt is reset to zero during PCS_Test. The counter is reflected in register 3.22 (see 45.2.3.8b).

55.3.5.4 State diagrams

Change the third paragraph of the existing text in 55.3.5.4 as shown below:

The 64B/65B Receive state diagram shown in Figure 55-16 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B receive block processed except for the transition from RX_WE to RX_E which occurs immediately after the RX_WE processes are complete.

Change the last paragraph of the existing text in 55.3.5.4 as shown below:

The PCS shall perform the functions of LFER Monitor, Transmit, and Receive as specified in these state diagrams. The PCS shall not perform the LFER Monitor function during LPI receive operation from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.

Insert the following text at the end of the existing text in 55.3.5.4:

Transitions surrounded by dashed rectangles indicate requirements for 10GBASE-T EEE-capable implementations.

Replace figures 55-14, 55-15 and 55-16 and Insert figures 55-15a, 55-16a and 55-16b as shown below:

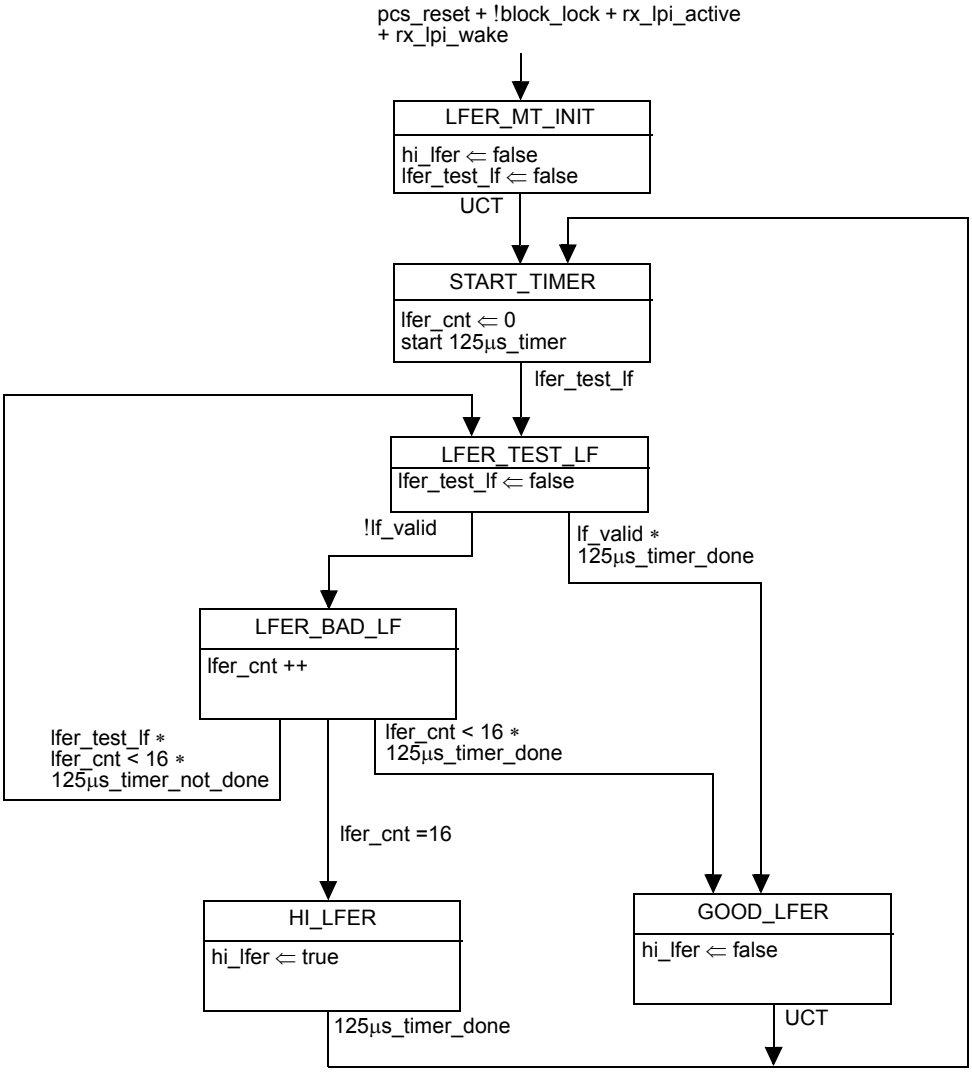


Figure 55–14—LFER monitor state diagram

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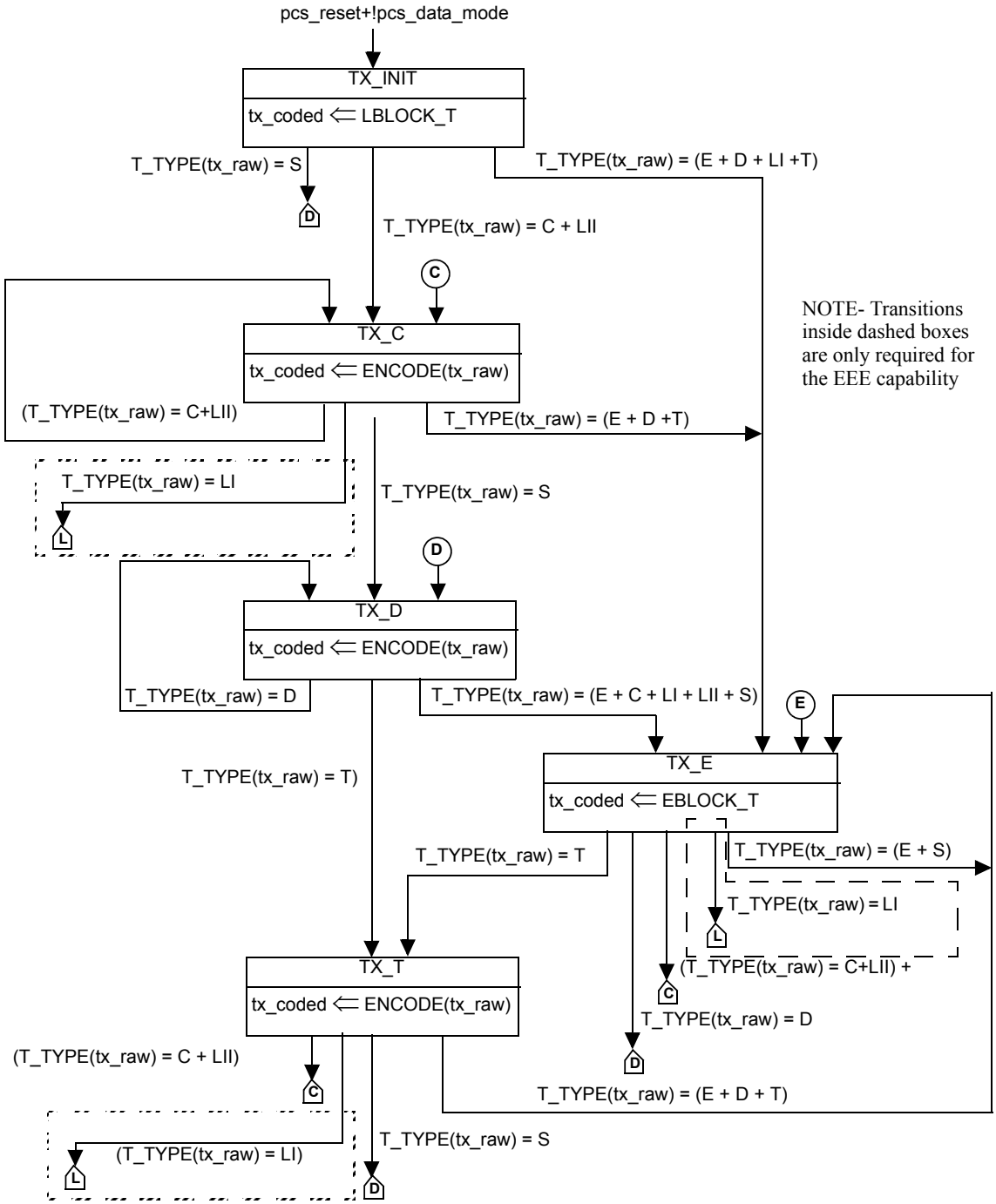


Figure 55–15—PCS 64B/65B Transmit state diagram part a)

NOTE- This figure is mandatory for PHYs with the EEE capability

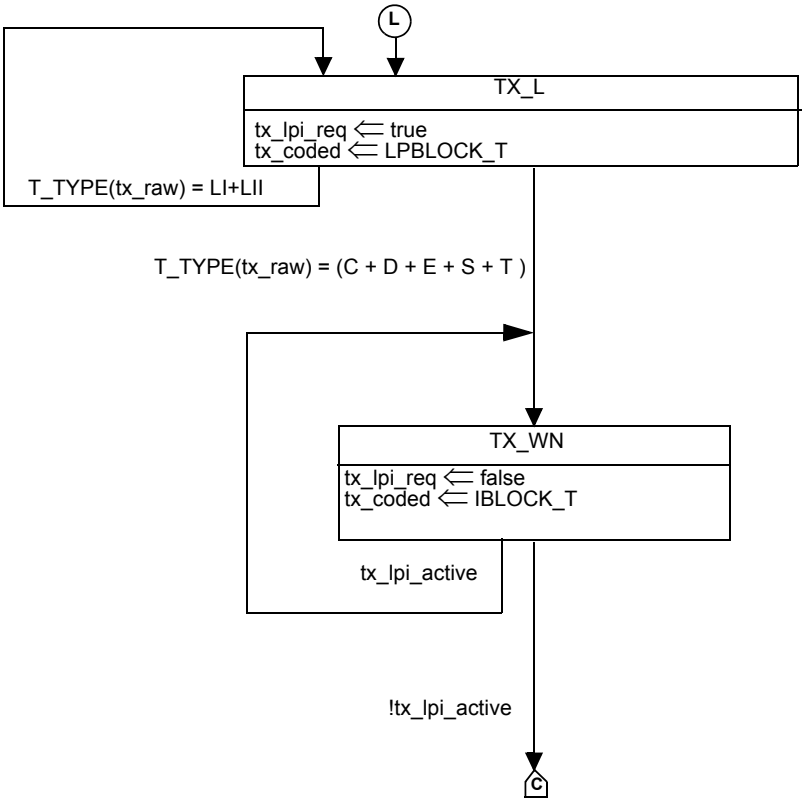


Figure 55–15a—PCS 64B/65B Transmit state diagram part b)

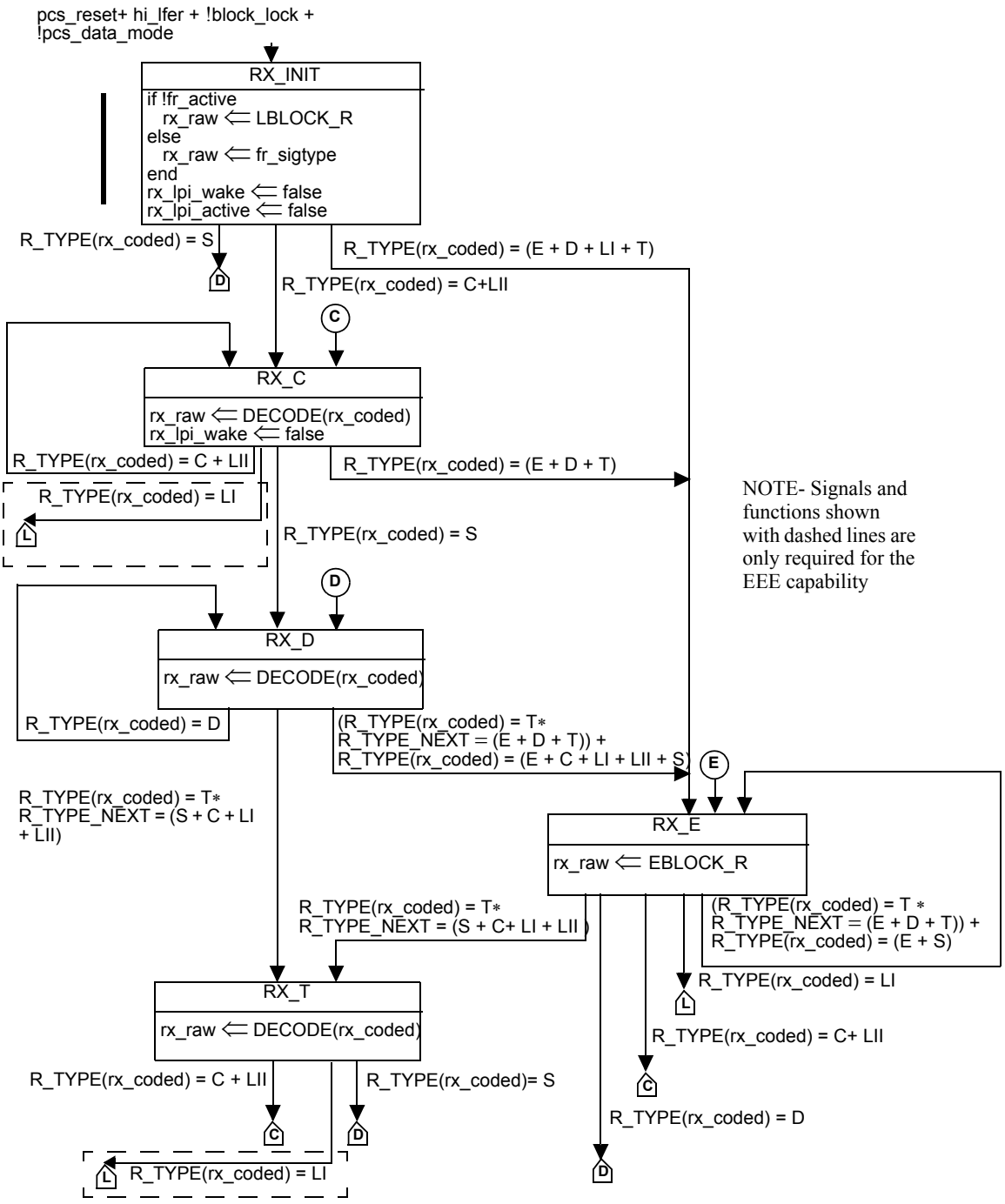


Figure 55–16—PCS 64B/65B Receive state diagram, part a)

NOTE- This figure is mandatory for PHYs with the EEE capability

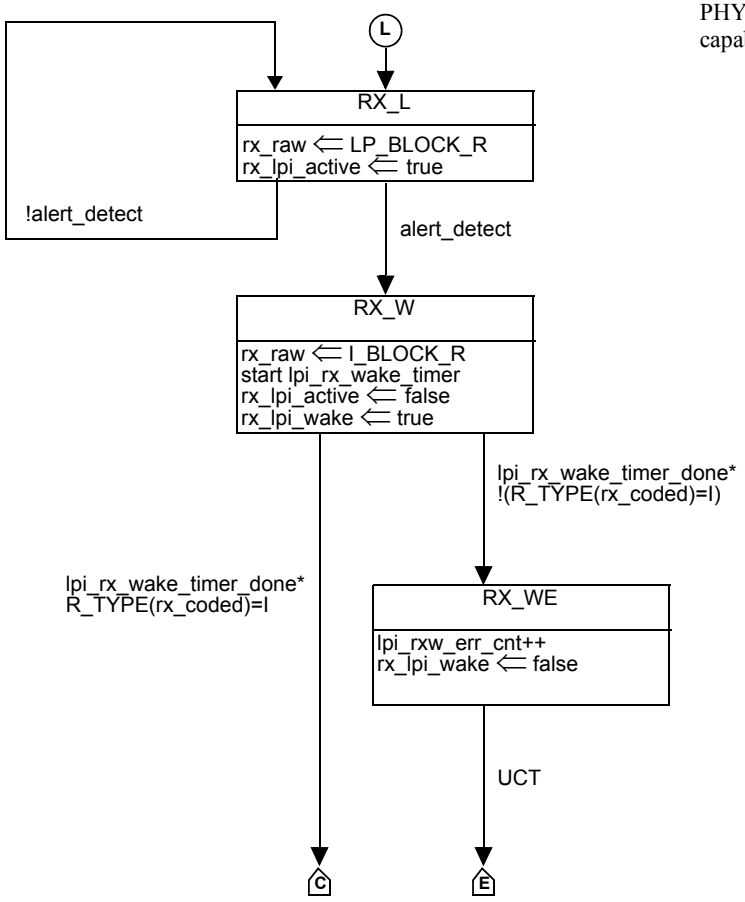


Figure 55–16a—PCS 64B/65B Receive state diagram, part b)

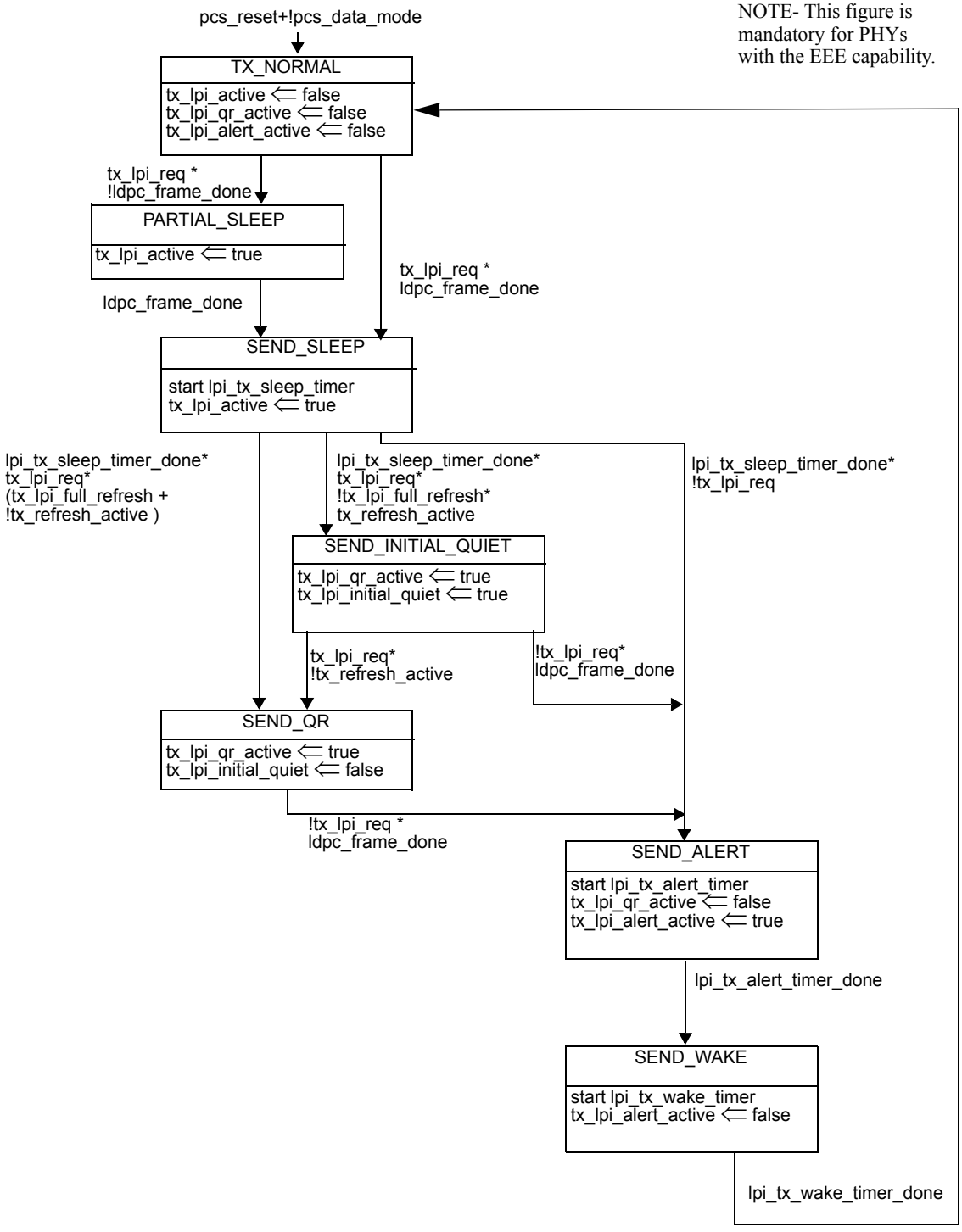


Figure 55–16b—EEE transmit state diagram

Insert the following text after the existing text in subclause 55.3.6.1

Rx LPI indication:

For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Receive state diagram (Figure 55–16a) is in the RX_L or RX_W states. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

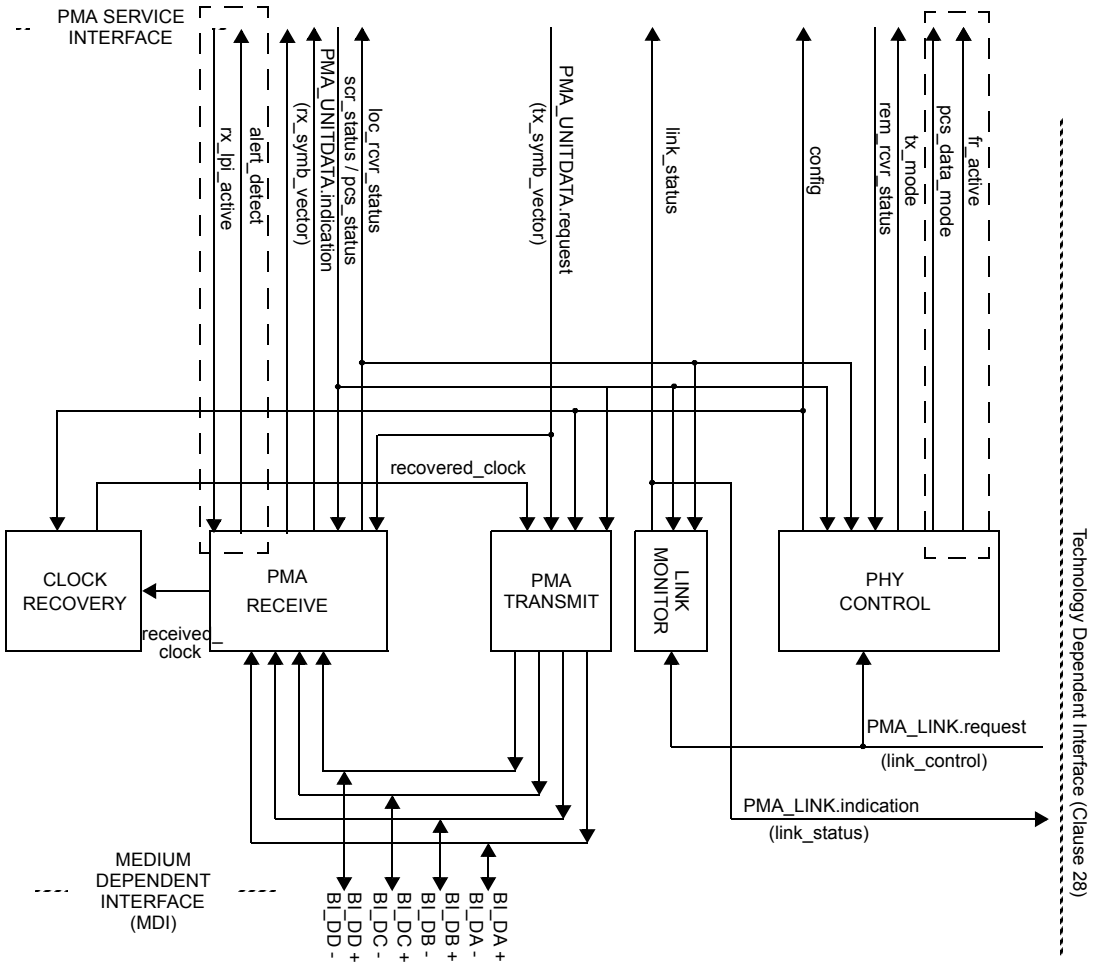
Tx LPI indication

For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Transmit state diagram (Figure 55–15a) is in the TX_L or TX_W states. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

55.4 Physical Medium Attachment (PMA) sublayer

55.4.1 PMA functional specifications

Replace Figure 55-17 with the figure shown below



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

NOTE- pcs_data_mode is required only for the EEE or fast retrain capabilities
alert_detect and rx_lpi_active are only required for the EEE capability
fr_active is only required for the fast retrain capability

Figure 55-17 -- PMA reference diagram

55.4.2.2 PMA Transmit function

Change text in 55.4.2.2 PMA Transmit function as shown below:

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. While send_fail is FALSE and ALERT is not indicated by tx_symb_vector then PMA transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively after processing with the THP, optional transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. When ALERT is indicated by tx_symb_vector the alert signal is transmitted as specified in 55.4.2.2.1. When send_fail is TRUE the link failure signal is transmitted as specified in 55.4.2.2.2. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 55.4.3.1, and shall comply with the electrical specifications given in 55.5.

When the PMA_CONFIG.indication parameter config is MASTER, for both normal and LPI operation, the PMA Transmit function shall continuously source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 55.5.3.3. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented and the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 55.4.2.7 while meeting the jitter requirements of 55.5.3.3. If loop timing is not implemented, the SLAVE PHY transmit clocking is identical to the MASTER PHY transmit clocking. A EEE capable PHY shall operate with loop timing when configured as SLAVE.

Insert the following text after the existing text in 55.4.2.2 PMA Transmit function:

EEE capable PHYs shall implement a PMA Transmit function that generates the alert signal as defined in 55.4.2.2.1. PHYs that support the fast retrain capability shall implement a PMA Transmit function that generates the link failure signal as defined in 55.4.2.2.2. If ALERT is indicated by tx_symb_vector at the same time as send_fail is TRUE then link failure signaling is transmitted.

Insert new subclauses 55.4.2.2.1 and 55.4.2.2.2 after the existing text in 55.4.2.2 PMA Transmit function as shown below:

55.4.2.2.1 Alert signal

PHYs that support the optional EEE capability will transmit the following PAM2 sequence when the PMA_UNITDATA.request parameter is set to ALERT. The alert signal is sent for a total of 4 LDPC frame periods and begins on a LDPC frame boundary. The alert signal is transmitted without THP filtering. The alert signal is transmitted on pair A when the PHY operates as a MASTER. The alert signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in subclause 55.3.4a.

When the PMA_CONFIG.indication(config) is MASTER the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_master =

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 -9 -9

-9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9

When the PMA_CONFIG.indication(config) is SLAVE the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_slave =

-9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9

-9 -9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

The alert signal is followed by a wake signal composed of repeated IDLE characters encoded using the 64B/65B encoding technique. At the start of the wake signal all THP feedback delay lines are initialized with zeros.

55.4.2.2.2 Link failure signal

PHYs that support the fast retrain capability transmit the link failure signal under the control of the Fast Retrain state diagram. The link failure signal indicates to the link partner that a link failure has been detected and that the link partners should begin the fast retrain procedure.

The link failure signal is sent for 4 LDPC frames and begins on a LDPC frame boundary. The link failure signal is transmitted without THP filtering. The link failure signal is transmitted on pair A when the PHY operates as a MASTER. The link failure signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in subclause 55.3.4a.

When the PMA_CONFIG.indication(config) is MASTER the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_master = xpr_master × -1

When the PMA_CONFIG.indication(config) is SLAVE the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_slave = xpr_slave × -1

Change the text in 55.4.2.4 as shown below:

55.4.2.4 PMA Receive function

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, ~~and~~ estimation, and LPI functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

Insert the following text after the existing text in 55.4.2.4:

PMA receive functions that support the optional EEE capability shall generate alert_detect when the alert signal is detected at the receiver. The PMA receive function asserts alert_detect after the entire alert signal (3.5 LDPC frame periods of the xpr_master or xpr_slave sequence and 0.5 frames of silence) has been detected. The alert signal is specified in 55.4.2.2.1. The criterion used to generate alert_detect is left to the implementor.

PHYs that support the fast retrain capability shall set link_fail_detect to TRUE when the link failure signal is reliably detected at the receiver. The PMA receive function asserts link_fail_detect after the entire link failure signal (3.5 LDPC frame periods of the xfr_master or xfr_slave sequence and 0.5 frames of silence) has been detected. The link failure signal is specified in 55.4.2.2.2. The criterion used to generate link_fail_detect is left to the implementor. It is highly recommended that the generation of link_fail_detect is qualified with repeated errored frames at the LDPC decoder output.

55.4.2.5 PHY Control function

55.4.2.5.14 Startup sequence

Insert the following text at the end of the second paragraph of 55.4.2.5.14 as shown below:

During normal training, prior to enabling the transmitter, the THP coefficients are set to zero.

Change the text in the eighth paragraph of 55.4.2.5.14 as shown below:

In SLAVE mode, PHY Control transitions to the PMA_Training_Init_S state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin=OK. The SLAVE shall respond using the fixed PBO transmit power level, PBO=4 (corresponding to a power backoff of 8dB). For PHYs with the EEE capability, further requirements for this transition are described in 55.3.4a.1.

Change the text in the fifteenth paragraph of 55.4.2.5.14 as shown below:

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, each PHY announces a transition to the PCS_Test (trans_to_PCS_Test=1) and starts the transition counter as described in 55.4.5.1. For PHYs with the EEE capability, further requirements for this transition are described in 55.3.4a.1.

Insert the following text after the existing text in 55.4.2.5.14:

After reaching the PCS_Data state PHYs with the EEE capability can transition to the LPI receive mode under the control of the link partner and to the LPI transmit mode under control of the local LPI client.

Insert a new subclause 55.4.2.5.15 after subclause 55.4.2.5.14

55.4.2.5.15 Fast retrain function

PHYs that support the fast retrain capability shall implement the fast retrain state diagram shown in Figure 55–27b. PHYs may request a fast retrain by setting the variable loc_fr_req to TRUE. This causes the transmission of an easily-detected link failure signal specified in 55.4.2.2.2. After completing the link failure signal the PHY shall transition to the PMA_Coeff_Exch state, keep its THP turned on with its previously-exchanged coefficients, and send PAM2 signaling within a time period equivalent to 9 LDPC frame periods.

After the detection of the link failure signal, a PHY shall transition to the PMA_Coeff_Exch state and respond with PAM2 signaling within a time period equivalent to 9 LDPC frame periods after receiving the link failure signal.

The PAM2 symbols are generated using the PMA sidestream scrambler polynomials shown in Figure 55-13. The training sequence without periodic re-initialization described in 55.3.4 shall be used during fast retraining, with the scramblers free-running from PCS Reset. If scrambler re-initialization is used for normal training, it shall be disabled and the scramblers shall begin free-running when the PHY Control state diagram enters the PCS_Test state and the variable fr_active is FALSE.

Note that reliable traffic on the transmitter may be interrupted when the local receiver requests a fast retrain.

Following the link failure signal, the two link partners transition back to the PMA_Coeff_Exch state and follow the training procedure described in 55.4.2.5.14, with the exception that the initial infofield countdown values are reduced as indicated in Figures 55-25 and 55-26.

To ensure interoperability the training times in Table 55–6a should be observed during the fast retrain.

Table 55–6a—Recommended fast retrain sequence timing

State	Recommended maximum time (ms)
PMA_Coeff_Exch state	20
PMA_Fine_Adjust state	10

Insert the following subclause after subclause 55.4.2.6

55.4.2.6a Refresh Monitor function

The Refresh monitor is required for PHYs which support the EEE capability. The Refresh monitor operates when the PHY is in the LPI receive mode. The Refresh monitor shall comply with the state diagram of Figure 55–16a. The function forces a link retrain if a refresh signal is not reliably detected within a moving time window equivalent to 50 complete quiet-refresh cycles (nominally equal to 8.192 ms), when the PHY is in the lower power receive mode.

55.4.4 Automatic MDI/MDI-X configuration

Insert the following text after the existing text in 55.4.4:

For EEE capable PHYs, the MDI/MDIX function configuration shall apply to refresh and alert signaling. For PHYs with the fast retrain capability, the MDI/MDIX function configuration shall apply to link failure signaling.

55.4.5 State variables

55.4.5.1 State diagram variables

Change the text in 55.4.5.1 as shown below:

transition_count

This variable reports the value of the transition counter contained in the InfoField sent to the remote device. Transition_count must comply with the state diagram description given in 55.4.6.2. When the message field contains a flag for a state transition, the transition counter denotes the remaining number of InfoField until the next state transition. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a counter value of 2^9 (10 ms). The SLAVE responds prior to the counter reaching 2^6 (1 ms) with the same flag and a count value matching the MASTER. Then both PHY's transition to PMA_Coeff_Exch within one PMA frame. The same sequence is performed in the transition to PMA_Fine_Adjust state and PCS_Test state using the trans_to_Fine_Adjust=1 and trans_to_PCS_Test=1 flags respectively. In EEE capable PHYs, synchronization of the PMA frames is tightly controlled as described in 55.3.4a.1. When the message field does not contain a flag for a state transition, the transition counter is set to zero and ignored by the receiver.
Values: 0 to 2^9

Insert the following variable definitions after all existing variable definitions in the existing 55.4.5.1

The following variables are required only for PHYs that support the EEE capability

lpi_refresh_detect

Set TRUE when the receiver has reliably detected refresh signaling and FALSE otherwise. The exact criteria left to the implementor.

pcs_data_mode

Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indicate primitive. In the absence of the optional EEE and fast retrain capabilities, the PHY operates as if the value of this variable is TRUE.

mtc

mtc is the transition count for a MASTER PHY during normal training and fast retraining. mtc shall be equal to 2^9 for normal training and 2^5 for fast retrain.

stc

stc is the transition count for a SLAVE PHY during normal training and fast retraining. stc shall be equal to 2^6 for normal training and 2^4 for fast retrain.

The following six variables are required only for PHYs that support the fast retrain capability:

fr_enable

This variable is set to TRUE if 1.147.0 is set to 1 and fast retrain is supported. The variable is set to FALSE otherwise.

loc_fr_req

Set TRUE when the receiver has detected a link failure condition and is requesting a fast retrain, set FALSE otherwise.

loc_fr_detect

Set TRUE when the receiver has reliably detected the link failure signal. It is highly recommended that loc_fr_detect is qualified with the reception of errored blocks at the LDPC decoder output. Set FALSE when the link failure signal is not detected.

send_link_fail

When set TRUE indicates that the PMA should send the link failure signal. When FALSE the variable has no effect.

fr_active

Set TRUE when the PHY is performing a fast retrain and set FALSE otherwise.

fast_retrain_flag

Set TRUE after the PHY generates or detects a link failure signal and set FALSE otherwise.

55.4.5.2 Timers

Insert the following timer definitions after all existing variable definitions in the existing 55.4.5.2

The following timer is required only for PHYs that support the EEE capability.

lpi_refresh_rx_timer
This timer is used to monitor link quality during the LPI receive mode. If the PHY does not reliably detect reliable refresh signaling before this timer expires then a full retrain is performed.
Values: The condition lpi_refresh_rx_timer_done becomes true upon timer expiration
Duration: This timer shall have a period equal to 50 complete quiet-refresh signal periods, equivalent to 8.192ms.

The following two timers are required only for PHYs that support the fast retrain capability:

link_fail_sig_timer
Determines the period of time the PHY sends the link failure signal.
Values: The condition link_fail_sig_timer_done becomes true upon timer expiration
Duration: This timer shall have a period equal to 4 LDPC frame periods.

fr_maxwait_timer
Determines the period of time the PHY has to transition its PCS Control State to PCS_Test following a fast retrain before the fast retrain is aborted and a full retrain performed.
Values: The condition fr_maxwait_timer_done becomes true upon timer expiration
Duration: This timer shall have a period equal to 30ms.

55.4.5.4 Counters

Insert the following counter definitions after all existing counter definitions in the existing 55.4.5.4

The following two counters are required only for PHYs that support the fast retrain capability:

fr_tx_counter

Counts the number of times the PHY initiates a fast link retrain by transmitting the link failure signal. This counter is reflected in MDIO register 1.147.10:6 specified in subclause 45.2.1.76a.2.

fr_rx_counter

Counts the number of times the PHY begins a fast link retrain in response to the detection of link failure signalling from the link partner. This counter is reflected in MDIO register 1.147.15:11 specified in subclause 45.2.1.76a.1.

55.4.6 State diagrams

55.4.6.1 PHY Control state diagram

Replace the existing Figure 55-24 with the new Figure 55-24 as shown below

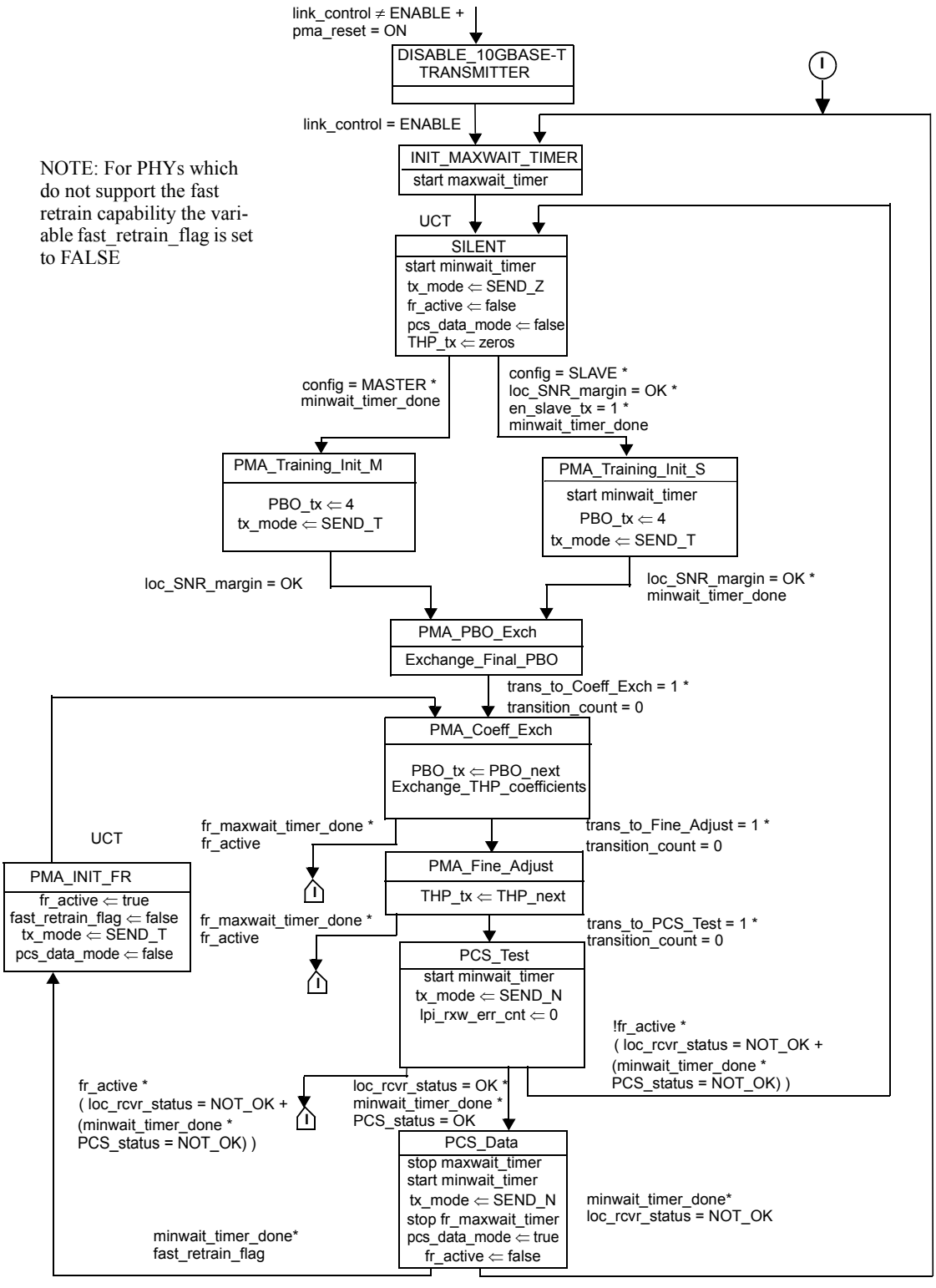


Figure 55–24—PHY Control state diagram

55.4.6.2 Transition counter state diagrams

Replace the existing state diagrams Figure 55-25 and Figure 55-26, with Figure 55-25 and Figure 55-26 as shown below

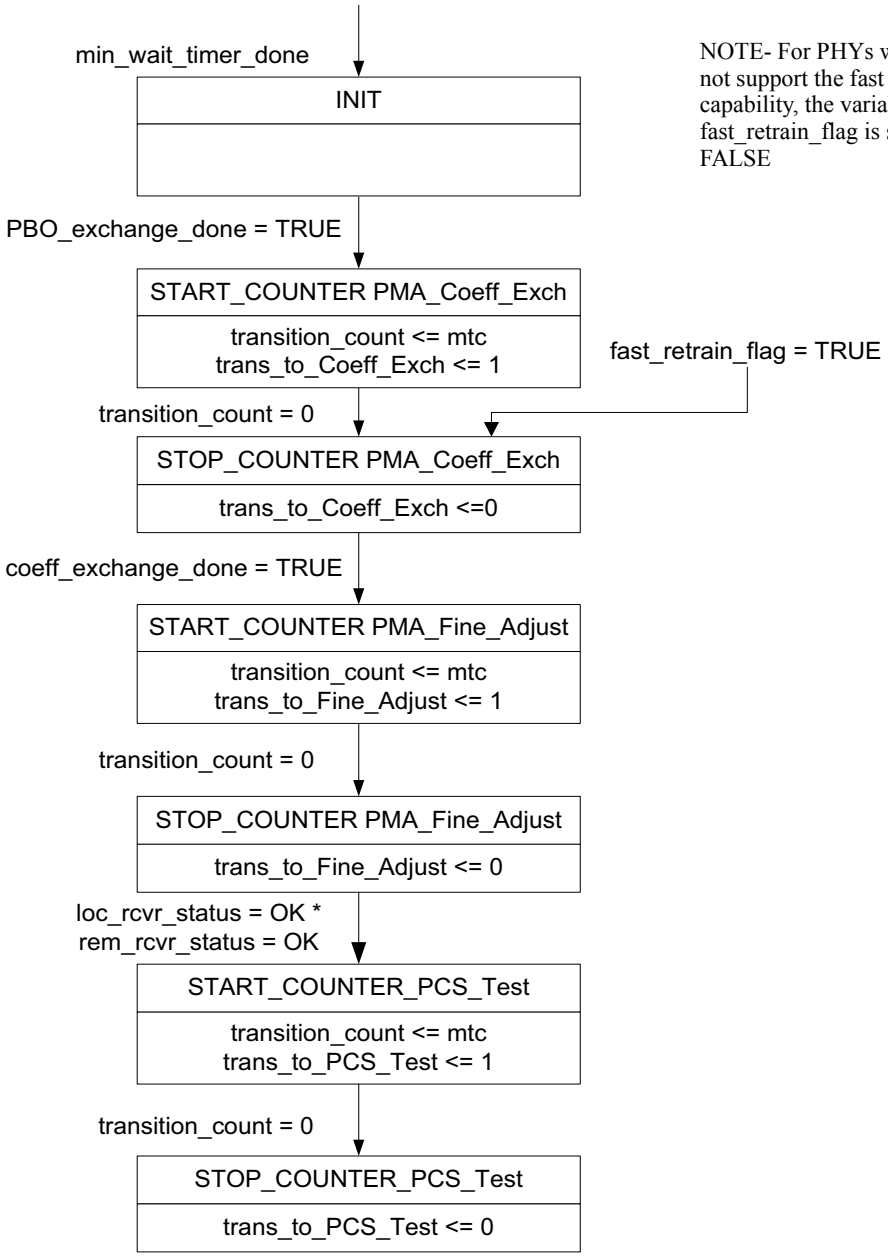


Figure 55–25—MASTER transition counter state diagram

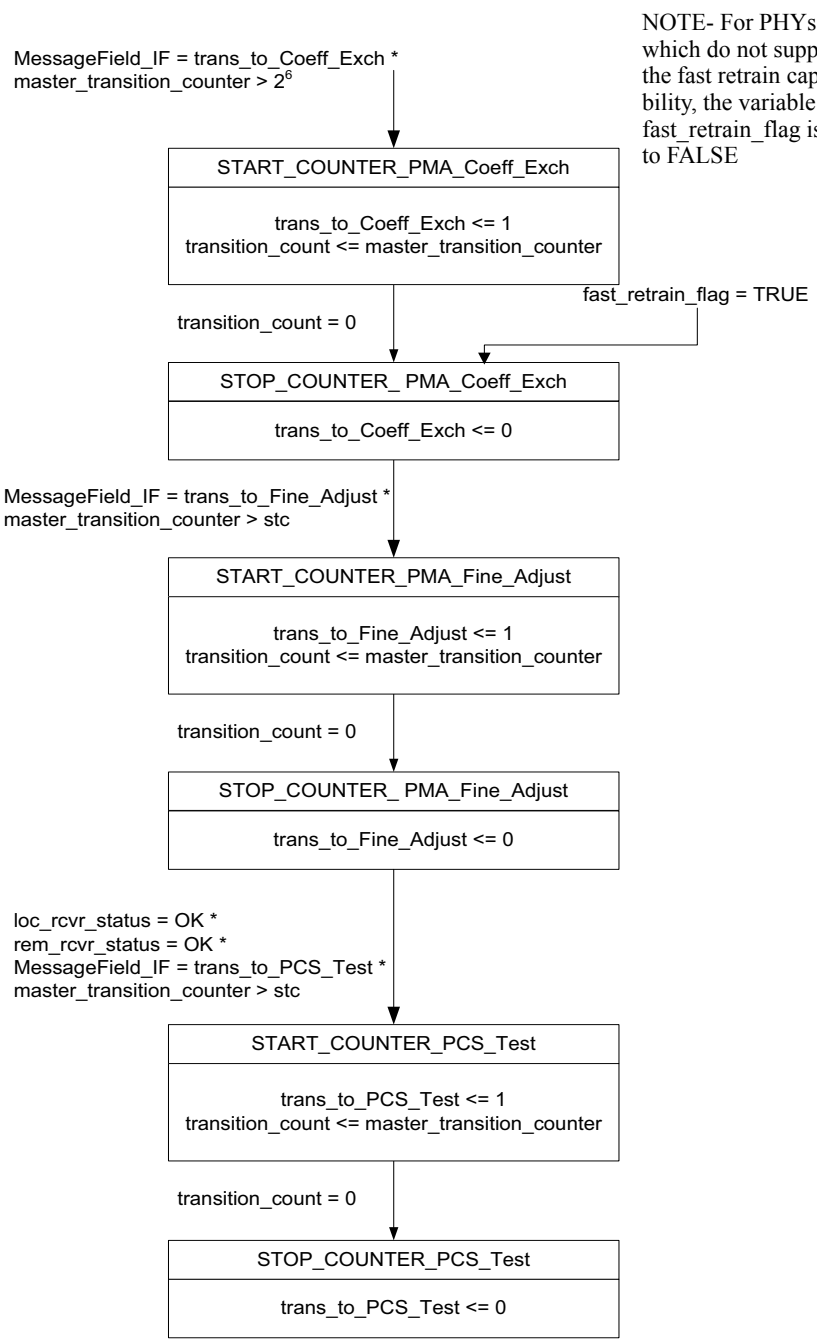


Figure 55–26—SLAVE transition counter state diagram

Insert a new subclause 55.4.6.4 after subclause 55.4.6.3, containing Figure 55-27a, as shown below

55.4.6.4 EEE Refresh monitor state diagram

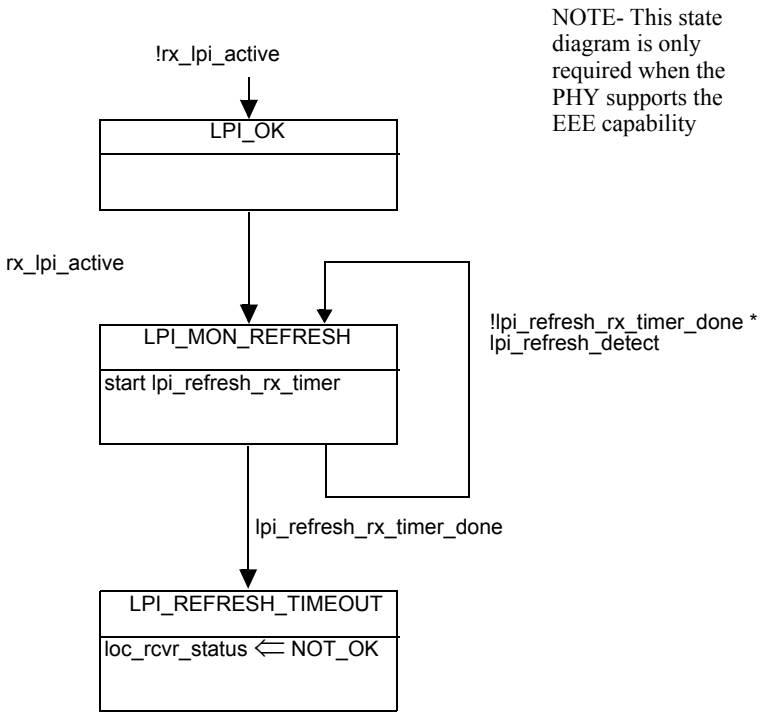


Figure 55–27a—EEE Refresh monitor state diagram

Insert a new subclause 55.4.6.5, containing Figure 55-27b, after subclause 55.4.6.4, as shown below

55.4.6.5 Fast retrain state diagram

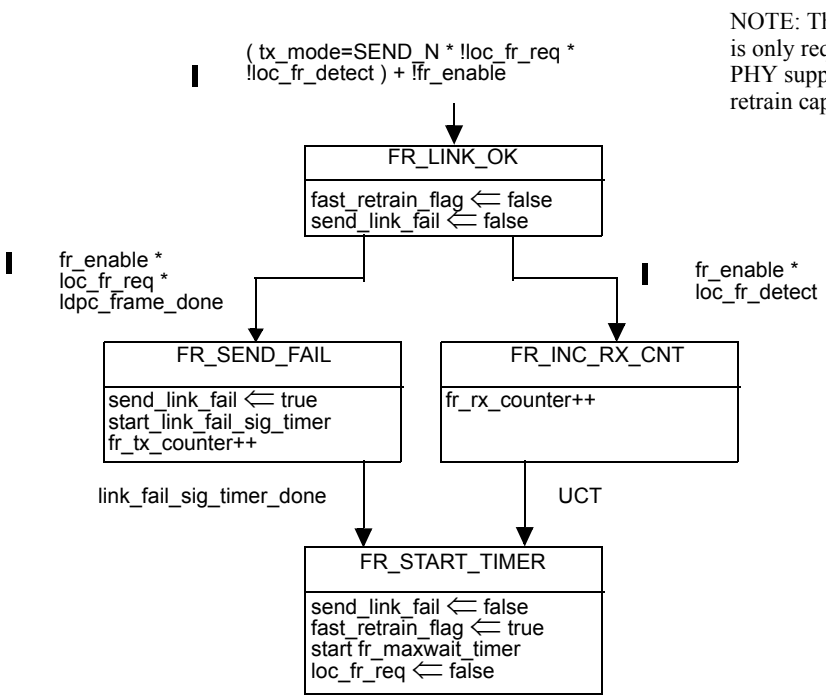


Figure 55–27b—Fast retrain control state diagram

55.5 PMA electrical specifications

55.5.3.5 Transmit clock frequency

Insert the following text after the existing text in 55.5.3.5:

When the transmitter is in the LPI transmit mode or when the receiver is in the LPI receive mode the transmitter clock short term rate of frequency variation shall be less than 0.1 ppm/second. The short term frequency variation limit shall also apply when switching to and from the LPI mode.

55.6 Management interfaces

10GBASE-T makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

55.6.1 Support for Auto-Negotiation

Change the list by adding (d) and (e) as new items in the list as shown below:

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.
c) To determine whether the local PHY performs PMA training pattern reset.
d) To determine whether the local PHY supports the EEE capability.
e) To determine whether the local PHY supports the fast retrain capability

Add new rows for bits U24, U23, U22 and U21 and edit the rows for bit U19 and for the remaining reserve bits in Table 55-11 as shown below:

Table 55–11—10GBASE-T Base and next pages bit assignments

Extended next page (Unformatted Message Code Field)		
U31:U25 ~~21~~	Reserved, transmit as 0	
U24	10GBASE-T EEE (1 = Advertise EEE capability for 10GBASE-T 0 = Do not advertise EEE capability for 10GBASE-T)	Defined in 45.2.7.13.4
U23	1000BASE-T EEE (1 = Advertise EEE capability for 1000BASE-T 0 = Do not advertise EEE capability for 1000BASE-T)	Defined in 45.2.7.13.5
U22	100BASE-TX EEE (1 = Advertise EEE capability for100BASE-TX 0 = Do not advertise EEE capability for 100BASE-TX)	Defined in 45.2.7.13.6
U21	Reserved	
U20	LD PMA training reset request (1 = Local Device requests that Link Partner reset PMA training PRBS every frame 0 = Local Device requests that Link Partner run PMA training PRBS continuously)	Defined in 45.2.7.10.5
U19	Fast retrain ability (1 = Advertise PHY as supporting fast retrain, 0 = Advertise PHY as not supporting fast retrain) ~~Reserved, transmit as 0~~	Defined in 45.2.7.10.5a

55.10 PHY labeling

Change the list of parameters by adding e) and f) as new items as shown below:

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability and units thereof
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 10GBASE-T)
d) Any applicable safety warnings
e) EEE support
f) Fast retrain support

55.12 Protocol implementation conformance statement (PICS) proforma for Clause 55—Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.12.2 Major capabilities/options

Insert the two rows shown below as the last two rows in the table:

Item	Feature	Subclause	Status	Support	Value/Comment
*EEE	Support of EEE capability		O	Yes [ ] No [ ]	55.1.3.3
*FR	Support of Fast Retrain capability		O	Yes [ ] No [ ]	55.4.2.5.15

55.12.3 Physical Coding Sublayer (PCS)

Change the table in 55.12.3 as shown below:

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	PCS Transmit function state diagram	55.3.2.2	M	Yes [ ]	See Figure 55–15
PCT1a	PCS Transmit function state diagram with EEE states	55.3.2.2	EEE:M	Yes [ ]	See Figure 55–15 and Figure 55–15a
PCT2	PCS Transmit bit ordering	55.3.2.2.4	M	Yes [ ]	See Figure 55–6 and Figure 55–8
PCT3	Invalid control code handling	55.3.2.2.6	M	Yes [ ]	
PCT4	/I/ insertion and deletion	55.3.2.2.9	M	Yes [ ]	
PCT4a	/LI/ insertion and deletion	55.3.2.2.10	EEE:M	Yes [ ]	
PCT5	/O/ deletion	55.3.2.2.12	M	Yes [ ]	
PCT6	Scrambler as MASTER	55.3.2.2.15	M	Yes [ ]	
PCT7	Scrambler as SLAVE	55.3.2.2.15	M	Yes [ ]	
PCT8	CRC8	55.3.2.2.16	M	Yes [ ]	See Figure 55–11
PCT9	LDPC encoding	55.3.2.2.17	M	Yes [ ]	Generator matrix is described in Annex 55A
PCT10	DSQ128 mapping	55.3.2.2.18	M	Yes [ ]	
PCT10a	EEE Transmit function state diagram	55.3.2.2.21	EEE:M	Yes [ ]	See Figure 55–16b
PCT10b	LP_IDLE input to scrambler during LPI mode	55.3.2.2.21	EEE:M	Yes [ ]	
PCT10c	lpi_tx_mode control	55.3.2.2.21	EEE:M	Yes [ ]	
PCT11	PCS test pattern mode	55.3.3	M	Yes [ ]	See Figure 55–6
PCT12	PMA training - MASTER scrambler	55.3.4	M	Yes [ ]	

Item	Feature	Subclause	Status	Support	Value/Comment
PCT13	PMA training - SLAVE scrambler	55.3.4	M	Yes [ ]	
PCT14	PMA training scrambler reset	55.3.4	M	Yes [ ]	If requested by Link Partner during Auto Negotiation
PCT15	PMA training scrambler initial state	55.3.4	M	Yes [ ]	In no case shall the scrambler state be initialized to all zeros
PCT15a	LPI active pair and refresh_active signals	55.3.4a.1	EEE:M	Yes [ ]	
PCT15b	alert signaling in place of refresh signaling	55.3.4a.3	EEE:M	Yes [ ]	
PCT15c	Slave synchronization	55.3.4a.1	EEE:M	Yes [ ]	
PCT15d	Quiet launch power	55.3.4a.2	EEE:M	Yes [ ]	
PCT15e	LPI sleep timer	55.3.5.2.3	EEE:M	Yes [ ]	
PCT15f	LPI alert timer	55.3.5.2.3	EEE:M	Yes [ ]	
PCT15g	LPI wake timer	55.3.5.2.3	EEE:M	Yes [ ]	
PCT15h	LPI rx wake timer	55.3.5.2.3	EEE:M	Yes [ ]	
PCT15i	LPI tx wake timer	55.3.5.2.3	EEE:M	Yes [ ]	
PCT15j	LPI scrambler	55.3.4a.3	EEE:M	Yes [ ]	The training sequence without periodic re-initialization described in 55.3.4 shall be used
PCT15k	Disable scrambler reinitialization	55.3.4a.3	EEE:M	Yes [ ]	
PCT15l	Refresh using THP	55.3.4a.3	EEE:M	Yes [ ]	
PCT15m	Reset THP at the start of refresh	55.3.4a.3	EEE:M	Yes [ ]	
PCT15n	Master alert on pair A, other pairs silent	55.3.4a.3	EEE:M	Yes [ ]	
PCT15o	Slave alert on pair C, other pairs silent	55.3.4a.3	EEE:M	Yes [ ]	
PCT15p	Inactive pairs transmit zeros	55.3.4a.3	EEE:M	Yes [ ]	
PCT16	ENCODE function	55.3.5.2.4	M	Yes [ ]	Encode the block as specified in 55.3.2.2.2
PCT17	PCS loopback setup	55.3.6.3	M	Yes [ ]	

55.12.4 Physical Medium Attachment (PMA)

Insert rows PMF8a and PMF8b, PMF10a and PMF10b, PMF16a-d, PMF17a and PMA18a after rows PMF8, PMF10, PMF16, PMF17 and PMF18 respectively:

Item	Feature	Subclause	Status	Support	Value/Comment
PMF8a	Generates alert signal	55.4.2.2	EEE:M	Yes [ ]	Generates the alert signal defined in 55.4.2.2.1
PMF8b	Generates link failure signaling	55.4.2.2	FR:M	Yes [ ] No [ ]	Generates the link failure signal defined in 55.4.2.2.2
PMF10a	Implement alert_detect	55.4.2.4	EEE:M	Yes [ ]	Generates alert_detect when the alert signal is detected at the receiver
PMF10b	Detect link failure signaling	55.4.2.4	FR:M	Yes [ ] No [ ]	Sets link_fail_detect to true when the link failure signal is detected
PMF16b	Implements fast retrain state diagram	55.4.2.5.15	FR:M	Yes [ ] No [ ]	
PMF16c	Behavior after fast retrain request	55.4.2.5.15	FR:M	Yes [ ] No [ ]	Transmit PAM2 within 9 LDPC frame periods following link failure request
PMF16d	Behavior after fast retrain signal detection	55.4.2.5.15	FR:M	Yes [ ] No [ ]	Transmit PAM2 within 9 LDPC frame periods following link failure signal detection
PMF17a	Refresh monitor state diagram	55.4.2.6a	EEE:M	Yes [ ] No [ ]	Implements state diagram of Figure 55-16a
PMF17b	Recommended fast retrain sequence timing	55.4.2.5.15	FR:O	Yes [ ] No [ ]	See Table 55-6a
PMF18a	MDIX for EEE refreshes and alert	55.4.4	EEE:M	Yes [ ]	

55.12.6 Management interface

Insert rows MF6a and MF6b after row MF6.

Item	Feature	Subclause	Status	Support	Value/Comment
MF6a	EEE advertisement	55.6.1.2	EEE:M	Yes [ ]	As defined in table 55-11
MF6b	Fast retrain ability advertisement	55.6.1.2	FR:M	Yes [ ]	As defined in table 55-11

55.12.6 PMA Electrical Specifications

Insert rows PME25a and PME25b after row PMA25

Item	Feature	Subclause	Status	Support	Value/Comment
PME25a	Maximum short term rate of frequency variation during LPI	55.5.3.5	EEE:M	Yes [ ]	Less than 0.1ppm/second
PME25b	Maximum short term rate of frequency variation when switching to and from LPI	55.5.3.5	EEE:M	Yes [ ]	Less than 0.1ppm/second

69. Introduction to Ethernet operation over electrical backplanes

69.1.1 Scope

Insert the following text as the last paragraph in 69.1.1:

Backplane Ethernet optionally supports Energy Efficient Ethernet (EEE) to reduce energy consumption. The EEE capabilities are advertised during Auto-Negotiation.

Editors' Notes: *To be removed prior to publication.*
Clause 69 is also being modified by P802.3ba which adds support for a 40Gb/s PHY.

69.1.2 Objectives

Change 69.1.2 by inserting item (f) to end of the list of objectives:

f) Optionally support EEE for 10 Gb/s rates or lower.

69.2 Summary of Backplane Ethernet Sublayers

69.2.3 Physical Layer signaling systems

Replace Table 69-1 with the following:

Table 69–1—Nomenclature and clause correlation

Nomenclature	Clause																			
	35		36	46		48	49	51	70	71	72	73	74	78	81		82	83	83A	84
	RS	GMII	1000BASE-X PCS/PMA	RS	XGMII	10GBASE-X PCS/PMA	10GBASE-R PCS	Serial PMA	1000BASE-KX PMD	10GBASE-KX4 PMD	10GBASE-KR PMD	Auto-Negotiation	BASE-R FEC	Energy Efficient Ethernet (EEE)	RS	XLGMII	40GBASE-R PCS	40GBASE-R PMA	XLAUI	40GBASE-KR4 PMD
1000BASE-KX	M[a]	O[a]	M						M			M		O						
10GBASE-KX4				M	O	M				M		M		O						
10GBASE-KR				M	O		M	M			M	M	O	O						
40GBASE-KR4												M	O		M	O	M	M	O	M

[a]O = Optional, M = Mandatory

Insert 69.2.6 as follows:

69.2.6 Low-Power Idle

With the optional EEE feature, described in Clause 78, Backplane Ethernet PHYs for 10Gb/s or lower can achieve lower power consumption during periods of low link utilization. The EEE capabilities are advertised during Auto-Negotiation for Backplane Ethernet. The Backplane Ethernet LPI allows each link direction to enter sleep, refresh or wake states asymmetric from the other direction.

70. Physical Medium Dependent Sublayer and Baseband Medium, Type 1000BASE-KX

70.1 Overview

Change Table 70-1 by inserting the row shown below as the last row of the table:

Table 70–1—PHY (Physical Layer) clauses associated with the 1000BASE-KX PMD

Associated clause	1000BASE-KX
78-- Energy Efficient Ethernet	Optional

Insert the following text at the end of section 70.1:

A 1000BASE-KX PHY with the optional Energy Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The "Assert LPI" request at the GMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as "Assert LPI" at the GMII. Upon the detection of "Assert LPI" at the GMII, an Energy Efficient 1000BASE-KX PHY continues transmitting for a pre-defined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the GMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the .

70.2 Physical Medium Dependent (PMD) service interface

Insert the following text at the end of section 70.2:

The PMD provides the following service interface signals if EEE is supported:

PMD_RXQUIET.request(rx_quiet)
PMD_TXQUIET.request(tx_quiet)

These messages signals are defined for the PCS in 36.2.5.1.6.

70.2.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into low power mode. See Clause 36.2.4.12a. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

70.2.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

70.2.1.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

70.2.1.3 Effect of receipt

This variable is from the receive process of the PCS to control the power saving function of the local PMD receiver. The 1000BASE-KX PHY receiver should put unused functional blocks into a low power state to save energy.

70.2.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a and to disable the PMD transmitter. See Clause 70.6.5. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

70.2.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

70.2.2.2 When generated

The PCS generates this primitive to request the appropriate PMD transmit LPI state.

70.2.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 70.6.5. The 1000BASE-KX PHY transmitter should put unused functional blocks into a lower power state to save energy.

70.6 PMD functional specifications

Change the text in 70.6.4 to read as follows:

70.6.4 PMD signal detect function

For 1000BASE-KX operation PMD signal detect is mandatory if EEE is supported. When EEE is not supported, the PMD signal detect is optional and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If EEE is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For EEE, the SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication is undefined. The signal energy from a compliant transmitter shall set

SIGNAL_DETECT to OK within 750 ns when transitioning from LPI quiet to active and set SIGNAL_DETECT to FAIL within 750 ns when transitioning from active to LPI quiet.

Change the 70.6.5 to read as follows:

70.6.5 PMD transmit disable function

The PMD transmit disable function is mandatory if EEE is supported and is otherwise optional. When implemented, it allows the transmitter to be disabled with a single variable.

a) When the PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 70–4.
b) If a PMD_fault (70.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 70.6.6, shall not be affected by PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_quiet is asserted within the time and voltage level specified in 70.7.1.5. The PMD_transmit_disable function shall turn on the transmitter after tx_quiet is de-asserted within a time and voltage level specified in 70.7.1.5.

Insert the following section after 70.6.9:

70.6.10 PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. EEE capabilities and parameters are advertised during the Backplane Auto-negotiation as described in Clause 45.2.7.13. The transmitter on the local device informs the link partner's receiver when to sleep, refresh and wake. The local receiver's transitions are controlled by the link partner's transmitter and change independently from the local transmitter's states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards /I/ during the wake phase.

If EEE is supported, the PMD transmit function enters into a when tx_quiet is set to TRUE and exits when tx_quiet is set to FALSE. While tx_quiet is TRUE the PMD transmitter functional blocks should be deactivated to conserve energy. The PMD receive function enters into a low power mode when rx_quiet is set to TRUE and exits when rx_quiet is set to FALSE. While rx_quiet is TRUE the PMD receiver functional blocks should be deactivated to conserve energy.

70.7 1000BASE-KX electrical characteristics

70.7.1 Transmitter characteristics

Change Table 70-4 as follows:

Transmitter characteristics at TP1 are summarized in Table 70–4 and detailed in 70.7.1.1 through 70.7.1.9.

Table 70–4—Transmitter characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Signaling speed	70.7.1.3	1.25 ± 100 ppm	GBd
Differential peak-to-peak output voltage	70.7.1.5	800 to 1600	mV
Differential peak-to-peak output voltage (max.) with TX disabled	70.6.5	30	mV
DC common-mode voltage limits	70.7.1.5	–0.4 to 1.9	V
Common-mode voltage deviation (max) during LPI	70.7.1.5	150	mV
Differential output return loss (min.)	70.7.1.6	[See Equation (70–1) and Equation (70–2)]	dB
Transition time[a] (20%–80%)	70.7.1.7	60 to 320	ps
Output jitter (max. peak-to-peak) Deterministic jitter[b] Random jitter Total jitter[c]	70.7.1.8	 0.10 0.15 0.25	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]Deterministic jitter is already incorporated into the differential output template.
[c]At BER 10^{-12}.

70.7.1.5 Output amplitude

Insert the following at the end of 70.7.1.5:

For EEE capability, the transmitter's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_quiet being asserted. Furthermore, the transmitters differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_quiet being de-asserted. The transmitter output shall be fully compliant within 5 µs after tx_quiet is set to FALSE. During LPI, the common mode shall be maintained to within +/- 150 mV of the pre-LPI value.

70.10 Protocol implementation conformance statement (PICS) proforma for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX[1]

Insert the following row at the end of the Table in Section 70.10.3:

70.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	LPI	70.6.10	Capable of LPI	O	Yes [ ] No [ ]

70.10.4 PICS proforma tables for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX.

Insert the following rows into the table in section 70.10.4.1:

70.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS5a	PMD Signal Detect during LPI	70.6.4	Indicate signal energy during LPI	LPI:M	Yes [ ] N/A [ ]
FS5b	Transmit Disable during LPI	70.6.5	Disable transmitter during tx_quiet	LPI:M	Yes [ ] N/A [ ]
FS5c	Signal Detect for EEE	70.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes[ ] N/A [ ]
FS5d	Transmit Disable	70.6.5	Disables Transmitter when PMD_Transmit_disable set to ONE	TD:M	Yes [ ] N/A [ ]
FS7a	tx_quiet disabled transmitter	70.7.1	Disables Transmitter when tx_quiet is asserted as specified in 70.7.1.5	LPI:M	Yes [ ] N/A [ ]

Insert the following rows into the table in section 70.10.4.4:

70.10.4.4 Transmitter electrical characteristics

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
TC8a	Output Amplitude LPI voltage	70.7.1.5	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC8b	Output Amplitude ON voltage	70.7.1.5	Greater than 720 mV within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] N/A [ ]

71. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KX4

71.1 Overview

Insert the following text at the end of section 71.1:

A 10GBASE-KX4 PHY with the optional Energy Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The "Assert LPI" request at the XGMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as "Assert LPI" at the XGMII. Upon the detection of "Assert LPI" at the XGMII, an Energy Efficient 10GBASE-KX4 PHY continues transmitting for a pre-defined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the XGMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

Change Table 71-1 by inserting the row shown below as a new row at the end of the table:

Table 71–1—PHY (Physical Layer) clauses associated with the 10GBASE-KX4 PMD

Associated clause	10GBASE-KX4
78--EEE	Optional

71.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KX4 PMD utilizes the PMD service interface defined in 53.1.1.

Insert the following text at the end of section 71.2:

The following primitives are defined on the PMD Service Interface when EEE is supported:

PMD_RXQUIET.request(rx_quiet)
PMD_TXQUIET.request(tx_quiet)

These messages are defined for the PCS in 48.2.6.1.6

71.2.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

71.2.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

71.2.1.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

71.2.1.3 Effect of receipt

This variable is from the Receive process of the PCS to control the power saving function of local receiver. The 10GBASE-KX4 PHY receiver should put unused functional blocks into a low power state to save energy.

71.2.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

71.2.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

71.2.2.2 When generated

The PCS generates this primitive to request the appropiate PMD transmit LPI state.

71.2.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 71.6.6. The 10GBASE-KX4 PHY transmitter should put unused functional block into a lower power state to save energy.

Change 71.6.4 to the following:

71.6.4 Global PMD signal detect function

For 10GBASE-KX4 operation Global PMD signal detect is mandatory if EEE is supported. When EEE is not implemented, the PMD signal detect is optional and its definition is beyond the scope of this standard. When Global PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If EEE is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For EEE, the SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_lane<3:0>) is undefined. The signal energy from a compliant transmitter shall set SIGNAL_DETECT to OK within 750 ns when transitioning from LPI quiet to active and set SIGNAL_DETECT to FAIL within 750 ns when transitioning from active to LPI quiet.

71.6.6 Global PMD transmit disable function

Change 71.6.6 to the following:

The Global_PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When implemented for normal operation, it allows all of the transmitters to be disabled with a single variable.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off all transmitter lanes after tx_quiet is asserted within a time and voltage level specified in 71.7.1.4. The PMD_transmit_disable function shall turn on all transmitter lanes after tx_quiet is de-asserted within a time and voltage level specified in 71.7.1.4.

Insert the following section after 71.6.11:

71.6.12 PMD LPI function

The PMD LPI function responds to transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. EEE capabilities and parameters, as described in 45.2.7, is advertised during the Backplane Auto-negotiation. The transmitter on the local device will inform the link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the link partner's transmitter and can change independent of the local transmitter states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards ||I|| during the wake phase.

If EEE is supported, the PMD transmit function enters into a low power mode when tx_quiet is set to TRUE and exits when tx_quiet is set to FALSE. While tx_quiet is TRUE the PMD transmitter functional blocks should be deactivated to conserve energy. The PMD receive function enters into a low power mode when rx_quiet is set to TRUE and exits when rx_quiet is set to FALSE. While rx_quiet is TRUE the PMD receiver functional blocks should be deactivated to conserve energy.

71.7 Electrical characteristics for 10GBASE-KX4

71.7.1 Transmitter characteristics

Change Table 71-4 as follows:

Transmitter characteristics at TP1 are summarized in Table 71–4.

Table 71–4—Transmitter characteristics for 10GBASE-KX4

Parameter	Subclause reference	Value	Units
Signaling speed, per lane	71.7.1.3	3.125 ± 100 ppm	GBd
Differential peak-to-peak output voltage	71.7.1.4	800 to 1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	71.6.6, 71.6.7	30	mV
Common-mode voltage limits	71.7.1.4	–0.4 to 1.9	V
Common-mode voltage deviation (max) during LPI	71.7.1.4	150	mV
Differential output return loss (min.)	71.7.1.5	[See Equation (71–1) and Equation (71–2)]	dB
Differential output template	71.7.1.6	[See Figure 71–5 and Table 71–5]	V
Transition time[a] (20%-80%)	71.7.1.7	60 to 130	ps
Output jitter (max. peak-to-peak) Random jitter Deterministic jitter Total jitter[b]	71.7.1.8	 0.27 0.17 0.35	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]At BER 10^{-12}.

71.7.1.4 Output amplitude

Insert the following at the end of 71.7.1.4:

For EEE capability, the transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_quiet being asserted. Furthermore, the transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_quiet being de-asserted. The transmitter output shall be fully compliant within 5 µs after tx_quiet is set to FALSE. During LPI, the common mode shall be maintained to within +/- 150mV of the pre-LPI value

71.7.2 Receiver characteristics

Modify Table 71-6 as follows:

Receiver characteristics at TP4 are summarized in Table 71–6 and detailed in 71.7.2.1 through 71.7.2.5.

Table 71–6—Receiver characteristics

Parameter	Subclause reference	Value	Units
Bit error ratio	71.7.2.1	10^{-12}	
Signaling speed, per lane	71.7.2.2	3.125 ± 100 ppm	GBd
Unit interval (UI) nominal	71.7.2.2	320	ps
Receiver coupling	71.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	71.7.2.4	1600	mV
EEE Signal Detect deactivation time (T_{SD}) from active to LPI quiet	71.6.4a	750	ns
EEE Signal Detect activation time (T_{SA}) from LPI quiet to active	71.6.4a	750	ns
Differential input return loss[a] (minimum)	71.7.2.5	[See Equation (71–1) and Equation (71–2)]	dB

[a]Relative to 100 Ω differential.

71.10 Protocol implementation conformance statement (PICS) proforma for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4[1]

Insert the following row at the end of the table in 71.10.3:

71.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	LPI function	71.6.10	LPI supported	O	Yes [ ] No [ ]

71.10.4 PICS proforma tables for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4

Insert the following rows into the table in section 71.10.4.2:

71.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS9a	Global_PMD_signal_detect during LPI	71.6.4	Detect signal energy during LPI	LPI:M	Yes [ ] N/A [ ]
FS9b	Signal Detect for EEE	71.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes [ ] N/A [ ]
FS12a	Global_PMD_transmit_disable during LPI	71.6.6	Disable transmitters during tx_quiet	LPI:M	Yes [ ] N/A [ ]
FS18	LPI function	71.6.12	PMD_RXQUIET.request and PMD_TXQUIET.request supported	LPI:M	Yes [ ] No [ ] N/A [ ]

Insert the following rows into the table in section 71.10.4.4:

71.10.4.2 Transmit electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC6a	Output Amplitude LPI voltage	71.7.1.4	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC6b	Output Amplitude ON voltage	71.7.1.4	Greater than 720 mV within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] N/A [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

72. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KR

72.1 Overview

Change table 72-1 to insert the row shown below as a new row at the end of the table:

Table 72–1—PHY (Physical Layer) clauses associated with the 10GBASE-KR PMD

Associated clause	10GBASE-KR
78—Energy Efficient Ethernet	Optional

Insert the following text at the end of section 72.1:

A 10GBASE-KR PHY with the optional Energy Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The "Assert LPI" request at the XGMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as "Assert LPI" at the XGMII. Upon the detection of "Assert LPI" at the XGMII, an Energy Efficient 10GBASE-KR PHY continues transmitting for a pre-defined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the XGMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

Change section 72.2 as follows:

72.2 Physical Medium Dependent (PMD) service interface

The PMD service interface is summarized as follows:

a) PMD_UNITDATA.request (as defined in 52.1.1)
b) PMD_UNITDATA.indication (as defined in 52.1.1)
c) PMD_SIGNAL.indication

If EEE is supported, the following primitives are also defined on the PMD Service Interface:

PMD_RX_MODE.request(rx_mode)
PMD_TX_MODE.request(tx_mode)

These messages are defined for the PCS in Clause 49.2.13.2.6.

72.2.1 PMD_RX_MODE.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_mode = DATA.

72.2.1.1 Semantics of the service primitive

PMD_RX_MODE.request (rx_mode)

The rx_mode parameter takes on one of two values: QUIET or DATA.

72.2.1.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

72.2.1.3 Effect of receipt

When rx_mode is QUIET, the PMD receive function may deactivate functional blocks to conserve energy. When rx_mode is DATA, the PMD receive function operates normally.

72.2.2 PMD_TX_MODE.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See sub-clause 72.6.5. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_mode = DATA.

72.2.2.1 Semantics of the service primitive

PMD_TX_MODE.request (tx_mode)

The tx_mode parameter takes on one of three ~~two~~ values: QUIET, ALERT, or DATA.

72.2.2.2 When generated

The PCS generates this primitive to request appropriate PMD transmit LPI state.

72.2.2.3 Effect of receipt

When tx_mode is QUIET, the PMD Transmit function may deactivate functional blocks to conserve energy. When tx_mode is ALERT, the PMD Transmit function transmits the alert pattern. And when it is DATA, the PMD Transmit function operates normally.

72.6 PMD functional specifications

72.6.2 PMD transmit function

Insert the following paragraphs at the end of section 72.6.2

If the optional Energy Efficient Ethernet (EEE) capability is supported (see Clause 78) then when tx_mode is set to ALERT, the PMD will transmit a repeating 16-bit pattern, hexadecimal 0xFF00. When tx_mode is ALERT, the transmitter equalizer taps are set to the preset state specified in 72.6.10.2.3.1. When tx_mode is DATA, the driver coeffcients are restored to their states resolved during training.

Change the text in section 72.6.4 to read as follows:

72.6.4 PMD signal detect function

The Global PMD signal detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is used by 10GBASE-KR to indicate the successful completion of the start-up protocol. When the PHY supports the optional EEE capability, PMD_SIGNAL.indication is also used to indicate when the ALERT signal is detected which corresponds to the beginning of a refresh or a wake. ~~PMD_SIGNAL.indication, while normally intended to be an indicator of signal presence, is used by 10GBASE-KR to indicate the successful completion of the start-up protocol.~~ If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.5.

The value of the SIGNAL_DETECT is defined by the training state diagram shown in Figure 72–5 when the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA. When the PHY supports the EEE capability, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that is the output of a channel that satisfies the requirements of all the parameters of both interference tolerance test channels defined in 72.7.2.1 when driven by a square wave pattern with a period of 16 unit intervals and peak-to-peak differential output amplitude of 720 mV. While rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after a valid ALERT signal is applied to the channel.

SIGNAL_DETECT shall be set to FAIL following system reset or the manual reset of the training state diagram. Upon completion of training, SIGNAL_DETECT shall be set to OK.

If training is disabled by management and EEE is not implemented, SIGNAL_DETECT shall be set to OK.

Change the text in 72.6.5 as indicated:

72.6.5 PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When this function is supported, it shall meet the requirements of this subclause.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 72–6.
b) If a PMD_fault (72.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 72.6.6, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 72.7.1.4. The PMD_transmit_disable function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 72.7.1.4.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.5.

Insert the following text at the end of 72.6.10.1:

72.6.10 PMD control function

72.6.10.1 Overview

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner.

The PMD control function implements the 10GBASE-KR start-up protocol. This protocol facilitates timing recovery and equalization while also providing a mechanism through which the receiver can tune the transmit equalizer to optimize performance over the backplane interconnect. The protocol supports these mechanisms through the continuous exchange of fixed-length training frames.

If EEE is supported, the PMD control function responds to PCS requests to transition in and out of quiet states.

Insert the following section after 72.6.10:

72.6.11. PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TX_MODE and PMD_RX_MODE requests. Implementation of the function is optional. EEE capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in Clause 45.2.7.13. The transmitter on the local device will inform the link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the link partner's transmitter and can change independent of the local transmitter states and transitions.

72.7 10GBASE-KR electrical characteristics

72.7.1 Transmitter characteristics

Change Table 72-6 as follows:

Transmitter characteristics at TP1 are summarized in Table 72–6 and detailed in 72.7.1.1 through 72.7.1.11.

Table 72–6—Transmitter characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Signaling speed	72.7.1.3	10.3125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	72.7.1.4	1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	72.6.5	30	mV
Common-mode voltage limits	72.7.1.4	0–1.9	V
Common-mode voltage deviation (max) during LPI	72.7.1.4	150	mV
Differential output return loss (min.)	72.7.1.5	[See Equation (72–4) and Equation (72–5)]	dB
Common-mode output return loss (min.)	72.7.1.6	[See Equation (72–6) and Equation (72–7)]	dB
Transition time (20%–80%)	72.7.1.7	24–47	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	72.7.1.8	 0.15 0.15 0.035 0.28	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

72.7.1.4 Output Amplitude

Insert the following at the end of 72.7.1.4:

For EEE capability, the transmitter's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_mode being set to QUIET and remain so while tx_mode is set to QUIET. Furthermore, the transmitter's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_mode being set to ALERT. The transmitter output shall be fully compliant within 5 μs after tx_mode is set to DATA. During LPI mode, the common mode shall be maintained to within +/- 150 mV of the pre-LPI value.

72.10 Protocol implementation conformance statement (PICS) proforma for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR[1]

Change the row for item FEC as shown below and insert a row for item LPI at the end of the table in section 72.10.3:

72.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
FEC	Forward Error Correction	72.1, 74	Device implements 10GBASE-R Forward Error Correction	O	Yes [ ] No [ ]
LPI	LPI	72.6.11	LPI	O	Yes [ ] No [ ]

72.10.4 PICS proforma tables for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR.

Insert the following rows into the table in section 72.10.4.2:

72.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS9a	Signal detect during LPI	72.6.4	Detect signal energy during LPI	LPI:M	Yes [ ] N/A[ ]
FS9b	Signal detect for EEE	72.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes [ ] N/A [ ]
FS10a	Transmit disable during LPI	72.6.5	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] N/A[ ]

Insert the following rows into the table in section 72.10.4.4:

72.10.4.4 Transmitter electrical characteristics

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Item	Feature	Subclause	Value/Comment	Status	Support
TC6a	Output Amplitude LPI voltage	72.7.1.4	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC6b	Output Amplitude ON voltage	72.7.1.4	Greater than 90% of previous level within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] N/A [ ]

73. Auto-Negotiation for Backplane Ethernet

73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for Backplane Ethernet[1]

73.11.4 PICS proforma tables for Auto-Negotiation for Backplane Ethernet.

73.11.4.9 Auto-Negotiation Annexes

Insert a new row at the end of the table in 73.11.4.9 as shown below:

Item	Feature	Subclause	Value/Comment	Status	Support
AN13	AN message code 10	73A.4	EEE technology message code	M	Yes [ ]

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74. Forward Error Correction (FEC) sublayer for BASE-R PHYs

74.4.1 Functional Block Diagram for 10GBASE-R PHYs

In 74.4.1 as modified by IEEE Std 802.3ba, replace Figure 74–2 as shown below:

Figure 74–2 shows the functional block diagram of FEC for 10GBASE-R PHY and the relationship between the PCS and PMA sublayers.

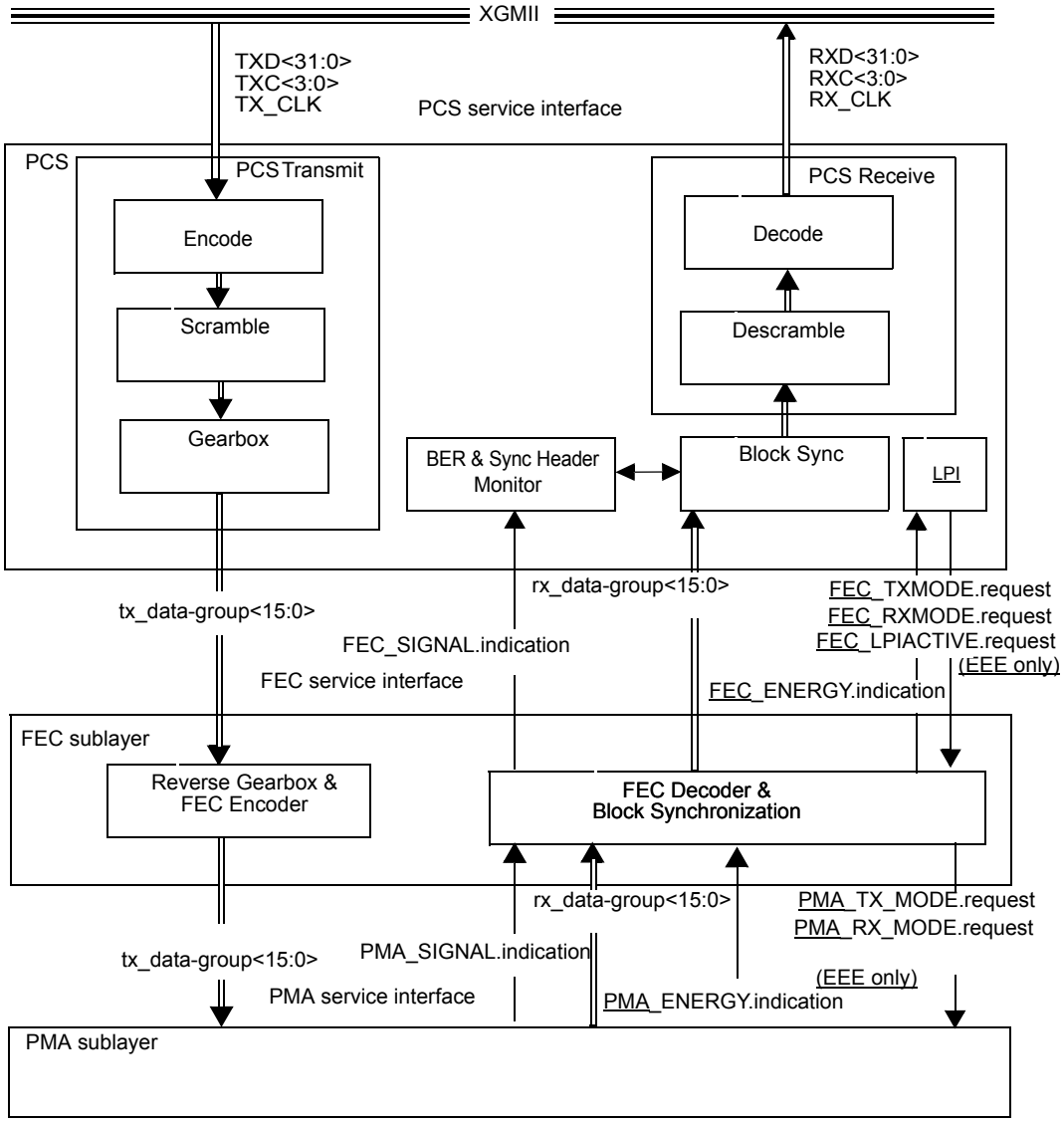

Figure 74–2—Functional block diagram for 10GBASE-R PHYs

74.5 FEC service interface

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Editor's Note: *To be removed prior to publication*

The changes in Clause 74 for EEE are only applicable to the 10GBASE-R PHY

74.5.1 10GBASE-R Service primitives

Change 74.5.1 as shown below by adding new primitive items after (c) and adding text as shown below:

The following primitives are defined within the FEC service interface:

a) FEC_UNITDATA.request(tx_data-group<15:0>)
b) FEC_UNITDATA.indication(rx_data-group<15:0>)
c) FEC_SIGNAL.indication(SIGNAL_OK)
d) FEC_TX_MODE.request(tx_mode)
e) FEC_RX_MODE.request(rx_mode)
f) FEC_ENERGY.indication(energy_detect)
g) FEC_LPI_ACTIVE.request(rx_lpi_active)

Items d, e, f and g are only required for the optional EEE capability.

The FEC service interface directly maps to the PMA service interface of the 10GBASE-R PCS defined in Clause 49. The FEC_UNITDATA.request maps to the PMA_UNITDATA.request primitive, the FEC_UNITDATA.indication maps to the PMA_UNITDATA.indication primitive, and the FEC_SIGNAL.indication maps to the PMA_SIGNAL.indication primitive of the 10GBASE-R PCS.

If the optional Energy Efficient Ethernet (EEE) capability is supported (see Clause 78) then the interface with the PMA sublayer (or FEC sublayer) includes rx_mode and tx_mode to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver.

Insert 74.5.1.4 through 74.5.1.7 as shown below after 74.5.1.3:

74.5.1.4 FEC_ENERGY.indication (optional)

FEC_ENERGY.indication(energy_detect)

A boolean variable that reflects the value of the energy detection primitive PMA_ENERGY.indication.

74.5.1.4.1 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.5 FEC_LPI_ACTIVE.request (optional)

FEC_LPI_ACTIVE.request(rx_lpi_active)

The rx_lpi_active parameter is a boolean variable sent from the PCS that is set to TRUE when LPI mode is active at the receiver and set to FALSE otherwise.

74.5.1.5.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.5.2 Effect of receipt

When rx_lpi_active is TRUE, rapid block lock as specified in 74.5.1.8 will be used to quickly determine the start of the FEC block during EEE REFRESH or WAKE. When rx_lpi_active is FALSE, rapid block lock will not be used.

74.5.1.6 FEC_RX_MODE.request (optional)

FEC_RX_MODE.request(rx_mode)

The rx_mode parameter is a variable sent from the PCS. It is set to QUIET while the receiver is in the RX_QUIET state and is set to DATA otherwise.

74.5.1.6.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.6.2 Effect of receipt

When rx_mode is QUIET, the FEC decoder logic may deactivate functional blocks to conserve energy. When rx_mode is DATA, the FEC decoder logic operates normally. The value rx_mode is passed to the client layer through PMA_RX_MODE(rx_mode).request.

74.5.1.7 FEC_TX_MODE.request (optional)

FEC_TX_MODE.request(tx_mode)

The tx_mode parameter is a variable sent from the PCS. It is set to QUIET while the transmitter is in the TX_QUIET state, it is set to ALERT while the transmitter is in the TX_ALERT state and is set to DATA otherwise.

74.5.1.7.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.7.2 Effect of receipt

When tx_mode is QUIET or ALERT, the FEC encoder logic may deactivate functional blocks to conserve energy. When tx_mode is DATA, the FEC encoder logic operates normally. The value tx_mode is passed to the client layer through PMA_TX_MODE(tx_mode).request.

Insert new subclause 74.7.4.8 after 74.7.4.7 as shown below:

74.7.4.8 FEC rapid block synchronization for EEE (optional)

If the optional EEE capability is supported then during the wake and refresh states the FEC decoder will be receiving one of the two types of deterministic blocks to achieve rapid block synchronization. During these

states the reverse gearbox of the remote FEC encoder will be receiving unscrambled data from the PCS sub-layer via 16-bit FEC_UNITDATA.request primitive. PCS sublayer will be encoding /I/ during the wake state and /LI/ during the refresh state, which produces the two types of deterministic FEC blocks.

When rx_lpi_active is TRUE and rx_mode is set to DATA, start a hold off timer whose duration is greater than or equal to 13.7μs and enable the FEC Rapid block lock mechanism, which will attempt to determine the FEC start of block location based on the deterministic pattern. When the rapid block lock is locked, the determined start of block location is used as the FEC lock state diagram candidate start of block location until the rapid block lock loses lock. Assuming the rapid block lock determined the correct start of block location, the FEC lock state diagram will achieve lock without requiring subsequent slips. The rapid block lock mechanism is implementation dependent and outside the scope of this standard. The FEC sub-layer shall hold off asserting SIGNAL_OK until one of the following two events occurs:

1) Two 65b payload blocks after the transition from deterministic FEC block to normal scrambled FEC block.

2) Expiration of the hold off timer

74.8.4 FEC Error monitoring capability

Change 74.8.4 by inserting a sentence after the first paragraph in 74.8.4 as shown below:

The following counters apply to FEC sublayer management and error monitoring. If an MDIO interface is provided (see Clause 45), it is accessed via that interface. If not, it is recommended that an equivalent access be provided. These counters are reset to zero upon read or upon reset of the FEC sublayer. When a counter reaches all ones, it stops counting. The counters' purpose is to help monitor the quality of the link.

These counters shall be disabled if FEC_LPI_ACTIVE.request(rx_lpi_active) is TRUE.

74.10.2.3 Functions

Change the third paragraph of 74.10.2.3 as shown below:

~~T_TYPE_NEXT~~

~~Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.~~

74.11 Protocol implementation conformance statement (PICS) proforma for Clause 74, Forward Error Correction (FEC) sublayer for BASE-R PHYs[1]

74.11.3 Major capabilities/options

Change 74.11.3 by adding one more row after the last one as shown below:

Item	Feature	Subclause	Value/Comment	Status	Support
EEE	Rapid Block Lock	74.7.4.8	Device implements Rapid block lock mechanism to support EEE	O	Yes[]/ No[]

74.11.6 FEC Error Monitoring

Change 74.11.6 by adding one more row after the last one as shown below:

Item	Feature	Subclause	Value/Comment	Status	Support
FEM4	FEC Error Monitoring during EEE	74.8.4	Disables FEC Error Monitoring during EEE as specified in 74.8.4	EEE:M	Yes[]

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78. Energy Efficient Ethernet (EEE)

78.1 Overview

The optional EEE capability combines the IEEE 802.3 Media Access Control (MAC) Sublayer with a family of Physical Layers defined to support operation in the Low Power Idle (LPI) mode. When the LPI mode is enabled, systems on both sides of the link can save power during periods of low link utilization.

EEE also provides a protocol to coordinate transitions to or from a lower level of power consumption and does this without changing the link status and without dropping or corrupting frames. The transition time in to and out of the lower level of power consumption is kept small enough to be transparent to upper layer protocols and applications.

For operation over twisted pair cabling systems, EEE supports the 100BASE-TX PHY, the 1000BASE-T PHY and the 10GBASE-T PHY. For operation over electrical backplanes, EEE supports the 1000BASE-KX PHY, the 10GBASE-KX4 PHY and the 10GBASE-KR PHY. EEE also supports XGMII extension using the XGXS for 10 Gb/s PHYs.

In addition to the above, EEE defines a 10 Mb/s MAU (10BASE-Te) with reduced transmit amplitude requirements. The 10BASE-Te MAU is fully interoperable with 10BASE-T MAUs over 100 m of class D (Category 5) or better cabling as specified in ISO/IEC 11801:1995. These requirements can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-B-1995. The definition of 10BASE-Te allows a reduction in power consumption.

EEE also specifies means to exchange capabilities between link partners to determine whether EEE is supported and to select the best set of parameters common to both devices. Clause 78 provides an overview of EEE operation. PICS for the optional EEE capability for each specific PHY type are specified in the respective PHY clauses. 78.4 contains the normative requirements for the Data Link Layer capabilities.

78.1.1 LPI Signaling

LPI signaling allows the LPI Client to indicate to the PHY, and to the link partner, that a break in the data stream is expected and the LPI Client can use this information to enter power saving modes that require additional time to resume normal operation. LPI signaling also informs the LPI Client when the link partner has sent such an indication.

The definition of LPI signaling assumes the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in the LPI mode.

78.1.1.1 Interlayer service interfaces

Figure 78–1 depicts the LPI Client and the RS interlayer service interfaces.

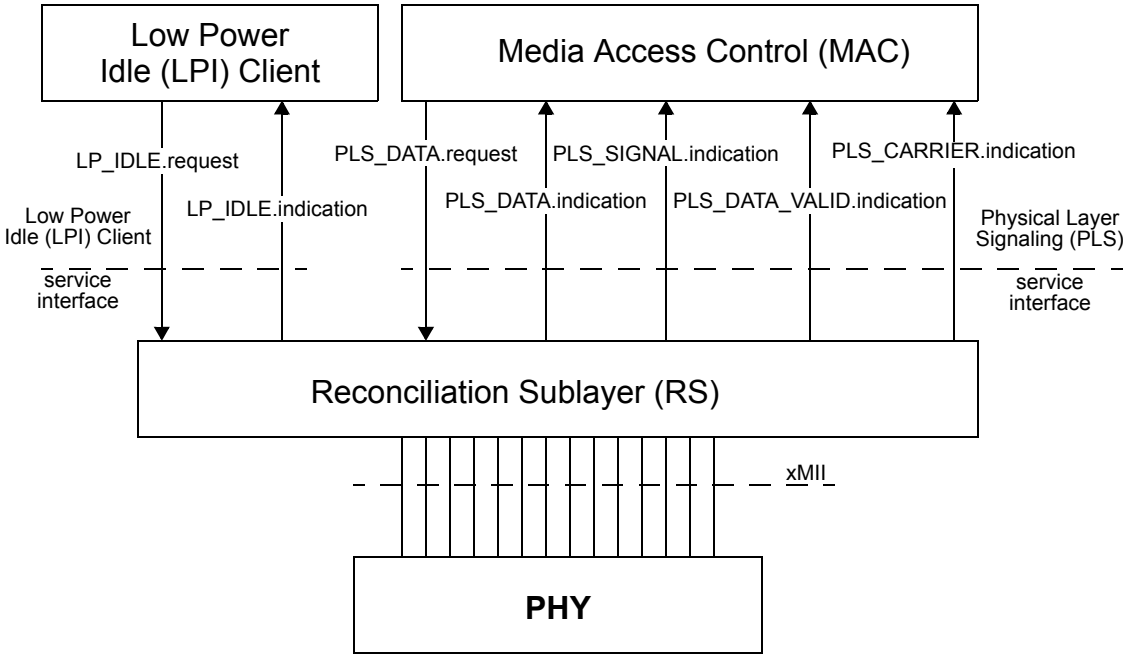


Figure 78–1—LPI Client and RS interlayer service interfaces

78.1.1.2 Responsibilities of LPI Client

The decision on when to signal LPI to the link partner is made by the LPI Client and communicated to the PHY through the RS. The LPI Client is also informed when the link partner is signaling LPI by the RS.

The conditions under which the LPI Client decides to send LPI, and what action are taken by the LPI Client when it receives LPI from the link partner, are implementation specific and beyond the scope of this standard.

78.1.2 LPI Client service interface

The following specifies the service interface provided by the RS to the LPI Client. These services are described in an abstract manner and do not imply any particular implementation.

The following primitives are defined:

LP_IDLE.request
LP_IDLE.indication

78.1.2.1 LP_IDLE.request

78.1.2.1.1 Function

A primitive used by the LPI Client to start or stop the signaling of LPI to the link partner.

78.1.2.1.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

LP_IDLE.request (LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT initiates the signaling of LPI to the link partner. DE-ASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined in any of the following cases:

a) link_status is not OK (see 28.2.6.1.1)
b) LPI_REQUEST=ASSERT within 1 second of the change of link_status to OK.
c) The PHY is indicating LOCAL FAULT
d) The PHY is indicating REMOTE FAULT

78.1.2.1.3 When generated

Specification of the time when this primitive is generated by the LPI client is out of the scope of this standard.

78.1.2.1.4 Effect of receipt

The receipt of this primitive will cause the RS to start or stop signaling LPI to the link partner.

78.1.2.2 LP_IDLE.indication

78.1.2.2.1 Function

A primitive that is used to indicate to the LPI Client that the link partner has started or stopped signaling LPI.

78.1.2.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

LP_IDLE.indication (LPI_INDICATION)

The LPI_INDICATION parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT indicates that the link partner has started signaling LPI. DE-ASSERT indicates that the link partner has stopped signaling LPI.

78.1.2.2.3 When generated

This primitive is generated by the PHY when it receives an LPI signal or a wake signal from its link partner.

78.1.2.2.4 Effect of receipt

The effect of receipt of this primitive by the LPI client is unspecified.

78.1.3 Reconciliation sublayer operation

LPI assert and detect functions are contained in the Reconciliation Sublayer as shown in Figure 78–2. The xMII interface in this diagram represents any of the family of medium independent interfaces supported by EEE.

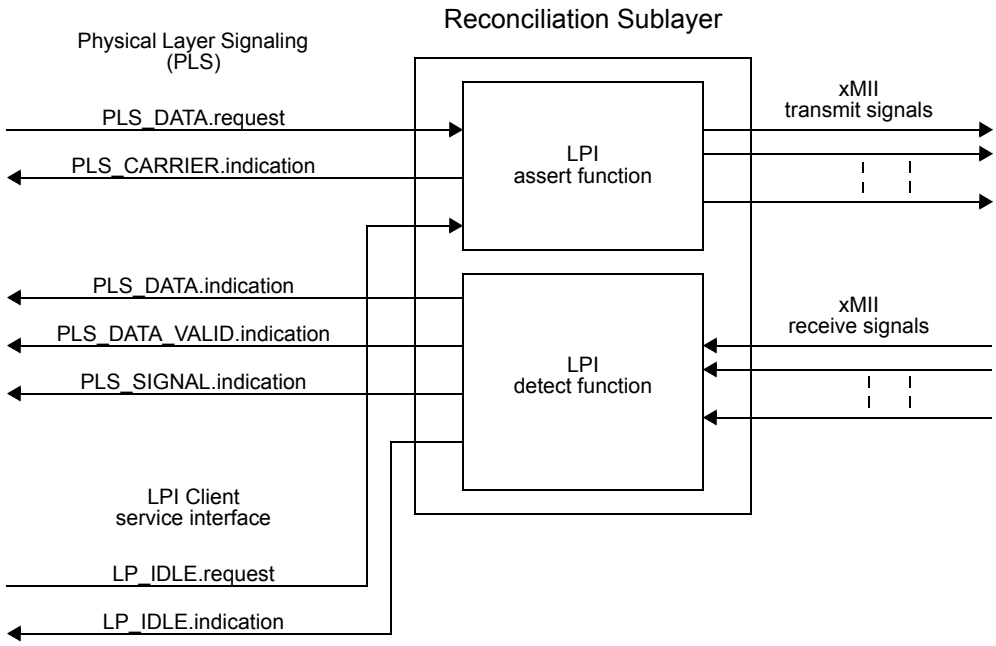


Figure 78–2—RS LPI assert and detect functions

The following provides an overview of RS LPI operation. The actual specification of RS LPI operation can be found in the respective RS clauses.

78.1.3.1 RS LPI assert function

In the absence of an LPI request, indicated by the LPI_REQUEST parameter set to DE-ASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function maps the PLS service interface to the transmit xMII signals as under normal conditions.

When an LPI request is asserted, indicated by the LPI_REQUEST parameter set to ASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function starts to transmit the 'Assert LPI' encoding on the xMII. The LPI assert function also sets the CARRIER_STATUS parameter to CARRIER_ON in the PLS_CARRIER.indication primitive of the PLS service interface. This will prevent the MAC from transmitting.

When the LPI request is de-asserted, indicated by the LPI_REQUEST parameter set to DE-ASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function starts to transmit the normal inter-frame encoding on the xMII. After a delay, the LPI assert function sets the CARRIER_STATUS parameter to CARRIER_OFF in the PLS_CARRIER.indication primitive of the PLS service interface, allowing the MAC to start transmitting again. This delay is provided to allow the link partner to prepare for normal operation. This delay has a PHY dependent default value but this value can be adjusted using the Data Link Layer capabilities defined in 78.4.

78.1.3.2 LPI detect function

In the absence of LPI, indicated by an encoding other than 'Assert LPI' on the receive xMII, the LPI detect function maps the receive xMII signals to the PLS service interface as under normal conditions.

At the start of LPI, indicated by the transition from normal inter-frame encoding to the 'Assert LPI' encoding on the receive xMII, the LPI detect function continues to indicate idle on the PLS service interface, but sets LP_IDLE.indication(LPI_INDICATION) to ASSERT.

At the end of LPI, indicated by the transition from the 'Assert LPI' encoding to any other encoding on the receive xMII, LP_IDLE.indication(LPI_INDICATION) is set to DE-ASSERT and the RS receive function resumes normal decode operation.

78.1.3.3 PHY LPI operation

The following provides an overview of PHY LPI operation. The specification of PHY LPI operation can be found in the respective PHY clauses (see Table 78–1).

78.1.3.3.1 PHY LPI transmit operation

When the start of 'Assert LPI' encoding on the xMII is detected, the PHY signals sleep to its link partner to indicate that the local transmitter is entering LPI mode.

The EEE capability in most PHYs (for example, 100BASE-TX, 10GBASE-T, 1000BASE-KX, 10GBASE-KR and 10GBASE-KX4) requires the local PHY transmitter to go quiet after sleep is signalled.

In the 1000BASE-T LPI mode, the local PHY transmitter goes quiet only after the local PHY signals sleep and receives a sleep signal from the remote PHY. If the remote PHY chooses not to signal LPI, then neither PHY can go into a low power mode, however LPI requests are passed from one end of the link to the other regardless and system energy savings can be achieved even if the PHY link does not go into a low power mode.

The transmit function of the local PHY is enabled periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity.

This quiet-refresh cycle continues until the reception of the normal inter-frame encoding on the xMII. The transmit function in the PHY communicates this to the link partner by sending a wake signal for a predefined period of time. The PHY then enters the normal operating state.

Figure 78–3 illustrates general principles of the EEE-capable transmitter operation.

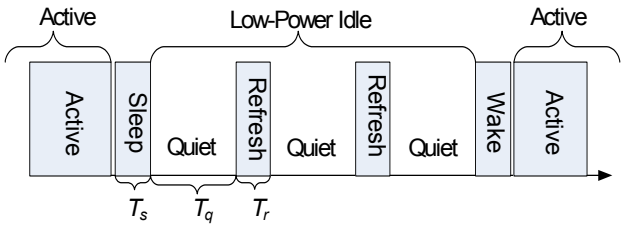


Figure 78–3—Overview of EEE LPI operation

No data frames are lost or corrupted during the transition to or from the LPI mode.

78.1.3.3.2 PHY LPI receive operation

In the receive direction, entering the LPI mode is triggered by the reception of a sleep signal from the link partner, which indicates that the link partner is about to enter the LPI mode. After sending the sleep signal, the link partner ceases transmission. When the receiver detects the sleep signal, the local PHY indicates 'Assert LPI' on the xMII and the local receiver can disable some functionality to reduce power consumption.

The link partner periodically transmits refresh signals that are used by the local PHY to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner initiates transition back to normal mode by transmitting the wake signal for a pre-determined period of time controlled by the LPI assert function in the RS. This allows the local receiver to prepare for normal operation and transition from the 'Assert LPI' encoding to the normal inter-frame encoding on the xMII. After a system specified recovery time, the link supports the nominal operational data rate.

78.1.4 EEE Supported PHY types

EEE defines a low power mode of operation for the 802.3 PHYs listed in Table 78–1. The table also lists the clauses associated with each PHY. Normative requirements for the EEE capability for each PHY type are in the associated clauses.

Table 78–1—Clauses associated with each PHY type

PHY type	Clause
10BASE-Te	14
100BASE-TX	24, 25
1000BASE-T	40
XGXS (XAUI)	47
1000BASE-KX	70, 35
10GBASE-T	55
10GBASE-KX4	71, 48
10GBASE-KR	72, 51, 49

78.2 LPI mode timing parameters description

T_s: The period of time that the PHY transmits the sleep signal before turning all transmitters off

T_q: The period of time that the PHY remains quiet before sending the refresh signal

T_r: Duration of the refresh signal

$T_{phy\_prop\_tx}$ The propagation delay of a given unit of data from the xMII to the MDI

$T_{phy\_prop\_rx}$ The propagation delay of a given unit of data from the MDI to the xMII

$T_{phy\_shrink\_tx}$ Transmitter shrinkage time is defined as the absolute time difference between the following two timing parameters:

- the delay between a transition from the 'Assert LPI' to "Normal Idle" at the xMII interface and the corresponding start of the wake signal at the MDI
- $T_{phy\_prop\_tx}$

$T_{phy\_shrink\_rx}$ Receiver shrinkage time is defined as the absolute time difference between the following two timing parameters:
- the delay between start of the wake signal at the MDI and the corresponding transition from 'Assert LPI' to "Normal Idle" at the xMII
- $T_{phy\_prop\_rx}$

T_{w_phy}: Parameter employed by the system which corresponds to the behavior of the PHY. It is the period of time between reception of an IDLE signal on the xMII interface and when the first data codewords are permitted on the xMII interface. The wake time of a compliant PHY does not exceed T_{w_phy} (min)

$T_{w\_sys\_tx}$: Parameter employed by the system which corresponds to its requirements. It is the longest period of time the system has to wait between a request to transmit and its readiness to transmit.

$T_{w\_sys\_rx}$: Parameter employed by the system which corresponds to its requirements. It is the minimum time required by the system between a request to wake and its readiness to receive data.

Table 78–2 summarizes three key EEE parameters (T_s, T_q, and T_r) for supported PHYs.

Table 78–2—Summary of the key EEE parameters for supported PHYs

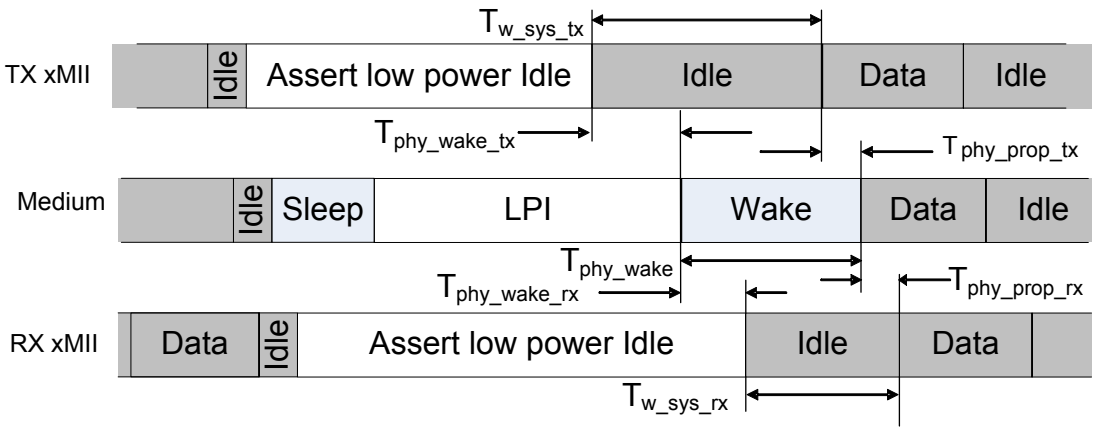
Protocol	T_s μs		T_q μs		T_r μs	
	min	max	min	max	min	max
100BASE-TX	200	220	20,000	22,000	200	220
1000BASE-T	182.0	202.0	20,000	24,000	198.0	218.2
1000BASE-KX	19.9	20.1	2,500	2,600	19.9	20.1
XGXS (XAUI)	19.9	20.1	2,500	2,600	19.9	20.1
10GBASE-KX4	19.9	20.1	2,500	2,600	19.9	20.1
10GBASE-KR	4.9	5.1	1,700	1,800	16.9	17.5
10GBASE-T	2.88	3.2	39.68	39.68	1.28	1.28

Figure 78–4 illustrates the relationship between the LPI mode timing parameters and the minimum system wake time.

78.3 Capabilities Negotiation

The EEE capability shall be advertised during the Auto-Negotiation stage. Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed at power up, on command from management, due to link failure, or due to user intervention.

During Auto-Negotiation, both link partners indicate their EEE capabilities. EEE is supported only if during auto-negotiation both the local device and link partner advertise the EEE capability for the resolved PHY type. If EEE is not supported, all EEE functionality is disabled and the LPI client does not assert LPI. If EEE is supported by both link partners for the negotiated PHY type then the EEE function can be used independently in either direction.



$T_{w\_sys\_tx}$ (min) = $T_{w\_sys\_rx}$ (min) + $T_{phy\_shrink\_tx}$ (max) + $T_{phy\_shrink\_rx}$ (max)
T_{w_phy} (min) = T_{phy_wake} (min) + $T_{phy\_shrink\_tx}$

$T_{w\_sys\_res}$ (min) is greater of $T_{w\_sys\_tx}$ (min) and T_{w_phy} (min)

$T_{phy\_shrink\_tx}$ (max) = ($T_{phy\_wake\_tx}$ (max) - $T_{phy\_prop\_tx}$ (min))
$T_{phy\_shrink\_rx}$ (max) = ($T_{phy\_wake\_rx}$(max) - $T_{phy\_prop\_rx}$ (min))

Where:

$T_{phy\_wake\_tx}$: xMII start of wake to MDI start of wake delay
$T_{phy\_prop\_tx}$: xMII to MDI data propagation delay
$T_{phy\_wake\_rx}$: MDI start of wake to xMII start of wake delay
$T_{phy\_prop\_rx}$: MDI to xMII data propagation delay
T_{phy_wake} : Minimum wake duration required by PHY

Figure 78–4—LPI mode timing parameters and their relationship to minimum system wake time

Additional capabilities and settings using L2 protocol frames, including the adjustment of the $T_{w\_sys\_tx}$ parameter, are described in 78.4.

78.4 Data Link Layer Capabilities

Additional capabilities and settings are supported using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Annex G of IEEE Std 802.1AB protocol (LLDP). Devices that require longer wake up times prior to being able to accept data on their receive paths may use the Data Link Layer capabilities defined in this section to negotiate for extended system wake up times from the transmitting link partner. This mechanism may allow for more or less aggressive energy saving modes.

The Data Link Layer capabilities shall be implemented for devices with an operating speed equal to or greater than 10 Gb/s and may be implemented for all other devices.

Implementations that use the Data Link Layer capabilities shall comply with all mandatory parts of IEEE Std 802.1AB; shall support the EEE Type, Length, Value (TLV) defined in 79.3.a; timing requirement in 78.4.1; and shall support the control state diagrams defined in 78.4.2.

The Data Link Layer capabilities are described from a unidirectional perspective on the link between transmitting and receiving link partners. For duplex EEE links that implement the Data Link Layer capabilities, each link partner shall implement the TLV, control and state diagrams for a transmitter as well as a receiver.

For purposes of Data Link Layer capabilities, all values that are negotiated and/or exchanged that have a fractional value shall be rounded up to the nearest integer number in microseconds.

78.4.1 Data Link Layer capabilities timing requirements

An EEE link partner shall send an LLDPDU containing an EEE TLV within 10 seconds of the Link Layer capability exchange being enabled when both the variables dll_enabled and dll_ready are asserted.

Editor's Notes: To be removed prior to publication
aLldpXdot3LocDllEnabled is the attribute required by the adopted baseline, described in diab_01_0409.pdf, that maps to tx_dll_enabled and rx_dll_enabled which is set at the end of a successful auto-negotiation between EEE capable PHYs upon receipt of a EEE capability message.

An LLDPDU containing an EEE TLV with an updated value for the "Echo Transmit $T_{w\_sys\_tx}$" field shall be sent within 10 seconds of receipt of an LLDPDU containing an EEE TLV where the value of "Transmit $T_{w\_sys\_tx}$" field is different from the previously communicated value.

An LLDPDU containing an EEE TLV with an updated value for the "Echo Receive $T_{w\_sys\_tx}$" field shall be sent within 10 seconds of receipt of an LLDPDU containing an EEE TLV where the value of "Receive $T_{w\_sys\_tx}$" field is different from the previously communicated value.

78.4.2 Control state diagrams

The control state diagrams for an EEE transmitting link partner and an EEE receiving link partner specify the externally observable behavior of an EEE transmitting link partner and an EEE receiving link partner implementing Data Link Layer capabilities respectively. EEE transmitting link partners implementing Data Link Layer capabilities shall provide the behavior of the state diagram as shown in Figure 78–5. EEE receiving link partners implementing Data Link Layer capabilities shall provide the behavior of the state diagram as shown in Figure 78–6.

78.4.2.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

78.4.2.2 Constants

PHY WAKE VALUE
: Integer (2 octets wide) representing the $T_{w\_sys\_tx}$ *(min)* defined for the PHY that is in use for the link. This parameter should be rounded up to the nearest integer number when it is calculated and examined according to 78.2 and Table 78–4.

78.4.2.3 Variables

Unless otherwise specified, all integers are assumed to be 2 octets wide

LocTxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the local system can support. This value is updated by the EEE DLL Transmitter state diagram. This variable maps into the aLldpXdot3LocTxTwSys attribute.

RemTxSystemValueEcho
: Integer that indicates the value Transmit $T_{w\_sys\_tx}$ echoed back by the remote system. This value maps from the aLldpXdot3RemTxTwSysEcho attribute.

LocRxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the local system requests from the remote system. This value is updated by the EEE Receiver L2 state diagram. This variable maps into the aLldpXdot3LocRxTwSys attribute.

RemRxSystemValueEcho
: Integer that indicates the value of Receive $T_{w\_sys\_tx}$ echoed back by the remote system. This value maps from the aLldpXdot3RemRxTwSysEcho attribute.

LocFbSystemValue
: Integer that indicates the value of fallback $T_{w\_sys\_tx}$ that the local system requests from the remote system. This value is updated by the local system software.

RemTxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the remote system can support. This value maps from the aLldpXdot3RemTxTwSys attribute.

LocTxSystemValueEcho
: Integer that indicates the remote system's Transmit $T_{w\_sys\_tx}$ that was used by the local system to compute the $T_{w\_sys\_tx}$ that it wants to request from the remote system. This value maps into the aLldpXdot3LocTxTwSysEcho attribute.

RemRxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the remote system requests from the local system. This value maps from the aLldpXdot3RemRxTwSys attribute.

LocRxSystemValueEcho
: Integer that indicates the remote systems Receive $T_{w\_sys\_tx}$ that was used by the local system to compute the $T_{w\_sys\_tx}$ that it can support. This value maps into the aLldpXdot3LocRxTwSysEcho attribute.

LocResolvedTxSystemValue
: Integer that indicates the current $T_{w\_sys\_tx}$ supported by the local system.

LocResolvedRxSystemValue
: Integer that indicates the current $T_{w\_sys\_tx}$ supported by the remote system.

TempTxVar
: Integer used to store the value of $T_{w\_sys\_tx}$.

TempRxVar
: Integer used to store the value of $T_{w\_sys\_tx}$.

local_system_change
: An implementation specific control variable that indicates that the local system wants to change either the Transmit $T_{w\_sys\_tx}$ or the Receive $T_{w\_sys\_tx}$.

tx_dll_ready
: Data Link Layer ready: This variable indicates that the tx system initialization is complete and is ready to update/receive LLDPDU containing EEE TLV. This variable is updated by the local system software.

rx_dll_ready
: Data Link Layer ready: This variable indicates that the rx system initialization is complete and is ready to update/receive LLDPDU containing EEE TLV. This variable is updated by the local system software.

NEW_TX_VALUE
: Integer that indicates the value of Tw_sys_tx that the local system can support.

NEW_RX_VALUE
: Integer that indicates the value of Tw_sys_tx that the local system wants the remote system to support.

A summary of cross-references between the EEE object class attributes and the transmit and receive control state diagrams, including the direction of the mapping, is provided in Table 78–3.

Table 78–3—Attribute to state diagram variable cross-reference

Entity	Object Class	Attribute	Mapping	State diagram variable
TX	oLldpXdot3LocSystems-Group	aLldpXdot3LocTxTwSys	⇐	LocTxSystemValue
		aLldpXdot3LocRxTwSysEcho	⇐	LocRxSystemValueEcho
		aLldpXdot3LocDllEnabled	⇒	tx_dll_enabled
		aLldpXdot3LocTxDllReady	⇐	tx_dll_ready
	oLldpXdot3RemSystems-Group	aLldpXdot3RemRxTwSys	⇒	RemRxSystemValue
		aLldpXdot3RemTxTwSysEcho	⇒	RemTxSystemValueEcho

Table 78–3—Attribute to state diagram variable cross-reference *(continued)*

Entity	Object Class	Attribute	Mapping	State diagram variable
RX	oLldpXdot3LocSystems-Group	aLldpXdot3LocRxTwSys	⇐	LocRxSystemValue
		aLldpXdot3LocTxTwSysEcho	⇐	LocTxSystemValueEcho
		aLldpXdot3LocFbTwSys	⇐	LocFbSystemValue
		aLldpXdot3LocDllEnabled	⇒	rx_dll_enabled
		aLldpXdot3LocRxDllReady	⇐	rx_dll_ready
	oLldpXdot3RemSystems-Group	aLldpXdot3RemTxTwSys	⇒	RemTxSystemValue
		aLldpXdot3RemRxTwSysEcho	⇐	RemRxSystemValueEcho

78.4.2.4 Functions

examine_Tx_change

This function computes the new value of $T_{w\_sys\_tx}$ that the local system can support when there is as updated request from the remote system or if local system conditions require a change in the value of the presently supported $T_{w\_sys\_tx}$. This function returns the following variable.

examine_Rx_change

This function computes the new value of $T_{w\_sys\_tx}$ that the local system wants the remote system to support. This function is called when the remote system wants to change its presently allocated $T_{w\_sys\_tx}$ or if local system conditions require a change in the value of $T_{w\_sys\_tx}$ presently supported by the remote system. This function returns the following variable.

78.4.2.5 State diagrams

Control for placing data on the medium rests with the transmitting side, hence $T_{w\_sys\_tx}$ is enforced by the transmitter. For a given path between link partners (i.e. a transmitter and its associated receiver), the transmitting link partner shall wait for the time indicated by the Transmit $T_{w\_sys\_tx}$ after de-asserting LPI (at the xMII) before sending data frames. The receiving link partner shall be ready to accept data based on its echoed value of Transmit link partner's $T_{w\_sys\_tx}$. This ensures that the link partners transition out of LPI mode and receive frames without loss or corruption.

The general state change procedure for transmitter is shown in Figure 78–5.

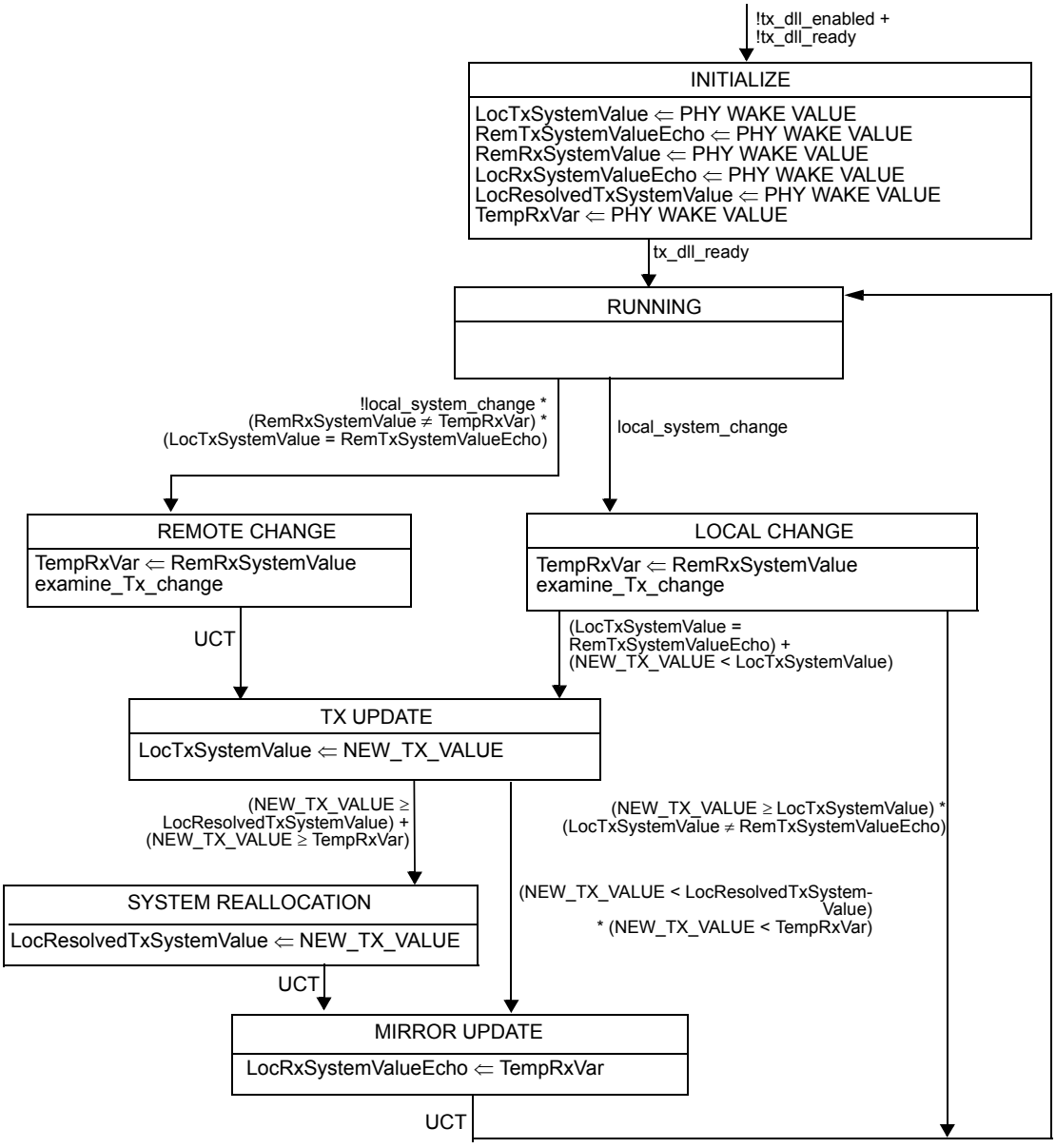


Figure 78–5—EEE DLL Transmitter State Diagram

The general state change procedure for receiver is shown in Figure 78–6.

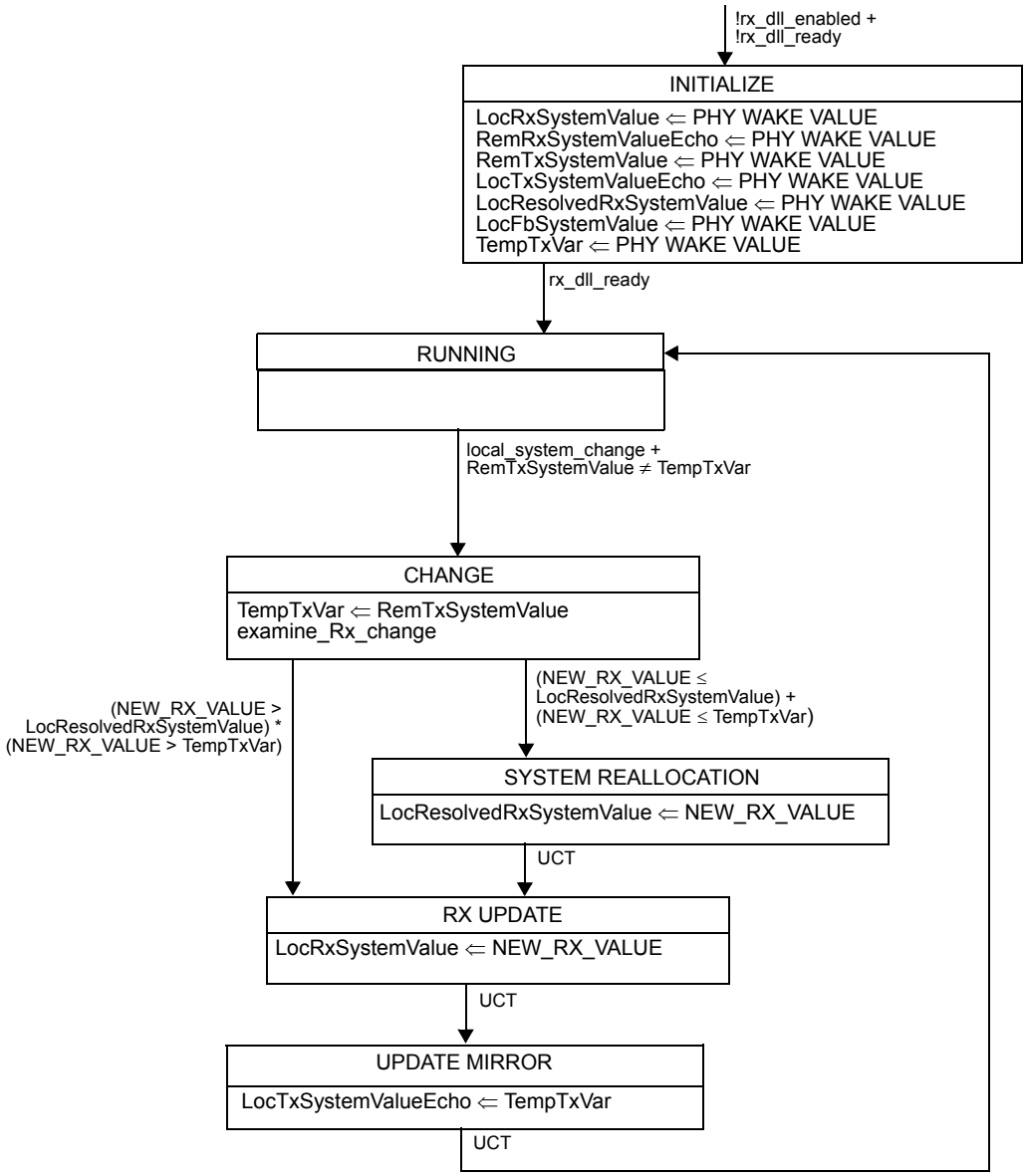


Figure 78–6—EEE DLL Receiver State Diagram

78.4.3 State change procedure across a link

The transmitting and receiving link partners utilize the LLDP mechanism to advertise their various attributes to the other entity.

The initial $T_{w\_sys\_tx}$ defaults governing the EEE operation of the link default to the wake values required by the PHYs. This provides for EEE operation and functionality on initialization and prior to the exchange and processing of the TLVs.

The receiving link partner may request a new $T_{w\_sys\_tx}$ value through the aLldpXdot3LocRxTwSys (30.12.2.1.24) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The request appears to the transmitting link partner as a change to the aLldpXdot3RemRxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The transmitting link partner responds to its receiving partner's request through the aLldpXdot3LocTxTwSys (30.12.2.1.22) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The transmitting link partner also copies the value of the aLldpXdot3RemRxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocRxTwSysEcho (30.12.3.1.19) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2).

The transmitting link partner may advertise new value of $T_{w\_sys\_tx}$ through the aLldpXdot3LocTxTwSys (30.12.2.1.22) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the receiving link partner as a change to the aLldpXdot3RemTxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The receiving link partner responds to a transmitter's request through the aLldpXdot3LocRxTwSys (30.12.3.1.19) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The receiving link partner also copies the value of the aLldpXdot3RemTxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocTxTwSysEcho (30.12.3.1.22) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the transmitting link partner as a change to the aLldpXdot3RemTxTwSysEcho (30.12.3.1.22) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3).

The state diagrams in Figure 78–5 and Figure 78–6 describe the behavior above.

78.4.3.1 Transmitting link partner's state change procedure across a link

A transmitting link partner is said to be in sync with the receiving link partner if the presently advertised value of Transmit *Tw_sys_tx* and the corresponding echoed value are equal.

During normal operation, the transmitting link partner is in the RUNNING state. If the transmitting link partner wants to initiate a change to the presently resolved value of $T_{w\_sys\_tx}$, the local_system_change is asserted and the transmitting link partner enters the LOCAL CHANGE state where NEW_TX_VALUE is computed. If the new value is smaller than the presently advertised value of $T_{w\_sys\_tx}$ or if the transmitting link partner is in sync with the receiving link partner, then it enters TX UPDATE state. Otherwise, it returns to the RUNNING state.

If the transmitting link partner sees a change in the $T_{w\_sys\_tx}$ requested by the receiving link partner, it recognizes the request only if it is in sync with the transmitting link partner. The transmitting link partner examines the request by entering the REMOTE CHANGE state where a NEW TX VALUE is computed and it then enters the TX UPDATE state.

Upon entering the TX UPDATE state, the transmitter updates the advertised value of Transmit $T_{w\_sys\_tx}$ with NEW_TX_VALUE. If the NEW_TX_VALUE is equal to or greater than either the resolved $T_{w\_sys\_tx}$ value or the value requested by the receiving link partner then it enters the SYSTEM REALLOCATION state where it updates the value of resolved $T_{w\_sys\_tx}$ with NEW_TX_VALUE. The transmitting link partner

enters the MIRROR UPDATE state either from the SYSTEM REALLOCATION state or directly from the TX UPDATE state. The UPDATE MIRROR state then updates the echo for the Receive $T_{w\_sys\_tx}$ and returns to the RUNNING state.

78.4.3.2 Receiving link partner's state change procedure across a link

A receiving link partner is said to be in sync with the transmitting link partner if the presently requested value of Receive $T_{w\_sys\_tx}$ and the corresponding echoed value are equal.

During normal operation, the receiving link partner is in the RUNNING state. If the receiving link partner wants to request a change to the presently resolved value of $T_{w\_sys\_tx}$, the local_system_change is asserted. When local_system_change is asserted or when the receiving link partner sees a change in the $T_{w\_sys\_tx}$ advertised by the transmitting link partner, it enters the CHANGE state where NEW_RX_VALUE is computed. If NEW_RX_VALUE is less than either the presently resolved value of $T_{w\_sys\_tx}$ or the presently advertised value by the transmitting link partner, it enters the SYSTEM REALLOCATION state where it updates the resolved value of $T_{w\_sys\_tx}$ to NEW_RX_VALUE. The receiving link partner ultimately enters the RX UPDATE state, either from the SYSTEM REALLOCATION state or directly from the CHANGE state.

In the RX UPDATE state, it updates the presently requested value to NEW_RX_VALUE, then it updates the echo for the Transmit $T_{w\_sys\_tx}$ in the UPDATE MIRROR state and finally goes back to the RUNNING state.

78.5 Communication link access latency

In the full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delay through the network. This implies that MAC, MAC Control sublayer, and PHY implementors conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and the concatenation of devices.

The EEE capability adds latency that has to be considered by the network designer. When in the LPI mode, the PHY link is not available immediately for transmission of data. The system has to wake it up by sending the normal IDLE code on the MAC interface. Following the reception of an IDLE code on the MAC interface, the PHY starts the wake up process. The maximal PHY recovery time, T_{w_phy} is defined for each PHY.

Transmit and/or Receive wait time shrinkage can happen when $T_{phy\_shrink\_rx}$ or $T_{phy\_shrink\_tx}$ (as defined in 78.1.3) are not zero. This has to be taken into consideration in designing or configuring the network.

Table 78–4 summarizes critical timing parameters for supported PHYs. These are listed here to assist the system designer in assessing the impact of EEE on the operation of the link.

Case-1 of the 1000BASE-T PHY applies to PHYs in Master mode. Case-2 of the 1000BASE-T PHY applies to PHYs in Slave mode.

Case-1 of the 10GBASE-KR PHY applies to PHYs without FEC. Case-2 of the 10GBASE-KR PHY applies to PHYs with FEC.

Case-1 of the 10GBASE-T PHY applies when the PHY is requested to transmit the Wake signal before transmission of the Sleep signal to the Link Partner is complete. Case-2 of the 10GBASE-T PHY applies when the PHY is requested to transmit the Wake signal after transmission of the Sleep signal to the Link Partner is complete and if the PHY has not indicated LOCAL FAULT at any time during the previous 10 ms.

Table 78–4—Summary of the LPI timing parameters for supported PHYs

PHY Type	Case	$T_{w\_sys\_tx}$ (min), in µs	T_{w_phy} (min), in µs	$T_{phy\_shrink\_tx}$ (max), in µs	$T_{phy\_shrink\_rx}$ (max), in µs	$T_{w\_sys\_rx}$ (min), in µs
100BASE-TX		30	20.5	5.0	15	10
1000BASE-T	Case-1	16.5	16.5	5.0	2.5	1.76
	Case-2	16.5	16.5	12.24	9.74	1.76
1000BASE-KX		13.26	11.25	5.0	6.5	1.76
XGXS (XAUI)		12.38	9.25	5.0	4.5	2.88
10GBASE-T	Case-1	7.36	7.36	4.48	0	2.88
	Case-2	4.48	4.48	1.6	0	2.88
10GBASE-KX4		12.38	9.25	5.0	4.5	2.88
10GBASE-KR	Case-1	15.38	12.25	5.0	7.5	2.88
	Case-2	17.38	14.25	5.0	9.5	2.88

78.5.1 10Gb/s PHY extension using XGXS

The XGXS can be inserted between the RS and a 10 Gb/s PHY to transparently extend the physical reach of the XGMII. The LPI signaling can operate through the XGXS with no change to the PHY timing parameters described in Table 78–4 or the operation of the Data Link Layer Capabilities negotiation described in 78.4.

If the DTE XS XAUI stop enable bit (5.0.9) is asserted, the DTE XS may stop signaling on the XAUI in the transmit direction to conserve energy. If the DTE XS XAUI stop enable bit is asserted, the RS defers sending data following deassertion of LPI by an additional time equal to $T_{w\_sys\_tx}$ - $T_{w\_sys\_rx}$ for the XGXS as shown in Table 78–4 (see 46.4a.2.1).

If the PHY XS XAUI stop enable bit (4.0.9) is asserted, the PHY XS may stop signaling on the XAUI in the receive direction to conserve energy. The receiver negotiates an additional time for the remote T_{w_sys} equal to $T_{w\_sys\_tx}$ - $T_{w\_sys\_rx}$ for the XGXS as shown in Table 78–4 before setting the PHY XS XAUI stop enable bit.

78.6 Protocol implementation conformance statement (PICS) proforma for EEE Data Link Layer Capabilities[1]

78.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to 78.4, EEE Data Link Layer Capabilities, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

78.6.2 Identification

78.6.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
1—Required for all implementations 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

78.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3az-2010, 78.4, EEE Data Link Layer Capabilities
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3az-2010, Clause 78, including 78.4, EEE Data Link Layer Capabilities.)	
Date of Statement	

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

78.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
10G	Support 10G or higher operation operation	78.4	Support for 10Gb/s or higher operation	O	Yes [ ] No [ ]
DLL1	DLL	78.4	DLL	10G:M	Yes [ ] N/A [ ]
DLL2	DLL	78.4	DLL	!10G:O	Yes [ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

DLL = DLL1 OR DLL 2

78.6.4 DLL Requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLR1	DLL Timing	78.4.1	Timing Requirements	DLL:M	Yes [ ] N/A [ ]
DLR2	DLL Control State Diagrams	78.4.2	State Machines for TX and RX	DLL:M	Yes [ ] N/A [ ]

79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and values (TLV) information elements

79.3 IEEE 802.3 Organizationally Specific TLVs

Replace Table 79-1 with the following:

Table 79–1—IEEE 802.3 Organizationally Specific TLVs

IEEE 802.3 subtype	TLV name	Subclause reference
1	MAC/PHY Configuration/Status	79.3.1
2	Power Via Medium Dependent Interface (MDI)	79.3.2
3	Link Aggregation (deprecated)	79.3.3
4	Maximum Frame Size	79.3.4
5	Energy Efficient Ethernet	79.3.a
6–255	Reserved	—

Insert the following sub-section after last sub-section in 79.3.

79.3.a EEE TLV

The EEE TLV is used to exchange information about the EEE Data Link Layer capabilities. Figure 79–1a shows the format of this TLV.

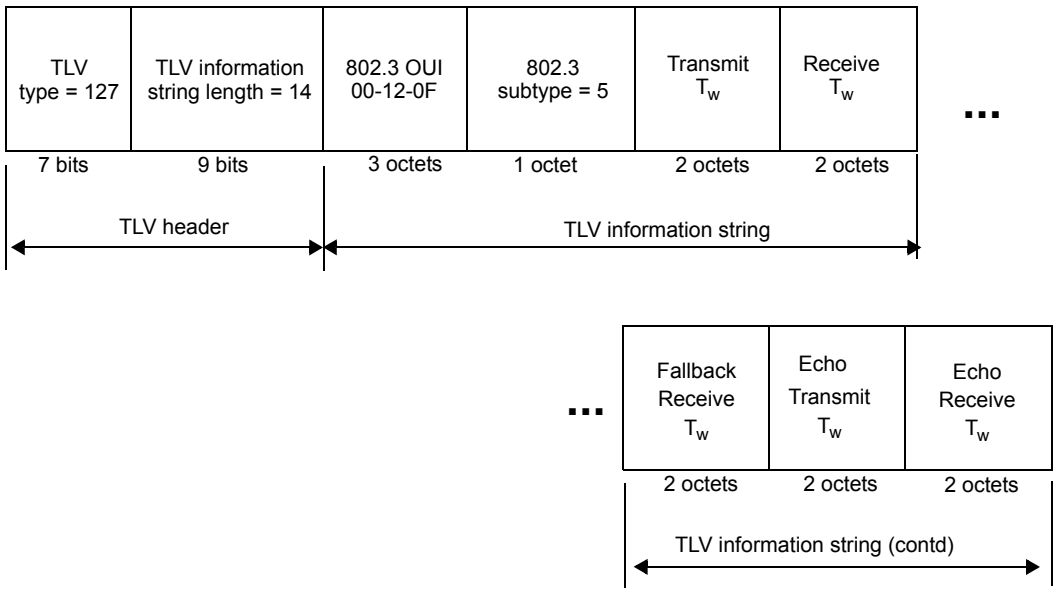


Figure 79–1a—EEE TLV format

79.3.a.1 Transmit T_w

Transmit $T_{w\_sys\_tx}$ (2 octets wide) shall be defined as the time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the Low Power Idle (LPI) mode. This is a function of the transmit system design and may be constrained, for example, by the transmit path buffering. The default value for Transmit $T_{w\_sys\_tx}$ is the T_{w_phy} defined for the PHY that is in use for the link. The Transmitting link partner expects that the Receiving link partner will be able to accept data after the time delay Transmit $T_{w\_sys\_tx}$ (expressed in microseconds).

79.3.a.2 Receive T_w

Receive $T_{w\_sys\_tx}$ (2 octets wide) shall be defined as the time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before starting the transmission data following the LPI. The default value for Receive $T_{w\_sys\_tx}$ is the T_{w_phy} defined for the PHY that is in use for the link. The Receive $T_{w\_sys\_tx}$ value can be larger but not smaller than the default. The extra wait time may be used by the receive link partner for power saving mechanisms that require a longer wake-up time than the PHY-layer definitions.

79.3.a.3 Fallback T_w

A receiving link partner may inform the transmitter of an alternate desired $T_{w\_sys\_tx}$. Since a receiving link partner is likely to have discrete levels for savings, this provides the transmitter with additional information that it may use for a more efficient allocation. As with the Receive $T_{w\_sys\_tx}$, this is 2 octets wide. Systems that do not implement this option default the value to be the same as that of the Receive $T_{w\_sys\_tx}$.

79.3.a.4 Echo Transmit and Receive T_w

The respective echo values shall be defined as the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner it can determine whether or not the remote link partner has received, registered and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

79.3.a.5 EEE TLV usage rules

An LLDPDU should contain no more than one EEE TLV.

79.7 IEEE 802.3 Organizationally Specific TLV selection management

79.7.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

Append Table 79–6 and Table 79–7 with the following:

The cross-references between the EEE TLV and the EEE local (30.12.2) and remote (30.12.3) object class attributes are listed in Table 79–6 and Table 79–7.

Table 79–6—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references

TLV name	TLV variable	LLDP Local System Group managed object class attribute
EEE	Transmit $T_{w\_sys\_tx}$	aLldpXdot3LocTxTwSys
	Receive $T_{w\_sys\_tx}$	aLldpXdot3LocRxTwSys
	Echo Transmit $T_{w\_sys\_tx}$	aLldpXdot3LocTxTwSysEcho
	Echo Receive $T_{w\_sys\_tx}$	aLldpXdot3LocRxTwSysEcho
	Fallback $T_{w\_sys\_tx}$	aLldpXdot3LocFbTwSys

Table 79–7—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
EEE	Transmit $T_{w\_sys\_tx}$	aLldpXdot3RemTxTwSys
	Receive $T_{w\_sys\_tx}$	aLldpXdot3RemRxTwSys
	Echo Transmit $T_{w\_sys\_tx}$	aLldpXdot3RemTxTwSysEcho
	Echo Receive $T_{w\_sys\_tx}$	aLldpXdot3RemRxTwSysEcho
	Fallback $T_{w\_sys\_tx}$	aLldpXdot3RemFbTwSys

79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and values (TLV) information elements[1]

79.5.3Major capabilities/options

Append Table in this section with the following:

Item	Feature	Subclause	Value/Comment	Status	Support
*EE	EEE TLV	79.5.a		O	Yes [ ] No [ ]

Insert the following sub-section after last sub-section in 79.5.

79.5.a EEE TLV

Item	Feature	Subclause	Value/Comment	Status	Support
EET1	Transmit T_w field	79.3.a.1	2 octets representing time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the LPI mode	EE:M	Yes [ ] N/A [ ]
EET2	Receive T_w field	79.3.a.2	2 octets representing time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before it starts transmitting data following the LPI	EE:M	Yes [ ] N/A [ ]
EET3	Fallback field	79.3.a.3	2 octets representing time (expressed in microseconds)	EE:O	Yes [ ] N/A [ ]
EET4	Echo Transmit and Receive T_w fields	79.3.a.4	2 octets representing time (expressed in microseconds)	EE:M	Yes [ ] N/A [ ]
EET5	Usage rules	79.3.a.5	LLDPDU contains no more than one EEE TLV	EE:O	Yes [ ] No [ ] N/A [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Annex 28C

(normative)

Next page Message Code field definitions

Change Table 28C-1 for the new message code definition:

Table 28C–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability to follow.using unformatted next page
~~10~~11.....	0	0	0	0	0	0	0	1	~~0~~ 1	0	~~1~~ 0	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

Insert 28C.12 for message code definition:

28C.12 Message code 10—EEE technology message code

Multiple clauses use next page message code 10 to indicate that EEE technology messages will follow the transmission of this page [the initial, Message (formatted) next page] with one unformatted next page. The contents of the unformatted code field bits (U10:U0) shall be as defined in 45.2.7.13.

EEE capability negotiation is defined in 78.3

Annex 28D

(normative)

Description of extensions to Clause 28 and associated annexes

Insert 28D.7 for extensions required for EEE:

28D.7 Extensions required for Energy Efficient Ethernet (Clause 78)

Energy Efficient Ethernet (Clause 78) makes use of Auto-Negotiation and requires additional MDIO registers. Autonegotiation is mandatory for all EEE PHYs that support LPI. Details are provided in 78.3.

Annex 73A

(normative)

Next page Message Code field definitions

Change Table 73A-1 by inserting a new row as shown below:

Table 73A–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability to follow.using unformatted next page

Insert 73A.4 for message code definition:

73A.4 Message code 10—EEE technology message code

Multiple clauses use next page message code 10 as an identifier for EEE technology. The EEE technology code message shall consist of only a Message next page. The message code field, 000 0000 1010 shall be contained in bits 10:0. The contents of the unformatted code bits (D47:D16) shall be as defined in 45.2.7.13.

EEE capability negotiation is defined in 78.3

Annex 74A

(informative)

Insert 74A.5, Table 74-A-5, 74A.6 and Table 74-A-6 after 74A.4 as shown below:

74A.5 Output of the FEC (2112, 2080) Encoder to Support Rapid Block during the wake state in EEE (optional)

If the optional EEE function is supported (see Clause 78) then the reverse gearbox of the remote FEC encoder will be receiving unscrambled data. PCS sublayer will be encoding /I/ during the wake state, which produces the deterministic FEC frame.

Table 74–A-5 provides the data stream at the output of the FEC (2112, 2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The example shows the stream of data in 64 bit format (33 64b symbols) generated from the output of the FEC (2112,2080) encoder after the PN-2112 scrambler.

Table 74–A-5— FEC block scrambled with PN-2112 sequence for the wake state

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	c3ffffffff555540		1e015555555552aa		a5fffff000015555		587ffeaaaaeaaaaa
	a96a7fffeffffe55		54a0000755551555		5e5aabfffff80000		552d0ffffeaaaa0a
	aa82aaabbffffff		f8cb5510000e5554		155a58aaabbfffb4		0006d55587ffefaa
	ab596abeaaad5fff		abfe151554000000		d555b55501aaaabf		ff52781515540bff
	feaa9152aaffaaa5		0ffeb5fff5f55414		00411a555555872a		baeff9db00141552
	0dffbd2aa11eabfe		aaad861fbaffa4a5		54140057f5410154		4aeaab87f8d58045
	455b54c2bfeaa7f8		abaaeafe0bfeabff		2aad455a01ffa540		0152aa0d7febf554
	41555556927fffba		fff1aaaa0a000dea		abbeaae1a55407ff		2d00105ad35bffeb
	f552a155abb5586a						

74A.6 Output of the FEC (2112, 2080) Encoder to Support Rapid Block during the refresh state in EEE (optional)

If the optional Energy Efficient Ethernet (EEE) capability is supported (see Clause 78) then the reverse gearbox of the remote FEC encoder will be receiving unscrambled data. PCS sublayer will be encoding /LI/ during the refresh state, which produces the deterministic FEC frame.

Table 74–A-6 provides the data stream at the output of the FEC (2112, 2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The example shows the stream of data in 64 bit format (33 64b symbols) generated from the output of the FEC (2112,2080) encoder after the PN-2112 scrambler.

Table 74–A-6— FEC block scrambled with PN-2112 sequence for the refresh state

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	c3cf9f3e7c535958		1e19653594d654a6		a5f3e7c060c0d653		5879f2b29a8a6b29
	a96979f3f7cf9e94		d4a18301594d2535		9e5a6a7cf9f41830		352d6f3e7daca612
	9a829acb7e7cf9f3		e0cb4d2060cfd652		195a54b29bdf3e37		0606d3599fcf8f6b
	285969b8a6b56f9f		6a7e1496520c1830		b595b59482aca6a7		cf327875d4d70df3
	e69a9162ca3e29a3		03e6b5e7c5959597		064d1a594d65e7eb		39e9f9dd0c0c2532
	cc7cbd29a712b3ce		ca6c061e39f9a8bd		6474c05734c20758		52dacb8798140343
	494364c28f8a667b		ada6f2fe13cecb3e		a9ab495a0de79520		c0d1ac0d79e7ed64
	2194d6569179f3a2		cf916b2a0b830be6		b38eca21a59584f9		2118203ad33b3e68
	f35eb9658ed5d943						