



PCI Express™ Technical Update

October 18, 2004
Taipei



Agenda

8:30	Registration	
9:00	PCIe Architecture Overview & 1.1 Updates	Bhatt
10:00	Phy Layer Design	Peng
11:00	Jitter Updates	Froelich
12:00	LUNCH	
1:00	Compliance Requirements	Hosler
2:00	PM BREAK	
2:30	Form Factor Updates <i>150W Gfx, Mini CEM, SIOM, Wireless, Cable</i>	Noble
4:00	Q&A	Bhatt, et al

■ Scalable/Extensible I/O Interconnect

- ✓ Scalable in performance and feature set
- ✓ Suitable for over 10-year horizon
- ✓ Mainstream commodity and high-end applications

■ Cost Effective

- ✓ At or below PCI cost structure at system level
- ✓ Implementable in commodity technology
- ✓ Low power, no side band signals
- ✓ 4 layer FR-4 PCBs, simple connectors, low manufacturing costs

■ Multiple Market Segments & Applications

- ✓ Mobile, desktop, server and communication devices
- ✓ Chip-to-chip, board-to-board, modules, docking, cables

■ Smooth Migration

- ✓ Preserves investments in mechanical & software ecosystem
- ✓ Provides path to future enhancements and proliferations

PCI Express Technology Primer

■ PCI Compatibility

- ✓ Configuration and PCI software driver model
- ✓ PCI power management software compatible

■ Performance

- ✓ Scalable frequency (initial 2.5GT/s)
- ✓ Scalable width (PCI Express x1, x2, x4, x8, x16, x32)
- ✓ Low latency and highest utilization (BW/pin)

■ Physical Interface

- ✓ Point-to-point, dual-simplex interconnect
- ✓ Differential low voltage signaling
- ✓ Embedded clocking
- ✓ Supports connectors, modules, cables, etc

■ Protocol

- ✓ Fully packetized split-transaction
- ✓ Credit-based flow control
- ✓ Hierarchical topology support
- ✓ Virtual channel mechanism

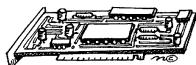
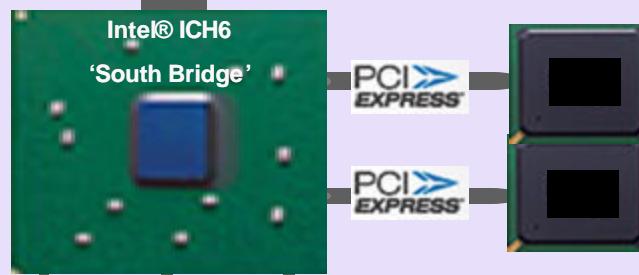
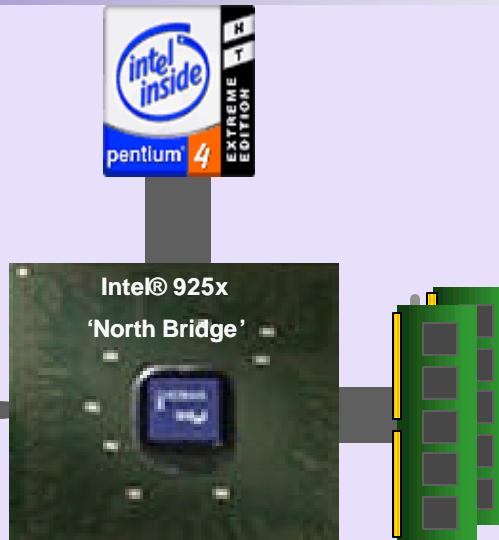
■ Advanced Capabilities

- ✓ CRC-based data integrity, hot plug, error logging

■ Enhanced Configuration Space

- ✓ Extensions and bridges into other architectures

PCI Express Technology Demo

PCI
EXPRESS™

**Cinema-Quality
Multimedia Experience
Through PCI Express x16
Graphics Implementation**

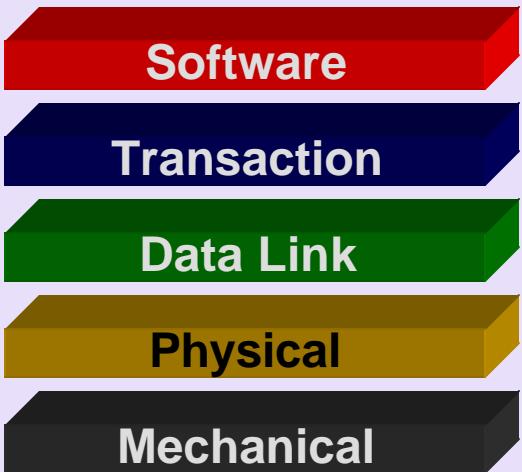
PCI Express Architecture Adoption

Application	Prior Technology	PCIe Configuration	Market Segment
Chipsets	Heterogeneous I/O	Unified I/O	Desktop, Mobile, Enterprise
Graphics	AGP 8X	PCI Express x16	Desktop, Mobile
General Purpose I/O	PCI	PCI Express x1	Desktop, Mobile
Gigabit LAN	PCI or LOM	PCI Express x1 or LOM	Desktop, Mobile
Client Plug-n-Play	PC Card	ExpressCard*	Desktop, Mobile
Internal Mobile	Mini PCI	PCI Express Mini Card	Mobile
Graphics	AGP 8X Pro	PCI Express x16	Workstations
Bridge	PCI-to-PCI-X	PCI Express-to-PCI-X	Enterprise
General Purpose I/O	PCI/PCI-X	PCI Express x4, x8	Enterprise
Server Module	n/a	PCI Express Server I/O Module	Enterprise
Communication Fabrics	Proprietary or Ethernet	Advanced Switching or Ethernet	Communications
Communication Control & Host Based Backplane	PCI	PCI Express	Communications
Communication Chip-to-Chip data	PCI/SPI/CSIX/Other	PCI Express or Advanced Switching	Communications

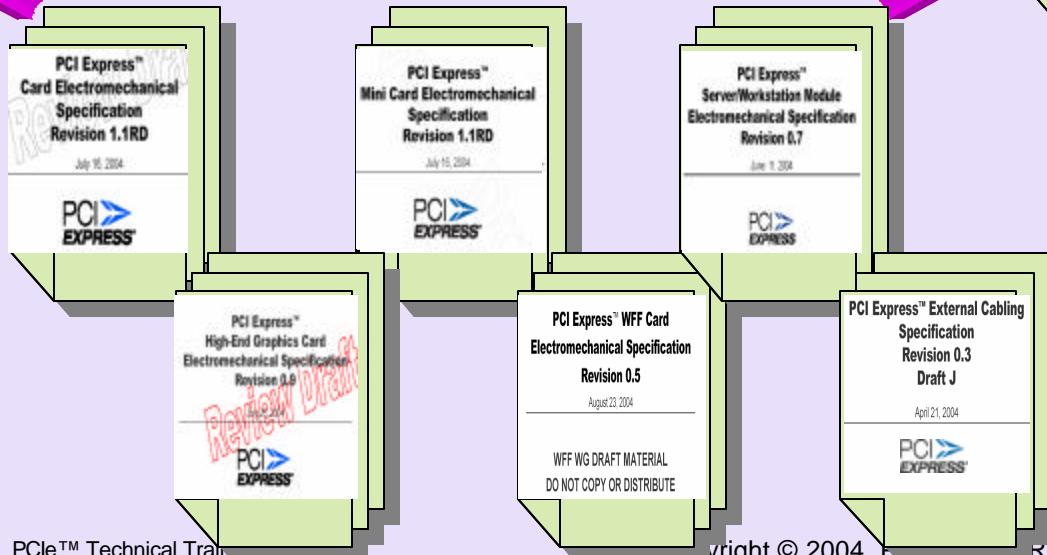
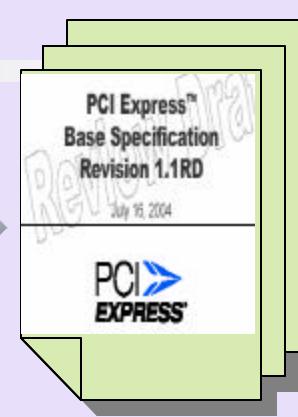
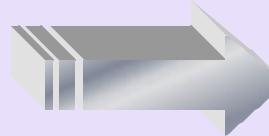
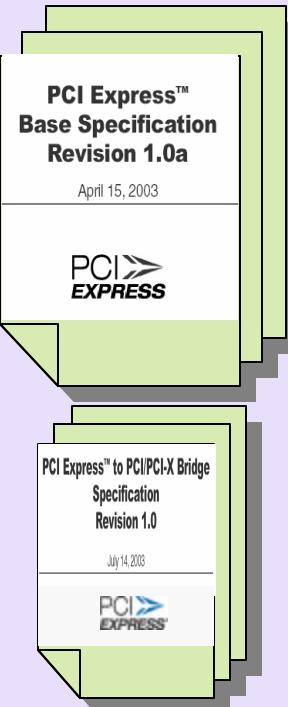
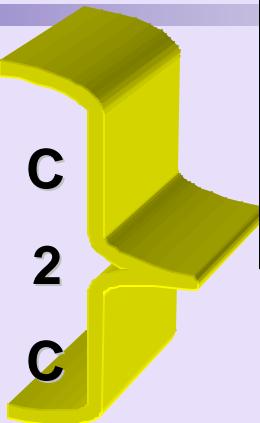
Applications Transitioning To PCIe Across The Industry



PCI Express Architecture Specifications



Cards/Slots, Modules, Cable, ...



PC Modular Expansion for Desktop and Mobile Systems



Switch Fabric Extensions to PCI Express Architecture



PICMG 3.4, AdvancedTCA for PCI Express Architecture

PCI Express 1.0a ECNs—Base

<u>Root Complex Topology Discovery</u>	Optional: enables software discovery of Root Complex Register Block to program extended capabilities	Software
<u>Integrated Devices/Event Collector</u>	Optional: allows integration of devices in a Root Complex; adds Root Complex Event Collector endpoint association capability	
<u>Reset Limit Adjustment</u>	Reduces time limit from end of Fundamental Reset to the entry to LTSSM Detect from 80ms to 20ms; clarifies PERST#. Must validate components against new limit.	
<u>Error Clarifications</u>	Clarifies and removes inconsistencies in the description of error handling	
<u>Multi-Function Virtual Channel</u>	Optional: defines new MFVC capability structure to enable QoS management such as mapping of traffic classes to VCs, etc	
<u>MMConfig/Enhanced Configuration</u>	Describes multiple enhancements to the way in which the memory-mapped configuration space is accessed in an improved and flexible manner	
<u>Training Error Removal</u>	Removes references to Training Error (chapters 4, 6-7) from the specification. Remove or disable Training Error if implemented.	
<u>Bridge Updates</u>	Incorporates VDM from the PCI Express Bridge specification and shows usage of the Bridge Configuration Retry Enable bit	
<u>MSI-X Addition</u>	Requires devices that support interrupts to implement MSI or MSI-X or both	
<u>Request Dependencies</u>	Clarifies the rules for forwarding packets by Root Complexes, Switches and End Points between different Virtual Channels	

PCI Express 1.0a ECNs—Base

Category	ECN Description
CRS Software Visibility	Describes Root Complex behavior for configuration requests that return the Configuration Request Retry Status (CRS)
Platform Reference Clock Power Management	Provides for platform clock power management reporting mechanism
VSEC	Defines Vendor-Specific Extended Capability in the RCRB in a standard and architected manner
<u>Return Loss</u>	Relaxes transmitter differential RL budget from 12dB to 10dB and receiver differential RL budget from 15dB to 10dB. Phy signal validation must comprehend these changes.
<u>PME Turn Off</u>	All components are potentially required to participate in PME_Turn_Off protocol and must comprehend these changes even if they have no special power management functionality.
Surprise Down Error	Introduces optional error logging mechanism to report unexpected link failure (transition from Active to Inactive)
<u>Flow Control Initialization</u>	Updates the FC Init protocol with clarifications to the permitted intervals. All components must verify compliance with these changes.
<u>Hot Plug</u>	Includes significant revisions to all hot plug specifications. System software impacted. Improves ability to validate hardware for correct hot plug functionality. Hardware simplifications may be enabled for some components.
Posted Request Acceptance	Imposes a limit on posted requests (memory writes) to relieve PCIe fabric congestion
<u>Jitter</u>	Incorporates many changes including Tx & Rx eye measurements done with 'clean' clock. Phy signal validation must comprehend the changes.



PCI Express 1.0a ECNs

CEM & Mini CEM



75W Graphics Power Limit	Increases PCI Express x16 graphics adapter power dissipation to 75W (from 60W)
Card Retention / Keep-out	Adds keep-outs on adapter cards for retention mechanism to enhance system structural integrity
PERST# Definition	Adds threshold for 12V, 3.3V, 3.3Vaux power rails to assert PERST# when a power rail falls below its tolerance
Color Connector	Recommends PCIe connectors on system boards be black to distinguish them from other (AGP) connectors
PRSNT#2 Clarification	Removes inconsistencies in the definition of the PRSNT#2 pins (eliminates the short middle PRSNT#2 pad)
S-Parameter Clarification	Corrects inconsistencies in the connector S-parameter and current rating tests; connector pin out revised to include new 12V pin for 75W
Connector Primary Datum Clarification	Clarifies the connector primary datum (datum Z) on the system board
Jitter	Bounds the peak-peak magnitude reference clock jitter in the phase jitter domain
CLKREQ# Dynamic Protocol	Enhances power management when PCIe links are idle; required for adapters and optional for host platforms
+3Vaux Typo Correction	Corrects typo in section 3.2.1 by adding +3.3Vaux to the list of power sources (others are +3.3V and +1.5V)
Wireless Disable	Redefines unused W_DISABLE# pin so that the system can disable radio operations to meet RF regulations
SIM/UIM Pin Definition	Adds signals to define an interface between User Identity Module (UIM) and a Wireless Wide Area Network (WWAN)
Chamfer	Improves manufacturability by increasing tolerance for the chamfered edge of the PCB

PCI Express 1.1 Summary

- PCI Express 1.1 specifications consolidate design learnings of past 2 years
- PCI Express 1.1 specifications in PCI-SIG member review now, release planned for 4Q04
 - ✓ PCI Express Base 1.1
 - ✓ PCI Express Card Electromechanical 1.1
 - ✓ PCI Express Mini Card Electromechanical 1.1
- PCI Express 1.1 revised C&I collateral expected in 1H05
- PCI Express 1.1 compliance testing planned for late 2H05
- PCI Express 1.0a Integrators List published at www.pcisig.com

2004

2005

2006

2007

PCI Express 1.0a Compliance

PCI Express 1.1 Compliance

Agenda

8:30	Registration	
9:00	PCIe Architecture Overview & 1.1 Updates	Bhatt
10:00	Phy Layer Design	Peng
11:00	Jitter Updates	Froelich
12:00	LUNCH	
1:00	Compliance Requirements	Hosler
2:00	PM BREAK	
2:30	Form Factor Updates <i>150W Gfx, Mini CEM, SIOM, Wireless, Cable</i>	Noble
4:00	Q&A	Bhatt, et al

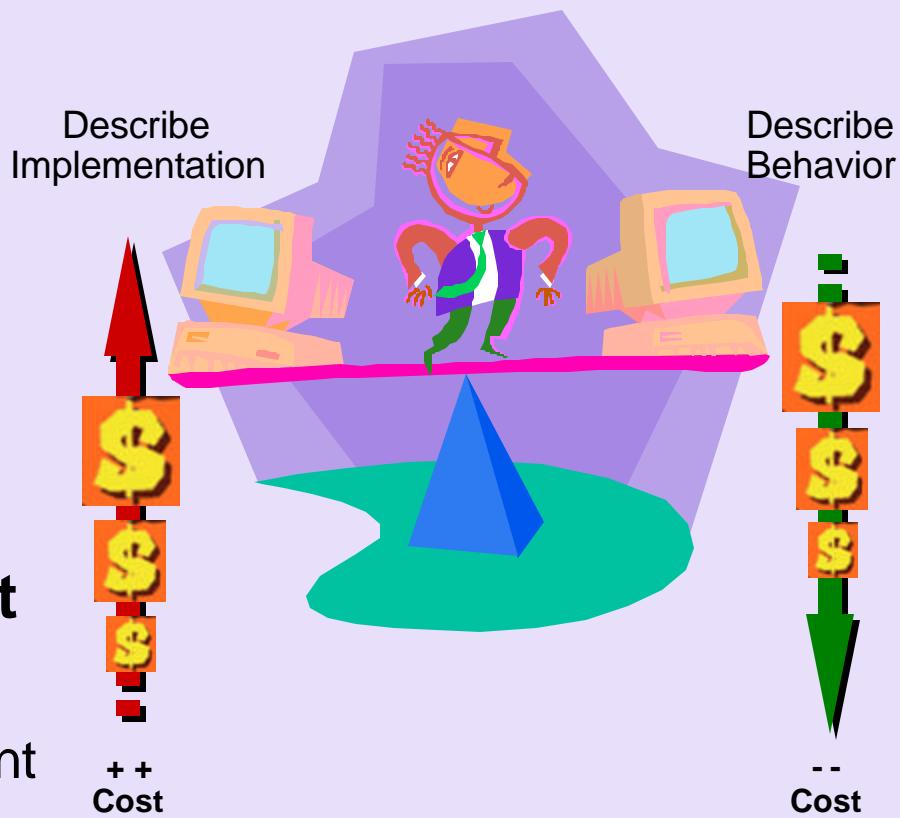
PCI Express Specification Balance

- **Unambiguously describe how PCI Express interfaces behave**

- ✓ Interoperable products
 - ✓ Vibrant competitive market
 - Encourage multiple implementations

- **State what must be done without stating how to do it**

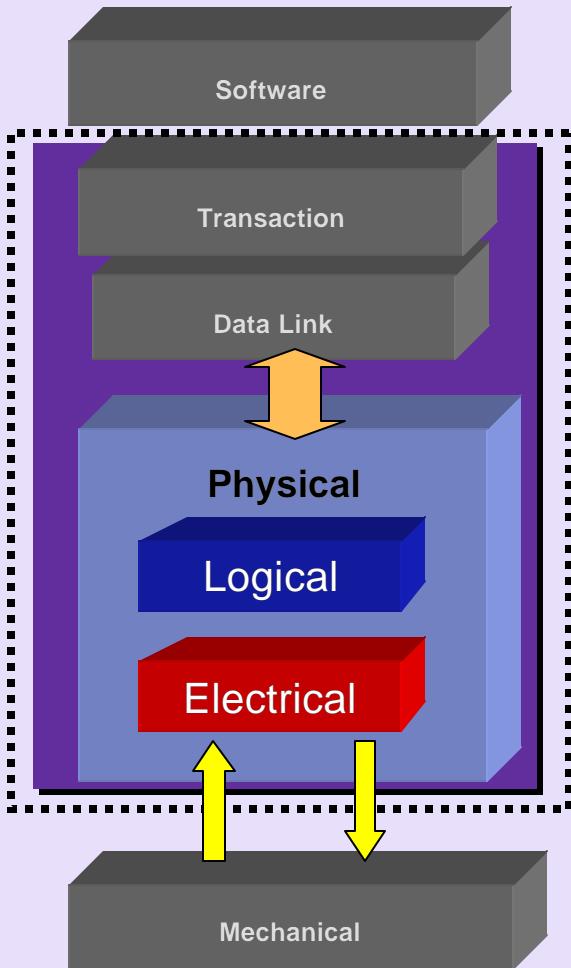
- ✓ Specify the interface behavior
 - ✗ Do not specify how to implement
 - ✗ Do not specify the system it operates in



PCI Express Physical Layer

- **PCI – PHY is digital in nature**
 - ✓ Parallel multi-drop bus
 - ✓ Bits, a clock, setup and hold times...
 - Jitter essentially ignored
- **PCI Express – PHY is analog in nature**
 - ✓ Based on serial technology
 - ✓ Techniques developed by the communication industry
- **A transition for microprocessor based systems**
 - ✓ Microwave theory/physics challenges dominate
 - ✓ Two PLLs communicating directly

PHY Layer Design Basics



■ Logical Functions

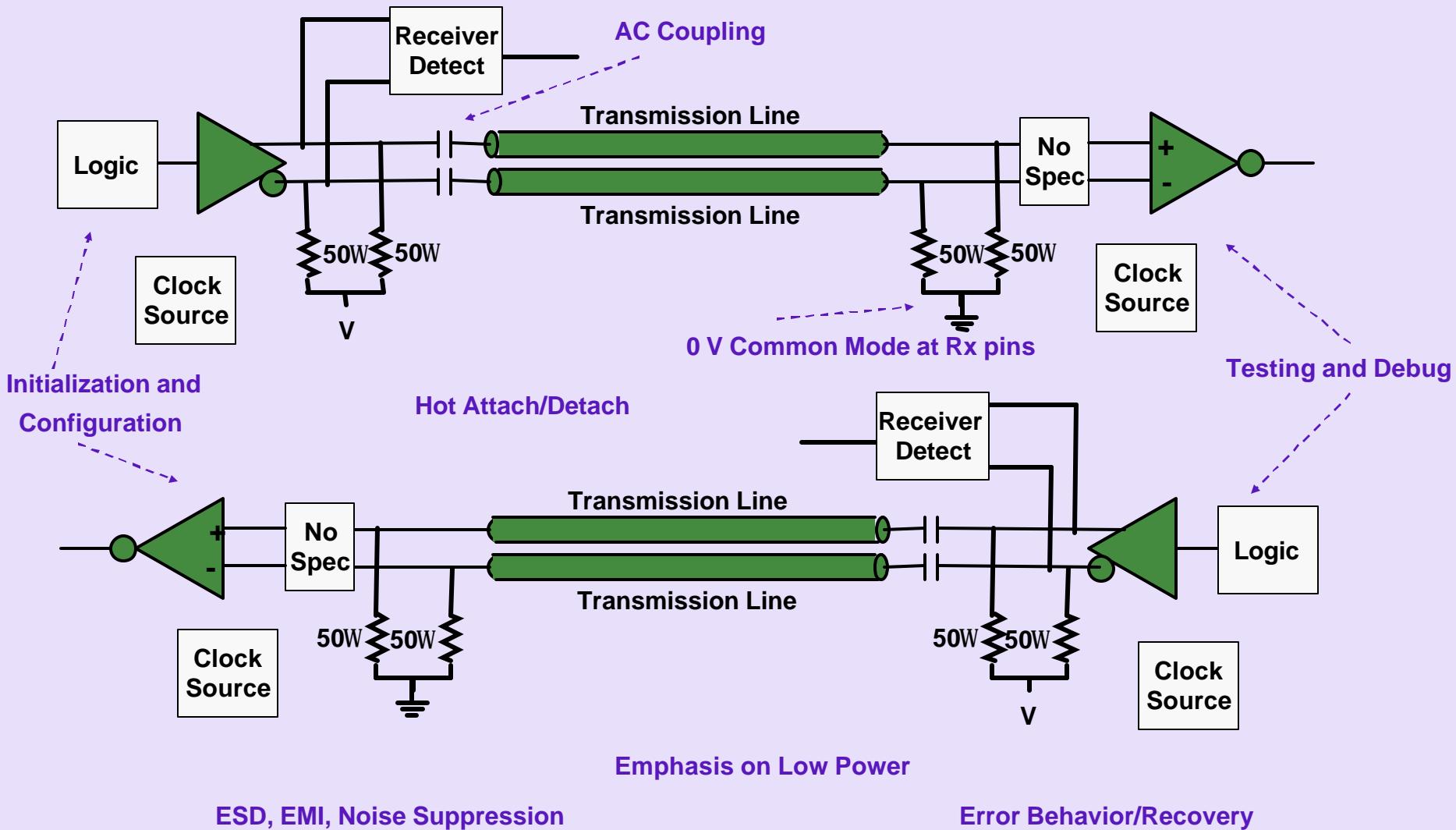
- ✓ Encoding/decoding/scrambling
- ✓ Reset, initialization, de-skew
- ✓ Built in test modes
- ✓ Configuration:
 - Speed, link width, lane mapping, Polarity
- ✓ Link power management

■ Electrical Functions

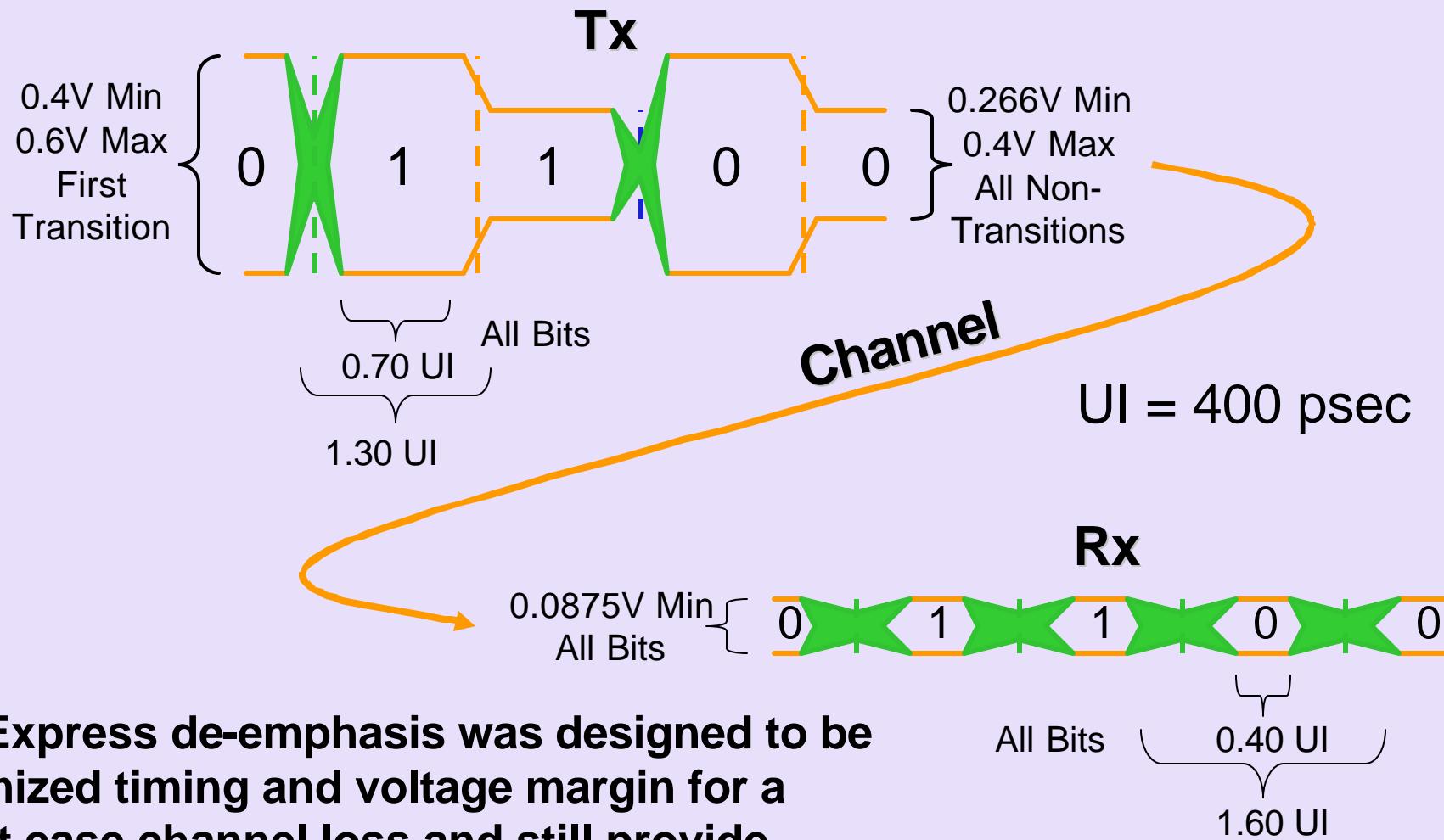
- ✓ Transmitter/receiver
- ✓ Clocks/PLLs
- ✓ Clock/data recovery

PHY Layer Upgrades Don't Impact Upper Layers

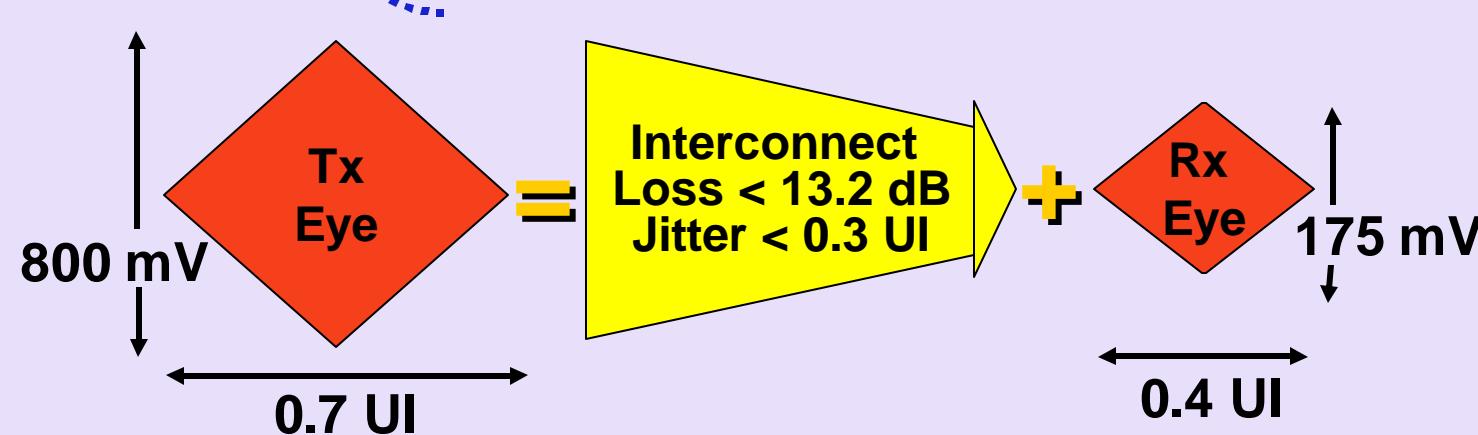
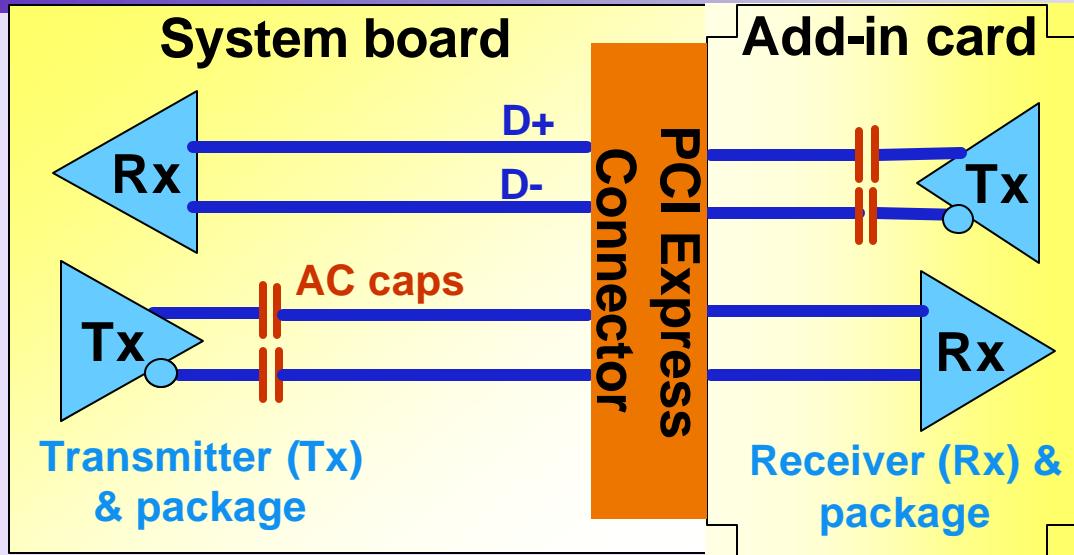
Pictorial Summary



Electrical Specifications



System Budget



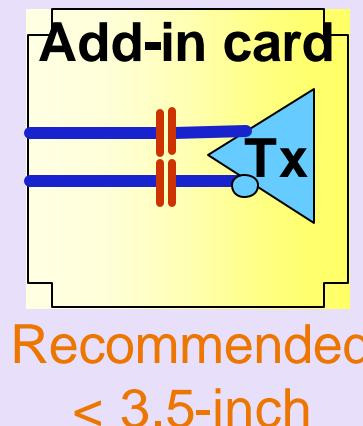
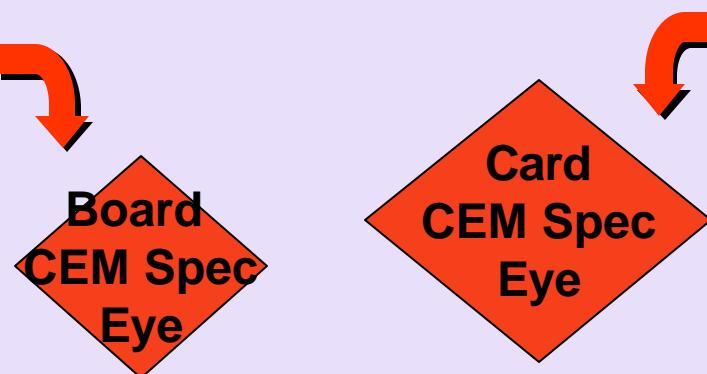
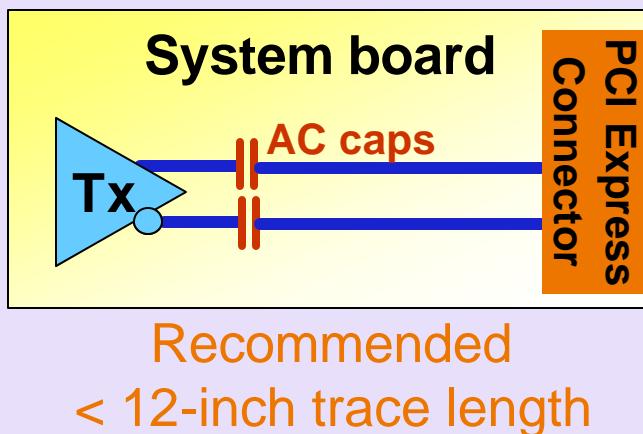
- ✓ Differential pairs
- ✓ AC coupled
- ✓ Lane-to-lane de-skew
- ✓ Polarity inversion
- ✓ On-chip equalization
- ✓ On-chip terminations

UI = Unit Interval as defined in the PCI Express Base 1.0a Specification

Card Electromechanical Interconnect Budget

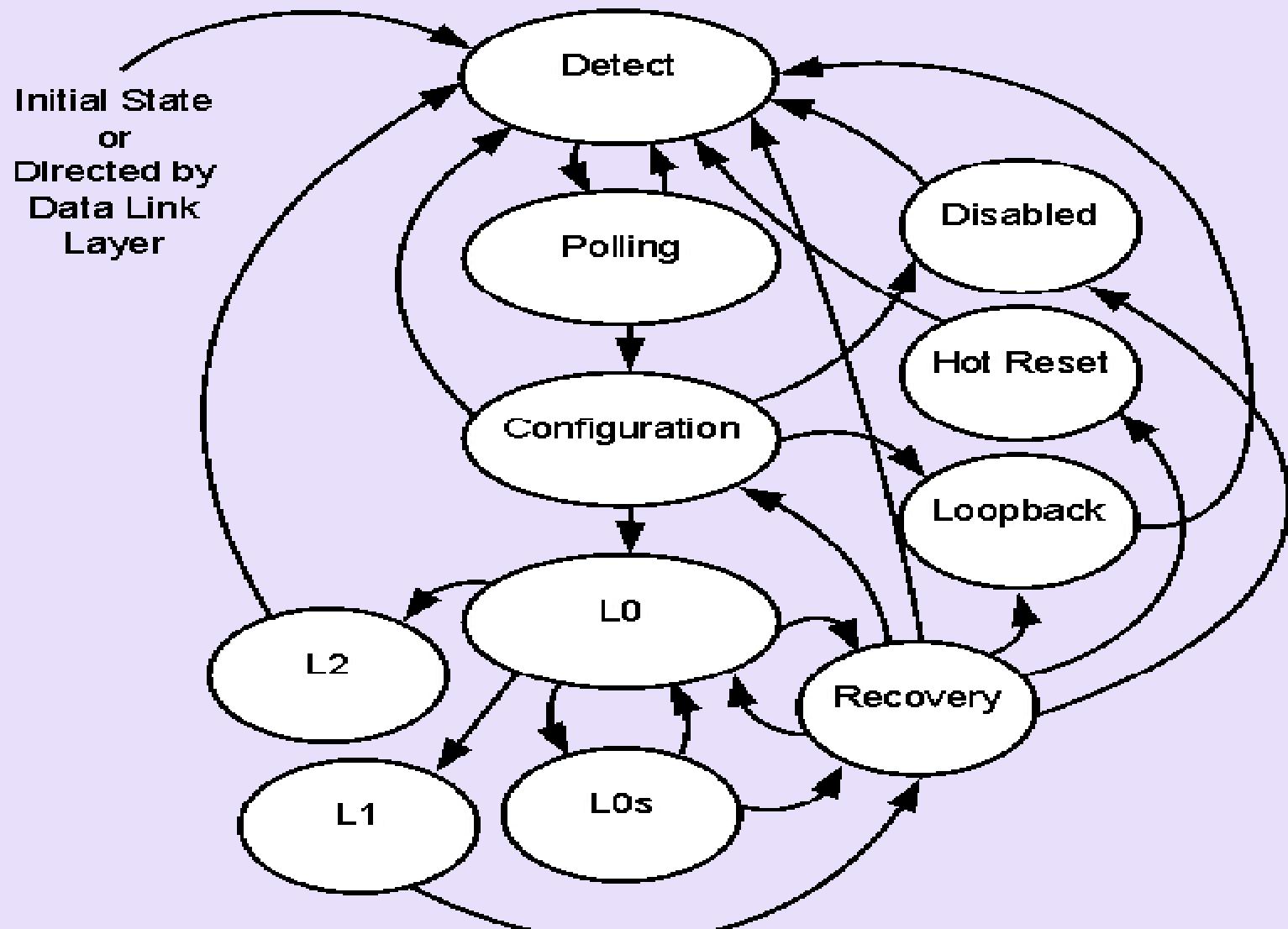
- Card Electromechanical (CEM) 1.0a specification defines budget allocation

- ✓ Loss and *jitter* are key parameters
- ✓ Target impedance not as critical
- ✓ Maintain differential pair symmetry
- ✓ Design tradeoffs: loss vs. trace length, etc.



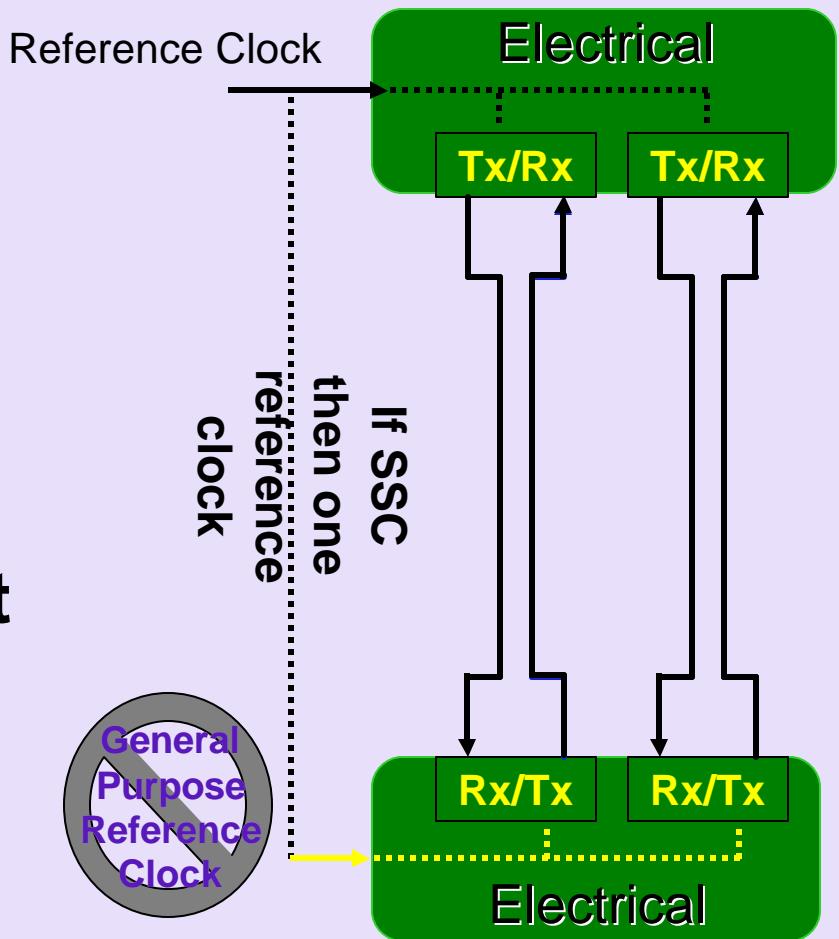
Manage Loss & Jitter To Meet Budget

Link Training & Status State Machine



Clocking Options

- All lanes within a port must transmit data using one frequency
- The ports at each end of a link may transmit data at slightly different frequencies
 - ✓ Tolerance = ± 300 ppm each



If SSC Used To Modulate Data Rate,
Then Both Ports Must Use Same Modulated Clock Source

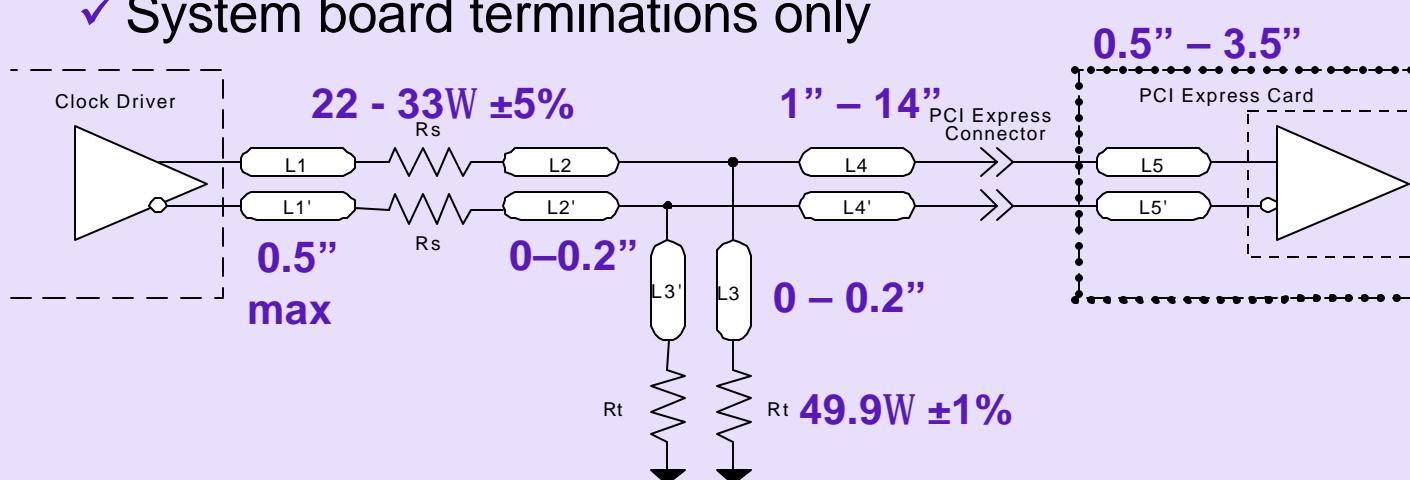
Reference Clock Routing

- Differential clock routing to each device and connector

- ✓ Use the same differential trace geometries
- ✓ Length matching to different devices *NOT* required!

- Clock driver requirements

- ✓ 100MHz with SSC support (e.g. CK410)
- ✓ Choose low jitter components
- ✓ System board terminations only



Physical Layer Challenges

■ Increase industry knowledge base

- ✓ What tradeoffs should we make?
 - Tx, Rx implementations
 - PLLs: construction and number
 - Clock distribution (both on-chip and off-chip)
 - Channel construction
 - Clock and data recovery algorithms
 - Test, debug, validation
 - Voltage and jitter budget allocation

Let Us Know What You Think!

Agenda

8:30	Registration	
9:00	PCIe Architecture Overview & 1.1 Updates	Bhatt
10:00	Phy Layer Design	Peng
11:00	Jitter Updates	Froelich
12:00	LUNCH	
1:00	Compliance Requirements	Hosler
2:00	PM BREAK	
2:30	Form Factor Updates <i>150W Gfx, Mini CEM, SIOM, Wireless, Cable</i>	Noble
4:00	Q&A	Bhatt, et al

PCI Express BER/Jitter Overview

- Base Specification Changes
 - ✓ New clock recovery function for measuring eye diagrams
 - ✓ PLL bandwidth restrictions
 - ✓ Tx eye budget reduction
- CEM Specification Changes
 - ✓ Rj / Dj tables and new budgets
 - ✓ Implied Rx tolerance mask
 - ✓ Reference clock specification and sample sizes
 - ✓ Base board measurement with “dirty” reference clock

These Changes Are In PCI Express 1.1 Specification

New Clock Recovery For Eye Measurement

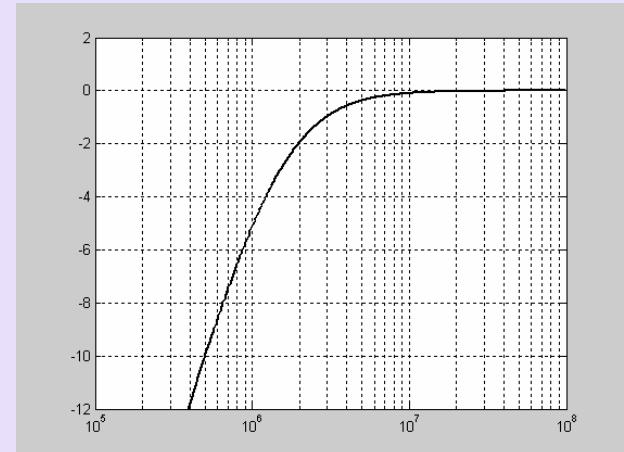
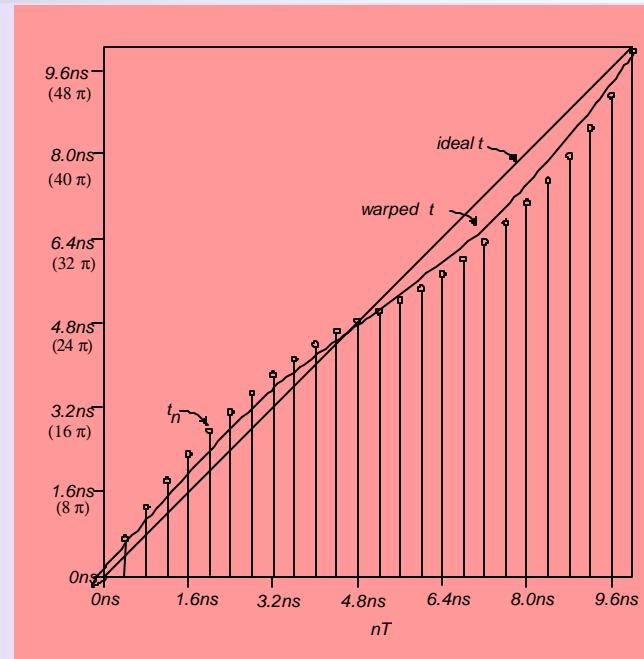
- The estimate of the ideal clock, T, in the phase jitter is the clock recovery

$$\Phi_n = t_n - nT, \quad n = 1, 2, \dots, \infty$$

- Recovery can be done in T or in Φ
 - ✓ Matlab code in jitter whitepaper that applies it in $\Phi(s)$
 - ✓ It can also be done as a sliding window using average T and looking across 416 UI

$$H_3(s) = \frac{s}{s + 2 * p * 1.5e6}$$

- This implies the minimum required performance of the data recovery circuit (DRC)



Jitter Method Frequency Response

- Produce Crossovers With Jitter At A Single Frequency
 - ✓ $C_n = n * \text{UnitInterval} + \text{JitAmp} * \sin(2\pi * n * \text{UnitInterval} * \text{JitFreq})$
- Peak to Peak Jitter = $2 * \text{JitAmp}$
- Analyze Data And Obtain JitterResult
- Compute $\log_{10}(\text{JitterResult}/(2 * \text{JitAmp}))$
- Repeat For Frequencies Throughout Range Of Interest

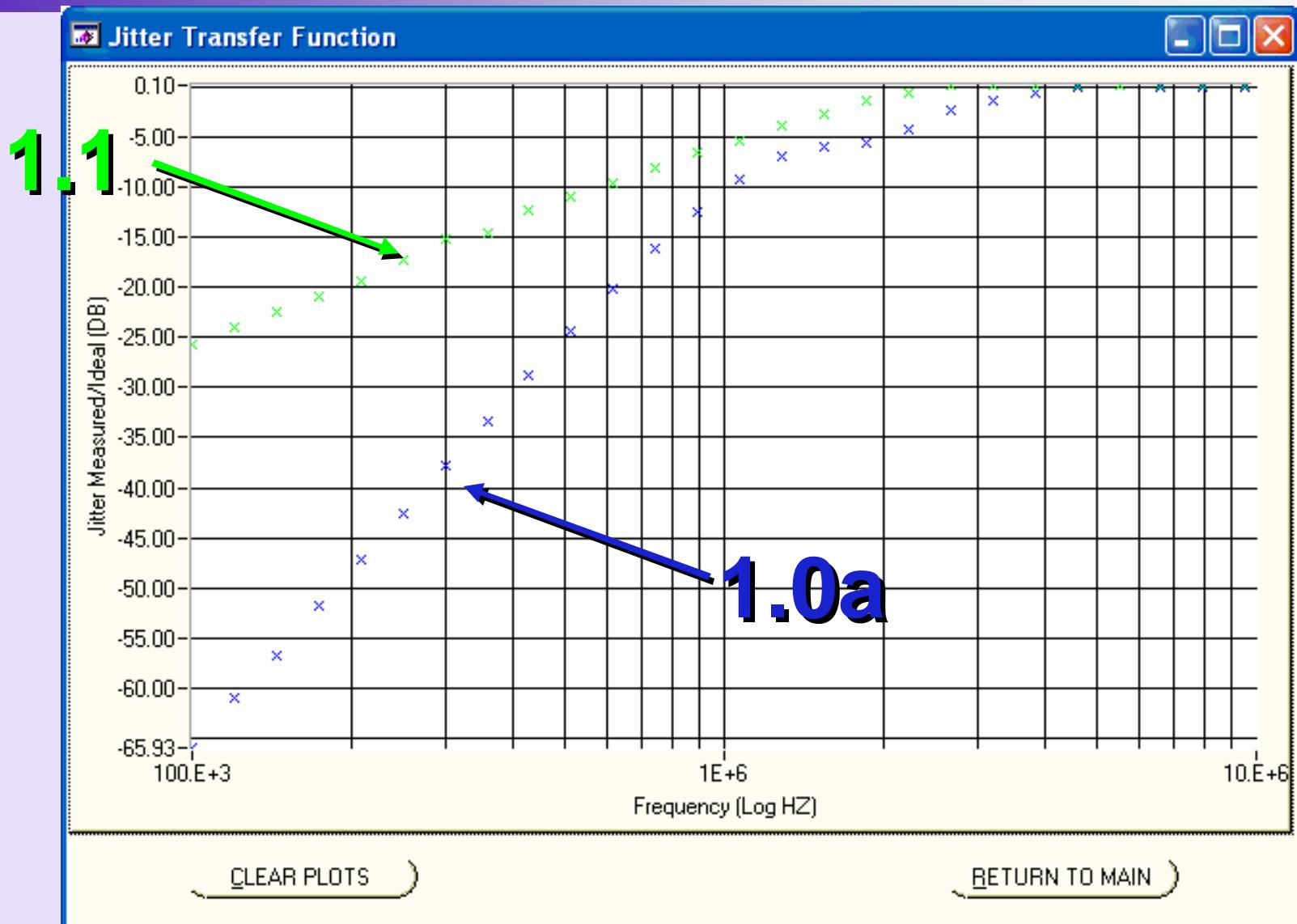
Assumes That Frequency Response Is Not Amplitude Dependent

Demo

1.0a Transmitter Jitter Method Frequency Response

1.1 Transmitter Jitter Method Frequency Response

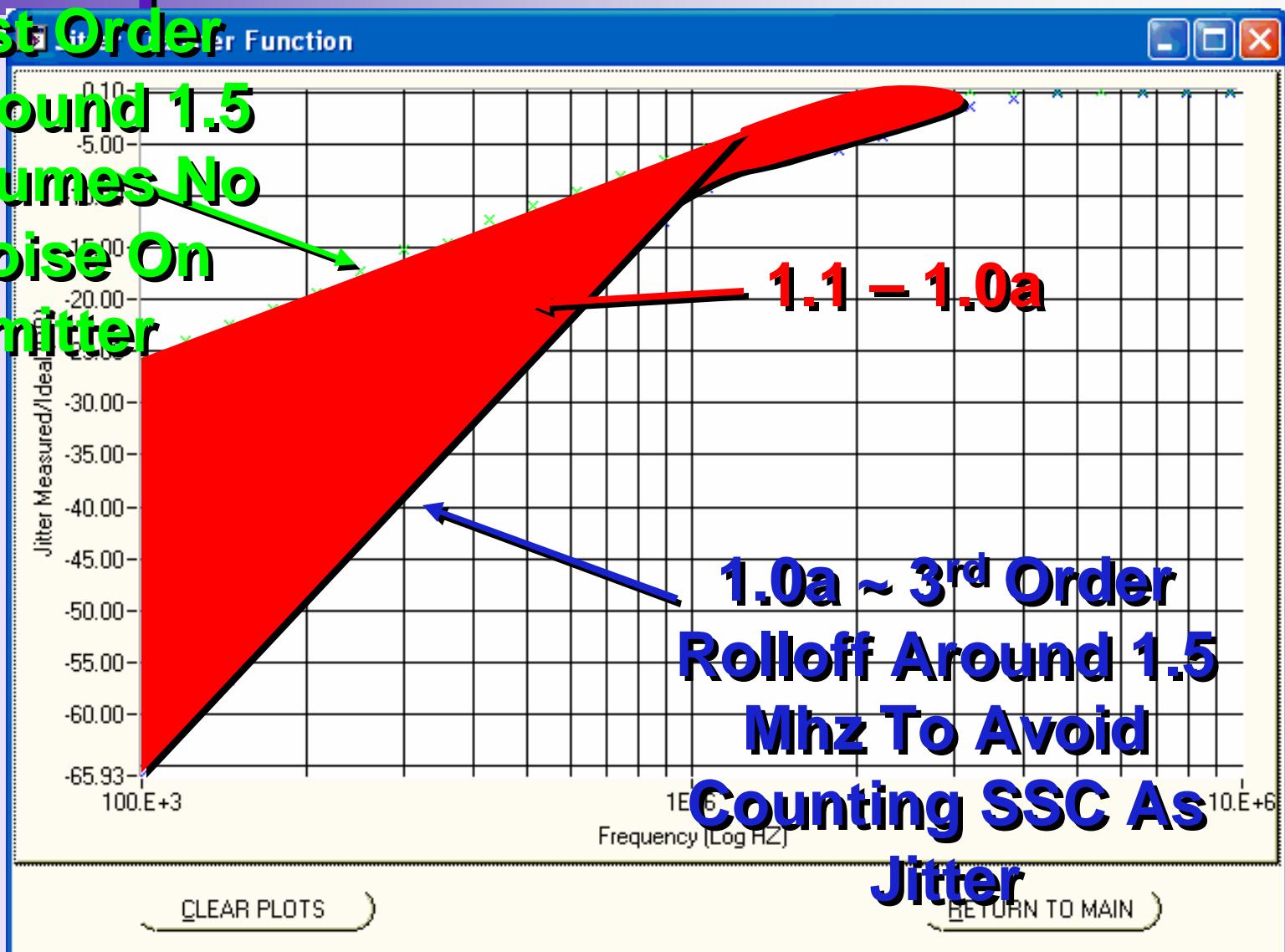
Frequency Response 1.0a/1.1



Response Delta - 1.0a/1.1

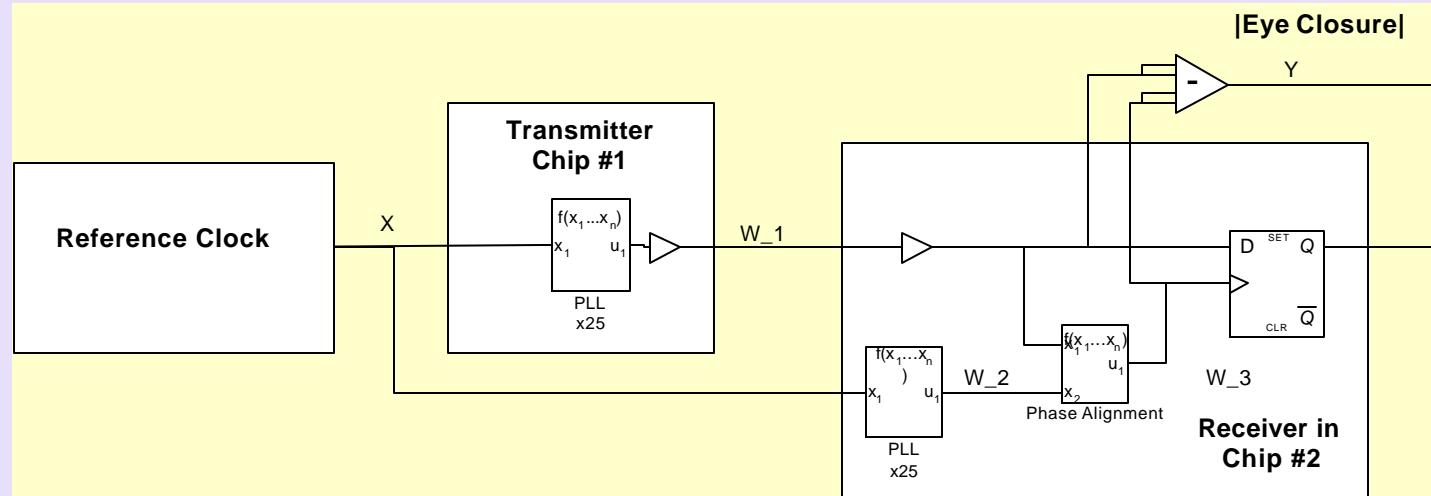
1.1 ~ First Order

Rolloff Around 1.5
Mhz. Assumes No
Clock Noise On
Transmitter



Tx PLL Bandwidth Restrictions

- Tx PLL bandwidth is between 1.5 and 22 MHz, peaking < 3dB
 - ✓ Based on second order transfer function
- Rx is implementation specific



Tx Eye Reduction

- Tx reduction from 120 ps to 100 ps
 - ✓ At 10⁻¹² BER
- Eye measurements are to be done with a “clean” clock
- The median to max measurement is over 1e6 samples using the compliance pattern

CEM System Budget

- Minimum Rj assumptions have been taken for the Tx, reference clock and the “Internals” of the Rx
- These Rj terms are convolved to achieve the total system budget
- This is then extrapolated to 10^-6 for the CEM and compliance numbers

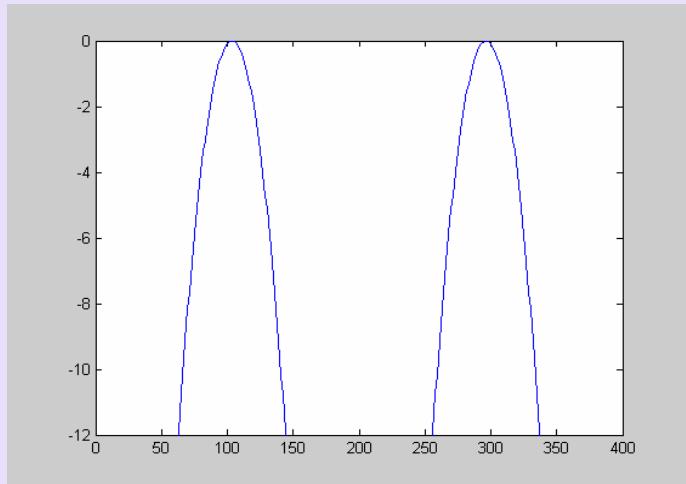
Jitter Contribution	Min Rj (ps) one sigma	Max Dj (ps) P-P	Tj at BER 10^-12 (ps)	Tj at BER 10^-6 (ps)
Tx	2.8	60.6	100	87
Ref Clock	4.7	41.9	108	86
Media	0	90	90	90
Rx	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

New CEM Jitter Budgets At Connectors (TJ at 10^-12)

	System Connector Jitter Limit (PP)	Add In Card Edge Fingers Jitter Limit (PP)
1.0a	217	163
1.1	167	126

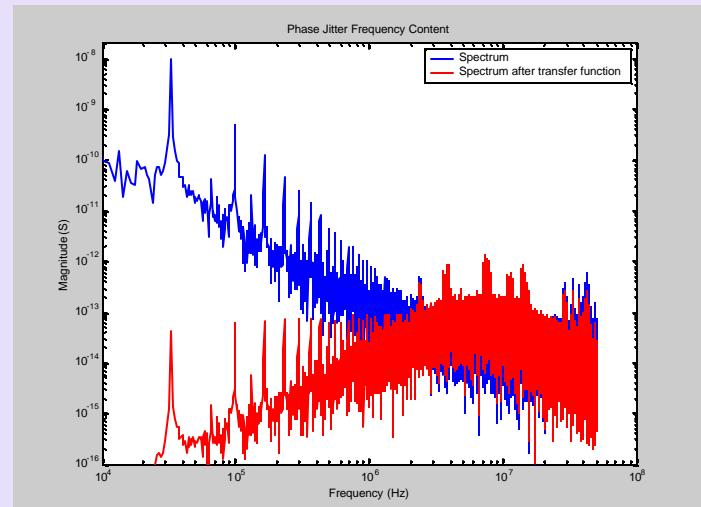
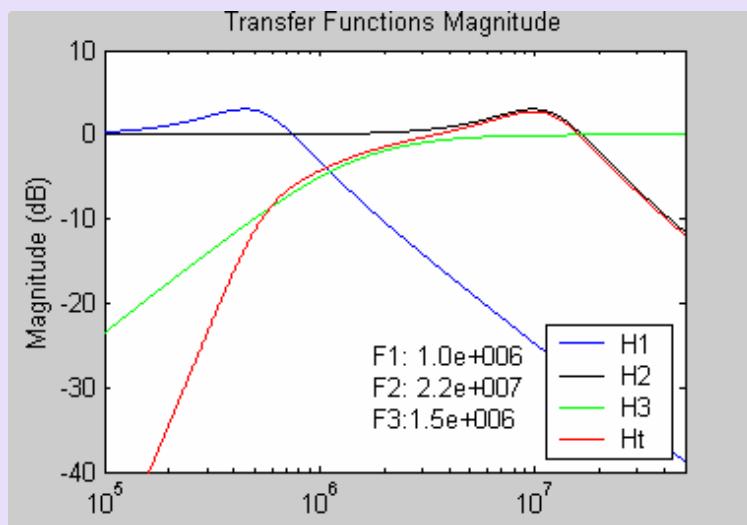
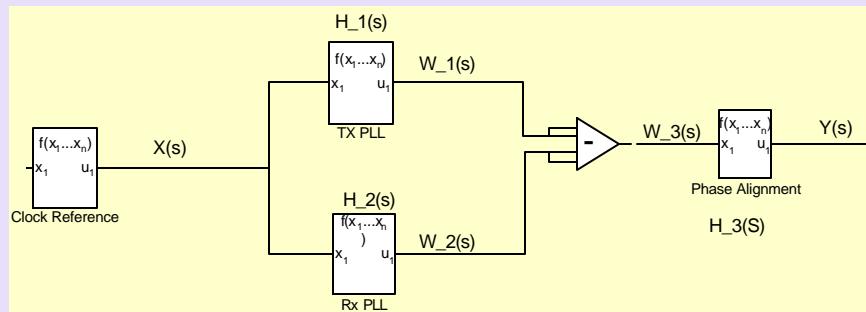
Implied Receiver Tolerance Mask

- Apply 193 ps of D_j
- Apply 5.4 ps of R_j
- BER of 10^{-12} should be met at the sample size tested
- More detail to follow in white paper



Reference Clock Specification

- The reference clock phase jitter is less than 86 ps
 - After the $(H_1 - H_2) * H_3$ transfer function has been applied
 - $H_1 = 1.5$, $H_2 = 22$, second order
 - 3 dB peaking
 - $H_3 = 1.5$ MHz, first order
 - Delay of 10 ns added to H_1 for transport delay



Reference Clock Jitter Algorithm

- Produce Interval Array
- Perform FFT Of Intervals
 - ✓ FFT Removes DC Offset
 - ✓ Effectively Removes Average Interval
- Apply Jitter Transfer Function In Frequency Domain
- Perform Inverse FFT
 - ✓ Data Is Now Interval Deltas From Average Interval After Frequency Transformation (Data)
- Integrate Data
 - ✓ $\text{IntData}_n = \text{IntData}_{n-1} + \text{Data}_n$
- Peak Peak Jitter
 - ✓ $\text{Max}(\text{IntData}) - \text{Min}(\text{IntData})$

Method Can Also Be Used For Transmitter Data With Small Changes

Demo Reference Clock Jitter Calculation

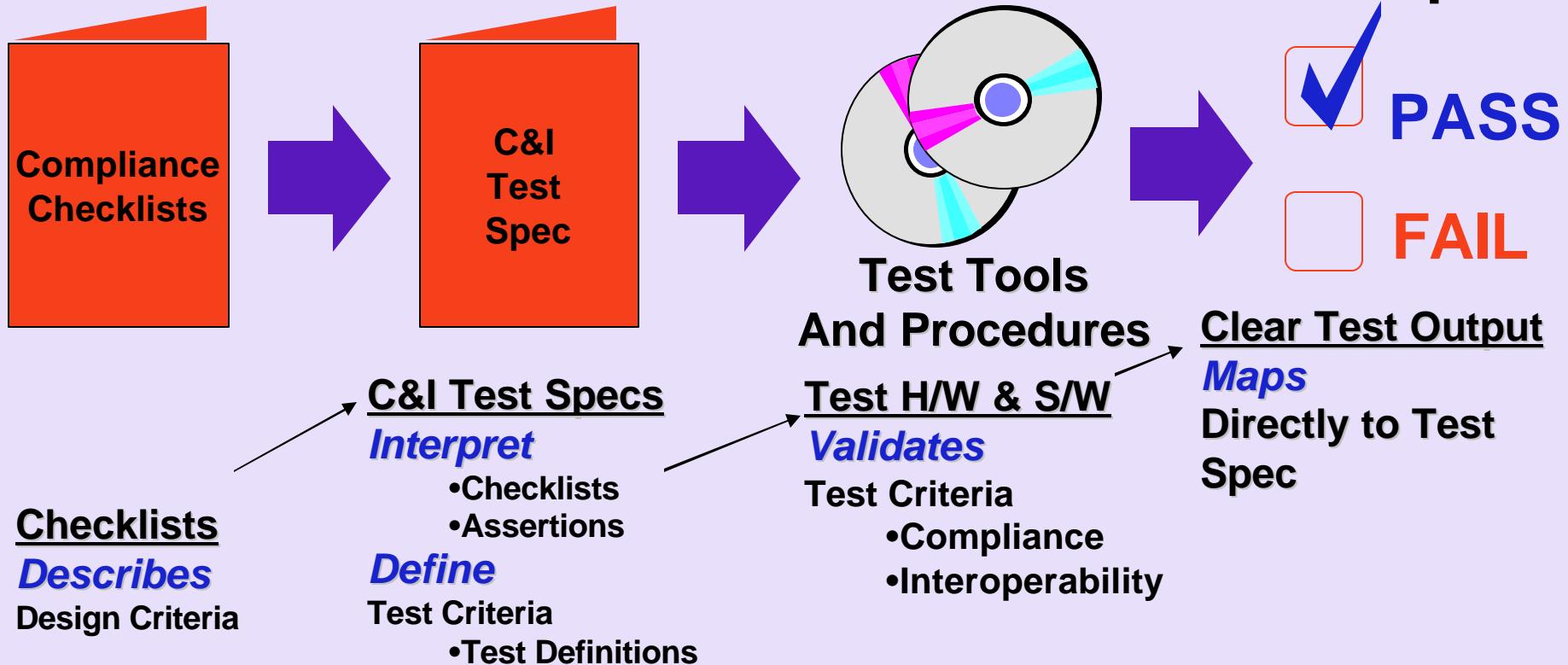
Physical Layer Summary

- The Tx specification is to be made with a clean clock
- The Tx bandwidth range and peaking is limited
- The reference clock phase jitter is limited
- The total system budget includes the convolution of R_j

Agenda

8:30	Registration	
9:00	PCIe Architecture Overview & 1.1 Updates	Bhatt
10:00	Phy Layer Design	Peng
11:00	Jitter Updates	Froelich
12:00	LUNCH	
1:00	Compliance Requirements	Hosler
2:00	PM BREAK	
2:30	Form Factor Updates <i>150W Gfx, Mini CEM, SIOM, Wireless, Cable</i>	Noble
4:00	Q&A	Bhatt, et al

PCI Express Compliance



Predictable Path To Design Compliance

PCI Express Checklists

- **Provide design-time ‘rules’ that implementations should follow**
 - ✓ Checklists for Root Complex, Endpoint, Switch, Add-in Card, and Motherboard
- **Simple set of ‘yes/no’ questions**
- **Checklists available on PCI-SIG website**
 - ✓ http://www.pcisig.com/specifications/pciexpress/technical_library

PHY.2.6#1	Training sequence ordered-sets are never scrambled but always 8b/10b encoded.	yes ____ no ____
PHY.3.1#25	The receiver terminations must remain enabled in Electrical Idle .	yes ____ no ____
PHY.3.2#5	The Beacon signal must contain minimum width pulses >= 2 ns.	yes ____ no ____

PCI Express Test Specs

- **Clear description of what is being tested**
- **Contains:**
 - ✓ Assertions
 - Prioritized set pulled from checklists
 - ✓ Test Descriptions
 - What a test does, and what assertions it checks

PCI Express Test Procedures

- **Describes how to run tests**
 - ✓ Required equipment
 - ✓ Equipment setup
 - ✓ Step-by-step instructions
- **Detailed procedures help ensure repeatability**
 - ✓ At Compliance Workshops
 - ✓ In development labs

Compliance Tools Goals

- **Wide deployment in development labs**
 - ✓ Tools and procedures should be useful and valuable in a development lab setting
- **Easy to use**
 - ✓ Clear documentation, clear procedures
- **Reasonable equipment cost**
 - ✓ ~\$50K
 - ✓ Ideally, equipment is useful for many other things besides PCI Express compliance testing

Compliance Test Areas

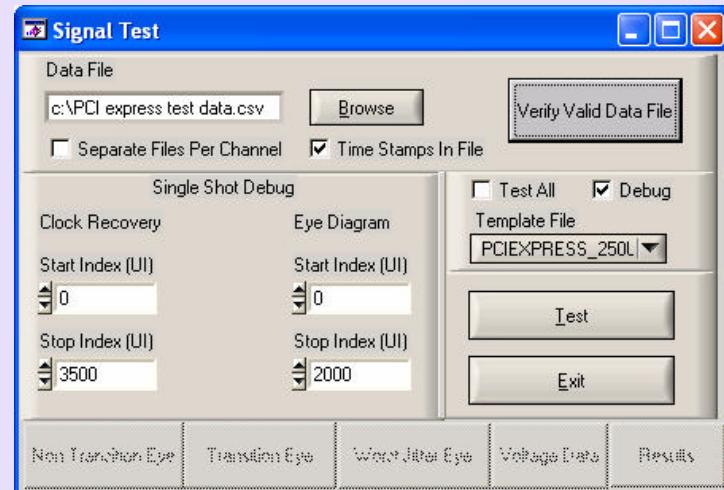
- **Physical layer**
 - ✓ Examine electrical signaling
- **Configuration Space**
 - ✓ Verify required fields and values
- **Link & Transaction layer (2 areas)**
 - ✓ Exercise protocol boundary conditions
 - ✓ Inject errors and check error handling
- **Platform Configuration**
 - ✓ Check BIOS handling of PCI Express devices

Available
on SIG website

Electrical Tests & Tools

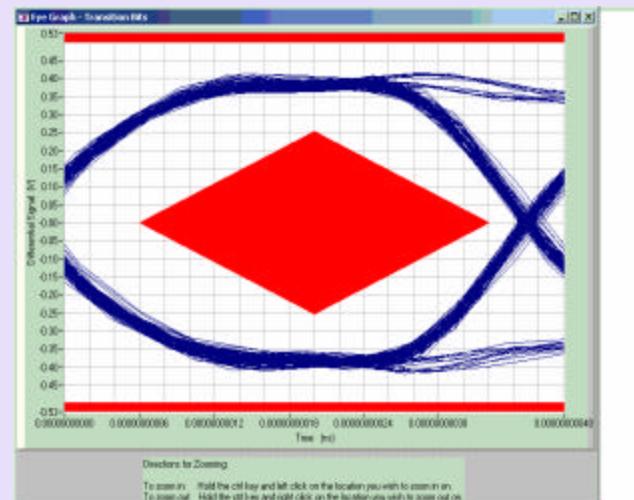
■ Signal Quality Analysis H/W and S/W

- ✓ Eye pattern, jitter and bit rate analysis
- ✓ Upstream and downstream signaling
- ✓ Electrical compliance base board
- ✓ Electrical compliance load board
- ✓ Stand-alone Windows-based eye diagram analysis S/W
- ✓ Electrical test procedures and Oscilloscope setup files



■ Jitter Analysis DLL

- ✓ Clock Recovery
- ✓ Interpolation
- ✓ Transition/non-transition eye points
- ✓ Goal - Promote consistent solutions

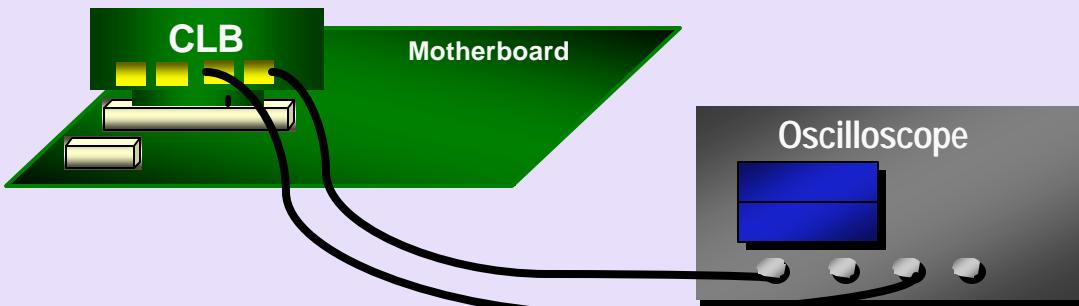


Motherboard Electrical Tools

- **Compliance Load Board**

- ✓ Root Complex electrical signal quality
- ✓ Systems & Motherboards
- ✓ Terminates Transmitters to utilize spec required compliance mode
- ✓ PCI Express x1, x4, x8, x16 test configurations
- ✓ Improved active probing geometries
- ✓ SMAs added to PCI Express x8 & x16, first-middle-last
- ✓ Analog loop back (Tx to Rx stuff option)
- ✓ Reference clock and Power probing

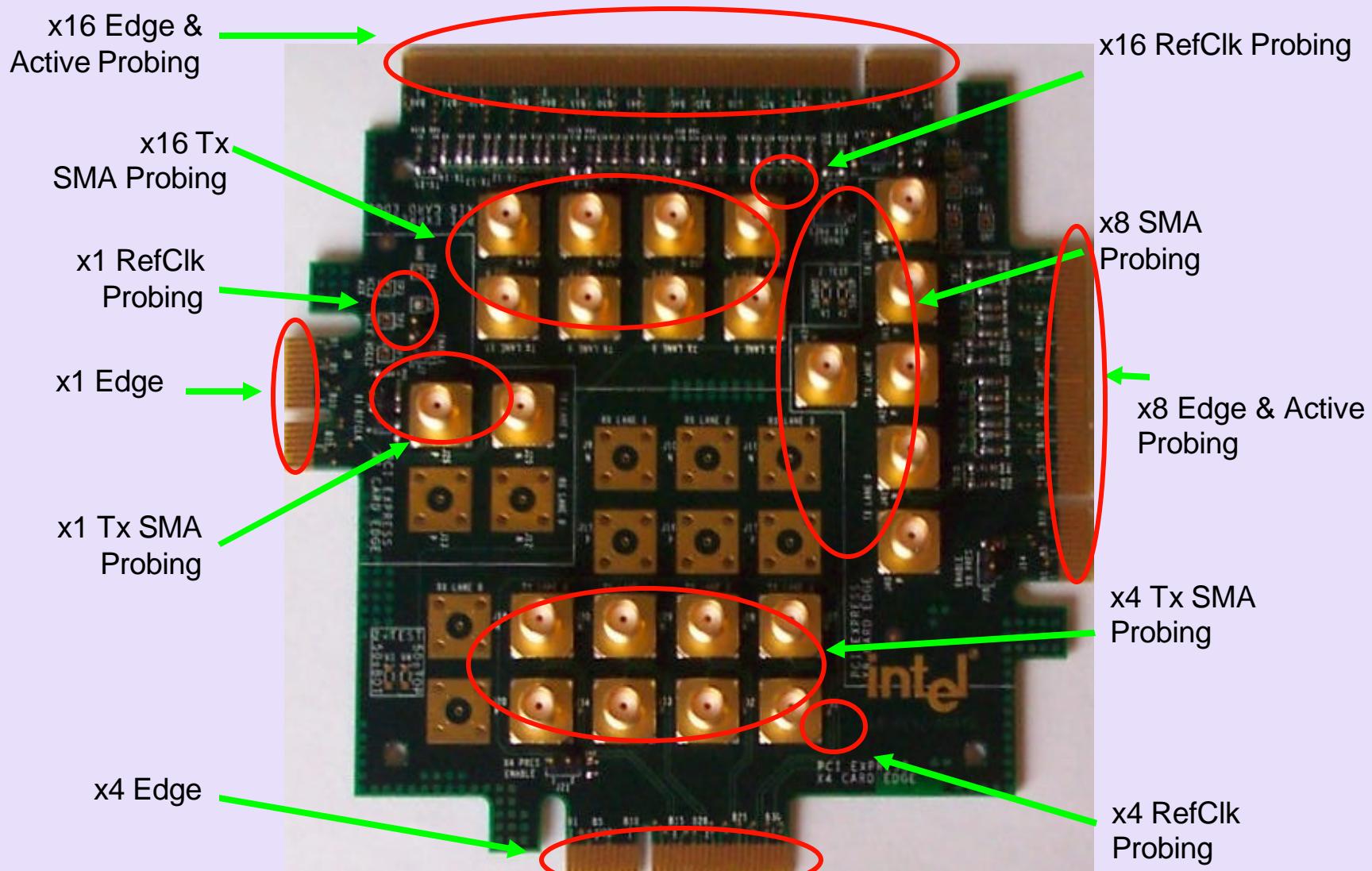
*Available thru
PCI SIG website*



- Capture waveform on oscilloscope
- Run Eye analysis software



CLB For PCI Express 1.0a



Reference Clock Jitter Testing

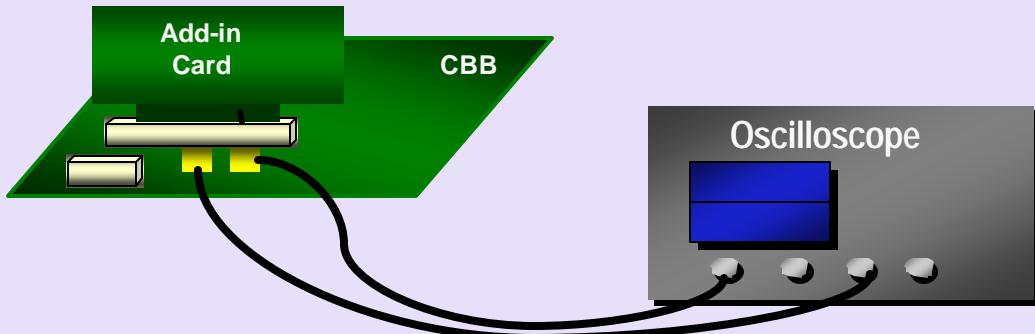
- New ECN puts tighter requirements on platform RefClk jitter
- New test being introduced to analyze jitter on RefClk
 - ✓ Will be integrated into SIGTEST tool
 - ✓ Will use standard Compliance Load Board
- Test will be introduced as FYI in Fall 2004 workshops

Adapter Electrical Tools

■ Compliance Base Board

- ✓ PCI Express x1, x16 connectors
 - PCI Express x16 provides termination x16 through x1
- ✓ Power adaptor + current measurement
- ✓ Rx for PCI Express x1 up to x8
- ✓ Reference clock or external input

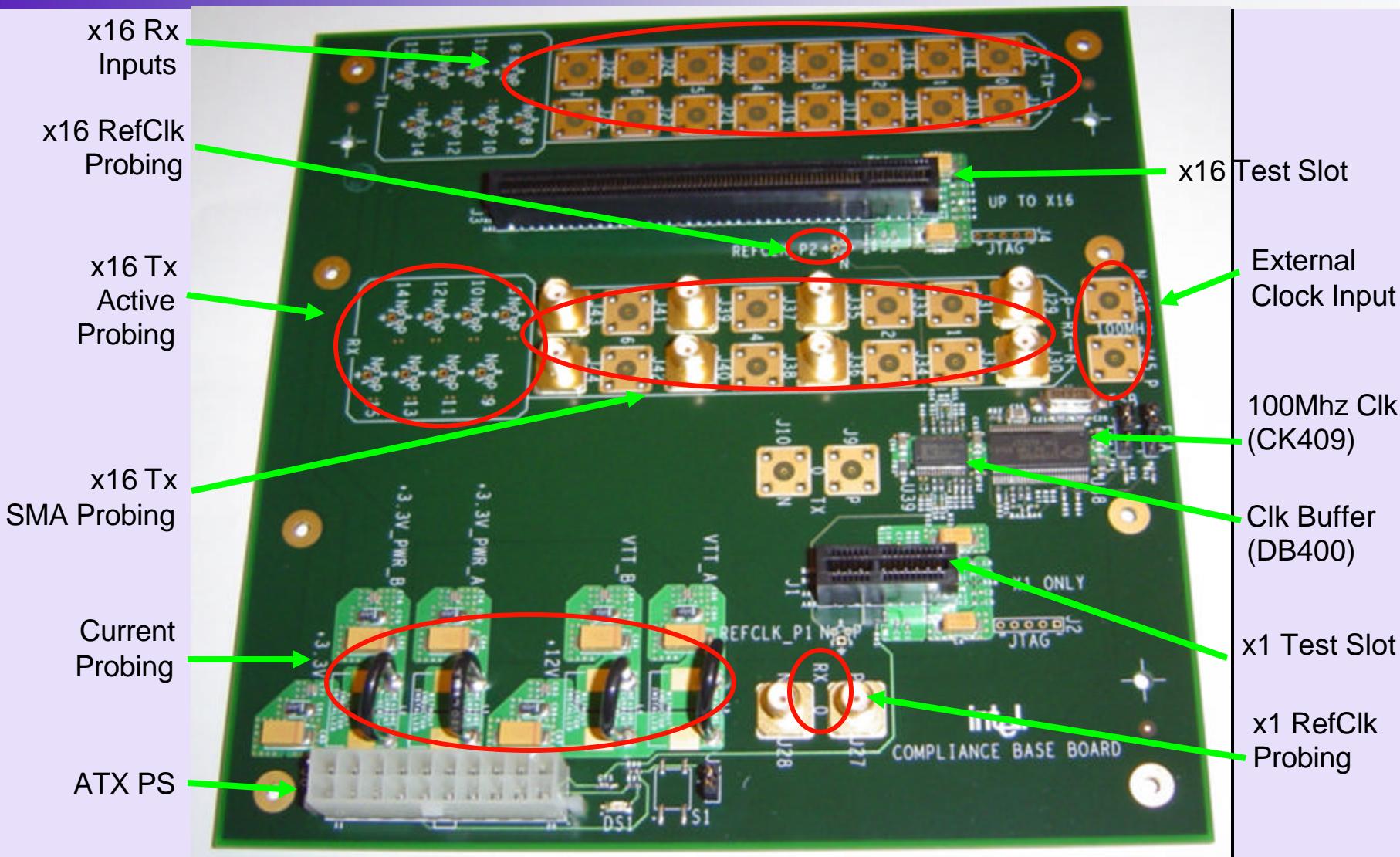
*Available thru
PCI SIG website*



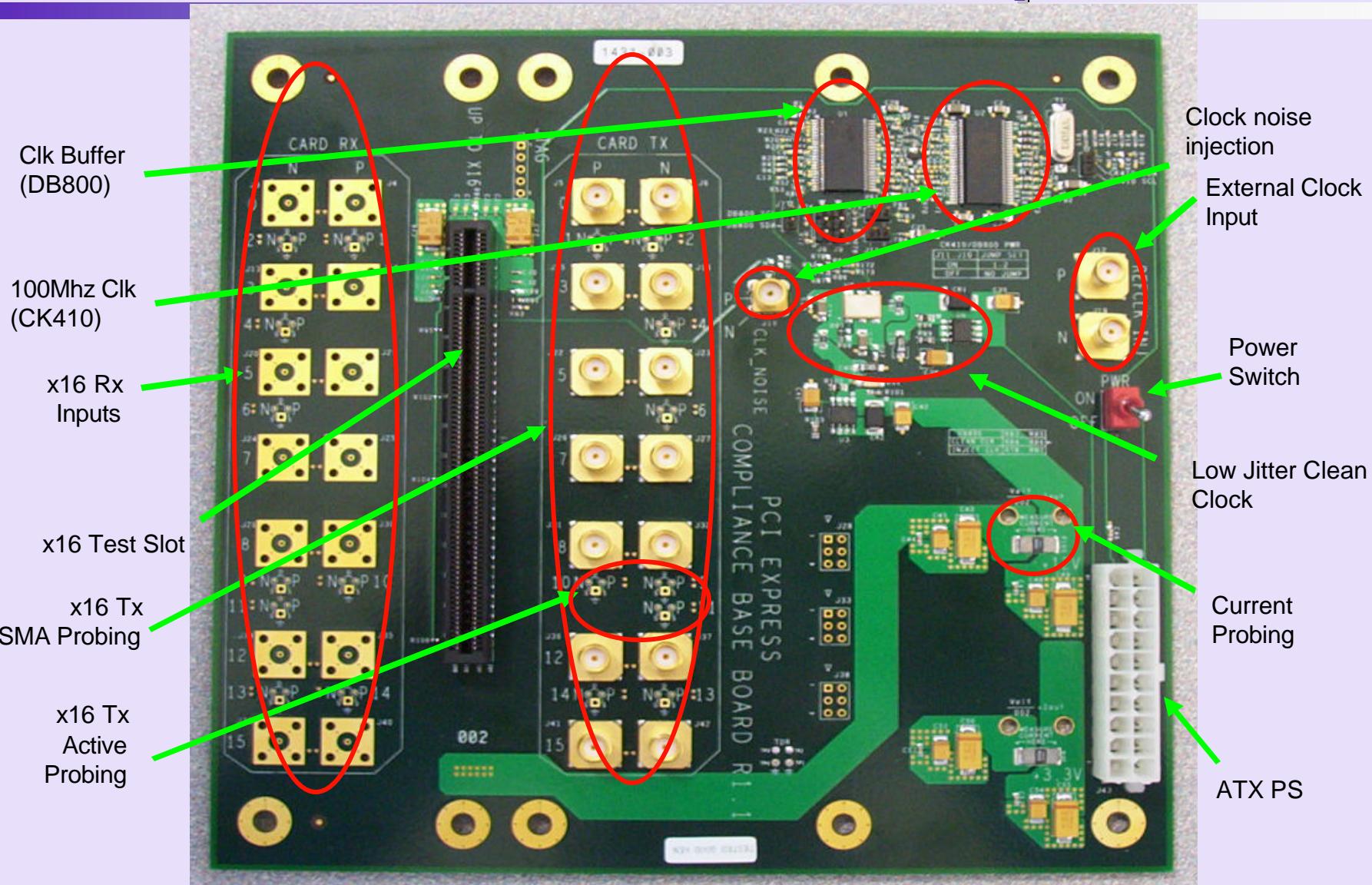
- Capture waveform on oscilloscope
- Run Eye analysis software



CBB For PCI Express 1.0a



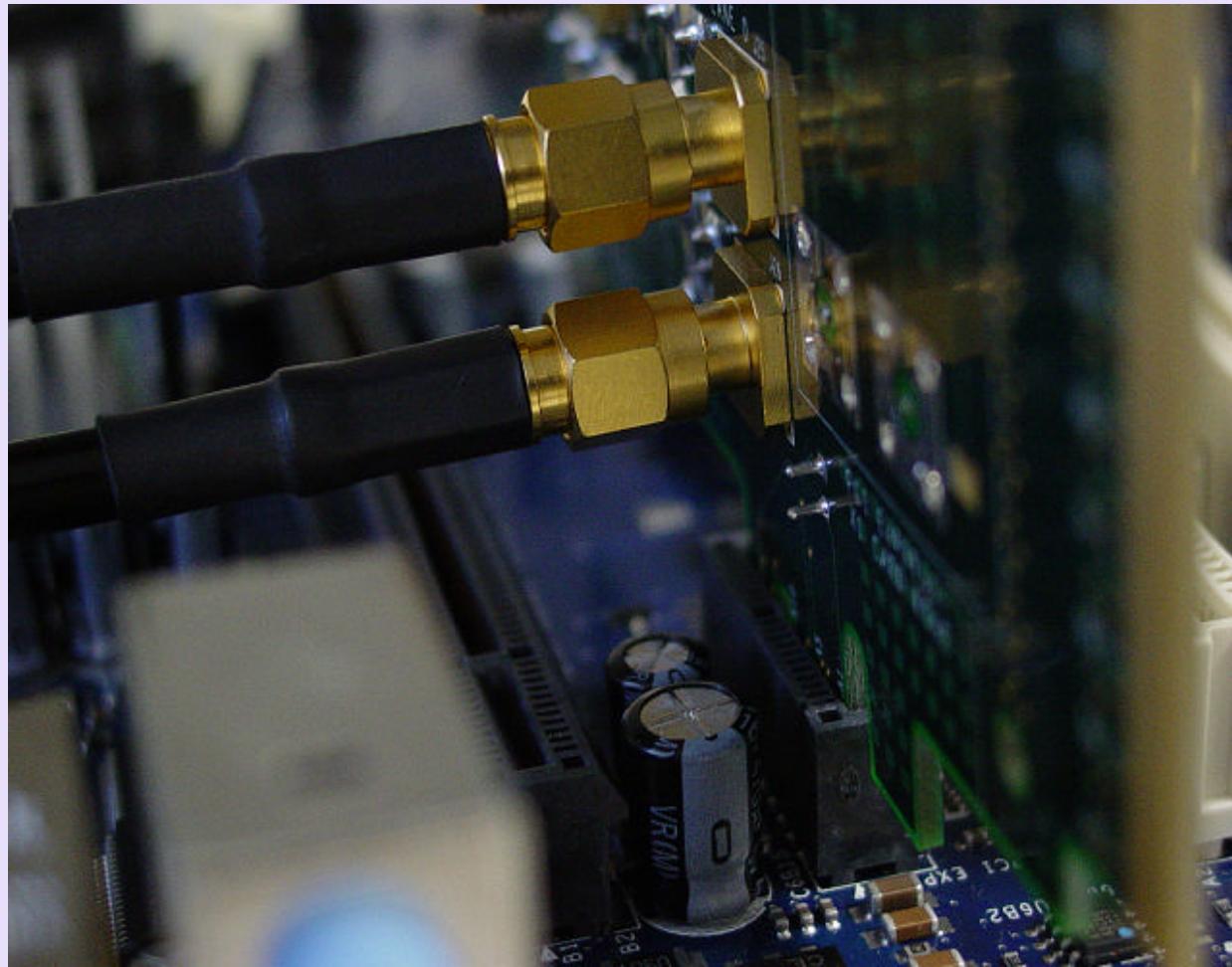
Revised CBB For PCI Express 1.1



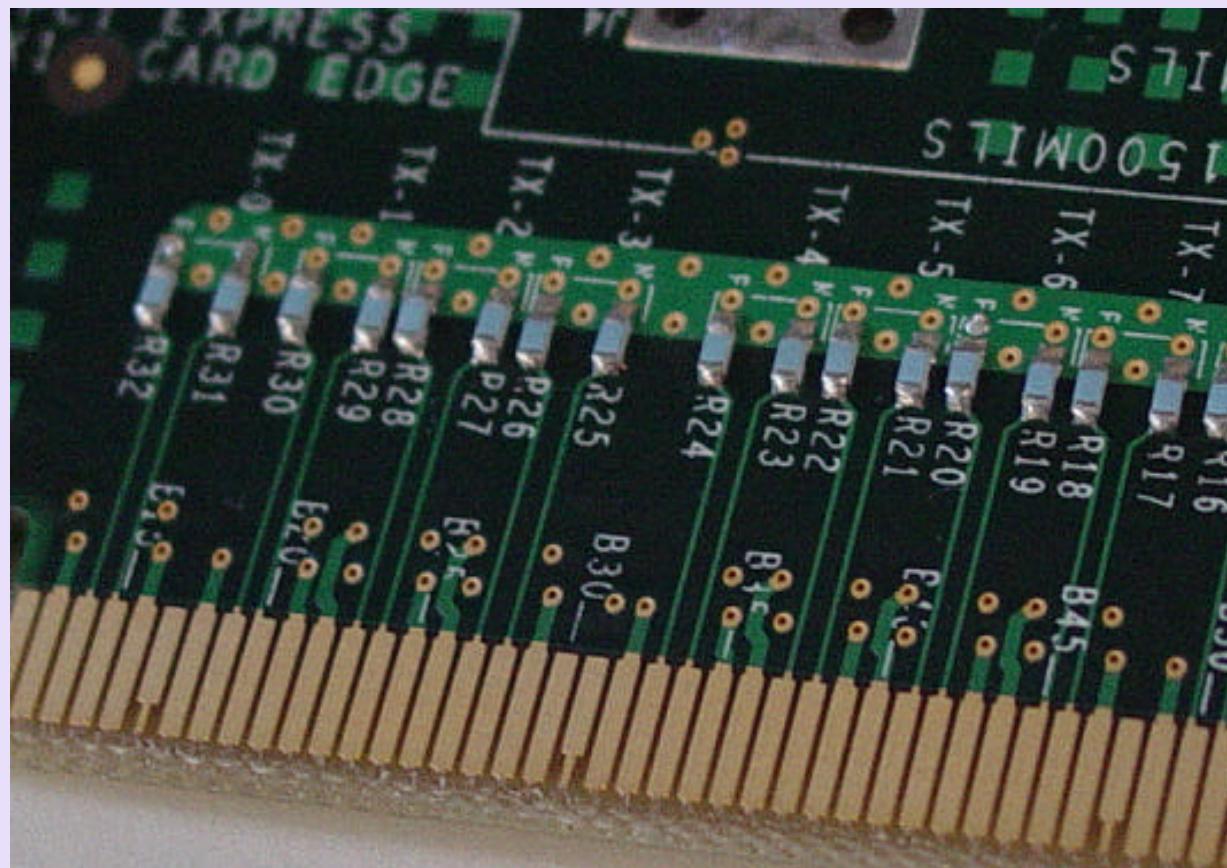
Clean Clock Testing

- Compliance base board built to have a RefClk with very little jitter
- Provides accurate picture of exactly how much jitter device-under-test has
- Will be introduced as FYI in Fall 2004 workshops
 - ✓ For availability of all test fixtures, visit www.pcisig.com

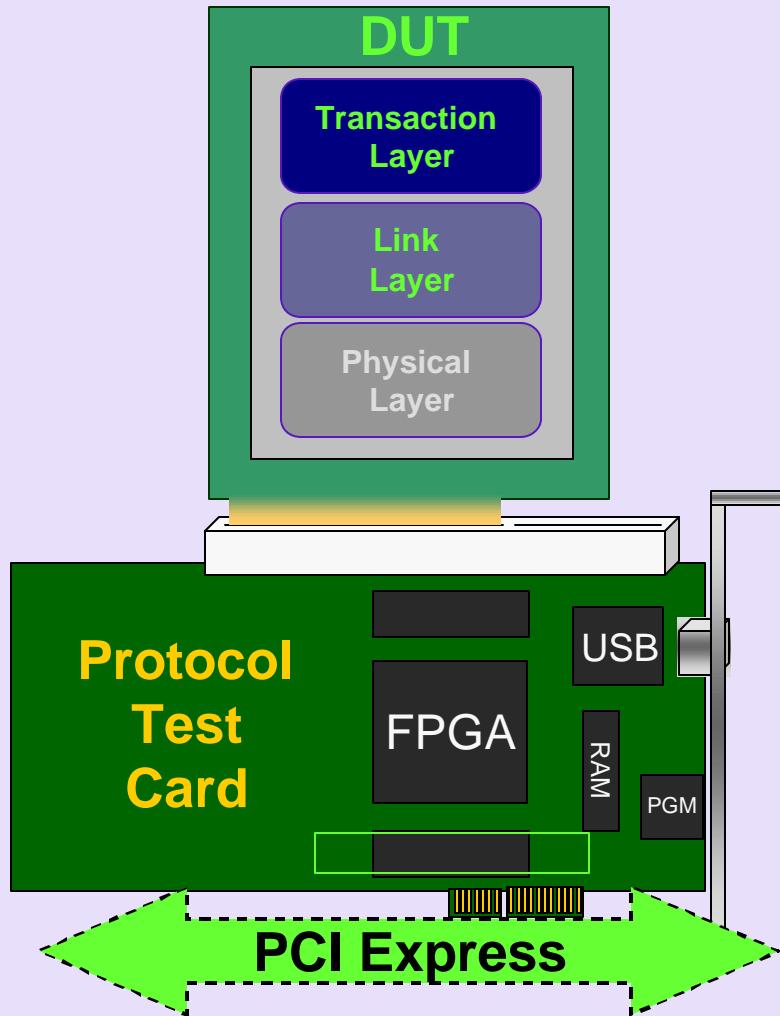
SMA Probing



Resistor Terminations

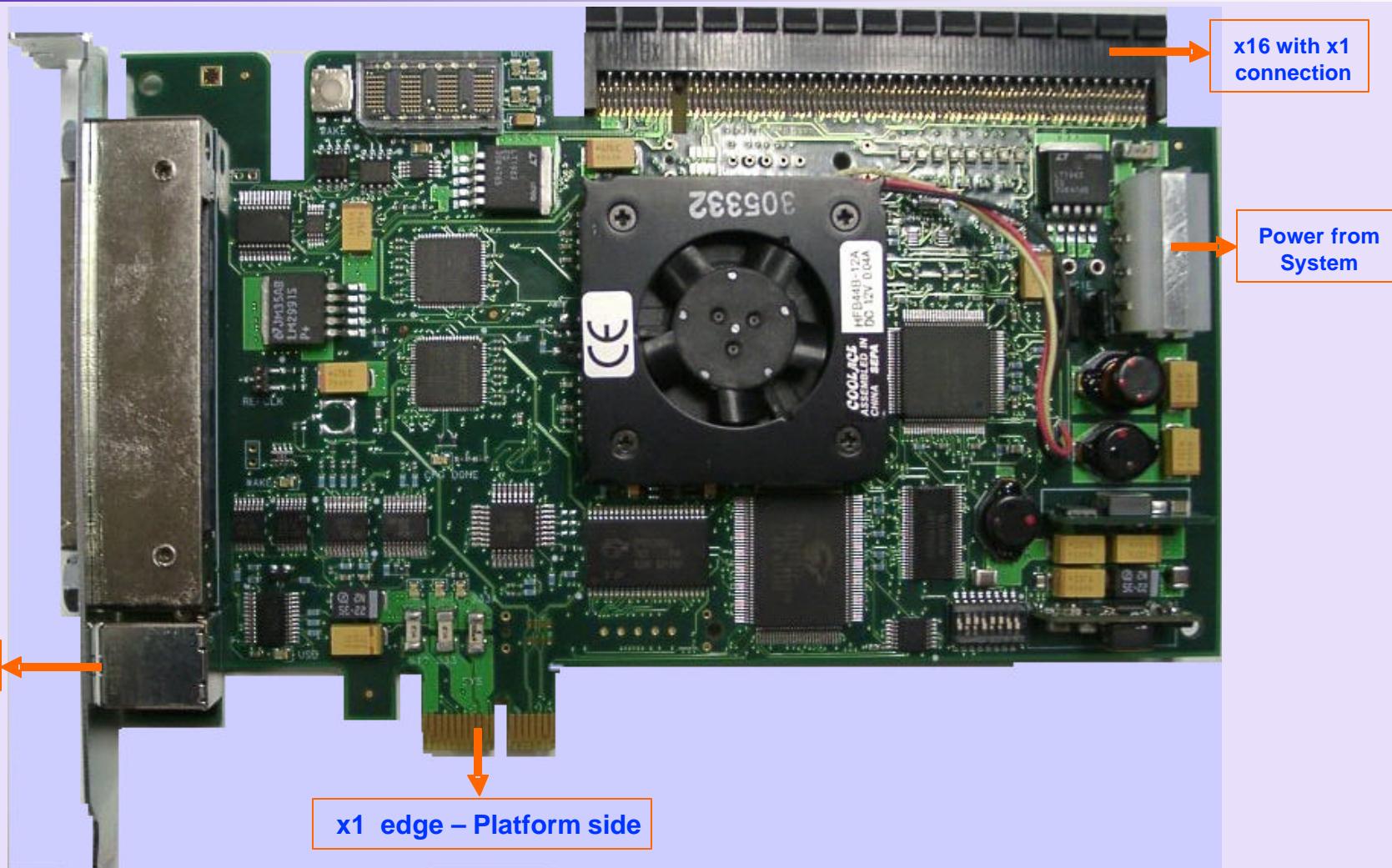


Protocol Testing



- **Test Control software** running on platform or Device Under Test (DUT) initiates test traffic
- **PTC monitors and acts on that traffic**
 - ✓ Checking protocol
 - ✓ Injecting errors

Protocol Test Card (PTC)



Link Compliance Tests

- Described in Data Link Test Spec
- Tests
 - ✓ Reserved fields – Device ignores them
 - ✓ NAK response – Device will resend after receiving NAK
 - ✓ Replay Timers – Device will resend packet if no response
 - ✓ Replay Count - Device will resend multiple times when no response
 - ✓ Link Retrain - Device will retrain if continued no response
 - ✓ Replay TLP order – Device replays TLPs in proper order
 - ✓ Bad CRC - Device detects, drops, and logs (DLLPs & TLPs)
 - ✓ Undefined packet – Device ignores
 - ✓ Bad Sequence Number – Device detects, drops, and logs
 - ✓ Duplicate TLP - Device returns data once

Link Replay Timer Test

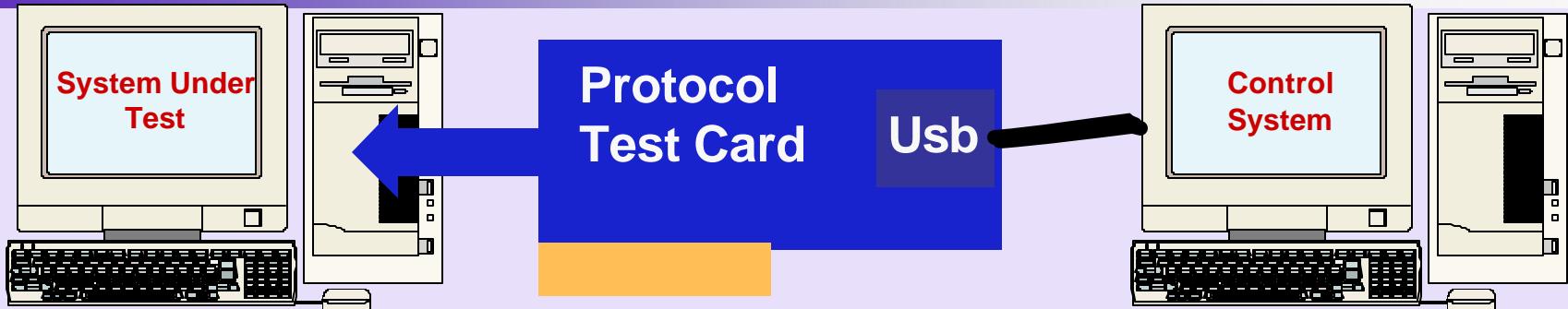
- Get device up and running
- Host does Config_Rd_Req to device
- PTC blocks Config_Rd_Completion from device
- PTC verifies that device ‘replays’ completion

Transaction Compliance Focus

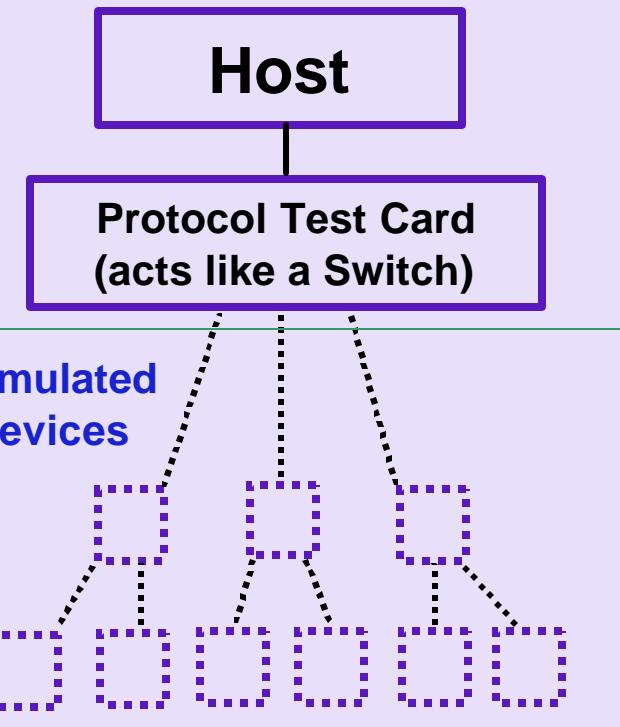
- **Basic Functional**
 - ✓ Completion request
 - ✓ Completion timeout
 - ✓ Read data
- **Baseline Messaging**
 - ✓ Legacy interrupts
 - ✓ Native power management
 - ✓ Native Hot Plug
 - ✓ Error Signaling
- **Flow Control**
 - ✓ Initialization
 - ✓ Transmit and Receive states
 - ✓ Negotiated link width
- **Virtual Channel**

See Test Spec
for Details

Platform BIOS Testing



- Protocol Test Card Can Represent Any Hierarchical Multi-Device/Bridge Topology



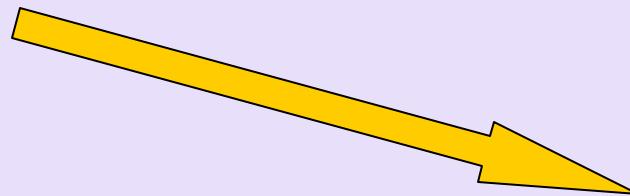
- Device Decodes All Type 0 and Type 1 Configuration Cycles

BIOS Test Areas

- **Multiple Functions per device**
- **Different BAR combinations**
 - ✓ I/O, Mem, 64bit
 - ✓ Various size requests
 - ✓ Prefetchable, non-prefetchable
- **Option ROMs**
 - ✓ Varying sizes
 - ✓ Different for each device function
 - ✓ Shrinkable, removable
- **Switches and Bridges**

PCI-SIG Compliance Program

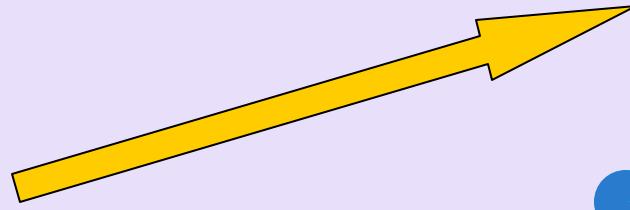
① **Compliance Tests**



② **Demonstrated Interoperability**



③ **Checklists**



Integrators List Requirements

- **Components have to be on motherboards or add-in cards**

- **Attend a Compliance Workshop**
 - ✓ Compliance testing is done there
 - ✓ Interoperability testing is done there

- **Turn in appropriate checklist**
 - ✓ Component vendors turn in single checklist
 - ✓ Motherboard and add-in card checklists reference checklist(s) of component(s) they are using

Top 5 ‘Things To Look For’

- ① Platform: Make sure RefClk is good**
- ② Device: Check operation with and without SSC**
- ③ Device: Must handle link resets and re-trains**
- ④ Platform: Support PCI Express x1 cards in all slots**
- ⑤ Platform: Support cards that take up to 1 second to respond after reset**

PCI Express Compliance Workshops

- October 18-22: Taipei, Taiwan
- December 6-10: Milpitas, CA
- 2005 calendar being planned
- Signup info on SIG website:
 - ✓ www.pcisig.com
- Full testing for systems and add-in cards
- Excellent opportunity for interoperability testing

Compliance Summary

- **Final PCI Express 1.1 specifications available in 4Q04**
 - ✓ Your compatible architecture for new designs!
- **PCI Express 1.1 compliance collateral coming in 1H05**
 - ✓ Check with PCI-SIG for availability of revised PCI Express 1.1 CBB
- **PCI Express BER/Jitter whitepapers available now**
- **PCI Express SIOM, 150W CEM specifications nearing completion (target: 4Q04-1Q05)**
- **PCI Express WFF, Cable specifications in 1H05**
- **For all PCI Express material, visit www.pcisig.com**

Agenda

8:30	Registration	
9:00	PCIe Architecture Overview & 1.1 Updates	Bhatt
10:00	Phy Layer Design	Peng
11:00	Jitter Updates	Froelich
12:00	LUNCH	
1:00	Compliance Requirements	Hosler
2:00	PM BREAK	
2:30	Form Factor Updates <i>150W Gfx, Mini CEM, SIOM, Wireless, Cable</i>	Noble
4:00	Q&A	Bhatt, et al

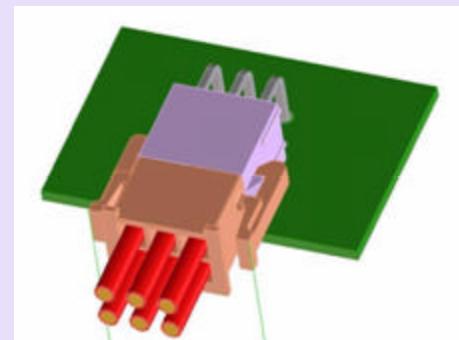
PCI Express High-End Graphics

■ Objectives

- ✓ Enable the richest graphics and multimedia experience on computing platforms
- ✓ Standardize power level and distribution

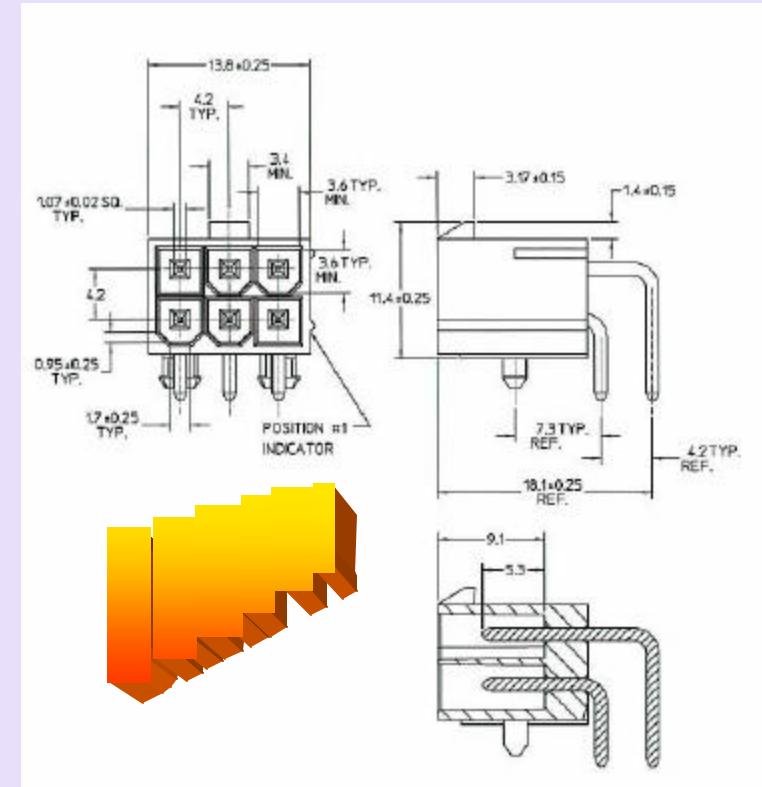
■ Increases PCI Express x16 graphics power dissipation to 150W

- ✓ Dedicated and unique power supply connector
 - 2x3 connector directly cabled to the PSU for supplemental 75W
 - Does not support dongles or adapters



Supplemental Power Connector

- PRELIMINARY drawing of the right-angle, through-hole PCB connector
 - ✓ 3 +12V pins, 2 ground pins, 1 sense pin (tied to ground in PSU or cable connector)
 - ✓ 8A/pin max current
 - ✓ Polarized
 - ✓ Retention lock
- Cable will use 18AWG wire
- 12V “rules”
 - ✓ Source has +5/-8 % tolerance
 - ✓ The card MUST keep this 12V rail separate from the 12V rail from the slot!
 - ✓ Max voltage variation between the 12V rails is 1.92V



Dimensions Subject To Change ... Do NOT Proceed With Design

High-End Graphics Current Status

- Version 0.9 of the PCI Express High-End Graphics specification has been released for PCI-SIG member review
 - ✓ Review period ends in October
 - ✓ Final expected in 4Q04-1Q05
- Initial focus is on ATX chassis solution
 - ✓ Card may use the space of the adjacent expansion slot
- BTX chassis specification in requirements phase

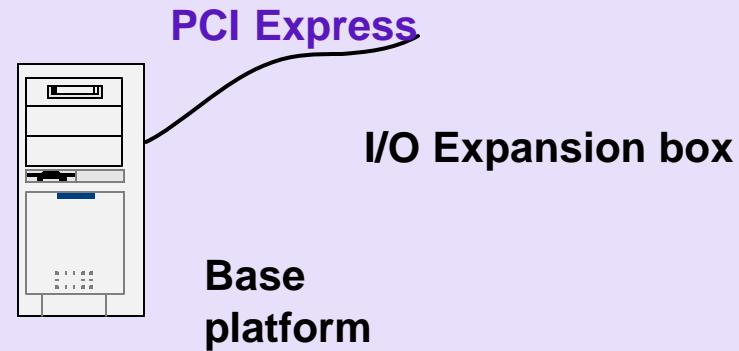
PCI Express External Cabling

- **Why?**
 - ✓ Extend PCI Express protocol / functionality across arbitrary distances and packaging
 - Needs that cannot be met using existing backplane connectivity
- **PCI Express Cable specification provides**
 - ✓ Standard cable connectors
 - ✓ Copper cabling attributes and electrical characteristics
 - Optical cabling will be addressed later
- **What it is NOT**
 - ✓ PCI Express external cabling is NOT a replacement for cabling to USB or 1394 peripherals!

Cabling Usage Models Example

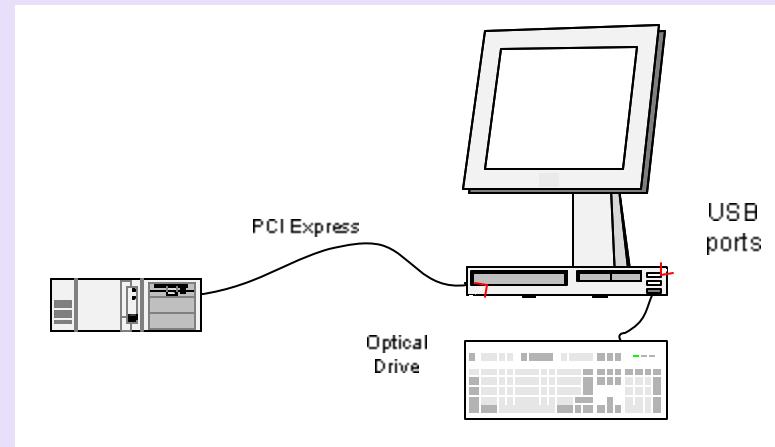
■ Expansion I/O

- ✓ Provide additional or different slot types beyond what is available in a base system
 - PCI Express CEM
 - PCI Express SIOM
 - ExpressCard® Module



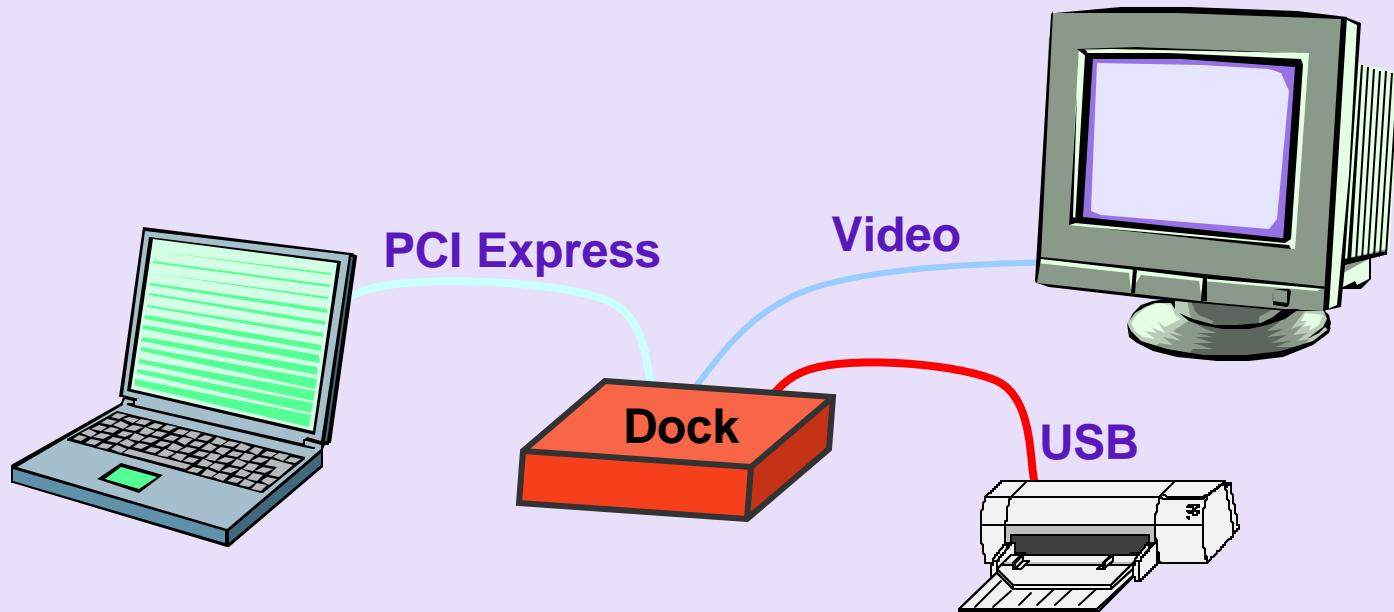
■ Split-system desktop

- ✓ Locate the user-accessible components (e.g. optical drive bay and USB ports) closer to the user
- ✓ Locate the “static” and “noisy” components (e.g. CPU, hard drive) further away from the user



Tethered Docking for Mobile Platforms Example

- Replace “rigid” docking station or port replicator with a tethered solution
 - ✓ Flexibility in placement of the laptop and docking station
 - ✓ Decouple laptop and docking station life-cycle



Cable Current Status

■ Evaluating connector proposals from suppliers

- ✓ PCI Express x1, x2, x4, x8 and x16 link widths
- ✓ Anticipate and support Gen2 signaling
- ✓ Sideband signals for compatibility with existing silicon and OS
 - Presence Detect, Reference Clock, WAKE#
- ✓ Optional power and SMBus for active signal conditioning within cable assembly

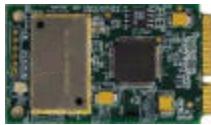
■ Cable length

- ✓ Simulations assume PCI Express signaling without additional equalization
 - 7 meters (without additional equalization or repeaters) seems feasible at the current 2.5Gbps
 - Active components (e.g. repeaters) will enable greater lengths
- ✓ Approximately 10dB of 13.2dB budget, at 1.25GHz, reserved for cable assembly
 - Includes cable loss, crosstalk, intra-pair skew, mated connectors, etc.
- ✓ Impact of Gen2 signaling currently unknown and not likely to be included with first release of the cable specification

■ Specification

- ✓ Revision 0.3 was released to and reviewed by PCI-SIG members
- ✓ Revision 0.5 is under development; expected release in September

Mobile Form Factor Summary

PCI Express Mini CEM	PCI Express WFF CEM	ExpressCard* Standard
Revision 1.1 – August 2004	0.5 Draft – August 2004	Release 1.0 – Sept. 2003
Communications-targeted BTO/CTO add-in card	Wireless-specific BTO/CTO add-in card	General purpose after-market upgrade module
Host I/O interfaces defined: PCI Express x1 and USB 2.0		
Communications-specific sideband signals defined		No application-specific sideband signals
	TBD	 

PCI-SIG

PCMCIA

PCI Express Mini CEM Updates

- **Revision 1.1 just completed**
 - ✓ In member review
- **Dynamic ref clock control defined**
 - ✓ CLKREQ# used in L1 link PM state
- **Wireless Disable feature defined**
 - ✓ Support required RF kill switch in platform
- **UIM/SIM interface defined**
 - ✓ Enable off-card SIM support in platform
- **Edge chamfer redefinition**
 - ✓ Improved manufacturability

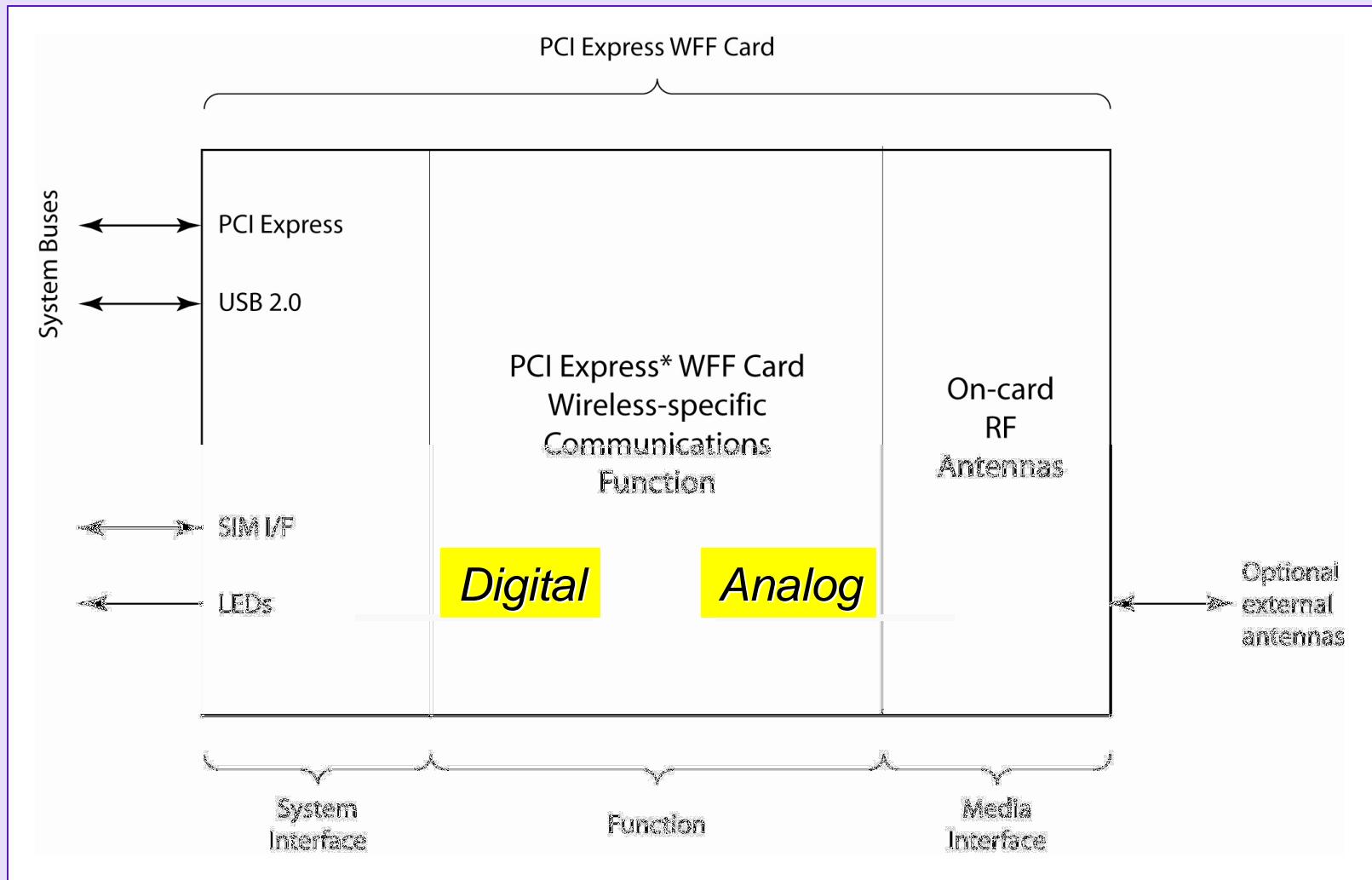
ExpressCard® Standard Updates

- Published addendum covers updates to Release 1.0
- Dynamic ref clock control defined
 - ✓ CLKREQ# used in L1 link PM state
- Module serial numbers
 - ✓ Used to establish eject dependencies for modules using both PCIe & USB with native operating system support
- PCIe reset and clock control clarification
 - ✓ Assure proper CLKREQ# to PERST# timing relationship
- Card presence & PCIe reset clarification
 - ✓ Assure proper PERST# operation prior to module insertion
- Connector guide feature improvement
 - ✓ Resolves potential slot door flap interference
- Label area clarification
 - ✓ Resolves potential label & grounding clip interference
- Finger grip dimension change
 - ✓ Resolves potential stacked slot interference

PCI Express Wireless Form Factor

- Targeting wireless applications intended to fit in notebook display lid
- BTO/CTO like PCI Express Mini CEM but:
 - ✓ Lower in profile – $\frac{1}{2}$ as thick
 - ✓ Larger in area – 2 $\frac{1}{2}$ times
 - ✓ Includes provisions for on-card antennas
 - ✓ Easier insertion / removal
- PCIe WFF CEM Spec currently at 0.5
 - ✓ Q1'05 targeted for 1.0 candidate release

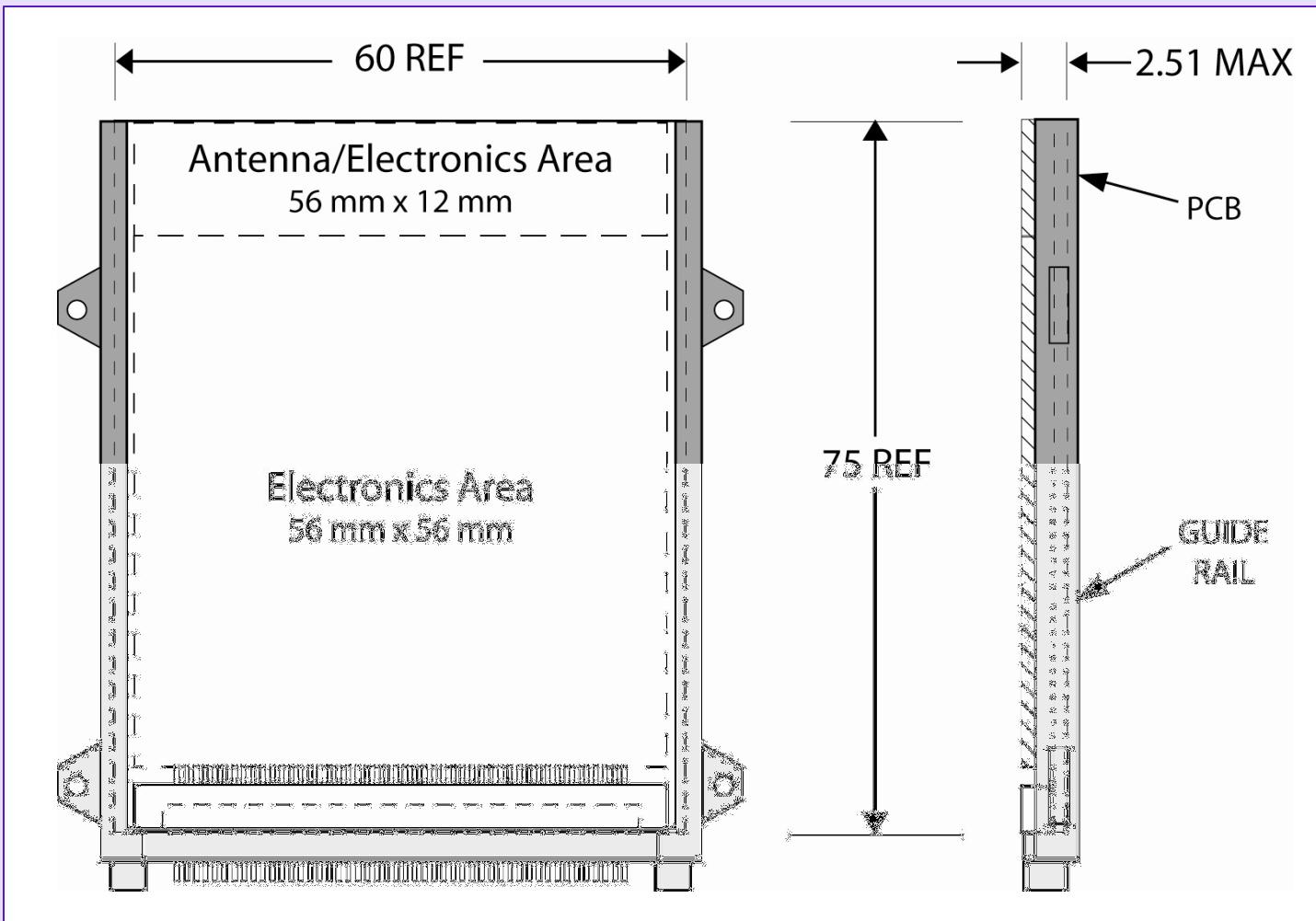
WFF CEM : Logical Representation



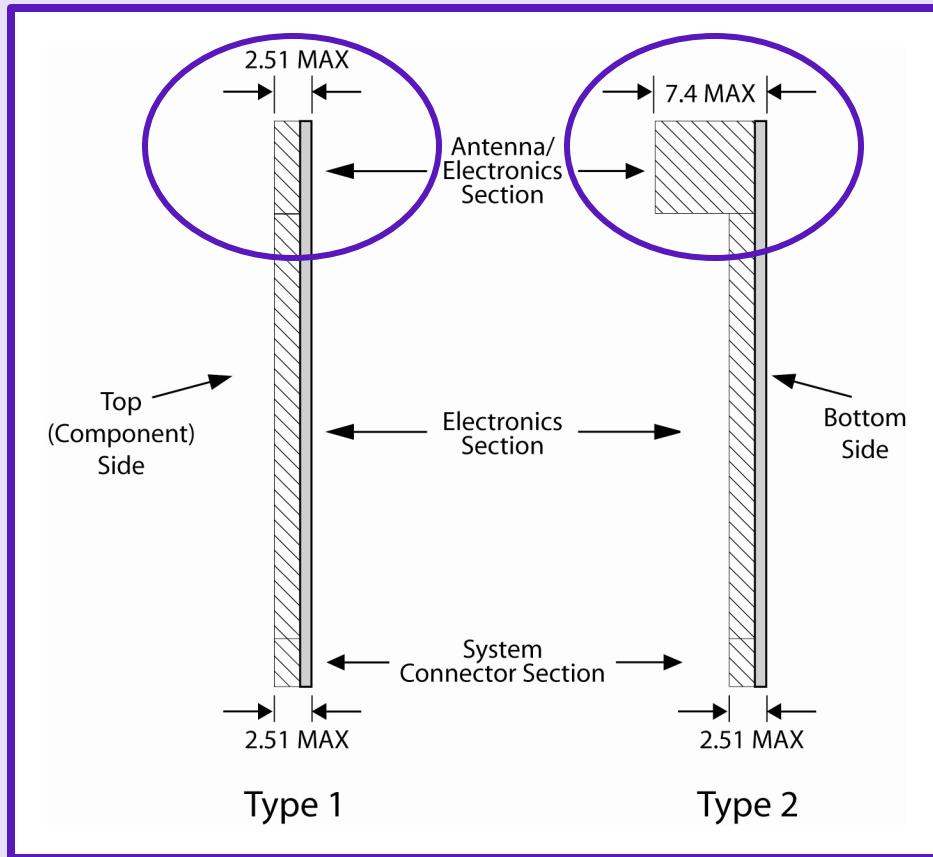
WFF CEM : Defining Characteristics

	Characteristics	Status
Wireless Targets	802.11a/b/g/n; CDMA 2000, GSM/GPRS, EDGE, WCDMA; 802.16a/e; UWB	✓
Antenna Support	Defined on-card area – 56mm x 12mm Two height options – 2.51mm or 7.4mm Optional off-card antenna support with two defined RF connectors	✓
Wireless Features	RF Disable, SIM support, Status Indicators, provision for coexistence solution	✓
Host Interfaces (OEM selectable)	PCI Express x1 with reset, ref clock with clock enable control, & wake support USB 2.0	✓
Power	+3.0V – +3.4V : 2.5A peak / 1.1A average / 250mA AUX support	Open
Thermals	2.5W TDP – <i>modeling/testing in progress</i>	Open
Host Connector	Beam-on-Blade style, single in-line 40 pin low durability (250 cycles)	✓

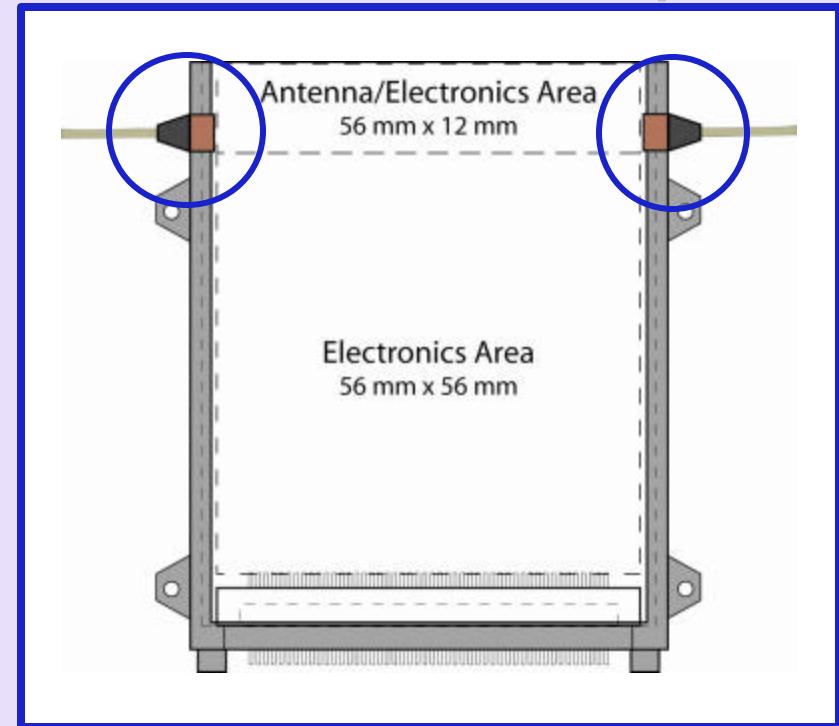
WFF CEM : Form-Factor Summary



On-card Antenna options



Off-card Antenna options



Coordination Between Platform OEMs & Card Vendors Required

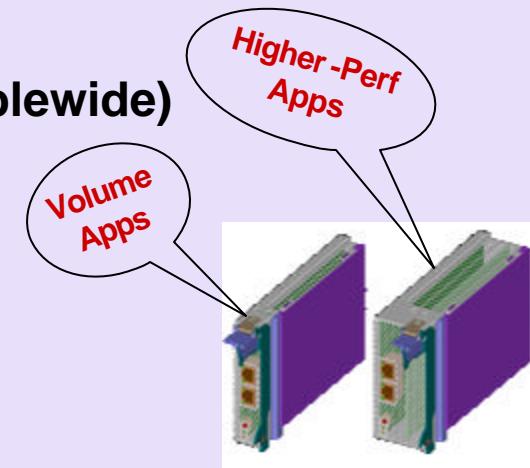
WFF CEM : Other Key Factors

- **Cabling through the notebook hinge required**
 - ✓ Complexity & performance depends on host interface
 - ✓ Significant factor impacting signal integrity & power delivery
- **Display thermals and interference**
 - ✓ LCD temperature sensitivities above 50°C
 - ✓ Major area of continued investigation & validation
- **On-card antenna limitations**
 - ✓ Some lower RF bands and diversity solutions may not fit
 - ✓ Complex multi-band radios may be challenging
 - ✓ Optional RF connections defined to augment on-card solutions

PCI Express Server I/O Module

■ Key Features

- ✓ Two module sizes defined (singlewide and doublewide)
 - Singlewide module (112mm x 170mm x 22mm)
 - Doublewide module (112mm x 170mm x 45mm)
- ✓ Closed chassis hot-plug
- ✓ Hot-plug is shared between adapter and system
- ✓ Module/chassis airflow requirements defined
- ✓ Backplane connector is enhanced PCI Express card connector (improved lead-in for blind mate)
- ✓ Electrical/thermal requirements are the same as PCI Express cards
- ✓ Module supports optional chassis lock feature
- ✓ Optional internal storage interface & sideband signals
- ✓ Module PCB area about the same as ½ length PCI card
- ✓ Singlewide supports up to 8 lanes, doublewide up to 16 lanes

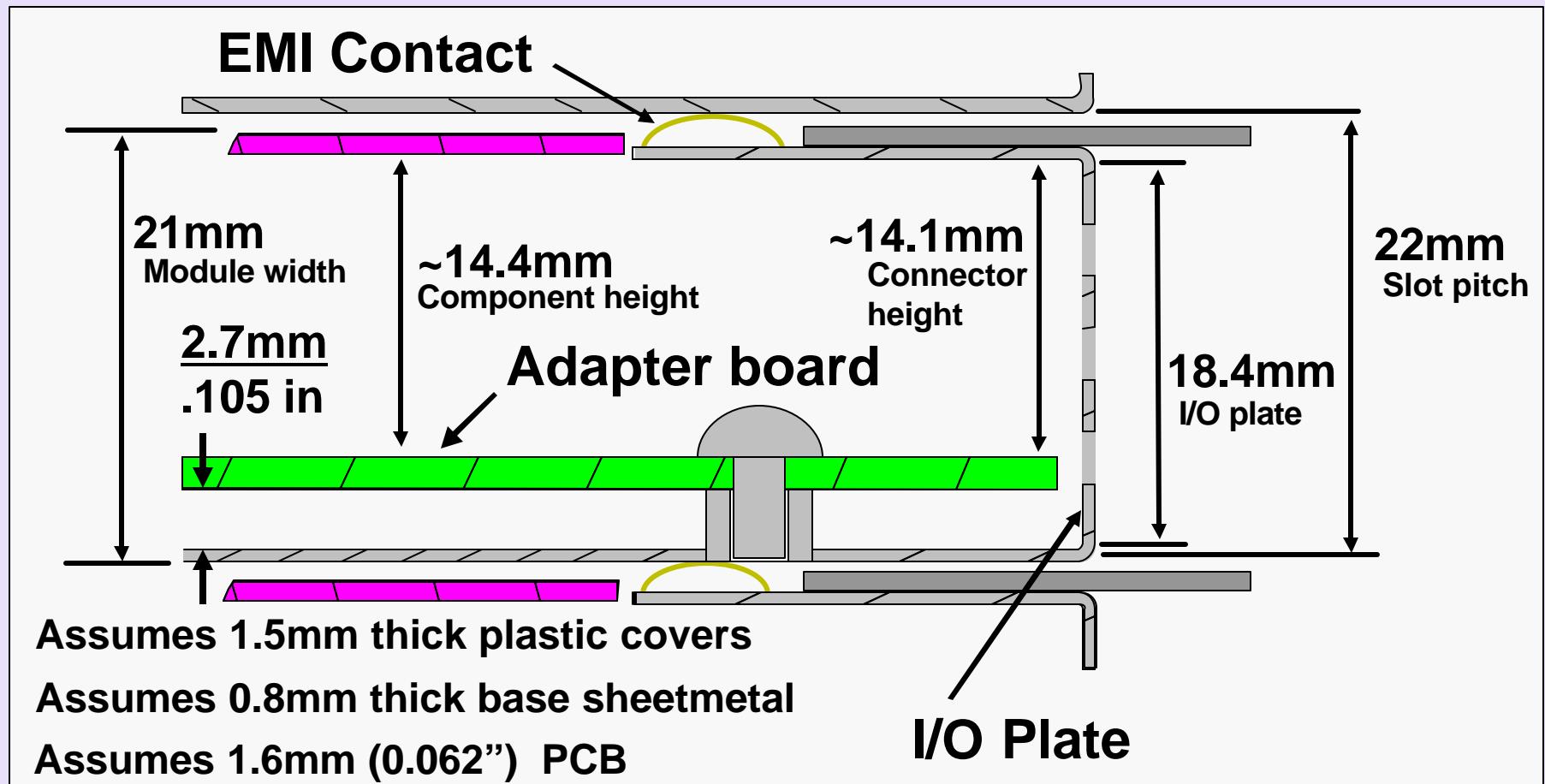


PCI Express Server I/O Benefits

- **Customer Replaceable**
 - ✓ Enables new service/support opportunities
- **Customer Friendly**
 - ✓ Hot-plug design prevents damage to adapter or chassis
- **Enhances System Reliability, Reduces Down Time**
- **Reduces I/O Footprint**
 - ✓ Modules sized for different applications
- **Enables System Design Flexibility**
 - ✓ I/O no longer tied to system board
 - ✓ Module slot can be placed in different chassis locations

SIOM Inter-Module Spacing

Cut-away view showing adapter board spacing

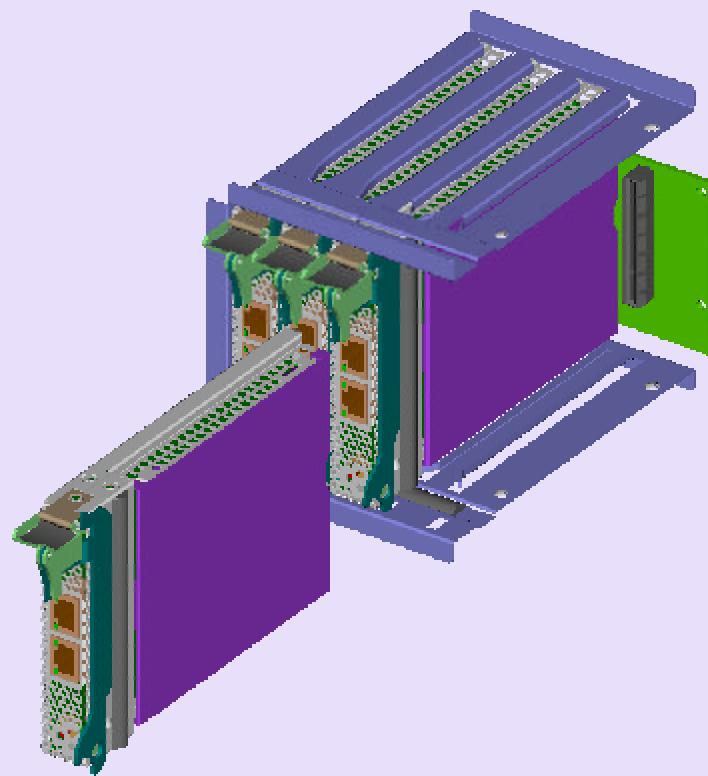


Inter-Module Component Space Is Less Than PCI Express Card

PCI Express Server I/O Module

■ Work-In-Process

- ✓ Systems management section review
- ✓ Mechanical section review
- ✓ EMI requirements review
- ✓ Hot-Plug section review
- ✓ Thermal section review



Form Factor Summary

- PCI Express High-End Graphics specification meets the needs of power-hungry GPUs for gamer applications
- PCI Express Wireless Card specification facilitates interference-free applications for mobile platforms
- PCI Express Cable specification enables disaggregated I/O and inter-chassis applications
- PCI Express SIOM specification enables hot-plugged and fully managed I/O modules for enterprise systems
- For all PCI Express specifications, visit www.pcisig.com

Agenda

8:30	Registration	
9:00	PCIe Architecture Overview & 1.1 Updates	Bhatt
10:00	Phy Layer Design	Peng
11:00	Jitter Updates	Froelich
12:00	LUNCH	
1:00	Compliance Requirements	Hosler
2:00	PM BREAK	
2:30	Form Factor Updates <i>150W Gfx, Mini CEM, SIOM, Wireless, Cable</i>	Noble
4:00	Q&A	Bhatt, et al

PCI  **SIG™**

