Information technology —
Telecommunications and information exchange between systems —
Local and metropolitan networks — specific requirements
Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications —

Amendment: Physical Layer and Management Parameters for 10 Gb/s Operation — Type 10GBASE-T

Sponsor

LAN MAN Standards Committee
of the
IEEE Computer Society

This Draft amendment to IEEE Std. 802.3 provides support to extend 10 Gb/s operation over ISO/IEC 11801:2002 Class E and Class F channels with a new Physical Layer (PHY) device. The PHY is known as 10GBASE-T. This draft D1.1 is being circulated as part of Task Force Ballot. The formal expiration date of this draft is November 19, 2004.

28. Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

28.1 Overview

28.1.1 Scope

Clause 28 describes the Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. The normative definitions for all extensions to Auto-Negotiation and all related register assignments for this standard are documented in Annex 28D.

The objective of the Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-Negotiation is performed using a modified 10BASE-T link integrity test pulse sequence, such that no packet or upper layer protocol overhead is added to the network devices (see Figure 28–1). Auto-Negotiation does not test the link segment characteristics (see 28.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10BASE-T, 100BASE-TX, and 100BASE-T4 compatible devices to be recognized, even though they may not provide Auto-Negotiation.

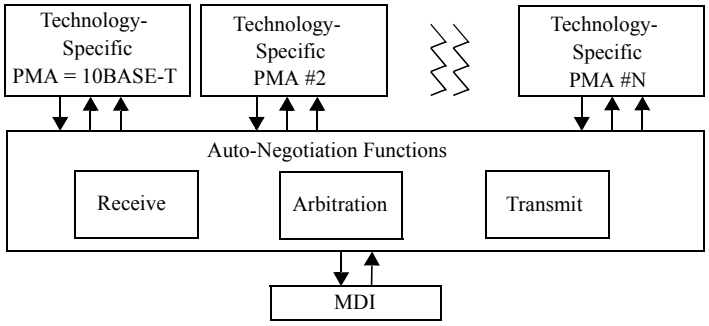


Figure 28–1—High-level model

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse (Figure 14–12). This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst. Each device capable of Auto-Negotiation issues FLP Bursts at power up, on command from management, or due to user interaction. The FLP Burst consists of a series of link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word that identifies the operational modes supported by the remote device, as well as some information used for the Auto-Negotiation function's handshake mechanism.

To maintain interoperability with existing 10BASE-T devices, the function also supports the reception of 10BASE-T compliant link integrity test pulses. 10BASE-T link pulse activity is referred to as the Normal Link Pulse (NLP) sequence and is defined in 14.2.1.1. A device that fails to respond to the FLP Burst sequence by returning only the NLP sequence is treated as a 10BASE-T compatible device.

28.1.2 Application perspective/objectives

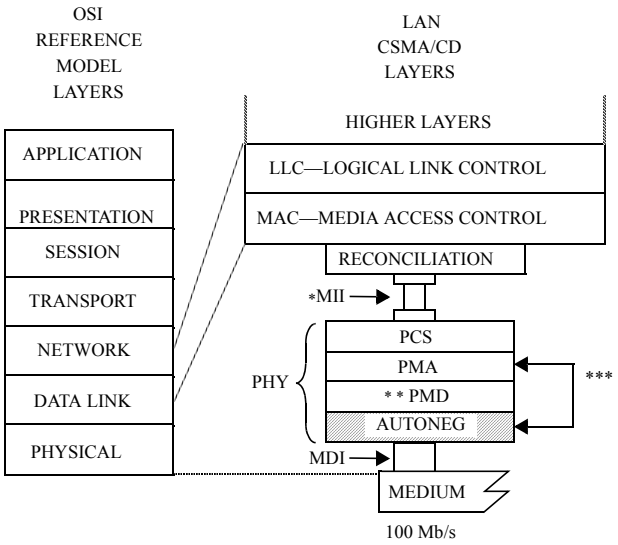
The Auto-Negotiation function is designed to be expandable and allow IEEE 802.3 compatible devices using an eight-pin modular connector to self-configure a jointly compatible operating mode. Implementation of the Auto-Negotiation function is optional. However, it is highly recommended that this method alone be utilized to perform the negotiation of the link operation.

The following are the objectives of Auto-Negotiation:

a) Must interoperate with the IEEE 802.3 10BASE-T installed base.
b) Must allow automatic upgrade from the 10BASE-T mode to the desired “High-Performance Mode.”
c) Requires that the 10BASE-T data service is the Lowest Common Denominator (LCD) that can be resolved. A 10BASE-T PMA is not required to be implemented, however. Only the NLP Receive Link Integrity Test function is required.
d) Reasonable and cost-effective to implement.
e) Must provide a sufficiently extensible code space to
    1) Meet existing and future requirements.
    2) Allow simple extension without impacting the installed base.
    3) Accommodate remote fault signals.
    4) Accommodate link partner ability detection.
f) Must allow manual or Network Management configuration to override the Auto-Negotiation.
g) Must be capable of operation in the absence of Network Management.
h) Must not preclude the ability to negotiate “back” to the 10BASE-T operational mode.
i) Must operate when
    1) The link is initially electrically connected.
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
j) The Auto-Negotiation function may be enabled by automatic, manual, or Network Management intervention.
k) Completes the base page Auto-Negotiation function in a bounded time period.
l) Will provide the basis for the link establishment process in future CSMA/CD compatible LAN standards that use an eight-pin modular connector.
m) Must not cause corruption of IEEE 802.3 Layer Management statistics.
n) Operates using a peer-to-peer exchange of information with no requirement for a master device (not master-slave).
o) Must be robust in the UTP cable noise environment.
p) Must not significantly impact EMI/RFI emissions.

28.1.3 Relationship to ISO/IEC 8802-3

The Auto-Negotiation function is provided at the Physical Layer of the OSI reference model as shown in Figure 28–2. Devices that support multiple modes of operation may advertise this fact using this function. The actual transfer of information of ability is observable only at the MDI or on the medium. Auto-Negotiation signaling does not occur across either the AUI or MII. Control of the Auto-Negotiation function may be supported through the Management Interface of the MII or equivalent. If an explicit embodiment of the MII is supported, the control and status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 28.2.4. If a physical embodiment of the MII management is not present, then it is strongly recommended that the implementation provide control and status mechanisms equivalent to those described in Clause 22 and 28.2.4 for manual and/or management interaction.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
*** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.

Figure 28–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

28.1.4 Compatibility considerations

The Auto-Negotiation function is designed to be completely backwards compatible and interoperable with 10BASE-T compliant devices. In order to achieve this, a device supporting the Auto-Negotiation function must provide the NLP Receive Link Integrity Test function as defined in Figure 28–18. The Auto-Negotiation function also supports connection to 100BASE-TX and 100BASE-T4 devices without Auto-Negotiation through the Parallel Detection function. Connection to technologies other than 10BASE-T, 100BASE-TX, or 100BASE-T4 that do not incorporate Auto-Negotiation is not supported.

Implementation of the Auto-Negotiation function is optional. For CSMA/CD compatible devices that use the eight-pin modular connector of ISO/IEC 8877: 1992 and that also encompass multiple operational modes, if a signaling method is used to automatically configure the preferred mode of operation, then the Auto-Negotiation function shall be used in compliance with Clause 28. If the device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities, the device shall implement the Auto-Negotiation function as administered by this specification. All future CSMA/CD implementations that use an eight-pin modular connector shall be interoperable with devices supporting Clause 28. If the implementor of a non-CSMA/CD eight-pin modular device wishes to assure that its operation does not conflict with CSMA/CD devices, then adherence to Clause 28 is recommended.

While this Auto-Negotiation function must be implemented in CSMA/CD compatible devices that utilize the eight-pin modular connector, encompass multiple operational modes, and offer an Auto-Negotiation mechanism, the use of this function does not mandate that the 10BASE-T packet data communication service must exist. A device that employs this function must support the 10BASE-T Link Integrity Test func-

tion through the NLP Receive Link Integrity Test state diagram. The device may also need to support other technology-dependent link test functions depending on the modes supported. Auto-Negotiation does not perform cable tests, such as detect number of conductor pairs (if more than two pairs are required) or cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring CRC or framing errors) to determine if the link segment is adequate.

28.1.4.1 Interoperability with existing 10BASE-T devices

During Auto-Negotiation, FLP Bursts separated by 16 ± 8 ms are transmitted. The FLP Burst itself is a series of pulses separated by 62.5 ± 7 µs. The timing of FLP Bursts will cause a 10BASE-T device that is in the LINK TEST PASS state to remain in the LINK TEST PASS state while receiving FLP Bursts. An Auto-Negotiation able device must recognize the NLP sequence from a 10BASE-T Link Partner, cease transmission of FLP Bursts, and enable the 10BASE-T PMA, if present. If the NLP sequence is detected and if the Auto-Negotiation able device does not have a 10BASE-T PMA, it will cease transmission of FLP Bursts, forcing the 10BASE-T Link Partner into the LINK TEST FAIL state(s) as indicated in Figure 14–6.

NOTE—Auto-Negotiation does not support the transmission of the NLP sequence. The 10BASE-T PMA provides this function if it is connected to the MDI. In the case where an Auto-Negotiation able device without a 10BASE-T PMA is connected to a 10BASE-T device without Auto-Negotiation, the NLP sequence is not transmitted because the Auto-Negotiation function has no 10BASE-T PMA to enable that can transmit the NLP sequence.

28.1.4.2 Interoperability with Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the base Link Code Word from the FLP Burst, and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's base Link Code Words by responding with FLP Bursts containing the Acknowledge Bit set. After both devices complete acknowledgment, and optionally, Next Page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in Annex 28B. It may subsequently be the responsibility of a technology-dependent link integrity test function to verify operation of the link prior to enabling the data service.

28.1.4.3 Cabling compatibility with Auto-Negotiation

Provision has been made within Auto-Negotiation to limit the resulting link configuration in situations where the cabling may not support the highest common capability of the two end points. The system administrator/installer must take the cabling capability into consideration when configuring a hub port's advertised capability. That is, the advertised capability of a hub port should not result in an operational mode that is not compatible with the cabling.

28.2 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PMA type, where more than one PMA type may exist. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the Auto-Negotiation Transmit, Receive, Arbitration, and NLP Receive Link Integrity Test functions and comply with the state diagrams of Figures 28–15 to 28–18. The Auto-Negotiation functions shall interact with the technology-dependent PMAs through the Technology-Dependent Interface. Technology-dependent PMAs include, but are not limited to, 100BASE-TX and 100BASE-T4. Technology-dependent link integrity test functions shall be implemented and interfaced to only if the device supports the given technology. For example, a 10BASE-T and 100BASE-TX Auto-Negotiation able device must implement and interface to the 100BASE-TX PMA/link integrity test function, but

does not need to include the 100BASE-T4 PMA/Link Integrity Test function. The Auto-Negotiation function shall provide an optional Management function that provides a control and status mechanism.

28.2.1 Transmit function requirements

The Transmit function provides the ability to transmit FLP Bursts. The first FLP Bursts exchanged by the Local Device and its Link Partner after Power-On, link restart, or renegotiation contain the base Link Code Word defined in 28.2.1.2. The Local Device may modify the Link Code Word to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multimode devices may Auto-Negotiate to a mode lower in priority than the highest common local ability.

28.2.1.1 Link pulse transmission

Auto-Negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link. Compliant 10BASE-T MAUs transmit link integrity test pulses as a mechanism to determine if the link segment is operational in the absence of packet data. The 10BASE-T NLP sequence is a pulse (Figure 14–12) transmitted every 16 ± 8 ms while the data transmitter is idle.

Auto-Negotiation substitutes the FLP Burst in place of the single 10BASE-T link integrity test pulse within the NLP sequence (Figure 28–3). The FLP Burst encodes the data that is used to control the Auto-Negotiation function. FLP Bursts shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PMA has been enabled.

FLP Bursts were designed to allow use beyond initial link Auto-Negotiation, such as for a link monitor type function. However, use of FLP Bursts beyond the current definition for link startup shall be prohibited. Definition of the use of FLP Bursts while in the FLP LINK GOOD state is reserved.

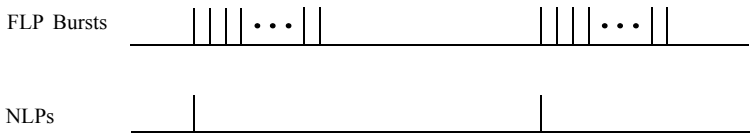


Figure 28–3—FLP Burst sequence to NLP sequence mapping

28.2.1.1.1 FLP burst encoding

FLP Bursts shall be composed of link pulses meeting the requirements of Figure 14–12. A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. Clock pulses are differentiated from data pulses by the spacing between pulses as shown in Figure 28–5 and enumerated in Table 28–1. Extended FLP Bursts contain 97 pulse positions with 49 clock pulses and 48 data pulses.

The encoding of data using pulses in an FLP Burst is illustrated in Figure 28–4.

28.2.1.1.2 Transmit timing

The first pulse in an FLP Burst shall be defined as a clock pulse. Clock pulses within an FLP Burst shall be spaced at 125 ± 14 µs. If the data bit representation of logic one is to be transmitted, a pulse shall occur 62.5

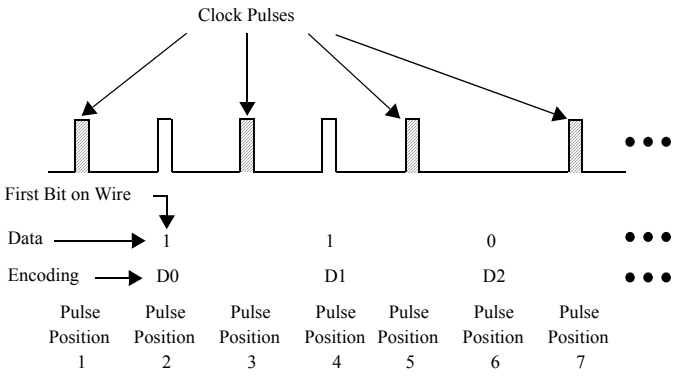


Figure 28–4—Data bit encoding within FLP Bursts

± 7 µs after the preceding clock pulse. If a data bit representing logic zero is to be transmitted, there shall be no link integrity test pulses within 111 µs of the preceding clock pulse.

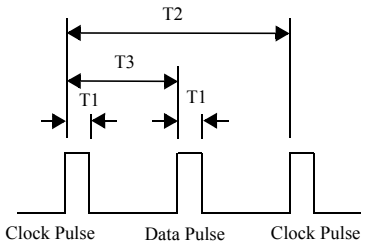


Figure 28–5—FLP Burst pulse-to-pulse timing

The first link pulse in consecutive FLP Bursts shall occur at a 16 ± 8 ms interval (Figure 28–6).

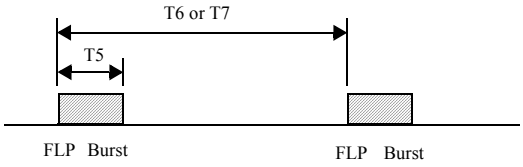


Figure 28–6—FLP Burst to FLP Burst timing

Table 28–1—FLP Burst timing summary

#	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–12)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	µs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs
T4	Pulses in a Burst	17		97	#

Table 28–1—FLP Burst timing summary *(continued)*

#	Parameter	Min.	Typ.	Max.	Units
T5	Burst Width		2		ms
T6	FLP Burst to FLP Burst	8	16	24	ms
T7	Optimized FLP Burst to FLP Burst	8		8.5	ms

28.2.1.2 Link Code Word encoding

The base Link Code Word (base page) transmitted within an FLP Burst shall convey the encoding shown in Figure 28–7. The Auto-Negotiation function may support additional pages using the Next Page function. Encodings for the Link Code Word(s) used in Next Page exchange are defined in 28.2.3.4. In an FLP Burst, D0 shall be the first bit transmitted.

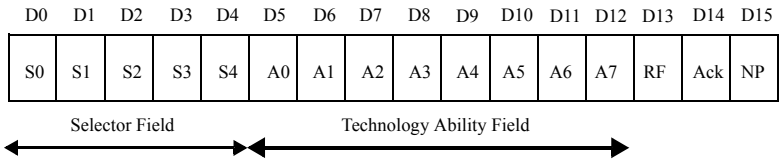


Figure 28–7—Base page encoding

28.2.1.2.1 Selector Field

Selector Field (S[4:0]) is a five bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector Field shall not be transmitted.

28.2.1.2.2 Technology Ability Field

Technology Ability Field (A[7:0]) is an eight bit wide field containing information indicating supported technologies specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector is described in Annex 28B.2 and in Annex 28D. Multiple technologies may be advertised in the Link Code Word. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a Link Partner and to resolve multiple common modes.

NOTE—While devices using a Selector Field value other than the IEEE 802.3 Selector Field value are free to define the Technology Ability Field bits, it is recommended that the 10BASE-T bit be encoded in the same bit position as in the IEEE 802.3 selector. A common bit position can be important if the technology using the other selector will ever coexist on a device that also offers a 10BASE-T mode.

28.2.1.2.3 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base Link Code Word. The default value is logic zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the Auto-Negotiation advertisement register (Register 4) is set to logic one, the RF bit in the transmitted base Link Code Word is set to logic one. When the RF bit in the received base Link Code

Word is set to logic one, the Remote Fault bit in the MII status register (Register 1) will be set to logic one, if the MII management function is present.

The Remote Fault bit shall be used in accordance with the Remote Fault function specifications (28.2.3.5).

28.2.1.2.4 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. The Acknowledge Bit is encoded in bit D14 regardless of the value of the Selector Field or Link Code Word encoding. If no Next Page information is to be sent, this bit shall be set to logic one in the Link Code Word after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logic one after the device has successfully received at least three consecutive and matching FLP Bursts (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the Auto-Negotiation Next Page transmit register (Register 7). In order to save the current received Link Code Word, it must be read from the Auto-Negotiation link partner ability register (Register 6) before the Next Page of transmit information is loaded into the Auto-Negotiation Next Page transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the Link Code Word shall be transmitted six to eight (inclusive) times.

28.2.1.2.5 Next Page

Next Page (NP) is encoded in bit D15 regardless of the Selector Field value or Link Code Word encoding. Support for transmission and reception of additional Link Code Word encodings is optional. If Next Page ability is not supported, the NP bit shall always be set to logic zero. If a device implements Next Page ability and wishes to engage in Next Page exchange, it shall set the NP bit to logic one. A device may implement Next Page ability and choose not to engage in Next Page exchange by setting the NP bit to a logic zero. The Next Page function is defined in 28.2.3.4.

28.2.1.3 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PMA to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Transmit Switch function shall connect only the FLP Burst generator controlled by the Transmit State Diagram, Figure 28–15, to the MDI.

When a PMA is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

28.2.2 Receive function requirements

The Receive function detects the NLP sequence using the NLP Receive Link Integrity Test function of Figure 28–18. The NLP Receive Link Integrity Test function will not detect link pass based on carrier sense.

The Receive function detects the FLP Burst sequence, decodes the information contained within, and stores the data in rx_link_code_word[16:1]. The Receive function incorporates a receive switch to control connection to the 100BASE-TX or 100BASE-T4 PMAs in addition to the NLP Receive Link Integrity Test function, excluding the 10BASE-T Link Integrity Test function present in a 10BASE-T PMA. If Auto-Negotiation detects link_status=READY from any of the technology-dependent PMAs prior to FLP Burst detection, the autoneg_wait_timer (28.3.2) is started. If any other technology-dependent PMA indicates link_status=READY when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the Link Partner using the base page and will flag this in the Local Device by setting the Parallel Detection Fault bit (6.4) in the Auto-Negotiation expansion

register. If a 10BASE-T PMA exists above the Auto-Negotiation function, it is not permitted to receive MDI activity in parallel with the NLP Receive Link Integrity Test function or any other technology-dependent function.

28.2.2.1 FLP Burst ability detection and decoding

In Figures 28–8 to 28–10, the symbol "t_0=0" indicates the event that caused the timers described to start, and all subsequent times given are referenced from that point. All timers referenced shall expire within the range specified in Table 28–9 in 28.3.2.

The Receive function shall identify the Link Partner as Auto-Negotiation able if it receives 6 to 17 (inclusive) consecutive link pulses that are separated by at least flp_test_min_timer time (5–25 µs) but less than flp_test_max_timer time (165–185 µs) as shown in Figure 28–8. The information contained in the FLP Burst that identifies the Link Partner as Auto-Negotiation able shall not be passed to the Arbitration function if the FLP Burst is not complete. The Receive function may use the FLP Burst that identifies the Link Partner as Auto-Negotiation able for ability matching if the FLP Burst is complete. However, it is not required to use this FLP Burst for any purpose other than identification of the Link Partner as Auto-Negotiation able. Implementations may ignore multiple FLP Bursts before identifying the Link Partner as Auto-Negotiation able to allow for potential receive equalization time.

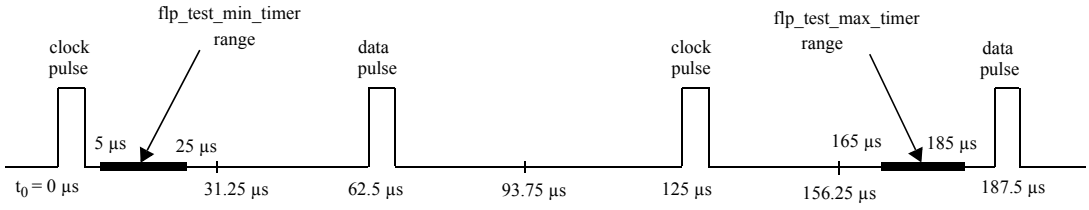


Figure 28–8—FLP detect timers (flp_test_min/max_timers)

The Receive function captures and decodes link pulses received in FLP Bursts. The first link pulse in an FLP Burst shall be interpreted as a clock link pulse. Detection of a clock link pulse shall restart the data_detect_min_timer and data_detect_max timer. The data_detect_min/max_timers enable the receiver to distinguish data pulses from clock pulses and logic one data from logic zero data, as follows:

a) If, during an FLP Burst, a link pulse is received when the data_detect_min_timer has expired while the data_detect_max_timer has not expired, the data bit shall be interpreted as a logic one (Figure 28–9).
b) If, during an FLP Burst, a link pulse is received after the data_detect_max_timer has expired, the data bit shall be interpreted as a logic zero (Figure 28–9) and that link pulse shall be interpreted as a clock link pulse.

As each data bit is identified it is stored in the appropriate rx_link_code_word[16:1] element.

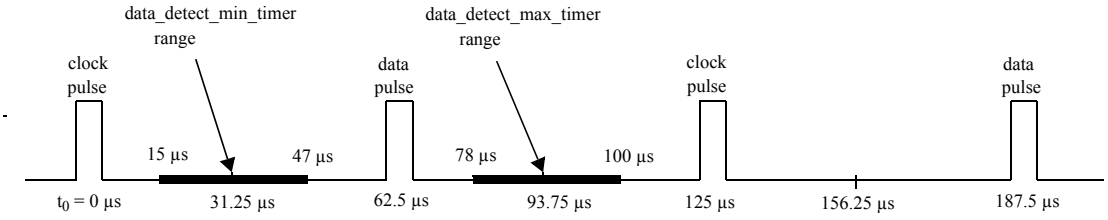
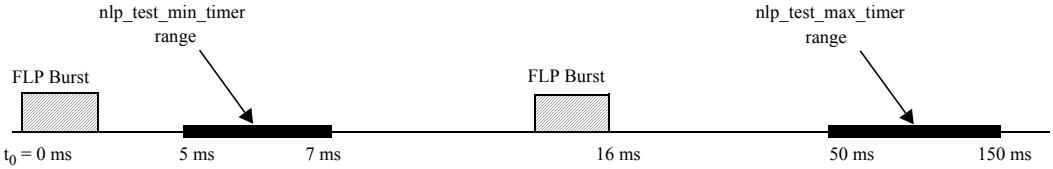


Figure 28–9—FLP data detect timers (data_detect_min/max_timers)

FLP Bursts conforming to the nlp_test_min_timer and nlp_test_max_timer timing as shown in Figure 28–10 shall be considered to have valid separation.



NOTE—The reference for the starting of the nlp_test_min_timer is from the beginning of the FLP Burst, as shown by t_0, while the reference for the starting of the nlp_test_max_timer is from the expiration of the nlp_test_min_timer.

Figure 28–10—FLP Burst timer (nlp_test_min/max_timers)

28.2.2.2 NLP detection

NLP detection is accomplished via the NLP Receive Link Integrity Test function in Figure 28–18. The NLP Receive Link Integrity Test function is a modification of the original 10BASE-T Link Integrity Test function (Figure 14–6), where the detection of receive activity will not cause a transition to the LINK TEST PASS state during Auto-Negotiation. The NLP Receive Link Integrity Test function also incorporates the Technology-Dependent Interface requirements.

28.2.2.3 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PMA once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Receive Switch function shall connect both the FLP Burst receiver controlled by the Receive state diagram, Figure 28–16, and the NLP Receive Link Integrity Test state diagram, Figure 28–18, to the MDI. During Auto-Negotiation, the Receive Switch function shall also connect the 100BASE-TX and 100BASE-T4 PMA receivers to the MDI if the 100BASE-TX and/or 100BASE-T4 PMAs are present.

When a PMA is connected to the MDI through the Receive Switch function, the signals at the PMA shall conform to all of the PHY's specifications.

28.2.2.4 Link Code Word matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in 28.3.1.

28.2.3 Arbitration function requirements

The Arbitration function ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgment, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PMA via the Technology-Dependent Interface (28.2.6).

28.2.3.1 Parallel detection function

The Local Device detects a Link Partner that supports Auto-Negotiation by FLP Burst detection. The Parallel Detection function allows detection of Link Partners that support 100BASE-TX, 100BASE-T4, and/or

10BASE-T, but do not support Auto-Negotiation. Prior to detection of FLP Bursts, the Receive Switch shall direct MDI receive activity to the NLP Receive Link Integrity Test state diagram, 100BASE-TX and 100BASE-T4 PMAs, if present, but shall not direct MDI receive activity to the 10BASE-T or any other PMA. If at least one of the 100BASE-TX, 100BASE-T4, or NLP Receive Link Integrity Test functions establishes link_status=READY, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=READY indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PMA indicating link_status=READY. If a PMA is enabled, the Arbitration function shall set link_control=DISABLE to all other PMAs and indicate that Auto-Negotiation has completed. On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the link partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function.

NOTE 1—Native 10BASE-T devices will be detected by the NLP Receive Link Integrity Test function, an integrated part of the Auto-Negotiation function. Hence, Parallel Detection for the 10BASE-T PMA is not required or allowed.

NOTE 2—When selecting the highest common denominator through the Parallel Detection function, only the half-duplex mode corresponding to the selected PMA may automatically be detected.

28.2.3.2 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PMAs and halt any transmit data and link pulse activity until the break_link_timer expires (28.3.2). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The Local Device shall resume Auto-Negotiation after the break_link_timer has expired by issuing FLP Bursts with the base page valid in tx_link_code_word[16:1].

Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PMA an opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PMA still indicates link_status=FAIL or link_status=READY.

28.2.3.3 Priority Resolution function

Since a Local Device and a Link Partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PMA enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the Local Device and Link Partner that has the highest priority as defined in Annex 28B. This technology is referred to as the Highest Common Denominator, or HCD, technology. If the Local Device receives a Technology Ability Field with a bit set that is reserved, the Local Device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the FLP LINK GOOD CHECK state. In the event that a technology is chosen through the Parallel Detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of “NULL,” indicating that no PMA receives link_control=ENABLE, and link_status_[HCD]=FAIL.

28.2.3.4 Next Page function

The Next Page function uses the standard Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data. Data is carried by optional Next Pages of information, which follow the transmission and acknowledgment procedures used for the base Link Code Word. Two types of Next Page encodings are defined: Message Pages and Unformatted Pages.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

Next Page operation is controlled by the same two mandatory control bits, Next Page and Acknowledge, used in the Base Link Code Word. Setting the NP bit in the Base Link Code Word to logic one indicates that the device is Next Page Able. If both a device and its Link Partner are Next Page Able, then Next Page exchange may occur. If one or both devices are not Next Page Able, then Next Page exchange will not occur and, after the base Link Code Words have been exchanged, the FLP LINK GOOD CHECK state will be entered. The Toggle bit is used to ensure proper synchronization between the Local Device and the Link Partner.

Next Page exchange occurs after the base Link Code Words have been exchanged. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages. Two message encodings are defined: Message Pages, which contain predefined 11 bit codes, and Unformatted Pages. Unformatted Pages can be combined to send extended messages. If the Selector Field values do not match, then each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be interpreted. If the Selector Field values match, then the convention governing the use of Message Pages shall be as defined by the Selector Field value definition. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Message Pages with Null message codes and the NP bit set to logic zero while its Link Partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages with Null message codes as the end of its Link Partner's Next Page information.

28.2.3.4.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 28–11 and Figure 28–12 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10–D0 shall be encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero.

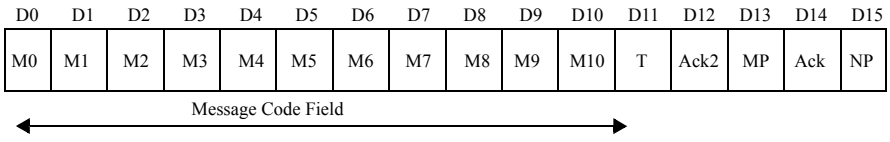


Figure 28–11—Message Page encoding

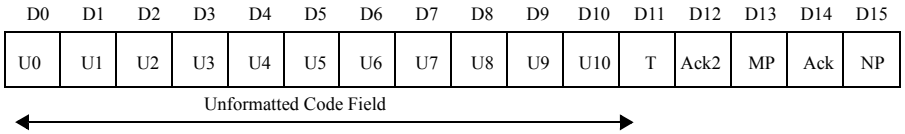


Figure 28–12—Unformatted Page encoding

28.2.3.4.2 Extended Next Page encodings

Extended Next Pages shall use the encoding shown in Figure 28-13 #CrossRef# for the message code field, flags field, and unformatted code field. The Message Code Field contains the 11-bit Message Code value. The 5-bit flags field contains the NP, Ack, MP, Ack2, and T bits. The Unformatted Code Field contains a 32-bit value..

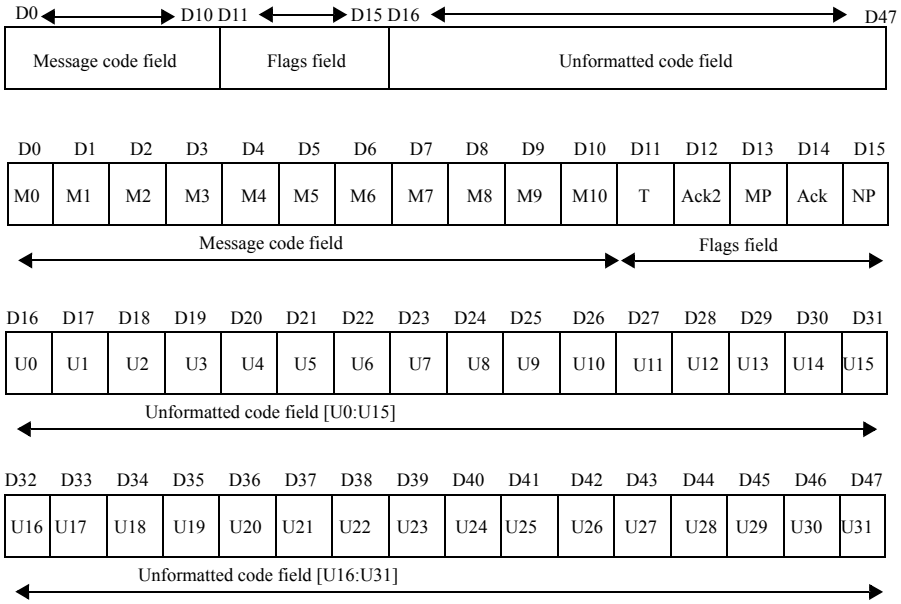


Figure 28–13—Extended Next Page Encoding

28.2.3.4.3 Next Page

Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows:

logic zero = last page.
logic one = additional Next Page(s) will follow.

28.2.3.4.4 Acknowledge

As defined in 28.2.1.2.4.

28.2.3.4.5 Message Page

Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

28.2.3.4.6 Acknowledge 2

Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = cannot comply with message.
logic one = will comply with message.

28.2.3.4.7 Toggle

Toggle (T) is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows:

logic zero = previous value of the transmitted Link Code Word equalled logic one.
logic one = previous value of the transmitted Link Code Word equalled logic zero.

28.2.3.4.8 Message Page encoding

Message Pages are formatted pages that carry a single predefined Message Code, which is enumerated in Annex 28C. Two-thousand and forty-eight Message Codes are available. The allocation of these codes will be controlled by the contents of Annex 28C. If the Message Page bit is set to logic one, then the bit encoding of the Link Code Word shall be interpreted as a Message Page.

28.2.3.4.9 Message Code Field

Message Code Field (M[10:0]) is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

28.2.3.4.10 Unformatted Page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining 11 bits may take on an arbitrary value. If the Message Page bit is set to logic zero, then the bit encoding of the Link Code Word shall be interpreted as an Unformatted Page.

28.2.3.4.11 Unformatted Code Field

Unformatted Code Field (U[10:0]) is an eleven bit wide field, which may contain an arbitrary value.

28.2.3.4.12 Extended Next Page encoding

Extended Next Pages carry a single predefined Message Code (M[10:0]), which is enumerated in Annex 28C #CrossRef#, and a single 32-bit Unformatted Code ([U31:0]), which may contain an arbitrary value.

28.2.3.4.13 Use of Next Pages

a) Both devices must indicate Next Page ability for either to commence exchange of Next Pages.
b) If both devices are Next Page able, then both devices shall send at least one Next Page.
c) Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.
d) A Message Code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted.
e) If a Message Code references Unformatted Pages, the Unformatted Pages shall immediately follow the referencing Message Code in the order specified by the Message Code.

f) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.
g) TBD

28.2.3.4.14 MII register requirements

The Next Page Transmit register defined in 28.2.4.1.6 shall hold the Next Page to be sent by Auto-Negotiation. Received Next Pages may be stored in the Auto-Negotiation link partner ability register.

28.2.3.5 Remote fault sensing function

The Remote Fault function may indicate to the Link Partner that a fault condition has occurred using the Remote Fault bit and, optionally, the Next Page function.

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault bit shall be optional. If the Local Device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault bit indication, then it shall transmit the Remote Fault bit with the value contained in the Auto-Negotiation advertisement register bit (4.13).

A Local Device may indicate it has sensed a fault to its Link Partner by setting the Remote Fault bit in the Auto-Negotiation advertisement register and renegotiating.

If the Local Device sets the Remote Fault bit to logic one, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes have been specified for this purpose.

The Remote Fault bit shall remain set until after successful negotiation with the base Link Code Word, at which time the Remote Fault bit shall be reset to a logic zero. On receipt of a base Link Code Word with the Remote Fault bit set to logic one, the device shall set the Remote Fault bit in the MII status register (1.4) to logic one if the MII management function is present.

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.

28.2.4.1 Media Independent Interface

The Auto-Negotiation function shall have five dedicated registers:

a) MII control register (Register 0).
b) MII status register (Register 1).
c) Auto-Negotiation advertisement register (Register 4).
d) Auto-Negotiation link partner ability register (Register 5).
e) Auto-Negotiation expansion register (Register 6).

If the Next Page function is implemented, the Auto-Negotiation next page transmit register (Register 7) shall be implemented.

28.2.4.1.1 MII control register

MII control register (Register 0) provides the mechanism to disable/enable and/or restart Auto-Negotiation. The definition for this register is provided in 28.2.4.1.

The Auto-Negotiation function shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13 and 0.8 shall have no effect on the link configuration, and the Auto-Negotiation process will determine the link configuration. If bit 0.12 is cleared to logic zero, then bits 0.13 and 0.8 will determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

A PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall be initiated by setting bit 0.9 to a logic one. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, then this bit will have no meaning, and should be written as zero. This bit is self-clearing. The Auto-Negotiation process shall not be affected by clearing this bit to logic zero.

28.2.4.1.2 MII status register

The MII status register (Register 1) includes information about all modes of operations supported by the Local Device's PHY, the status of Auto-Negotiation, and whether the Auto-Negotiation function is supported by the PHY or not. The definition for this register is provided in 28.2.4.2.

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of Registers 4, 5, and 6 are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of Registers 4, 5, and 6 are meaningless. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

When read as logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

When read as a one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

28.2.4.1.3 Auto-Negotiation advertisement register (Register 4) (R/W)

This register contains the Advertised Ability of the PHY. (See Table 28–2). The bit definition for the base page is defined in 28.2.1.2. On power-up, before Auto-Negotiation starts, this register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4.12:5) is set based on the values set in the MII status register (Register 1) (1.15:11) or equivalent. See also Annex 28D.

Only the bits in the Technology Ability Field that represent the technologies supported by the Local Device may be set. Any of the Technology Ability Field bits that may be set can also be cleared by management before a renegotiation. This can be used to enable management to Auto-Negotiate to an alternate common mode.

The management entity may initiate renegotiation with the Link Partner using alternate abilities by setting the Selector Field (4.4:0) and Technology Ability Field (4.12:5) to indicate the preferred mode of operation and setting the Restart Auto-Negotiation bit (0.9) in the control register (Register 0) to logic one.

Table 28–2—Advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

Any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a renegotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be examined by software to determine the highest common denominator technology.

28.2.4.1.4 Auto-Negotiation link partner ability register (Register 5) (RO)

All of the bits in the Auto-Negotiation link partner ability register are read only. A write to the Auto-Negotiation link partner ability register shall have no effect.

This register contains the Advertised Ability of the Link Partner's PHY. (See Tables 28–3 and 28–4.) The bit definitions shall be a direct representation of the received Link Code Word (Figure 28–7). Upon successful completion of Auto-Negotiation, status register (Register 1) Auto-Negotiation Complete bit (1.5) shall be set to logic one. If the Next Page function is supported, the Auto-Negotiation link partner ability register may be used to store Link Partner Next Pages.

Table 28–3—Link partner ability register bit definitions (Base Page)

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

Table 28–4—Link partner ability register bit definitions (Next Page)

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.3.4	RO
5.14	Acknowledge	See 28.2.3.4	RO
5.13	Message Page	See 28.2.3.4	RO

Table 28–4—Link partner ability register bit definitions (Next Page) *(continued)*

Bit(s)	Name	Description	R/W
5.12	Acknowledge 2	See 28.2.3.4	RO
5.11	Toggle	See 28.2.3.4	RO
5.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

The values contained in this register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or, if used with Next Page exchange, after the Page Received bit (6.1) has been set to logic one.

NOTE—If this register is used to store Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

28.2.4.1.5 Auto-Negotiation expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register shall have no effect. (See Table 28–5.)

Table 28–5—Expansion register bit definitions

Bit(s)	Name	Description	R/W	Default
6.15:5	Reserved	Write as zero, ignore on read	RO	0
6.4	Parallel Detection Fault	1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able	RO	0
6.2	Next Page Able	1 = Local Device is Next Page able 0 = Local Device is not Next Page able	RO	0
6.1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able	RO	0

Bits 6.15:5 are reserved for future Auto-Negotiation expansion.

The Parallel Detection Fault bit (6.4) shall be set to logic one to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires. The Parallel Detection Fault bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

The Link Partner Next Page Able bit (6.3) shall be set to logic one to indicate that the Link Partner supports the Next Page function. This bit shall be reset to logic zero to indicate that the Link Partner does not support the Next Page function.

The Next Page Able bit (6.2) shall be set to logic one to indicate that the Local Device supports the Next Page function. The Next Page Able bit (6.2) shall be set to logic zero if the Next Page function is not supported.

The Page Received bit (6.1) shall be set to logic one to indicate that a new Link Code Word has been received and stored in the Auto-Negotiation link partner ability register. The Page Received bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

The Link Partner Auto-Negotiation Able bit (6.0) shall be set to logic one to indicate that the Link Partner is able to participate in the Auto-Negotiation function. This bit shall be reset to logic zero if the Link Partner is not Auto-Negotiation able.

28.2.4.1.6 Auto-Negotiation Next Page transmit register (Register 7) (R/W)

The Auto-Negotiation Next Page Transmit register contains the Next Page Link Code Word to be transmitted when Next Page ability is supported. (See Table 28–6.) The contents are defined in 28.2.3.4. On power-up, this register shall contain the default value of 2001H, which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid Next Page Message Code that the device wishes to transmit. Writing to this register shall set mr_next_page_loaded to true.

Table 28–6—Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0, ignore on read	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code field	See 28.2.3.4	R/W

28.2.4.1.7 Auto-Negotiation Link Partner Ability register (Register 8) (RO)

Support for 100BASE-T2 and 1000BASE-T requires support for Next Page and the provision of an Auto-Negotiation Link Partner Next Page Ability register (register 8) to store Link Partner Next Pages as shown in Table 28–7. All of the bits in the Auto-Negotiation Link Partner Next Page Ability register are read only. A write to the Auto-Negotiation Link Partner Next Page Ability register shall have no effect.

The values contained in this register are only guaranteed to be valid after the Page Received bit (6.1) has been set to logical one or once Auto-Negotiation has successfully completed, as indicated by bit 1.5.

NOTE—If this register is used to store multiple Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

Table 28–7—Link Partner Next Page Ability register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	see 28.2.3.4	RO
8.14	Acknowledge	see 28.2.3.4	RO
8.13	Message Page	see 28.2.3.4	RO
8.12	Acknowledge 2	see 28.2.3.4	RO
8.11	Toggle	see 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	see 28.2.3.4	RO

28.2.4.1.8 State diagram variable to MII register mapping

The state diagrams of Figures 28–15 to 28–18 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface that may be connected to the MII management function or other equivalent function. Table 28–8 describes how the MII registers map to the management function interface signals.

Table 28–8—State diagram variable to MII register mapping

State diagram variable	MII register
mr_adv_ability[16:1]	4.15:0 Auto-Negotiation advertisement register
mr_autoneg_complete	1.5 Auto-Negotiation Complete
mr_autoneg_enable	0.12 Auto-Negotiation Enable
mr_lp_adv_ability[16:1]	5.15:0 Auto-Negotiation link partner ability register
mr_lp_autoneg_able	6.0 Link Partner Auto-Negotiation Able
mr_lp_np_able	6.3 Link Partner Next Page Able
mr_main_reset	0.15 Reset
mr_next_page_loaded	Set on write to Auto-Negotiation Next Page Transmit register; cleared by Arbitration state diagram
mr_np_able	6.2 Next Page Able
mr_np_tx[16:1]	7.15:0 Auto-Negotiation Next Page Transmit Register
mr_page_rx	6.1 Page Received
mr_parallel_detection_fault	6.4 Parallel Detection Fault
mr_restart_negotiation	0.9 Auto-Negotiation Restart
set if Auto-Negotiation is available	1.3 Auto-Negotiation Ability

28.2.4.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

28.2.5 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability[16:1]. A device shall comply with all Next Page function requirements, including the provision of the mr_np_able, mr_lp_np_able, and mr_next_page_loaded variables (or their logical equivalents), in order to permit the NP bit to be set to logic one in the transmitted Link Code Word.

NOTE—Storage of a valid base Link Code Word is required to prevent a deadlock situation where negotiation must start again while Next Pages are being transmitted. If a shared transmit register were used, then renegotiation could not occur when Next Pages were being transmitted because the base Link Code Word would not be available. This requirement can be met using a number of different implementations, including use of temporary registers or register stacks.

28.2.6 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

28.2.6.1 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS, repeater client, or Auto-Negotiation function a means of determining the validity of received code elements.

28.2.6.1.1 Semantics of the service primitive

PMA_LINK.indicate(link_status)

The link_status parameter shall assume one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled (READY), intact and enabled (OK), or not intact (FAIL). When link_status=FAIL or link_status=READY, the PMA_CARRIER.indicate and PMA_UNITDATA.indicate primitives are undefined.

28.2.6.1.2 When generated

A technology-dependent PMA and the NLP Receive Link Integrity Test state diagram (Figure 28–18) shall generate this primitive to indicate the value of link_status.

28.2.6.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagrams of Figure 28–17.

28.2.6.2 PMA_LINK.request

This primitive is generated by Auto-Negotiation to allow it to enable and disable operation of the PMA.

28.2.6.2.1 Semantics of the service primitive

PMA_LINK.request(link_control)

The link_control parameter shall assume one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

The link_control=SCAN_FOR_CARRIER mode is used by the Auto-Negotiation function prior to receiving any FLP Bursts or link_status=READY indications. During this mode, the PMA shall search for carrier and report link_status=READY when carrier is received, but no other actions shall be enabled.

The link_control=DISABLE mode shall be used by the Auto-Negotiation function to disable PMA processing.

The link_control=ENABLE mode shall be used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions.

28.2.6.2.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagrams of Figure 28–16 and Figure 28–17.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINK.request(DISABLE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINK.request(link_control) is implementation dependent.

28.2.6.2.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the NLP Receive Link Integrity Test state diagram (Figure 28–18) and the receiving technology-dependent link integrity test function, based on the intent specified in the primitive semantics.

28.2.6.3 PMA_LINKPULSE.request

This primitive is generated by Auto-Negotiation to indicate that a valid Link Pulse, as transmitted in compliance with Figure 14–12, has been received.

28.2.6.3.1 Semantics of the service primitive

PMA_LINKPULSE.request (linkpulse)

The linkpulse parameter shall assume one of two values: TRUE or FALSE.

The linkpulse=FALSE mode shall be used by the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.

The linkpulse=TRUE mode shall be used by the Auto-Negotiation function to indicate that a valid Link Pulse has been received.

28.2.6.3.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–16.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request (FALSE) message shall be issued to all technology-dependent PMAs. If Auto-

Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINKPULSE.request (linkpulse) is implementation dependent.

28.2.6.3.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.3 State diagrams and variable definitions

The notation used in the state diagrams (Figures 28–15 to 28–18) follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the "mr_x" notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the MII interface are covered in 28.2.4 and 22.2.4. The variables, timers, and counters used in the state diagrams are defined in 28.3, 14.2.3, and 28.2.6.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram, Arbitration state diagram, and NLP Receive Link Integrity Test state diagram as depicted in 28.3. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

The functional reference diagram (Figure 28–14) provides a generic example, illustrated with initial PMA implementations and showing the mechanism for expansion. New PMAs are documented in Annex 28D.

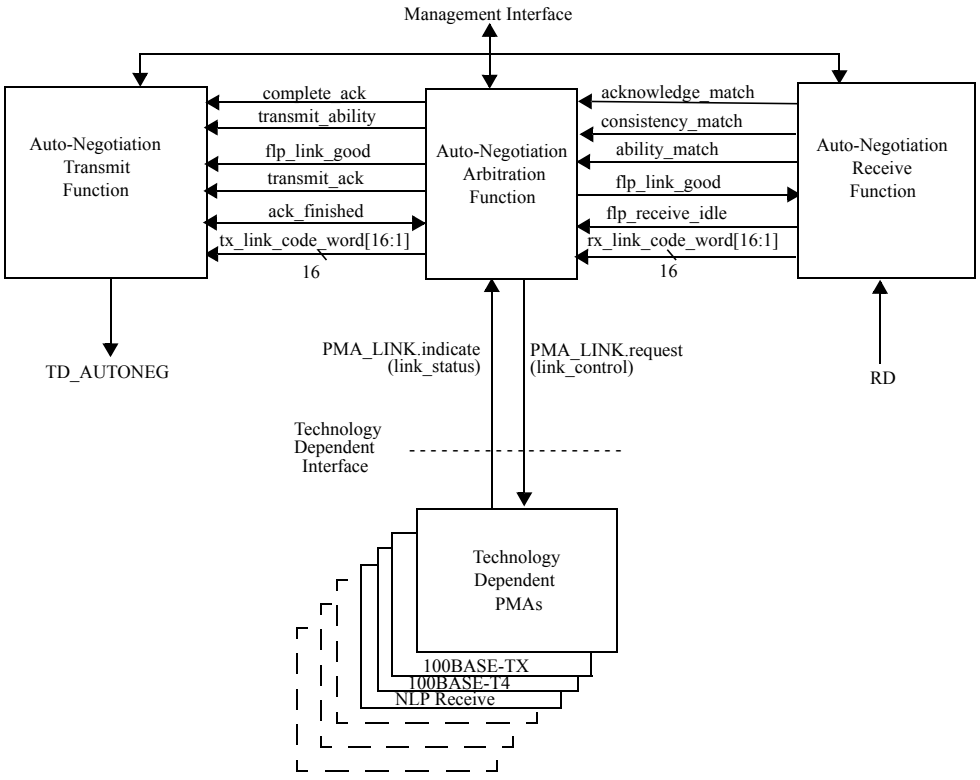


Figure 28–14—Functional reference diagram

28.3.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all;	represents all specific technology-dependent PMAs supported in the Local Device and the NLP Receive Link Integrity Test state diagram.
1GigT;	represents that the 1000BASE-T PMA is the signal source.
HCD;	represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function. To select 10BASE-T, LIT is used instead of NLP to enable the full 10BASE-T Link Integrity Test function state diagram.
notHCD;	represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function.
TX;	represents that the 100BASE-TX PMA is the signal source.
T4;	represents that the 100BASE-T4 PMA is the signal source.
NLP;	represents that the NLP Receive Link Integrity Test function is the signal source.
PD;	represents all of the following that are present: 100BASE-TX PMA, 100BASE-T4 PMA, and the NLP Receive Link Integrity Test state diagram.
LIT;	represents the 10BASE-T Link Integrity Test function state diagram is the signal source or destination.

Variables with [16:1] appended to the end of the variable name indicate arrays that can be directly mapped to 16-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

— Any integer.
— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bit.

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the MII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive Link Code Words match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive Link Code Words have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive Link Code Words have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [16:1]

A 16-bit array that contains the last Link Code Word that caused ability_match = true. For each element in the array:

Values: zero; data bit is logicial zero.
one; data bit is logical one.

ack_finished

Status indicating that the final remaining_ack_cnt Link Code Words with the Ack bit set have been transmitted.

Values: false; more Link Code Words with the Ack bit set to logic one must be transmitted.
true; all remaining Link Code Words with the Ack bit set to logic one have been transmitted.

acknowledge_match

Indicates that three consecutive Link Code Words match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive Link Code Words have not been received with the Acknowledge bit set (default).
true; three matching and consecutive Link Code Words have been received with the Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial Link Code Word encoding used to communicate the device's abilities.

Values: false; a page other than base Link Code Word is being transmitted.
true; the base Link Code Word is being transmitted.

complete_ack

Controls the counting of transmitted Link Code Words that have their Acknowledge bit set.

Values: false; transmitted Link Code Words with the Acknowledge bit set are not counted (default).
true; transmitted Link Code Words with the Acknowledge bit set are counted.

consistency_match

Indicates that the Link Code Word that caused ability_match to be set is the same as the Link Code Word that caused acknowledge_match to be set.

Values: false; the Link Code Word that caused ability_match to be set is not the same as the Link Code Word that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
true; the Link Code Word that caused ability_match to be set is the same as the Link Code Word that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

desire_np

Status indicating that the Local Device desires to engage in Next Page exchange. This information comes from the setting of the NP bit in the base Link Code Word stored in the Auto-Negotiation

advertisement register (Register 4).

Values: false; Next Page exchange is not desired.
true; Next Page exchange is desired.

flp_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).
true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

flp_receive_idle

Indicates that the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

Values: false; the Receive state diagram is not in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state (default).
true; the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

incompatible_link

Parameter used following Priority Resolution to indicate the resolved link is incompatible with the Local Device settings. A device's ability to set this variable to true is optional.

Values: false; A compatible link exists between the Local Device and Link Partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control

This variable is defined in 28.2.6.2.1.

link_status

This variable is defined in 28.2.6.1.1.

linkpulse

This variable is defined in 28.2.6.3.1.

Values: false; linkpulse is set to false after any Receive State Diagram state transition (default).
true; linkpulse is set to true when a valid Link Pulse is received.

mr_autoneg_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable

Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[16:1]

A 16-bit array that contains the Advertised Abilities Link Code Word.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_adv_ability[16:1]

A 16-bit array that contains the Link Partner's Advertised Abilities Link Code Word. For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_np_able

Status indicating whether the Link Partner supports Next Page exchange.

Values: false; the Link Partner does not support Next Page exchange.
true; the Link Partner supports Next Page exchange.

mr_np_able

Status indicating whether the Local Device supports Next Page exchange.

Values: false; the Local Device does not support Next Page exchange.
true; the Local Device supports Next Page exchange.

mr_lp_autoneg_able

Status indicating whether the Link Partner supports Auto-Negotiation.

Values: false; the Link Partner does not support Auto-Negotiation.
true; the Link Partner supports Auto-Negotiation.

mr_main_reset

Controls the resetting of the Auto-Negotiation state diagrams.

Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded

Status indicating whether a new page has been loaded into the Auto-Negotiation Next Page Transmit register (Register 7).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[16:1]

A 16-bit array that contains the new Next Page to transmit. For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the Link Code Word has been written to mr_lp_adv_ability[16:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault

Error condition indicating that while performing Parallel Detection, either flp_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the Auto-Negotiaion expansion register.

1) link_status_ [NLP] = READY

2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; Exactly one of the above three indications was true when the autoneg_wait_timer expired, and flp_receive_idle = true.
true; either zero or more than one of the above three indications was true when the autoneg_wait_timer expired, or flp_receive_idle = false.

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values: false; renegotiation is not taking place.
true; renegotiation is started.

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

page_size

Condition indicating the size of Next Page that the device is prepared to transmit and receive.

Values: 16; the device does not support extended Next Pages or is not in the process of transmitting or receiving extended Next Pages(default).
48; the device supports extended Next Pages and is in the process of transmitting or receiving extended Next Pages.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low power mode set via MII control register bit 0.11.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

rx_link_code_word[16:1]

A 16-bit array that contains the data bits to be received from an FLP Burst.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that flp_receive_idle = true and only one the of the following indications is being received:

1) link_status_[NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; either zero or more than one of the above three indications are true or flp_receive_idle = false.
true; Exactly one of the above three indications is true and flp_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: idle; Auto-Negotiation prevents transmission of all link pulses on the MDI.
link_test_pulse; Auto-Negotiation causes a single link pulse as defined by Figure 14–12 to be transmitted on the MDI.

toggle_rx

Flag to keep track of the state of the Link Partner's Toggle bit.

Values: 0; Link Partner's Toggle bit equals logic zero.
1; Link Partner's Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the Local Device's Toggle bit.

Values: 0; Local Device's Toggle bit equals logic zero.
1; Local Device's Toggle bit equals logic one.

transmit_ability

Controls the transmission of the Link Code Word containing tx_link_code_word[16:1].

Values: false; any transmission of tx_link_code_word[16:1] is halted (default).
true; the transmit state diagram begins sending tx_link_code_word[16:1].

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[16:1] to be transmitted.

Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[16:1] to a logic zero (default).
true; sets the Acknowledge bit in the transmitted tx_link_code_word[16:1] to a logic one.

transmit_disable

Controls the transmission of tx_link_code_word[16:1].

Values: false; tx_link_code_word[16:1] transmission is allowed (default).
true; tx_link_code_word[16:1] transmission is halted.

tx_link_code_word[16:1]

A 16-bit array that contains the data bits to be transmitted in an FLP Burst. This array may be loaded from mr_adv_ability or mr_np_tx.
For each element within the array:

Values: Zero; data bit is logical zero.
One; data bit is logical one.

28.3.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer

Timer for the amount of time to wait before evaluating the number of link integrity test functions with link_status=READY asserted. The autoneg_wait_timer shall expire 500–1000 ms from the assertion of link_status=READY from the 100BASE-TX PMA, 100BASE-T4 PMA, or the NLP Receive State diagram.

break_link_timer
: Timer for the amount of time to wait in order to assure that the Link Partner enters a Link Fail state. The timer shall expire 1200–1500 ms after being started.

data_detect_max_timer
: Timer for the maximum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_max_timer shall expire 78–100 μs from the last clock pulse.

data_detect_min_timer
: Timer for the minimum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_min_timer shall expire 15–47 μs from the last clock pulse.

flp_test_max_timer
: Timer for the maximum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_min_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_max_timer shall expire 165–185 μs from the last link pulse.

flp_test_min_timer
: Timer for the minimum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_max_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_min_timer shall expire 5–25 μs from the last link pulse.

interval_timer
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 55.5–-69.5 μs from each clock pulse and data bit.

link_fail_inhibit_timer
: Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750–1000 ms after entering the FLP LINK GOOD CHECK state.

  NOTE—The link_fail_inhibit_timer expiration value must be greater than the time required for the Link Partner to complete Auto-Negotiation after the Local Device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state. The maximum time difference between a Local Device and its Link Partner completing Auto-Negotiation is

  (Maximum FLP Burst to FLP Burst separation) × (Maximum number of FLP Bursts needed to complete acknowledgment) = (24 ms) × (8 bursts) = 192 ms.

  For example, 100BASE-T4 requires approximately 460 ms to enter link_status=OK for a total minimum link_fail_inhibit_timer time of 652 ms. The lower bound for the link_fail_inhibit_timer was chosen to provide adequate margin for the current technologies and any future PMAs.

nlp_test_max_timer
: Timer for the maximum time that no FLP Burst may be seen before forcing the receive state diagram to the IDLE state. The nlp_test_max_timer shall expire 50–150 ms after being started or restarted.

nlp_test_min_timer
: Timer for the minimum time between two consecutive FLP Bursts. The nlp_test_min_timer shall expire 5–7 ms after being started or restarted for devices that do not support extended Next Pages, and shall expire 6.5–7 ms after being started or restarted for devices that do support extended Next Pages.

transmit_link_burst_timer

Timer for the separation of a transmitted FLP Burst from the next FLP Burst. The transmit_link_burst_timer shall expire 5.7-22.3 ms after the last transmitted link pulse in an FLP Burst.

Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
autoneg_wait_timer	500		1000	ms
break_link_timer	1200		1500	ms
data_detect_min_timer	15		47	µs
data_detect_max_timer	78		100	µs
flp_test_min_timer	5		25	µs
flp_test_max_timer	165		185	µs
interval_timer	55.5	62.5	69.5	µs
link_fail_inhibit_timer	750		1000	ms
nlp_test_max_timer	50		150	ms
nlp_test_min_timer	5		7	ms
transmit_link_burst_timer	5.7	14	22.3	ms

28.3.3 State diagram counters

flp_cnt

A counter that may take on integer values from 0 to 17. This counter is used to keep a count of the number of FLPs detected to enable the determination of whether the Link Partner supports Auto-Negotiation.

Values: not_done; 0 to 5 inclusive.
done; 6 to 17 inclusive.
init; counter is reset to zero.

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional Link Code Words with the Acknowledge Bit set to logic one to be sent to ensure that the Link Partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to (page_size+1). This counter is used to keep a count of data bits received from an FLP Burst and to ensure that when erroneous extra pulses are received, the first 16 bits are kept while the rest are ignored. When this variable reaches page_size or (page_size+1), enough data bits have been received. This counter does not increment beyond (page_size+1) and does not return to 0 until it is reinitialized.

Values: not_done; 1 to (page_size-1) inclusive.
done; page_size or (page_size+1)
init; counter is reset to zero.
rx_bit_cnt_check; 10 to 17 inclusive.

tx_bit_cnt

A counter that may take on integer values from 1 to (page_size+1). This counter is used to keep a count of data bits sent within an FLP Burst. When this variable reaches (page_size+1), all data bits have been sent.

Values: not_done; 1 to page_size inclusive.
done; (page_size+1).
init; counter is initialized to 1.

28.3.4 State diagrams

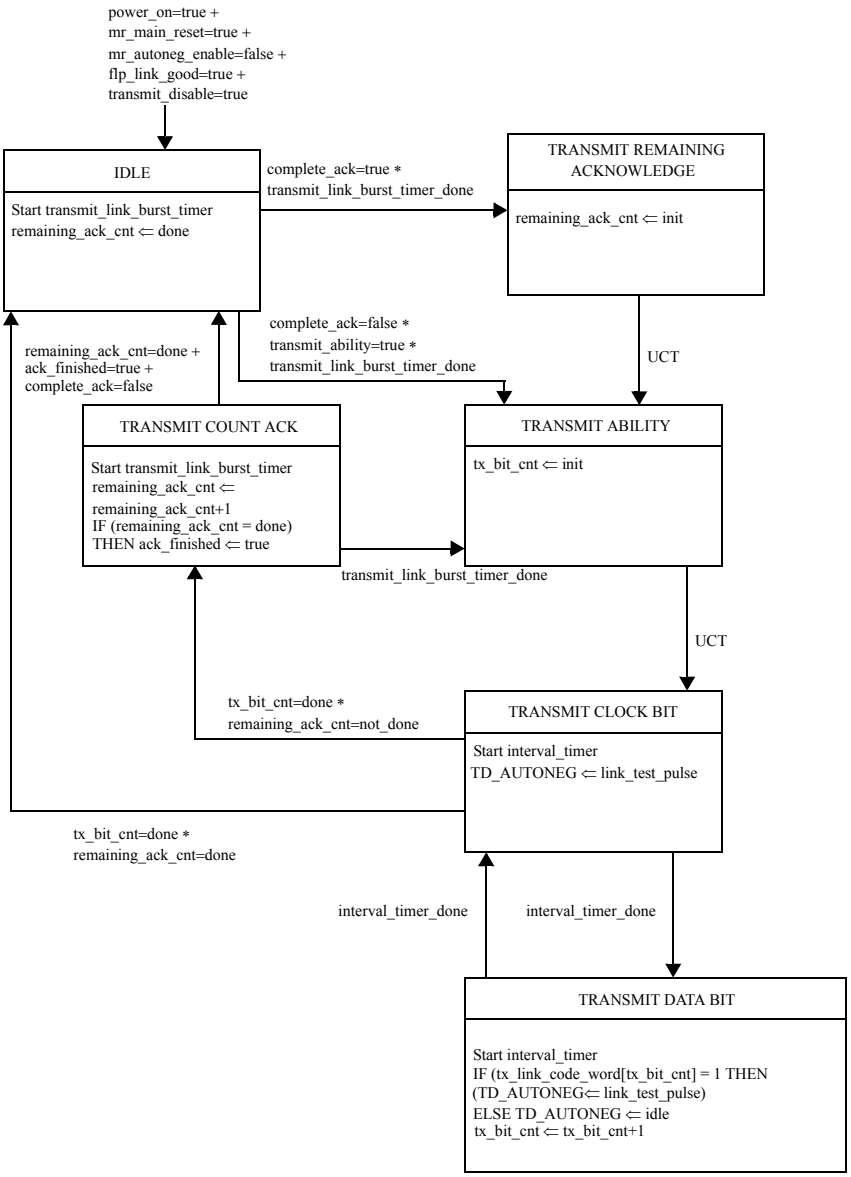


Figure 28–15—Transmit state diagram

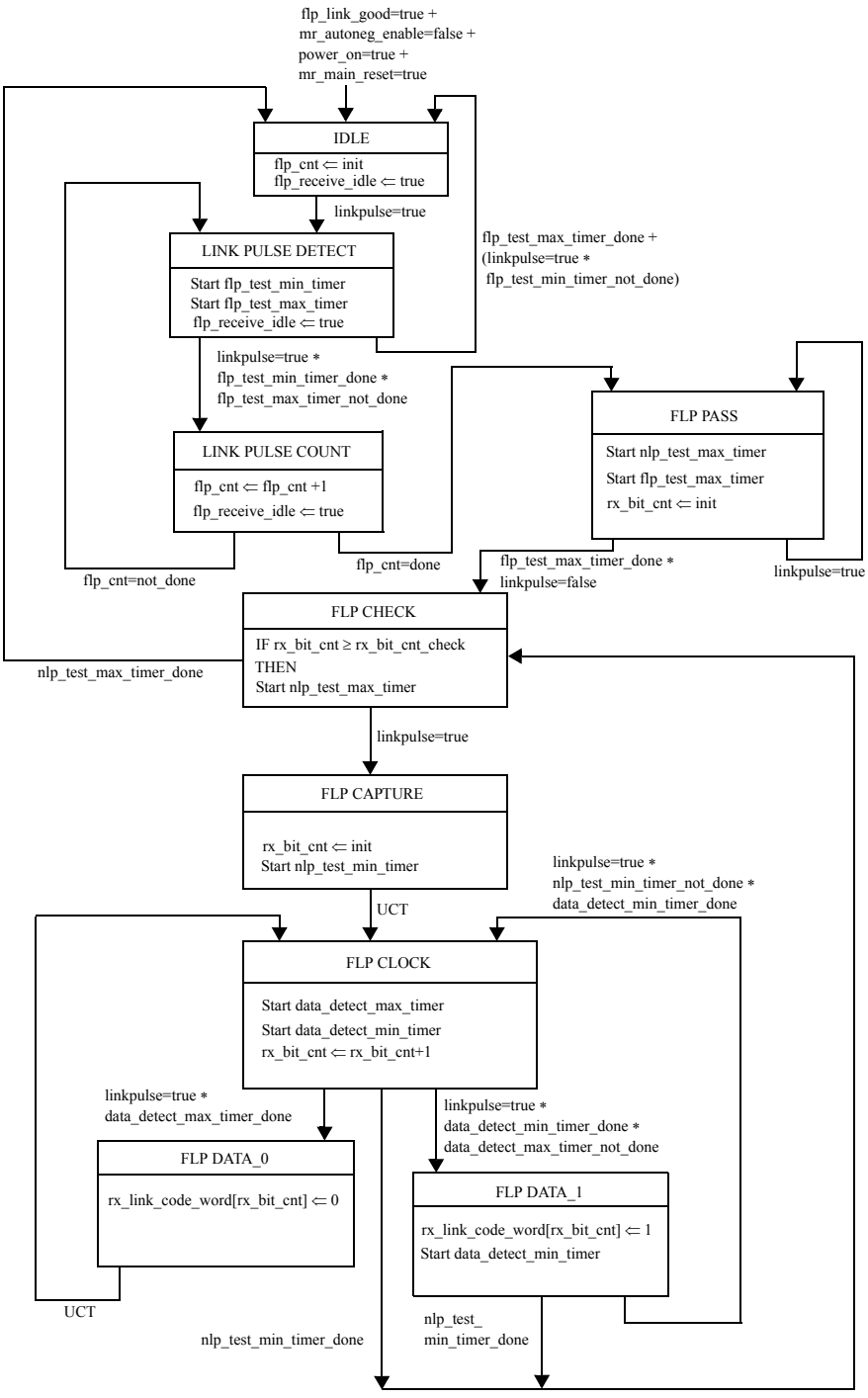
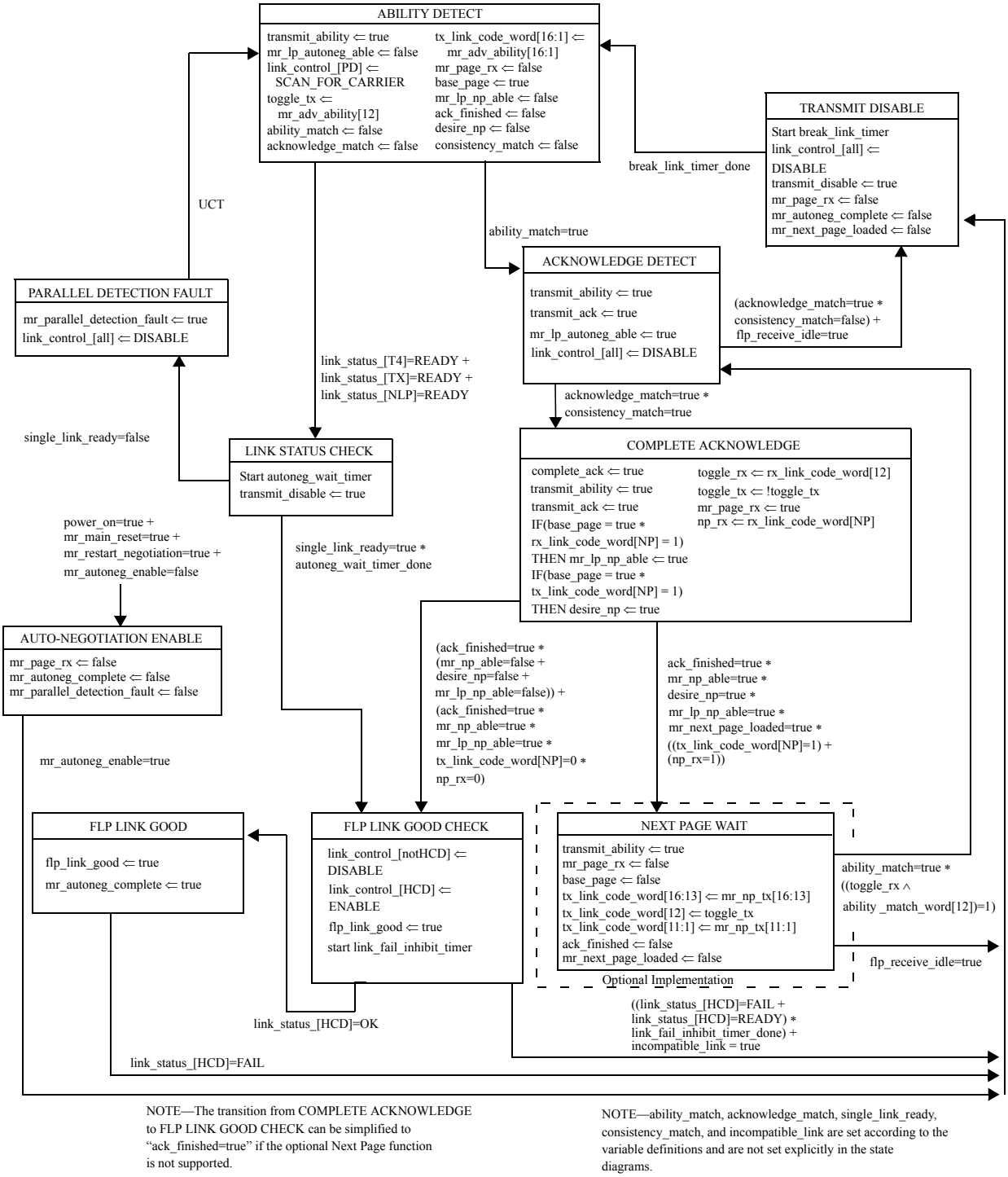


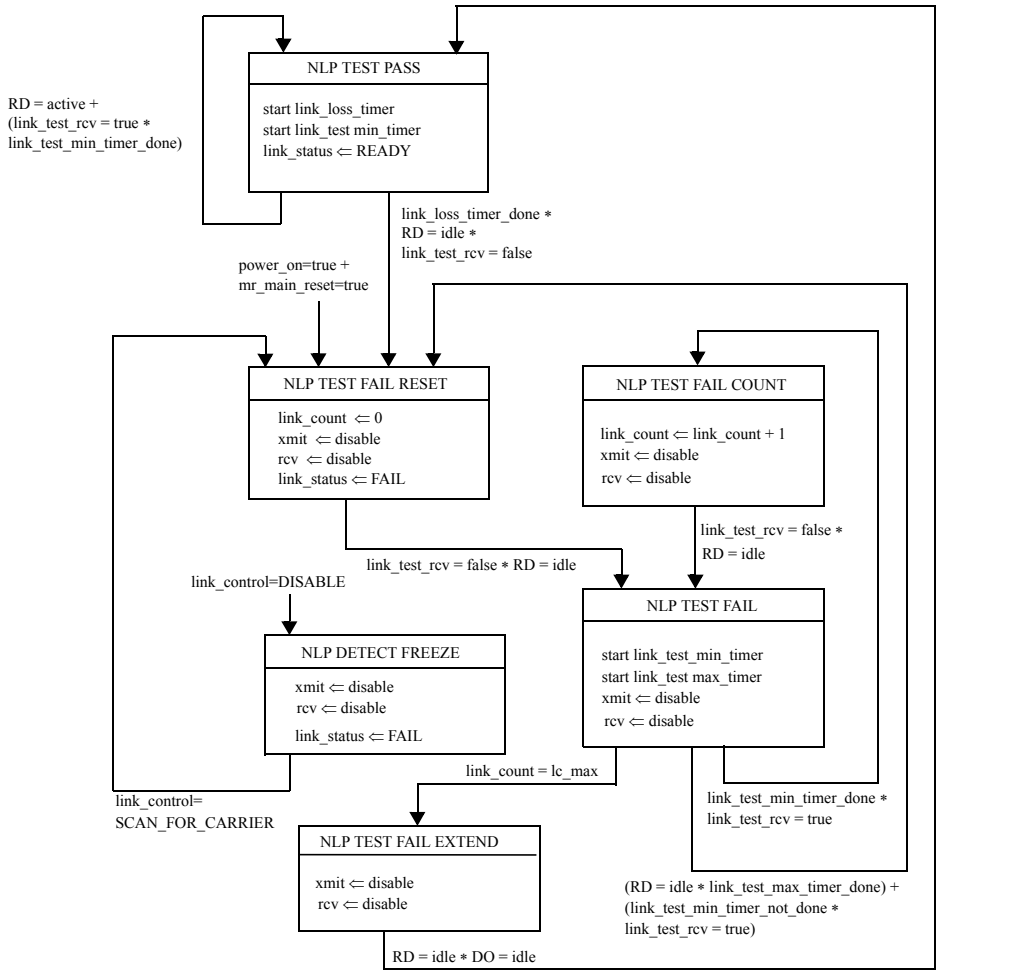
Figure 28–16—Receive state diagram



NOTE—The transition from COMPLETE ACKNOWLEDGE to FLP LINK GOOD CHECK can be simplified to "ack_finished=true" if the optional Next Page function is not supported.

NOTE—ability_match, acknowledge_match, single_link_ready, consistency_match, and incompatible_link are set according to the variable definitions and are not set explicitly in the state diagrams.

Figure 28–17—Arbitration state diagram



NOTE—The variables link_control and link_status are viewed as dedicated signals by the NLP Receive Link integrity Test state diagram, but are viewed as link_control_[NLP] and link_status_[NLP] by the Auto-Negotiation Arbitration state diagram, Figure 28–17.

Figure 28–18—NLP Receive Link Integrity Test state diagram

28.4 Electrical specifications

The electrical characteristics of pulses within FLP Bursts shall be identical to the characteristics of NLPs and shall meet the requirements of Figure 14–12.

It is the responsibility of the technology-specific Transmit and Receive functions to interface to the MDI correctly.

NOTE—The requirements relative to the interface to the MDI are specified via the Transmit Switch and Receive Switch functions.

28.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair[1]

28.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

28.5.2 Identification

28.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

28.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required?No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

28.5.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/comment
10BT	Implementation supports a 10BASE-T data service	28.1.2	O		N/A
*NP	Implementation supports Next Page function	28.1.2	O		N/A
*MII	Implementation supports the MII Management Interface	28.1.2	O/1		N/A
MGMT	Implementation supports a non-MII Management Interface	28.1.2	O/1		N/A
*NOM	Implementation does not support management	28.1.2	O/1		N/A
*RF	Implementation supports Remote Fault Sensing	28.2.3.5	O		N/A

28.5.4 PICS proforma tables for Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

28.5.4.1 Scope

Item	Feature	Subclause	Status	Support	Value/comment
1	MII Management Interface control and status registers	28.1.3	MII:M		Implemented in accordance with the definitions in Clause 22 and 28.2.4
2	CSMA/CD compatible devices using an eight-pin modular connector and using a signaling method to automatically configure the preferred mode of operation	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
3	Device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
4	Future CSMA/CD implementations that use an eight-pin modular connector	28.1.4	M		Interoperable with devices compliant with Clause 28

28.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Status	Support	Value/comment
1	Transmit	28.2	M		Complies with Figure 28–15
2	Receive	28.2	M		Complies with Figure 28–16
3	Arbitration	28.2	M		Complies with Figure 28–17
4	NLP Receive Link Integrity Test	28.2	M		Complies with Figure 28–18
5	Technology-Dependent Interface	28.2	M		Complies with 28.2.6
6	Technology-dependent link integrity test	28.2	M		Implemented and interfaced to for those technologies supported by device
7	Management	28.2	O		MII based or alternate management

28.5.4.3 Transmit function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	FLP Burst transmission	28.2.1.1	M		Not transmitted once Auto-Negotiation is complete and highest common denominator PMA has been enabled. Prohibited other than for link start-up
2	FLP Burst composition	28.2.1.1.1	M		Pulses in FLP Bursts meet the requirements of Figure 14–12
3	FLP Burst pulse definition	28.2.1.1.1	M		17 odd-numbered pulse positions represent clock information; 16 even-numbered pulse positions represent data information
4	The first pulse in an FLP Burst	28.2.1.1.2	M		Defined as a clock pulse for timing purposes
5	FLP Burst clock pulse spacing	28.2.1.1.2	M		Within an FLP Burst, spacing is 125 ± 14 μs
6	Logic one data bit representation	28.2.1.1.2	M		Pulse transmitted 62.5 ± 7 μs after the preceding clock pulse
7	Logic zero data bit representation	28.2.1.1.2	M		No link integrity test pulses within 111 μs of the preceding clock pulse
8	Consecutive FLP Bursts	28.2.1.1.2	M		The first link pulse in each FLP Burst is separated by 16 ± 8 ms
9	FLP Burst base page	28.2.1.2	M		Conforms to Figure 28–7
10	FLP Burst bit transmission order	28.2.1.2	M		Transmission is D0 first to D15 last

28.5.4.3 Transmit function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
11	Selector Field values	28.2.1.2.1	M		Only defined values transmitted
12	Technology Ability Field values	28.2.1.2.2	M		Implementation supports a data service for each ability set in the Technology Ability Field
13	Remote Fault bit	28.2.1.2.3	M		Used in accordance with the Remote Fault function specifications
14	Acknowledge bit set, no Next Page to be sent	28.2.1.2.4	M		Set to logic one in the Link Code Word after the reception of at least three consecutive and consistent FLP Bursts
15	Acknowledge bit set, Next Page to be sent	28.2.1.2.4	NP:M		Set to logic one in the transmitted Link Code Word after the reception of at least three consecutive and consistent FLP Bursts and the current receive Link Code Word is saved
16	Number of Link Code Words sent with Acknowledge bit set	28.2.1.2.4	M		6 to 8 inclusive after COMPLETE ACKNOWLEDGE state entered
17	Device does not implement optional Next Page ability	28.2.1.2.5	M		NP=0 in base Link Code Word
18	Device implements optional Next Page ability and wishes to engage in Next Page exchange	28.2.1.2.5	NP:M		NP=1 in base Link Code Word
19	Transmit Switch function on completion of Auto-Negotiation	28.2.1.3	M		Enables the transmit path from a single technology-dependent PMA to the MDI once the highest common denominator has been selected
20	Transmit Switch function during Auto-Negotiation	28.2.1.3	M		Connects FLP Burst generator governed by Figure 28–15 to the MDI
21	Signals presented at MDI after connection through Transmit Switch from PMA	28.2.1.3	M		Conform to appropriate PHY specifications

28.5.4.4 Receive function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	Timer expiration	28.2.2.1	M		Timer definition in 28.3.2, values shown in Table 28–9
2	Identification of Link Partner as Auto-Negotiation able	28.2.2.1	M		Reception of 6 to 17 (inclusive) consecutive link pulses separated by at least flp_test_min_timer time but less than flp_test_max_timer time
3	First FLP Burst identifying Link Partner as Auto-Negotiation able	28.2.2.1	M		Data recovered is discarded if FLP Burst is incomplete
4	First link pulse in an FLP Burst	28.2.2.1	M		Interpreted as a clock link pulse
5	Restart of the data_detect_min_timer and data_detect_max_timer	28.2.2.1	M		Detection of a clock link pulse (Figure 28–9)
6	Reception of logic one	28.2.2.1	M		Link pulse received between greater than data_detect_min_timer time and less than data_detect_max_timer time after a clock pulse (Figure 28–9)
7	Reception of logic zero	28.2.2.1	M		Link pulse received after greater than data_detect_max_timer time after clock pulse, is treated as clock pulse (Figure 28–9)
8	FLP Bursts separation	28.2.2.1	M		Conforms to the nlp_test_min_timer and nlp_test_max_timer timing (Figure 28–10)
9	Receive Switch function on completion of Auto-Negotiation	28.2.2.3	M		Enables the receive path from the MDI to a single technology-dependent PMA once the highest common denominator has been selected
10	Receive Switch function during Auto-Negotiation	28.2.2.3	M		Connects the MDI to the FLP and NLP receivers governed by Figures 28–16 and 28–18, and to the 100BASE-TX and 100BASE-T4 receivers if present
11	Signals presented to PMA after connection through Receive Switch from MDI	28.2.2.3	M		Conform to appropriate PHY specifications
12	Generation of ability_match, acknowledge_match, and consistency_match	28.2.2.4	M		Responsibility of Receive function in accordance with 28.3.1

28.5.4.5 Arbitration functions

Item	Feature	Subclause	Status	Support	Value/comment
1	MDI receive connection during Auto-Negotiation, prior to FLP detection	28.2.3.1	M		Connected to the NLP Receive Link Integrity Test state diagram, and the link integrity test functions of 100BASE-TX and/or 100BASE-T4. Not connected to the 10BASE-T or any other PMA
2	Parallel detection operational mode selection	28.2.3.1	M		Set link_control=ENABLE for the single PMA indicating link_status=READY when the autoneg_wait_timer expires
3	Parallel detection PMA control	28.2.3.1	M		Set link_control=DISABLE to all PMAs except the selected operational PMA and indicate Auto-Negotiation has completed
4	Parallel detection setting of link partner ability register	28.2.3.1	M		On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the link partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function
5	Response to renegotiation request	28.2.3.2	M		Disable all technology-dependent link integrity test functions and halt transmit activity until break_link_timer expires
6	Auto-Negotiation resumption	28.2.3.2	M		Issue FLP Bursts with base page valid in tx_link_code_word[16:1] after break_link_timer expires
7	Priority resolution	28.2.3.3	M		Single PMA connected to MDI is enabled corresponding to Technology Ability Field bit common to both Local/Link Partner Device and that has highest priority as defined by Annex 28B
8	Effect of receipt of reserved Technology Ability Field bit on priority resolution	28.2.3.3	M		Local Device ignores during priority resolution
9	Effect of parallel detection on priority resolution	28.2.3.3	M		Local Device considers technology identified by parallel detection as HCD
10	Values for HCD and link_status_[HCD] in the event there is no common technology	28.2.3.3	M		HCD=NULL link_status_[HCD]=FAIL

28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
11	Message Page to Unformatted Page relationship for non-matching Selector Fields	28.2.3.4	NP:M		Each series of Unformatted Pages is preceded by an Message Page containing a message code that defines how the following Unformatted Page(s) will be interpreted
12	Message Page to Unformatted Page relationship for matching Selector Fields	28.2.3.4	NP:M		Use of Message Pages is specified by the Selector Field value
13	Transmission of Null message codes	28.2.3.4	NP:M		Sent with NP=0 on completion of all Next Pages while Link Partner continues to transmit valid Next Page information
14	Reception of Null message codes	28.2.3.4	NP:M		Recognized as indicating end of Link Partner's Next Page information
15	Next Page encoding	28.2.3.4.1	NP:M		Comply with Figures 28–11 and 28–12 for the NP, Ack, MP, Ack2, and T bits
16	Message/Unformatted Code Field	28.2.3.4.1	NP:M		D10-D0 encoded as Message Code Field if MP=1 or Unformatted Code Field if MP=0
17	NP bit encoding	28.2.3.4.3	NP:M		Logic 0=last page, logic 1=additional Next Page(s) follow
18	Message Page bit encoding	28.2.3.4.5	NP:M		Logic 0=Unformatted Page, logic 1=Message Page
19	Ack2 bit encoding	28.2.3.4.6	NP:M		Logic 0=cannot comply with message; logic 1= will comply with message
20	Toggle	28.2.3.4.7	NP:M		Takes the opposite value of the Toggle bit in the previously exchanged Link Code Word
21	Toggle encoding	28.2.3.4.7	NP:M		Logic zero = previous value of the transmitted Link Code Word equalled logic one Logic one = previous value of the transmitted Link Code Word equalled logic zero
22	Message Page encoding	28.2.3.4.8	NP:M		If MP=1, Link Code Word interpreted as Message Page
23	Message Code Field	28.2.3.4.9	NP:M		Combinations not shown in Annex 28B are reserved and may not be transmitted
24	Unformatted Page encoding	28.2.3.4.10	NP:M		If MP=0, Link Code Word interpreted as Unformatted Page

28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
25	Minimum Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, both send a minimum of one Next Page
26	Multiple Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, exchange continues until neither Local/Remote Device has additional information; device sends Next Page with Null Message Code if it has no information to transmit
27	Unformatted Page ordering	28.2.3.4.13	NP:M		Unformatted Pages immediately follow the referencing Message Code in the order specified by the Message Code
28	Next Page Transmit register	28.2.3.4.14	NP:M		Defined in 28.2.4.1.6
29	Next Page receive data	28.2.3.4.14	NP:O		May be stored in Auto-Negotiation link partner ability register
30	Remote Fault sensing	28.2.3.5	RF:M		Optional
31	Transmission of RF bit by Local Device	28.2.3.5	M		If Local Device has no method to set RF bit, it must transmit RF bit with value of RF bit in Auto-Negotiation advertisement register (4.13)
32	RF bit reset	28.2.3.5	M		Once set, the RF bit remains set until successful renegotiation with the base Link Code Word
33	Receipt of Remote Fault indication in Base Link Code Word	28.2.3.5	MII:M		Device sets the Remote Fault bit in the MII status register (1.4) to logic one if MII is present

28.5.4.6 Management function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	Mandatory MII registers for Auto-Negotiation	28.2.4.1	MII:M		Registers 0, 1, 4, 5, 6
2	Optional MII register for Auto-Negotiation	28.2.4.1	MII* NP:M		Register 7
3	Auto-Negotiation enable	28.2.4.1.1	MII:M		Set control register Auto-Negotiation Enable bit (0.12)

28.5.4.6 Management function requirements ***(continued)***

Item	Feature	Subclause	Status	Support	Value/comment
4	Manual Speed/Duplex settings	28.2.4.1.1	MII:M		When bit 0.12 set, control register Speed Detection (0.13) and Duplex Mode (0.8) are ignored, and the Auto-Negotiation function determines link configuration
5	Control register (Register 0) Restart Auto-Negotiation (0.9) default	28.2.4.1.1	MII:M		PHY returns value of one in 0.9 until Auto-Negotiation has been initiated
6	Control register (Register 0) Restart Auto-Negotiation (0.9) set	28.2.4.1.1	MII:M		When 0.9 set, Auto-Negotiation will (re)initiate. On completion, 0.9 will be reset by the PHY device. Writing a zero to 0.9 at any time has no effect
7	Control register (Register 0) Restart Auto-Negotiation (0.9) reset	28.2.4.1.1	MII:M		0.9 is self-clearing; writing a zero to 0.9 at any time has no effect
8	Status register (Register 1) Auto-Negotiation Complete (1.5) reset	28.2.4.1.2	MII:M		If bit 0.12 reset, or a PHY lacks the ability to perform Auto-Negotiation, (1.5) is reset
9	Status register (Register 1) Remote Fault (1.4)	28.2.4.1.2	MII:M		Set by the PHY and remains set until either the status register is read or the PHY is reset
10	Advertisement register power on default	28.2.4.1.3	MII:M		Selector field as defined in Annex 28A; Ack=0; Technology Ability Field based on MII status register (1.15:11) or logical equivalent
11	Link partner ability register read/write	28.2.4.1.4	MII:M		Read only; write has no effect
12	Link partner ability register bit definitions	28.2.4.1.4	MII:M		Direct representation of the received Link Code Word (Figure 28–7)
13	Status register (Register 1) Auto-Negotiation Complete (1.5) set	28.2.4.1.4	MII:M		Set to logic one upon successful completion of Auto-Negotiation
14	Auto-Negotiation expansion register (Register 6)	28.2.4.1.5	MII:M		Read only; write has no effect
15	Link Partner Auto-Negotiation Able bit (6.0)	28.2.4.1.5	MII:M		Set to indicate that the Link Partner is able to participate in the Auto-Negotiation function
16	Page Received bit (6.1) set	28.2.4.1.5	MII:M		Set to indicate that a new Link Code Word has been received and stored in the Auto-Negotiation link partner ability register
17	Page Received bit (6.1) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)

28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
18	The Next Page Able bit (6.2) set	28.2.4.1.5	NP* MII:M		Set to indicate that the Local Device supports the Next Page function
19	The Link Partner Next Page Able bit (6.3) set	28.2.4.1.5	MII:M		Set to indicate that the Link Partner supports the Next Page function
20	Parallel Detection Fault bit (6.4) set	28.2.4.1.5	MII:M		Set to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires
21	Parallel Detection Fault bit (6.4) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)
22	Next Page Transmit register default	28.2.4.1.6	NP* MII:M		On power-up, contains value of 2001 H
23	Write to Next Page Transmit register	28.2.4.1.6	NP* MII:M		mr_next_page_loaded set to true
24	Absence of management function	28.2.5	NOM:M		Advertised abilities provided through a logical equivalent of mr_adv_ability[16:1]
25	Next Page support in absence of MII management	28.2.5	NOM:M		Device must provide logical equivalent of mr_np_able, mr_lp_np_able, or mr_next_page_loaded variables in order to set NP bit in transmitted Link Code Word

28.5.4.7 Technology-dependent interface

Item	Feature	Subclause	Status	Support	Value/comment
1	PMA_LINK.indicate(link_status) values	28.2.6.1.1	M		link_status set to READY, OK or FAIL
2	PMA_LINK.indicate(link_status) generation	28.2.6.1.2	M		Technology-dependent PMA and NLP Receive Link Integrity Test state diagram (Figure 28–18) responsibility
3	PMA_LINK.indicate(link_status), effect of receipt	28.2.6.1.3	M		Governed by the state diagram of Figure 28–17
4	PMA_LINK.request(link_control) values	28.2.6.1.3	M		link_control set to SCAN_FOR_CARRIER, DISABLE, or ENABLE

28.5.4.7 Technology-dependent interface *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
5	Effect of link_control=SCAN_FOR_CARRIER	28.2.6.2.1	M		PMA to search for carrier and report link_status=READY when carrier is received, but no other actions are enabled
6	Effect of link_control=DISABLE	28.2.6.2.1	M		Disables PMA processing
7	Effect of link_control=ENABLE	28.2.6.2.1	M		Control passed to a single PMA for normal processing functions
8	PMA_LINK.request(link_control) generation	28.2.6.2.2	M		Auto-Negotiation function responsibility in accordance with Figures 28–16 and 28–17
9	PMA_LINK.request(link_control) default upon power-on, reset, or release from power-down	28.2.6.2.2	M		link_control = DISABLE state to all technology-dependent PMAs
10	PMA_LINK.request(link_control) effect of receipt	28.2.6.2.3	M		Governed by Figure 28–18 and the receiving technology-dependent link integrity test function
11	The linkpulse parameter shall	28.2.6.3.1	M	Yes [ ]	TRUE or FALSE.
12	The linkpulse=FALSE shall be used	28.2.6.3.1	M	Yes [ ]	By the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.
13	The linkpulse=TRUE shall be used	28.2.6.3.1	M	Yes [ ]	By the Auto-Negotiation function to indicate that a valid Link Pulse has been received.
14	The Auto-Negotiation function shall generate linkpulse	28.2.6.3.2	M	Yes [ ]	To indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–16.
15	Upon power-on or reset, if Auto-Negotiation is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request(FALSE) message shall be	28.2.6.3.2	M	Yes [ ]	Issued to all technology-dependent PMAs.
16	The effect of the receipt of linkpulse shall be governed	28.2.6.3.3	M	Yes [ ]	By the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.5.4.8 State diagrams

Item	Feature	Subclause	Status	Support	Value/comment
1	Adherence to state diagrams	28.3	M		Implement all features of Figures 28–15 to 28–18. Identified options to Figures 28–15 to 28–18 are permitted
3	Ambiguous requirements	28.3	M		State diagrams take precedence in defining functional operation
4	autoneg_wait_timer	28.3.1	M		Expires between 500–1000 ms after being started
5	break_link_timer	28.3.2	M		Expires between 1200–1500 ms after being started
6	data_detect_min_timer	28.3.2	M		Expires between 15–47 μs from the last clock pulse
7	data_detect_max_timer	28.3.2	M		Expire between 78–100 μs from the last clock pulse
8	flp_test_max_timer	28.3.2	M		Expires between 165–185 μs from the last link pulse
9	flp_test_min_timer	28.3.2	M		Expires between 5–25 μs from the last link pulse
10	interval_timer	28.3.2	M		Expires 55.5–69.5 μs from each clock pulse and data bit
11	link_fail_inhibit_timer	28.3.2	M		Expires 750–1000 ms after entering the FLP LINK GOOD CHECK state
12	nlp_test_max_timer	28.3.2	M		Expires between 50–150 ms after being started if not restarted
13	nlp_test_min_timer	28.3.2	M		Expires between 5–7 ms after being started if not restarted
14	transmit_link_burst_timer	28.3.1	M		Expires 5.7–22.3 ms after the last transmitted link pulse in an FLP Burst

28.5.4.9 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/comment
1	Pulses within FLP Bursts	28.4	M		Identical to the characteristics of NLPs and meet the requirements of Figure 14–12

28.5.4.10 Auto-Negotiation annexes

Item	Feature	Annex	Status	Support	Value/comment
1	Selector field, S[4:0] values in the Link Code Word	Annex 28A	M		Identifies base message type as defined by Table 28A–1
2	Selector field reserved combinations	Annex 28A	M		Transmission not permitted
3	Relative priorities of the technologies supported by the IEEE 802.3 Selector Field value	28B.3	M		Defined in Annex 28B.3
4	Relative order of the technologies supported by IEEE 802.3 Selector Field	28B.3	M		Remain unchanged
5	Addition of new technology	28B.3	M		Inserted into its appropriate place in the priority resolution hierarchy, shifting technologies of lesser priority lower in priority
6	Addition of vendor-specific technology	28B.3	M		Priority of IEEE 802.3 standard topologies maintained, vendor-specific technologies to be inserted into an appropriate location
7	Message Code Field	Annex 28C	NP:M		Defines how following Unformatted Pages (if applicable) are interpreted
8	Message Code Field reserved combinations	Annex 28C	NP:M		Transmission not permitted
9	Auto-Negotiation reserved code 1	28C.1	NP:M		Transmission of M10 to M0 equals 0, not permitted
10	Null Message Code	28C.2	NP:M		Transmitted during Next Page exchange when the Local Device has no information to transmit and Link Partner has additional pages to transmit
11	Remote Fault Identifier Message Code	28C.5	NP:M		Followed by single Unformatted Page to identify fault type with types defined in 28C.5

28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/comment
12	Organizationally Unique Identifier Message Code	28C.6	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of OUI (bits 23:13) with MSB in U10; Second Unformatted Page contains next most significant 11 bits of OUI (bits 12:2), with MSB in U10; Third Unformatted Page contains the least significant 2 bits of OUI (bits 1:0) with MSB in U10, bits U8:0 contains user-defined code specific to OUI; Fourth Unformatted Page contains user-defined code specific to OUI
13	PHY Identifier Message Code	28C.7	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of PHY ID (2.15:5) with MSB in U10; Second Unformatted Page contains PHY ID bits 2.4:0 to 3.15:10, with MSB in U10; Third Unformatted Page contains PHY ID bits 3.9:0, with MSB in U10, and U0 contains user-defined code specific to PHY ID; Fourth Unformatted Page contains user-defined code specific to PHY ID
14	Auto-Negotiation reserved code 2	28C.8	NP:M		Transmission of M10 to M0 equals 1, not permitted

28.6 Auto-Negotiation expansion

Auto-Negotiation is designed in a way that allows it to be easily expanded as new technologies are developed. When a new technology is developed, the following things must be done to allow Auto-Negotiation to support it:

a) The appropriate Selector Field value to contain the new technology must be selected and allocated.
b) A Technology bit must be allocated for the new technology within the chosen Selector Field value.
c) The new technology's relative priority within the technologies supported within a Selector Field value must be established.

Code space allocations are enumerated in Annex 28A, Annex 28B, and Annex 28C. Additions and insertions to the annexes are allowed. No changes to existing bits already defined are allowed.

Annex 28A

(normative)

Selector Field definitions

The Selector Field, S[4:0] in the Link Code Word, shall be used to identify the type of message being sent by Auto-Negotiation. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Selector Field uses a 5-bit binary encoding, which allows 32 messages to be defined. All unspecified combinations are reserved. Reserved combinations shall not be transmitted.

Table 28A–1—Selector Field value mappings

S4	S3	S2	S1	S0	Selector description
0	0	0	0	0	Reserved for future Auto-Negotiation development
0	0	0	0	1	IEEE Std 802.3
0	0	0	1	0	IEEE Std 802.9 ISLAN-16T
0	0	0	1	1	IEEE Std 802.5
1	1	1	1	1	Reserved for future Auto-Negotiation development[a]

[a]For up-to-date information on the allocation of Auto-Negotiation Selector fields see http://www.ieee802.org/3/selectors/selectors.html

Annex 28B

(normative)

IEEE 802.3 Selector Base Page definition

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the base page encoding.

As new IEEE 802.3 LAN technologies are developed, a reserved bit in the Technology Ability field may be assigned to each technology by the standards body.

The new technology will then be inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation standard. The relative hierarchy of the existing technologies will not change, thus providing backward compatibility with existing Auto-Negotiation implementations.

It is important to note that the reserved bits are required to be transmitted as logic zeros. This guarantees that devices implemented using the current priority table will be forward compatible with future devices using an updated priority table.

28B.1 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

28B.2 Technology Ability Field bit assignments

The Technology bit field consists of bits D5 through D12 (A0–A7, respectively) in the IEEE 802.3 Selector Base Page. Table 28B–1 summarizes the bit assignments.

Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Setting Bit A5 or Bit A6 indicates that the DTE has implemented both the optional MAC control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium. The encoding of Bits A5 and A6 is specified in Table 28B–2.

Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair category 3
A1	10BASE-T full duplex	Two-pair category 3
A2	100BASE-TX	Two-pair category 5
A3	100BASE-TX full duplex	Two-pair category 5
A4	100BASE-T4	Four-pair category 3
A5	PAUSE operation for full duplex links	Not applicable
A6	Asymmetric PAUSE operation for full duplex Links	Not applicable
A7	Extended Next Page	Not applicable

Table 28B–2—Pause encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

28B.3 Priority resolution

Since two devices may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

a) 10GBASE-T full duplex
b) 1000BASE-T full duplex
c) 1000BASE-T
d) 100BASE-T2 full duplex
e) 100BASE-TX full duplex
f) 100BASE-T2
g) 100BASE-T4
h) 100BASE-TX
i) 10BASE-T full duplex
j) 10BASE-T

The rationale for this hierarchy is straightforward. 10BASE-T is the lowest common denominator and therefore has the lowest priority. Full duplex solutions are always higher in priority than their half duplex counterparts. 1000BASE-T has a higher priority than 100 Mb/s technologies. 100BASE-T2 is ahead of 100BASE-TX and 100BASE-T4 because 100BASE-T2 runs across a broader spectrum of copper cabling and can support a wider base of configurations. 100BASE-T4 is ahead of 100BASE-TX because 100BASE-T4 runs across a broader spectrum of copper cabling. The relative order of the technologies specified herein shall not be changed. As each new technology is added, it shall be inserted into its appropriate place in the list, shifting technologies of lesser priority lower in priority. If a vendor-specific technology is implemented, the priority of all IEEE 802.3 standard technologies shall be maintained, with the vendor specific technology inserted at any appropriate priority location.

The use of the PAUSE operation for full duplex links (as indicated by bits A5 and A6) is orthogonal to the negotiated data rate, medium, or link technology. The setting of these bits indicates the availability of additional DTE capability when full duplex operation is in use. The PAUSE function shall be enabled according to Table 28B–3 only if the Highest Common Denominator is a full duplex technology. There is no priority resolution associated with the PAUSE operation.

Table 28B–3—Pause resolution

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	Don’t care	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don’t care	1	Don’t care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

28B.4 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a Message Code that defines how the following Unformatted Pages will be used.

Next Page message codes should be allocated globally across Selector Field values so that meaningful communication is possible between technologies using different Selector Field values.

Annex 28C

(normative)

Next Page Message Code Field definitions

The Message Code Field of a message page used in Next Page exchange shall be used to identify the meaning of a message. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Message Code Field uses an 11-bit binary encoding that allows 2048 messages to be defined. All Message Codes not specified shall be reserved for IEEE use or allocation.

Table 28C–1—Message code field values

Message Code #	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message Code Description
0	0	0	0	0	0	0	0	0	0	0	0	Reserved for future Auto-Negotiation use
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
2	0	0	0	0	0	0	0	0	0	1	0	One UP with Technology Ability Field follows
3	0	0	0	0	0	0	0	0	0	1	1	Two UPs with Technology Ability Field follow
4	0	0	0	0	0	0	0	0	1	0	0	One UP with Binary coded Remote fault follows
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	PHY Identifier Tag Code
7	0	0	0	0	0	0	0	0	1	1	1	100BASE-T2 Technology Message Code. 100BASE-T2 Ability Page to follow using Unformatted Next Page
8	0	0	0	0	0	0	0	1	0	0	0	1000BASE-T Technology Message Code. Two 1000BASE-T Ability Pages to follow using Unformatted Next Pages.
9	0	0	0	0	0	0	0	1	0	0	1	10GBASE-T and 1000BASE-T Technology Message Code.
10.....	0	0	0	0	0	0	0	1	0	1	0	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

28C.1 Message code #0—Auto-Negotiation reserved code 1

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.2 Message code #1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 28.2.3.4 for more details.

28C.3 Message code #2—Technology Ability extension code 1

This Message Code is reserved for future expansion of the Technology Ability Field and indicates that a defined user code with a specific Technology Ability Field encoding follows.

28C.4 Message code #3—Technology Ability extension code 2

This Message Code is reserved for future expansion of the Technology Ability Field and indicates that two defined user codes with specific Technology Ability Field encodings follow.

28C.5 Message code #4—Remote fault number code

This Message Code shall be followed by a single user code whose encoding specifies the type of fault that has occurred. The following user codes are defined:

0: RF Test
This code can be used to test Remote Fault operation.
1: Link Loss
2: Jabber
3: Parallel Detection Fault
This code may be sent to identify when bit 6.4 is set.

28C.6 Message code #5—Organizationally Unique Identifier (OUI) tag code

The OUI Tagged Message shall consist of a single message code of 0000 0000 0101 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the OUI (bits 23:13) with the most significant bit in bit 10 of the user code. The second user code shall contain the next most significant 11 bits of the OUI (bits 12:2) with the most significant bit in bit 10 of the user code. The third user code shall contain the remaining least significant 2 bits of the OUI (bits 1:0) with the most significant bit in bit 10 of the user code. Bits 8:0 of the fourth user contain a user-defined user code value that is specific to the OUI transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the OUI transmitted.

28C.7 Message code #6—PHY identifier tag code

The PHY ID tag code message shall consist of a single message code of 0000 0000 0110 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the PHY ID

(2.15:5) with the most significant bit in bit 10 of the user code. The second user code shall contain bits 2.4:0 to 3.15:10 of the PHY ID with the most significant bit in bit 10 of the user code. The third user code shall contain bits 3.9:0 of the PHY ID with the most significant bit in bit 10 of the user code. Bit 0 in the third user code shall contain a user-defined user code value that is specific to the PHY ID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the PHY ID transmitted.

28C.8 Message code #2047— Auto-Negotiation reserved code 2

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.9 Message code #7—100BASE-T2 technology message code

Clause 32 (100BASE-T2) uses Next Page Message Code 7 to indicate that T2 implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages which contain information defined in 32.5.4.2.

28C.10 Message Code #8—1000BASE-T technology message code

Clause 40 (1000BASE-T) uses Next Page Message Code 8 to indicate that 1000BASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages that contain information defined in 40.5.1.2.

28C.11 Message Code #9—10GBASE-T and 1000BASE-T technology message code

#CrossRef# Clause 55 (10GBASE-T) uses Next Page Message Code 9 to indicate that 10GBASE-T and 1000BASE-T abilities are contained within this extended Next Page. The Next Page that contains this information is defined in #CrossRef# TBD.

Annex 28D

(normative)

Description of extensions to Clause 28 and associated annexes

28D.1 Introduction

This annex is to be used to document extensions and modifications to Clause 28 required by IEEE 802.3 clauses and other standards that use Auto-Negotiation and that were approved after June 1995. It provides a single location to define such extensions and modifications without changing the basic contents of Clause 28.

Subclause 28D.2 lists those clauses and standards that require extensions to Clause 28 and provides pointers to the subclauses where those extensions are listed.

28D.2 Extensions to Clause 28

28D.2.1 Extensions required for Clause 31 (full duplex)

Clause 31 (full duplex) requires the use of Auto-Negotiation. Extensions to Clause 28 and associated annexes required for the correct operation of full duplex are shown in 28D.3.

28D.2.2 Extensions required for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) requires the use of Auto-Negotiation. Extensions to Clause 28 required for correct operation of 100BASE-T2 are shown in 28D.4.

28D.3 Extensions for Clause 31

Full duplex requires the use of bit A5 in the Technology Ability Field of the IEEE 802.3 Selector Base Page. (This bit is also defined as MII bit 4.10.) This bit was previously defined as “reserved for future technology.”

Bit	Technology	Minimum cabling requirement
A5	PAUSE operation for full duplex links	Not applicable

Bit A5 (PAUSE operation for full duplex links) signifies that the DTE has implemented both the optional MAC Control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium.

28D.4 Extensions for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 32.5.

Auto-Negotiation is mandatory for 100BASE-T2 (32.1.3.4).

100BASE-T2 introduces the concept of MASTER and SLAVE to define DTEs and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER/SLAVE status (32.5.4.3).

100BASE-T2 uses unique next page transmit and receive registers (MII Registers 8, 9 and 10) in conjunctions with Auto-Negotiation. These registers are in addition to Registers 0–7 as defined in 28.2.4 (32.5.2).

100BASE-T2 use of Auto-Negotiation generates information which is stored in configuration and status bits defined for the MASTER-SLAVE Control register (MII Register 9) and the MASTER-SLAVE Status register (MII Register 10).

100BASE-T2 requires an ordered exchange of next page messages (32.5.1).

100BASE-T2 parameters are configured based on information provided by the ordered exchange of next page messages.

100BASE-T2 adds new message codes to be transmitted during Auto-Negotiation (32.5.4.2).

100BASE-T2 adds 100BASE-T2 full duplex and half duplex capabilities to the priority resolution table (28B.3) and MII Status Register (22.2.4.2).

T2 is defined as a valid value for “x” in 28.3.1 (e.g., link_status_T2). T2 represents that the 100BASE-T2 PMA is the signal source.

28D.5 Extensions required for Clause 40 (1000BASE-T)

Clause 40 (1000BASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 40.5.

a) Auto-Negotiation is mandatory for 1000BASE-T. (40.5.1)
b) 1000BASE-T requires an ordered exchange of Next Page messages. (40.5.1.2)
c) 1000BASE-T parameters are configured based on information provided by the ordered exchange of NEXT Page messages.
d) 1000BASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.(40.5.2)
e) 1000BASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2 and 40.5.1.1), which are required in addition to registers 0-8 as defined in 28.2.4.
f) 1000BASE-T adds new message codes to be transmitted during Auto-Negotiation. (40.5.1.3)
g) 1000BASE-T adds 1000BASE-T full duplex and half duplex capabilities to the priority resolution table. (28B.3) and MII Extended Status Register (22.2.2.4)
h) 1000BASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_1GigT.) 1GigT represents that the 1000BASE-T PMA is the signal source.
i) 1000BASE-T supports Asymmetric Pause as defined in Annex 28B.

28D.6 Extensions required for #CrossRef# Clause 55 (10GBASE-T)

#CrossRef# Clause 55 (10GBASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in #CrossRef# TBD.

a) Auto-Negotiation is mandatory for 10GBASE-T. (#CrossRef# TBD)
b) 10GBASE-T requires an ordered exchange of Next Page messages. (#CrossRef# TBD)
c) 10GBASE-T parameters are configured based on information provided by the ordered exchange of NEXT Page messages.
d) 10GBASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.(#CrossRef# TBD)
e) 10GBASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2, 40.5.1.1, and #CrossRef# TBD), which are required in addition to registers 0-8 as defined in 28.2.4.
f) 10GBASE-T adds new message codes to be transmitted during Auto-Negotiation. (#CrossRef# TBD)
g) 10GBASE-T adds 10GBASE-T full duplex capabilities to the priority resolution table. (28B.3) and TBD (#CrossRef# TBD)
h) 10GBASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_10GigT.) 10GigT represents that the 10GBASE-T PMA is the signal source.
i) TBD

55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.1 Overview

The 10GBASE-T PHY is one of the 10 Gigabit Ethernet family of high-speed CSMA/CD network specifications. The 10GBASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium specifications are intended for users who want 10 Gb/s performance over balanced twisted-pair structured cabling systems. 10GBASE-T signaling requires four pairs of balanced cabling, as specified in ISO/IEC 11801 Edition 2 with appropriate augmentation as specified in Clause 55.7.

This clause defines the type 10GBASE-T PCS, type 10GBASE-T PMA sublayer, and type 10GBASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 10GBASE-T Physical layer (PHY). Functional, electrical and mechanical specifications for the type 10GBASE-T PCS, PMA, and MDI are provided in this document. This clause also specifies the baseband medium used with 10GBASE-T.

55.1.1 Objectives

The following are the objectives of 10GBASE-T:

a) Support full duplex operation at 10 Gb/s over four connector structured four-pair, twisted-pair copper cabling with distances of:
   1) 100 m on four pair Class F balanced copper cabling as specified in ISO/IEC 11801 Edition 2 (with additional requirements specified in Clause 55.7).
   2) At least 55 m to 100 m on four pair Class E balanced copper cabling as specified in ISO/IEC 11801 Edition 2 (with additional requirements specified in Clause 55.7).

b) Preserve the 802.3/Ethernet frame format at the MAC Client service Interface.

c) Preserve minimum and maximum frame size of the current 802.3 Standard.

d) Support Auto-Negotiation (Clause 28).

e) Meet CISPR/FCC Class A EMC limits.

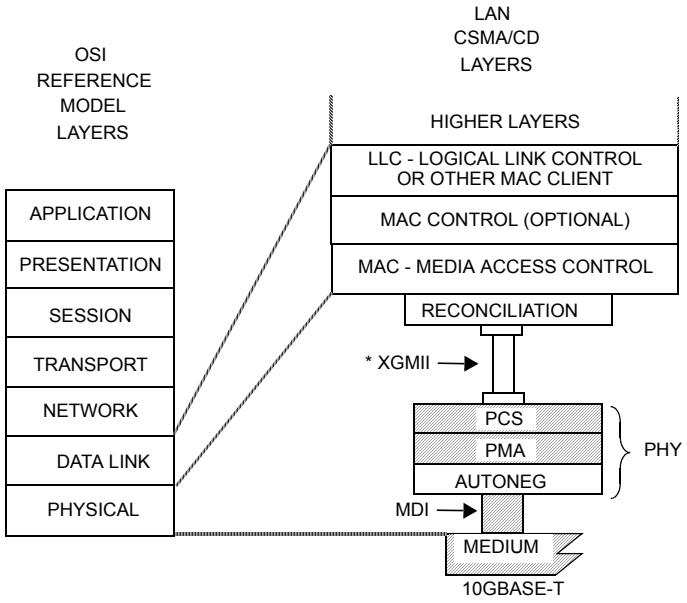
f) Support a Bit Error Rate of less than or equal to 10^{-12} on all supported distances and Classes

Editor's Note: When the extrapolation of the Class E specifications specified in Clause 55.7 is incorporated into the appropriate TIA/ISO/IEC specifications, we will pull in references to these in here. Frequency extrapolation of the Class E specification is already available in the TR-42 Draft Technical Report entitled "Assessment of installed class E and class F cabling performance beyond their maximum specified frequencies.

Upon approval of the objective by the 802.3 Working Group, an additional item,a 3) will be added after a 2) This will state: 3) 100 m on four pair Augmented Class E balanced copper cabling as specified in Clause 55.7.

55.1.2 Relationship of 10GBASE-T to other standards

Relations between the 10GBASE-T PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 55–1. The PHY sub-layers (shown shaded) in Figure 55–1 connect one Clause 4 Media Access Control (MAC) layer to the medium.



MDI = MEDIUM DEPENDENT INTERFACE
XGMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE

*XGMII is optional.

Figure 55–1—Type 10GBASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

55.1.3 Operation of 10GBASE-T

The 10GBASE-T PHY employs full duplex baseband transmission over four pairs of balanced cabling. The aggregate data rate of 10 Gb/s is achieved by transmission at a data rate of 2500 Mb/s over each wire pair, as shown in Figure 55–2. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signaling with a modulation rate of 800 Msymbols/s is used on each of the wire pairs. The transmitted symbols are selected from a four-dimensional 12-level symbol constellation. Each four-dimensional symbol can be viewed as a 4-tuple (A_n, B_n, C_n, D_n) of one-dimensional symbols taken from the set {-11, -9, -7, -5, -3, -2, -1, 1, 3, 5, 7, 9, 11}. 10GBASE-T uses a continuous signaling system; in the absence of data, control symbols are transmitted. Data and Control symbols are embedded in a framing scheme which runs continuously after startup of the link. 12-level Pulse Amplitude Modulation (PAM12) is employed for transmission over each wire pair. The modulation symbol rate of 800 Msymbols/s results in a symbol period of 1.25 ns.

A 10GBASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see TBD). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented, the SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 55–3. If loop timing is not implemented, the

SLAVE PHY clocking is identical to the MASTER PHY clocking. In a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

The PCS and PMA subclauses of this document are summarized in 55.1.3.1 and 55.1.3.2. Figure 55–3 shows the functional block diagram.

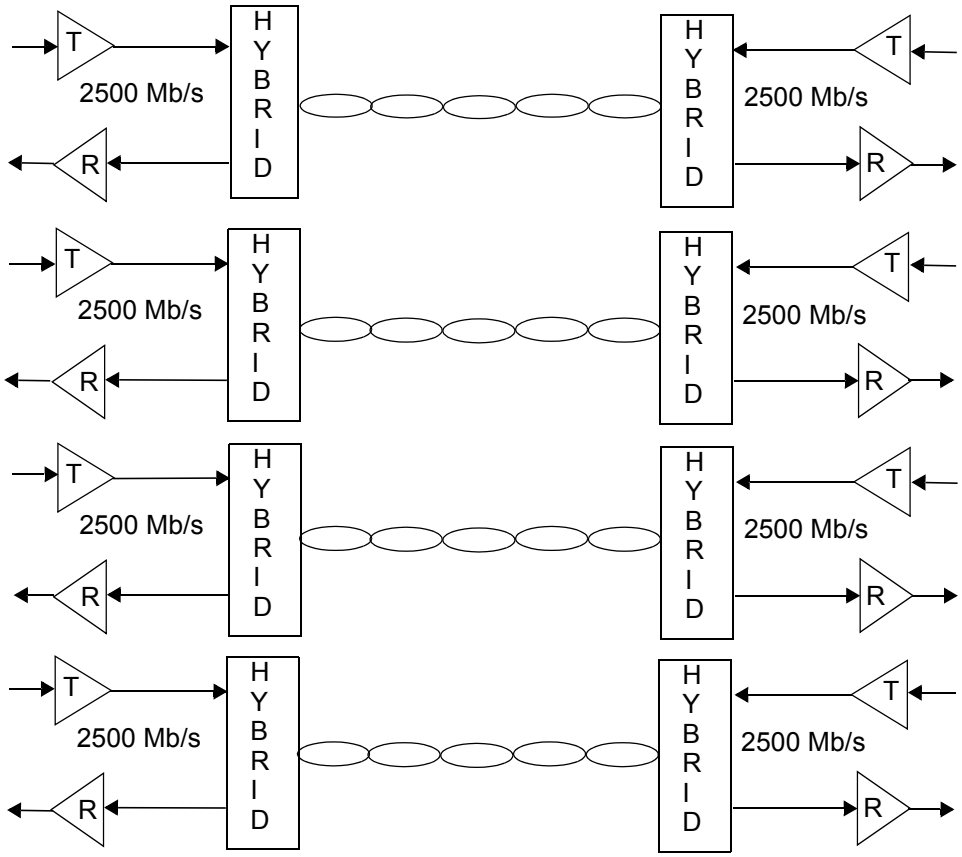


Figure 55–2—10GBASE-T topology

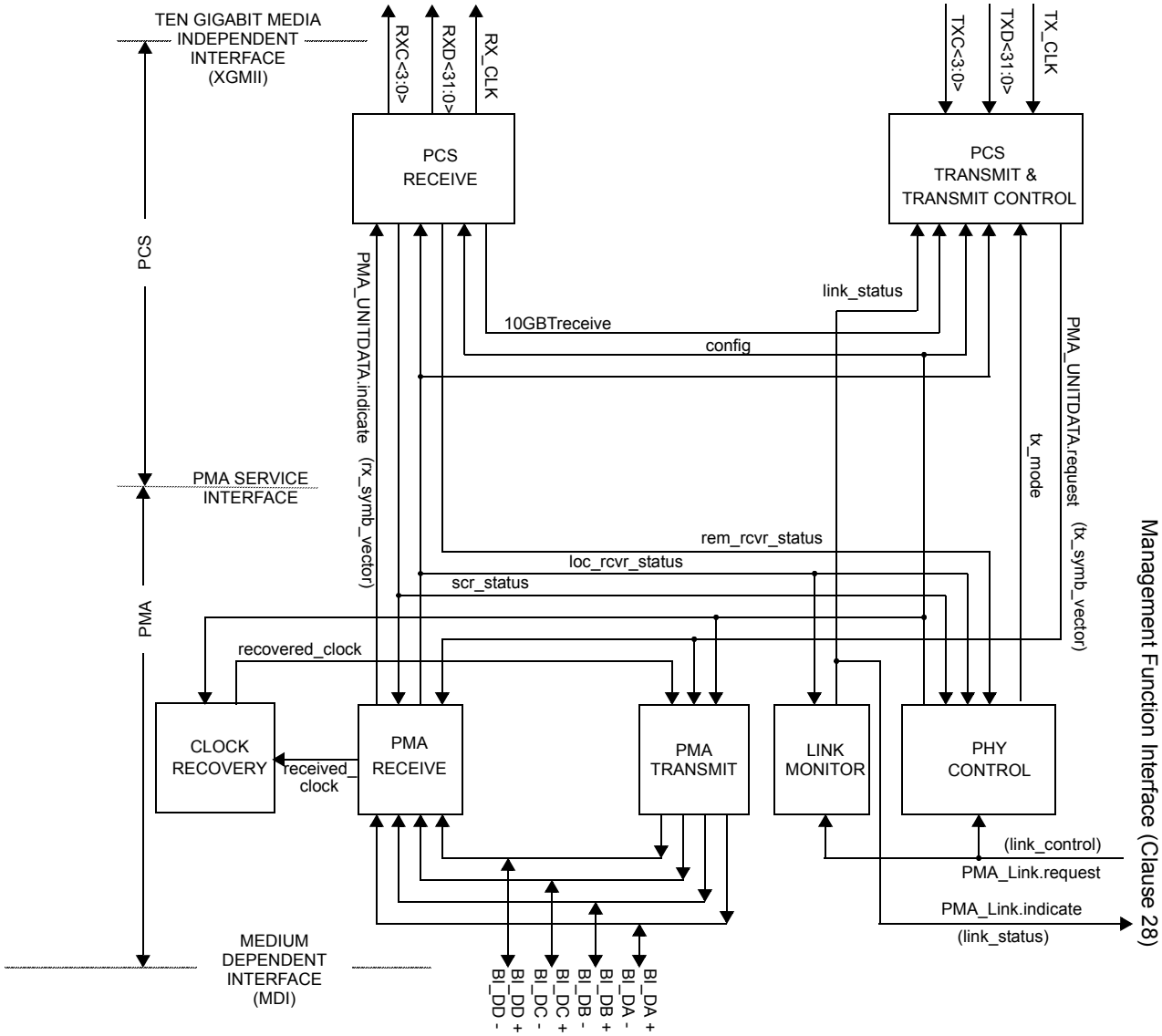


Figure 55–3—Functional block diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

55.1.3.1 Physical Coding Sublayer (PCS)

The 10GBASE-T PCS couples a Ten Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 10GBASE-T Physical Medium Attachment (PMA) sublayer.

In the transmit direction, in normal mode, the PCS takes eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the XGMII start of packet boundary as indicated by the XGMII transmit control signals (TXCn = 1). The resulting 65-bit blocks are taken in groups of TBD to form an LDPC transmit frame. TBD bits of the frame are encoded using a (TBD,TBD) LDPC encoder and mapped to cosets in the PAM12 constellation. The remaining TBD bits are left uncoded and mapped to the partitions in the PAM12 constellation. The result is an LDPC block consisting of TBD four dimensional PAM12 symbols.

. An LDPC frame sync header of TBD four dimensional signals is then added to the head of TBD LDPC block(s) to generate a continuous stream of four dimensional symbols that is passed on the PMA via PMA_UNITDATA.request signal. The PMA transmit block operates continuously this stream of four dimensional symbols. Details of the mapping are covered in TBD.

In the receive direction, in normal mode, the PCS processes code-groups received from the remote PHY via the PMA in TBD symbol blocks and maps them to the XGMII service interface in the receive path. In this receive processing scheme, symbol clock synchronization is done by the PMA receive function.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

The PCS functions and state diagrams are specified in 55.3. The signals provided by the PCS at the XGMII conform to the interface requirements of Clause 46. The PCS Service Interfaces to the XGMII and the PMA are abstract message-passing interfaces specified in 55.2.

55.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the balanced cabling physical medium via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at 800 Msymbols/s over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four transmitters to generate continuous time analog signals on each of the four pairs BI_DA, BI_DB, BI_DC and BI_DD, as described in 55.4.3.1. In normal mode, each four dimensional symbol received from the PCS transmit function undergoes multiple stages of processing. First the symbol goes through a Tomlinson Harashima Precoder (THP) which maps the PAM12 input in each dimension of the four dimensional symbol into a quasi-continuous discrete time value in the range {-12, 12}. This THP processed four dimensional symbol stream is then processed through a transmit shaping filter and is then passed on to four digital to analog converters (DAC). The DAC outputs may be further processed with continuous time filters to roll off the high frequency spectral response to limit high frequency emissions and are then applied to the four balanced pairs via the MDI port.

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC and BI_DD, as described in 55.4.3.2. The receivers are responsible for acquiring symbol timing and, when operating in normal mode, for cancelling echo, near end cross talk, far end cross talk and equalizing the signal. The 4-D symbols are provided to the PCS receive function via the PMA_UNITDATA.indicate message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the start-up functions required

for successful 10GBASE-T operation. It determines whether the PHY operates in a normal state, enabling data transmission over the link segment, or whether the PHY sends special code-groups that are used in the training mode. The latter occurs when either one or both of the PHYs that share a link segment are not operating reliably.

PMA functions and state diagrams are specified in 55.4. PMA electrical specifications are given in 55.5.

55.1.4 Signaling

10GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including

a) Forward Error Correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to four dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.

The PHY operates in two basic modes, normal mode or training mode. In normal mode, PCS generates a continuous stream of four dimensional symbols that are transmitted via the PMA at TBD power levels. In training mode, the PCS is directed to generate only TBD symbols for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See the PCS reference diagram in 55.2.)

55.1.5 Inter-sublayer interfaces

All implementations of the balanced cabling link are compatible at the MDI. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. When the PHY is incorporated within the physical bounds of a single-port device or a multiport device, implementation of the XGMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

55.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementor.

55.2 10GBASE-T Service Primitives and Interfaces

10GBASE-T transfers data and control information across the following four service interfaces:

a) Ten Gigabit Media Independent Interface (XGMII)
b) Management Function Interface
c) PMA Service Interface
d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Management Function Interface is specified in Clause 45. The PMA Service Interface is defined in 55.2.2 and the MDI is defined in 55.8.

55.2.1 Management Function Interface

10GBASE-T uses the following service primitives to exchange status indications and control signals across the Management Function Interface as specified in Clause 28:

Editor's note: These primitives have been taken from Clause 40 (1000BASE-T). Are these valid for 10GBASE-T? If we need changes to these, please provide comments.

PMA_LINK.request (link_control)

PMA_LINK.indicate (link_status)

55.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

55.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL.PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

55.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

55.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 55.4.2.5.

55.2.1.2 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation algorithm about the status of the underlying link.

55.2.1.2.1 Semantics of the primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY(PB)	The Link Monitor function indicates that a 10GBASE-T link is intact and ready to be established.
OK(PB)	The Link Monitor function indicates that a valid 10GBASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

PB is a parameter that can take any value from 1 to TBD and indicates the power backoff mode.

55.2.1.2.2 When generated

The PMA generates this primitive continuously to indicate the value of link_status in compliance with the state diagram given in Figure 55–20.

55.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is TBD.

55.2.2 PMA Service Interface

10GBASE-T uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

Editor's note: These primitives have been taken from Clause 40. Are these valid for 10GBASE-T? If we need changes to these, please provide comments.

PMA_TXMODE.indicate (tx_mode)

PMA_CONFIG.indicate (config)

PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indicate (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_RXSTATUS.indicate (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

The use of these primitives is illustrated in Figure 55–4.

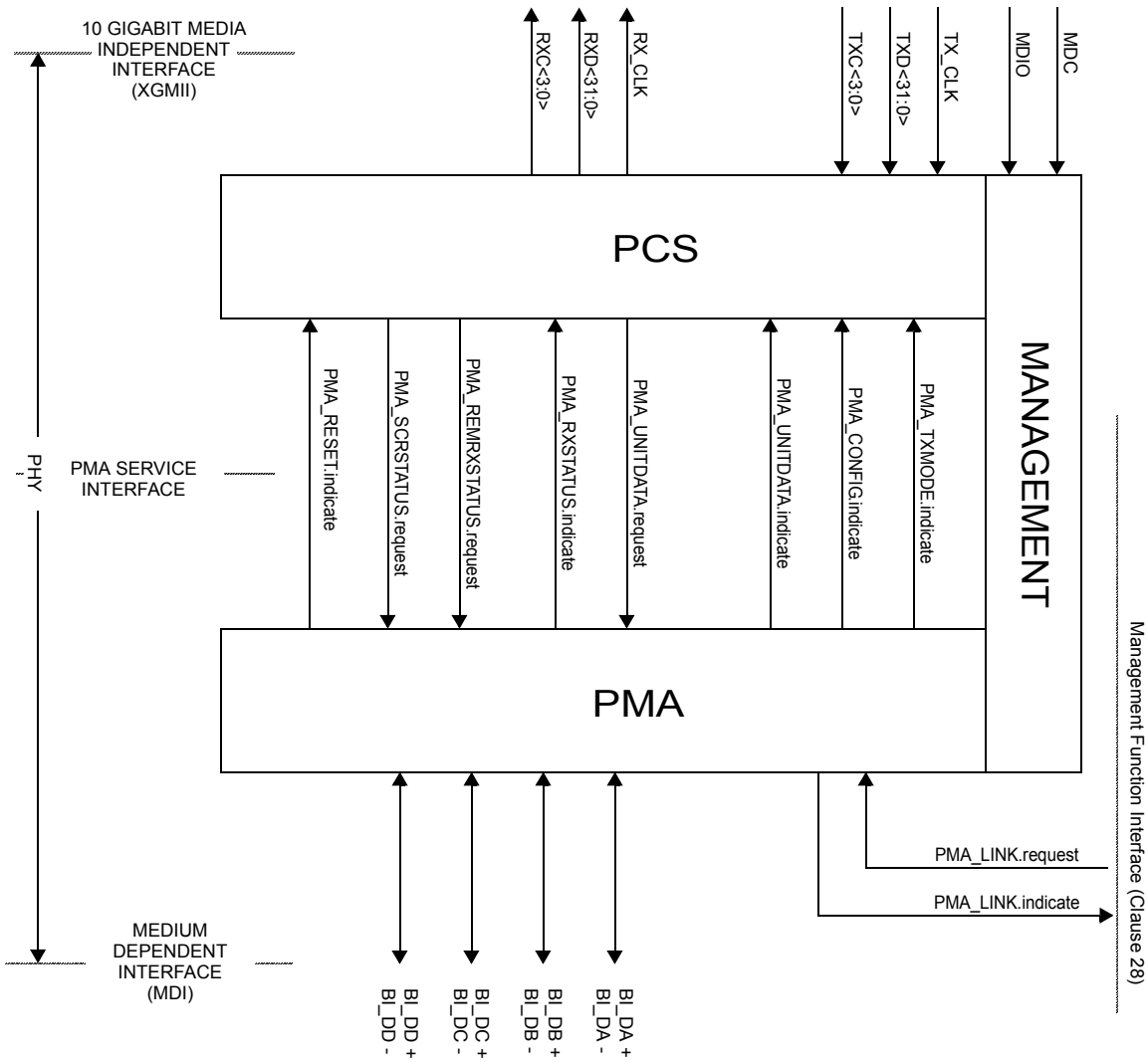


Figure 55–4—10GBASE-T service interfaces

55.2.3 PMA_TXMODE.indicate

The transmitter in a 10GBASE-T link normally sends over the four pairs, four dimensional symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

55.2.3.1 Semantics of the primitive

PMA_TXMODE.indicate (tx_mode)

PMA_TXMODE.indicate specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of four dimensional symbols representing an XGMII data stream in normal mode.

SEND_T This value is continuously asserted in case transmission of sequences of code-groups representing the startup mode is to take place.

SEND_Z This value is continuously asserted in case transmission of zeros is required.

55.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indicate messages continuously.

55.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 55.3.2.2.

55.2.4 PMA_CONFIG.indicate

Each PHY in a 10GBASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (55.6.1). The result of this negotiation is provided to the PMA.

55.2.4.1 Semantics of the primitive

PMA_CONFIG.indicate (config)

PMA_CONFIG.indicate specifies to PCS and PMA Transmit via the parameter config whether the PHY must operate as a MASTER PHY or as a SLAVE PHY and the power backoff level at which the transmitter shall operate. The parameter config can take on one of the following two values of the form:

MASTER(PB) This value is continuously asserted when the PHY must operate as a MASTER PHY.

SLAVE(PB) This value is continuously asserted when the PHY must operate as a SLAVE PHY.

PB can take any value from 1 to TBD to indicate the power backoff mode.

55.2.4.2 When generated

PMA generates PMA_CONFIG.indicate messages continuously.

55.2.4.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

55.2.5 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 55.3.2.2 to represent XGMII data and control streams or other sequences.

55.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. Each symbol may take on one of the values in the set {-11,-9, -7, -5, -3, -1, 1, 3, 5, 7, 9, 11}.

The symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

55.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_4D) synchronously with every transmit clock cycle.

55.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with the Tomlinson Harashima Precoder (THP), the transmit filter and other specified PMA transmit processing. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD for cancelling the echo and Near End Cross Talk (NEXT).

55.2.6 PMA_UNITDATA.indicate

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

55.2.6.1 Semantics of the primitive

PMA_UNITDATA.indicate (rx_symb_vector)

During reception the PMA_UNITDATA.indicate simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symb_vector parameter takes on the form:

SYMB_4D A vector of the four 1-D symbols that is the receiver's best estimate of the information bits that were sent by the remote transmitter across the four pairs.

55.2.6.2 When generated

The PMA generates PMA_UNITDATA.indicate (SYMB_4D) messages synchronously every 4 symbols received at the MDI. The nominal rate of the PMA_UNITDATA.indicate primitive is 800 MHz, as governed by the recovered clock.

55.2.6.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

55.2.7 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

Editor's note: Do we need to create a similar primitive to communicate status of PCS descrambler?

55.2.7.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The descrambler has achieved synchronization.
NOT_OK	The descrambler is not synchronized.

55.2.7.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

55.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.4.2.3, 55.4.2.4, and 55.4.6.1.

55.2.8 PMA_RXSTATUS.indicate

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams.

55.2.8.1 Semantics of the primitive

PMA_RXSTATUS.indicate (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

55.2.8.2 When generated

PMA Receive generates PMA_RXSTATUS.indicate messages continuously on the basis of signals received at the MDI.

55.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–19 and in subclauses 55.2 and 55.4.6.2.

55.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementor. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS receive decoding is achieved.

55.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

55.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis on signals received at the MDI.

55.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–19.

55.2.10 PMA_RESET.indicate

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indicate primitive can take on one of two values:

TRUE	Reset is enabled.
FALSE	Reset is not enabled.

55.2.10.1 When generated

The PMA Reset function is executed as described in 55.4.2.1.

55.2.10.2 Effect of receipt

The effect of receipt of this primitive is specified in 55.4.2.1.

55.3 Physical Coding Sublayer (PCS)

Editor's note: Clause 49 (PCS for 64/66B, type 10GBASE-R) has been used as the starting point for most of the PCS for this draft of 10GBASE-T in addition to some sections of Clause 40 (1000BASE-T).

55.3.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-T PCS to transfer information to and from a PCS client. The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

55.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 55–5, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 55–5. Management is specified in Clause 30.

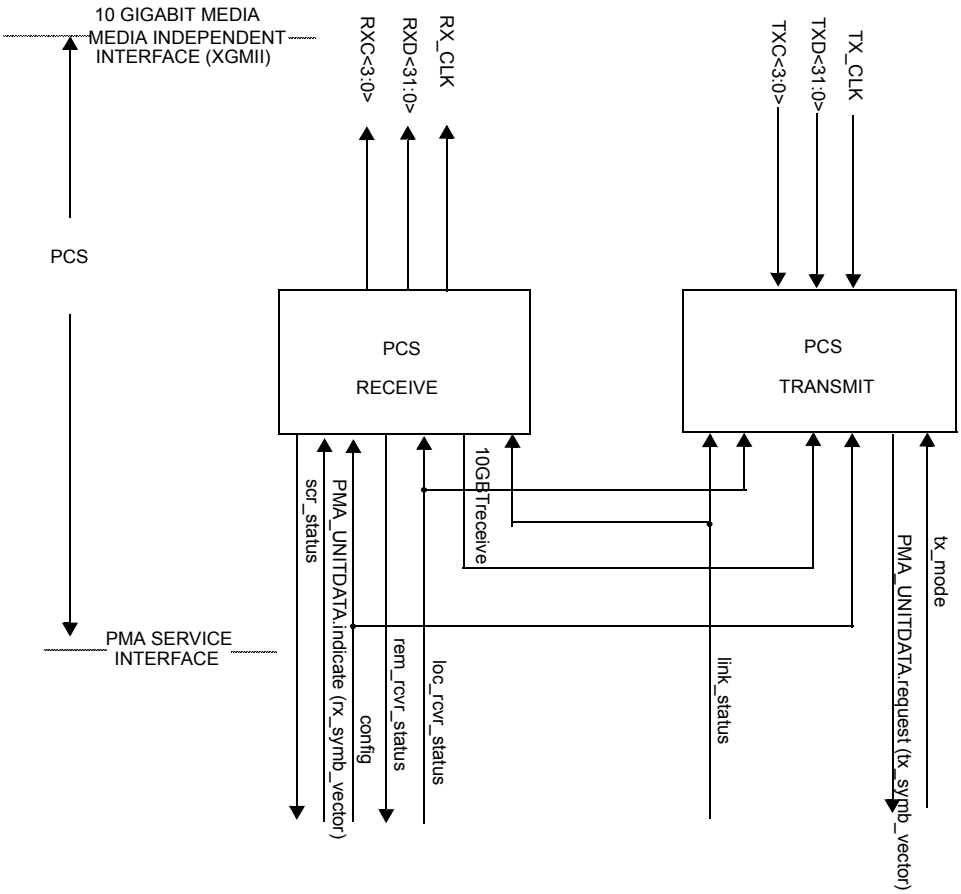


Figure 55–5—PCS reference diagram

55.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

55.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 55–15.

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 64B/65B block is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates 65B blocks based upon the TXD <31:0> and TXC <3:0> signals on the XGMII. The subsequent functions of the PCS Transmit process then pack the resulting bits into Low Density Parity Check (LDPC) blocks and then put N (N is either 1, 2, 3 or 4) LDPC blocks into a frames. Transmit data-units are sent to the PMA or service interface via the PMA_UNITDATA.request primitive, respectively.

When the receive channel is in normal mode, the PCS Synchronization process continuously monitors PMA_SIGNAL.indicate(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indicate primitive. It attains frame and block synchronization based on the LDPC frame synchronization headers and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the sync_status flag to indicate whether the PCS has obtained synchronization.

When the PCS Synchronization process has obtained synchronization, the LDPC Block Error Rate (LBER) monitor process monitors the signal quality asserting hi_lber if excessive errors are detected. When sync_status is asserted and hi_lber is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is 1.25 ns. If a PMA_TXMODE.indicate message has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

Editor's note: Clause 49 transports idle as 64B/65B control payload. Should we preserve a PMA idle mode with binary level PAM for PMA training?

If a PMA_TXMODE.indicate message has the value SEND_T, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values {-7, 7}

are transmitted in this case. This value keeps the power in the training mode the same as the power in normal mode. Training mode encoding also takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner.

In the normal mode of operation, the PMA_TXMODE.indicate message has the value SEND_N, and the PCS Transmit function uses a 65B-LDPC coding technique to generate at each symbol period code-groups that represent data or control. During transmission, the 65B bits are scrambled by the PCS using a PCS scrambler, then encoded into a code-group of four dimensional symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a block LDPC encoder.

55.3.3 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into frames of LDPC blocks, and vice versa, using a 65B-LDPC coding scheme. The LDPC frame synchronization headers of the blocks allow establishment of block boundaries by the PCS Synchronization process. Blocks are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks as provided by the rules in 55.3.4.

55.3.4 65B-LDPC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encoding defined by the transmission code ensure that sufficient information is present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any LDPC block errors that may occur during transmission and reception of information. In addition, the synchronization headers of the code enable the receiver to achieve block alignment on the incoming PHY bit stream.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 55–6 for transmit and Figure 55–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 55.3.4.3 for information on how blocks containing control characters are mapped.

55.3.4.1 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/ and /T/ are labeled C_0 to C_7. The control character for ordered_set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

Two consecutive XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfers.

Contents of block type fields, data octets and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1e is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<64:0> and RxB<64:0> respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

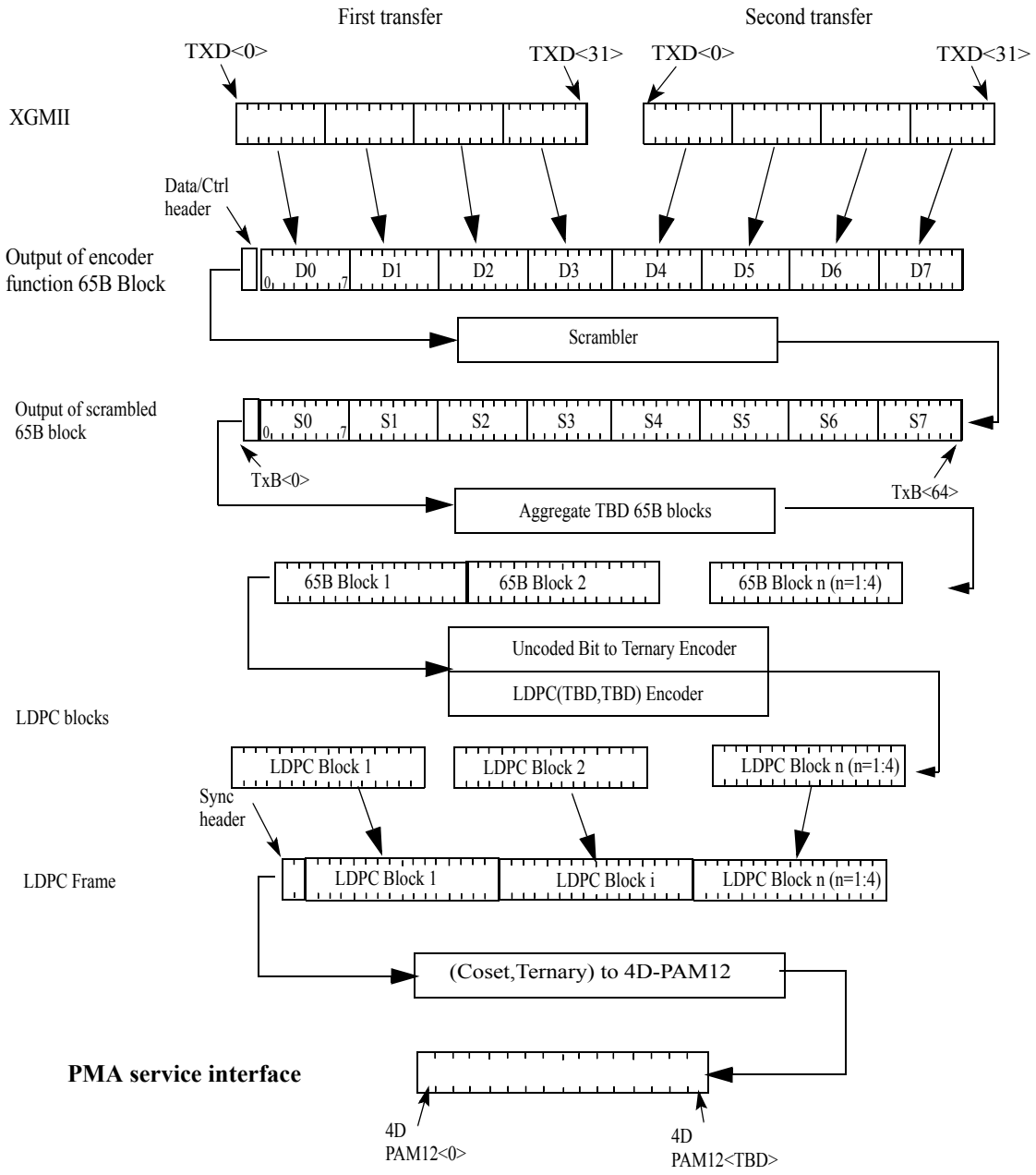


Figure 55–6—PCS Transmit Bit Ordering

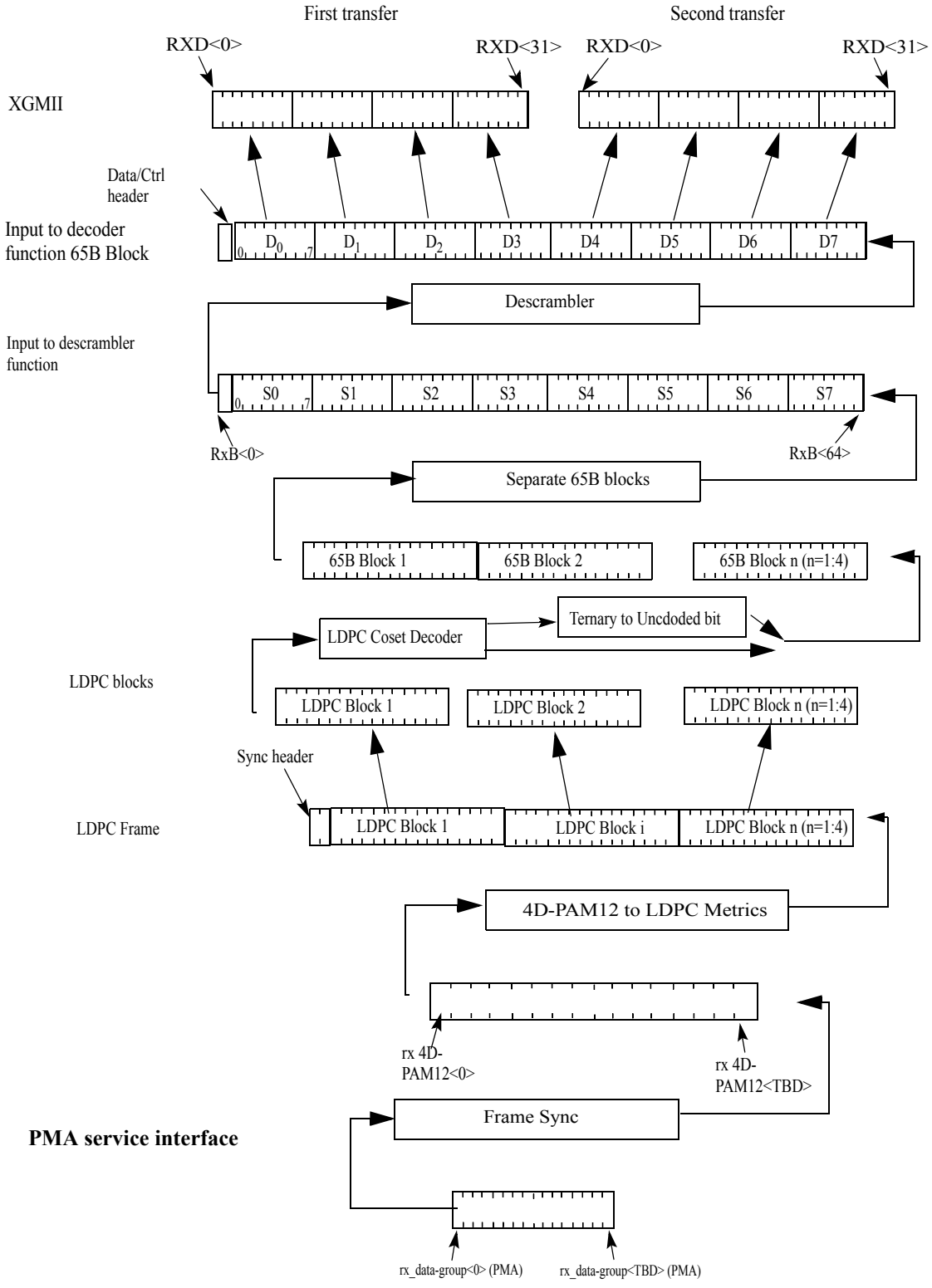


Figure 55–7—PCS Receive Bit Ordering

55.3.4.2 Transmission order

Block bit transmission order is illustrated in Figure 55–6 and Figure 55–7. Note that these figures show the mapping from XGMII to 64B/65B block for a block containing eight data characters.

55.3.4.3 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code or a 4-bit O Code. Each control block contains eight characters.

The format of the blocks is as shown in Figure 55–8. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown in normal hexadecimal. For example the block type field 0x1e is sent as 01111000 representing bits 1 through 8 of the 65 bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[1] are reserved.

55.3.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-T PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-T PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-T PCS encodes the ordered_set control codes using a combination of the block type field and a 4-bit O code for each ordered_set. The 10GBASE-T PCS encodes each of the other control characters into a 7-bit C code).

The control characters and their mappings to 10GBASE-T control codes and XGMII control codes are specified in Table 55–1. All XGMII and 10GBASE-T control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

55.3.4.5 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 10 Gigabit Ethernet uses one kind of ordered_set: the sequence ordered_set (see 46.3.4). The sequence ordered_set control character is denoted /Q/. An addi-

[1]The block type field values have been chosen to have a 4-bit Hamming distance between them. The only unused value which maintains the Hamming distance is 0x00.

Input Data	data ctrl bit	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\,C_1\,C_2\,C_3/O_4\,D_5\,D_6\,D_7$	1	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\,C_1\,C_2\,C_3/S_4\,D_5\,D_6\,D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/S_4\,D_5\,D_6\,D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/O_4\,D_5\,D_6\,D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/C_4\,C_5\,C_6\,C_7$	1	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	1	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	1	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	1	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	1	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	1	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 55–8—64B/65B Block Formats

tional ordered_set, the signal ordered_set, has been reserved and it begins with another control code. The 4-bit O field encodes the control code. See Table 55–1 for the mappings.

55.3.4.6 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 55–1.
c) Any O code contains a value not in Table 55–1.
d) The set of eight XGMII characters does not have a corresponding block format in Figure 55–8.

55.3.4.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

Table 55–1—Control Codes

Control Character	Notation	XGMII Control Code	10GBASE-T Control Code	10GBASE-T O Code	8B/10B Code[a]
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
start	/S/	0xfb	Encoded by block type field		K27.7
terminate	/T/	0xfd	Encoded by block type field		K29.7
error	/E/	0xfe	0x1e		K30.7
Sequence ordered_set	/Q/	0x9c	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/[b]	0x1c	0x2d		K28.0
reserved1		0x3c	0x33		K28.1
reserved2	/A/	0x7c	0x4b		K28.3
reserved3	/K/	0xbc	0x55		K28.5
reserved4		0xdc	0x66		K28.6
reserved5		0xf7	0x78		K23.7
Signal ordered_set[c]	/Fsig/	0x5c	Encoded by block type field plus O code	0xF	K28.2

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.
[b]The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.
[c]Reserved for INCITS T11 Fibre Channel use.

55.3.4.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<0:7> and RXD<0:7>). Receipt of an /S/ on any other octet of TxD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

55.3.4.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

55.3.4.10 ordered_set (/O/)

The ordered_set control characters (/O/) indicate the start of an ordered_set. There are two kinds of ordered sets: the sequence ordered_set and the signal ordered_set (which is reserved). When it is necessary to designate the control character for the sequence ordered_set specifically, /Q/ will be used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered_set.

Sequence ordered_sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered_sets are not deleted for clock compensation.

55.3.4.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. It is also sent when invalid blocks are received. The /E/ allows physical sublayers such as the XGXS and PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 55.3.12.2.3 for further information.

55.3.5 Transmit process

The transmit process generates blocks based upon the TXD<31:0> and TXC<3:0> signals received from the XGMII. Two XGMII data transfers are encoded into each block. It takes TBD PMA_UNITDATA transfers to send a block of data. Therefore, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly TBD1:TBD2, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process will need to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the transmit process state machine. The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

55.3.6 PCS Scrambler.

The payload of the block is scrambled with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 55–9. This implements the scrambler polynomial:[2]

$$G(x) = 1 + x^{39} + x^{58} \quad (55–1)$$

There is no requirement on the initial value for the scrambler. In no case shall the scrambler state be initialized to all zeros. The scrambler is run continuously on all payload bits.

55.3.7 65B-LDPC

The 65B/LDPC adapts between the 65-bit width of the 65B blocks and the 4D-PAM12 width of the PMA. When the transmit channel is operating in normal mode, the 65B-LDPC sends 4D-PAM12 of transmit data at a time via PMA_UNITDATA.request primitives. The UNITDATA.request primitives are fully packed with bits.

[2]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (55–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

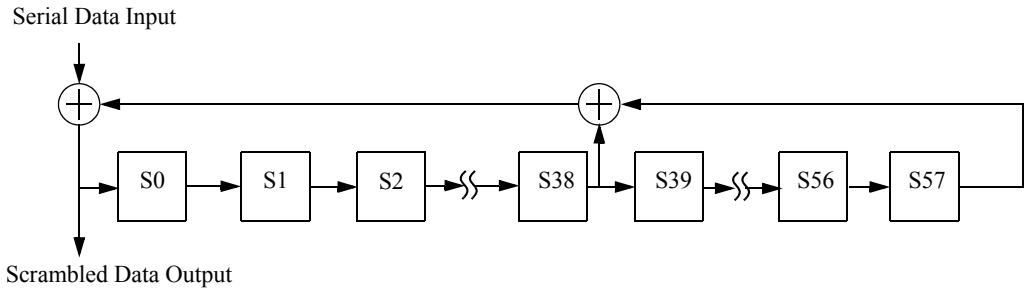


Figure 55–9—Scrambler

55.3.8 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 4D-PAM12 PMA_UNITDATA.request primitives. It shall form a 4D PAM12 stream from the primitives by concatenating requests with the PAMs of each primitive in order from rx_data-group<0> to rx_data-group<TBD> (see Figure 55–7). It obtains lock to the LDPC frames and the 65-bit blocks in the bit stream using the frame sync headers and outputs 65-bit blocks. Lock is obtained as specified in the block lock state machine shown in Figure 55–13.

55.3.9 PCS Descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementation shown in Figure 55–10.

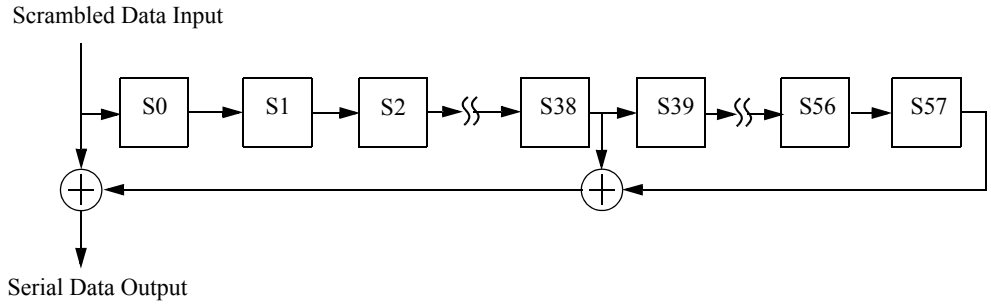


Figure 55–10—Descrambler

55.3.10 Receive function

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed. PCS Receive checks the received framing and signals the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The received 65B-LDPC frames are decoded into blocks of 65-bits to obtain the signals RXD<31:0> and RXC<3:0> for transmission to the XGMII. Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized to a TBD1:TBD2 ratio, the receive process will insert idles, delete idles, or delete sequence ordered sets to adapt between rates. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Transmit functions via the parameter 10GBTreceive.

The receive process decodes blocks as specified in the receive state machine shown in Figure 55–16.

55.3.11 PMA Side-stream scrambler polynomials

Editor's note: For PMA training the side-stream scrambler from 1000BASE-T has been used for this initial draft. This results in two different scramblers, one from Clause 49 for scrambling the 65B blocks and the second from Clause 40 for PAM training. Please provide comments.

The PCS Transmit function employs side-stream scrambling for 2-level PAM PMA training. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indicate message assumes the value of SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 55–11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementor. In no case shall the scrambler state be initialized to all zeros.

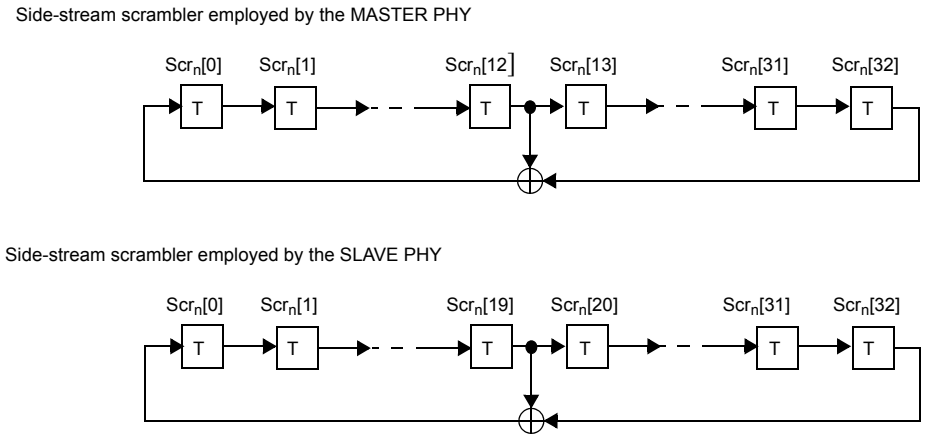


Figure 55–11—A realization of side-stream scramblers by linear feedback shift registers

55.3.11.1 Generation of bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$

TBD.

55.3.11.2 Generation of 4-D symbols TA_n, TB_n, TC_n, TD_n

TBD.

55.3.11.3 Decoding of code-groups

TBD.

55.3.11.4 Receiver descrambler polynomials

The PHY shall descramble the PMA training stream and return the proper sequence of code-groups. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

55.3.12 Detailed functions and state diagrams

55.3.12.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

55.3.12.2 State diagram parameters

55.3.12.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /E/ in all the eight character locations.

IFRAME_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /I/ in all the eight character locations

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing two Local Fault ordered_sets. The Local Fault ordered_set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing two Local Fault ordered sets.

55.3.12.2.2 Variables

config
: The config parameter set by PMA and passed to the PCS via the PMA_CONFIG.indicate primitive. Values: MASTER, SLAVE

lber_test_sh
: Boolean variable that is set true when a new LDPC block is available for testing and false when LBER_TEST_SH state is entered. A new LDPC header is available for testing when the Block Sync process has accumulated enough bits from the PMA to evaluate the header of the next block

block_lock
: Boolean variable that is set true when receiver acquires block delineation

hi_lber
: Boolean variable which is asserted true when the lber_cnt exceeds TBD indicating a bit error ratio >TBD

reset

Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>

Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 55–8. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>

Vector containing two successive XGMII transfers. RXC<0> through RXC<3> for the first transfer are placed in rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are placed in rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are placed in rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

sh_valid

Boolean indication that is set true if received LDPC block has valid parity bits.

signal_ok

Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indicate(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done

Boolean variable that is asserted true when the SLIP requested by the Block Lock State Machine has been completed indicating that the next candidate frame sync position can be tested.

test_sh

Boolean variable that is set true when a new sync header is available for testing and false when TEST_SH state is entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA to evaluate the header of the next block

tx_coded<64:0>

Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 55–8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>

Vector containing two successive XGMII transfers. TXC<0> through TXC<3> for the first transfer are placed in tx_raw<0> through tx_raw<3>, respectively. TXC<0> through TXC<3> for the second transfer are placed in tx_raw<4> through tx_raw<7>, respectively. TXD<0> through TXD<31> for the first transfer are placed in tx_raw<8> through tx_raw<39>, respectively. TXD<0> through TXD<31> for the second transfer are placed in tx_raw<40> through tx_raw<71>, respectively.

55.3.12.2.3 Functions

DECODE(rx_coded<64:0>)

In the PCS Receive process, this function takes as its argument TBD values of rx_symb_vector from the PMA and decodes the 65B-LDPC bit vector returning TBD vectors rx_raw<71:0> which is sent to the XGMII. The DECODE function shall decode the block as specified in 55.3.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning TBD values of tx_symb_vector. The ENCODE function shall encode the block as specified in 55.3.4.

R_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 65-bit rx_coded vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains a sync header of 1 and one of the following:

a) A block type field of 0x1e and eight valid control characters other than /E/;

b) A block type field of 0x2d or 0x4b, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a sync header of 1 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a sync header of 1, a block type field of 0x87, 0x99, 0xaa, 0xb4, 0xcc, 0xd2, 0xe1 or 0xff and all control characters are valid.

D; The vector contains a sync header of 0.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-R control code specified in Table 55–1. A valid O code is one containing an O code specified in Table 55–1.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP

Causes the next candidate 65B-LDPC block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible symbol positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains one of the following:
a) eight valid control characters other than /O/, /S/, /T/ and /E/;
b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;
c) two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 55–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 55–1.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT

Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

55.3.12.2.4 Counters

lber_cnt
: Count up to a maximum of TBD of the number of invalid LDPC codeword within the current TBD μs period.

sh_cnt
: Count of the number of sync headers checked within the current TBD LDPC frame window.

sh_invalid_cnt
: Count of the number of invalid sync headers within the current TBD LDPC frame window.

55.3.12.2.5 Timers

symb_timer
: Continuous timer: The condition symb_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.
Duration: TBD ns nominal. (See clock tolerance in 55.5.6.2.)

Symb-timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

55.3.12.3 Messages

PMA_UNITDATA.indicate (rx_symb_vector)
: A signal sent by PMA Receive indicating that a vector of four symbols is available in rx_symb_vector. (See 55.2.6.)

PMA_UNITDATA.request (tx_symb_vector)
: A signal sent to PMA Transmit indicating that a vector of four PAM12 symbols is available in tx_symb_vector. (See 55.2.5.)

PUDI
: Alias for PMA_UNITDATA.indicate (rx_symb_vector).

PUDR
: Alias for PMA_UNITDATA.request (tx_symb_vector).

STD
: Alias for symb_timer_done.

55.3.12.4 State diagrams

The Lock state machine shown in Figure 55–13 determines when the PCS has obtained lock to the received data stream. The LBER Monitor state machine shown in Figure 55–14 monitors the received signal for high LDPC block error ratio.

The Transmit state machine shown in Figure 55–15 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the Transmit state machine sends Local Fault ordered sets when reset is asserted, the scrambler and 65B-LDPC may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the PMA service interface.

The Receive state machine shown in Figure 55–16 controls the decoding of received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of Lock, LBER Monitor, Transmit and Receive as specified in these state machines.

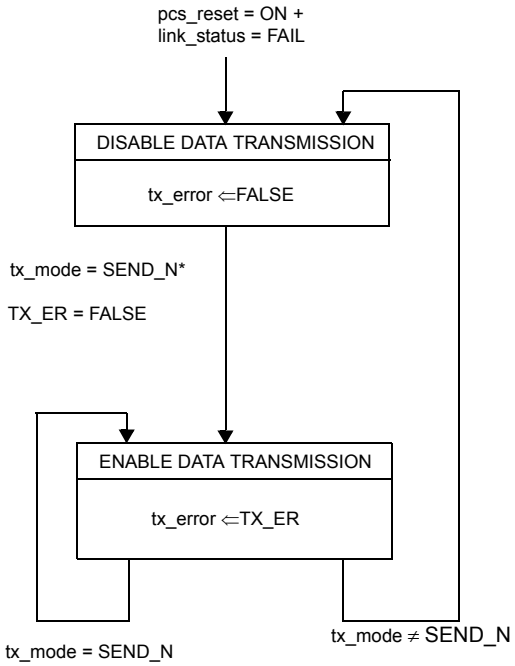


Figure 55–12—PCS Data Transmission Enabling state diagram

55.3.13 PCS Management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

55.3.13.1 Status

PCS_status:
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_lber is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_lber:
: Indicates the state of the hi_lber variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

55.3.13.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

lber_count:
: TBD-bit counter that counts each time LBER_BAD_SH state is entered. This counter is reflected

in MDIO register bits 3.33.13:8. Note that this counter counts a maximum of TBD counts per TBD μs since the LBER_BAD_SH can be entered a maximum of TBD times per TBD μs window.

errored_block_count:

TBD-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0.

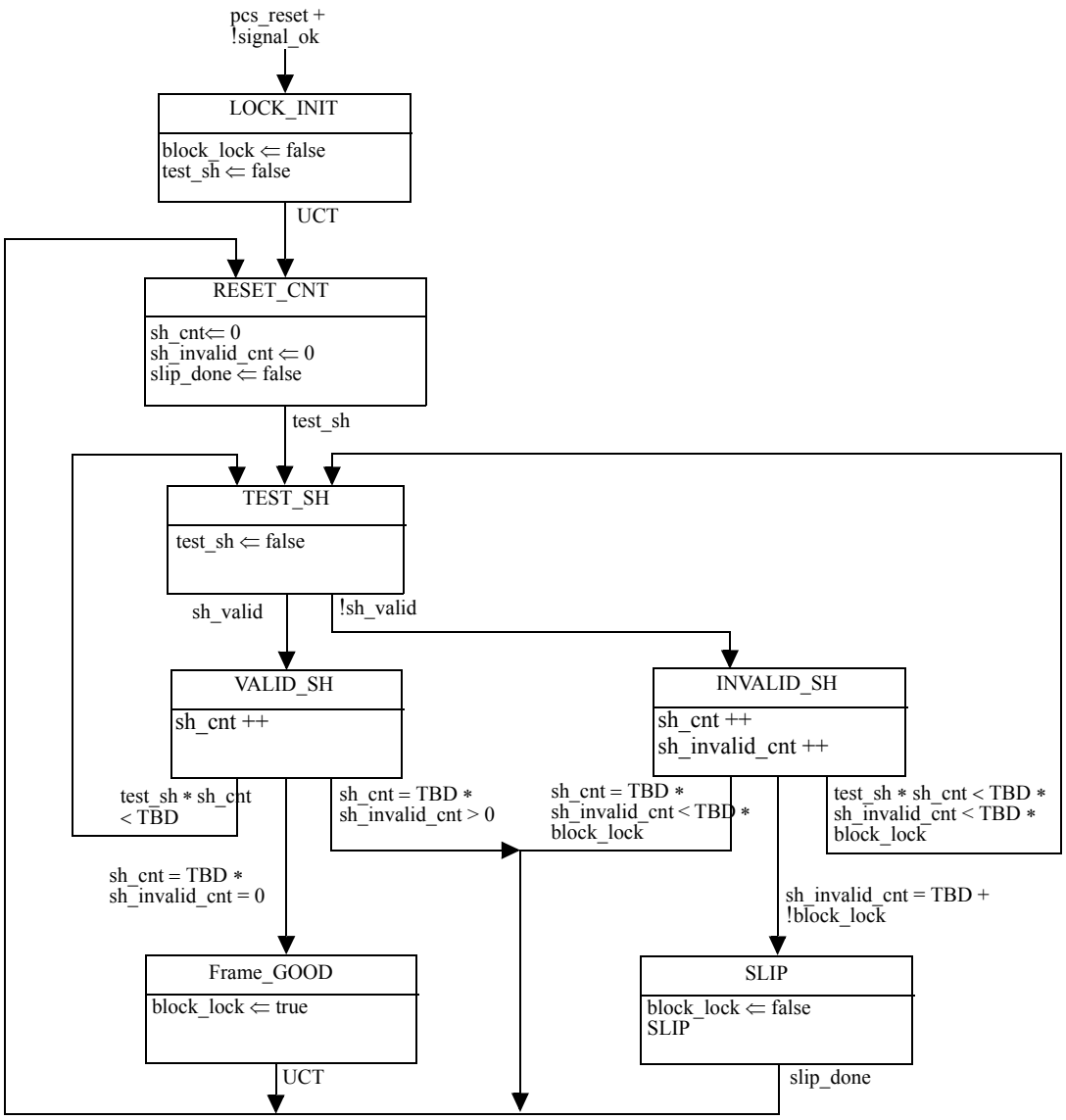


Figure 55–13—Lock state machine

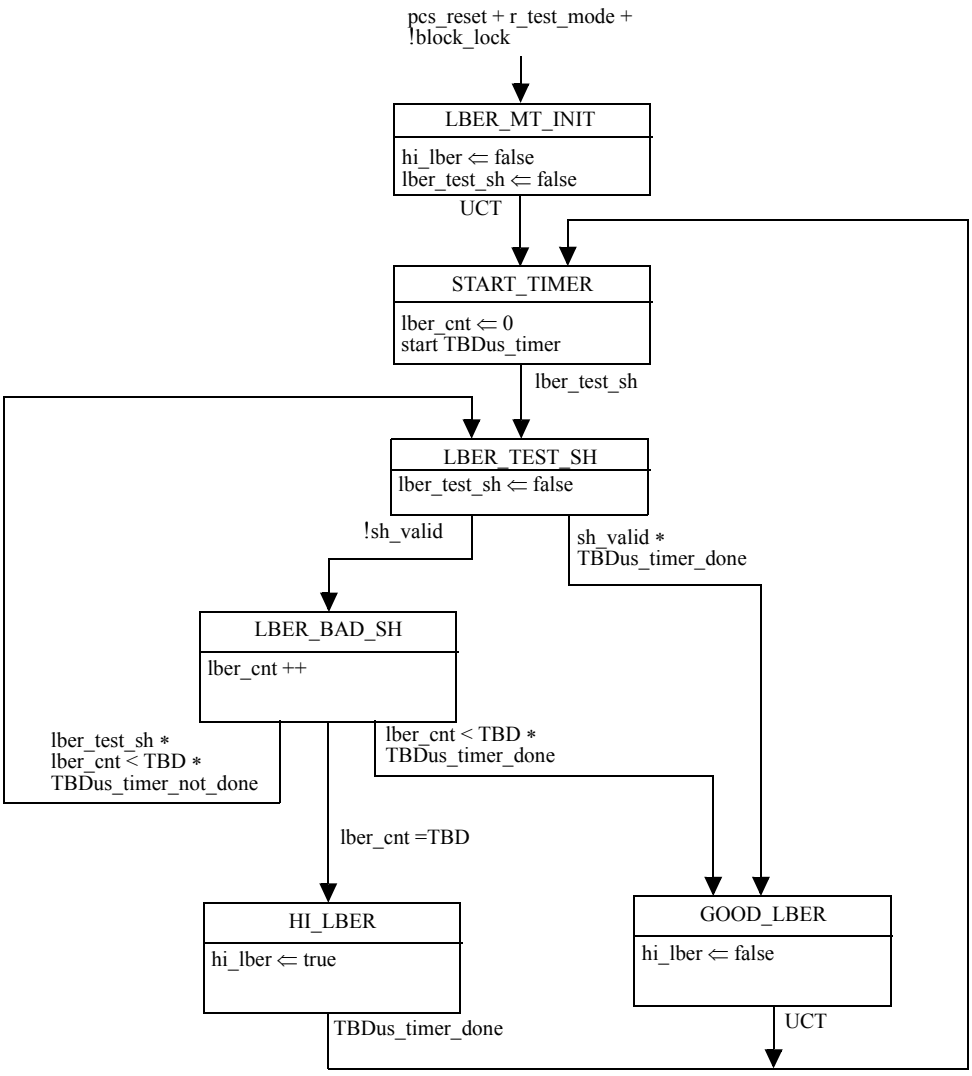


Figure 55–14—LBER monitor state machine

55.3.13.3 Loopback

Editor's note: PCS for 1000BASE-T does not appear to include loop back modes. This can be useful. Please comment.

The PCS shall be placed in Loopback mode when the Loopback bit in MDIO register TBD is set to a logic one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of TBD PAM12 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

55.4 Physical Medium Attachment (PMA) sublayer

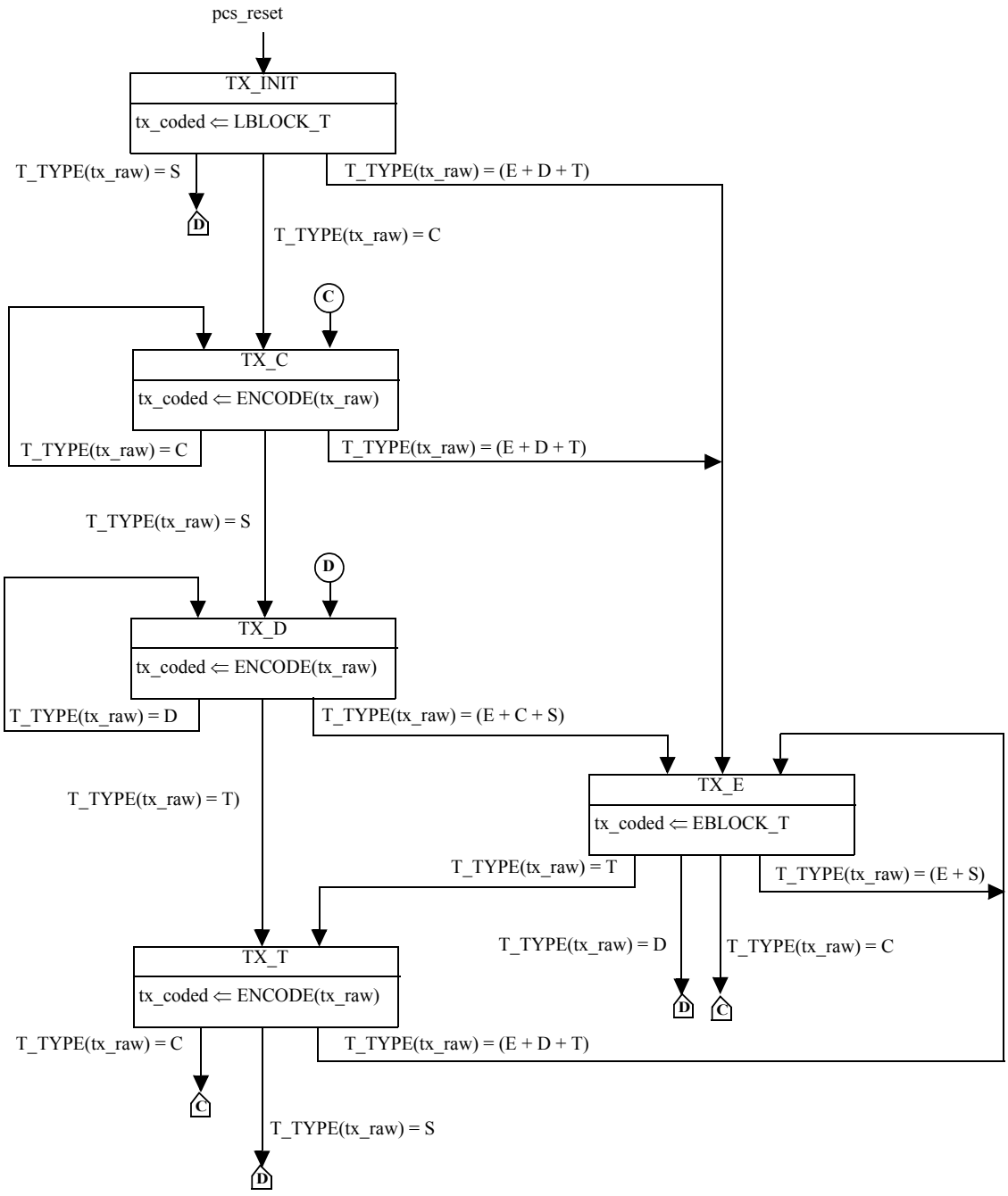


Figure 55–15—PCS Transmit state machine

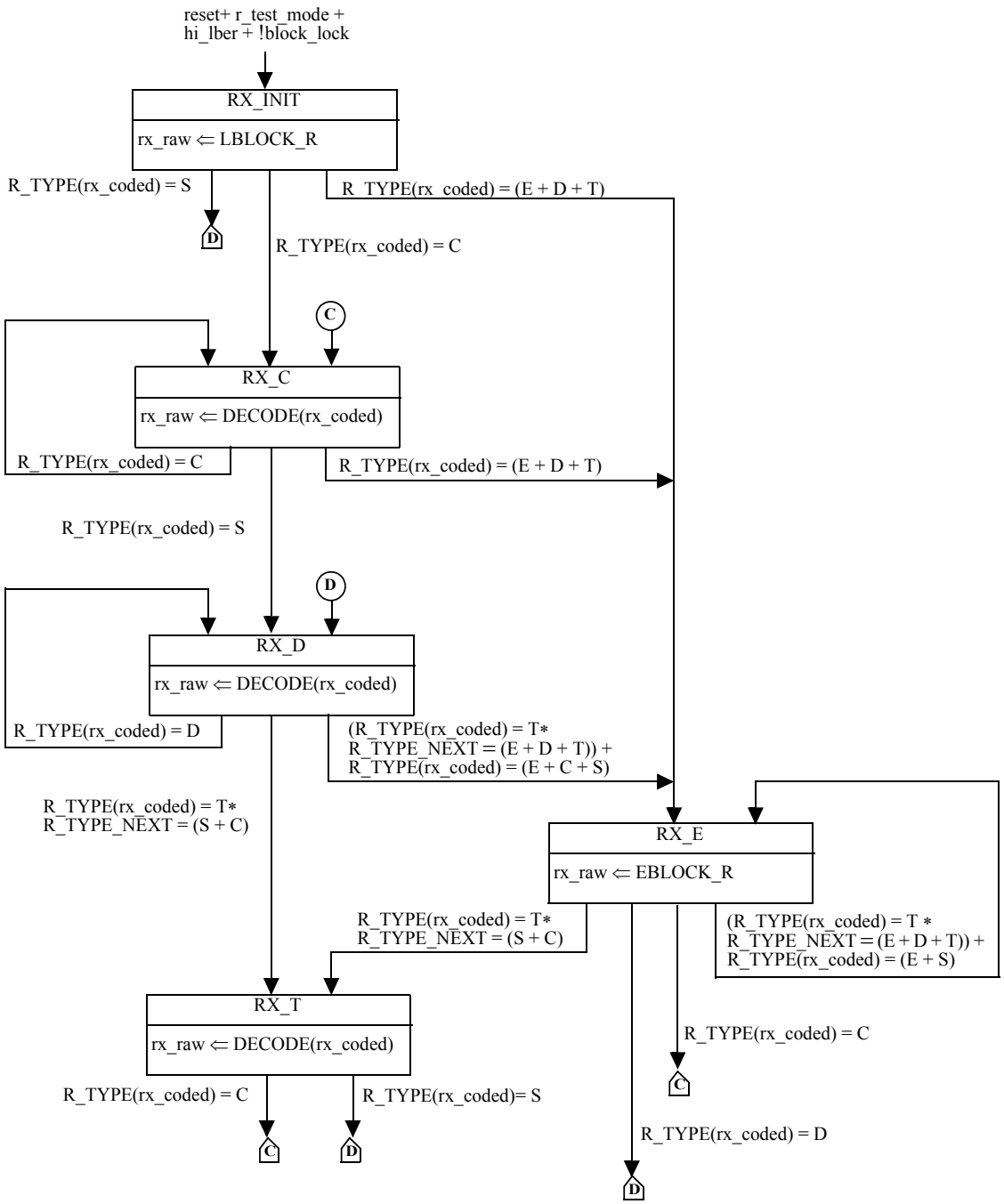


Figure 55–16—PCS Receive state machine

Editor's note: Clause 40 has been used as the starting point for most of the PMA for this initial draft of 10GBASE-T. Please provide comments.

55.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 55.2.2 to the 10GBASE-T baseband medium, specified in 55.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 55.8.

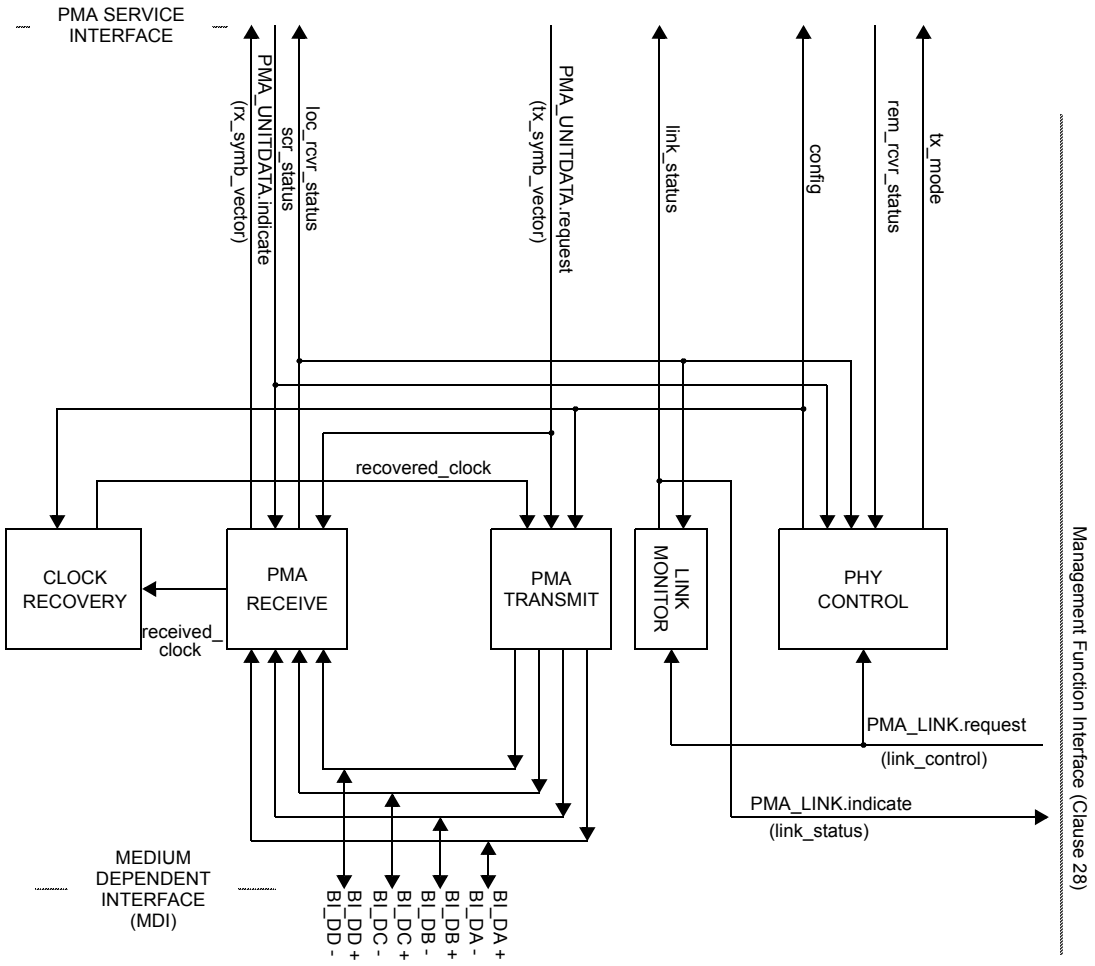


Figure 55–17—PMA reference diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

55.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor,

and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 55–17, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 55–17. The management interface and its functions are specified in Clause 22.

Editor's note: Should we include references to Clause 28 and Clause 30 in addition to Clause 22?

55.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see Clause 46.TBD)
b) The receipt of a request for reset from the management entity

PMA Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

55.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively after processing with the THP, TBD transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 55.4.3.1, and shall comply with the electrical specifications given in 55.5.

When the PMA_CONFIG.indicate parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 55.5.4.1. The MASTER/SLAVE relationship may include loop timing (TBD). If loop timing is implemented and the PMA_CONFIG.indicate parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 55.4.2.6 while meeting the jitter requirements of 55.5.4.1. If loop timing is not implemented, the SLAVE PHY clocking is identical to the MASTER PHY clocking.

55.4.2.3 PMA Receive function

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 55.4.3.2. The PMA shall translate the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DB into the PMA_UNITDATA.indicate parameter rx_symb_vector with equivalent LBER of less than 10^{-TBD} over a channel meeting the requirements of 55.7.

Editor's note: Following a related concept to 1000BASE-T we have assumed a frame/block error rate instead of a bit error rate measurement. As a reference, Clause 40 specifies FER=1e-7 for packets of size 128bytes.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

55.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 55–19 (TBD).

During Auto-Negotiation PHY Control is in the DISABLE 10GBASE-T TRANSMITTER state and the transmitters are disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the SLAVE SILENT state. Upon entering this state, the maxwait timer is started and PHY Control forces transmission of zeros by setting tx_mode=SEND_Z. The transition out of the SLAVE SILENT state depends on whether the PHY is operating in MASTER or SLAVE mode. In MASTER mode, PHY Control transitions immediately to the PMA TRAINING state. In SLAVE mode, PHY Control transitions to the TRAINING state only after the SLAVE PHY converges its decision feedback equalizer (DFE), acquires timing, and acquires its descrambler state, and sets scr_status=OK**.**

For the SLAVE PHY, the final convergence of the adaptive filter parameters is completed in the TRAINING state. The MASTER PHY performs all its receiver convergence functions in the TRAINING state. Upon entering the PMA TRAINING state, the minwait_timer is started and PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T. After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the minwait_timer expires and the condition loc_rcvr_status=OK is satisfied, PHY Control transitions into TBD.

The normal mode of operation corresponds to the SEND PCS DATA state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 55.3.2.1.

55.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 55–20.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 10GBASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

55.4.2.6 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the LDPC block-error rate indicated in 55.4.2.3 is achieved. The received clock signal must be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

55.4.3 MDI

Communication through the MDI is summarized in 55.4.3.1 and 55.4.3.2.

55.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is Pulse Amplitude Modulation. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$b_i = \left(a_i + \sum_k b_{i-k}\alpha_k \right) mod 12$$

$$s(t) = \sum_k b_k h_1(t - kT)$$

In the above equation, a_i represents the PAM12 symbol from the set {-11, -9, -7, -5, -3, -1, 1, 3, 5, 7, 9,11} to be transmitted at time iT, α_k denotes the THP coefficients, and $h_1(t)$ denotes the system symbol response at the MDI. The THP coefficients shall be selected from a predetermined set and shall be fixed after startup. This symbol response shall comply with the electrical specifications given in 55.5.

55.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_k a_{k,\,agmt} h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel between the transmit symbol source and the receive MDI and $w(t)$ is a term that represents the contribution of various noise sources. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD shall be processed within the PMA Receive function to yield the received symbols rx_symb_vector.

55.4.4 Automatic MDI/MDI-X Configuration

Automatic MDI/MDI-X Configuration is intended to eliminate the need for crossover cables between similar devices. Implementation of an automatic MDI/MDI-X configuration is required for 10GBASE-T devices. The automatic configuration method used shall comply with the following specifications. The assignment of pin-outs for a 10GBASE-T crossover function cable is shown in Table 55–9 in 55.8.

55.4.4.1 Description of Automatic MDI/MDI-X state machine

The Automatic MDI/MDI-X state machine facilitates switching the BI_DA(C)+ and BI_DA(C)– with the BI_DB(D)+ and BI_DB(D)– signals respectively prior to the auto-negotiation mode of operation so that fast link pulses can be transmitted and received in compliance with Clause 28 Auto-Negotiation specifications. The correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. This algorithm uses an 11-bit Linear Feedback Shift Register (LFSR) to create a pseudo-random sequence that each end of the link uses to determine its proposed configuration. Upon making the selection to either MDI or MDI-X, the node waits for a specified amount of time while evaluating its receive channel to determine whether the other end of the link is sending link pulses or PHY-dependent data. If link pulses or PHY-dependent data are detected, it remains in that configuration. If link pulses or PHY-dependent data are not detected, it increments its LFSR and makes a decision to switch based on the value of the next bit. The state machine does not move from one state to another while link pulses are being transmitted.

55.4.4.2 Pseudo-random sequence generator

One possible implementation of the pseudo-random sequence generator using a linear-feedback shift register is shown in Figure 55–18. The bits stored in the shift register delay line at time n are denoted by S[10:0]. At each sample period, the shift register is advanced by one bit and one new bit represented by S[0] is generated. Switch control is determined by S[10].

Editor's note: This scrambler has been taken from Clause 40. This results in a third different scrambler, in addition to the one from Clause 49 for scrambling the 65B blocks and the second from Clause 40 for PAM training. Please provide comments.

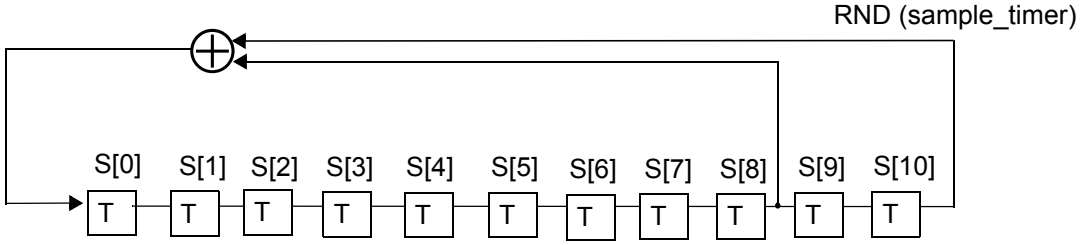


Figure 55–18—Automatic MDI/MDI-X linear-feedback shift register

55.4.5 State variables

55.4.5.1 State diagram variables

config

The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indicate primitive.

Values: MASTER or SLAVE

link_control

This variable is defined in 28.2.6.2.

Link_Det

This variable indicates linkpulse = true or link_status = READY has occurred at the receiver since the last time sample_timer has been started.

Values: TRUE: linkpulse = true or link_status = READY has occurred since the last time sample_timer has been started.

FALSE: otherwise

55.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop timer” is asserted.

A_timer

An asynchronous (to the Auto-Crossover State Machine) free-running timer that provides for a relatively arbitrary reset of the state machine to its initial state. This timer is used to reduce the probability of a lock-up condition where both nodes have the same identical seed initialization at the same point in time.

Values: The condition A_timer_done becomes true upon timer expiration.

Duration: This timer shall have a period of TBD ± TBD%.

Initialization of A_timer is implementation specific.

maxwait_timer

A timer used to limit the amount of time during which a receiver dwells in the SLAVE SILENT and TRAINING states. The timer shall expire TBD ± TBD ms if config = MASTER or TBD ± TBD ms if config = SLAVE. This timer is used jointly in the PHY Control and Link Monitor stage diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 55–19.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the PMA TRAINING, SEND IDLE, or DATA states. The timer shall expire TBD ± TBDμs after being started.

sample_timer

This timer provides a long enough sampling window to ensure detection of Link Pulses or link_status, if they exist at the receiver.

Values: The condition sample_timer_done becomes true upon timer expiration.

Duration: This timer shall have a period of TBD ± TBD ms.

stabilize_timer

A timer used to control the minimum time that loc_rcvr_status must be OK before a transition to Link Up can occur. The timer shall expire TBD ± TBD μs after being started.

55.4.6 State Diagrams

55.4.6.1 PHY Control state diagram

Editor’s note: Clause 40 has been used as the starting point for this initial PHY Control state diagram with some additional outline THP states. The THP effect in the PHY start-up requires additional input for the Task Force. Please provide comments.

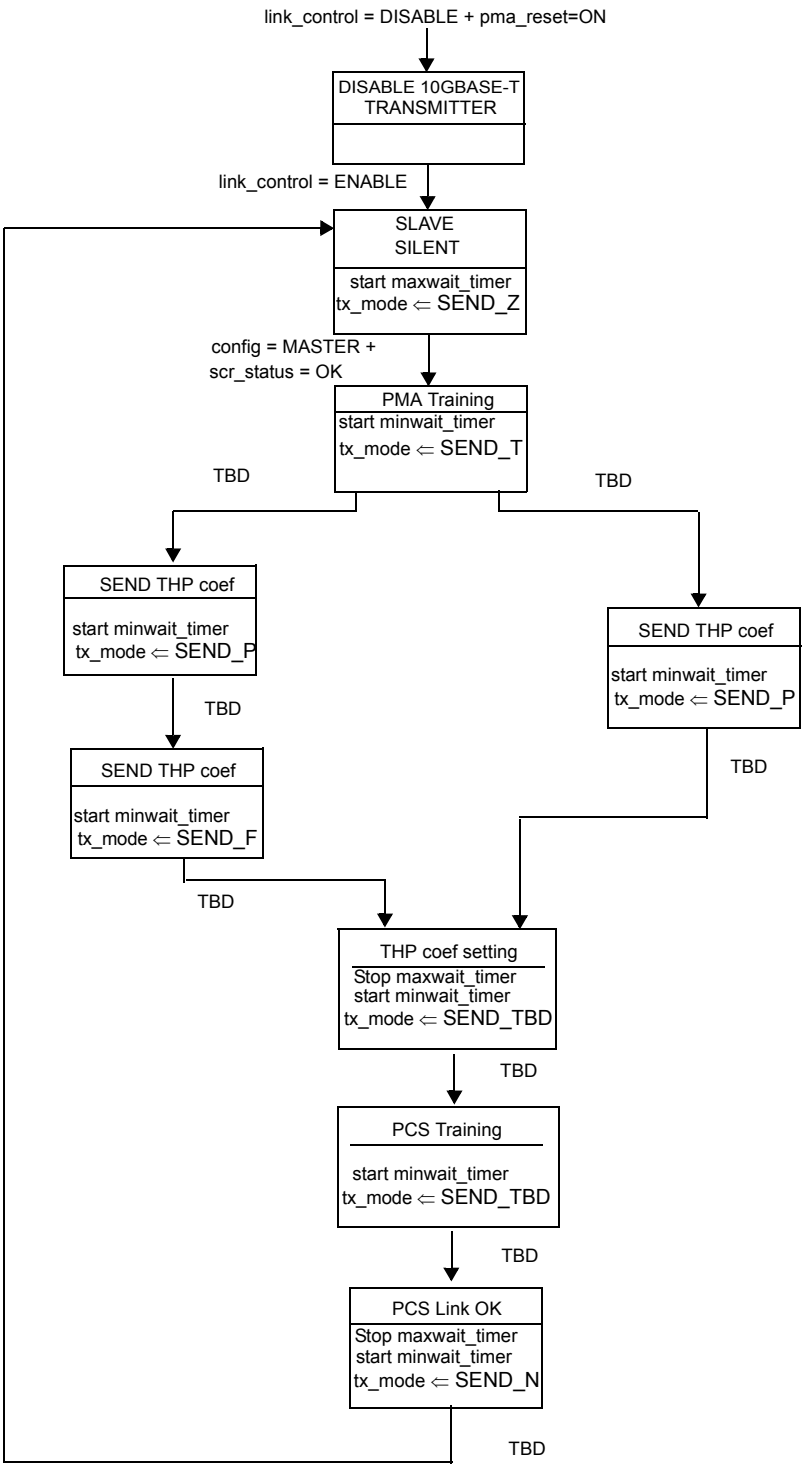
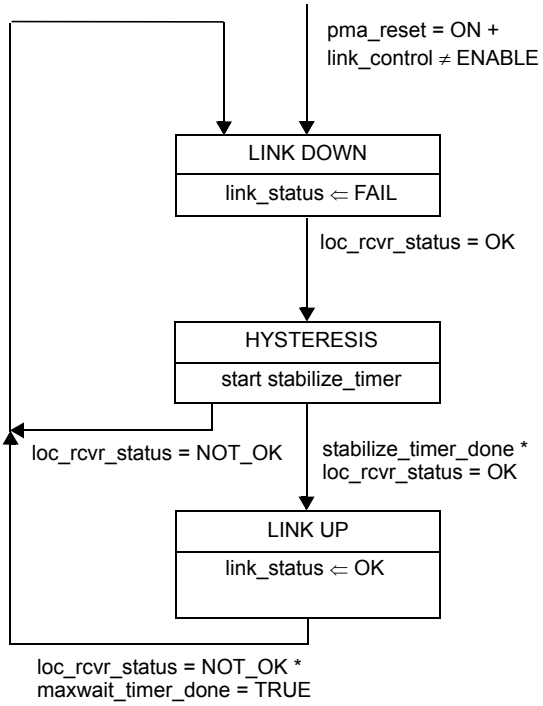


Figure 55–19—PHY Control state diagram

55.4.6.2 Link Monitor state diagram



NOTES
1—maxwait_timer is started in PHY Control state diagram (see Figure 55–19).
2—The variables link_control and link_status are designated as link_control_(10GigT) and link_status_(10GigT), respectively, by the Auto-Negotiation Arbitration state diagram (TBD Figure 28–16).

Figure 55–20—Link Monitor state diagram

55.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

Common-mode tests use the common-mode return point as a reference.

55.5.1 Isolation requirement

The PHY shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

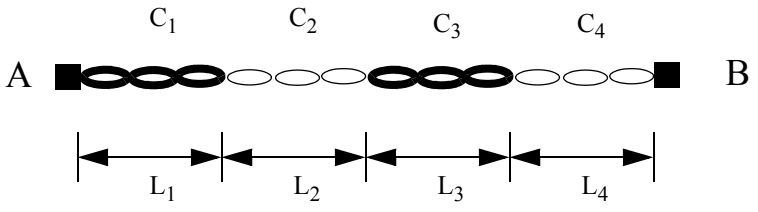
a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950-1: 2001.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950-1: 2001.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950-1: 2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

Editor's note: Text in Clause 55.5.1 copied from 1000BASE-T standard, section 40.6.1.1 with updates to some of the references. Are there additional updates?

55.5.1.1 Test channel

To perform the transmitter MASTER-SLAVE timing jitter tests described in this clause, a test channel is required to ensure that jitter is measured under conditions of poor signal to echo ratio. This test channel shall be constructed by combining 100 Ω and 120 Ω cable segments that both meet or exceed ISO/IEC 11801 augmented by link segment specified in Clause 55.7 for each pair, as shown in Figure 55–21, with the lengths and additional restrictions on parameters described in Table 55–2. The ends of the test channel shall be terminated with connectors meeting or exceeding ISO/IEC 11801:2001 Class E specifications. The return loss of the resulting test channel shall meet the return loss requirements of Clause 55.7.2.3 and the crosstalk requirements of Clause 55.7.3.3.



Identical for each of the four pairs.

Figure 55–21—Test channel topology for each cable pair

Table 55–2—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at TBD freq)
1	$L_1=x_1$	120 ± 5Ω	TBD
2	$L_2=x$	100 ± 5Ω	TBD
3	$L_3=x_2$	120 ± 5Ω	TBD
4	$L_4=y$	100 ± 5Ω	TBD

Editor's Note: —x_1, x_2, x and y as well as the Attenuation numbers are TBD.

55.5.2 Test modes

Note: Fs equals 800 and is the symbol rate in MHz.

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, and transmitted jitter.

For a PHY with an MDIO management interface, these modes shall be enabled by setting ***TBD*** bits(10GBASE-T Control Register) of the MDIO Management register set as shown in Table-55–3. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a MDIO shall provide a means to enable these modes for conformance testing.

Table 55–3—MDIO management register settings for test modes

Bit 1 TBD	Bit 2 TBD	Bit 3 TBD	Mode
0	0	0	Normal operation
0	0	1	Test mode 1—Transmit waveform test
0	1	0	Test mode 2—Transmit jitter test in MASTER mode
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode
1	0	0	Test mode 4—Transmit distortion test
1	0	1	Reserved, operations not identified.
1	1	0	Reserved, operations not identified.
1	1	1	Reserved, operations not identified.

When test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 55.4.3.1 continually from all four transmitters, with the THP turned off:

{{3 +12 followed by 125 0 symbols}, {3 –12 followed by 125 0 symbols},{3 +6 followed by 125 0 symbols},{3 –6 followed by 125 0 symbols}, {128 +12 symbols, 128 –12 symbols, 128 +12 symbols, 128 –12 symbols}, {4096 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the test mode is enabled. A typical transmitter output is shown in Figure 55–22. The transmitter shall time the transmitted symbols from a 800MHz ± 0.01% clock in the MASTER timing mode.

Editor's Note: The above sequence has been adapted from the sequence used in 1000BASE-T. Reasons for this choice are provided in the editor's note in 55.5.3.1, when peak differential output and level accuracy are discussed. This sequence has not been discussed by the task force and alternate proposals for the sequence are welcome. Power back-off of the transmitter when transmitting data over shorter cable lengths has been discussed in the task force. When an appropriate methodology and numbers are agreed upon in the task force, some/all of the test modes described herein may have to be modified/enhanced by additional test modes to test the transmitter.

When test mode 2 is enabled, the PHY shall transmit, with THP turned off, the data symbol sequence, {+12, –12} repeatedly on all channels. The transmitter shall time the transmitted symbols from an 800MHz ± 0.01% clock in the MASTER timing mode.

When test mode 3 is enabled, the PHY shall transmit the data symbol sequence {+12, -12} repeatedly on all channels. The transmitter shall time the transmitted symbols from an 800MHz ± 0.01% clock in the SLAVE timing mode. A typical transmitter output for transmitter test modes 2 & 3 in is shown in Figure 55–23.

Editor's note: The waveforms shown in Figure 55–22 and Figure 55–23 assume a peak-to-peak output swing of 2V differential. These are illustrative waveforms and can be adjusted once both the parameters are finalized by the task force.

When test mode 4 is enabled, the PHY shall transmit, with the THP turned off, transmitted symbols, timed from a 800MHz ± 0.01% clock in the MASTER timing mode, defined as follows:

Symbols corresponding to a single frequency tone, with frequencies of (800MHz/1024)*13, (800MHz/1024)*23, (800MHz/1024)*53, (800MHz/1024)*101, (800MHz/1024)*167.

Symbols corresponding to dual frequency tones in the pairs of [(800MHz/1024)*179, (800MHz/1024)*181], [(800MHz/1024)*277, (800MHz/1024)*281], [(800MHz/1024)*397, (800MHz/1024)*401], [(800MHz/1024)*499, (800MHz/1024)*503],

The peak to peak symbols used in this test, for both single and dual frequency tones correspond to ± M.

Editor's Note: Please provide comments and/or alternatives on the above specification for test mode 4. As written, this deviates from the 1000BASE-T approach because time domain distortion tests based on a scrambled sequence will be hard/marginal to measure with currently available test equipment. This is because of the higher speed and the lower distortion specifications. This issue was discussed in detail in http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf *at the July 2004 meeting.*

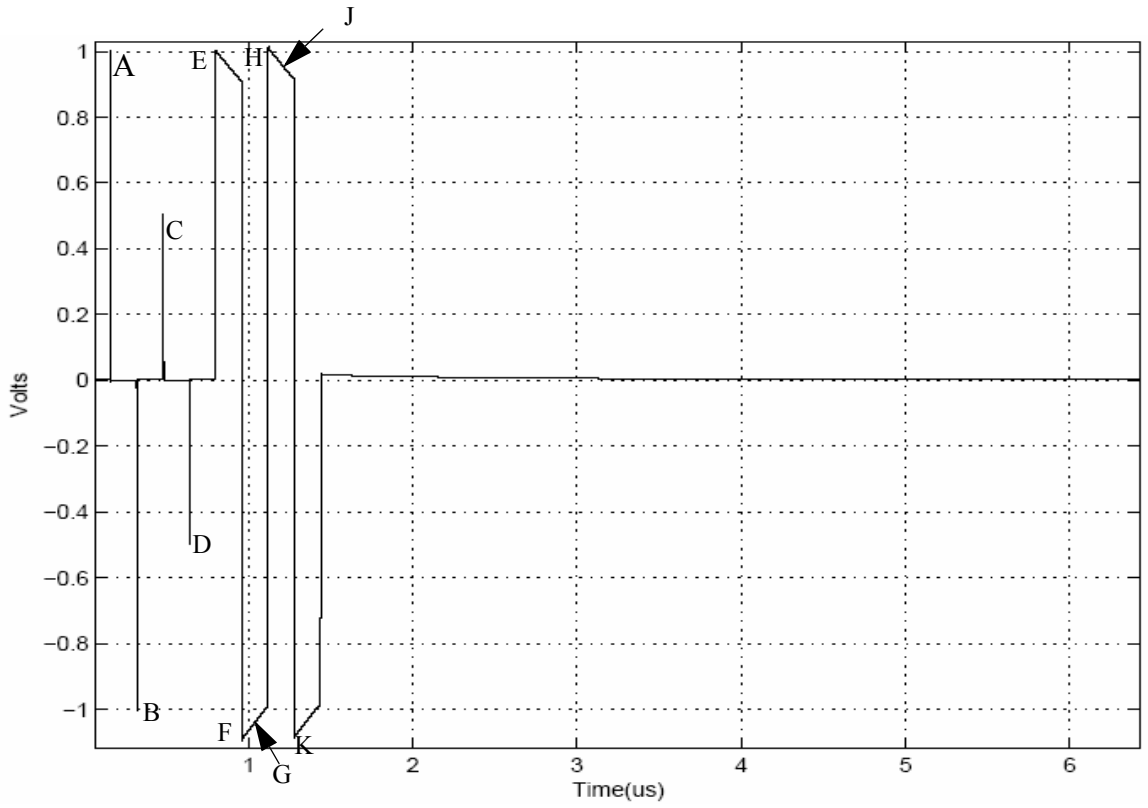


Figure 55–22—Example of transmitter test mode 1 waveform (1 cycle): informative

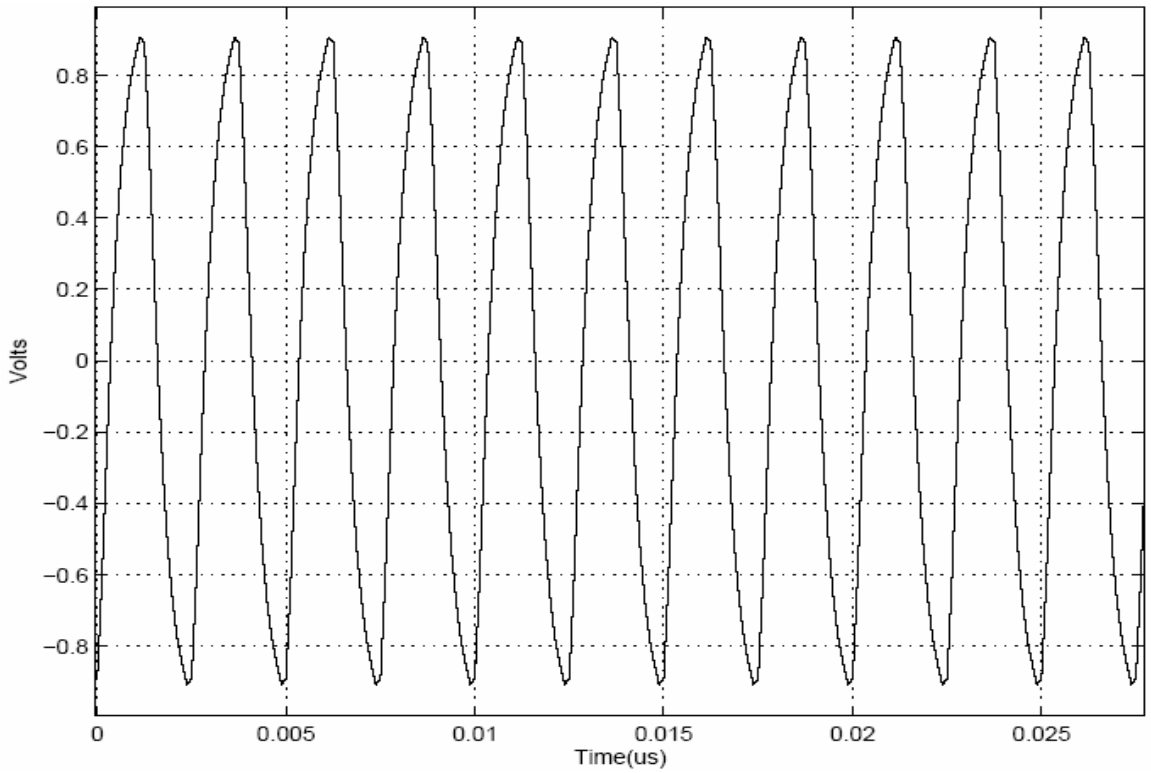


Figure 55–23—Example of transmitter test modes 2 & 3 waveform: informative

55.5.2.1 Test Fixtures

The following fixtures (illustrated by Figure 55–24, Figure 55–25 and Figure 55–26), or their functional equivalents, shall be used for measuring the transmitter specifications described in 55.5.3.

Editor's note: The next three figures have been changed from the 1000BASE-T test setups in places where deemed necessary. Figure 55–25 includes a power summer device to subtract the outputs of the transmitter and provide correct impedance transformation from the 50 Ω single-ended output impedances to a 50 Ω Spectrum Analyzer input. Comments/alternate proposals are welcome.

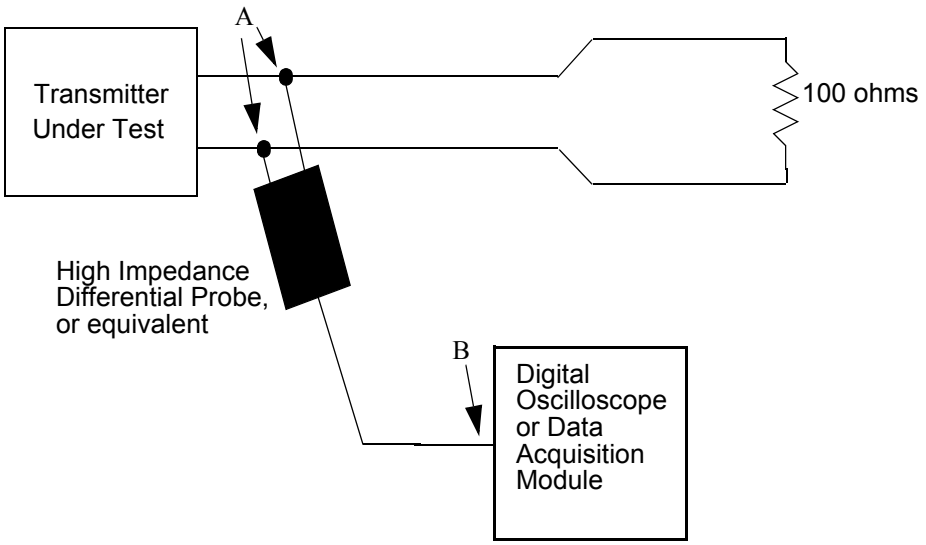


Figure 55–24—Transmitter test fixture 1 for template and droop measurement

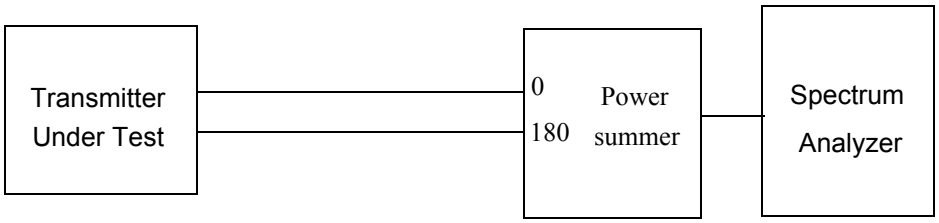


Figure 55–25—Transmitter test fixture 2 for linearity measurement

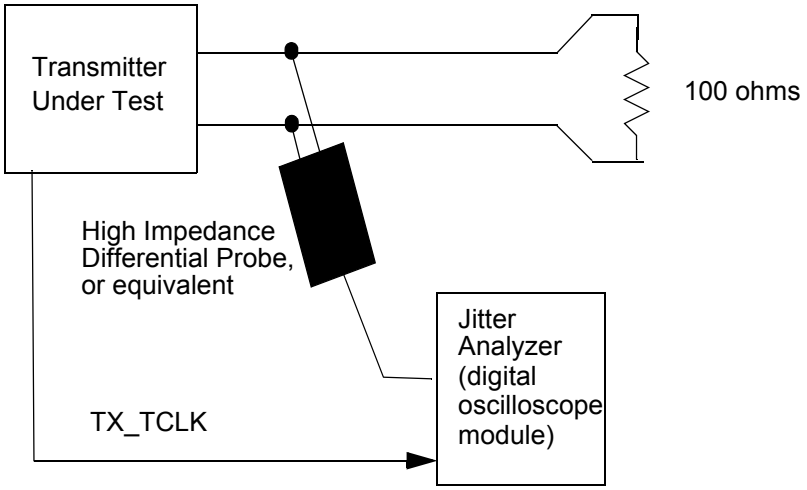


Figure 55–26—Transmitter test fixture 3 for transmitter jitter measurement

To allow for measurement of transmitted jitter in test mode 2 and 3, for both master and slave modes, the PHY shall provide access to the 800MHz rate symbol clock, TX_TCLK, that times the transmitted symbols (see 55.4.2.2). The PHY shall provide a means to enable this clock output if it is not normally enabled.

55.5.3 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 55.4.2.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

55.5.3.1 Peak differential output voltage and level accuracy

The peak value of the waveform at points A, B, C, D, E, F, H indicated in Figure 55–22 is defined by measuring the peak of the absolute value of the waveform between the time interval of [$2/F_s$ $3/F_s$] μsec after the start time of the corresponding non-zero symbol (±12, ±6). The time instants corresponding to these peak measured values are defined as t_A, t_B, t_C, t_D, t_E, t_F, t_H

The peak value of the waveform at points A and B, as defined above, shall fall within the range of 1V ±5%.

These measurements are to be made for each pair while operating in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable.

The peak of the waveforms at points A and B shall differ by less than 1%.

The peak of the waveform at points C and D as defined above shall differ by less than 2% from 0.5 times the average of the peaks of the waveform at points A and B.

Editor's note: The peak value is defined in such a way for two reasons. Firstly the waveform may not settle to the correct peak in one baud period with the recommended bandwidth specification for the transmitter. Secondly the magnetics may exhibit a significant insertion loss(IL) variation at high frequencies, and have a well controlled IL variation only at low frequencies.

The range is chosen to be tighter at ±5% as opposed to ±10% in 1000BASE-T. This is to reduce the possible significant margin loss in the system, which would occur if a transmitter transmits a 10% lower voltage and the receiver receiving the data of such a transmitter, is in presence of ANEXT interferers which are 10% higher. The peak voltage must be between 1V and 1.25V based on the motion in

http://www.ieee802.org/3/an/public/jul04/motions_1_0704.pdf

The peak voltage is chosen at the lower end, i.e. at 1V, as a suggested value in this draft, for various reasons discussed in the following presentations:

http://www.ieee802.org/3/an/public/may04/gupta_1_0504.pdf

http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf

Level matching accuracy requirements are kept similar to 1000BASE-T, the linearity of the transmitter is defined separately as an overriding test on the level matching accuracy. Comments/Suggestions on the numbers/methodology discussed in this clause are welcome.

55.5.3.2 Maximum output droop

The magnitude of the value of the waveform at point G, as defined in Figure 55–22, shall be greater than 94.5% of the peak value of the waveform at point F as defined in 55.5.3.1. These measurements are to be made for each pair while in test mode 1 and observing the differential signal output at the MDI using transmit test fixture 1 with no intervening cable. Point G is defined as the waveform at exactly 0.08 μsec after time instant t_F. Additionally, the magnitude of the value of the waveform at point J as defined in Figure 55–22 shall be greater than 94.5% of the magnitude of the peak value of the waveform at point H, as defined in 55.5.3.1. Point J is defined as the waveform at exactly 0.08 μsec after time instant t_H.

Editor's note: The numbers described above are similar to those discussed in the presentation:

http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf

The droop is chosen with 10% margin for a 100kHz transformer high pass pole. Alternatives proposals are welcome.

55.5.3.3 Differential output templates

The voltage waveforms around points A, B, C, D defined in Figure 55–22, after the normalization described herein, shall lie within the time domain template 1 defined in Figure 55–27 and the piecewise linear interpolation between the points in Table-55–4. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point A is normalized by dividing by the peak value of the waveform at A.

The waveform around point B is normalized by dividing by the negative of the peak value of the waveform at A.

The waveform around point C is normalized by dividing by 1/2 the peak value of the waveform at A.

The waveform around point D is normalized by dividing by the negative of 1/2 the peak value of the waveform at A.

The voltage waveforms around points F and H defined in Figure 55–22, after the normalization described herein, shall lie within the time domain template 2 defined in Figure 55–27 and the piecewise linear interpolation between the points in Table-55–5. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point F is normalized by dividing by the peak value of the waveform at F.

The waveform around point H is normalized by dividing by the peak value of the waveform at H.

*Editor's Note: The templates are to be created with the following assumptions about the elements in the transmit path. Deviation from 1000BASE-T include the elimination of the digital filter, and the elimination of the 2MHz high pass test filter. The -3dB frequency of the two pole continuous time filter is chosen to be 0.9*Fs/2 to 0.75*Fs mainly because the transformer will not have significant excess bandwidth because of the presence of an additional pole at the output. Comments are welcome.*

1. Ideal DAC.

2. Two pole continuous time low pass filter with -3dB frequency varying from $0.45*F_s$ to $0.75*F_s$.

3. Single pole continuous time high pass filter (transformer high pass) with pole varying from 1Hz to 100kHz.

4. Additionally, +0.025 to be added to the upper template and –0.025 to be added to the lower template to allow for noise and measurement error.

Editor's note: The Figure 55–27 and Table-55–4 and Table-55–5 have been borrowed from 1000BASE-T and are place holders in this draft. The templates/tables can be generated when the above assumptions are accepted by the Task Force - either as is, or with modifications.

NOTE—The transmit templates are not intended to address electromagnetic radiation limits.

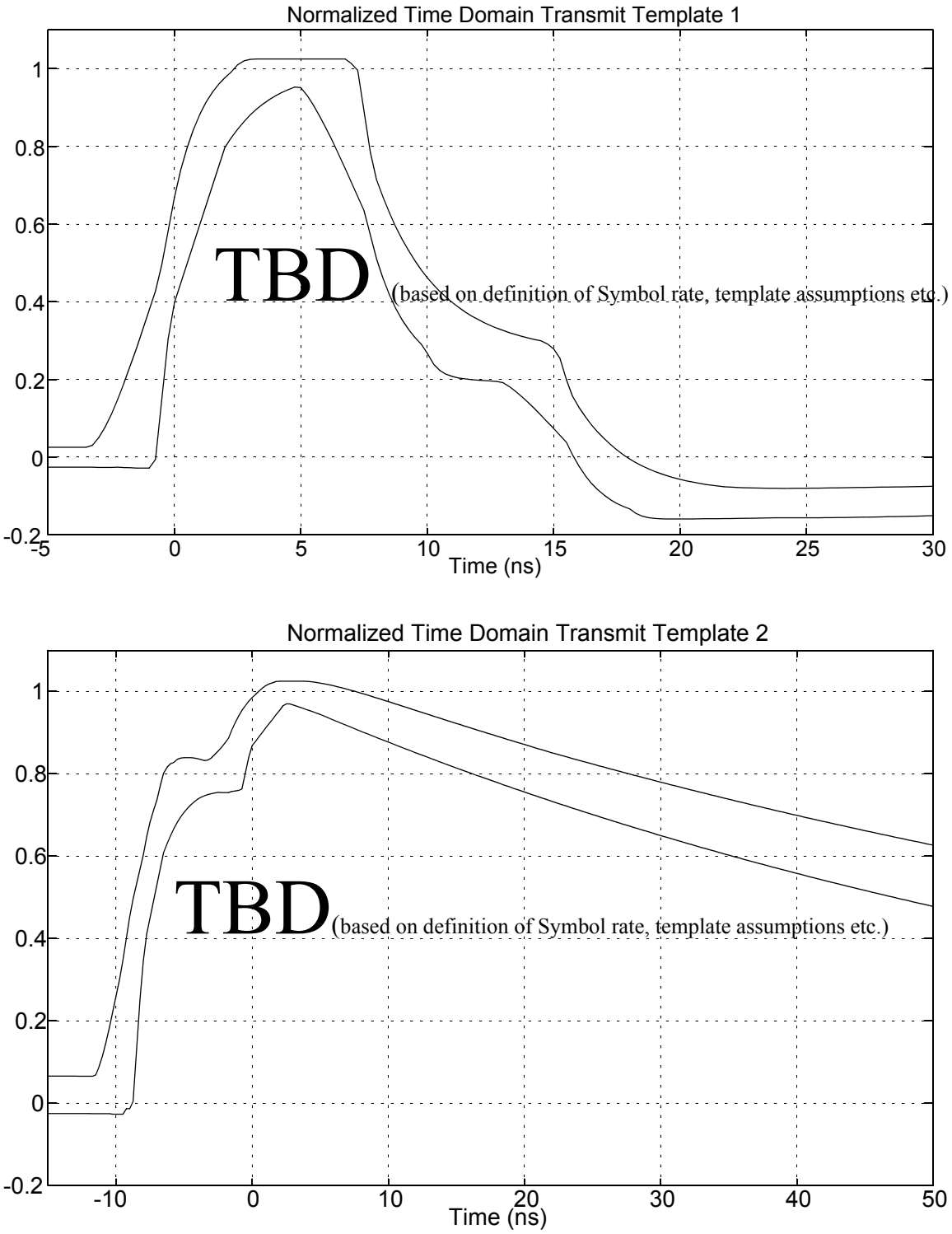


Figure 55–27—Normalized transmit templates as measured at MDI using transmit test fixture 1

Table 55–4—Normalized time domain voltage template 1

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–5.00	tbd	–tbd	tbd	tbd	tbd

Table 55–5—Normalized time domain voltage template 2

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–15.00	tbd	tbd	tbd	tbd	tbd

55.5.4 Transmitter linearity.

When in test mode 4 and observing the spectrum of the differential signal output at the MDI using transmitter test fixture 2, for each pair, with no intervening cable, the transmitter linearity mask to be defined as follows.

The SFDR of the transmitter when subject to single tone inputs producing output with peak to peak transmit amplitude shall be:

better than X_{nonlin} dB in the frequency range, f ε (0.1, f_1] MHz, f_1 is in MHz

and better than [X_{nonlin}-$X_{nlslope}$*log10(f/f_1)] dB, for f ε (f_1, 800/6] MHz.

The Signal to Intermodulation distortion ratio of the transmitter, for dual tone inputs, producing output with peak to peak transmit amplitude, shall be better than:

[X_{nonlin} +2.5- $X_{nlslope}$*log10(f/f_1)] dB for f ε (800/6, 800/2]MHz

The specification on transmit linearity, is provided for the interoperability of the far end device. As a normative specification, the parameter X_{nonlin} = 65dB, parameter f_1= 25MHz, and parameter $X_{nlslope}$ =20dB. The recommended specification is X_{nonlin} = 68dB and parameter $X_{nlslope}$ =0dB.

Editor's note: The above specification assumes a frequency domain approach to measuring transmitter non-linearity. The rationale for taking the frequency domain approach was explained in section 55.5.2. Alternate proposals to this methodology/numbers chosen above are welcome.

The "normative" and "recommended" specification is provided in accordance with the motion in the IEEE July meeting.

http://www.ieee802.org/3/an/public/jul04/motions_1_0704.pdf

The recommended specification on transmitter linearity will enable the local receiver to achieve the echo cancellation required to meet its BER performance requirements without need for non-linear cancellers and external hybrids. If the transceiver uses other techniques to suppress the impact of local transmitter nonlinearity and can meet its performance requirements in their presence, compliance with the recommended linearity requirement is not required.

55.5.4.1 Transmitter timing jitter

When in test mode 2 or test mode 3, the peak-to-peak jitter J_{txout} of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX_TCLK is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be less than J_1. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be less than J_{1filt}.

$$H_{jf1}(f) = \frac{jf}{jf + bw1} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 55.5.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be less than J_2 after the receiver is properly receiving the data. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be no more than J_{2filt} greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$.

$$H_{jf2}(f) = \frac{jf}{jf + bw2} \qquad f \text{ in Hz}$$

For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least 10^6 clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

Editor's note: Methodology borrowed from 1000BASE-T. Please suggest alternatives if you want it changed. The parameters J_1, J_2, J_{1filt}, J_{2filt}, bw1, bw2 are TBD.

55.5.5 Transmit clock frequency

The symbol transmission rate on each pair of the master PHY shall be 800MHz ± 0.01%.

55.5.6 Receiver electrical specifications

The PMA shall provide the Receive function specified in 55.4.2.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall be within the limits specified in 55.7.

55.5.6.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 55.5.3 and have passed through a link specified in 55.7 are received with a BER less than 10^{-12} and sent to the PCS after link reset completion. This specification shall be satisfied by an LDPC code block error rate less than 10^{-TBD}.

55.5.6.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a symbol rate within the range 800MHz ± 0.01%.

55.5.7 Common-mode noise rejection

This specification is provided to limit the sensitivity of the PMA receiver to common-mode noise from the cabling system. Common-mode noise generally results when the cabling system is subjected to electromagnetic fields.

The common mode signal that the transceiver shall be subject to, while maintaining link performance, with a LDPC block error rate less than 10^{-TBD}, should be <= 2.8V for f ε $(1,f_1]$ MHz, and <= $2.8*f_1/f$ for f ε $(f_1,$ 500) MHz, f_1 in MHz.

Editor's note: Methodology to be agreed upon. Parameter f_1 TBD. Initial recommendation of f_1=80MHz. An appropriate test set-up TBD to realize and test the above specification up to 500MHz, similar to 1000BASE-T standard.

55.5.7.1 Alien Crosstalk noise rejection

While receiving data from a transmitter specified in 55.5.3 through a link segment specified in 55.7 connected to all MDI duplex channels, a receiver shall operate with an LDPC block error rate of less than 10^{-TBD} with four noise sources at the specified levels representing alien NEXT, one connected to each of the four pairs. The noise sources shall be connected to each of the MDI inputs using Category 6 balanced cable of a maximum length of 0.5m. The noise source shall meet the ANEXT specifications in 55.7.3.4.

Editor's note: Please suggest specific ways to generate the ANEXT noise source. Some methods to generate the noise source to model ANEXT were discussed in the presentation:

http://www.ieee802.org/3/an/public/jul04/gupta_1_0704.pdf

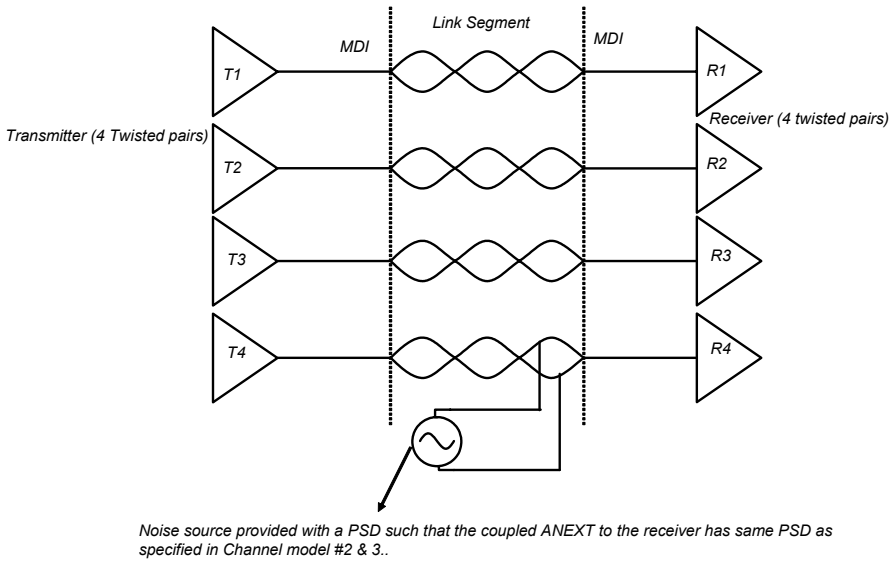


Figure 55–28—ANEXT noise rejection test

55.6 Management interface

10GBASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

55.6.1 Support for Auto-Negotiation

All 10GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE. All 10GBASE-T PHYs shall provide support for extended Next Pages as defined in 28.2.3.4.2#CrossRef# and shall support optimized FLP Burst to FLP burst timing as defined in 28.2.1.1.1 #CrossRef#.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for the following two primary purposes for 10GBASE-T:

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

This relationship is necessary for establishing the timing control and start-up sequencing of each PHY.

55.6.1.1 10GBASE-T use of registers during Auto-Negotiation

A 10GBASE-T PHY shall use the management register definitions and values specified in Table 55–6 #CrossRef#.

Table 55–6—10GBASE-T Registers

Register	Bit	Name	Description	Type [a]
0	0.15:0	MII control register	Defined in 28.2.4.1.1	RO
1	1.15:0	MII status register	Defined in 28.2.4.1.2	RO
4	4.15:0	Auto-Negotiation advertisement register	The Selector Field (4.4:0) is set to the appropriate code as specified in Annex 28A. The Technology Ability Field bits 4.12:5 are set to the appropriate code as specified in Annexes 28B and 28D. Bit 4.15 is set to logical one to indicate the desired exchange of Next Pages describing the gigabit extended capabilities.	R/W
5	5.15:0	Auto-Negotiation link partner ability register	Defined in 28.2.4.1.4. 10GBASE-T implementations do not use this register to store Auto-Negotiation Link Partner Next Page data.	RO
6	6.15:0	Auto-Negotiation expansion register	Defined in 28.2.4.1.5	RO
7	7.15:0	Auto-Negotiation Next Page transmit register	Defined in 28.2.4.1.6	R/W
8	8.15:0	Auto-Negotiation link partner Next Page register	Defined in 28.2.4.1.8	RO
TBD	TBD	Test mode bits	TBD	R/W

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

Table 55–6—10GBASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
TBD	TBD	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual configuration value 0=Disable MASTER-SLAVE Manual configuration value Default bit value is 0.	R/W
TBD	TBD	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when TBD is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when TBD is set to logical one. Default bit value is 0.	R/W
TBD	TBD	Port type	Bit TBD is to be used to indicate the preference to operate as MASTER (multiport device) or as SLAVE (single-port device) if the MASTER-SLAVE Manual Configuration Enable bit, TBD, is not set. Usage of this bit is described in TBD. 1=Multiport device 0=single-port device	R/W
TBD	TBD	10GBASE-T Full Duplex	1 = Advertise PHY is 10GBASE-T full duplex capable. 0 = Advertise PHY is not 10GBASE-T full duplex capable.	R/W
TBD	TBD	Reserved	Write as 0, ignore on read.	R/W
TBD	TBD	MASTER-SLAVE configuration fault	Configuration fault, as well as the criteria and method of fault detection, is PHY specific. The MASTER-SLAVE Configuration Fault bit will be cleared each time register TBD is read via the management interface and will be cleared by a 10GBASE-T PMA reset. This bit will self clear on Auto-Negotiation enable or Auto-Negotiation complete.This bit will be set if the number of failed MASTER-SLAVE resolutions reaches TBD. For l0GBASE-T, the fault condition will occur when both PHYs are forced to be MASTERs or SLAVEs at the same time using bits TBD and TBD. Bit TBD should be set via the MASTER-SLAVE Configuration Resolution function described in TBD. 1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC
TBD	TBD	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO
TBD	TBD	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status=OK) 0 = Local Receiver not OK (loc_rcvr_status=NOT_OK) Defined by the value of loc_rcvr_status as per TBD.	RO
TBD	TBD	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status=OK) 0 = Remote Receiver not OK (rem_rcvr_status=NOT_OK) Defined by the value of rem_rcvr_status as per TBD.	RO
TBD	TBD	LP 10GBASE-T FD	1 = Link Partner is capable of 10GBASE-T full duplex 0 = Link Partner is not capable of 10GBASE-T full duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

Table 55–6—10GBASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
TBD	TBD	Reserved	Reserved	RO
TBD	TBD	Idle Error Count	Bits TBD indicate the Idle Error count, where TBD is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and are to be held at all ones in case of overflow (see TBD).	RO/SC
TBD	TBD	Extended status register	See 22.2.4.4	RO

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

55.6.1.2 10GBASE-T Auto-Negotiation page use

10GBASE-T PHYs shall exchange a 10GBASE-T and 1000BASE-T formatted extended Next Page, as specified in Table 55-7 #CrossRef#, immediately following the exchange of the Base Page

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 10GBASE-T message page exchange.

Table 55–7—10GBASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
BASE PAGE		
D15	1 (to indicate that Next Pages follow)	
D14:D13	As specified in 28.2.1.2	Management register 4
D12	1 (to indicate extended Next Pages follow)	Management register 4
D11:D0	As specified in 28.2.1.2	Management register 4
Extended Next Page (Message Code Field and Flags Field)		
M10:M0	9	
T	As specified in 28.2.3.4.7	
Ack2	0	
MP	1 (to indicate this is the	
Ack	As specified in 28.2.3.4.4	
NP	As specified in 28.2.3.4.3	
Extended Next Page (Unformatted Message Code Field)		
U31:U20	Reserved transmit as 0	
U19		
U18		
U17		

Table 55–7—10GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Bit definition	Register location
U16	10GBASE-T (1 = support of 10GBASE-T and 0 = no support)	GMII register TBD (MASTER-SLAVE Control register)
U15	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	GMII register TBD (MASTER-SLAVE Control register)
U14	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	GMII register TBD (MASTER-SLAVE Control register)
U13	Port type bit (1 = multiport device and 0 = single-port device)	GMII register TBD (MASTER-SLAVE Control register)
U12	10GBASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE.) This bit is ignored if TBD =0.	GMII register TBD (MASTER-SLAVE Control register)
U11	10GBASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit TBD.	GMII register TBD (MASTER-SLAVE Control register)
U10	MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value(10:0)
U9	MASTER-SLAVE Seed Bit 9 (SB9)	
U8	MASTER-SLAVE Seed Bit 8 (SB8)	
U7	MASTER-SLAVE Seed Bit 7 (SB7)	
U6	MASTER-SLAVE Seed Bit 6 (SB6)	
U5	MASTER-SLAVE Seed Bit 5 (SB5)	
U4	MASTER-SLAVE Seed Bit 4 (SB4)	
U3	MASTER-SLAVE Seed Bit 3 (SB3)	
U2	MASTER-SLAVE Seed Bit 2 (SB2)	
U1	MASTER-SLAVE Seed Bit 1 (SB1)	
U0	MASTER-SLAVE Seed Bit 0 (SB0)	

55.6.1.3 Sending Next Pages

Implementors who do not wish to send additional Next Pages (i.e., Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28 and the Next Pages defined in 50.6.1.2 #CrossRef#. Implementors who wish to send additional Next Pages are advised to consult Annex 40C.

55.6.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using TBD with the 10GBASE-T Technology Ability Next Page bit values specified in TBD and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–13.)

The following four equations are used to determine these relationships:

manual_MASTER = U0 * U1
manual_SLAVE = U0 * !U1

single-port device = !U0 * !U2,
multiport device = !U0 * U2

where

U0 is bit 0 of unformatted page 1,
U1 is bit 1 of unformatted page 1, and
U2 is bit 2 of unformatted page 1 (see Table 55–7).

A 10GBASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies may result in contention. The resolution function of TBD is defined to handle any relationship conflicts.

Table 55–8—10GBASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

The rationale for the hierarchy illustrated in Table 55–8 is straightforward. A 10GBASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed

value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_10GigT=FAIL (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementor. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 2^{11}– 2. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 10.15 shall be set to logical zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit TBD) and the MASTER-SLAVE Config Value bit (control register bit TBD) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Configuration fault condition, thus the MASTER-SLAVE Configuration fault bit (status register bit TBD) shall be set to logical one. The MASTER-SLAVE Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_1GigT shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–16) when the highest common denominator (HCD) technology is 10GBASE-T. The resulting MASTER-SLAVE value is used by the 10GBASE-T PHY control (TBD).

If MASTER-SLAVE Manual Configuration is disabled (bit TBD is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit TBD of the 10GBASE-T Status Register is set to logical zero and bit TBD is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 10GBASE-T returns control to Auto_Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–16) and passes the value MASTER or SLAVE to PMA_CONFIG.indicate (see TBD.)
b) *Unsuccessful:* link_status_10GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–16.)
c) *Fault detected:* (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit TBD of the 10GBASE-T Status Register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER SLAVE relationship via the seed method have failed. When a fault is detected, link_status_10GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 10GBASE-T is selected as the highest common denominator; otherwise, it is assumed to have passed this condition

55.7 Link segment characteristics

10GBASE-T is designed to operate over ISO/IEC 11801 Class E or Class F 4-Pair balanced cabling that meets the additional requirements specified in 55.7. Each of the four pairs supports an effective data rate of (2500) Mbps in each direction simultaneously. The term "link segment" used in this clause refers to four duplex channels. The term "duplex channel" will be used to refer to a single channel with full duplex capability. Specifications for a link segment apply equally to each of the four duplex channels. All implementations of the balanced cabling link segment specification shall be compatible at the MDI.

55.7.1 Cabling system characteristics

The cabling system used to support 10GBASE-T requires 4 pairs of ISO/IEC 11801 Class E or Class F balanced cabling with a nominal impedance of 100 Ω.

Additionally:

a) 10GBASE-T uses a star topology with Class E or Class F balanced cabling used to connect PHY entities.
b) 10GBASE-T is an ISO/IEC 11801 Class E and Class F application with the additional transmission requirements specified in 55.7.

55.7.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Class E link segment of at least 55 to 100 meters and a Class F link segment of 100 meters will provide a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, nominal impedance, NEXT loss, ELFEXT loss, and return loss. In addition, link segment requirements are specified in subclause 55.7.3.2 for alien crosstalk.

Link segment testing shall be conducted using source and load impedances of 100 Ω.

The link segment transmission parameters of insertion loss and ELFEXT loss specified in 55.7 are ISO/IEC 11801 Class E specifications extended by extrapolating the formulas to a frequency up to 500 MHz. The link segment transmission parameters of NEXT loss, MDNEXT loss and Return Loss specified in 55.7 are ISO/IEC 11801 Class E specifications extended beyond 250 MHz by utilizing the equations referenced in TIA TR42 D1.0 TSB-155.

Note—The Class F and Augmented Category 6 (Augmented Class E) channel limits meet or exceed the Clause 55 Class E link segment specifications. Class F and Augmented Category 6 (Augmented Class E) specifications are referenced only when applicable to requirements specific to Class F and Augmented Category 6 such as power sum alien NEXT (PS ANEXT) and Insertion Loss.

55.7.2.1 Insertion loss

The insertion loss of each duplex channel shall be less than

$$1.05\left(1.82\times\sqrt{f}+0.169\times f+\frac{0.25}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f} \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 500 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

55.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 500 MHz.

55.7.2.3 Return loss

Each link segment duplex channel shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 500 MHz. The reference impedance shall be 100 Ω.

$$\text{Return\_Loss}(f) = \begin{cases} 19 & 1 \le f < 10 \\ 24 - 5\log 10(f) & 10 \le f < 40 \\ 32 - 10\log 10(f) & 40 \le f < 400 \\ 6 & 400 \le f \le 500 \end{cases} \quad \text{(dB)}$$

where f is the frequency in MHz.

55.7.3 Coupling parameters

55.7.3.1 Coupling parameters between duplex channels

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. In addition, each duplex channel can be disturbed by more than one duplex channel. To ensure the total NEXT loss and FEXT loss coupled into a duplex channel is limited, multiple disturber Near-End Crosstalk (MDNEXT) and multiple disturber ELFEXT (MDELFEXT) loss is specified.

55.7.3.1.1 Near-End Crosstalk (NEXT)

55.7.3.1.1.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the bit error rate objective specified in 55.1. The NEXT loss between any two duplex channels of a link segment shall be at least

$$-20 \times \log 10\left(10^{\frac{74.3 - 15\log 10(f)}{-20}} + 2 \times 10^{\frac{94 - 20\log 10(f)}{-20}}\right) \quad \text{(dB)}$$

where f is the frequency $(1 \le f < 330)$ in MHz.

The NEXT loss between any two duplex channels of a link segment shall be at least

$$31 - 50 \times \log 10\left(\frac{f}{330}\right) \quad \text{(dB)}$$

where f is the frequency $(330 \le f \le 500)$ in MHz.

55.7.3.1.1.2 Multiple Disturber Near-End Crosstalk (MDNEXT) loss

Since four duplex channels are used to transfer data between PMDs, the NEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels.

To ensure the total NEXT coupled into a duplex channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses. The Power Sum loss between a duplex channel and the three adjacent disturbers shall be greater than

$$-20 \times \log 10\left(10^{\frac{72.3 - 15\log 10(f)}{-20}} + 2 \times 10^{\frac{90 - 20\log 10(f)}{-20}}\right) \quad \text{(dB)}$$

where f is the frequency $1 \le f < 330$ in MHz and

$$28 - 42 \times \log 10\left(\frac{f}{330}\right) \quad \text{(dB)}$$

where f is the frequency $(330 \le f \le 500)$ in MHz.

55.7.3.1.1.3 Multiple-Disturber Power Sum Near-End Crosstalk (PS NEXT) loss

PS NEXT loss is determined by summing the power of the three individual pair-to-pair differential NEXT loss values over the frequency range 1 MHz to 500 MHz. as follows:

$$-10 \times \log 10 \sum_{i=1}^{n} 10^{\frac{-NL(f)i}{10}} \quad \text{(dB)}$$

where

NL(f)i is the magnitude in dB of NEXT loss at frequency f of pair combination i

i is the 1, 2, or 3 (pair-to-pair combination)

n is the number of pair-to-pair combinations

55.7.3.1.2 Far-End Crosstalk (FEXT)

55.7.3.1.2.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in 55.1.1. Far-End Crosstalk

(FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end.

Editor's Note: For 1000BASE-T the error rate is specified as symbol error rate, frame error rate and bit error rate. For 10GBASE-T D1.0, as a starting point, the BER objective of 10^-12 specified in 55.1 will be utilized throughout subclause 55.7.

FEXT loss is defined as

$$\text{FEXT\_Loss(f)} = 20 \times \log 10\left(\frac{V_{pds(f)}}{V_{pcn(f)}}\right) \qquad \text{(dB)}$$

and ELFEXT_Loss is defined as

$$\text{ELFEXT\_Loss(f)} = 20 \times \log 10\left(\frac{V_{pds(f)}}{V_{pcn(f)}}\right) - \text{SLS\_Loss(f)} \qquad (dB)$$

where

*V*pds	is the peak voltage of disturbing signal (near-end transmitter)
*V*pcn	is the peak crosstalk noise at far end of disturbed channel
SLS_Loss	is the insertion loss of disturbed channel in dB

The worst pair ELFEXT loss between any two duplex channels shall be greater than

$$-20 \times \log 10\left(10^{\frac{67.8 - 20\log 10(f)}{-20}} + 4 \times 10^{\frac{83.1 - 20\log 10(f)}{-20}}\right) \qquad \text{(dB)}$$

where *f* is the frequency over the range of 1 MHz to 500 MHz.

55.7.3.1.2.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses. The Power Sum loss between a duplex channel and the three adjacent disturbers shall be greater than

$$-20 \times \log 10\left(10^{\frac{64.8 - 20\log 10(f)}{-20}} + 4 \times 10^{\frac{80.1 - 20\log 10(f)}{-20}}\right) \quad \text{(dB)}$$

where f is the frequency over the range of 1 MHz to 500 MHz.

55.7.3.1.2.3 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PS ELFEXT) loss

PS ELFEXT loss is determined by summing the power of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 1 MHz to 500 MHz as follows:

$$\text{PSELFEXT\_Loss(f)} = -10 \times \log_{10} \sum_{i=1}^{i=n} 10^{\frac{-EL(f)i}{10}}$$

where

EL(f)i is the magnitude of ELFEXT loss at frequency f of pair combination i
i is the 1, 2, or 3 (pair-to-pair combination)
n is the number of pair-to-pair combinations

55.7.3.2 Coupling parameters between link segments

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise.

Editor's Note: Text needs to be added to clearly identify the alien crosstalk dependencies.

55.7.3.2.1 Multiple Disturber Alien Near-End Crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error rate objective specified in 55.1. To ensure the total Alien NEXT coupled into a duplex channel is limited, multiple disturber Alien NEXT loss is specified as the power sum of the individual Alien NEXT disturbers.

55.7.3.2.1.1 Multiple-Disturber Power Sum Near-End Crosstalk (PS ANEXT) loss

ANEXT loss is determined by summing the power of the individual pair-to-pair differential Alien NEXT loss values over the frequency range 1 MHz to 500 MHz. as follows:

$$-10 \times \log 10 \sum_{i=1}^{n} 10^{\frac{-AN(f)i}{10}} \quad \text{(dB)}$$

where

AN(f)i is the magnitude in dB of ANEXT loss at frequency f of pair combination i

i is the pair-to-pair combination (1 to n)

n is the number of pair-to-pair combinations between link segments

The Power Sum ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is defined by the equations:

$$PSANEXT \geq \begin{Bmatrix} X1 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ X1 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{Bmatrix}$$

where f is the frequency in MHz and X1 = the intercept at f=100 MHz. The intercept is referred to as the PS ANEXT constant.

55.7.3.2.1.2 PS ANEXT for a Class E Channel

For a 100 meter Class E channel with the maximum insertion loss of 55.7.2.1 the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT \geq \begin{Bmatrix} 62 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ 62 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{Bmatrix}$$

55.7.3.2.1.3 PS ANEXT for a Class F Channel

For a 100 meter Class F channel the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT \geq \begin{Bmatrix} 60 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ 60 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{Bmatrix}$$

where f is the frequency in MHz.

The PS ANEXT for a Class F channel specified in 55.7.3.2.1.3 assumes the maximum insertion loss of a Class F channel in 55.7.3.3.1

Note: The PS ANEXT values listed above are are for certification of the channel. For simulating PHY performance to estimate system margin, the PS ANEXT numbers must be increased by 2.5 dB. This represents the difference between the limit line, which is used for channel certification, and the average value of PS ANEXT which will be lower than the limit line.

Editors Note: Alien crosstalk is not adequately specified in the ISO/IEC 11801 or TIA cabling standards. The PS ANEXT limits for both Class F and Class E are the minimum requirements for 100 meter operation and are not intended to represent the PS ANEXT performance limits of the cabling (i.e., the PS ANEXT performance of the cabling may be better than the minimum requirements specified in 10GBASE-T). TIA TR42 has initiated Project SP-3-4426-AD10 to develop augmented Category 6 cabling. The resulting requirements will be presented in a new revision or addendum to the TIA-568-B standard.

55.7.3.2.1.4 PS ANEXT for an Augmented Category 6 (Augmented Class E) Channel

For a 100 meter Augmented Category 6 (Augmented Class E) channel the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT \geq \left\{ \begin{array}{ll} 60 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \leq f \leq 100 \\ 60 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \leq 500 \end{array} \right\}$$

The PS ANEXT for an Augmented Category 6 (Augmented Class E) Channel specified in 55.7.3.2.1.4 assumes the maximum insertion loss of an Augmented Category 6 (Augmented Class E) channel in 55.7.3.3.2.

Editor's note: PSAFEXT limits need to be added with reference to test methods.

55.7.3.2.2 Multiple Disturber Alien Far-End Crosstalk (MDAFEXT) loss (ffs)

55.7.3.2.2.1 Multiple -Disturber Power Sum Alien Far-End Crosstalk (PS AFEXT) loss (ffs)

55.7.3.3 PS ANEXT loss to insertion loss ratio requirements

To ensure reliable operation, a minimum signal to noise ratio (SNR) must be maintained. The minimum SNR is assured for 100 meters of Class E by meeting the requirements of 55.7.1 through 55.7.3.2.1.2 and for 100 meters of Class F by meeting the additional requirement of 55.7.3.2.1.3.

The PS ANEXT loss requirement of 55.7.3.2.1.2 can be relaxed based on a reduction in the maximum insertion loss specified in 55.7.2.1. The insertion loss reduction can be achieved by scaling the length of the Class E link segment or using Class F cabling for the link segment with the additional requirement of 55.7.3.2.1.3 or using Augmented Category 6 (Augmented Class E) Channel for the link segment as specified in 55.7.3.2.1.4 and 55.7.3.3.2.

55.7.3.3.1 Insertion Loss for a Class F Channel

The PS ANEXT for a Class F Channel assumes the maximum insertion loss of a Class F channel.

The insertion loss of a Class F duplex channel shall be less than

$$1.05\left(1.8 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 4 \times 0.02 \times \sqrt{f} \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 500 MHz. This includes the attenuation of the balanced cabling pairs, including the cords and connecting hardware losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

NOTE— The Class F insertion loss is an improvement of 2.1 dB at 250 MHz over the Class E insertion loss specifications resulting in a 2 dB relaxation in the Class F PS ANEXT requirement.

55.7.3.3.2 Insertion Loss for an Augmented Category 6 (Augmented Class E) Channel

The insertion loss of an Augmented Category 6 (Augmented Class E) Channel shall be less than

$$1.05\left(1.8\times\sqrt{f}+0.01\times f+\frac{0.2}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f} \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 500 MHz. This includes the attenuation of the balanced cabling pairs, including the cords and connecting hardware losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

55.7.3.3.3 Insertion Loss Scaling

For the purpose of adjusting the PS ANEXT the insertion loss is assumed to scale linearly with length.

The Scaled Class E IL is defined by the following equation:

$$\text{Scaled\_Class\_E\_IL} = \frac{\text{Length\_m}}{100}\times 1.05\left(1.82\times\sqrt{f}+0.0169\times f+\frac{0.25}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f}\,\text{(dB)}$$

where Length is in meters.

55.7.3.3.4 Insertion Loss of a Category 6 channel of 55 meters

ISO/IEC 11801 classes for balanced cabling refer to cabling channel distances of 100 meters. For cabling channels less than 100 meters the Category of the components comprising the channel applies (e.g., Category 6 components provide Class E balanced cabling performance).

The insertion loss of a Category 6 channel of 55 meters is defined by the following equation:

$$\text{Scaled\_Class\_E\_IL}(55m) = \frac{55}{100}\times 1.05\left(1.82\times\sqrt{f}+0.0169\times f+\frac{0.25}{\sqrt{f}}\right)+4\times 0.02\times\sqrt{f}\,\text{(dB)}$$

55.7.3.4 PS ANEXT Adjustment

The adjusted PS ANEXT loss requirement is determined by first calculating the PS ANEXT_constant and utilizing the constant in the PS ANEXT limit line model.

The PS ANEXT_constant is defined by the following equation:

$$\text{PSANEXT\_constant} = 62 - (\text{CE\_IL\_250}MHz - \text{SCE\_IL\_250}MHz) \times \frac{15}{15.6} \quad \text{(dB)}$$

where

CE_IL_250 MHz is the Class E insertion loss at 250 MHz

SCE_IL_250 MHz is the scaled Class E insertion loss at 250 MHz.

55.7.3.4.1 PS ANEXT for a Category 6 channel of 55 meters

For a Category 6 channel of 55 meters with worst case insertion loss of 55.7.3.3.4 the PS ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall be greater than

$$PSANEXT > \left\{ \begin{array}{ll} 47 - 10\log 10(\frac{f}{100}) \quad (dB) & 1 \le f \le 100 \\ 47 - 15\log 10(\frac{f}{100}) \quad (dB) & 100 < f \le 500 \end{array} \right\}$$

where f is the frequency in MHz.

55.7.4 Delay

In order to simultaneously send data over four duplex channels in parallel, the propagation delay of each duplex channel as well as the difference in delay between any two of the four channels are specified. This ensures the 10 Gbps data that is divided across four channels can be properly reassembled at the far-end receiver.

55.7.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 500 MHz.

55.7.4.2 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 2 MHz to 500 MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns within the above requirement.

55.7.5 Noise environment

Editor's Note: The noise environment (55.7.5) sub clause is extracted from 1000BASE-T specification with minor changes. This text will likely evolve to reflect the 10GBASE-T noise environment assumptions.

The 10GBASE-T noise environment consists of noise from many sources. The primary noise sources that impact the objective BER are NEXT and echo interference, which are reduced to a small residual noise using cancellers. The remaining noise sources, which are secondary sources, are discussed in the following list. The 10GBASE-T noise environment consists of the following:

a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bi-directional transmission of data and by impedance mismatches in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.

b) Near-End Crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver will experience NEXT interference from three adjacent transmitters. NEXT cancellers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor.

c) Far-End Crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be cancelled in the same way as echo and NEXT interference although the symbols from the remote transmitters are not immediately available.

d) Inter-Symbol Interference (ISI) noise. ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same channel.

e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and non-linear channel characteristics.

f) Noise coupled between link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise.Since the transmitted symbols from the alien NEXT noise source are not available to the cancellation processor (they are in another cable), it is very difficult to cancel the alien NEXT noise. To ensure robust operation the alien NEXT noise must meet the specification of 55.7.5.

g) The background noise for 10GBASE-T is expected not to exceed -150 dBm/Hz.. A background noise limit of -150 dBm/Hz was assumed in the 10GBASE-T Matlab simulation models.

55.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 55.4.4 for a description of the automatic MDI/MDI-X configuration.

55.8.1 MDI connectors

Eight-pin connectors meeting the requirements of subclause 3 and Figures 1 through 4 of IEC 60603-7: 1995 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 55–29 and Figure 55–30. The assignment of PMA signals to connector contacts for PHYs is shown in Table 55–9. The PHY shall be capable of reversing the polarity of the contacts for any PMA signal to correct for a mis-wired channel between any two PHY entities within the link segment.

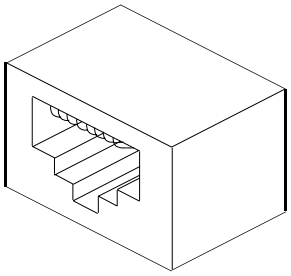


Figure 55–29—MDI connector

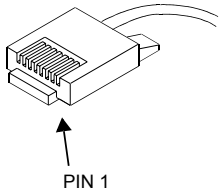


Figure 55–30—Balanced cabling connector

Table 55–9—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

55.8.2 Crossover function

It is a functional requirement that a crossover function be implemented in every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or else-where in the link segment. The MDI connector for a 10GBASE-T PHY shall be marked with the graphical symbol X. The crossover function specified here is not compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a single-port device to a multiport device, it is recommended that the crossover be implemented in the PHY local to the multiport device. It is recommended that the crossover be visible to an installer from one of the PHYs. It is further recommended that, in networks in which the topology identifies either a central backbone segment or a central device, the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

Editor's note: The MDI crossover function has been made mandatory rather than optional.

55.8.3 MDI electrical specifications

The MDI connector (jack) when mated with a specified balanced cabling connector (plug) shall meet the electrical requirements for Category 6 connecting hardware for use with 100-ohm Category 6 cable as specified in ANSI/TIA/EIA-568-B.2:2002 and ISO/IEC 11801:2002.

The mated MDI/balanced cabling connector pair shall have a FEXT loss not less than $43.1 - 20\log_{10}(f/100)$ (where f is the frequency over the range 1 MHz to 500 MHz) between all contact pair combinations shown in Table 55–9.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5), when released from power-down mode, or when external power is first applied to the PHY.

55.8.3.1 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω ± TBD% is attenuated, relative to the incident signal, at least 16 dB over the frequency range of 1.0 MHz to 40 MHz and at least $16 - 10\log_{10}(f/40)$ dB over the frequency range 40 MHz to 500 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data or control symbols.

55.8.3.2 MDI impedance balance

Impedance balance is a measurement of the impedance-to-ground difference between the two MDI contacts used by a duplex link channel and is referred to as common-mode-to-differential-mode impedance balance. Over the frequency range 1.0 MHz to 500.0 MHz, the common-mode-to-differential-mode impedance balance of each channel of the MDI shall exceed

$$45 - 4\log_{10}\left(\frac{f}{50}\right) \quad \text{dB}$$

where f is the frequency in MHz when the transmitter is transmitting random or pseudo random data. Test-mode 4 may be used to generate an appropriate transmitter output.

The balance is defined as

$$20\log_{10}\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 55–31 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.

NOTES

1—Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

2—The imbalance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

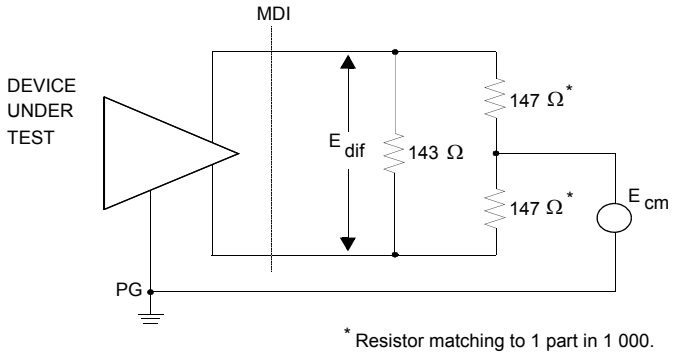


Figure 55–31—MDI impedance balance test circuit

Editor's note: The impedance balance equation was obtained by processing the data provided by Pulse on the magnetics. Other factors contributing to the imbalance may require us to modify the above requirement. Please provide feedback on the feasibility of the above proposal.

55.8.3.3 MDI common-mode output voltage

The magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 55–32, shall be less than 15 mV peak-to-peak when transmitting data.

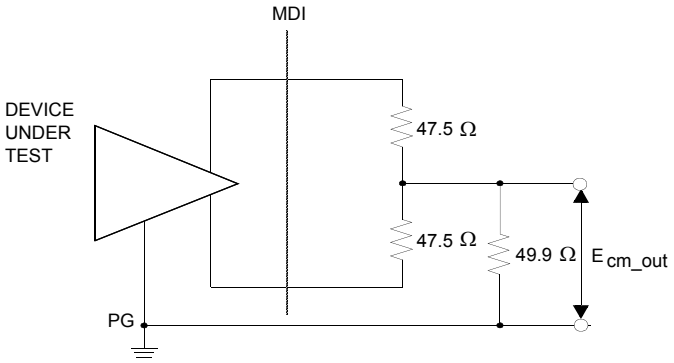


Figure 55–32—Common-mode output voltage test circuit

Editor's note: 1000BASE-T specified 50 mV as the maximum permissible common-mode output voltage. That number has been reduced to 15 mV to because reducing it should make it easier to pass EMI. We need feedback from the Task Force on whether this value is feasible from an implementation point of view from both the PHY vendors and the magnetics manufacturers.

NOTE—The imbalance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

55.8.3.4 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Each wire pair shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 55–33). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

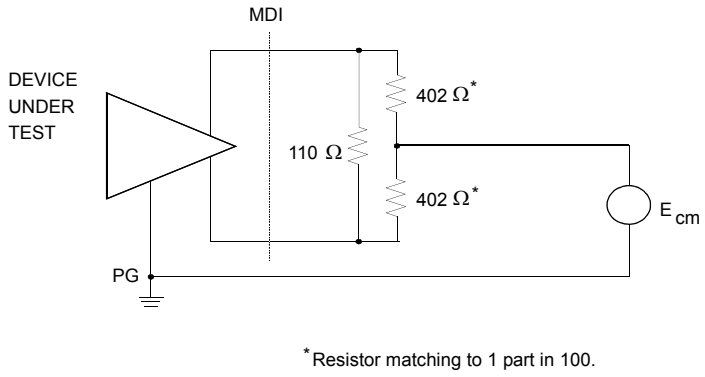


Figure 55–33—MDI fault tolerance test circuit

55.9 Environmental specifications

55.9.1 General safety

All equipment meeting this standard shall conform to IEC 60950-1: 2001.

55.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational

system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

Editor's note: References have been updated; the frequency range of interest is now from 1MHz to 500MHz. The equations have been updated to reflect this and the formulae have been adjusted.

55.9.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

55.9.4 Telephone voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10GBASE-T. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard. The following maximums generally apply.

a) Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.
a) Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10GBASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltage shall not result in any safety hazard.

55.9.5 Electromagnetic emissions

A system integrating the 10GBASE-T shall comply with applicable local and national codes for the limitation of electromagnetic interference.

55.9.6 Temperature and humidity

A system integrating the 10GBASE-T is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

55.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 10GBASE-T)
d) Any applicable safety warnings

55.11 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI.

55.11.1 MDI to XGMII delay constraints

Every 10GBASE-T PHY associated with a XGMII shall comply with the bit delay constraints specified in Table 55–10 for full duplex operation. These constraints apply for all 10GBASE-T PHYs.

Table 55–10—MDI to XGMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
XGMII ⇔ MDI ⇔XGMII ⇔ MDI	SFD coming in on XGMII on one PHY and coming out of the XGMII on the other PHY with two PHYs connected back to back with 10m cable	—	TBD	TBD	TBD
XGMII ⇔ MDI	TBD	—	TBD	TBD	TBD

Editor's note: Delay is measureable easily on two PHYs connected back to back however this delay will vary depending on timing of arrival of the SFD on the XGMII relative to start of LDPC code. Delay from XGMII to MDI will be hard to measure because all symbols are encoded and buried inside LDPC code words. It may make sense to have an optional flag put in which is detectable on the MDI port solely to enable easy detection of delays while testing.

55.12 Protocol implementation conformance statement (PICS) proforma for Clause 55—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 10GBASE-T[3]

The supplier of a protocol implementation that is claimed to conform to this clause shall complete the Protocol Implementation Conformance Statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so it can be used for its intended purpose and may further publish the completed PICS.

55.12.1 Identification

55.12.1.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTES 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

55.12.1.2 Protocol summary

Identification of protocol specification	IEEE Std 802.an:?, Clause 55, Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer, and baseband medium, type 10GBASE-T
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21—The answer Yes means that the implementation does not conform to the standard)	
Date of Statement	

55.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*XGMII	PHY associated with XGMII	TBD	O	Yes [ ] No [ ]	

55.12.3 Clause conventions

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	The values of all components in test circuits shall be	TBD	M	Yes [ ]	Accurate to within ±1% unless otherwise stated.

55.12.4 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	The PCS shall	TBD	M	Yes [ ]	

55.12.4.1 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function shall	TBD	M	Yes [ ]	

55.12.4.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	TBD	M	Yes [ ]	

55.12.5 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	TBD	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity or from PHY Control.
PMF2	PMA Transmit shall	TBD	M	Yes [ ]	
PMF3	The four transmitters shall be driven by the same transmit clock, TX_TCLK	TBD	M	Yes [ ]	
PMF4	PMA Transmit shall	TBD	M	Yes [ ]	Follow the mathematical description given in TBD.
PMF5	PMA Transmit shall comply with	TBD	M	Yes [ ]	The electrical specifications given in TBD.
PMF6	When the PMA_CONFIG.indicate parameter config is MASTER, the PMA Transmit function shall	TBD	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of TBD.
PMF7	When the PMA_CONFIG.indicate parameter config is SLAVE, the PMA Transmit function shall	TBD	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock of TBD while meeting the jitter requirements of TBD.

55.12.6 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	All 10GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.	TBD	M	Yes [ ]	

55.12.6.1 10GBASE-T Specific Auto-Negotiation Requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	10GBASE-T PHYs shall	TBD	M	Yes [ ]	TBD
AN2	The MASTER-SLAVE relationship shall be determined during Auto-Negotiation	TBD	M	Yes [ ]	TBD

55.12.7 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME3	The PHY shall provide electrical isolation between	TBD	M	Yes [ ]	The port device circuits including frame ground, and all MDI leads.

55.12.8 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	All implementations of the balanced cabling link shall	TBD	M	Yes [ ]	Be compatible at the MDI.

55.12.9 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	TBD	M	Yes [ ]	8-Way connector as per IEC TBD.