IEEE P802.3bj™/D2.1

Draft Standard for Ethernet Amendment X: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2012. This amendment adds 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables. Draft D2.1 is prepared for Working Group ballot. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2012 adds 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables.

Keywords: 100 Gb/s Ethernet; 100GBASE-CR10; 100GBASE-CR4; 100GBASE-KR4; 100GBASE-KP4; 40 Gb/s Ethernet; 40GBASE-CR4; 40GBASE-KR4; 802.3bj; Auto-Negotiation (AN); Backplane Ethernet; Energy Efficient Ethernet (EEE); Ethernet; Forward Error Correction (FEC); physical medium attachment (PMA) sublayer; physical medium dependent (PMD) sublayer.

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Introduction

Editor's Note (to be removed prior to publication):

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

One exception to IEEE style that is consciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecutively with arabic page numbers.

This introduction is not part of IEEE P802.3bj, IEEE Draft Standard for Ethernet. Amendment X: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2012 and are not maintained as separate documents.

At the date of IEEE Std 802.3bj-201X publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2012

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 90 and Annex 83A through Annex 86A. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 89 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bj™-201X

This amendment includes changes to IEEE Std 802.3-2012 and adds Clause 91 through Clause 94 as well as associated annexes. This amendment adds 100 Gb/s Physical Layer (PHY) specifications and management parameters for operation on electrical backplanes and twinaxial copper cables. This amendment also specifies optional Energy Efficient Ethernet (EEE) for 40 Gb/s and 100 Gb/s operation over electrical backplanes and copper cables.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Draft Standard for Ethernet Amendment X: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. Change is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

1. Introduction

1.4 Definitions

Insert the following definition after 1.4.50:

1.4.50a 100GBASE-P: An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding and a PMD that employs pulse amplitude modulation with more than 2 levels. (See IEEE Std 802.3, Clause 80.)

Change 1.4.51 as follows:

1.4.51 100GBASE-R: ~~An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 82 for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82.)~~ An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding and a PMD that employs 2-level pulse amplitude modulation. (See IEEE Std 802.3, Clause 80.)

Insert the following definitions after 1.4.51:

1.4.51a 100GBASE-R encoding: The physical coding sublayer encoding defined in Clause 82 for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82.)

1.4.51b 100GBASE-CR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m. (See IEEE Std 802.3, Clause 92.)

Insert the following definitions after 1.4.53:

1.4.53a 100GBASE-KP4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz. (See IEEE Std 802.3, Clause 94.)

1.4.53b 100GBASE-KR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz. (See IEEE Std 802.3, Clause 93.)

Change 1.4.60 as follows:

1.4.60 40GBASE-R: ~~An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 82 for 40 Gb/s operation. (See IEEE Std 802.3, Clause 82.)~~ An IEEE 802.3 family of Physical Layer devices using 40GBASE-R encoding and a PMD that employs 2-level pulse amplitude modulation. (See IEEE Std 802.3, Clause 80.)

Insert the following definition after 1.4.60:

1.4.60a 40GBASE-R encoding: The physical coding sublayer encoding defined in Clause 82 for 40 Gb/s operation. (See IEEE Std 802.3, Clause 82.)'

Insert the following definition after 1.4.210:

1.4.210a frame loss ratio: The number of transmitted frames not received as valid by the MAC divided by the total number of transmitted frames.

1.5 Abbreviations

Insert the following new abbreviation into the definitions list in alphabetical order:

DLL Data Link Layer

30. Management

30.2.5 Capabilities

I*nsert two new objects into Table 30-1e, before aIdleErrorCount:*

Table 30–1e—Capabilities

			DTE								Repeater					MAU									
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	10GBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Auto-Negotiation Package (mandatory)	
oMAU managed object class (30.5.1)																									
aRSFECBIPErrorCount	ATTRIBUTE	GET																			X				
aRSFECLaneMapping	ATTRIBUTE	GET																			X				

Insert four new objects into Table 30-1e, before aSNROpMarginChnlA:

Table 30–1e—Capabilities

			DTE							Repeater					MAU								
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	10GBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Auto-Negotiation Package (mandatory)
oMAU managed object class (30.5.1)																							
aRSFECBypassAbility	ATTRIBUTE	GET																				X	
aRSFECIndicationAbility	ATTRIBUTE	GET																				X	
aRSFECBypassEnable	ATTRIBUTE	GET-SET																				X	
aRSFECIndicationEnable	ATTRIBUTE	GET-SET																				X	

Insert the following at the end of Table 30-7:

Table 30–7—LLDP Capabilities

			LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
oLldpXdot3Config managed object class (30.12.1)				
oLldpXdot3LocSystemsGroup managed object class (30.12.2)				
aLldpXdot3LocTxFw	ATTRIBUTE	GET	X	
aLldpXdot3LocTxFwEcho	ATTRIBUTE	GET	X	

Table 30–7—LLDP Capabilities *(continued)*

				LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
aLldpXdot3LocRxFw	ATTRIBUTE	GET		X	
aLldpXdot3LocRxFwEcho	ATTRIBUTE	GET		X	
oLldpXdot3RemSystemsGroup managed object class (30.12.3)					
aLldpXdot3RemTxFw	ATTRIBUTE	GET			X
aLldpXdot3RemTxFwEcho	ATTRIBUTE	GET			X
aLldpXdot3RemRxFw	ATTRIBUTE	GET			X
aLldpXdot3RemRxFwEcho	ATTRIBUTE	GET			X

30.3.2.1.2 aPhyType

Change entry in APPROPRIATE SYNTAX and insert a new entry below that as shown:

APPROPRIATE SYNTAX:

...

100GBASE-R Clause 82 100 Gb/s multi-PCS lane ~~64B/66B~~ using 2-level PAM

100GBASE-P Clause 82 100 Gb/s multi-PCS lane using >2-level PAM

30.3.2.1.3 aPhyTypeList

Change entry in APPROPRIATE SYNTAX and insert a new entry below that as shown:

APPROPRIATE SYNTAX:

...

100GBASE-R Clause 82 100 Gb/s multi-PCS lane ~~64B/66B~~ using 2-level PAM

100GBASE-P Clause 82 100 Gb/s multi-PCS lane using >2-level PAM

30.5.1.1.2 aMAUType

Change entry in APPROPRIATE SYNTAX and insert new entries below that as shown:

APPROPRIATE SYNTAX:

...

100GBASE-R Multi-lane PCS as specified in Clause 82 over undefined 100GBASE-R or 100GBASE-P PMA/PMD

100GBASE-CR4 100GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 92

100GBASE-KR4	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 93
100GBASE-KP4	100GBASE-P PCS/PMA over an electrical backplane PMD as specified in Clause 94

30.5.1.1.11 aBIPErrorCount

Change the first paragraph in BEHAVIOUR DEFINED AS section of 30.5.1.1.11 as shown:

BEHAVIOUR DEFINED AS:

For 40/100GBASE-R PHYs and 100GBASE-P PHYs, an array of BIP error counters. The counters will not increment for other PHY types. The indices of this array (0 to n – 1) denote the PCS lane number where n is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane. Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.

30.5.1.1.12 aLaneMapping

Change the first paragraph in BEHAVIOUR DEFINED AS section of 30.5.1.1.12 as shown:

BEHAVIOUR DEFINED AS:

For 40/100GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to n – 1) denote the service interface lane number where n is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.

Change 30.5.1.1.15, 16, 17, 18 for RS-FEC:

30.5.1.1.15 aFECability

ATTRIBUTE

APPROPRIATE SYNTAX:

~~A ENUMERATION~~ An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC supported
not supported	FEC not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error correction (see 65.2 and Clause 74) or supports the Clause 91 mandatory RS-FEC.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute will map to the FEC capability register (see 45.2.8.2 or 45.2.1.89).;

30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

~~A ENUMERATION~~ An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known

disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the optional FEC sublayer for forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled for a PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable FEC_enable~~d~~ in Clause 74.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute will map to the FEC control register (see 45.2.8.3) for 1000BASE-PX or FEC enable bit in BASE-R FEC control register (see 45.2.1.90).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/40/100GBASE-R, and 100GBASE-P PHYs, an array of corrected FEC block counters. The counters will not increment for other PHY types. The indices of this array (0 to N - 1) denote the PCS lane or FEC lane number where N is the number of PCS lanes or FEC lanes in use. The number of PCS lanes or FEC lanes in use is set to one for PHYs that do not use PCS lanes or FEC lanes. Each element of this array contains a count of corrected FEC blocks for that PCS lane or FEC lane.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.8.5, 45.2.1.91 and 45.2.1.93, or 45.2.1.92c).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, ~~PHYs or~~ 10/40/100GBASE-R, and 100GBASE-P PHYs, an array of uncorrectable FEC block counters. The counters will not increment for other PHY types. The indices of this array (0 to N - 1) denote the PCS lane or FEC lane number where N is the number of PCS lanes or FEC lanes in use. The number of PCS lanes or FEC lanes in use is set to one for PHYs that do not use PCS lanes or FEC lanes. Each element of this array contains a count of

uncorrectable FEC blocks for that PCS lane or FEC lane.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane.

If a Clause 45 MDIO Interface ~~to the PCS~~ is present, then this attribute will map to the FEC uncorrectable blocks counter(s) (see 45.2.8.6, 45.2.1.92, and 45.2.1.94, or 45.2.1.92d).;

Insert 30.5.1.1.26, 27, 28, 29, 30, 31 after 30.5.1.1.25:

30.5.1.1.26 aRSFECBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 100GBASE-R and 100GBASE-P PHYs, an array of BIP error counters. The counters will not increment for other PHY types. The indices of this array (0 to N - 1) denote the PCS lane number where N is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane.

Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.

If a Clause 45 MDIO Interface is present, then this attribute will map to the BIP error counters (see 45.2.1.92h and 45.2.1.92i).;

30.5.1.1.27 aRSFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:

For 100GBASE-R and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to N - 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.

If a Clause 45 MDIO Interface is present, then this attribute will map to the Lane mapping registers (see 45.2.1.92j and 45.2.1.92k).;

30.5.1.1.28 aRSFECBypassAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC bypass ability supported
not supported	FEC bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC bypass ability (see 91.5.3.3).

If a Clause 45 MDIO Interface is present, then this attribute will map to the RS-FEC capability register (see 45.2.1.92b).;

30.5.1.1.29 aRSFECIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC error indication bypass ability supported
not supported	FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC error indication bypass ability (see 91.5.3.3).
If a Clause 45 MDIO Interface is present, then this attribute will map to the RS-FEC capability register (see 45.2.1.92b).;

30.5.1.1.30 aRSFECBypassEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC bypass disabled
enabled	FEC bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC bypass function (see 91.5.3.3).
A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute will map to the RS-FEC control register (see 45.2.1.92b).;

30.5.1.1.31 aRSFECIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC error indication bypass disabled
enabled	FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function (see 91.5.3.3).
A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute will map to the RS-FEC control register (see 45.2.1.92b).;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert 100GBASE-CR4, 100GBASE-KR4, and 100GBASE-KP4 after 100GBASE-CR10 as shown:

APPROPRIATE SYNTAX:
A SEQUENCE that meets the requirements of the description below:

global	Reserved for future use
other	See 30.2.5
unknown	Initializing, true state or type not yet known
10BASE-T	10BASE-T half duplex as defined in Clause 14
10BASE-TFD	Full duplex 10BASE-T as defined in Clause 14 and Clause 31
100BASE-T4	100BASE-T4 half duplex as defined in Clause 23
100BASE-TX	100BASE-TX half duplex as defined in Clause 25
100BASE-TXFD	Full duplex 100BASE-TX as defined in Clause 25 and Clause 31
FDX PAUSE	PAUSE operation for full duplex links as defined in Annex 31B
FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
100BASE-T2	100BASE-T2 half duplex as defined in Clause 32
100BASE-T2FD	Full duplex 100BASE-T2 as defined in Clause 31 and Clause 32
1000BASE-X	1000BASE-X half duplex as specified in Clause 36
1000BASE-XFD	Full duplex 1000BASE-X as specified in Clause 31 and Clause 36
1000BASE-T	1000BASE-T half duplex PHY as specified in Clause 40
1000BASE-TFD	Full duplex 1000BASE-T PHY as specified in Clause 31 and as specified in Clause 40
Rem Fault1	Remote fault bit 1 (RF1) as specified in Clause 37
Rem Fault2	Remote fault bit 2 (RF2) as specified in Clause 37
10GBASE-T	10GBASE-T PHY as specified in Clause 55
1000BASE-KXFD	Full duplex 1000BASE-KX as specified in Clause 70
10GBASE-KX4FD	Full duplex 10GBASE-KX4 as specified in Clause 71
10GBASE-KRFD	Full duplex 10GBASE-KR as specified in Clause 72
40GBASE-KR4	40GBASE-KR4 as specified in Clause 84
40GBASE-CR4	40GBASE-CR4 as specified in Clause 85
100GBASE-CR10	100GBASE-CR10 as specified in Clause 85
100GBASE-CR4	100GBASE-CR4 as specified in Clause 92
100GBASE-KR4	100GBASE-KR4 as specified in Clause 93
100GBASE-KP4	100GBASE-KP4 as specified in Clause 94
Rem Fault	Remote fault bit (RF) as specified in Clause 73
FEC Capable	FEC ability as specified in Clause 73 (see 73.7) and Clause 74
FEC Requested	FEC requested as specified in Clause 73 (see 73.7) and Clause 74
isoethernet	IEEE Std 802.9 ISLAN-16T

30.12 Layer Management for Link Layer Discovery Protocol (LLDP)

30.12.2 LLDP Local System Group managed object class

30.12.2.1 LLDP Local System Group attributes

Insert new subclauses 30.12.2.1.30 through 30.12.2.1.33 after 30.12.2.1.29:

30.12.2.1.30 aLldpXdot3LocTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemFW as defined in 78.4.2.3;

30.12.2.1.31 aLldpXdot3LocTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemFWEcho as defined in 78.4.2.3;

30.12.2.1.32 aLldpXdot3LocRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemFW as defined in 78.4.2.3;

30.12.2.1.33 aLldpXdot3LocRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE

DLL transmitter state diagram. This attribute maps to the variable LocRxSystemFWEcho as defined in 78.4.2.3;

30.12.3 LLDP Remote System Group managed object class

30.12.3.1 LLDP Remote System Group attributes

Insert new subclauses 30.12.3.1.24 through 30.12.2.1.27 after 30.12.2.1.23:

30.12.3.1.24 aLldpXdot3RemTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemFW as defined in 78.4.2.3;

30.12.3.1.25 aLldpXdot3RemTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemFWEcho as defined in 78.4.2.3;

30.12.3.1.26 aLldpXdot3RemRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemFW as defined in 78.4.2.3;

30.12.3.1.27 aLldpXdot3RemRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemFWEcho as defined in 78.4.2.3;

45. Management Data Input/Output (MDIO) Interface

45.2.1 PMA/PMD registers

Replace the 3 identified reserved rows in Table 45-3 with the rows shown in the 3 instances:

Table 45–3—PMA/PMD registers

Register address	Register name	Clause
~~1.162 through 1.169~~	~~Reserved~~	
1.162 through 1.164	PMA overhead control 1, 2, and 3 registers	45.2.1.88a
1.165, 1.166	PMA overhead status 1 and 2 registers	45.2.1.88b
1.167 through 1.169	Reserved	

Table 45–3—PMA/PMD registers

Register address	Register name	Clause
~~1.176 through 1.299~~	~~Reserved~~	
1.176 through 1.199	Reserved	
1.200	RS-FEC control register	45.2.1.92a
1.201	RS-FEC status register	45.2.1.92b
1.202, 1.203	RS-FEC corrected codewords counter	45.2.1.92c
1.204, 1.205	RS-FEC uncorrected codewords counter	45.2.1.92d
1.206	RS-FEC lane mapping register	45.2.1.92e
1.207 through 1.209	Reserved	
1.210 through 1.217	RS-FEC symbol error counter, FEC lanes 0 to 3	45.2.1.92f
1.218 through 1.229	Reserved	
1.230 through 1.249	RS-FEC BIP error counter, PCS lanes 0 to 19	45.2.1.92h
1.250 through 1.269	RS-FEC PCS lane mapping, lanes 0 to 19	45.2.1.92j
1.270 through 1.279	Reserved	
1.280 through 1.283	RS-FEC PCS alignment status 1 through 4	45.2.1.92l
1.284 through 1.299	Reserved	

Table 45–3—PMA/PMD registers

Register address	Register name	Clause
~~1.1410 through 1.1499~~	~~Reserved~~	
1.1410 through 1.1449	Reserved	
1.1450 through 1.1453	PMD training pattern, lanes 0 to 3	45.2.1.98a
1.1454 through 1.1499	Reserved	

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

Change the first row of Table 45-5 and insert the following rows below that row:

Table 45–5—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1.15:~~8~~10	Reserved	~~Ignore on read~~ Value always 0, writes ignored	RO
1.1.9	PIASA	PMA ingress AUI stop ability	RO
1.1.8	PEASA	PMA egress AUI stop ability	RO

[a]RO = Read only

Insert the following subclauses before 45.2.1.2.1:

45.2.1.2.a PMA ingress AUI stop ability (1.1.9)

If bit 1.1.9 is set to one, then the PMA is indicating that the PMA sublayer attached by the ingress AUI is permitted to stop signaling during LPI. If the bit is set to zero then the PMA is indicating that the PMA sublayer attached by the ingress AUI is not permitted to stop signaling during LPI. If the PMA sublayer attached by the ingress AUI does not support EEE capability or is not capable to stop signaling then this bit has no effect.

45.2.1.2.b PMA egress AUI stop ability (1.1.8)

If bit 1.1.8 is set to one, then the PMA is indicating that the PMA sublayer attached by the egress AUI is permitted to stop signaling during LPI. If the bit is set to zero then the PMA is indicating that the PMA sublayer attached by the egress AUI is not permitted to stop signaling during LPI. If the PMA sublayer attached by the egress AUI does not support EEE capability or is not capable to stop signaling then this bit has no effect.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45-7 as follows:

Insert the following subclauses before 45.2.1.6.1:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:~~6~~10	Reserved	Value always 0, writes ignored	R/W
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7:6	Reserved	Value always 0, writes ignored	R/W
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = reserved for future use ~~1 0 1 1 x x = reserved for future use~~ 1 0 1 1 1 1 = reserved for future use 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD type 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD type 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD type 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD type 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD type 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD type 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD type 1 0 0 1 1 x = reserved for future use 1 0 0 1 0 1 = reserved for future use 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD type 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD type 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD type 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD type 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD type 0 1 1 1 x x = reserved 0 1 1 0 1 1 = reserved 0 1 1 0 1 0 = 10GBASE-PR-U3 0 1 1 0 0 1 = 10GBASE-PR-U1 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 1 0 1 0 1 = 10GBASE-PR-D3 0 1 0 1 0 0 = 10GBASE-PR-D2 0 1 0 0 1 1 = 10GBASE-PR-D1 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 1 1 1 1 = 10BASE-T PMA/PMD type 0 0 1 1 1 0 = 100BASE-TX PMA/PMD type 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD type 0 0 1 1 0 0 = 1000BASE-T PMA/PMD type 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD type 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD type 0 0 1 0 0 1 = 10GBASE-T PMA type 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD type 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

[a]R/W = Read/Write

45.2.1.6.a PMA ingress AUI stop enable (1.7.9)

If bit 1.7.9 is set to 1 then the PMA may stop the ingress direction AUI signaling during LPI otherwise it shall keep active signaling on that AUI. If the PMA does not support EEE capability or is not able to stop the ingress direction AUI signaling (see 45.2.1.2.a) then this bit has no effect.

45.2.1.6.b PMA egress AUI stop enable (1.7.8)

If bit 1.7.8 is set to 1 then the PMA may stop the egress direction AUI signaling during LPI otherwise it shall keep active signaling on that AUI. If the PMA does not support EEE capability or is not able to stop the egress direction AUI signaling (see 45.2.1.2.b) then this bit has no effect.

45.2.1.7.4 Transmit fault (1.8.11)

Insert the following rows at the bottom of Table 45-9:

Table 45–9—Transmit fault description location

PMA/PMD	Description location
100GBASE-CR4	92.7.10
100GBASE-KR4	93.7.10
100GBASE-KP4	94.3.8

45.2.1.7.5 Receive fault (1.8.10)

Insert the following rows at the bottom of Table 45-10:

Table 45–10—Receive fault description location

PMA/PMD	Description location
100GBASE-CR4	92.7.11
100GBASE-KR4	93.7.11
100GBASE-KP4	94.3.9

Change 45.2.1.8 for transmit disable:

45.2.1.8 PMD transmit disable register (Register 1.9)

The assignment of bits in the PMD transmit disable register is shown in Table 45-11. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single lane and has implemented the transmit disable function shall use bit 1.9.0

to control the function. Such devices shall ignore writes to bits 1.9.10:1 and return a value of zero for those bits when they are read. The transmit disable function for the 10GBASE-KR PMD is described in 72.6.5, for 10GBASE-LRM serial PMDs in 68.4.7, and for other serial PMDs in 52.4.7. The transmit disable function for the 10GBASE-LX4 PMD is described in 53.4.7. The transmit disable function for the 10GBASE-CX4 PMD is described in 54.5.6. The transmit disable function for 10GBASE-KX4 is described in 71.6.6. The transmit disable function for the 10GBASE-T PMA is described in 55.4.2.3. The transmit disable function for 40GBASE-KR4 is described in 84.7.6. The transmit disable function for 40GBASE-CR4 and 100GBASE-CR10 is described in 85.7.6. The transmit disable function for 40GBASE-SR4 and 100GBASE-SR10 is described in 86.5.7. The transmit disable function for 40GBASE-FR is described in 89.5.6. The transmit disable function for 40GBASE-LR4 is described in 87.5.7. The transmit disable function for 100GBASE-LR4 and 100GBASE-ER4 is described in 88.5.7. The transmit disable function for 100GBASE-CR4 is described in 92.7.6. The transmit disable function for 100GBASE-KR4 is described in 93.7.6. The transmit disable function for 100GBASE-KP4 is described in 94.3.6.6.

45.2.1.12 40G/100G PMA/PMD extended ability register (Register 1.13)

Insert the following rows into Table 45–15 in place of the reserved row for bits 1.13.14:12:

Table 45–15—40G/100G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.13.14	100GBASE-CR4 ability	1 = PMA/PMD is able to perform 100GBASE-CR4 0 = PMA/PMD is not able to perform 100GBASE-CR4	RO
1.13.13	100GBASE-KR4 ability	1 = PMA/PMD is able to perform 100GBASE-KR4 0 = PMA/PMD is not able to perform 100GBASE-KR4	RO
1.13.12	100GBASE-KP4 ability	1 = PMA/PMD is able to perform 100GBASE-KP4 0 = PMA/PMD is not able to perform 100GBASE-KP4	RO

[a]RO = Read only

Insert the following subclauses after 45.2.1.12.1:

45.2.1.12.1a 100GBASE-CR4 ability (1.13.14)

When read as a one, bit 1.13.14 indicates that the PMA/PMD is able to operate as a 100GBASE-CR4 PMA/PMD type. When read as a zero, bit 1.13.14 indicates that the PMA/PMD is not able to operate as a 100GBASE-CR4 PMA/PMD type.

45.2.1.12.1b 100GBASE-KR4 ability (1.13.13)

When read as a one, bit 1.13.13 indicates that the PMA/PMD is able to operate as a 100GBASE-KR4 PMA/PMD type. When read as a zero, bit 1.13.13 indicates that the PMA/PMD is not able to operate as a 100GBASE-KR4 PMA/PMD type.

45.2.1.12.1c 100GBASE-KP4 ability (1.13.12)

When read as a one, bit 1.13.12 indicates that the PMA/PMD is able to operate as a 100GBASE-KP4 PMA/PMD type. When read as a zero, bit 1.13.12 indicates that the PMA/PMD is not able to operate as a 100GBASE-KP4 PMA/PMD type.

Change 45.2.1.80 as follows:

45.2.1.80 BASE-R PMD status register (Register 1.151)

The BASE-R PMD status register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, ~~or~~ Clause 85, Clause 92, Clause 93, or Clause 94. The assignment of bits in the BASE-R PMD status register is shown in Table 45–59.

Change the first paragraph of 45.2.1.81 as follows:

45.2.1.81 BASE-R LP coefficient update, lane 0 register (Register 1.152)

The BASE-R LP coefficient update, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, ~~or~~ Clause 85, Clause 92, Clause 93, or Clause 94. The BASE-R LP coefficient update, lane 0 register reflects the contents of the first 16-bit word of the training frame most recently received from the control channel for lane 0 or for a single lane PHY.

Change the first paragraph of 45.2.1.82 as follows:

45.2.1.82 BASE-R LP status report, lane 0 register (Register 1.153)

The BASE-R LP status report, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, ~~or~~ Clause 85, Clause 92, Clause 93, or Clause 94. The BASE-R LP status report, lane 0 register reflects the contents of the second 16-bit word of the training frame most recently received from the control channel for lane 0 or for a single lane PHY.

Change the first paragraph of 45.2.1.83 as follows:

45.2.1.83 BASE-R LD coefficient update, lane 0 register (Register 1.154)

The BASE-R LD coefficient update, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, ~~or~~ Clause 85, Clause 92, Clause 93, or Clause 94. The BASE-R LD coefficient update, lane 0 register reflects the contents of the first 16-bit word of the outgoing training frame as defined by the LD receiver adaptation process in 72.6.10.2.5 for lane 0 or for a single lane PHY.

Change the first paragraph of 45.2.1.84 as follows:

45.2.1.84 BASE-R LD status report, lane 0 register (Register 1.155)

The BASE-R LD status report, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, ~~or~~ Clause 85, Clause 92, Clause 93, or Clause 94. The BASE-R LD status report, lane 0 register reflects the contents of the second 16-bit word of the current outgoing training frame, as defined in the training state diagram in Figure 72–5 for lane 0 or for a single lane PHY.

Insert 45.2.1.88a, 45.2.1.88b before 45.2.1.89 for PMA overhead control and status:

45.2.1.88a PMA overhead control 1, 2, and 3 registers (Register 1.162 through 1.164)

Assignment of bits in the PMA overhead control 1, 2, and 3 registers is shown in Table 45–67b. These bits shall be reset to the default values indicated in Table 45–67a upon PHY reset. For the 100GBASE-KP4 PHY the use of these registers is specified in 94.2.2.3 and 94.2.3.1.

Table 45–67a—PMA overhead control 1, 2, and 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.162.15:13	Reserved	Value always zero, writes ignored	RO
1.162.12:8	PMA transmit overhead sequence 0	Sequence of overhead groups for lane 0 Default = 00110	R/W
1.162.7:0	PMA transmit overhead pattern	Bit pattern for 8-bit transmit overhead group Default = 01100110	R/W
1.163.15	Reserved	Value always zero, writes ignored	RO
1.163.14:10	PMA transmit overhead sequence 3	Sequence of overhead groups for lane 3 Default = 11001	R/W
1.163.9:5	PMA transmit overhead sequence 2	Sequence of overhead groups for lane 2 Default = 10101	R/W
1.163.4:0	PMA transmit overhead sequence 1	Sequence of overhead groups for lane 1 Default = 01010	R/W
1.164.15:8	Reserved	Value always zero, writes ignored	RO
1.164.7:0	PMA receive overhead pattern	Bit pattern for 8-bit receive overhead group Default = 01100110	R/W

[a]R/W = Read/Write, RO Read only

45.2.1.88b PMA overhead status 1 and 2 registers (Register 1.165, 1.166)

Assignment of bits in the PMA overhead status 1 and 2 registers is shown in Table 45–67b. These bits shall be reset to all zeros upon PHY reset. For the 100GBASE-KP4 PHY the use of these registers is specified in 94.2.3.1.

Table 45–67b—PMA overhead control 1, 2, and 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.165.15:12	Reserved	Value always zero, writes ignored	RO
1.165.11:6	PMA receive status 1	Sequence of overhead groups for lane 1	RO
1.165.5:0	PMA receive status 0	Sequence of overhead groups for lane 0	RO
1.166.15:12	Reserved	Value always zero, writes ignored	RO
1.166.11:6	PMA receive status 3	Sequence of overhead groups for lane 3	RO
1.166.5:0	PMA receive status 2	Sequence of overhead groups for lane 2	RO

[a]R/W = Read/Write, RO Read only

Insert 45.2.1.92a through 45.2.1.92k before 45.2.1.93 for RS-FEC registers:

45.2.1.92a RS-FEC control register (Register 1.200)

The assignment of bits in the RS-FEC control register is shown in Table 45–71a.

Table 45–71a—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.200.15:2	Reserved	Value always zero, writes ignored	RO
1.200.1	FEC bypass indication enable	1 = FEC decoder does not indicate errors to the PCS 0 = FEC decoder indicates errors to the PCS layer	R/W
1.200.0	FEC bypass correction enable	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	R/W

[a]R/W = Read/Write, RO Read only

45.2.1.92a.1 FEC bypass correction enable (1.200.0)

When this bit is set to one the Reed-Solomon decoder performs error detection without error correction (see 91.5.3.3). When this bit is set to zero, the decoder also performs error correction. Writes to this bit are ignored and reads return a zero if the RS-FEC does not have the ability to bypass correction (see 91.5.3.3).

45.2.1.92a.2 FEC bypass indication enable(1.200.1)

This bit enables the RS-FEC decoder to bypass error indication to the upper layers (PCS) through the sync bits for the BASE-R PHY in the Local Device. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the PCS through the sync bits. Writes to this bit are ignored and reads return a zero if the RS-FEC does not have the ability to bypass indicating decoding errors to the PCS layer (see 91.5.3.3).

45.2.1.92b RS-FEC status register (Register 1.201)

The assignment of bits in the RS-FEC status register is shown in Table 45–71b.

Table 45–71b—RS-FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.201.15	PCS align status	1 = FEC decoder has locked and aligned all PCS lanes 0 = FEC decoder has not locked and aligned all PCS lanes	RO
1.201.14:3	Reserved	Value always zero, writes ignored	RO
1.201.2	RS-FEC high SER	1 = FEC errors have exceeded threshold 0 = FEC errors have not exceeded threshold	RO/LH
1.201.1	FEC bypass indication ability	1 = FEC decoder has the ability to bypass error indication 0 = FEC decoder does not have the ability to bypass error indication	RO
1.201.0	FEC bypass correction ability	1 = FEC decoder has the ability to bypass error correction 0 = FEC decoder does not have the ability to bypass error correction	RO

[a]RO Read only, LH Latching high

45.2.1.92b.1 FEC bypass correction ability (1.201.0)

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass error correction. The bit is set to zero if this ability is not supported.

45.2.1.92b.2 FEC bypass indication ability (1.201.1)

The Reed-Solomon decoder may have the option to perform error detection without error indication (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

45.2.1.92b.3 RS-FEC high SER (1.201.2)

When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 91.5.3.3) and is set to zero otherwise. The bit is set to zero if FEC_bypass_indication_enable is set to zero. This bit shall be implemented with latching high behavior.

45.2.1.92b.4 PCS align status (1.201.15)

When read as a one, bit 1.201.15 indicates that the RS-FEC described in Clause 91 has locked and aligned all transmit PCS lanes. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not locked and aligned all transmit PCS lanes.

45.2.1.92c RS-FEC corrected codewords counter (Register 1.202, 1.203)

The assignment of bits in the RS-FEC corrected codewords counter register is shown in Table 45–71c. See 91.6.6 for a definition of this register. These bits shall be reset to all zeros when the register is read by the

management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.202, 1.203 are used to read the value of a 32-bit counter. When registers 1.202 and 1.203 are used to read the 32-bit counter value, the register 1.202 is read first, the value of the register 1.203 is latched when (and only when) register 1.202 is read and reads of register 1.203 returns the latched value rather than the current value of the counter.

Table 45–71c—RS-FEC corrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.202.15:0	FEC corrected codewords lower	FEC_corrected_cw_counter[15:0]	RO, NR
1.203.15:0	FEC corrected codewords upper	FEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.92d RS-FEC uncorrected codewords counter (Register 1.204, 1.205)

The assignment of bits in the RS-FEC uncorrected codewords counter register is shown in Table 45–71d. See 91.6.7 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.204, 1.205 are used to read the value of a 32-bit counter. When registers 1.204 and 1.205 are used to read the 32-bit counter value, the register 1.204 is read first, the value of the register 1.205 is latched when (and only when) register 1.204 is read and reads of register 1.205 returns the latched value rather than the current value of the counter.

Table 45–71d—RS-FEC uncorrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.204.15:0	FEC uncorrected codewords lower	FEC_uncorrected_cw_counter[15:0]	RO, NR
1.205.15:0	FEC uncorrected codewords upper	FEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.92e RS-FEC lane mapping register (Register 1.206)

The assignment of bits in the RS-FEC lane mapping register is shown in Table 45–71e. When read as a one, bit 1.206.15 indicates that the RS-FEC described in Clause 91 has locked and aligned all receive lanes. When read as a zero, bit 1.206.15 indicates that the RS-FEC has not locked and aligned all receive lanes. When the RS-FEC detects and locks the RS-FEC for PMA service interface lane 0, the detected RS-FEC lane number is recorded bits 1:0 in this register. Similarly, the detected RS-FEC lane numbers for PMA service lanes 1, 2, and 3 are recorded in register bits 3:2, 5:4, and 7:6 respectively. The contents of the RS-FEC

lane mapping register bits 7:0 are valid when RS-FEC align status (1.206.15) is set to one and are invalid otherwise.

Table 45–71e—RS-FEC lane mapping register

Bit(s)	Name	Description	R/W[a]
1.206.15	RS-FEC align status	1 = RS-FEC receive lanes locked and aligned 0 = RS-FEC receive lanes not locked and aligned	RO
1.206.14:8	Reserved		RO
1.206.7:6	RS-FEC lane 3 mapping	RS-FEC lane mapped to PMA lane 3	RO
1.206.5:4	RS-FEC lane 2 mapping	RS-FEC lane mapped to PMA lane 2	RO
1.206.3:2	RS-FEC lane 1 mapping	RS-FEC lane mapped to PMA lane 1	RO
1.206.1:0	RS-FEC lane 0 mapping	RS-FEC lane mapped to PMA lane 0	RO

[a]RO = Read only

45.2.1.92f RS-FEC symbol errors counter lane 0 (Register 1.210, 1.211)

The assignment of bits in the RS-FEC symbol errors counter lane 0 register is shown in Table 45–71f. Symbol errors detected in FEC lane 0 are counted and shown in register 1.210.15:0 and 1.211.15:0. See 91.6.10 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.210, 1.211 are used to read the value of a 32-bit counter. When registers 1.210 and 1.211 are used to read the 32-bit counter value, the register 1.210 is read first, the value of the register 1.211 is latched when (and only when) register 1.210 is read and reads of register 1.211 returns the latched value rather than the current value of the counter.

Table 45–71f—RS-FEC symbol errors counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.210.15:0	FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO, NR
1.211.15:0	FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.92g RS-FEC symbol errors counter lanes 1 through 3 (Register 1.212, 1.213, 1.214, 1.215, 1.216, 1.217)

The behavior of the RS-FEC symbol errors counters, lanes 1 through 3 is identical to that described for FEC lane 0 in 45.2.1.92f. Errors detected in each FEC lane are counted and shown in the corresponding register. FEC lane 1, lower 16 bits are shown in register 1.212; FEC lane 1, upper 16 bits are shown in register 1.213; FEC lane 2, lower 16 bits are shown in register 1.214; through register 1.217 for FEC lane 3, upper 16 bits.

45.2.1.92h RS-FEC BIP error counter lane 0 (Register 1.230)

The assignment of bits in the RS-FEC BIP error counter lane 0 is shown in Table 45–71g. The RS-FEC described in Clause 91 calculates a BIP value for each PCS lane (see 91.5.2.4, 91.6.11). Errors detected in PCS lane 0 are counted and shown in register 1.230.15:0. The 16-bit counter shall be reset to all zeros when register 1.230 is read or upon PMA/PMD reset. The 16-bit counter shall be held at all ones in the case of overflow.

Table 45–71g—RS-FEC BIP error counter, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.230.15:0	BIP error counter, lane 0	Errors detected by BIP in PCS lane 0	RO

[a]RO = Read only

45.2.1.92i RS-FEC BIP error counter, lanes 1 through 19 (Registers 1.231 through 1.249)

The behavior of the RS-FEC BIP error counters, lanes 1 through 19 is identical to that described for PCS lane 0 in 45.2.1.92h. Errors detected in each PCS lane are counted and shown in register bits 15:0 in the corresponding register. PCS lane 1 is shown in register 1.231; PCS lane 2 is shown in register 1.232; through register 1.249 for PCS lane 19.

45.2.1.92j RS-FEC PCS lane 0 mapping register (Register 1.250)

The assignment of bits in the RS-FEC PCS lane 0 mapping register is shown in Table 45–71h. When the RS-FEC instance of the multi-lane PCS described in Clause 82 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the Lane 0 mapping register is valid when the transmit PCS lane alignment status bit (register 1.201.15) is set to one and is invalid otherwise (see 45.2.1.92b).

Table 45–71h—Lane 0 mapping register bit definitions

Bit(s)	Name	Description	R/W[a]
1.250.15:5	Reserved	Value always 0, writes ignored	RO
1.250.4:0	Lane 0 mapping	PCS lane received in service interface lane 0	RO

[a]RO = Read only

45.2.1.92k RS-FEC PCS lanes 1 through 19 mapping registers (Registers 1.251 through 1.269)

The definition of Lanes 1 through 19 mapping registers is identical to that described for lane 0 in 45.2.1.92j. The lane mapping for lane 1 is in register 1.251; lane 2 is in register 1.252; etc.

45.2.1.92l RS-FEC PCS alignment status 1 register (Register 1.280)

The assignment of bits in the RS-FEC PCS alignment status 1 register is shown in Table 45–71i. All the bits in the RS-FEC PCS alignment status 1 register are read only; a write to the RS-FEC PCS alignment status 1 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC PCS alignment status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–71i—RS-FEC PCS alignment status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.280.15:8	Reserved	Value always zero, writes ignored	RO
1.280.7	Block 7 lock	1 = Lane 7 is locked 0 = Lane 7 is not locked	RO
1.280.6	Block 6 lock	1 = Lane 6 is locked 0 = Lane 6 is not locked	RO
1.280.5	Block 5 lock	1 = Lane 5 is locked 0 = Lane 5 is not locked	RO
1.280.4	Block 4 lock	1 = Lane 4 is locked 0 = Lane 4 is not locked	RO
1.280.3	Block 3 lock	1 = Lane 3 is locked 0 = Lane 3 is not locked	RO
1.280.2	Block 2 lock	1 = Lane 2 is locked 0 = Lane 2 is not locked	RO
1.280.1	Block 1 lock	1 = Lane 1 is locked 0 = Lane 1 is not locked	RO
1.280.0	Block 0 lock	1 = Lane 0 is locked 0 = Lane 0 is not locked	RO

[a]RO = Read only

45.2.1.92l.1 Block 7 lock (1.280.7)

When read as a one, bit 1.280.7 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 7. When read as a zero, bit 1.280.7 indicates that the RS-FEC transmit function lane 7 has not achieved block lock. This bit reflects the state of block_lock[7] (see 91.5.2.1).

45.2.1.92l.2 Block 6 lock (1.280.6)

When read as a one, bit 1.280.6 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 6. When read as a zero, bit 1.280.6 indicates that the RS-FEC transmit function lane 6 has not achieved block lock.. This bit reflects the state of block_lock[6] (see 91.5.2.1).

45.2.1.92l.3 Block 5 lock (1.280.5)

When read as a one, bit 1.280.5 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 5. When read as a zero, bit 1.280.5 indicates that the RS-FEC transmit function lane 5 has not achieved block lock.. This bit reflects the state of block_lock[5] (see 91.5.2.1).

45.2.1.92l.4 Block 4 lock (1.280.4)

When read as a one, bit 1.280.4 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 4. When read as a zero, bit 1.280.4 indicates that the RS-FEC transmit function lane 4 has not achieved block lock.. This bit reflects the state of block_lock[4] (see 91.5.2.1).

45.2.1.92l.5 Block 3 lock (1.280.3)

When read as a one, bit 1.280.3 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 3. When read as a zero, bit 1.280.3 indicates that the RS-FEC transmit function lane 3 has not achieved block lock.. This bit reflects the state of block_lock[3] (see 91.5.2.1).

45.2.1.92l.6 Block 2 lock (1.280.2)

When read as a one, bit 1.280.2 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 2. When read as a zero, bit 1.280.2 indicates that the RS-FEC transmit function lane 2 has not achieved block lock.. This bit reflects the state of block_lock[2] (see 91.5.2.1).

45.2.1.92l.7 Block 1 lock (1.280.1)

When read as a one, bit 1.280.1 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 1. When read as a zero, bit 1.280.1 indicates that the RS-FEC transmit function lane 1 has not achieved block lock.. This bit reflects the state of block_lock[1] (see 91.5.2.1).

45.2.1.92l.8 Block 0 lock (1.280.0)

When read as a one, bit 1.280.0 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 0. When read as a zero, bit 1.280.0 indicates that the RS-FEC transmit function lane 0 has not achieved block lock.. This bit reflects the state of block_lock[0] (see 91.5.2.1).

45.2.1.92m RS-FEC PCS alignment status 2 register (Register 1.281)

The assignment of bits in the RS-FEC PCS alignment status 2 register is shown in Table 45–71j. All the bits in the RS-FEC PCS alignment status 2 register are read only; a write to the RS-FEC PCS alignment status 2 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC PCS alignment status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

45.2.1.92m.1 Block 19 lock (1.281.11)

When read as a one, bit 1.281.11 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 19. When read as a zero, bit 1.281.11 indicates that the RS-FEC transmit function lane 19 has not achieved block lock. This bit reflects the state of block_lock[19] (see 91.5.2.1).

45.2.1.92m.2 Block 18 lock (1.281.10)

When read as a one, bit 1.281.10 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 18. When read as a zero, bit 1.281.10 indicates that the RS-FEC transmit function lane

Table 45–71j—RS-FEC PCS alignment status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.281.15:12	Reserved	Value always zero, writes ignored	RO
1.281.11	Block 19 lock	1 = Lane 19 is locked 0 = Lane 19 is not locked	RO
1.281.10	Block 18 lock	1 = Lane 18 is locked 0 = Lane 18 is not locked	RO
1.281.9	Block 17 lock	1 = Lane 17 is locked 0 = Lane 17 is not locked	RO
1.281.8	Block 16 lock	1 = Lane 16 is locked 0 = Lane 16 is not locked	RO
1.281.7	Block 15 lock	1 = Lane 15 is locked 0 = Lane 15 is not locked	RO
1.281.6	Block 14 lock	1 = Lane 14 is locked 0 = Lane 14 is not locked	RO
1.281.5	Block 13 lock	1 = Lane 13 is locked 0 = Lane 13 is not locked	RO
1.281.4	Block 12 lock	1 = Lane 12 is locked 0 = Lane 12 is not locked	RO
1.281.3	Block 11 lock	1 = Lane 11 is locked 0 = Lane 11 is not locked	RO
1.281.2	Block 10 lock	1 = Lane 10 is locked 0 = Lane 10 is not locked	RO
1.281.1	Block 9 lock	1 = Lane 9 is locked 0 = Lane 9 is not locked	RO
1.281.0	Block 8 lock	1 = Lane 8 is locked 0 = Lane 8 is not locked	RO

[a]RO = Read only

18 has not achieved block lock This bit reflects the state of block_lock[18] (see 91.5.2.1).

45.2.1.92m.3 Block 17 lock (1.281.9)

When read as a one, bit 1.281.9 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 17. When read as a zero, bit 1.281.9 indicates that the RS-FEC transmit function lane 17 has not achieved block lock This bit reflects the state of block_lock[17] (see 91.5.2.1).

45.2.1.92m.4 Block 16 lock (1.281.8)

When read as a one, bit 1.281.8 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 16. When read as a zero, bit 1.281.8 indicates that the RS-FEC transmit function lane 16 has not achieved block lock This bit reflects the state of block_lock[16] (see 91.5.2.1).

45.2.1.92m.5 Block 15 lock (1.281.7)

When read as a one, bit 1.281.7 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 15. When read as a zero, bit 1.281.7 indicates that the RS-FEC transmit function lane 15 has not achieved block lock This bit reflects the state of block_lock[15] (see 91.5.2.1).

45.2.1.92m.6 Block 14 lock (1.281.6)

When read as a one, bit 1.281.6 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 14. When read as a zero, bit 1.281.6 indicates that the RS-FEC transmit function lane 14 has not achieved block lock This bit reflects the state of block_lock[14] (see 91.5.2.1).

45.2.1.92m.7 Block 13 lock (1.281.5)

When read as a one, bit 1.281.5 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 13. When read as a zero, bit 1.281.5 indicates that the RS-FEC transmit function lane 13 has not achieved block lock This bit reflects the state of block_lock[13] (see 91.5.2.1).

45.2.1.92m.8 Block 12 lock (1.281.4)

When read as a one, bit 1.281.4 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 12. When read as a zero, bit 1.281.4 indicates that the RS-FEC transmit function lane 12 has not achieved block lock This bit reflects the state of block_lock[12] (see 91.5.2.1).

45.2.1.92m.9 Block 11 lock (1.281.3)

When read as a one, bit 1.281.3 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 11. When read as a zero, bit 1.281.3 indicates that the RS-FEC transmit function lane 11 has not achieved block lock This bit reflects the state of block_lock[11] (see 91.5.2.1).

45.2.1.92m.10 Block 10 lock (1.281.2)

When read as a one, bit 1.281.2 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 10. When read as a zero, bit 1.281.2 indicates that the RS-FEC transmit function lane 10 has not achieved block lock This bit reflects the state of block_lock[10] (see 91.5.2.1).

45.2.1.92m.11 Block 9 lock (1.281.1)

When read as a one, bit 1.281.1 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 9. When read as a zero, bit 1.281.1 indicates that the RS-FEC transmit function lane 9 has not achieved block lock This bit reflects the state of block_lock[9] (see 91.5.2.1).

45.2.1.92m.12 Block 8 lock (1.281.0)

When read as a one, bit 1.281.0 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 8. When read as a zero, bit 1.281.0 indicates that the RS-FEC transmit function lane 8 has not achieved block lock This bit reflects the state of block_lock[8] (see 91.5.2.1).

45.2.1.92n RS-FEC PCS alignment status 3 register (Register 1.282)

The assignment of bits in the RS-FEC PCS alignment status 3 register is shown in Table 45–71k. All the bits in the RS-FEC PCS alignment status 3 register are read only; a write to the RS-FEC PCS alignment status 3 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all

bits in the RS-FEC PCS alignment status 3 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–71k—RS-FEC PCS alignment status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.282.15:8	Reserved	Value always zero, writes ignored	RO
1.282.7	Lane 7 aligned	1 = Lane 7 alignment marker is locked 0 = Lane 7 alignment marker is not locked	RO
1.282.6	Lane 6 aligned	1 = Lane 6 alignment marker is locked 0 = Lane 6 alignment marker is not locked	RO
1.282.5	Lane 5 aligned	1 = Lane 5 alignment marker is locked 0 = Lane 5 alignment marker is not locked	RO
1.282.4	Lane 4 aligned	1 = Lane 4 alignment marker is locked 0 = Lane 4 alignment marker is not locked	RO
1.282.3	Lane 3 aligned	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked	RO
1.282.2	Lane 2 aligned	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked	RO
1.282.1	Lane 1 aligned	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked	RO
1.282.0	Lane 0 aligned	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked	RO

[a]RO = Read only

45.2.1.92n.1 Lane 7 aligned (1.282.7)

When read as a one, bit 1.282.7 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 7. When read as a zero, bit 1.282.7 indicates that the RS-FEC transmit function lane 7 has not achieved alignment marker lock. This bit reflects the state of am_lock[7] (see 91.5.2.2).

45.2.1.92n.2 Lane 6 aligned (1.282.6)

When read as a one, bit 1.282.6 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 6. When read as a zero, bit 1.282.6 indicates that the RS-FEC transmit function lane 6 has not achieved alignment marker lock. This bit reflects the state of am_lock[6] (see 91.5.2.2).

45.2.1.92n.3 Lane 5 aligned (1.282.5)

When read as a one, bit 1.282.5 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 5. When read as a zero, bit 1.282.5 indicates that the RS-FEC transmit function lane 5 has not achieved alignment marker lock. This bit reflects the state of am_lock[5] (see 91.5.2.2).

45.2.1.92n.4 Lane 4 aligned (1.282.4)

When read as a one, bit 1.282.4 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 4. When read as a zero, bit 1.282.4 indicates that the RS-FEC transmit function lane 4 has not achieved alignment marker lock. This bit reflects the state of am_lock[4] (see 91.5.2.2).

45.2.1.92n.5 Lane 3 aligned (1.282.3)

When read as a one, bit 1.282.3 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 3. When read as a zero, bit 1.282.3 indicates that the RS-FEC transmit function lane 3 has not achieved alignment marker lock. This bit reflects the state of am_lock[3] (see 91.5.2.2).

45.2.1.92n.6 Lane 2 aligned (1.282.2)

When read as a one, bit 1.282.2 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 2. When read as a zero, bit 1.282.2 indicates that the RS-FEC transmit function lane 2 has not achieved alignment marker lock. This bit reflects the state of am_lock[2] (see 91.5.2.2).

45.2.1.92n.7 Lane 1 aligned (1.282.1)

When read as a one, bit 1.282.1 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 1. When read as a zero, bit 1.282.1 indicates that the RS-FEC transmit function lane 1 has not achieved alignment marker lock. This bit reflects the state of am_lock[1] (see 91.5.2.2).

45.2.1.92n.8 Lane 0 aligned (1.282.0)

When read as a one, bit 1.282.0 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 1.282.0 indicates that the RS-FEC transmit function lane 0 has not achieved alignment marker lock. This bit reflects the state of am_lock[0] (see 91.5.2.2).

45.2.1.92o RS-FEC PCS alignment status 4 register (Register 1.283)

The assignment of bits in the RS-FEC PCS alignment status 4 register is shown in Table 45–71l. All the bits in the RS-FEC PCS alignment status 4 register are read only; a write to the RS-FEC PCS alignment status 4 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC PCS alignment status 4 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

45.2.1.92o.1 Lane 19 aligned (1.283.11)

When read as a one, bit 1.283.11 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 19. When read as a zero, bit 1.283.11 indicates that the RS-FEC transmit function lane 19 has not achieved alignment marker lock. This bit reflects the state of am_lock[19] (see 91.5.2.2).

45.2.1.92o.2 Lane 18 aligned (1.283.10)

When read as a one, bit 1.283.10 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 18. When read as a zero, bit 1.283.10 indicates that the RS-FEC transmit function lane 18 has not achieved alignment marker lock. This bit reflects the state of am_lock[18] (see 91.5.2.2).

Table 45–71l—RS-FEC PCS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.283.15:12	Reserved	Value always zero, writes ignored	RO
1.283.11	Lane 19 aligned	1 = Lane 19 alignment marker is locked 0 = Lane 19 alignment marker is not locked	RO
1.283.10	Lane 18 aligned	1 = Lane 18 alignment marker is locked 0 = Lane 18 alignment marker is not locked	RO
1.283.9	Lane 17 aligned	1 = Lane 17 alignment marker is locked 0 = Lane 17 alignment marker is not locked	RO
1.283.8	Lane 16 aligned	1 = Lane 16 alignment marker is locked 0 = Lane 16 alignment marker is not locked	RO
1.283.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
1.283.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
1.281.28	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
1.283.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
1.283.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
1.283.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
1.283.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
1.283.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a]RO = Read only

45.2.1.92o.3 Lane 17 aligned (1.283.9)

When read as a one, bit 1.283.9 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 17. When read as a zero, bit 1.283.9 indicates that the RS-FEC transmit function lane 17 has not achieved alignment marker lock. This bit reflects the state of am_lock[17] (see 91.5.2.2).

45.2.1.92o.4 Lane 16 aligned (1.283.8)

When read as a one, bit 1.283.8 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 16. When read as a zero, bit 1.283.8 indicates that the RS-FEC transmit function lane 16 has not achieved alignment marker lock. This bit reflects the state of am_lock[16] (see

91.5.2.2).

45.2.1.92o.5 Lane 15 aligned (1.283.7)

When read as a one, bit 1.283.7 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 15. When read as a zero, bit 1.283.7 indicates that the RS-FEC transmit function lane 15 has not achieved alignment marker lock. This bit reflects the state of am_lock[15] (see 91.5.2.2).

45.2.1.92o.6 Lane 14 aligned (1.283.6)

When read as a one, bit 1.283.6 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 14. When read as a zero, bit 1.283.6 indicates that the RS-FEC transmit function lane 14 has not achieved alignment marker lock. This bit reflects the state of am_lock[14] (see 91.5.2.2).

45.2.1.92o.7 Lane 13 aligned (1.281.28)

When read as a one, bit 1.281.28 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 13. When read as a zero, bit 1.281.28 indicates that the RS-FEC transmit function lane 13 has not achieved alignment marker lock. This bit reflects the state of am_lock[13] (see 91.5.2.2).

45.2.1.92o.8 Lane 12 aligned (1.283.4)

When read as a one, bit 1.283.4 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 12. When read as a zero, bit 1.283.4 indicates that the RS-FEC transmit function lane 12 has not achieved alignment marker lock. This bit reflects the state of am_lock[12] (see 91.5.2.2).

45.2.1.92o.9 Lane 11 aligned (1.283.3)

When read as a one, bit 1.283.3 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 11. When read as a zero, bit 1.283.3 indicates that the RS-FEC transmit function lane 11 has not achieved alignment marker lock. This bit reflects the state of am_lock[11] (see 91.5.2.2).

45.2.1.92o.10 Lane 10 aligned (1.283.2)

When read as a one, bit 1.283.2 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 10. When read as a zero, bit 1.283.2 indicates that the RS-FEC transmit function lane 10 has not achieved alignment marker lock. This bit reflects the state of am_lock[10] (see 91.5.2.2).

45.2.1.92o.11 Lane 9 aligned (1.283.1)

When read as a one, bit 1.283.1 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 9. When read as a zero, bit 1.283.1 indicates that the RS-FEC transmit function lane 9 has not achieved alignment marker lock. This bit reflects the state of am_lock[9] (see 91.5.2.2).

45.2.1.92o.12 Lane 8 aligned (1.283.0)

When read as a one, bit 1.283.8 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 1.283.8 indicates that the RS-FEC transmit function lane 0 has not achieved alignment marker lock. This bit reflects the state of am_lock[8] (see 91.5.2.2).

Insert 45.2.1.98a before 45.2.1.99 for PMD training pattern:

45.2.1.98a PMD training pattern lanes 0 through 3 (Register 1.1450 through 1.1453)

The assignment of bits in the PMD training pattern registers, lane 0 through 3, is shown in Table 45–72a. Register 1.1450 controls the PMD training pattern for PMD lane 0; register 1.1451 controls the PMD training pattern for PMD lane 1; etc.

Table 45–72a—PMD training pattern bit definitions

Bit(s)	Name	Description	R/W[a]
1.1450.15:13	Reserved	Value always zero, writes ignored	RO
1.1450.12:11	Polynomial identifier	Identifier (0, 1, 2, or 3) selecting polynomial for PRBS	R/W
1.1450.10:0	Seed	11 bit, binary seed for sequence	R/W

[a]R/W = Read/Write, RO Read only

Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training in the particular PMD lane according to the definition in 92.7.12. The polynomial identifier for each lane shall be unique; therefore no two lanes have the same identifier. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11. Register bits 10:0 contain the 11-bit seed for the sequence, where register bit 0 gives seed bit S0; register bit 1 gives seed bit S1; etc. through register bit 10 gives seed bit S10. The default seeds are (binary): for lane 0, 10101111110; for lane 1, 11001000101; for lane 2, 11100101101; for lane 3, 11110110110. This produces the following initial output (hexadecimal representation where the hex symbols are transmitted from left to right and the most significant bit of each hex symbol is transmitted first): for lane 0, fbf1cb3e; for lane 1, fbb1e665; for lane 2, f3fdae46; for lane 3, f2ffa46b.

Change the reserved row in Table 45-73 and insert new rows immediately beneath it and insert the paragraph at the end of 45.2.1.100 as follows:

45.2.1.100 PRBS pattern testing control (Register 1.1501)

Table 45–73PRBS pattern testing control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1501.15:~~8~~11	Reserved	Value always zero, writes ignored	RO
1.1501.10	QPRBS13 pattern enable	1 = Enable QPRBS13 test-pattern 0 = Disable QPRBS13 test-pattern	R/W
1.1501.9	JP03B pattern enable	1 = Enable JP03B test-pattern 0 = Disable JP03B test-pattern	R/W
1.1501.8	JP03A pattern enable	1 = Enable JP03A test-pattern 0 = Disable JP03A test-pattern	R/W

[a]R/W = Read/Write, RO = Read only

Register 1.1501 bit 8 enables testing with the JP03A pattern defined in 94.2.9.1. Register 1.1501 bit 9 enables testing with the JP03B pattern defined in 94.2.9.2. Register field 1.1501 bit 10 enables testing with the QPRBS13 pattern defined in 94.2.9.3. The assertion of bits 1.1501.8, 1.1501.9, 1.1501.10 are mutually exclusive. If more than one bit is asserted the behavior is undefined. The assertion of 1.1501.8, 1.1501.9, and 1.501.10 operates in conjunction with register 1.1501 bit 3. If bit 1.1501.3 is not asserted then 1.1501.8, 1.1501.9, and 1.1501.10 have no effect.

45.2.3 PCS registers

Change row of Table 45-99 as follows:

Table 45–99—PMA/PMD registers

Register address	Register name	Subclause
3.20	EEE control and capability register	45.2.3.9

Change title of subclause 45.2.3.9 as follows:

45.2.3.9 EEE control and capability (Register 3.20)

Change title of Table 45-105, replace the reserved row for bits 3.20.15:7 as shown, and replace the reserved row for bit 3.20.0 as shown:

Table 45–105—EEE control and capability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15	LPI modes supported	1 = Only fast wake mode is supported 0 = Both fast wake and deep sleep modes are supported	RO
3.20.~~15:7~~14	Reserved	~~Ignore on read~~ Value always 0, writes ignored	RO
3.20.13	100GBASE-CR4 EEE	1 = EEE is supported for 100GBASE-CR4 0 = EEE is not supported for 100GBASE-CR4	RO
3.20.12	100GBASE-KR4 EEE	1 = EEE is supported for 100GBASE-KR4 0 = EEE is not supported for 100GBASE-KR4	RO
3.20.11	100GBASE-KP4 EEE	1 = EEE is supported for 100GBASE-KP4 0 = EEE is not supported for 100GBASE-KP4	RO
3.20.10	100GBASE-CR10 EEE	1 = EEE is supported for 100GBASE-CR10 0 = EEE is not supported for 100GBASE-CR10	RO
3.20.9	Reserved	~~Ignore on read~~ Value always 0, writes ignored	RO
3.20.8	40GBASE-CR4 EEE	1 = EEE is supported for 40GBASE-CR4 0 = EEE is not supported for 40GBASE-CR4	RO
3.20.7	40GBASE-KR4 EEE	1 = EEE is supported for 40GBASE-KR4 0 = EEE is not supported for 40GBASE-KR4	RO
3.20.0	~~Reserved~~ LPI_FW	~~Ignore on read~~ 1 = Fast wake mode is used for LPI function 0 = Deep sleep is used for LPI function	~~RO~~ R/W

[a] R/W = Read/Write, RO = Read only

Insert the following subclauses before 45.2.3.9.1:

45.2.3.9.a LPI modes supported (3.20.15)

If the device only supports fast wake for LPI operation as defined in 78.5, this bit shall be set to a one. If the device supports both fast wake and deep sleep for LPI operation, this bit shall be set to a zero. This bit is not valid for PHYs with rates less than 40 Gb/s, writes are ignored and reads return a zero.

45.2.3.9.b 100GBASE-CR4 EEE supported (3.20.13)

If the device supports EEE operation for 100GBASE-CR4 as defined in 92.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.9.c 100GBASE-KR4 EEE supported (3.20.12)

If the device supports EEE operation for 100GBASE-KR4 as defined in 93.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.9.d 100GBASE-KP4 EEE supported (3.20.11)

If the device supports EEE operation for 100GBASE-KP4 as defined in 94.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.9.e 100GBASE-CR10 EEE supported (3.20.10)

If the device supports EEE operation for 100GBASE-CR10 as defined in 85.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.9.f 40GBASE-CR4 EEE supported (3.20.8)

If the device supports EEE operation for 40GBASE-CR4 as defined in 85.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.9.g 40GBASE-CR4 EEE supported (3.20.7)

If the device supports EEE operation for 40GBASE-KR4 as defined in 84.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

Insert the following subclause after 45.2.3.9.6:

45.2.3.9.7 LPI_FW (3.20.0)

If the device supports Fast Wake as defined in 78.5, this bit selects Fast Wake or deep sleep operation. Setting 3.20.0 to one selects Fast Wake, setting to zero selects deep sleep. This bit is ignored by devices that do not support Fast Wake and this bit defaults to one for devices that support Fast Wake.

45.2.7 Auto-Negotiation registers

45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

Change Table 45–189 as shown:

Table 45–189—Backplane Ethernet, BASE-R copper status register (Register 7.48) bit definitions

Bit(s)	Name	Description	RO[a]
7.48.15:~~9~~12	Reserved	~~Ignore on read~~ Value always 0, writes ignored	RO
7.48.11	100GBASE-CR4	1 = PMA/PMD is negotiated to perform 100GBASE-CR4 0 = PMA/PMD is not negotiated to perform 100GBASE-CR4	RO
7.48.10	100GBASE-KR4	1 = PMA/PMD is negotiated to perform 100GBASE-KR4 0 = PMA/PMD is not negotiated to perform 100GBASE-KR4	RO
7.48.9	100GBASE-KP4	1 = PMA/PMD is negotiated to perform 100GBASE-KP4 0 = PMA/PMD is not negotiated to perform 100GBASE-KP4	RO
7.48.8	100GBASE-CR10	1 = PMA/PMD is negotiated to perform 100GBASE-CR10 0 = PMA/PMD is not negotiated to perform 100GBASE-CR10	RO
7.48.7	Reserved	~~Ignore on read~~ Value always 0, writes ignored	RO
7.48.6	40GBASE-CR4	1 = PMA/PMD is negotiated to perform 40GBASE-CR4 0 = PMA/PMD is not negotiated to perform 40GBASE-CR4	RO
7.48.5	40GBASE-KR4	1 = PMA/PMD is negotiated to perform 40GBASE-KR4 0 = PMA/PMD is not negotiated to perform 40GBASE-KR4	RO
7.48.4	BASE-R FEC negotiated	1 = PMA/PMD is negotiated to perform BASE-R FEC 0 = PMA/PMD is not negotiated to perform BASE-R FEC	RO
7.48.3	10GBASE-KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR 0 = PMA/PMD is not negotiated to perform 10GBASE-KR	RO
7.48.2	10GBASE-KX4	1 = PMA/PMD is negotiated to perform 10GBASE-KX4 or CX4 0 = PMA/PMD is not negotiated to perform 10GBASE-KX4/CX4	RO
7.48.1	1000BASE-KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX 0 = PMA/PMD is not negotiated to perform 1000BASE-KX	RO
7.48.0	BP AN ability	If a Backplane, BASE-R copper PHY type is implemented, this bit is set to 1	RO

[a]RO = Read only

Change 45.2.7.12.2 as shown:

45.2.7.12.2 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11)

When the AN process has been completed as indicated by the AN complete bit, these bits (1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, 100GBASE-CR4) indicate the negotiated port type. Only one of these bits is set depending on the priority resolution function. System developers need to distinguish between parallel detection of 10GBASE-KX4 and 10GBASE-CX4 based on the MDI and media type present.

45.2.7.13 EEE advertisement (Register 7.60)

Change Table 45–190 as shown:

Table 45–190—EEE advertisement register (Register 7.60) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.60.15	LPI modes supported	1 = Advertise that the PHY only supports fast wake for LPI operation 0 = Do not advertise that the PHY supports fast wake only (the PHY supports both fast wake and deep sleep)	73.7.7.1; U15	R/W
7.60.14~~15:7~~	Reserved	~~Ignore on read~~ Value always 0, writes ignored		RO
7.60.13	100GBASE-CR4 EEE	1 = Advertise that the 100GBASE-CR4 has EEE capability 0 = Do not advertise that the 100GBASE-CR4 has EEE capability	73.7.7.1; U13	R/W
7.60.12	100GBASE-KR4 EEE	1 = Advertise that the 100GBASE-KR4 has EEE capability 0 = Do not advertise that the 100GBASE-KR4 has EEE capability	73.7.7.1; U12	R/W
7.60.11	100GBASE-KP4 EEE	1 = Advertise that the 100GBASE-KP4 has EEE capability 0 = Do not advertise that the 100GBASE-KP4 has EEE capability	73.7.7.1; U11	R/W
7.60.10	100GBASE-CR10 EEE	1 = Advertise that the 100GBASE-CR10 has EEE capability 0 = Do not advertise that the 100GBASE-CR10 has EEE capability	73.7.7.1; U10	R/W

Table 45–190—EEE advertisement register (Register 7.60) bit definitions

7.60.9	Reserved	Value always 0, writes ignored		RO
7.60.8	40GBASE-CR4 EEE	1 = Advertise that the 40GBASE-CR4 has EEE capability 0 = Do not advertise that the 40GBASE-CR4 has EEE capability	73.7.7.1; U8	R/W
7.60.7	40GBASE-KR4 EEE	1 = Advertise that the 40GBASE-KR4 has EEE capability 0 = Do not advertise that the 40GBASE-KR4 has EEE capability	73.7.7.1; U7	R/W
7.60.6	10GBASE-KR EEE	1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	73.7.7.1; U6	R/W
7.60.5	10GBASE-KX4 EEE	1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	73.7.7.1; U5	R/W
7.60.4	1000BASE-KX EEE	1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	73.7.7.1; U4	R/W
7.60.3	10GBASE-T EEE	1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	28.2.3.4.1; U3 / 55.6.1; U24	R/W
7.60.2	1000BASE-T EEE	1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	28.2.3.4.1; U2 / 55.6.1; U23	R/W
7.60.1	100BASE-TX EEE	1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	28.2.3.4.1; U1 / 55.6.1; U22	R/W
7.60.0	Reserved	~~Ignore on read~~ Value always 0, writes ignored		RO

[a]R/W = Read/Write, RO = Read only

Insert 45.2.7.13.a through 45.2.7.13.g before 45.2.7.13.1 as follows:

45.2.7.13.a LPI modes supported (7.60.15)

Support for only fast wake mode for LPI operation, as defined in 82.2.18.2.2, shall be advertised if this bit is set to one. This bit is not set for PHYs with rates less than 40 Gb/s and for PHYs that support both fast wake and deep sleep.

45.2.7.13.b 100GBASE-CR4 EEE supported (7.60.13)

Support for EEE operation for 100GBASE-CR4, as defined in 92.1, shall be advertised if this bit is set to one.

45.2.7.13.c 100GBASE-KR4 EEE supported (7.60.12)

Support for EEE operation for 100GBASE-KR4, as defined in 93.1, shall be advertised if this bit is set to one.

45.2.7.13.d 100GBASE-KP4 EEE supported (7.60.11)

Support for EEE operation for 100GBASE-KP4, as defined in 94.1, shall be advertised if this bit is set to one.

45.2.7.13.e 100GBASE-CR10 EEE supported (7.60.10)

Support for EEE operation for 100GBASE-CR10, as defined in 85.1, shall be advertised if this bit is set to one.

45.2.7.13.f 40GBASE-CR4 EEE supported (7.60.8)

Support for EEE operation for 40GBASE-CR4, as defined in 85.1, shall be advertised if this bit is set to one.

45.2.7.13.g 40GBASE-KR4 EEE supported (7.60.7)

Support for EEE operation for 40GBASE-KR4, as defined in 84.1, shall be advertised if this bit is set to one.

45.2.7.14 EEE link partner ability (Register 7.61)

Change Table 45–191 as shown:

Table 45–191—EEE link partner ability (Register 7.61) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.61.15	LPI modes supported	1 = Link partner is advertising only support for fast wake 0 = Link partner is not advertising only fast wake (support for both fast wake and deep sleep)	73.7.7.1; U15	RO
7.61.14~~15~~ ~~.7~~	Reserved	~~Ignore on read~~ Value always 0, writes ignored		RO
7.61.13	100GBASE-CR4 EEE	1 = Link partner is advertising EEE capability for 100GBASE-CR4 0 = Link partner is not advertising EEE capability for 100GBASE-CR4	73.7.7.1; U13	RO
7.61.12	100GBASE-KR4 EEE	1 = Link partner is advertising EEE capability for 100GBASE-KR4 0 = Link partner is not advertising EEE capability for 100GBASE-KR4	73.7.7.1; U12	RO
7.61.11	100GBASE-KP4 EEE	1 = Link partner is advertising EEE capability for 100GBASE-KP4 0 = Link partner is not advertising EEE capability for 100GBASE-KP4	73.7.7.1; U11	RO

Table 45–191—EEE link partner ability (Register 7.61) bit definitions *(continued)*

7.61.10	100GBASE-CR10 EEE	1 = Link partner is advertising EEE capability for 100GBASE-CR10 0 = Link partner is not advertising EEE capability for 100GBASE-CR10	73.7.7.1; U10	RO
7.61.9	Reserved	Value always 0, writes ignored		RO
7.61.8	40GBASE-CR4 EEE	1 = Link partner is advertising EEE capability for 40GBASE-CR4 0 = Link partner is not advertising EEE capability for 40GBASE-CR4	73.7.7.1; U8	RO
7.61.7	40GBASE-KR4 EEE	1 = Link partner is advertising EEE capability for 40GBASE-KR4 0 = Link partner is not advertising EEE capability for 40GBASE-KR4	73.7.7.1; U7	RO
7.61.6	10GBASE-KR EEE	1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	73.7.7.1; U6	RO
7.61.5	10GBASE-KX4 EEE	1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for 10GBASE-KX4	73.7.7.1; U5	RO
7.61.4	1000BASE-KX EEE	1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	73.7.7.1; U4	RO
7.61.3	10GBASE-T EEE	1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	28.2.3.4.1; U3 / 55.6.1; U24	RO
7.61.2	1000BASE-T EEE	1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	28.2.3.4.1; U2 / 55.6.1; U23	RO
7.61.1	100BASE-TX EEE	1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	28.2.3.4.1; U1 / 55.6.1; U22	RO
7.61.0	Reserved	~~Ignore on read~~ Value always 0, writes ignored		RO

[a]R/W = Read/Write, RO = Read only

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) Interface[1]

45.5.3.2 PMA/PMD MMD options

Insert the following row below FEC-R in the table in 45.5.3.2 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*RS-FEC	Implementation of RS-FEC	45.2.1.92b		PMA:O	Yes [ ] No [ ]

45.5.3.3 PMA/PMD management functions

Insert the following row above MM117 in the table in 45.5.3.3 as follows, unchanged rows are not shown:

Item	Feature	Subclause	Value/Comment	Status	Support
MM117a	RS-FEC counters are reset when read or upon PHY reset.	45.2.1.92c, 45.2.1.92d, 45.2.1.92e, 45.2.1.92g, 45.2.1.92h, 45.2.1.92i		RS-FEC:M	Yes [ ] N/A [ ]
MM117b	RS-FEC counters are held at all ones in the case of overflow	45.2.1.92c, 45.2.1.92d, 45.2.1.92e, 45.2.1.92g, 45.2.1.92h, 45.2.1.92i		RS-FEC:M	Yes [ ] N/A [ ]

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69. Introduction to Ethernet operation over electrical backplanes

69.1.1 Scope

Replace the second, third, and fourth paragraphs in 69.1.1 with the following:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC at 1000 Mb/s, 10 Gb/s, 40 Gb/s, or 100 Gb/s providing a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface. For 1000 Mb/s operation, the family of 1000BASE-X Physical Layer signaling systems is extended to include 1000BASE-KX. For 10 Gb/s operation, two Physical Layer signaling systems are defined. For operation over four logical lanes, the 10GBASE-X family is extended to include 10GBASE-KX4. For serial operation, the 10GBASE-R family is extended to include 10GBASE-KR. For 40 Gb/s operation, there is 40GBASE-KR4 that operates over four lanes. For 100 Gb/s operation, the 100GBASE-R family is extended to include 100GBASE-KR4 and 100GBASE-KP4 that operate over four lanes. Auto-Negotiation enables PHY selection amongst Backplane Ethernet Physical Layer signaling systems. Energy Efficient Ethernet (EEE) is optionally supported for all Backplane Ethernet PHYs.

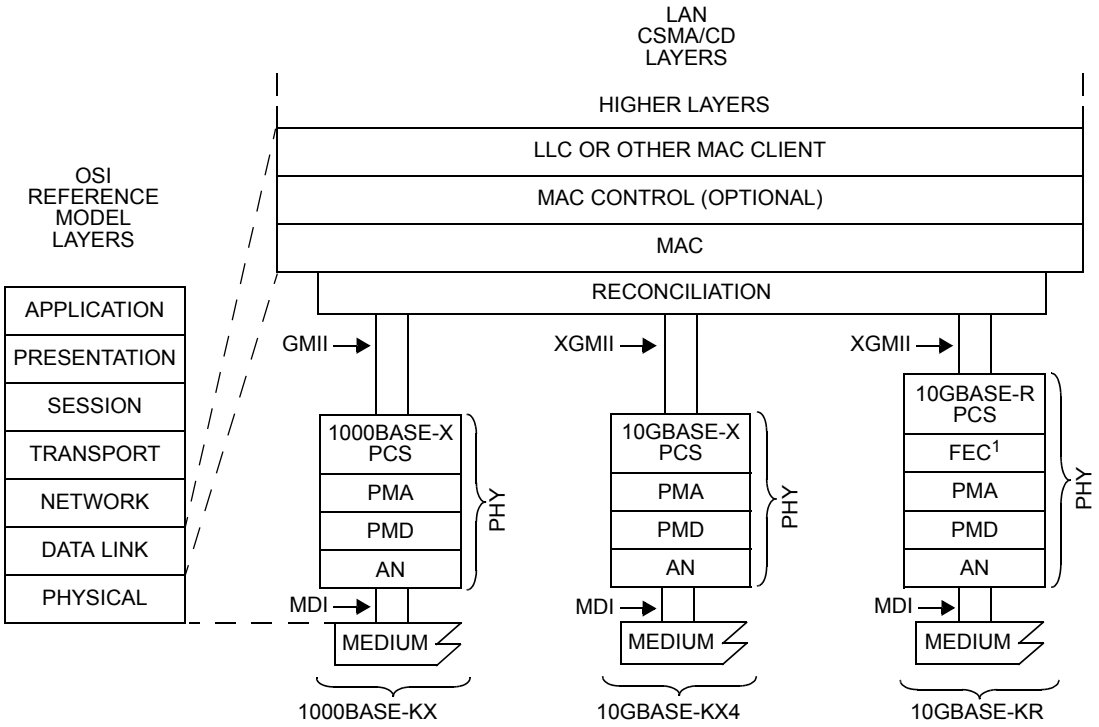
Delete subclause 69.1.2.

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change the first paragraph as shown:

Backplane Ethernet couples the IEEE 802.3 (CSMA/CD) MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1 and Figure 69–1a.

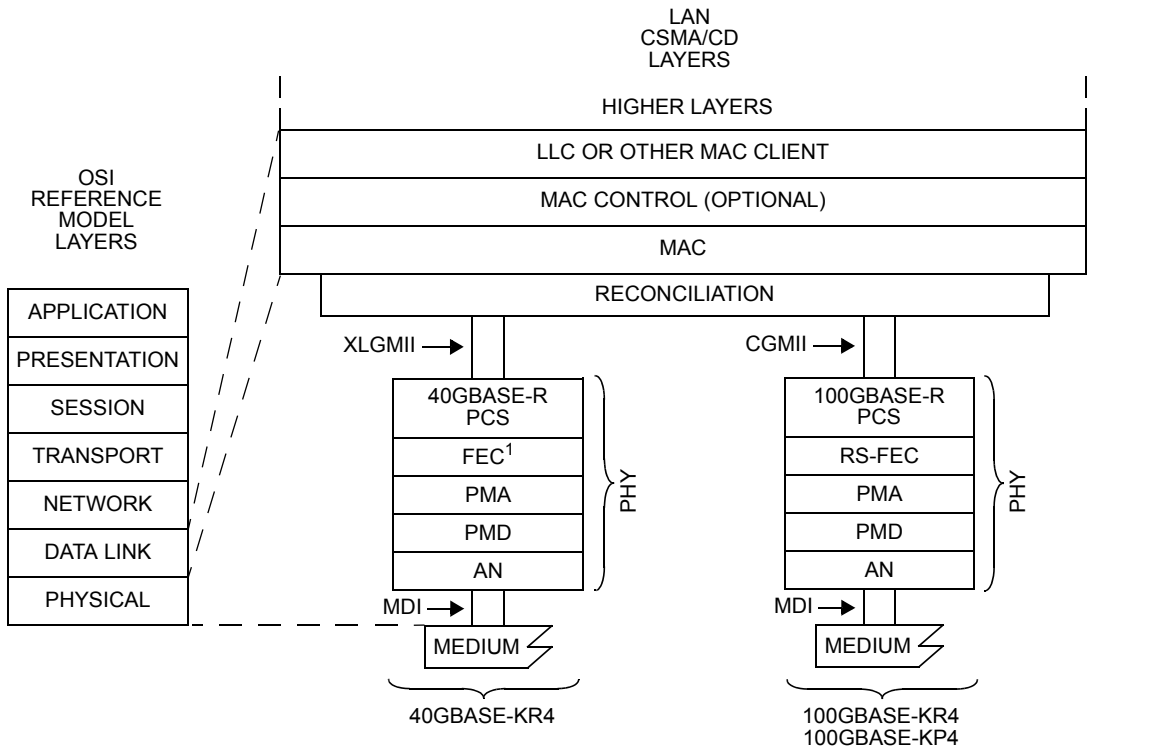
Replace Figure 69–1 and insert Figure 69–1a as shown:



AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL

Figure 69–1—Architectural positioning of 1 Gb/s and 10 Gb/s Backplane Ethernet



AN = AUTO-NEGOTIATION
CGMII = 100 GIGABIT MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FEC
XLGMII = 40 GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL

Figure 69–1a—Architectural positioning of 40 Gb/s and 100 Gb/s Backplane Ethernet

Change item f) and insert item g) as shown:

f) ~~The MDI as specified in Clause 70 for 1000BASE-KX, Clause 71 for 10GBASE-KX4, Clause 72 for 10GBASE-KR, or Clause 84 for 40GBASE-KR4.~~ The PMA service interface, which, when physically implemented as XLAUI (40 Gigabit Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A.

g) The PMA service interface, which, when physically implemented as CAUI (100 Gigabit Attachment Unit Interface) at an observable interconnection port, uses a 10-lane data path as specified in Annex 83A.

h) The MDI for 1000BASE-KX and 10GBASE-KR use a serial data path while the MDI for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, and 100GBASE-KP4 use a four lane data path.

69.2.1 Reconciliation sublayer and media independent interfaces

Change the first paragraph as shown:

The Clause 35 RS and GMII, the Clause 46 RS and XGMII, and the Clause 81 RS ~~and~~, XLGMII, and CGMII are employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.3 Physical Layer signaling systems

Insert the following two paragraphs after the fourth paragraph:

Backplane Ethernet also specifies 100GBASE-KR4 for 100 Gb/s operation using 2-level pulse amplitude modulation (PAM) over four differential signal pairs in each direction for a total of eight pairs where the insertion loss of each pair does not exceed 35 dB at 12.9 GHz. The embodiment of 100GBASE-KR4 employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the PMA defined in Clause 83, and the PMD defined in Clause 93.

Backplane Ethernet also specifies 100GBASE-KP4 for 100 Gb/s operation using 4-level PAM over four differential signal pairs in each direction for a total of eight pairs where the insertion loss of each pair does not exceed 33 dB at 7 GHz. The embodiment of 100GBASE-KP4 employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, and the PMA and PMD defined in Clause 94.

Change the last paragraph as shown:

Table 69–1 and Table 69–1a specify ~~specifies~~ the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Replace Table 69-1 (moving 40GBASE-KR4 to Table 69-1a) and insert Table 69-1a as shown:

Table 69–1—Nomenclature and clause correlation for 1 Gb/s and 10 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause													
	35		36	46		48	49	51	70	71	72	73	74	78
	RS	GMII	1000BASE-X PCS/PMA	RS	XGMII	10GBASE-X PCS/PMA	10GBASE-R PCS	Serial PMA	1000BASE-KX PMD	10GBASE-KX4 PMD	10GBASE-KR PMD	Auto-Negotiation	BASE-R FEC	Energy-Efficient Ethernet (EEE)
1000BASE-KX	M[a]	O[a]	M						M			M		O
10GBASE-KX4				M	O	M				M		M		O
10GBASE-KR				M	O		M	M			M	M	O	O

[a]O = Optional, M = Mandatory

Table 69–1a—Nomenclature and clause correlation for 40 Gb/s and 100 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause															
	73	74	78	81			82		83		83A		84	91	93	94
	Auto-Negotiation	BASE-R FEC	Energy-Efficient Ethernet (EEE)	RS	XLGMII	CGMII	40GBASE-R PCS	100GBASE-R PCS	40GBASE-R PMA	100GBASE-R PMA	XLAUI	CAUI	40GBASE-KR4 PMD	RS-FEC	100GBASE-KR4 PMD	100GBASE-KP4 PMA/PMD
40GBASE-KR4	M[a]	O[a]	O	M	O		M		M		O		M			
100GBASE-KR4	M		O	M		O		M		M		O		M	M	
100GBASE-KP4	M		O	M		O		M				O		M		M

[a]O = Optional, M = Mandatory

69.2.6 Low-Power Idle

Change the first sentence as shown:

With the optional EEE feature, described in Clause 78, Backplane Ethernet PHYs ~~for 10Gb/s or lower~~ can achieve lower power consumption during periods of low link utilization.

69.3 Delay constraints

Insert the following two paragraphs after the last paragraph:

For 100GBASE-KR4, normative delay specifications may be found in 81.1.4, 82.5, 83.5.4, 91.4, and 93.4 and also referenced in 80.4.

For 100GBASE-KP4, normative delay specifications may be found in 81.1.4, 82.5, 91.4, and 94.3.3 and also referenced in 80.4.

69.5 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph as shown:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 91, Clause 93, Clause 94, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

73. Auto-Negotiation for backplane and copper cable assembly

Change the first paragraph of Clause 73 as shown:

Auto-Negotiation defined in this clause was originally intended for use with Backplane Ethernet PHYs. It is also specified for use with 40GBASE-CR4, 100GBASE-CR10, and 100GBASE-CR4 PHYs.

73.3 Functional specifications

Change the last sentence of the third paragraph as shown:

These functions shall comply with the state diagrams from Figure 73–9 through Figure 73–11. The Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology-Dependent interface (see 73.9). Technology-Dependent PHYs include 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, ~~and~~ 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, and 100GBASE-CR4.

73.5.1 DME electrical specifications

Change the last paragraph as shown:

For any multi-lane PHY, DME pages shall be transmitted only on lane 0. The transmitters on other lanes should be disabled as specified in 71.6.7, 84.7.7, ~~or~~ 85.7.7, 92.7.7, 93.7.7, or 94.3.6.7.

73.6.4 Technology Ability Field

Change Table 73–4 as shown:

Table 73–4—Technology Ability Field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3	40GBASE-KR4
A4	40GBASE-CR4
A5	100GBASE-CR10
A6	100GBASE-KP4
A7	100GBASE-KR4
A8	100GBASE-CR4
~~A6~~A9 through A24	Reserved for future technology

Replace the second to last paragraph ("40GBASE-CR4 and...") with the following:

A PHY for operation over an electrical backplane (e.g. 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 100GBASE-KP4, 100GBASE-KR4) shall not be advertised simultaneously with a PHY for operation over a copper cable assembly (e.g. 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4) as the MDI and physical medium are different.

Change the last paragraph as shown:

The fields A[24:~~69~~69] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.6.10 Transmit Switch function

Change 73.6.10 as shown:

~~The Transmit Switch function shall enable the transmit path from a single technology-dependent PHY to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.~~

~~During Auto-Negotiation, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit State Diagram to the MDI.~~

During Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit State Diagram to the MDI.

Upon entry into the AN_GOOD_CHECK state, the Transmit Switch function shall connect the transmit path from a single technology-dependent (highest common denominator) PHY to the MDI.

When a PHY is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

73.7 Receive function requirements

Change the last sentence as shown:

The receive function incorporates a receive switch to control connection to the 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR 40GBASE-KR4, 40GBASE-CR4,~~ or~~ 100GBASE-CR10, 100GBASE-KR4, 100GBASE-KP4, or 100GBASE-CR4 PHYs.

73.7.1 DME page reception

Change the first sentence as shown:

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY (1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4~~, or~~ 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, or 100GBASE-CR4). The DME transmit signal level and receive sensitivity are specified in 73.5.1.

73.7.2 Receive Switch function

Change 73.7.2 as shown:

~~The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PHY once a highest common denominator choice has been made and Auto-Negotiation has completed.~~

~~During Auto-Negotiation, the Receive Switch function shall connect the DME page receiver controlled by the Receive state diagram to the MDI and the Receive Switch function shall also connect the 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PMA receivers to the MDI if the PMAs are present.~~

During Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state, the Receive Switch function shall connect the DME page receiver to the MDI. For the Parallel Detection function, the Receive Switch function shall also connect the receive path of the 1000BASE-KX and 10GBASE-KX4 PHY to the MDI when those PHYs are present.

Upon entry into the AN_GOOD_CHECK state, the Receive Switch function shall connect the receive path from a single technology-dependent (highest comment denominator) PHY to the MDI.

73.7.6 Priority Resolution function

Change Table 73–5 as shown:

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	100GBASE-CR4	100 Gb/s 4 lane, highest priority
2	100GBASE-KR4	100 Gb/s 4 lane
3	100GBASE-KP4	100 Gb/s 4 lane
~~1~~4	100GBASE-CR10	100 Gb/s 10 lane~~, highest priority~~
~~2~~5	40GBASE-CR4	40 Gb/s 4 lane
~~3~~6	40GBASE-KR4	40 Gb/s 4 lane
~~4~~7	10GBASE-KR	10 Gb/s 1 lane
~~5~~8	10GBASE-KX4	10 Gb/s 4 lane
~~6~~9	1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10.7 State diagram variables

Insert new values for the variable "x" as shown:

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all; represents all specific technology-dependent PMAs supported in the local device.
1GKX; represents that the 1000BASE-KX PMA is the signal source.
10GKR; represents that the 10GBASE-KR PMA is the signal source.
10GKX4; represents that the 10GBASE-KX4 or 10GBASE-CX4 PMA is the signal source.
40GKR4; represents that the 40GBASE-KR4 PMD is the signal source.
40GCR4; represents that the 40GBASE-CR4 PMD is the signal source.
100GCR10; represents that the 100GBASE-CR10 PMD is the signal source.
100GKP4; represents that the 100GBASE-KP4 PMD is the signal source.
100GKR4; represents that the 100GBASE-KR4 PMD is the signal source.
100GCR4; represents that the 100GBASE-CR4 PMD is the signal source.

HCD; represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.

notHCD; represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.

PD; represents all of the following that are present: 1000BASE-KX PMA, 10GBASE-KX4 PMA or 10GBASE-CX4 PMA, 10GBASE-KR PMA, 40GBASE-KR4 PMD, 40GBASE-CR4 PMD, and 100GBASE-CR10 PMD.

Change the definition of the variable single_link_ready as shown:

single_link_ready

Status indicating that an_receive_idle = true and only one the of the following indications is being received:

1) link_status_[1GKX] = OK
2) link_status_[10GKX4] = OK
3) link_status_[10GKR] = OK
4) link_status_[40GKR4] = OK
5) link_status_[40GCR4] = OK
6) link_status_[100GCR10] = OK
<u>7) link_status_[100GKP4] = OK</u>
<u>8) link_status_[100GKR4] = OK</u>
<u>9) link_status_[100GCR4] = OK</u>

Values: false; either zero or more than one of the above indications are true or an_receive_idle = false.
true; Exactly one of the above indications is true and an_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for backplane and copper cable assembly[2]

73.11.4.3 Link codeword encoding

Insert item LE8a after item LE8 and change LE14, LE15, and LE17 as shown:

Item	Feature	Subclause	Value/Comment	Status	Support
LE8a	Technology ability reserved fields	73.6.4	Sent as zero and ignored by the receiver	M	Yes [ ]
LE14	Transmit switch function ~~after Auto-Negotiation~~upon entry into the AN_GOOD_CHECK state	73.6.10	~~Enable transmit path upon completion of Auto-Negotiation~~ Connect the transmit path of HCD PHY to the MDI	M	Yes [ ]
LE15	Transmit switch function during Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state	73.6.10	Connect only DME page generator to MDI	M	Yes [ ]
LE17	Incompatible abilities	73.6.4	~~40GBASE-CR4 and 40GBASE-KR4 shall not be advertised simultaneously~~ PHYs for operation over electrical backplane are not simultaneously advertised with PHYs for operation over copper cable	M	Yes [ ]

73.11.4.4 Receive function requirements

Change RF1 through RF3 as shown:

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Receive switch function ~~after Auto-Negotiation~~upon entry into the AN_GOOD_CHECK state	73.7.2	~~Enable receive path at completion of Auto-Negotiation~~ Connect the receive path of HCD PHY to the MDI	M	Yes [ ]
RF2	Receive switch function during Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state	73.7.2	Connect DME page receiver to MDI	M	Yes [ ]
RF3	Receive switch function during Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state	73.7.2	Connect ~~present PMA receivers to MDI~~receive path of the 1000BASE-KX and 10GBASE-KX4 PHY when present.	M	Yes [ ]

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

74. Forward Error Correction (FEC) sublayer for BASE-R PHYs

Change the first paragraph of 74.7.4.8 as follows:

74.7.4.8 FEC rapid block synchronization for EEE (optional)

If the optional EEE capability is supported then during the wake and refresh states the FEC decoder will be receiving one of the two types of deterministic blocks to achieve rapid block synchronization. During these states the reverse gearbox of the remote FEC encoder will be receiving unscrambled data from the PCS sublayer via 16-bit FEC_UNITDATA.request primitive. A Clause 49 PCS sublayer ~~will be encoding~~ encodes /I/ during the wake state and /LI/ during the refresh state, which produces the two types of deterministic FEC blocks. A Clause 82 PCS sublayer also encodes /I/ during the wake state and /LI/ during the refresh state, but in addition inserts Rapid Alignment Markers into each of the PCS Lanes (see 82.2.8a). This causes the two types of deterministic FEC blocks to have a number of 65-bit words within the deterministic FEC block replaced with Rapid Alignment Markers thus not matching the two deterministic patterns as shown in Tables 74A-5 and 74A-6. The locations of the Rapid Alignment Markers, though consistent for each Rapid FEC block for each entry into the wake or refresh states, can be different for a different entry. This modification to the two deterministic patterns needs to be taken into account by the Rapid FEC Lock implementation

78. Energy-Efficient Ethernet (EEE)

Change 78.1 to add 100 Gb/s Ethernet:

78.1 Overview

The optional EEE capability combines the IEEE 802.3 Media Access Control (MAC) Sublayer with a family of Physical Layers defined to support operation in the Low Power Idle (LPI) mode. When the LPI mode is enabled, systems on both sides of the link can save power during periods of low link utilization.

EEE also provides a protocol to coordinate transitions to or from a lower level of power consumption and does this without changing the link status and without dropping or corrupting frames. The transition time in to and out of the lower level of power consumption is kept small enough to be transparent to upper layer protocols and applications.

Table 78–1 specifies clauses for EEE operation over twisted-pair cabling systems, twinax cable, and electrical backplanes; for XGMII extension using the XGXS for 10 Gb/s PHYs; and for inter sublayer service interfaces using the XLAUI for 40 Gb/s PHYs and CAUI for 100 Gb/s PHYs.

~~For operation over twisted-pair cabling systems, EEE supports the 100BASE-TX PHY, the 1000BASE-T PHY, and the 10GBASE-T PHY. For operation over electrical backplanes, EEE supports the 1000BASE-KX PHY, the 10GBASE-KX4 PHY, and the 10GBASE-KR PHY. EEE also supports XGMII extension using the XGXS for 10 Gb/s PHYs.~~

In addition to the above, EEE defines a 10 Mb/s MAU (10BASE-Te) with reduced transmit amplitude requirements. The 10BASE-Te MAU is fully interoperable with 10BASE-T MAUs over 100 m of class D (Category 5) or better cabling as specified in ISO/IEC 11801:1995. These requirements can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-B-1995. The definition of 10BASE-Te allows a reduction in power consumption.

EEE also specifies means to exchange capabilities between link partners to determine whether EEE is supported and to select the best set of parameters common to both devices. Clause 78 provides an overview of EEE operation. PICS for the optional EEE capability for each specific PHY type are specified in the respective PHY clauses. Normative requirements for Data Link Layer capabilities are contained in 78.4.

Editors' Note (to be removed prior to publication):

The PHY list in 78.1.3.3.1 is not changed as this is presented with "e.g." and does not need to be definitive.

78.1.3 Reconciliation sublayer operation

78.1.3.3 PHY LPI operation

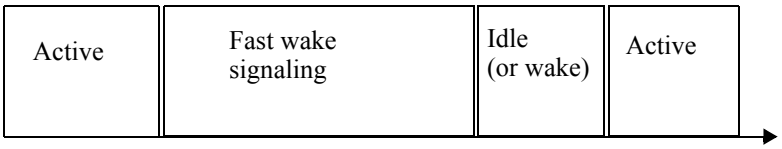
78.1.3.3.1 PHY LPI transmit operation

Insert the following text and figure at the end of 78.1.3.3.1

For PHYs with an operating speed of 40 Gb/s or 100 Gb/s that implement the optional EEE capability, two modes of LPI operation may be supported. Deep sleep refers to the mode for which the transmitter ceases transmission during the quiet state (as shown in Figure 78–3); Fast wake refers to the mode for which the transmitter continues to transmit signals during the fast wake state so that the receiver can resume operation with a shorter wake time (as shown in Figure 78–3a). Only deep sleep is defined for PHYs with an operating

speed less than 40 Gb/s. Fast wake is mandatory for 40 Gb/s and 100 Gb/s PHYs that implement EEE; deep sleep is an additional option for those PHYs.

Physical layer signaling continues with higher layer functions suspended during fast wake signaling



Note: Fast wake signaling continually indicates LPI in a normally constituted data stream.

Figure 78–3a—Overview of Fast Wake operation

WARNING

The signaling in deep sleep operation precludes transparent mapping of the link over Optical Transport Networks. Only fast wake operation should be enabled for any link that is intended for transparent OTN mapping.

Change the title of subclause 78.1.4

78.1.4 PHY types which may support EEE ~~Supported PHY types~~

Change the table title and body as shown in Table 78–1 for 40 Gb/s and 100 Gb/s Ethernet:

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
10BASE-Te	14
100BASE-TX	24, 25
1000BASE-T	40
XGXS (XAUI)	47, 48
1000BASE-KX	70, ~~35~~36

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
10GBASE-T	55
10GBASE-KX4	71, 48
10GBASE-KR	72, 51, 49, 74
40GBASE-CR4	82, 83, 85, 74
40GBASE-KR4	82, 83, 84, 74
100GBASE-CR10	82, 83, 85, 74
100GBASE-KP4	82, 91, 94
100GBASE-KR4	82, 83, 91, 93
100GBASE-CR4	82, 83, 91, 92
XLAUI/CAUI	83A

78.2 LPI mode timing parameters description

Change table title and column heading and insert rows at the bottom of Table 78–2:

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

~~Protocol~~ PHY or interface type	T_s (μs)		T_q (μs)		T_r (μs)	
	Min	Max	Min	Max	Min	Max
40GBASE-CR4	0.9	1.1	1 700	1 800	5.9	6.5
40GBASE-KR4	0.9	1.1	1 700	1 800	5.9	6.5
100GBASE-CR10	0.9	1.1	1 700	1 800	5.9	6.5
100GBASE-CR4	0.9	1.1	1 700	1 800	5.9	6.5
100GBASE-KR4	0.9	1.1	1 700	1 800	5.9	6.5
100GBASE-KP4	0.9	1.1	1 700	1 800	5.9	6.5
XLAUI/CAUI	0.9	1.1	1 700	1 800	5.9	6.5

Change the first 2 paragraphs of 78.3 as shown:

78.3 Capabilities Negotiation

~~The EEE capability shall be advertised during the Auto-Negotiation stage~~ PHYs capable of deep sleep operation shall advertise that capability during the Auto-Negotiation stage. Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is

performed at power up, on command from management, due to link failure, or due to user intervention. Fast wake capability may also be advertised using L2 protocol frames.

During Auto-Negotiation, both link partners indicate their EEE capabilities. EEE is supported only if during Auto-Negotiation both the local device and link partner advertise the EEE capability for the resolved PHY type. If EEE is not supported, all EEE functionality is disabled and the LPI client does not assert LPI. EEE deep sleep operation shall not be enabled unless both the local device and link partner advertise deep sleep capability during Auto-Negotiation for the resolved PHY type. If EEE is supported by both link partners for the negotiated PHY type, then the EEE function can be used independently in either direction.

Change the second and third paragraphs of 78.4 as shown:

78.4 Data Link Layer Capabilities

The Data Link Layer capabilities shall be implemented for devices with an operating speed equal to or greater than 10 Gb/s and may be implemented for all other devices. The use of the EEE fast wake TLV shall be interpreted as an indication that the device supports EEE fast wake operation, regardless of the capability advertised during the Auto-Negotiation stage. A device shall not indicate deep sleep capability using the EEE fast wake TLV unless both the local device and link partner advertise deep sleep capability during Auto-Negotiation for the resolved PHY type.

Implementations that use the Data Link Layer capabilities shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the EEE Type, Length, Value (TLV) defined in 79.3.5; timing requirement in 78.4.1; and shall support the control state diagrams defined in 78.4.2. Devices with an operating speed equal to or greater than 40 Gb/s shall support EEE fast wake TLV as defined in 79.3.6.

78.4 Data Link Layer Capabilities

78.4.2 Control state diagrams

78.4.2.3 Variables

Insert the following variable definitions into 78.4.2.3 preserving alphabetical order

LocTxSystemFW
: Boolean variable that indicates the state of FW_enable that the local transmit system can support. This value is updated by the EEE DLL Fast Wake Tx state diagram. This variable maps into the aLldpXdot3LocTxFw attribute.

RemTxSystemFWEcho
: Boolean variable that indicates the state of transmit FW_enable echoed back by the remote system. This value maps from the aLldpXdot3RemTxFwEcho attribute.

LocRxSystemFW
: Boolean variable that indicates the state of FW_enable that the local receive system requests from the remote system. This value is updated by the EEE DLL Fast Wake Rx state diagram. This variable maps into the aLldpXdot3LocRxFw attribute.

RemRxSystemFWEcho
: Boolean variable that indicates the state of receive FW_enable echoed back by the remote system. This value maps from the aLldpXdot3RemRxFwEcho attribute.

RemTxSystemFW
: Boolean variable that indicates the FW_enable that the remote transmit system requests from the local system. This value maps from the aLldpXdot3RemTxFw attribute.

LocTxSystemFWEcho
: Boolean variable that indicates the remote system's transmit FW_enable that was used by the local system to decide the FW_enable that it wants to request from the remote system. This value maps into the aLldpXdot3LocTxFwEcho attribute.

RemRxSystemFW
: Boolean variable that indicates the FW_enable that the remote receive system requests from the local system. This value maps from the aLldpXdot3RemRxFw attribute.

LocRxSystemFWEcho
: Boolean variable that indicates the remote system's receive FW_enable that was used by the local system to decide the FW_enable that it can support. This value maps into the aLldpXdot3LocRxFwEcho attribute.

LocResolvedTxSystemFW
: Boolean that indicates the current FW_enable supported by the local system.

LocResolvedRxSystemFW
: Boolean that indicates the current FW_enable supported by the remote system.

TempTxFW
: Boolean used to store the value of FW_enable.

TempRxFW
Boolean used to store the value of FW_enable.

local_system_FW_change
An implementation specific control variable that indicates that the local system wants to change either the Transmit FW_enable or the Receive FW_enable.

NEW_TX_FW
Boolean that indicates the value of transmit FW_enable that the local system can support.

NEW_RX_FW
Boolean that indicates the value of receive FW_enable that the local system wants the remote system to support.

Insert the following rows into Table 78-3 as shown:

Table 78–3—Attribute to state diagram variable cross-reference

Entity	Object class	Attribute	Mapping	State diagram variable
TX	oLldpXdot3LocSystemsGroup	aLldpXdot3LocTxTwSys	⇐	LocTxSystemValue
		aLldpXdot3LocRxTwSysEcho	⇐	LocRxSystemValueEcho
		aLldpXdot3LocDllEnabled	⇒	tx_dll_enabled
		aLldpXdot3LocTxDllReady	⇐	tx_dll_ready
		aLldpXdot3LocTxFw	⇐	LocTxSystemFW
		aLldpXdot3LocRxFwEcho	⇐	LocRxSystemFWEcho
	oLldpXdot3RemSystemsGroup	aLldpXdot3RemRxTwSys	⇒	RemRxSystemValue
		aLldpXdot3RemTxTwSysEcho	⇒	RemTxSystemValueEcho
		aLldpXdot3RemRxFw	⇒	RemRxSystemFW
		aLldpXdot3RemTxFwEcho	⇒	RemTxSystemFWEcho
RX	oLldpXdot3LocSystemsGroup	aLldpXdot3LocRxTwSys	⇐	LocRxSystemValue
		aLldpXdot3LocTxTwSysEcho	⇐	LocTxSystemValueEcho
		aLldpXdot3LocFbTwSys	⇐	LocFbSystemValue
		aLldpXdot3LocDllEnabled	⇒	rx_dll_enabled
		aLldpXdot3LocRxDllReady	⇐	rx_dll_ready
		aLldpXdot3LocRxFw	⇐	LocRxSystemFW
		aLldpXdot3LocTxFwEcho	⇐	LocTxSystemFWEcho
	oLldpXdot3RemSystemsGroup	aLldpXdot3RemTxTwSys	⇒	RemTxSystemValue
		aLldpXdot3RemRxTwSysEcho	⇐	RemRxSystemValueEcho
		aLldpXdot3RemTxFw	⇒	RemTxSystemFW
		aLldpXdot3RemRxFwEcho	⇐	RemRxSystemFWEcho

78.4.2.4 Functions

Insert the following functions into 78.4.2.4 preserving alphabetical order

examine_TxFW_change

This function decides if the new value of FW_enable is acceptable by the local transmit system when there is an updated request from the remote system or if local system conditions require a change in the value of the presently supported FW_enable.

examine_RxFW_change

This function decides if the new value of FW_enable is acceptable by the local receive system when there is an updated request from the remote system or if local system conditions require a change in the value of the presently supported FW_enable.

78.4.2.5 State diagrams

Insert the following text and state diagrams at the end of 78.4.2.5

The general state change procedure for transmitter Fast Wake is shown in Figure 78–7.

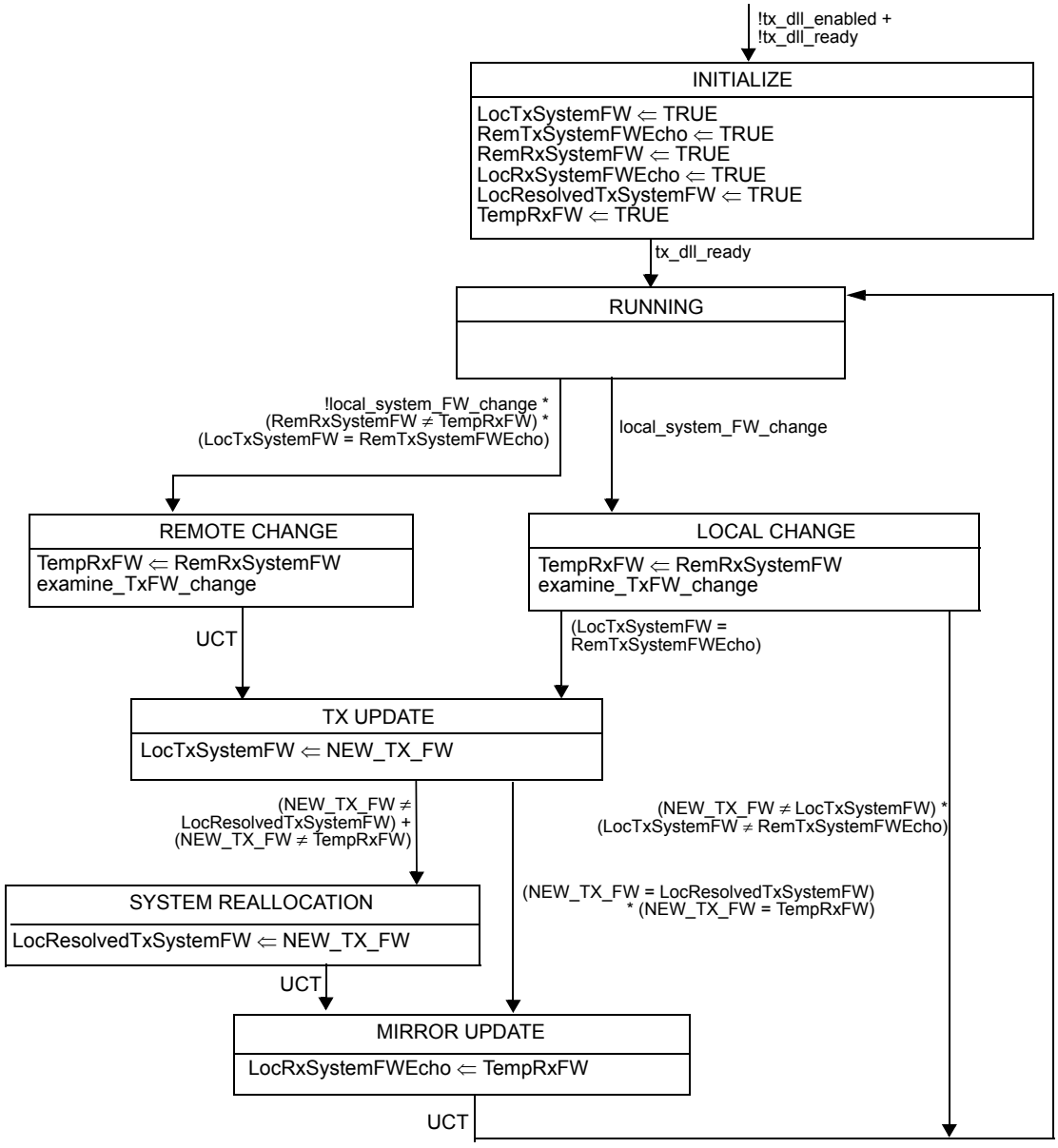


Figure 78–7—EEE DLL Transmitter Fast Wake State Diagram

The general state change procedure for receiver is shown in Figure 78–8.

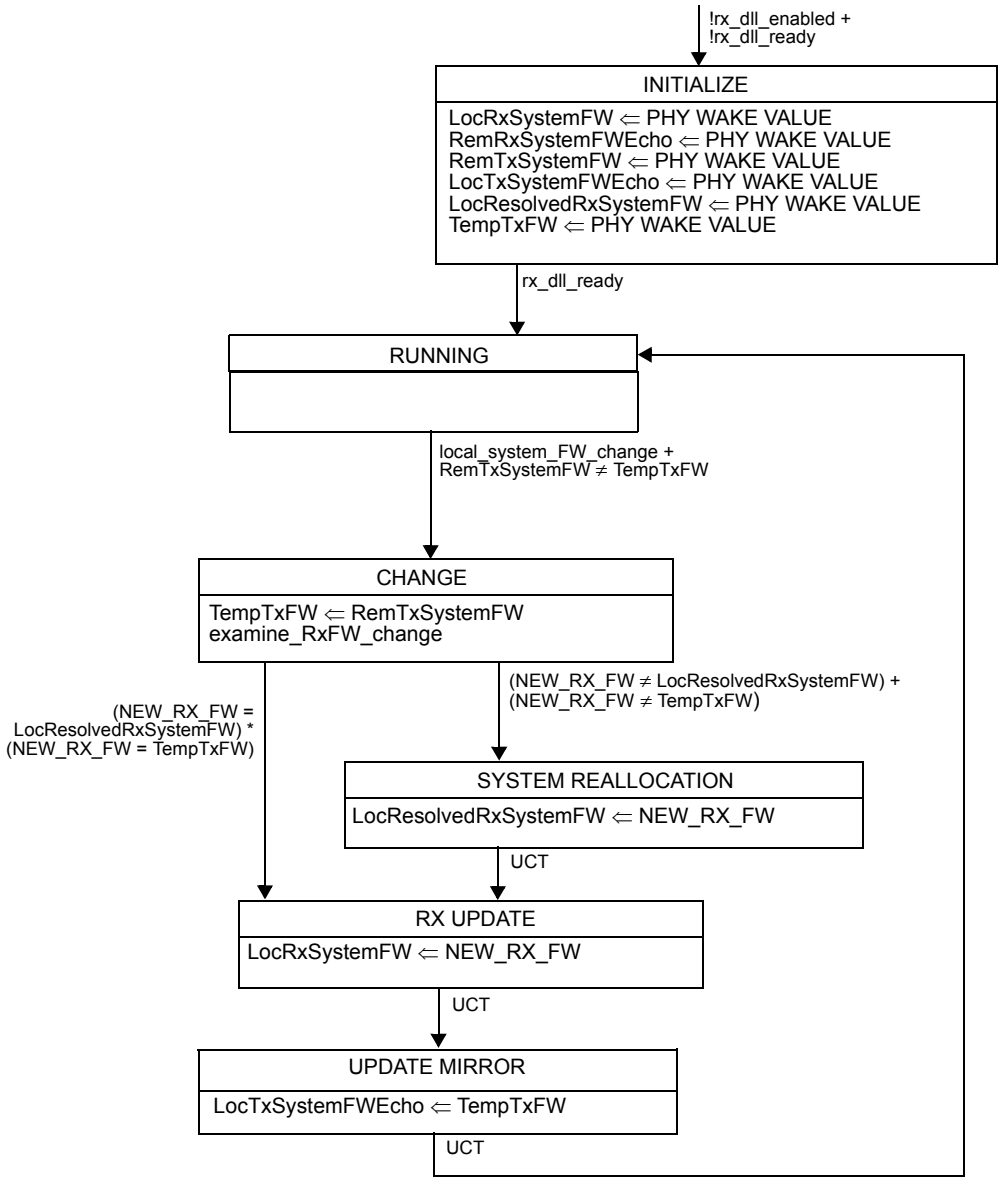


Figure 78–8—EEE DLL Receiver Fast Wake State Diagram

78.4.3 State change procedure across a link

Insert the following at the end of 78.4.3

The default state of Fast_Wake_Enable is TRUE for all PHYs that support the function. This provides for EEE operation and functionality on initialization and prior to the exchange and processing of the TLVs.

The receiving link partner may request a change of Fast_Wake_enable through the aLldpXdot3LocRxFW (30.12.2.1.32) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The request appears to the transmitting link partner as a change to the aLldpXdot3RemRxFW (30.12.3.1.26) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The transmitting link partner responds to its receiving partner's request through the aLldpXdot3LocTxFW (30.12.2.1.30) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The transmitting link partner also copies the value of the aLldpXdot3RemRxFW (30.12.3.1.26) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocRxFWEcho (30.12.2.1.33) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2).

The transmitting link partner may advertise a change of Fast_Wake_Enable through the aLldpXdot3LocTxFW (30.12.3.1.24) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the receiving link partner as a change to the aLldpXdot3RemTxFW (30.12.3.1.24) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The receiving link partner responds to a transmitter's request through the aLldpXdot3LocRxFW (30.12.2.1.32) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The receiving link partner also copies the value of the aLldpXdot3RemTxFW (30.12.3.1.24) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocTxFWEcho (30.12.2.1.31) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the transmitting link partner as a change to the aLldpXdot3RemTxFWEcho (30.12.3.1.25) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3).

The state diagrams in Figure 78–7 and Figure 78–8 describe the behavior above.

78.4.3.1 Transmitting link partner’s state change procedure across a link

Insert the following at the end of 78.4.3.1

A transmitting link partner is said to be in sync with the receiving link partner if the presently advertised value of Transmit Fast_Wake_Enable and the corresponding echoed value are equal.

During normal operation, the transmitting link partner is in the RUNNING state. If the transmitting link partner wants to initiate a change to the presently resolved value of Fast_Wake_Enable, the local_system_change is asserted and the transmitting link partner enters the LOCAL CHANGE state where NEW_TX_FW is computed. If the transmitting link partner is in sync with the receiving link partner, then it enters TX UPDATE state. Otherwise, it returns to the RUNNING state.

If the transmitting link partner sees a change in the Fast_Wake_Enable requested by the receiving link partner, it recognizes the request only if it is in sync with the transmitting link partner. The transmitting link partner examines the request by entering the REMOTE CHANGE state where a NEW_TX_FW is computed and it then enters the TX UPDATE state.

Upon entering the TX UPDATE state, the transmitter updates the advertised value of Transmit Fast_Wake_Enable with NEW_TX_FW. If the NEW_TX_FW is different to either the resolved Fast_Wake_Enable value or the value requested by the receiving link partner then it enters the SYSTEM REALLOCATION state where it updates the value of resolved Fast_Wake_Enable with NEW_TX_FW. The transmitting link partner enters the MIRROR UPDATE state either from the SYSTEM REALLOCATION

state or directly from the TX UPDATE state. The UPDATE MIRROR state then updates the echo for the Receive Fast_Wake_Enable and returns to the RUNNING state.

78.4.3.2 Receiving link partner's state change procedure across a link

Insert the following at the end of 78.4.3.2

A receiving link partner is said to be in sync with the transmitting link partner if the presently requested value of Receive Fast_Wake_Enable and the corresponding echoed value are equal.

During normal operation, the receiving link partner is in the RUNNING state. If the receiving link partner wants to request a change to the presently resolved value of Fast_Wake_Enable, the local_system_change is asserted. When local_system_change is asserted or when the receiving link partner sees a change in the Fast_Wake_Enable advertised by the transmitting link partner, it enters the CHANGE state where NEW_RX_FW is computed. If NEW_RX_FW is different to either the presently resolved value of Fast_Wake_Enable or the presently advertised value by the transmitting link partner, it enters the SYSTEM REALLOCATION state where it updates the resolved value of Fast_Wake_Enable to NEW_RX_FW. The receiving link partner ultimately enters the RX UPDATE state, either from the SYSTEM REALLOCATION state or directly from the CHANGE state.

In the RX UPDATE state, it updates the presently requested value to NEW_RX_FW, then it updates the echo for the Transmit Fast_Wake_Enable in the UPDATE MIRROR state and finally goes back to the RUNNING state.

78.5 Communication link access latency

Change table title and column heading and insert rows at the bottom of Table 78-4, insert text immediately before the table as follows:

Case-1 of the 40GBASE-CR4, 40GBASE-KR4, and 100GBASE-CR10 PHYs applies to PHYs without FEC in deep sleep. Case-2 of these PHYs applies to PHYs with FEC in deep sleep. Case-3 of these PHYs applies to PHYs in fast wake.

Case-1 of the 100GBASE-CR4, 100GBASE-KR4, and 100GBASE-KP4 PHYs applies to PHYs in deep sleep. Case-2 of these PHYs applies to PHYs in fast wake.

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
40GBASE-CR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2
	Case-3	0.34	0.3	0	0	0.25
40GBASE-KR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2
	Case-3	0.34	0.3	0	0	0.25
100GBASE-CR10	Case-1	5.5	5.5	2	3	1
	Case-2	7.5	7.5	2	3	1
	Case-3	0.34	0.3	0	0	0.25
100GBASE-CR4	Case-1	5.5	5.5	2	3	1
	Case-2	0.34	0.3	0	0	0.25
100GBASE-KR4	Case-1	5.5	5.5	2	3	1
	Case-2	0.34	0.3	0	0	0.25
100GBASE-KP4	Case-1	5.5	5.5	2	3	1
	Case-2	0.34	0.3	0	0	0.25
XLAUI/CAUI		5.5	5.5	2	3	1

Insert 78.5.2 after 78.5.1 for PHY extension:

78.5.2 40 Gb/s and 100 Gb/s PHY extension using XLAUI or CAUI

40 Gb/s and 100 Gb/s PHYs may be extended using XLAUI and CAUI as a physical instantiation of the inter-sublayer service interface to separate functions between devices. The LPI signaling can operate across XLAUI/CAUI with no change to the PHY timing parameters described in Table 78–4 or the operation of the Data Link Layer Capabilities negotiation described in 78.4.

If PMA Egress AUI Stop Enable (PEASE, see 83.3; MDIO register bit 1.7.8) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI/CAUI in the transmit direction to conserve energy. If PEASE is asserted, the RS defers sending data following deassertion of LPI by an additional time equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ as shown in Table 78–4 for each PMA with PEASE asserted (see 81.3a.2.1).

If PMA Ingress AUI Stop Enable (PIASE, see 83.3; MDIO register bit 1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI/CAUI in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} (equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI/CAUI as shown in Table 78–4) for each PMA with PIASE to be asserted before setting the PIASE bits.

78.6 Protocol implementation conformance statement (PICS) proforma for EEE Data Link Layer Capabilities[3]

Editor's Note (to be removed prior to publication):

No changes to the PICS are required for 100 Gb/s Ethernet.

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements

79.3 IEEE 802.3 Organizationally Specific TLVs

Change the reserved row of Table 79-1 and insert a new row above it as shown:

Table 79–1—IEEE 802.3 Organizationally Specific TLVs

IEEE 802.3 subtype	TLV name	Subclause reference
6	EEE Fast Wake	79.3.6
~~6~~7–255	Reserved	—

Insert the following subclause after 79.3.5

79.3.6 EEE Fast Wake TLV

The EEE Fast Wake TLV is used to exchange information about the EEE Fast Wake capabilities. This TLV is only used by systems operating at links speeds >10 Gb/s. Figure 79–7 shows the format of this TLV.

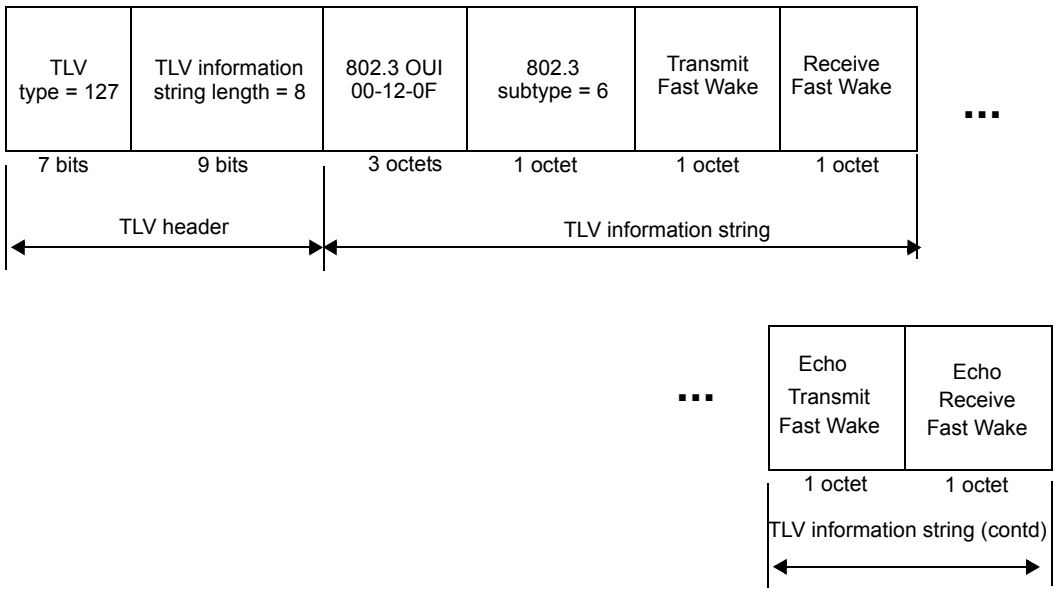


Figure 79–7—EEE Fast Wake TLV format

79.3.6.1 Transmit Fast Wake

Transmit Fast Wake (1 octet wide) is a logical indication that the transmit LPI state diagram intends to use the Fast Wake function (corresponding to the variable LPI_FW in 82.2.18.2.2). Transmit Fast Wake = 1 corresponds to LPI_FW being TRUE; Transmit Fast Wake = 0 corresponds to LPI_FW being FALSE. The default value for Transmit Fast Wake is 1 (TRUE). Transmit Fast Wake is set to TRUE unless the PHY is capable of deep sleep operation as determined by the PHY type and the results of auto-negotiation.

79.3.6.2 Receive Fast Wake

Receive Fast Wake (1 octet wide) is a logical indication that the receive LPI state diagram is expecting its link partner to use the Fast Wake function (corresponding to the variable LPI_FW in 82.2.18.2.2). Receive Fast Wake = 1 corresponds to LPI_FW being TRUE; Receive Fast Wake = 0 corresponds to LPI_FW being FALSE. The default value for Receive Fast Wake is 1 (TRUE). Receive Fast Wake is set to TRUE unless the PHY is capable of deep sleep operation as determined by the PHY type and the results of auto-negotiation.

79.3.6.3 Echo of Transmit Fast Wake and Receive Fast Wake

The respective echo values are the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner, it can determine whether or not the remote link partner has received, registered and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

79.4 IEEE 802.3 Organizationally Specific TLV selection management

79.4.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

Change the second paragraph of 79.4.2 and insert rows following the last rows of Table 79–9 and Table 79–10 as shown:

The cross-references between the EEE TLV, the EEE Fast Wake TLV, and the EEE local (30.12.2) and remote (30.12.3) object class attributes are listed in Table 79–9 and Table 79–10.

Table 79–9—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references

TLV name	TLV variable	LLDP Local System Group managed object class attribute
EEE Fast Wake	Transmit Fast Wake	aLldpXdot3LocTxFw
	Receive Fast Wake	aLldpXdot3LocRxFw
	Echo Transmit Fast Wake	aLldpXdot3LocTxFwEcho
	Echo Receive Fast Wake	aLldpXdot3LocRxFwEcho

Table 79–10—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
EEE Fast Wake	Transmit Fast Wake	aLldpXdot3RemTxFw
	Receive Fast Wake	aLldpXdot3RemRxFw
	Echo Transmit Fast Wake	aLldpXdot3RemTxFwEcho
	Echo Receive Fast Wake	aLldpXdot3RemRxFwEcho

79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and values (TLV) information elements[4]

79.5.3Major capabilities/options

Insert the following row after the last row of the major capabilities table in 79.5.3 as shown:

Item	Feature	Subclause	Value/Comment	Status	Support
*EEFW	EEE Fast Wake TLV	79.5.6a		O	Yes [ ] No [ ]

Insert the following subclause after 79.5.6:

79.5.6a EEE TLV

Item	Feature	Subclause	Value/Comment	Status	Support
EFW1	Transmit Fast Wake field	79.3.6.1	1 octet representing fast wake option for transmit LPI function	EEFW: M	Yes [ ] N/A [ ]
EFW2	Receive Fast Wake field	79.3.6.2	1 octet representing fast wake option for receive LPI function	EEFW: M	Yes [ ] N/A [ ]
EFW3	Echo Transmit and Receive Fast Wake fields	79.3.6.3	2 octets representing received Fast Wake options	EEFW: M	Yes [ ] N/A [ ]
EFW4	Usage rules		LLDPDU contains no more than one EEE Fast Wake TLV	EEFW: O	Yes [ ] No [ ] N/A [ ]

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

80. Introduction to 40 Gb/s and 100 Gb/s networks

Change the first paragraph of subclause 80.1.1 as shown.

80.1.1 Scope

~~40 Gigabit and 100 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a Media Independent Interface to 40 Gb/s and 100 Gb/s Physical Layer entities such as those specified in Table 80–1~~

This clause describes the general requirements for 40 Gigabit and 100 Gigabit Ethernet. 40 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 40 Gb/s, coupled with any IEEE 802.3 40GBASE Physical Layer implementation. 100 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 100 Gb/s, coupled with any IEEE 802.3 100GBASE Physical Layer implementation. 40 Gb/s and 100 Gb/s Physical Layer entities such as those specified in Table 80–1, provide a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface. 40 Gigabit and 100 Gigabit Ethernet is defined for full duplex operation only.

Editor's note (to be removed prior to final publication):

The above text merges the responses to (required) comments #15 and #174 from draft 2.0. The responses to these comments were contradictory and could not be simultaneously implemented.

Delete subclause 80.1.2 as shown.

~~**80.1.2 Objectives**~~

~~The following are the objectives of 40 Gigabit and 100 Gigabit Ethernet:~~

- ~~a) Support the full duplex Ethernet MAC.~~
- ~~b) Preserve the IEEE 802.3 Ethernet frame format utilizing the IEEE 802.3 MAC.~~
- ~~c) Preserve minimum and maximum frame size of IEEE Std 802.3.~~
- ~~d) Support a BER better than or equal to 10^{-12} at the MAC/PLS service interface.~~
- ~~e) Provide appropriate support for Optical Transport Network (OTN).~~
- ~~f) Support a MAC data rate of 40 Gb/s.~~
- ~~g) Provide Physical Layer specifications that support 40 Gb/s operation over up to the following:~~
  - ~~1) At least 10 km on single-mode fiber (SMF)~~
  - ~~2) At least 2 km on single-mode fiber (SMF)~~
  - ~~3) At least 100 m on OM3 multimode fiber (MMF)~~
  - ~~4) At least 7 m over a copper cable assembly~~
  - ~~5) At least 1 m over a backplane~~
- ~~h) Support a MAC data rate of 100 Gb/s.~~
- ~~i) Provide Physical Layer specifications that support 100 Gb/s operation over up to the following:~~
  - ~~1) At least 40 km on single-mode fiber (SMF)~~
  - ~~2) At least 10 km on single-mode fiber (SMF)~~
  - ~~3) At least 100 m on OM3 multimode fiber (MMF)~~
  - ~~4) At least 7 m over a copper cable assembly~~

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

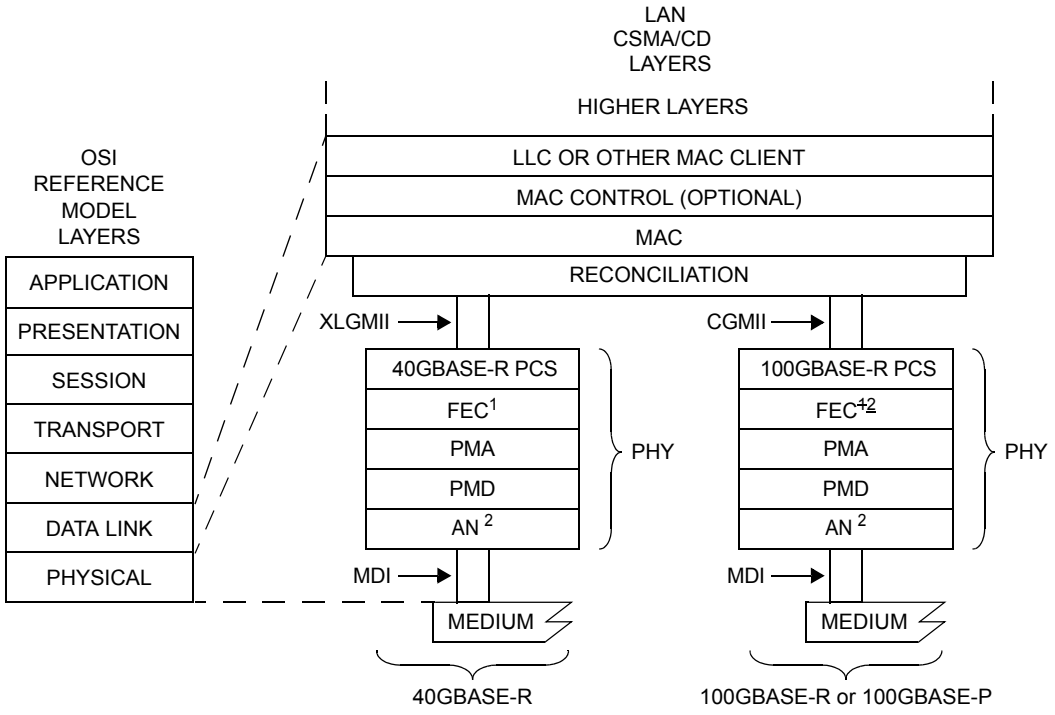
Change item h) as shown.

h) The MDIs as specified ~~in Clause 84 for 40GBASE-KR4,~~ in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, in Clause 87 for 40GBASE-LR4, ~~and~~ in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4, and in Clause 92 for 100GBASE-CR4 all use a 4 lane data path.

Insert item j) as shown.

j) Although there is no electrical or mechanical specification of the MDI for backplane Physical Layers, the PMDs as specified in Clause 84 for 40GBASE-KR4, in Clause 93 for 100GBASE-KR4 and in Clause 94 for 100GBASE-KP4 all use a 4 lane data path.

Change figure 80-1 as shown.



AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE
NOTE 2—CONDITIONAL BASED ON PHY TYPE

Figure 80–1—Architectural positioning of 40 Gigabit and 100 Gigabit Ethernet

Change 80.1.4 as shown.

80.1.4 Nomenclature

The nomenclature employed by the 40 Gigabit and 100 Gigabit Physical Layers is explained as follows.

The alpha-numeric prefix 40GBASE in the port type (e.g., 40GBASE-R) represents a family of Physical Layer devices operating at a speed of 40 Gb/s. The alpha-numeric prefix 100GBASE in the port type (e.g., 100GBASE-R) represents a family of Physical Layer devices operating at a speed of 100 Gb/s.

40GBASE-R or 100GBASE-R represents a family of Physical Layer devices using the Clause 82 Physical Coding Sublayer ~~a physical coding sublayer~~ for 40 Gb/s or 100 Gb/s operation over multiple PCS lanes (see Clause 82) ~~based on 64B/66B block encoding~~ and a PMD implementing 2-level pulse amplitude modulation (PAM). Some 100GBASE-R Physical Layer devices also use the transcoding and FEC of Clause 91. Some 40GBASE-R and 100GBASE-R physical layer devices also may use FEC of Clause 74.

100GBASE-P represents Physical Layer devices using the Clause 82 Physical Coding Sublayer for 100 Gb/s operation over multiple PCS lanes (see Clause 82) and a PMD implementing more than 2-level pulse amplitude modulation (PAM). Some 100GBASE-P Physical Layer devices also use the transcoding and FEC of Clause 91.

Physical Layer devices listed in Table 80–1 are defined for operation at 40 Gb/s and 100 Gb/s.

Insert the following rows between 40GBASE-LR4 and 100GBASE-CR10 to Table 80-1.

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
100GBASE-KR4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 2-level pulse amplitude modulation over four lanes of an electrical back-plane, with a total insertion loss up to 35 dB at 12.9 GHz (see Clause 93)
100GBASE-KP4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over four lanes of an electrical back-plane, with a total insertion loss up to 33 dB at 7 GHz (see Clause 94)
100GBASE-CR4	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m (see Clause 92)

Change 80.1.5 as follows

80.1.5 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 80–2 and Table 80–2a specify ~~specifies~~ the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures must meet the requirements of the corresponding clauses.

Replace Table 80-2 and insert Table 80-2a as shown

Table 80–2—Nomenclature and clause correlation (40GBASE)

Nomenclature	Clause[a]														
	73	74	78	81		82	83	83A	83B	84	85	86	86A	87	89
	Auto-Negotiation	BASE-R FEC	EEE	RS	XLGMII	40GBASE-R PCS	40GBASE-R PMA	XLAUI	XLAUI	40GBASE-KR4 PMD	40GBASE-CR4 PMD	40GBASE-SR4 PMD	XLPPI	40GBASE-LR4 PMD	40GBASE-FR PMD
40GBASE-KR4	M	O	O	M	O	M	M	O		M					
40GBASE-CR4	M	O	O	M	O	M	M	O			M				
40GBASE-SR4				M	O	M	M	O	O			M	O		
40GBASE-FR				M	O	M	M	O	O						M
40GBASE-LR4				M	O	M	M	O	O				O	M	

[a]O = Optional, M = Mandatory.

Table 80–2a—Nomenclature and clause correlation (100GBASE)

Nomenclature	Clause[a]																	
	73	74	78	81		82	83	83A	83B	85	86	86A	88		91	92	93	94
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI	CAUI	100GBASE-CR10 PMD	100GBASE-SR10 PMD	CPPI	100GBASE-LR4 PMD	100GBASE-ER4 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD
100GBASE-KR4	M		O	M	O	M	M	O							M		M	
100GBASE-KP4	M		O	M	O	M	O	O							M			M
100GBASE-CR4	M		O	M	O	M	M	O							M	M		
100GBASE-CR10	M	O	O	M	O	M	M	O		M								
100GBASE-SR10				M	O	M	M	O	O		M	O						
100GBASE-LR4				M	O	M	M	O	O				M					
100GBASE-ER4				M	O	M	M	O	O					M				

[a]O = Optional, M = Mandatory.

Change 80.2.2 as shown.

80.2.2 Physical Coding Sublayer (PCS)

The terms 40GBASE-R, ~~and~~ 100GBASE-R, and 100GBASE-P refer to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 82 and the PMA specifications defined in Clause 83 or Clause 94. ~~The 40GBASE-R and 100GBASE-R~~ Clause 82 PCSs perform encoding (decoding) of data from (to) the XLGMII/CGMII to 64B/66B code blocks, distribute the data to multiple lanes, and transfer the encoded data to the PMA.

Change 80.2.3 as shown.

80.2.3 Forward Error Correction (FEC) sublayers

~~The~~ A Forward Error Correction sublayer is ~~an optional sublayer for~~ available for all 40GBASE-R and 100GBASE-R copper and backplane PHYs. It is optional for 40GBASE-KR4, 40GBASE-CR4 and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR4, 100GBASE-KR4 and 100GBASE-KP4 PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers~~, is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis~~.

The BASE-R FEC ~~sublayer~~ (see Clause 74) is instantiated for each PCS lane, and operates autonomously on a per PCS lane basis ~~specified in Clause 74~~. The Reed-Solomon FEC (see Clause 91) is instantiated once and requires 20 PCS lanes and 4 PMA lanes for operation.

80.2.4 Physical Medium Attachment (PMA) sublayer

Change the second paragraph of 80.2.4 as shown.

The 40GBASE-R and 100GBASE-R PMAs are specified in Clause 83 and the PMA specific to the 100GBASE-KP4 is specified in Clause 94.

80.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph of 80.2.5 as shown.

The 40GBASE-R, ~~and~~ 100GBASE-R, and 100GBASE-P PMDs and their corresponding media are specified in Clause 84 through Clause 89 and Clause 92 through Clause 94.

80.2.6 Auto-Negotiation

Change the last sentence as shown.

Clause 73 Auto-Negotiation is used by the 40 Gb/s and 100 Gb/s backplane PHYs (40GBASE-KR4, 100GBASE-KP4, and 100GBASE-KR4~~see Clause 84~~) and the 40 Gb/s and 100 Gb/s copper PHYs (40GBASE-CR4, ~~and~~ 100GBASE-CR10, and 100GBASE-CR4~~see Clause 85~~).

Change the first paragraph of 80.3 as shown.

80.3 Service interface specification method and notation

The service interface specification for 40GBASE-R, ~~and~~ 100GBASE-R, and 100GBASE-P Physical Layers is as per the definition in 1.2.2. Note that the 40GBASE-R, ~~and~~ 100GBASE-R, and 100GBASE-P inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the

transfer of multiple independent streams of data units, as explained in 80.3.1 through 80.3.3.

Insert the following at the end of 80.3.1:

80.3.1 Inter-sublayer service interface

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.3) then the inter-sublayer service interface includes four additional primitives defined as follows:

IS_TX_MODE.request
IS_RX_MODE.request
IS_ENERGY_DETECT.indication
IS_RX_LPI_ACTIVE.request

The IS_TX_MODE.request primitive is used to communicate the state of the PCS LPI transmit function to other sublayers in the PHY. The IS_RX_MODE.request primitive is used to communicate the state of the PCS LPI receive function to other sublayers. The IS_RX_LPI_ACTIVE.request primitive is used to communicate to the FEC that the PCS is using its receive LPI function. The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence.

80.3.2 Inter-sublayer service interface

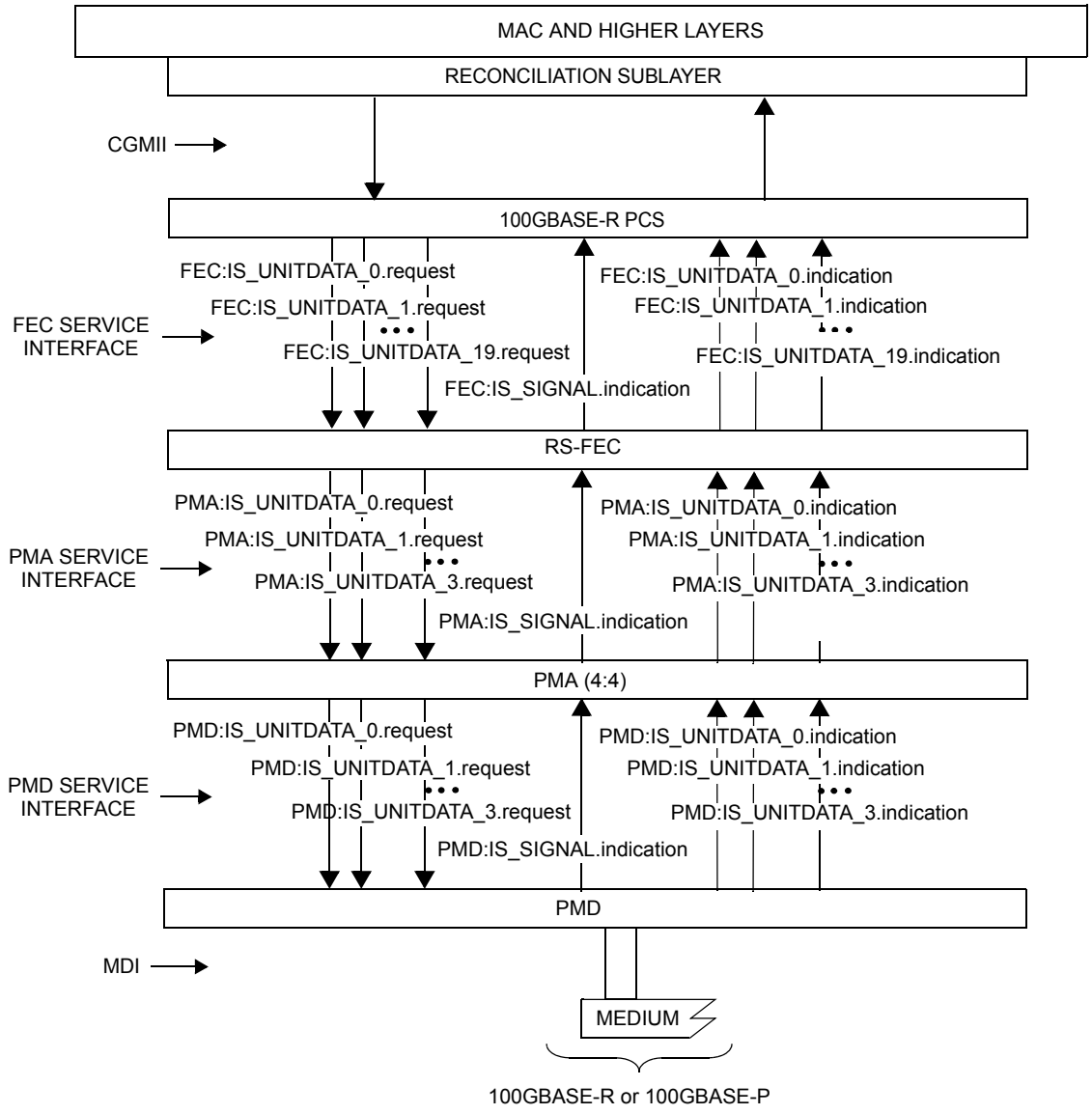
Change the second paragraph of 80.3.2 as shown:

Examples of inter-sublayer service interfaces for 40GBASE-R, ~~and~~ 100GBASE-R, and 100GBASE-P with their corresponding instance names are illustrated in Figure 80–2, ~~and~~ Figure 80–3, Figure 80–3a and Figure 80–3b. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

Editor's note (to be removed prior to final publication):

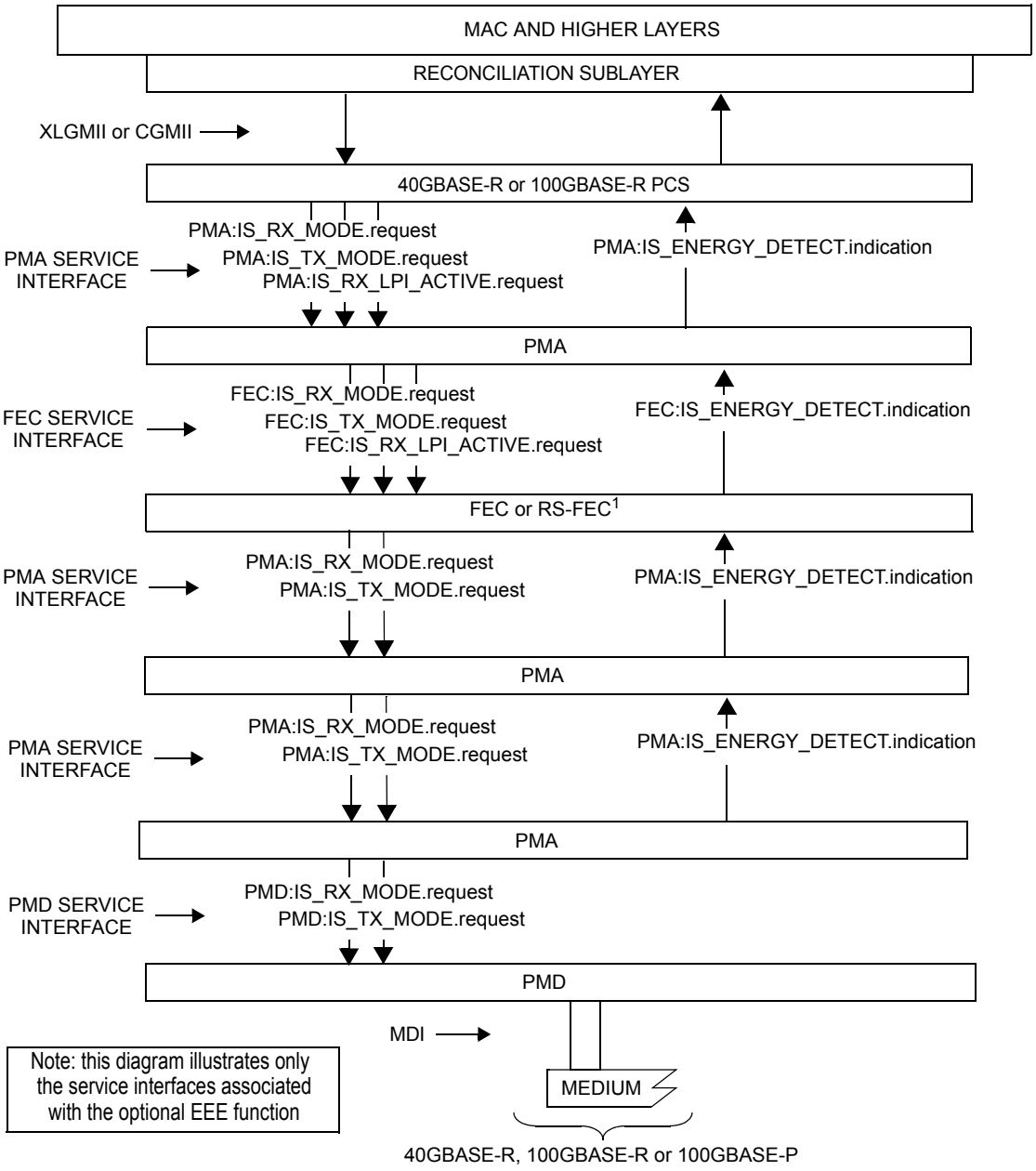
Comments 61, 76, 77, 78, 79, 80, 129, (and indirectly, comment 115) against draft 1.1 require the addition of items to figures 80-2, 80-3 and 80-3a. The editor has split the optional EEE items into a separate figure to preserve readability for these figures.

Insert Figure 80–3a and Figure 80–3b after Figure 80–3:



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 80–3a—100GBASE-R and 100GBASE-P inter-sublayer service interfaces with RS-FEC



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 80–3b—Optional inter-sublayer service interfaces for EEE support

Insert 80.3.3.4 and 80.3.3.5 after 80.3.3.3.3:

80.3.3.4 IS_TX_MODE.request

The IS_TX_MODE.request primitive communicates the tx_mode parameter generated by the PCS Transmit Process for EEE capability to invoke the appropriate PMA, FEC and PMD transmit EEE states. Without EEE deep sleep mode capability, the primitive is never invoked and the sublayers behave as if tx_mode = DATA.

80.3.3.4.1 Semantics of the service primitive

IS_TX_MODE.request(tx_mode)

The tx_mode parameter takes on one of up to six values: DATA, SLEEP, QUIET, FW, ALERT or BYPASS.

80.3.3.4.2 When generated

This primitive is generated to indicate the low power mode of the transmit path.

80.3.3.4.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives this primitive. In general, when tx_mode is DATA the sublayer operates normally and when tx_mode is QUIET, the sublayer may go into a low power mode.

80.3.3.5 IS_RX_MODE.request

The IS_RX_MODE.request primitive communicates the rx_mode parameter generated by the PCS LPI receive function to other sublayers. Without EEE capability (with the deep sleep mode option), the primitive is never invoked and the sublayers behave as if rx_mode = DATA.

80.3.3.5.1 Semantics of the service primitive

IS_RX_MODE.request(rx_mode)

The rx_mode parameter takes on one of two values: DATA or QUIET.

80.3.3.5.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function.

80.3.3.5.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives this primitive. In general, when rx_mode is DATA the sublayer operates normally and when rx_mode is QUIET, the sublayer may go into a low power mode.

80.3.3.6 IS_RX_LPI_ACTIVE.request

The IS_RX_LPI_ACTIVE.request primitive communicates to the FEC that the PCS LPI receive function is active. This primitive may be passed through a PMA sublayer but has no effect on that sublayer. This primitive is only used for a PMA sublayer that is between the PCS and a Clause 74 FEC sublayer, in all other cases the primitive is never invoked and has no effect. Without EEE capability (with the deep sleep mode option), the primitive is never invoked and has no effect.

80.3.3.6.1 Semantics of the service primitive

IS_RX_LPI_ACTIVE.request(rx_lpi_active)

The parameter rx_lpi_active is Boolean.

80.3.3.6.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function.

80.3.3.6.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the FEC sublayer that receives this primitive. In general, when rx_lpi_active is true the FEC sublayer uses rapid block lock to reestablish FEC operation following a period of quiescence.

80.3.3.7 IS_ENERGY_DETECT.indicate

The IS_ENERGY_DETECT.indicate primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence. Without EEE deep sleep mode capability, the primitive is never invoked and has no effect.

80.3.3.7.1 Semantics of the service primitive

IS_ENERGY_DETECT.indicate(energy_detect)

The parameter energy_detect is Boolean.

80.3.3.7.2 When generated

This primitive is generated by the PMA, reflecting the state of the signal_detect parameter received from the PMD.

80.3.3.7.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the PCS sublayer that receives this primitive. This parameter is used to indicate that activity has returned on the interface following a period of quiescence.

80.4 Delay constraints

Insert rows in Table 80-3 as shown (insert 100GBASE-R RS-FEC below 100GBASE-R FEC; insert the other 3 rows below 100GBASE-R PMA):

Table 80–3—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
100GBASE-R RS-FEC	40960	80	409.60	See 91.4.
100GBASE-KR4 PMD	2048	4	20.48	Includes delay of one direction through backplane medium.See 93.4.
100GBASE-KP4 PMA/PMD	8192	16	81.92	Includes delay of one direction through backplane medium.See 94.2.5.
100GBASE-CR4 PMD	2048	4	20.48	Does not include delay of cable medium. See 92.4.

[a] For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.110 for the definition of bit time.)
[b] For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

80.5 Skew constraints

Change NOTE 1 in Figure 80-4 as shown:

NOTE1—~~OPTIONAL OR OMITTED DEPENDING~~ CONDITIONAL BASED ON PHY TYPE

Change NOTE 1 in Figure 80-5 as shown:

NOTE1—~~OPTIONAL OR OMITTED DEPENDING~~ CONDITIONAL BASED ON PHY TYPE

Insert Figure 80–5a with introductory text after Figure 80-5:

The skew points are similarly illustrated for a PHY incorporating RS-FEC (see Clause 91) in Figure 80–5a.

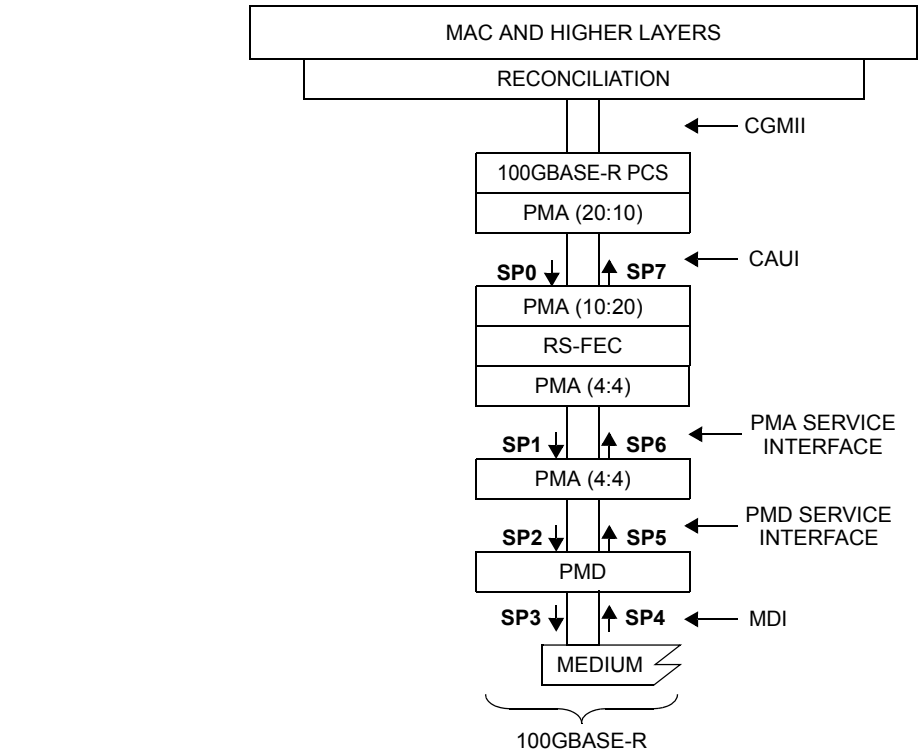


Figure 80–5a—100GBASE-R Skew points with RS-FEC and CAUI

Change Table 80-4 and 80-5 as shown:

Table 80–4—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 40GBASE-R PCS lane (UI)[b]	Maximum Skew for 100GBASE-R PCS lane (UI)[c]	Notes[d]
SP0	29	N/A	≈ 150	See 83.5.3.1
SP1	29	≈ 299	≈ 150	See 83.5.3.1
SP2	43	≈ 443	≈ 222	See 83.5.3.3 or 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP3	54	≈ 557	≈ 278	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP4	134	≈ 1382	≈ 691	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP5	145	≈ 1495	≈ 748	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP6	160	≈ 1649	≈ 824	See 83.5.3.5
SP7	29	N/A	≈ 150	See 83.5.3.5
At PCS receive	180	≈ 1856	≈ 928	See 82.2.12
At RS-FEC transmit	49	N/A	≈ 258	See 91.5.2.2
At RS-FEC receive[e]	180	N/A	≈ 4641	See 91.5.3.1
At PCS receive (with RS-FEC)	49	N/A	≈ 258	See 82.2.12

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PCS lane signaling rate of 10.3125 GBd.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 100GBASE-R, based on 1 UI equals 193.939394 ps at PCS lane signaling rate of 5.15625 GBd.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.
[e]The skew at the RS-FEC receive is the skew between RS-FEC lanes. The symbol ≈ indicates approximate equivalent of maximum Skew in UI for RS-FEC lanes with a signaling rate of 25.78125 Gb/s.

Table 80–5—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 10.3125 GBd PMD lane (UI)[a]	Maximum Skew Variation for 25.78125 GBd PMD lane (UI)[b]	Notes[c]
SP0	0.2	≈ 2	N/A	See 83.5.3.1
SP1	0.2	≈ 2	N/A	See 83.5.3.1
SP2	0.4	≈ 4	≈ 10	See 83.5.3.3 or 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP3	0.6	≈ 6	≈ 15	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP4	3.4	≈ 35	≈ 88	See 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP5	3.6	≈ 37	≈ 93	See 83.5.3.4 or 84.5 or 85.5 or 86.3.2 or 87.3.2 or 88.3.2 or 89.3.2 or 92.5 or 93.5
SP6	3.8	≈ 39	~~N/A~~≈ 98	See 83.5.3.5
SP7	0.2	≈ 2	N/A	See 83.5.3.5
At PCS receive	4	≈ 41	N/A	See 82.2.12
At RS-FEC transmit	0.4	N/A	N/A	See 91.5.2.2
At RS-FEC receive[d]	4	N/A	N/A	See 91.5.3.1
At PCS receive (with RS-FEC)	0.4	N/A	N/A	See 82.2.12

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PMD lane signaling rate of 10.3125 GBd.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 100GBASE-R, based on 1 UI equals 38.787879 ps at PMD lane signaling rate of 25.78125 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.
[d]The skew at the RS-FEC receive is the skew between RS-FEC lanes.

80.7 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 80.7 as shown:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, Clause 73, Clause 74, Clause 81 through Clause 89, Clause 91 through Clause 94, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

81. Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation (XLGMII and CGMII)

81.1 Overview

Change NOTE 1 in Figure 81-1 as shown:

NOTE1—~~OPTIONAL OR OMITTED DEPENDING~~ CONDITIONAL BASED ON PHY TYPE

81.1.1 Summary of major concepts

Insert item g) at the end of the list of major concepts:

g) The XLGMII and CGMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy Efficient Ethernet (EEE) (see Clause 78).

81.1.7 Mapping of XLGMII/CGMII signals to PLS service primitives

Change 81.1.7 for LPI operation:

The Reconciliation Sublayer (RS) shall map the signals provided at the XLGMII/CGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 40 Gb/s and 100 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the XLGMII/CGMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 81.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e. link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 40 Gb/s and 100 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

81.1.7.3 Mapping of PLS_CARRIER.indication

Change 81.1.7.3 for carrier indication definition:

40 Gb/s and 100 Gb/s operation supports full duplex operation only. The RS never generates this primitive for PHYs that do not support EEE.

For PHYs that support EEE capability, CARRIER_STATUS is set in response to LPI_REQUEST as shown in Figure 81–10a.

81.3 XLGMII/CGMII functional specifications

81.3.1.2 TXC<7:0> (transmit control)

Insert the following at the end of 81.3.1.2:

A PHY with EEE capability shall interpret the combination of TXC and TXD as shown in Table 81–3 as an assertion of LPI. Transition into and out of the LPI state is shown in Figure 81–6a.

Change the first reserved row of Table 81-3 and insert a new row immediately below it as follows:

Table 81–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
1	00 through 05~~06~~	Reserved	—
1	06	Only valid on all eight lanes simultaneously to request LPI	No applicable parameter (Normal inter-frame)

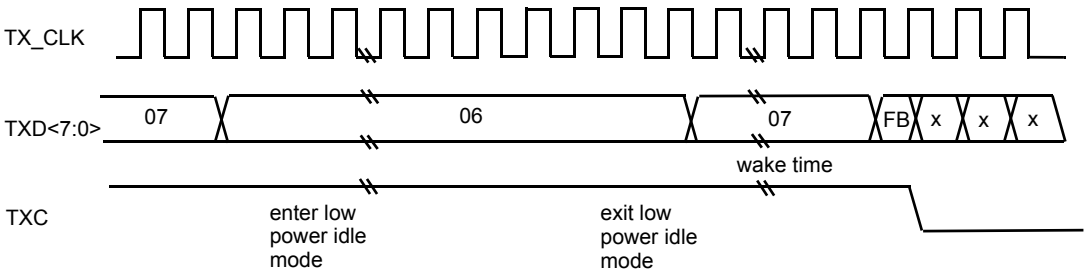
Insert 81.3.1.5 after 81.3.1.4 for transmit LPI transition:

81.3.1.5 Transmit direction LPI transition

LPI operation and the LPI client are described in 78.1. The RS requests the PHY to transition to the LPI state by asserting TXC and setting TXD to 0x06 (in all lanes). The RS maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The RS asserts TXC and asserts IDLE on lanes 0 to 7 in order to make the PHY transition out of the LPI state. The RS should not present a start code for valid transmit data until after the wake up time specified for the PHY ($T_{w\_sys\_tx}$). The wake times are shown in Table 78–4

Figure 81–6a shows the behavior of TXC and TXD<7:0> during the transition into and out of the LPI state.



Note: TXC and TXD are shown for one lane, all 8 lanes behave identically during LPI

Figure 81–6a—LPI transition

Table 81–3 summarizes the permissible encodings of TXD<63:0>, TXC<7:0>.

81.3.2.2 RXC<7:0> (receive control)

Change the first reserved row of Table 81-4 and insert a new row immediately below it as follows:

Table 81–4—Permissible lane encodings of RXD and RXC

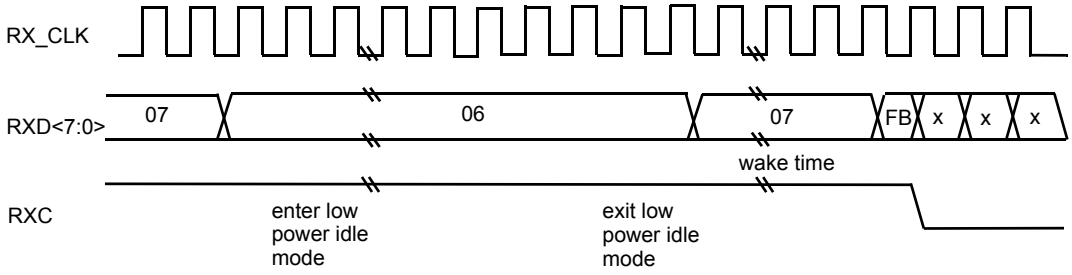
RXC	RXD	Description	PLS_DATA.indication parameter
1	00 through 05~~06~~	Reserved	—
1	06	Only valid on all eight lanes simultaneously to indicate LP_IDLE is asserted	No applicable parameter (Normal inter-frame)

Insert 81.3.2.4 after 81.3.2.3 for receive LPI transition:

81.3.2.4 Receive direction LPI transition

LPI operation and the LPI client are described in 78.1. When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the RS by asserting RXC and setting RXD to 0x06 (in all lanes). The PHY maintains these signals in this state while it remains in the LPI state. When the PHY receives signals from the link partner to indicate transition out of the LPI state it indicates this to the RS by asserting RXC and asserting idle on all lanes 0 to 7 to return to a normal interframe state. The RS shall interpret the LPI coding as shown in Table 81–4.

Figure 81–8a shows the behavior of RXC and RXD<7:0> during LPI transitions.



Note: RXC and RXD are shown for one lane, all 8 lanes behave identically during LPI
Note: In some instances, LPI may be followed by characters other than IDLE during wake time

Figure 81–8a—LPI transition

81.3.4 Link fault signaling

Change the third paragraph of 81.3.4 as follows:

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition, a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS stops sending MAC data or LPI, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). When Remote Fault status is received by an RS, the RS stops sending MAC data or LPI, and continuously gener-

ates Idle control characters. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data or LPI. Note that this behavior only supports bidirectional operation.

Insert a new section, 81.3a before 81.4:

81.3a LPI Assertion and Detection

Certain PHYs support Energy Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the RS to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the XLGMII and CGMII signals as shown in Figure 81–9a.

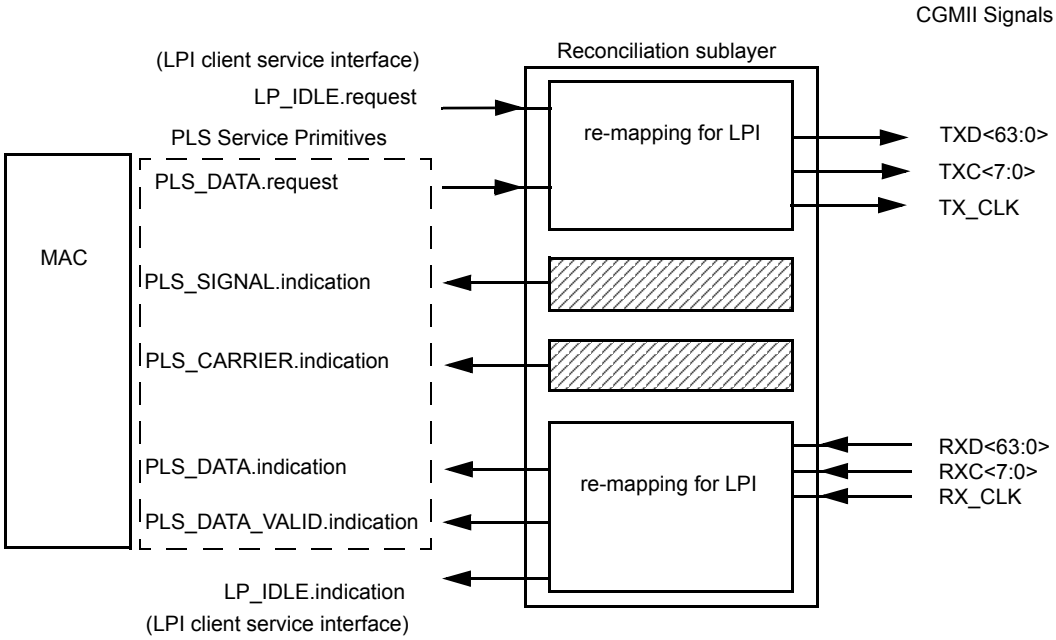


Figure 81–9a—LPI assertion and detection mechanism

The definition of TXC<7:0> and TXD<63:0> is derived from the state of PLS_DATA.request (81.1.7), except when it is overridden by an assertion of Remote Fault or LP_IDLE.request.

Similarly, RXC<7:0> and RXD<63:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected.

PLS_CARRIER.indication(CARRIER_STATUS) will be set to CARRIER_ON when the link is in LPI mode. See 81.1.7.3.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

81.3a.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or de-assertion of LPI from the link partner.

Values: DEASSERT: The link partner is operating with normal inter-frame behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT initiates the signaling of LPI to the link partner. DE-ASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 73.9.1.1) or within 1 second of the change of link_status to OK.

81.3a.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been de-asserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state diagram using PLS_CARRIER.indication(CARRIER_STATUS). The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 81–10a.

Editor's note (to be removed prior to final publication):

The state diagram conventions described in 80.6 apply to all of the state diagrams in this clause.

81.3a.2.1 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

LPI_CARRIER_STATUS

The LPI_CARRIER_STATUS variable indicates how the CARRIER_STATUS parameter is controlled by the LPI_REQUEST parameter. The LPI_CARRIER_STATUS is either TRUE or FALSE as determined by the Transmit LPI state diagram in Figure 81–10a.

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values: FALSE: The device is completely powered (default).
TRUE: The device has not been completely powered.

reset

Used by management to control the resetting of the RS.

Values: FALSE: Do not reset the RS (default).
TRUE: Reset the RS.

tw_timer

A timer that counts the time since the de-assertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2. If PMA Ingress AUI Stop Enable (PIASE) bit (1.7.9) is asserted for any of the PMA sublayers, the terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 plus additional time equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI and CAUI as shown in Table 78–4 for each PMA with PIASE to be asserted. The signal tw_timer_done is asserted when tw_timer reaches its terminal count.

81.3a.2.2 State Diagram

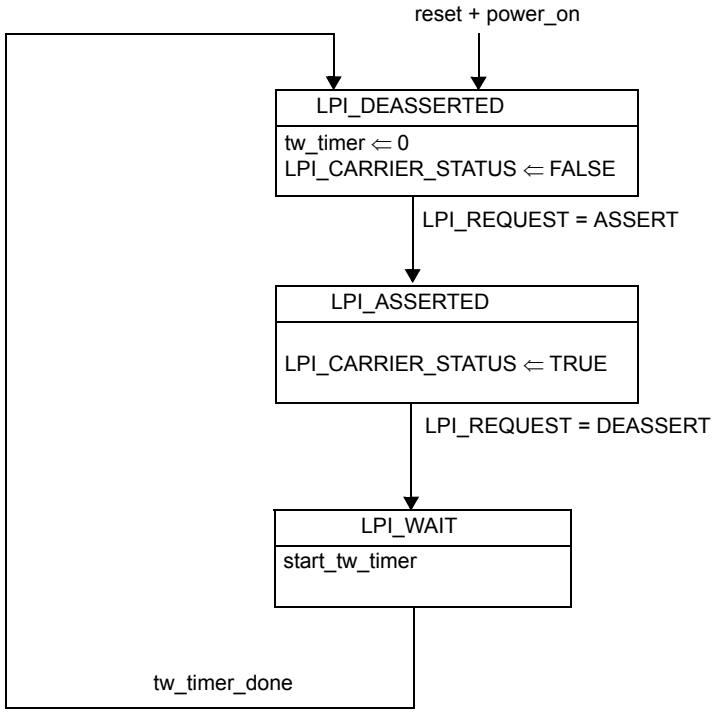


Figure 81–10a—Transmit LPI State Diagram

81.3a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time after it requests the de-assertion of LPI. Buffering and queue management should be designed to accommodate this.

81.3a.4 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal DATA_NOT_VALID on PLS_DATA_VALID.indication while it is detecting LP_IDLE on the XLGMII and CGMII. The receive system should be aware that data frames may arrive at the XLGMII and CGMII following the de-assertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time.

If the PMA Ingress AUI Stop Enable (PIASE) bit (1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI and CAUI in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} (equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI and CAUI as shown in Table 78–4) for each PMA with PIASE to be asserted before setting the PIASE bits.

81.4 Protocol implementation conformance statement (PICS) proforma for Clause 81, Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation[5]

81.4.2.3 Major capabilities/options

Insert the following row at the end of the table in 81.4.2.3:

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	81.1.7		O	Yes [ ] No [ ]

Insert the new subclause 81.4.3.6 after 81.4.3.5 for LPI functions:

81.4.3.6 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	81.3.1.2	As defined in Table 81–3	LPI:M	Yes [ ] N/A [ ]
L2	Assertion of LPI wake time	81.3a.2	As described by Figure 81–10a	LPI:M	Yes [ ] N/A [ ]
L3	Assertion of LPI in Rx direction	81.3.2.2	As defined in Table 81–4	LPI:M	Yes [ ] N/A [ ]
L4	Signal DATA_NOT_VALID on PLS_DATA_VALID.indication	81.3a.4	While detecting LP_IDLE on XLGMII or CGMII	LPI:M	Yes [ ] N/A [ ]

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

Editor's note (to be removed prior to final publication):

The state diagram conventions described in 82.2.18.1 apply to all of the state diagrams in this clause.

82.1.3 Summary of 40GBASE-R and 100GBASE-R sublayers

Change NOTE 1 in Figure 82-1 as follows:

NOTE 1—~~OPTIONAL OR OMITTED DEPENDING~~ CONDITIONAL BASED ON PHY TYPE

Change 82.1.4 as follows:

82.1.4 Inter-sublayer interfaces

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XLGMII/CGMII. The lower interface of the PCS connects to the PMA sublayer to support a PMD. If the optional FEC sublayer is implemented (see Clause 74) and an optional physical instantiation, i.e., XLAUI or CAUI, is not implemented directly below the PCS sublayer, then the lower interface connects to the FEC sublayer. For Physical Layers that use Clause 91 RS-FEC, if an optional physical instantiation, i.e. CAUI, is not implemented directly below the PCS sublayer, then the lower interface connects to the FEC sublayer. The 40GBASE-R PCS has a nominal rate at the PMA/FEC service interface of 10.3125 Gtransfers/s per PCS lane, which provides capacity for the MAC data rate of 40 Gb/s. The 100GBASE-R PCS has a nominal rate at the PMA/FEC service interface of 5.15625 Gtransfers/s per PCS lane, which provides capacity for the MAC data rate of 100 Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

82.1.4.1 PCS service interface (XLGMII/CGMII)

The PCS service interface allows the 40GBASE-R or 100GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is precisely defined as the Media Independent Interface (XLGMII/CGMII) in Clause 81.

82.1.4.2 Physical Medium Attachment (PMA) or Forward Error Correction (FEC) service interface

The PMA or FEC service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The PMA/FEC Service Interface supports the exchange of encoded data between the PCS and PMA or FEC sublayer. The PMA or FEC service interface is defined in 83.3 or 94.2.1 and is an instance of the inter-sublayer service interface definition in 80.3 or 91.2.

Change Figure 82-2 in 82.1.5 for the functional block diagram:

82.1.5 Functional block diagram

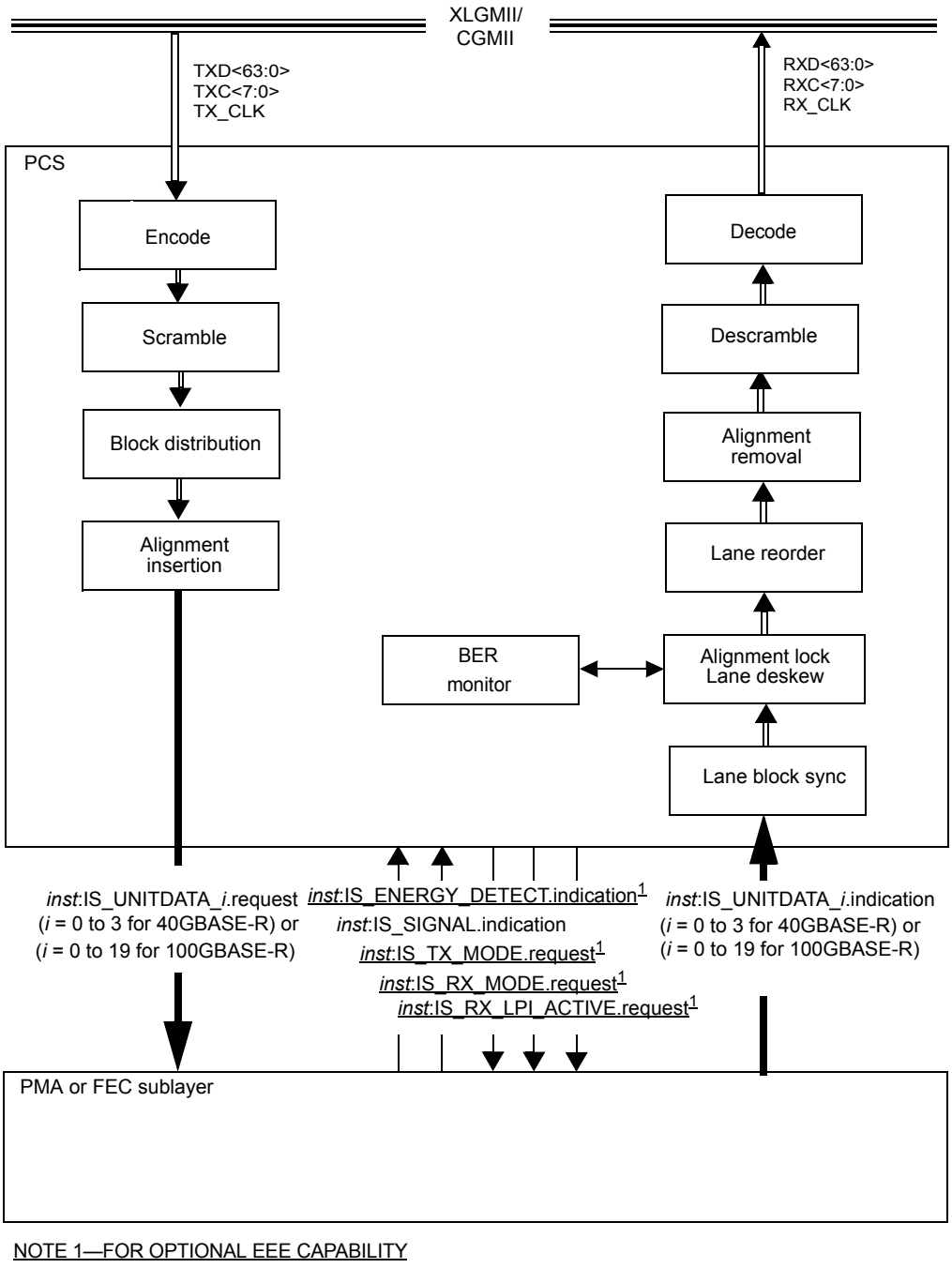


Figure 82–2—Functional block diagram

Change 82.2.3.4 for the control codes

82.2.3.4 Control codes

The same set of control characters are supported by the XLGMII/CGMII and the PCS. The representations of the control characters are the control codes. XLGMII/CGMII encodes a control character into an octet (an eight bit value). The 40GBASE-R and 100GBASE-R PCS encode the start and terminate control characters implicitly by the block type field. The 40GBASE-R and 100GBASE-R PCS encode the ordered_set control

codes using the block type field. The 40GBASE-R and 100GBASE-R PCS encode each of the other control characters into a 7-bit control code.

The control characters and their mappings to 40GBASE-R and 100GBASE-R control codes and XLGMII/CGMII control codes are specified in Table 82–1. All XLGMII/CGMII, 40GBASE-R, and 100GBASE-R control code values that do not appear in the table shall not be transmitted and shall be considered an error if received. The ability to transmit or receive Low Power Idle (LPI) is required for PHYs that support EEE (see Clause 78). If EEE has not been negotiated, LPI shall not be transmitted and shall be treated as an error if received.

Insert LPI row in Table 82-1 between the idle and start rows:

Table 82–1—Control codes

Control character	Notation	XLGMII/ CGMII control code	40/100GBASE-R O code	40GBASE-R and 100GBASE-R control code
LPI	/LI/	0x06		0x06

Change 82.2.3.6 for LPI definition:

82.2.3.6 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XLGMII/CGMII. Idle control characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 8. /I/s may be added following idle control characters or ordered sets. They shall not be added while data is being received.

To communicate LPI, the LPI control character /LI/ is sent continuously in place of /I/. LPI control characters are transmitted when LPI control characters are received from the XLGMII or CGMII. LPI characters may be added or deleted by the PCS to adapt between clock rates in a similar manner to idle control characters. /LI/ insertion and deletion shall occur in groups of 8. /LI/s inserted for clock compensation may only be inserted following other LPI characters.

Insert 82.2.8a after 82.2.8 for RAM definition:

82.2.8a Rapid alignment marker insertion

For the optional EEE capability, an alternate method of alignment is used when operating in the deep sleep low power state. Rapid Alignment Markers (RAMs) function in a similar manner to the alignment markers described in 82.2.7. RAMs are sent in the place of normal alignment markers when the transmitter has an LPI transmit state other than TX_ACTIVE or TX_FW while down_count_done = FALSE. Additionally, the BIP component defined for alignment markers is replaced by a count down field (CD) so that the transition from RAMs to normal alignment markers can be indicated. The RAMs shall be inserted after every 7 66-bit blocks on each 100G PCS lane and every 15 66-bit blocks on each 40G PCS lane. RAM insertion is performed in the same manner as shown in Figure 82–7 and Figure 82–9a. The transition from RAMs to normal alignment markers is shown in Figure 82–9a. The count down field is also used to communicate some of the states of the tx_mode when it is not being used to coordinate the transition. After the LPI Transmit state diagram transitions from TX_ACTIVE to TX_SLEEP, the first RAM shall be inserted after at least one block of /LI/ has been transmitted on PCS lane 0. In order to force the RAMs to coincide with the

start of an FEC block, the distance between the first RAM and preceding normal alignment marker shall be a multiple of 4 66-bit blocks.

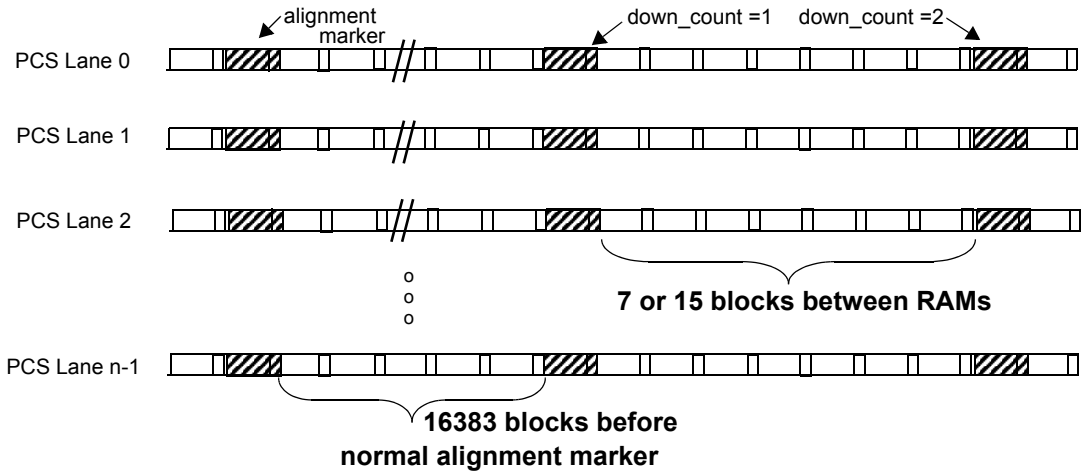


Figure 82–9a—RAM transition

The format of the RAMs is shown in Figure 82–9b.

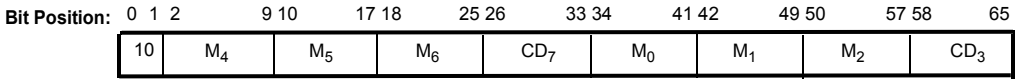


Figure 82–9b—RAM format

The content of the RAMs shall be as shown in Table 82–2a for 100GBASE-R or Table 82–3a for 40GBASE-R. Note that these are similar to normal alignment markers, with CD_3 replacing BIP_3 and CD_7 replacing BIP_7 and also M_0 through M_2 and CD_3 swapped with M_4 through M_6 and CD_7 respectively. As an example, the lane marker for 100GBASE-R lane number 0 is sent as (left most bit sent first):

10 01111100 11101001 01111011 CD_7 10000011 00010110 10000100 CD_3

After the RAMs are inserted, data is sent to the PMA or FEC sublayer adjacent to the PCS.

The value of the CD_3 field is derived by the bit-wise XOR of the down_count variable with the M_0 value for the lane (therefore the last 5 RAMs sent by a 100GBASE-R PCS on PCS lane 0 would have CD_3 values: 0xC4, 0xC5, 0xC2, 0xC3, 0xC0; for PCS lane 1 these would be: 0x98, 0x99, 0x9E, 0x9F, 0x9C). The CD_7 field is the bit-wise inversion of CD_3. The CD field is used by the link partner to understand the expected transition from RAMs to normal AMs. It may also be used by a device with a detached PMA or FEC sublayer to infer the state of the PCS.

If the EEE capability is supported, BIP statistics are only updated when the receiver is in the RX_ACTIVE state (see Figure 82–17). In all other states, the running parity is not calculated. The BIP statistics will be first updated after transitioning from RAMs to normal AMs on the first received normal AM when LPI_FW is FALSE and on the second received AM when LPI_FW is TRUE.

Table 82–2a—100GBASE-R RAM encodings

PCS lane number	Encoding[a] {M_4, M_5, M_6, CD_7, M_0, M_1, M_2, CD_3}	PCS lane number	Encoding[a] {M_4, M_5, M_6, CD_7, M_0, M_1, M_2, CD_3}
0	0x3E, 0x97, 0xDE, CD_7, 0xC1, 0x68, 0x21, CD_3	10	0x02, 0x93, 0x66, CD_7, 0xFD, 0x6C, 0x99, CD_3
1	0x62, 0x8E, 0x71, CD_7, 0x9D, 0x71, 0x8E, CD_3	11	0x46, 0x6E, 0xAA, CD_7, 0xB9, 0x91, 0x55, CD_3
2	0xA6, 0xB4, 0x17, CD_7, 0x59, 0x4B, 0xE8, CD_3	12	0xA3, 0x46, 0x4D, CD_7, 0x5C, 0xB9, 0xB2, CD_3
3	0xB2, 0x6A, 0x84, CD_7, 0x4D, 0x95, 0x7B, CD_3	13	0xE5, 0x07, 0x42, CD_7, 0x1A, 0xF8, 0xBD, CD_3
4	0x0A, 0xF8, 0xF6, CD_7, 0xF5, 0x07, 0x09, CD_3	14	0x7C, 0x38, 0x35, CD_7, 0x83, 0xC7, 0xCA, CD_3
5	0x22, 0xEB, 0x3D, CD_7, 0xDD, 0x14, 0xC2, CD_3	15	0xCA, 0xC9, 0x32, CD_7, 0x35, 0x36, 0xCD, CD_3
6	0x65, 0xB5, 0xD9, CD_7, 0x9A, 0x4A, 0x26, CD_3	16	0x3B, 0xCE, 0xB3, CD_7, 0xC4, 0x31, 0x4C, CD_3
7	0x84, 0xBA, 0x99, CD_7, 0x7B, 0x45, 0x66, CD_3	17	0x52, 0x29, 0x48, CD_7, 0xAD, 0xD6, 0xB7, CD_3
8	0x5F, 0xDB, 0x89, CD_7, 0xA0, 0x24, 0x76, CD_3	18	0xA0, 0x99, 0xD5, CD_7, 0x5F, 0x66, 0x2A, CD_3
9	0x97, 0x36, 0x04, CD_7, 0x68, 0xC9, 0xFB, CD_3	19	0x3F, 0x0F, 0x1A, CD_7, 0xC0, 0xF0, 0xE5, CD_3

[a]Each octet is transmitted LSB to MSB.

Table 82–3a—40GBASE-R RAM encodings

PCS lane number	Encoding[a] {M_4, M_5, M_6, CD_7, M_0, M_1, M_2, CD_3}
0	0x6F, 0x89, 0xB8, CD_7, 0x90, 0x76, 0x47, CD_3
1	0x0F, 0x3B, 0x19, CD_7, 0xF0, 0xC4, 0xE6, CD_3
2	0x3A, 0x9A, 0x64, CD_7, 0xC5, 0x65, 0x9B, CD_3
3	0x5D, 0x86, 0xC2, CD_7, 0xA2, 0x79, 0x3D, CD_3

[a]Each octet is transmitted LSB to MSB.

Change 82.2.11 and Figure 82-10 for LPI override of synchronization:

82.2.11 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 4 (for 40GBASE-R) or 20 (for 100GBASE-R) IS_UNITDATA_*i*.indication primitives. The PCS forms 4 or 20 bit streams from the primitives by concatenating the bits from the indications of each primitive in order from each *inst*:IS_UNITDATA_0.indication to *inst*:IS_UNITDATA_3.indication or

inst:IS_UNITDATA_0.indication to *inst*:IS_UNITDATA_19.indication. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–10.

If EEE is not supported then block_lock is identical to rx_block_lock. Otherwise the relationship between block_lock and rx_block_lock is given by Figure 82–17 the LPI receive state diagram.

82.2.12 PCS lane deskew

Insert the following at the end of 82.2.12, change Figures 82-11 and 82-12 for LPI override of align status:

If EEE is not supported then align_status is identical to rx_align_status. Otherwise the relationship between align_status and rx_align_status is given by Figure 82–17 the LPI receive state diagram.

Insert a row at the end of Table 82-5 as shown:

Table 82–5—Skew tolerance requirements

PCS	Maximum skew	Maximum skew variation
100GBASE-R with RS-FEC	49 ns (~258 bits)	0.4ns (~2 bits)

82.2.18.2.2 Variables

Insert a note in 82.2.18.2.2 below the definition for "align_status":

NOTE: If the EEE capability is supported, then this variable is affected by the LPI receive state diagram. If the EEE capability is not supported then this variable is identical to rx_align_status controlled by the Alignment marker lock state diagram.

Insert a note in 82.2.18.2.2 below the definition for "block_lock":

NOTE: If the EEE capability is supported, then this variable is affected by the LPI receive state diagram. If the EEE capability is not supported then this variable is identical to rx_block_lock controlled by the Block lock state diagram.

Insert the following new variables at appropriate places in 82.2.18.2.2:

rx_align_status
: Variable used by the PCS lane deskew process to reflect the status of the PCS lane-to-lane alignment. This variable is set true when all lanes are synchronized and aligned, set false when the deskew process is not complete.

rx_block_lock<x>
: Variable used by the Block lock state diagram to reflect the status of the code-group delineation for each lane. This variable is set true when the receiver acquires block delineation.

Insert the following new text and variables at the end of the existing subclause 82.2.18.2.2:

The following variables are used only for the EEE capability.

down_count_done
: Boolean variable that indicates that the down_count counter has reached zero.

down_count_enable
: Boolean variable controlling decrement of the counter down_count. This variable is set by the LPI transmit state diagram.

energy_detect
: A parameter generated by the PMA/PMD sublayer to reflect the state of the received signal .In the PMD this has the same definition as parameter signal_detect and is passed through without modification by the PMA (and FEC).

LPI_FW
: Boolean variable controlling the wake mode for the LPI transmit function. This variable is set true when the transmitter is to use the Fast Wake mechanism, and false when the transmitter is to use the optional deep sleep mechanism. This variable defaults true and may only be set to false if the optional deep sleep mode is supported.

received_tx_mode
: Variable reflecting state of the LPI transmit function for the link partner. The value of this variable is inferred from the coding of the RAMs of the incoming data stream and may take the values defined for tx_mode.

rx_lpi_active
: A Boolean variable that is set to true when the receiver is in a low power state and set to false when it is in an active state and capable of receiving data.

Rx LPI indication:
: A Boolean variable indicating the current state of the receive LPI function. This flag is set to true (register bit set to one) when the LPI receive state diagram is in any state other than RX_ACTIVE. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

rx_mode
: A variable reflecting state of the LPI receive function as described by the LPI receive state diagram (Figure 82–17).The parameter has one of two values : DATA and QUIET.

scrambler_bypass
: This Boolean variable is used to bypass the Tx PCS scrambler in order to assist rapid synchronization following low power idle. When set to TRUE, the PCS will pass the unscrambled data from the scrambler input rather than the scrambled data from the scrambler output. The scrambler will continue to operate normally, shifting input data into the delay line. When scrambler_bypass is set to FALSE the PCS will pass scrambled data from the scrambler output.

scr_bypass_enable
: A Boolean variable used to indicate to the transmit LPI state diagram that the scrambler bypass option is required. The PHY shall set scr_bypass_enable = TRUE if Clause 74 FEC is in use. The PHY shall set scr_bypass_enable = FALSE if this FEC is not in use.

tx_mode
: A variable reflecting state of the LPI transmit function as described by the LPI transmit state diagram (Figure 82–16). When tx_mode is set to QUIET the sublayer may go into a low power state.

82.2.18.2.3 Functions

Change 89.2.18.2.3 function definitions for LPI block types:

AM_SLIP

Causes the next candidate block position to be tested. The precise method for determining the next candidate block position is not specified and is implementation dependent. However, an implementation shall ensure that all possible blocks are evaluated.

DECODE(rx_coded<65:0>)

Decodes the 66-bit vector returning rx_raw<71:0>, which is sent to the XLGMII/CGMII. The DECODE function shall decode the block as specified in 82.2.3.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<65:2> is sent to the scrambler. The two bits of the sync header bypass the scrambler. The ENCODE function shall encode the block as specified in 82.2.3.

R_TYPE(rx_coded<65:0>)

This function classifies the current rx_coded<65:0> vector as belonging to one of the following ~~five~~ types, depending on its contents. The classification results are returned via the r_block_type variable.

Values: C; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x1E and eight valid control characters other than /E/ or /LI/;
b) A block type field of 0x4B.
LI; For EEE capability, the LI type is supported where the vector contains a sync header of 10, a block type field of 0x1E and eight control characters of 0x06 (/LI/).
S; The vector contains a sync header of 10 and the following:
a) A block type field of 0x78.
T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a sync header of 01.
E; The vector does not meet the criteria for any other value.

Valid control characters are specified in Table 82–1.

Note: A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

R_TYPE_NEXT

This function classifies the 66-bit rx_coded vector that immediately follows the current rx_coded<65:0> vector as belonging to one of the five types defined in R_TYPE, depending on its contents. It is intended to perform a prescient end of packet check. The classification results are returned via the r_block_type_next variable.

SLIP

Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_TYPE = (tx_raw<71:0>)

This function classifies each 72-bit tx_raw vector as belonging to one of the following ~~five~~ types depending on its contents. The classification results are returned via the t_block_type variable.

Values: C; The vector contains one of the following:
a) Eight valid control characters other than /O/, /S/, /T/, /LI/, and /E/;
b) One valid ordered set.
LI; For EEE capability, this vector contains eight /LI/ characters.

S; The vector contains an /S/ in its first character, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XLGMII/CGMII control code specified in Table 82–1. A valid ordered_set consists of a valid /O/ character in the first character and data characters in the seven characters following the /O/. A valid /O/ is any character with a value for O code in Table 82–1.
Note: A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

82.2.18.2.4 Counters

Change the definition for am_counter in 82.2.18.2.4 for RAMs:

am_counter
This counter counts 16383 66-bit blocks that separate two consecutive alignment markers. This counter counts 7 66-bit blocks for 100GBASE-R PCS or 15 66-bit blocks for 40GBASE-R PCS that separate two consecutive rapid alignment markers for the optional EEE capability.

Insert new counters into 82.2.18.2.4, and new timers into 82.2.18.2.5 in support of the LPI state diagrams. In each case, insert the new text at the end of the existing subclause:

The following counters are used only for the EEE capability.

down_count
A counter that is used in rapid alignment markers and is decremented each time a RAM is sent while variable down_count_enable = true. The counter initial value is set by the LPI transmit state diagram. When the down_count counter reaches zero it will set the variable down_count_done = true.
wake_error_counter
A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.10)

82.2.18.2.5 Timers

The following timers are used only for the EEE capability.

one_us_timer
A timer used to count approximately 1 μs intervals. The timer terminal count is set to T_{1U}. When the timer reaches terminal count it will set one_us_timer_done = true.
rx_tq_timer
This timer is started when the PCS receiver enters the RX_SLEEP state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set rx_tq_timer_done = true.
rx_tw_timer
This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count is set to a value no larger than the maximum value given for T_{WR} in Table 82–5b. When the timer reaches terminal count it will set rx_tw_timer_done = true.

rx_wf_timer

This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the QUIET state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count it will set the rx_wf_timer_done = true.

scr_byp_timer

This timer is started when the PCS transmitter enters the TX_SCR_BYPASS state. The timer terminal count is set to T_{BYP}. When the timer reaches terminal count it will set the scr_byp_timer_done = true.

tx_ts_timer

This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = true.

tx_tq_timer

This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = true.

tx_tw_timer

This timer is started when the PCS transmitter enters the TX_WAKE or FW_TX_WAKE state. The timer terminal count is set to T_{WL}. When the timer reaches terminal count it will set the tx_tw_timer_done = true.

tx_tw2_timer

This timer is started when the PCS transmitter enters the TX_WAKE2 state. The timer terminal count is set to T_{WL2}. When the timer reaches terminal count it will set the tx_tw2_timer_done = true.

82.2.18.3 State diagrams

Insert 82.2.18.3.1, Table 82–5a, and Table 82–5b at the end of 82.2.18.3:

82.2.18.3.1 LPI state diagrams

A PCS which supports the EEE capability shall implement the LPI transmit and receive processes as shown in Figure 82–16 and Figure 82–17. The transmit LPI state diagram controls tx_mode which disables the transmitter when it is set to QUIET. The receive LPI state diagram controls block_lock during LPI and signals the end of LPI to the receive state diagram.

Following a period of LPI, the receiver is required to achieve block synchronization within the wakeup time specified (See Figure 82–17). The implementation of the block synchronization state diagram should use techniques to ensure that block lock is achieved with minimal numbers of slip attempts. If Fast Wake is selected then the receiver is expected to maintain sufficient state to allow much faster wake up.

The LPI functions shall use timer values for these state diagrams as shown in Table 82–5a for transmit and Table 82–5b for receive.

Table 82–5a—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to QUIET, LPI_FW = FALSE	0.9	1.1	µs
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to FW, LPI_FW = TRUE	240	260	ns
T_{QL}	Local Quiet Time from when tx_mode is set to QUIET or FW to entry into the TX_WAKE state	1.7	1.8	ms
T_{WL}	Time spent in the TX_WAKE state, LPI_FW = FALSE	1.5	1.6	µs
T_{WL}	Time spent in the FW_TX_WAKE state, LPI_FW = TRUE	312	332	ns
T_{WL2}	Time spent in the TX_WAKE2 state	2.4	2.5	µs
T_{BYP}	Time spent in the TX_SCR_BYPASS state, 40 Gb/s operation	0.9	1.1	µs
T_{BYP}	Time spent in the TX_SCR_BYPASS state, 100 Gb/s operation	1.9	2.1	µs
T_{1U}	Time spent in the TX_ALERT state	1.1	1.3	µs

Table 82–5b—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for energy_detect to be set to true while in the RX_SLEEP and RX_QUIET or RX_FW states before asserting receive fault	2	3	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, LPI_FW = TRUE.	—	300	ns
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, LPI_FW = FALSE, scr_bypass_enable = FALSE.	—	4.5	µs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, LPI_FW = FALSE, scr_bypass_enable = TRUE, 40 Gb/s.	—	5.5	µs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, LPI_FW = FALSE, scr_bypass_enable = TRUE, 100 Gb/s.	—	6.5	µs
T_{WTF}	Wake time fault recovery time	—	10	ms

82.3.1 PMD MDIO function mapping

Insert the following row at the bottom of Table 82-6 in 82.3.1:

Table 82–6—MDIO/PMD control variable mapping

MDIO control variable	PCS register name	Register/ bit number	PCS control variable
LPI_FW	LPI fast wake enable	3.20.0	LPI_FW

Insert the following rows at the bottom of Table 82-7 in 82.3.1:

Table 82–7—MDIO/PMD status variable mapping

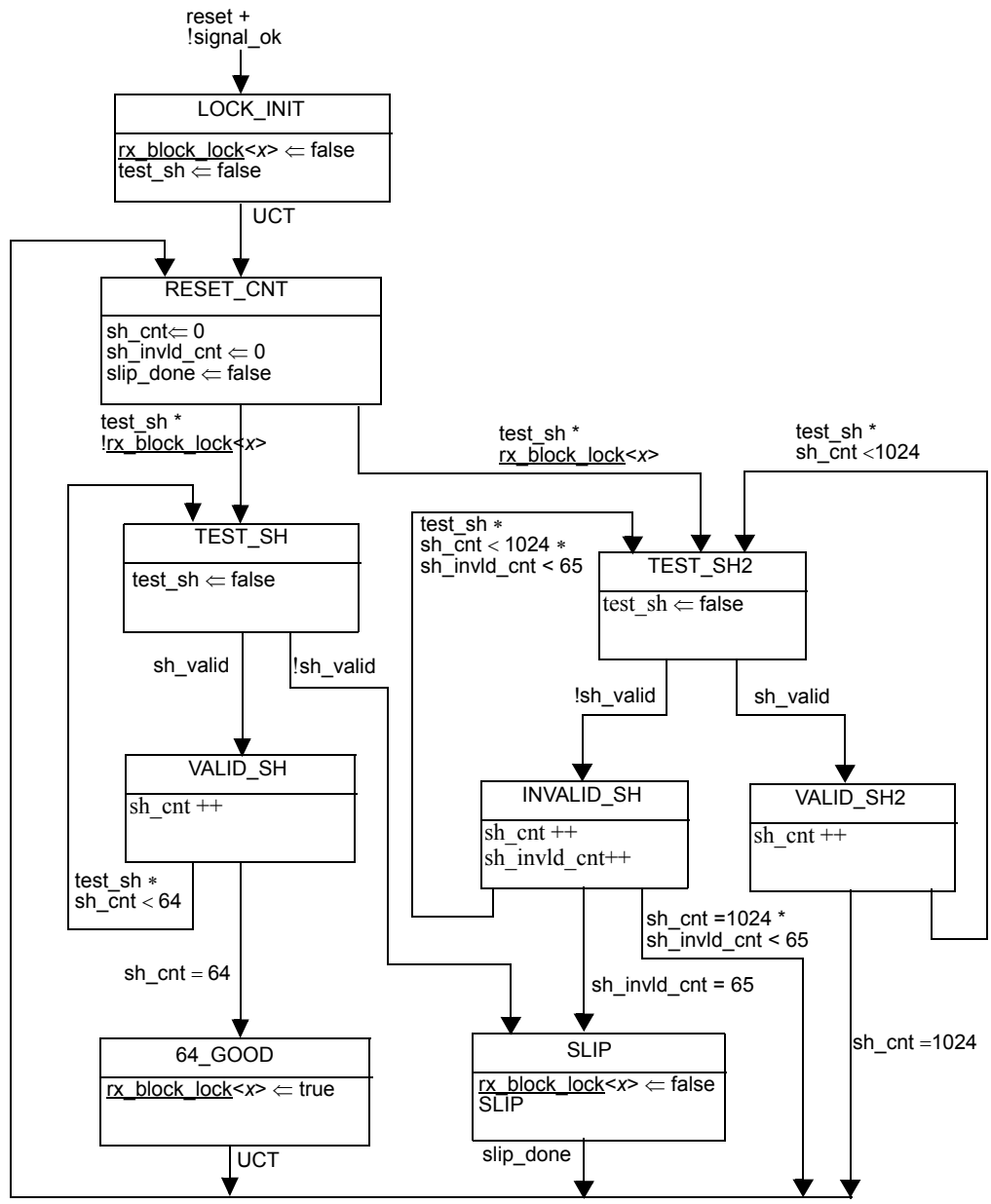
MDIO status variable	PCS register name	Register/ bit number	PCS status variable
Tx LPI indication	Tx LPI indication	3.1.9	Tx LPI indication
Tx LPI received	Tx LPI received	3.1.11	Tx LPI received
Rx LPI indication	Rx LPI indication	3.1.8	Rx LPI indication
Rx LPI received	Rx LPI received	3.1.10	Rx LPI received
Wake_error_counter	Wake_error_counter	3.22	Wake_error_counter

82.6 Auto-Negotiation

Change 82.6 to add new PHY types

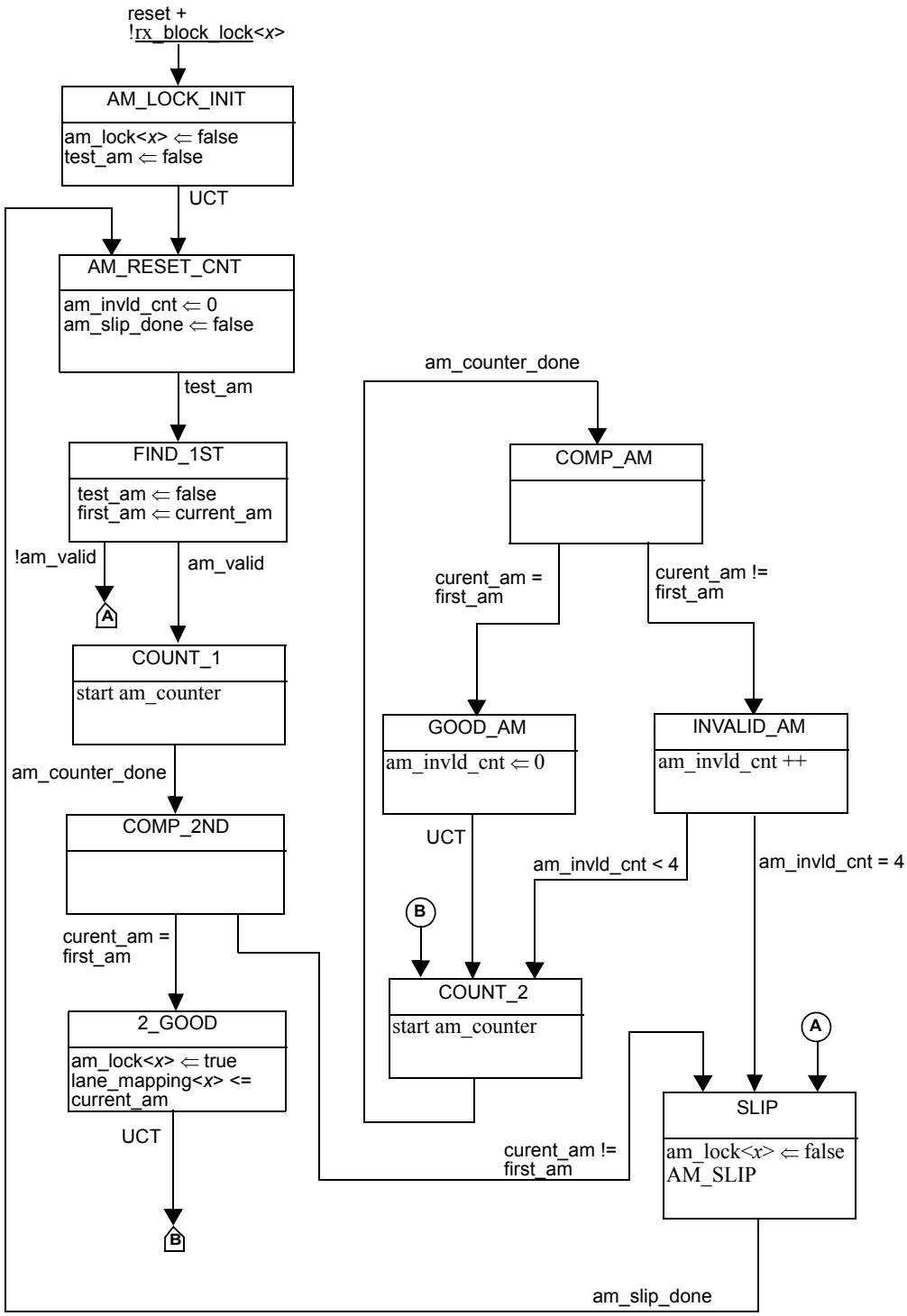
The following requirements apply to a PCS used with a 40GBASE-KR4 PMD, 40GBASE-CR4 PMD, ~~or~~ 100GBASE-CR10, 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-KP4 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

Change figures 82-10, 82-11, 82-12, 82-13, 82-14 and 82-15; insert figures 82-16 and 82-17



NOTE— rx_block_lock<*x*> refers to the received lane *x* of the service interface, where *x* = 0:3 (for 40GBASE-R) or 0:19 (for 100GBASE-R)

Figure 82–10—Block lock state diagram



NOTE— am_lock<*x*> refers to the received lane *x* of the service interface, where *x* = 0:3 (for 40GBASE-R) or 0:19 (for 100GBASE-R)

Figure 82–11—Alignment marker lock state diagram

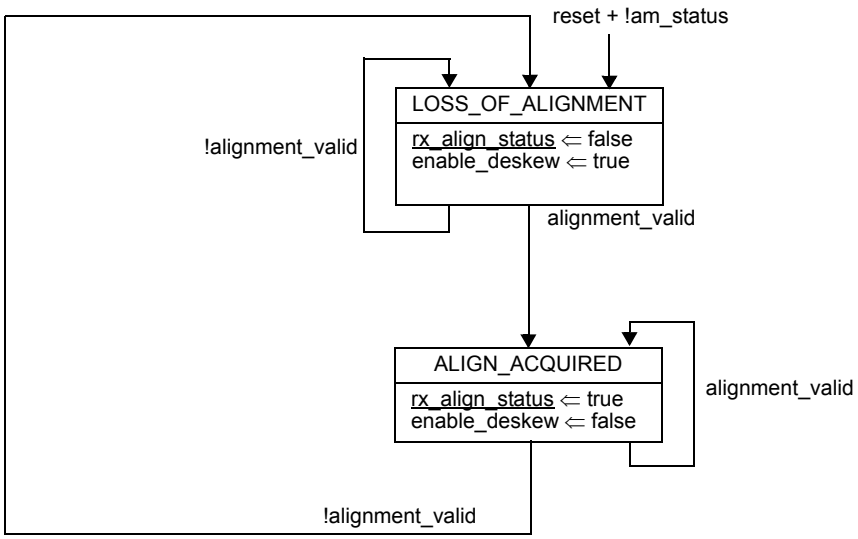


Figure 82–12—PCS deskew state diagram

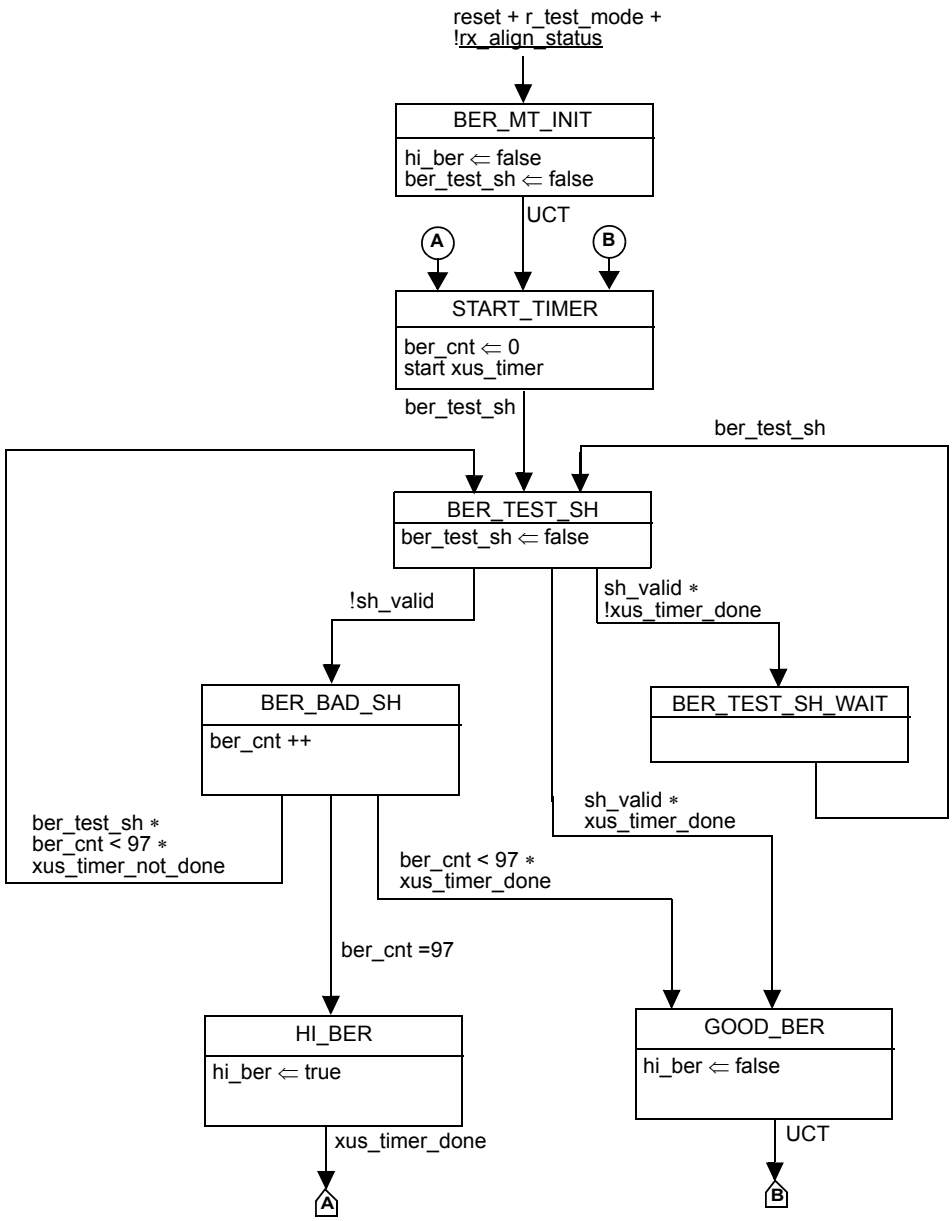


Figure 82–13—BER monitor state diagram

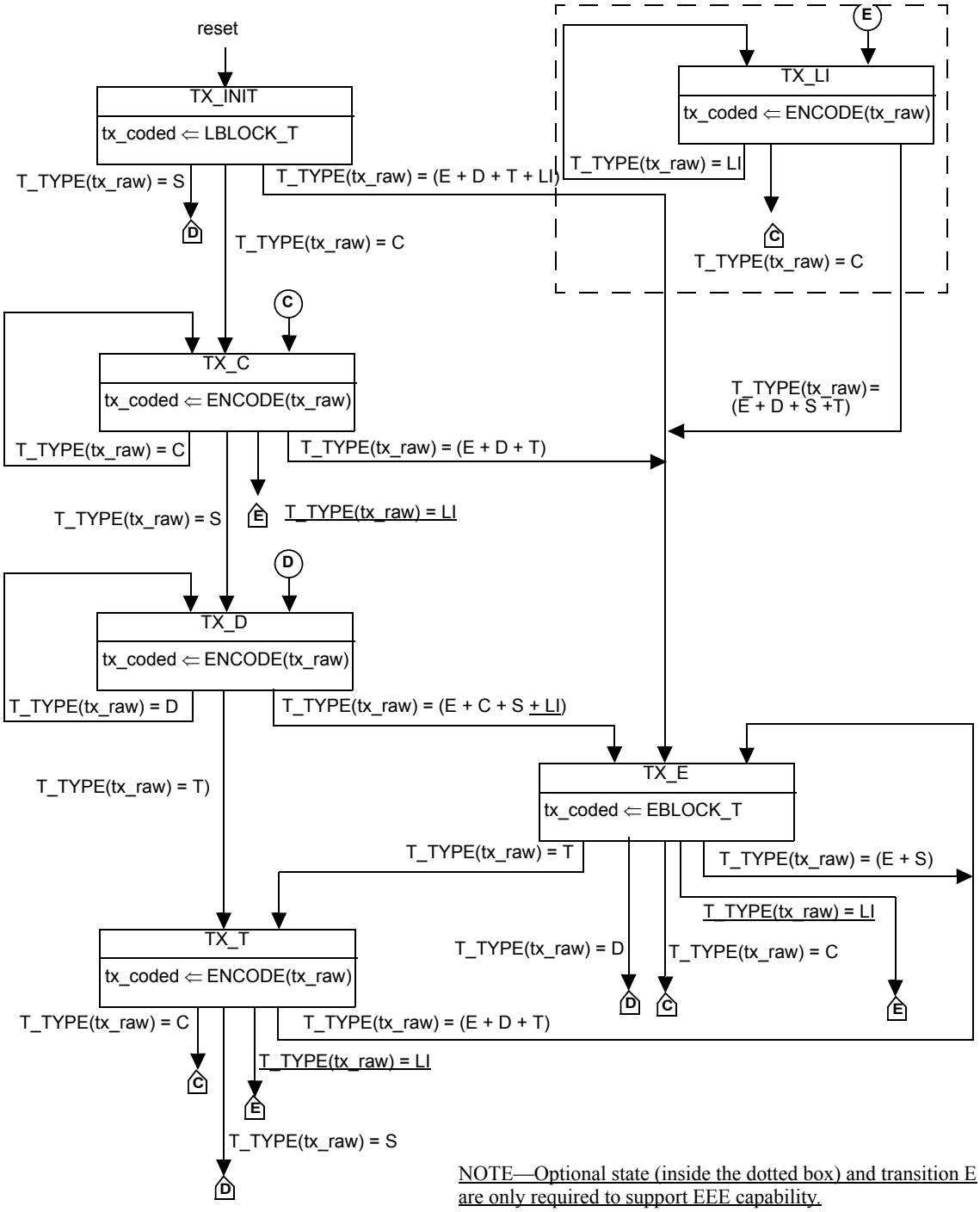
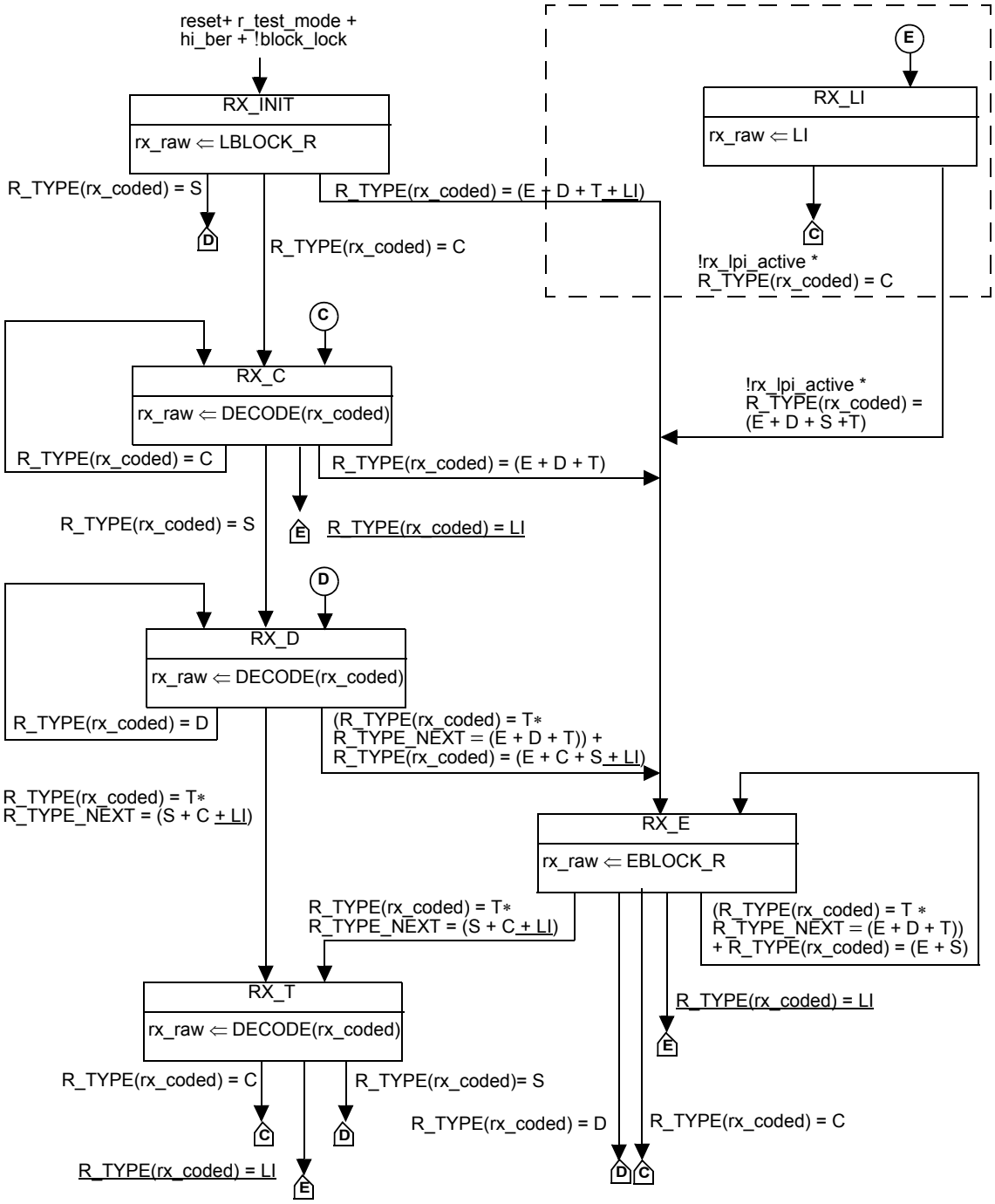


Figure 82–14—Transmit state diagram



NOTE—Optional state (inside the dotted box) and transition E are only required to support EEE capability.

Figure 82–15—Receive state diagram

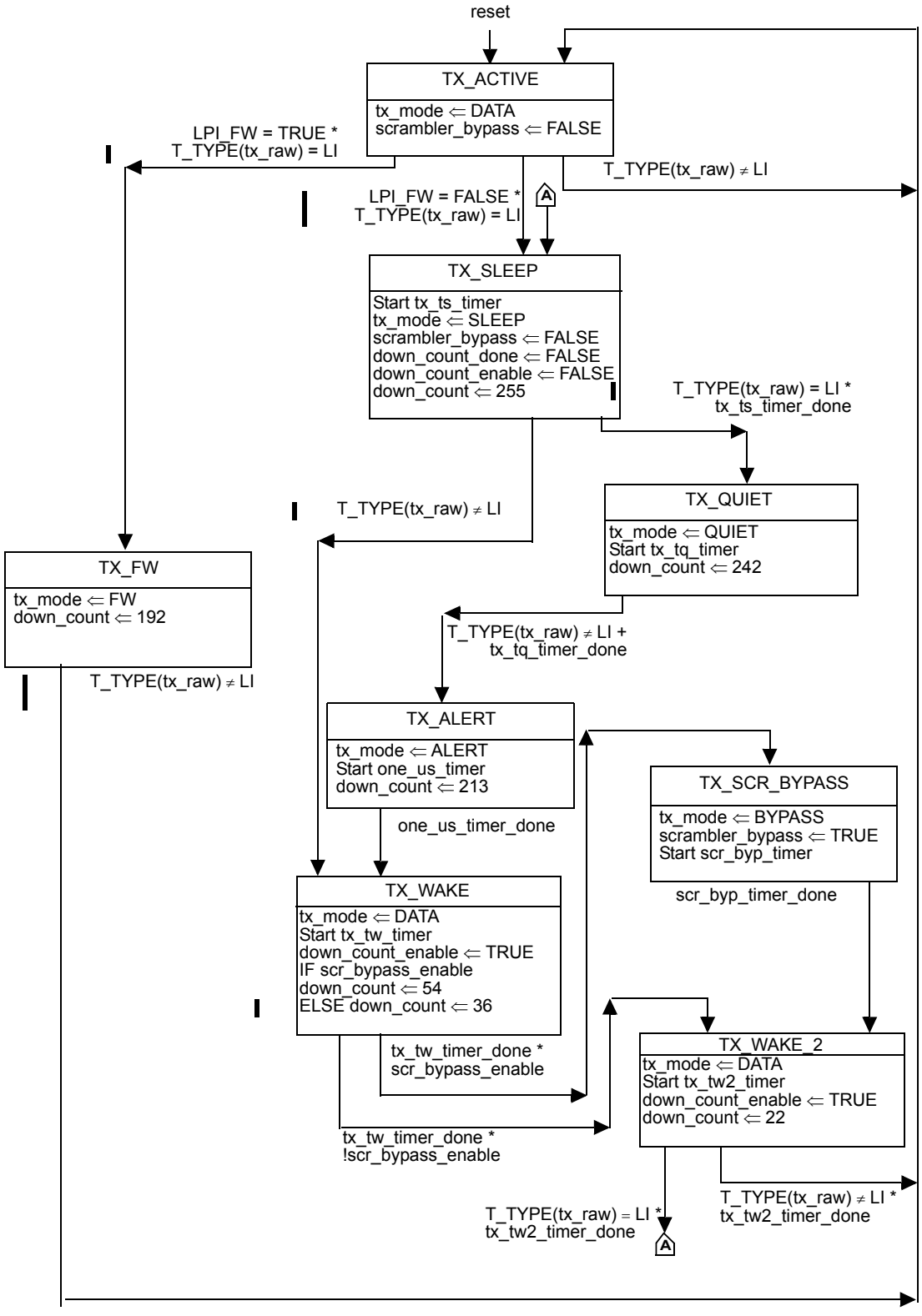


Figure 82–16—LPI Transmit state diagram

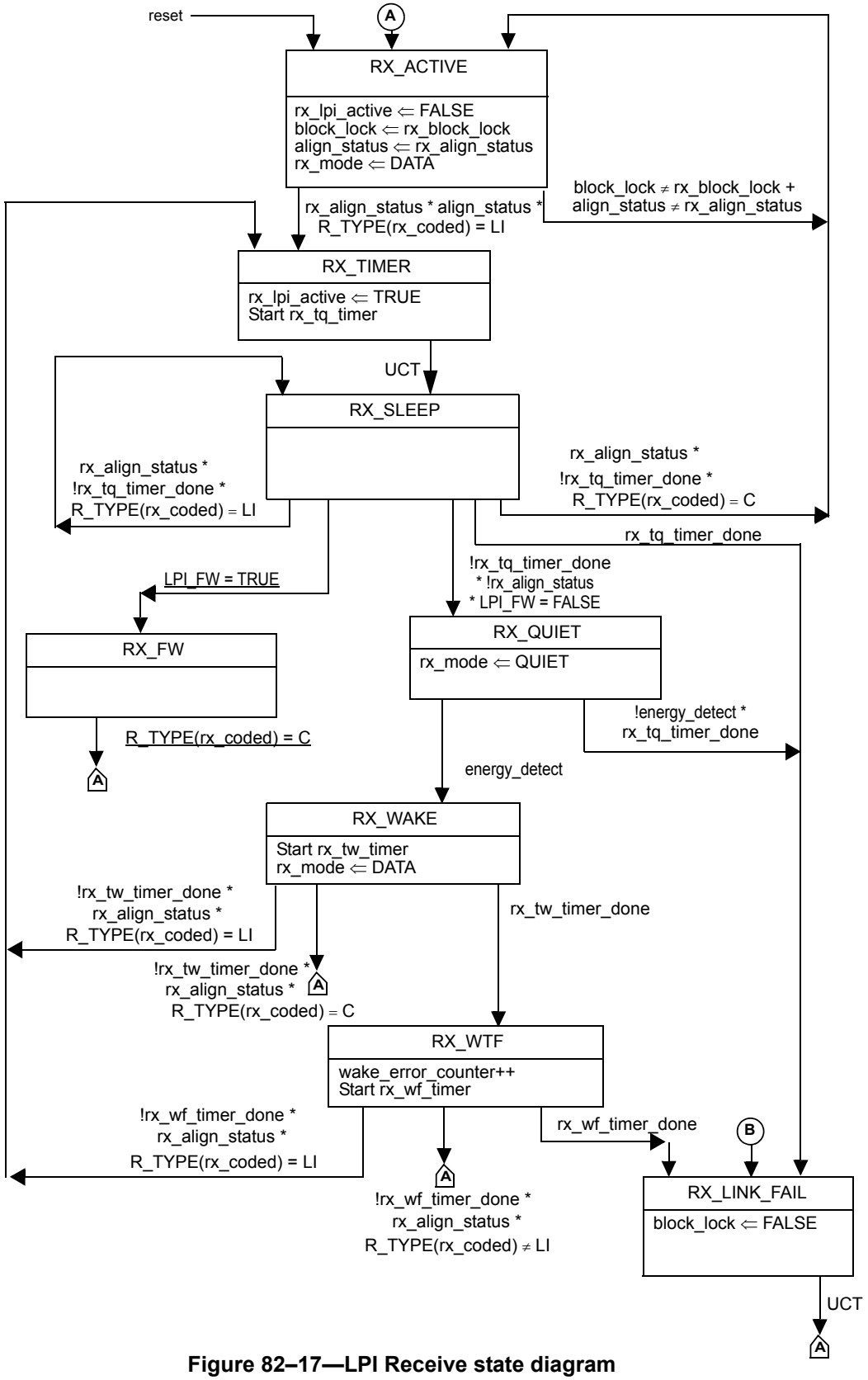


Figure 82–17—LPI Receive state diagram

82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R[6]

Insert the following row at the end of the table in 82.7.3:

82.7.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	82.2.3.4		O	Yes [ ] No [ ]

Change rows AN1* and AN2 in 82.7.6.5:

82.7.6.5 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
AN1*	Support for use with a 40GBASE-KR4, 40GBASE-CR4, ~~or~~ 100GBASE-CR10 PMD, 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-KP4	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ]
AN2	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with ~~10GBASE-KR PMD~~, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10 PMD, 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-KP4	AN1:M	Yes [ ]

Insert the new subclause 82.7.6.6 after 82.7.6.5 for LPI functions:

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

82.7.6.6 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Support for both wake modes	82.2.18.2.2	Variable LPI_FW may be true or false	LPI:O	Yes [ ] No [ ]
LP-02	Insertion and deletion of LPIs in groups of 8	82.2.3.6		LPI:M	Yes [ ] No [ ]
LP-03	RAM insertion	82.2.8a	Insertion of Rapid Alignment Markers meets the requirements of 82.2.8a	LPI:M	Yes [ ] No [ ]
LP-04	Transmit state diagrams	82.2.18.3	Support LPI operation in Figure 82–14	LPI:M	Yes [ ] No [ ]
LP-05	Receive state diagrams	82.2.18.3	Support LPI operation in Figure 82–15	LPI:M	Yes [ ] No [ ]
LP-06	LPI transmit state diagrams	82.2.18.3.1	Meets the requirements of Figure 82–16	LPI:M	Yes [ ] No [ ]
LP-07	LPI receive state diagrams	82.2.18.3.1	Meets the requirements of Figure 82–17	LPI:M	Yes [ ] No [ ]
LP-08	LPI transmit timing	82.2.18.3.1	Meets the requirements of Table 82–5a	LPI:M	Yes [ ] No [ ]
LP-09	LPI receive timing	82.2.18.3.1	Meets the requirements of Table 82–5b	LPI:M	Yes [ ] No [ ]

83. Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R

83.1 Overview

Change NOTE 1 in Figure 83-1 as shown:

NOTE1—~~OPTIONAL OR OMITTED DEPENDING~~ CONDITIONAL BASED ON PHY TYPE

Change the first paragraph of 83.1.1 as follows:

83.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) that is common to two families of (40 Gb/s and 100 Gb/s) Physical Layer implementations, known as 40GBASE-R and 100GBASE-R. The PMA allows the PCS (specified in Clause 82) to connect in a media-independent way with a range of physical media. The 40GBASE-R PMA(s) can support any of the 40 Gb/s PMDs in Table 80–2. The 100GBASE-R PMA(s) can support any of the 100 Gb/s PMDs in ~~Table 80–2~~Table 80–2a, but does not provide the PMD service interfaces for 100GBASE-KP4 (Clause 94). The terms 40GBASE-R and 100GBASE-R are used when referring generally to Physical Layers using the PMA defined in this clause.

83.3 PMA service interface

Change third paragraph of 83.3 for FEC types:

If the PMA client is the PCS or ~~an~~ a BASE-R FEC sublayer (see Clause 74), the PMA (or PMA client) continuously sends four (for 40GBASE-R) or twenty (for 100GBASE-R) parallel bit streams to the PMA client (or PMA), each at the nominal signaling rate of the PCSL. If the PMA client is the 100GBASE-R RS-FEC sublayer (see Clause 91), the PMA continuously sends four parallel bit streams to the PMA client (or PMA), each at 25.78125 GBd.

Insert the following at the end of 83.3 for the EEE service interface:

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.3) then the inter-sublayer service interface includes three additional primitives defined as follows:

IS_TX_MODE.request
IS_RX_MODE.request
IS_ENERGY_DETECT.indication

The IS_TX_MODE.request primitive is used to communicate the state of the PCS LPI transmit function to other sublayers in the PHY. The IS_RX_MODE.request primitive is used to communicate the state of the PCS LPI receive function to other sublayers. The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence.

A physically instantiated service interface with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option (see 78.3) may enter a low power state to conserve energy during periods of low link utilization. The ability to support transition to a low power state in the ingress direction is indicated by register 1.1.9 (PMA Ingress AUI Stop Ability, PIASA) and register 1.1.8 for the egress direction (PMA Egress AUI Stop Ability, PEASA). Transition to the low power state is enabled in the ingress direction by

register 1.7.9 (PMA Ingress AUI Stop Enable, PIASE) and register 1.7.8 for the egress direction (PMA Egress AUI Stop Enable, PEASE). The system shall not assert the enable bit for an interface unless the corresponding ability bit at the other side of the interface is also asserted. If the PIASE bit is TRUE, then the PMA may disable transmitters on the physical instantiation of the ingress AUI when rx_mode is QUIET. If the PEASE bit is TRUE, then the PMA may disable transmitters on the physical instantiation of the egress AUI when tx_mode is QUIET.

Change the second paragraph of 83.5.3 as follows:

83.5.3 Skew and Skew Variation

Any PMA that combines PCSLs from different input lanes onto the same output lane must tolerate Skew Variation between the input lanes without changing the PCSL positions on the output. Skew and Skew Variation are defined in 80.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP0, SP1, and SP2 in the transmit direction and SP5, ~~and~~ SP6, and SP7 in the receive direction as defined in 80.5 and illustrated in Figure 80–4, ~~and~~ Figure 80–5, and Figure 80–5a.

Insert 83.5.3.a before 83.5.3.1 as follows:

83.5.3.a Skew generation toward SP0

In an implementation with one or more physically instantiated CAUI interfaces, the PMA that sends data in the transmit direction toward the CAUI that is closest to the RS-FEC (SP0 in Figure 80–5a) shall produce no more than 29 ns of Skew between PCSLs toward the CAUI, and no more than 200 ps of Skew Variation.

Insert 83.5.3.7 after 83.5.3.6 as follows:

83.5.3.7 Skew generation toward SP7

In an implementation with one or more physically instantiated CAUI interfaces and RS-FEC, at SP7 (the receive direction of the CAUI closest to the PCS), the PMA or group of PMAs between the RS-FEC and the CAUI closest to the PCS shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the CAUI in the Rx direction.

Change the first paragraph of 83.5.8 as follows:

83.5.8 PMA local loopback mode

PMA local loopback shall be provided by the PMA adjacent to the PMD for 40GBASE-KR4, 40GBASE-CR4, ~~and~~ 100BASE-CR10, 100GBASE-KR4, and 100GBASE-CR4 PMDs. PMA local loopback mode is optional for other PMDs or for PMAs not adjacent to the PMD. If it is implemented, it shall be as described in this subclause (83.5.8).

83.6 PMA MDIO function mapping

Insert rows at the end of Table 83-2 for fast wake and stop enable:

Insert rows at the end of Table 83-3 for stop ability:

Table 83–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PIASE	PMA ingress AUI stop enable	1.7.9	PIASE
PEASE	PMA egress AUI stop enable	1.7.8	PEASE

Table 83–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PIASA	PMA ingress AUI stop ability	1.1.9	PIASA
PEASA	PMA egress AUI stop ability	1.1.8	PEASA

83.7 Protocol implementation conformance statement (PICS) proforma for Clause 83, Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R[7]

Change the row identified and insert the LPI row at the end of the table in 83.7.3:

83.7.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*KRCR	PMA adjacent to the PMD for 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-CR4, or 100GBASE-CR10	83.5.8		O	Yes [ ] No [ ]
*LPI	Implementation of LPI with the deep sleep mode option	83.3		O	Yes [ ] No [ ]

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84. Physical Medium Dependent sublayer and baseband medium, type 40GBASE-KR4

84.1 Overview

Insert a row at the end of Table 84-1 for EEE:

Table 84–1—Physical Layer clauses associated with the 40GBASE-KR4 PMD

Associated clause	40GBASE-KR4
78—Energy Efficient Ethernet	Optional

Insert the following at the end of 84.1:

40GBASE-KR4 PHYs with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78).

84.2 Physical Medium Dependent (PMD) service interface

Insert the following at the end of 84.2 for the EEE service interface

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.3) then the inter-sublayer service interface includes two additional primitives defined as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

The TX_MODE parameter takes on one of six values: DATA, SLEEP, QUIET, FW, ALERT or BYPASS. When TX_MODE = QUIET, transmission is disabled; when TX_MODE = ALERT, the alert signal is transmitted. Note: if Clause 74 FEC is in use, only the values DATA, QUIET and ALERT may be passed through the FEC to the PMD.

The RX_MODE parameter is used to communicate the state of the PCS LPI receive function and takes the value QUIET or DATA.

84.3 PCS requirements for Auto-Negotiation (AN) service interface

Insert the following paragraph at the end of 84.3:

The 40GBASE-KR4 PHY may be extended using XLAUI as a physical instantiation of the inter-sublayer service interface between devices. If XLAUI is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

84.7 PMD functional specifications

84.7.2 PMD Transmit function

Insert the following at the end of 84.7.2 for the EEE function:

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78) then when tx_mode is set to ALERT, the adjacent PMA sends a repeating 16-bit pattern, hexadecimal 0xFF00, to the PMD, which the PMD transmits. When tx_mode is ALERT, the transmitter equalizer taps shall be set to the preset state specified in 72.6.10.2.3.1. When tx_mode is QUIET, the transmitter shall be disabled as specified in 84.7.6. For all other states of tx_mode, the driver coefficients are restored to their states resolved during training.

84.7.4 Global PMD signal detect function

Insert the following at the end of the first paragraph:

When the PHY supports the optional EEE capability with the deep sleep mode, PMD_SIGNAL.indication is also used to indicate when the ALERT signal is detected, which corresponds to the beginning of a refresh or a wake.

Insert the following at the beginning of the second and third paragraphs:

When the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA

Insert the following at the end of the third paragraph:

When the PHY supports the EEE capability with the deep sleep mode, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that corresponds to an ALERT transmission (see 84.7.2) from the link partner. While rx_mode = QUIET, SIGNAL_DETECT shall be held at FAIL as long as the signal at the receiver input corresponds to a QUIET tx_mode (see 84.7.6) of the link partner.

84.7.6 Global PMD transmit disable function

Change 84.7.6 for the EEE transmit_disable:

The Global_PMD_transmit_disable function is mandatory if EEE with the deep sleep mode option is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 72–7.
b) If a PMD_fault (84.7.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 84.7.8, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 72.7.1.4. The PMD_transmit_disable

function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 72.7.1.4.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.7.

84.11 Protocol implementation conformance statement (PICS) proforma for Clause 84, Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-KR4[8]

Insert the following row at the end of the table in 84.11.3:

84.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI with the deep sleep mode option	84.1		O	Yes [ ] No [ ]

84.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and base-band medium, type 40GBASE-CR4 and 100GBASE-CR10

Insert the following rows at the end of the table in 84.11.4.1:

84.11.4.1 PMD functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
FS13	Transmit function for EEE	84.7.2	Transmitter behavior during ALERT and QUIET	LPI:M	Yes [ ] No [ ]
FS14	Signal detect function for EEE	84.7.4		LPI:M	Yes [ ] No [ ]
FS15	Transmit disable during LPI	84.7.6	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] No [ ]

Insert the following rows at the end of the table in 84.11.4.3:

84.11.4.3 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC3	Output Amplitude LPI voltage	84.7.6	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] No [ ]
TC4	Output Amplitude ON voltage	84.7.6	Greater than 90% of previous level within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] No [ ]

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85. Physical Medium Dependent sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10

85.1 Overview

Insert a row at the end of Table 85-1 for EEE:

Table 85–1—Physical Layer clauses associated with the 40GBASE-CR4 and 100GBASE-CR10 PMDs

Associated clause	40GBASE-CR4	100GBASE-CR10
78—Energy Efficient Ethernet	Optional	Optional

Insert the following at the end of 85.1:

100GBASE-CR10 and 40GBASE-CR4 PHYs with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78).

85.2 Physical Medium Dependent (PMD) service interface

Insert the following at the end of 85.2 for the EEE service interface

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.3) then the inter-sublayer service interface includes two additional primitives defined as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

The TX_MODE parameter takes on one of eight values: DATA, SLEEP, QUIET, FW, ALERT, RF_ALERT, WAKE or RF_WAKE. When TX_MODE = QUIET, transmission is disabled; when TX_MODE = ALERT or RF_ALERT, the alert signal is transmitted. Note: if Clause 74 FEC is in use, only the values DATA, QUIET and ALERT may be passed through the FEC to the PMD.

The RX_MODE parameter is used to communicate the state of the PCS LPI receive function and takes the value QUIET or DATA.

85.3 PCS requirements for Auto-Negotiation (AN) service interface

Insert the following paragraph at the end of 85.3:

The 40GBASE-CR4 PHY may be extended using XLAUI a physical instantiation of the inter-sublayer service interface between devices. Similarly, the 100GBASE-CR10 PHY may be extended using CAUI. If XLAUI or CAUI is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to

relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

85.7 PMD functional specifications

85.7.2 PMD Transmit function

Insert the following at the end of 85.7.2 for the EEE function:

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78) then when tx_mode is set to ALERT, the adjacent PMA sends a repeating 16-bit pattern, hexadecimal 0xFF00, to the PMD, which the PMD transmits. When tx_mode is ALERT, the transmitter equalizer taps are set to the preset state specified in 85.8.3.3.1. When tx_mode is QUIET, the transmitter is disabled as specified in 85.7.6. For all other states of tx_mode, the driver coefficients are restored to their states resolved during training.

85.7.4 Global PMD signal detect function

Insert the following at the end of the first paragraph:

When the PHY supports the optional EEE capability with deep sleep mode, PMD_SIGNAL.indication is also used to indicate when the ALERT signal is detected, which corresponds to the beginning of a refresh or a wake.

Insert the following at the beginning of the second and third paragraphs:

When the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA

Insert the following at the end of the third paragraph:

When the PHY supports the EEE capability with deep sleep mode, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that corresponds to an ALERT transmission (see 85.7.2) from the link partner. While rx_mode = QUIET, SIGNAL_DETECT shall be held at FAIL as long as the signal at the receiver input corresponds to a QUIET tx_mode (see 85.7.6) of the link partner.

85.7.6 Global PMD transmit disable function

Change 85.7.6 for the EEE transmit_disable:

The Global_PMD_transmit_disable function is mandatory if EEE with the deep sleep mode option is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 85–5.
b) If a PMD_fault (85.7.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 85.7.8, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 72.7.1.4. The PMD_transmit_disable

function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 72.7.1.4.

85.8.3 Transmitter characteristics

Insert the following row immediately above the row for Amplitude peak-to-peak (max) in Table 85-5 in 85.8.3:

Table 85–5—Transmitter characteristics at TP2 summary

Parameter	Subclause reference	Value	Units
Common-mode voltage deviation (max) during LPI	72.7.1.4	150	mV

85.13 Protocol implementation conformance statement (PICS) proforma for Clause 85, Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10[9]

Insert the following row at the end of the table in 85.13.3:

85.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI with the deep sleep mode option	85.2		O	Yes [ ] No [ ]

85.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and base-band medium, type 40GBASE-CR4 and 100GBASE-CR10

Insert the following rows at the end of the table in 85.13.4.1:

85.13.4.1 PMD functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
PF19	Signal detect during LPI	85.7.4	Detect signal energy during LPI	LPI:M	Yes [ ] No [ ]
PF20	Signal detect for EEE	85.7.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes [ ] No [ ]
PF21	Transmit disable during LPI	85.7.6	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] No [ ]

Insert the following rows at the end of the table in 85.13.4.3:

[9] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

85.13.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DS6	Output Amplitude LPI voltage	85.7.6	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] No [ ]
DS7	Output Amplitude ON voltage	85.7.6	Greater than 90% of previous level within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] No [ ]

91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

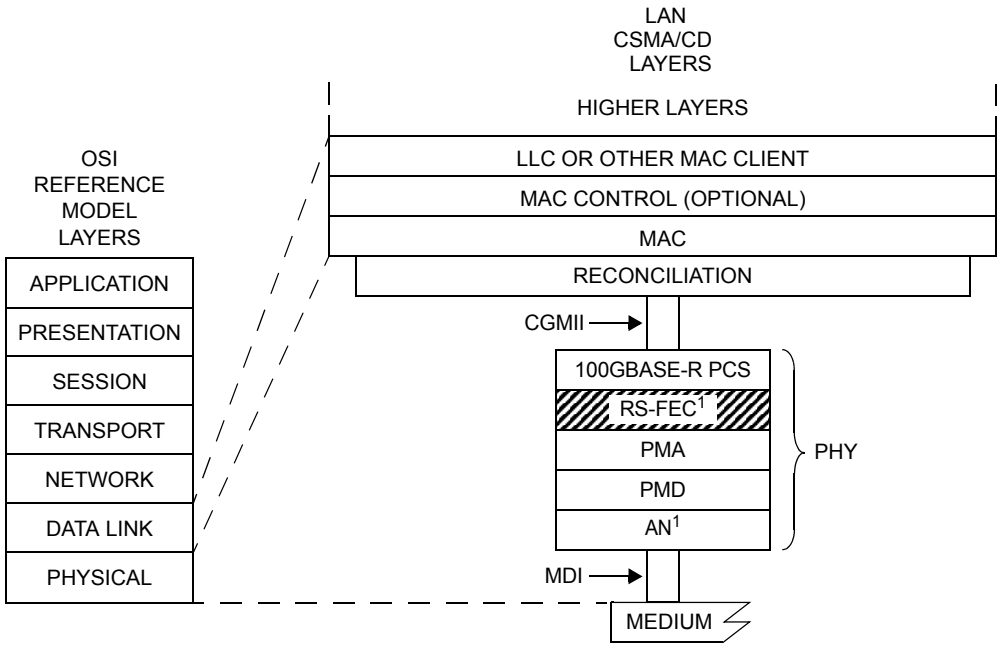
91.1 Overview

91.1.1 Scope

This clause specifies a Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs.

91.1.2 Position of RS-FEC in the 100GBASE-R sublayers

Figure 91–1 shows the relationship of the RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.



AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 91–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

91.2 FEC service interface

This subclause specifies the services provided by the RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (refer to Annex 83A) in which case a PMA will be the client of the FEC service interface.

The FEC service interface is an instance of the inter-sublayer service interface defined in 80.3. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication

The RS-FEC operates on twenty parallel bit streams, hence $i = 0$ to 19. The PCS (or PMA) continuously sends twenty parallel bit streams to the RS-FEC, one per lane, each at a nominal signaling rate of 5.15625 GBd. The RS-FEC continuously sends twenty parallel bit streams to the PCS (or PMA), one per lane, each at a nominal signaling rate of 5.15625 GBd

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to false. When SIGNAL_OK is FAIL, the rx_bit parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

If the optional EEE capability is supported, then the FEC service interface includes three additional primitives as follows:

FEC:IS_TX_MODE.request
FEC:IS_RX_MODE.request
FEC:IS_ENERGY_DETECT.indication

91.3 PMA compatibility

The RS-FEC sublayer requires that the PMA service interface consist of exactly four upstream lanes and exactly four downstream lanes. Therefore, the RS-FEC sublayer may be a client of the PMA sublayer defined in Clause 83 when the PMA service interface width, *p*, is set to 4. The RS-FEC sublayer may also be a client of the PMA sublayer defined in Clause 94.

In addition, all PMA service interfaces between the RS-FEC sublayer and the PMD sublayer are required to consist of four or fewer upstream lanes and four or fewer downstream lanes. A consequence of this constraint is that a physical instantiation of the 10-lane PMA service interface (CAUI) may not be used below the RS-FEC sublayer.

91.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 40960 bit times (80 pause_quanta or 409.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

91.5 Functions within the RS-FEC sublayer

91.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 91–2.

91.5.2 Transmit function

91.5.2.1 Lane block synchronization

The RS-FEC transmit function forms 20 bit streams by concatenating the bits from each of the 20 FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–10.

91.5.2.2 Alignment lock and deskew

Once the RS-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–11. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all 20 lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–12. The RS-FEC transmit function shall support a maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps. Skew and Skew Variation are defined in 80.5.

91.5.2.3 Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The RS-FEC transmit function shall order the PCS lanes according to the PCS lane number.

91.5.2.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors will result in am_lock being set to false for a given PCS lane, but until that happens it is sufficient to remove the block in the alignment marker position.

For the optional EEE capability, transitions between normal alignment markers and Rapid Alignment markers result in changes in relative position and frequency of alignment markers. These transitions are detected by the Transmit LPI state diagram (see Figure 91–10) and this information is used by the alignment marker removal function to determine which 66-bit blocks are to be removed.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (refer to 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.249) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The incoming bit error ratio can be estimated by dividing the BIP block error ratio by a factor of 1081344.

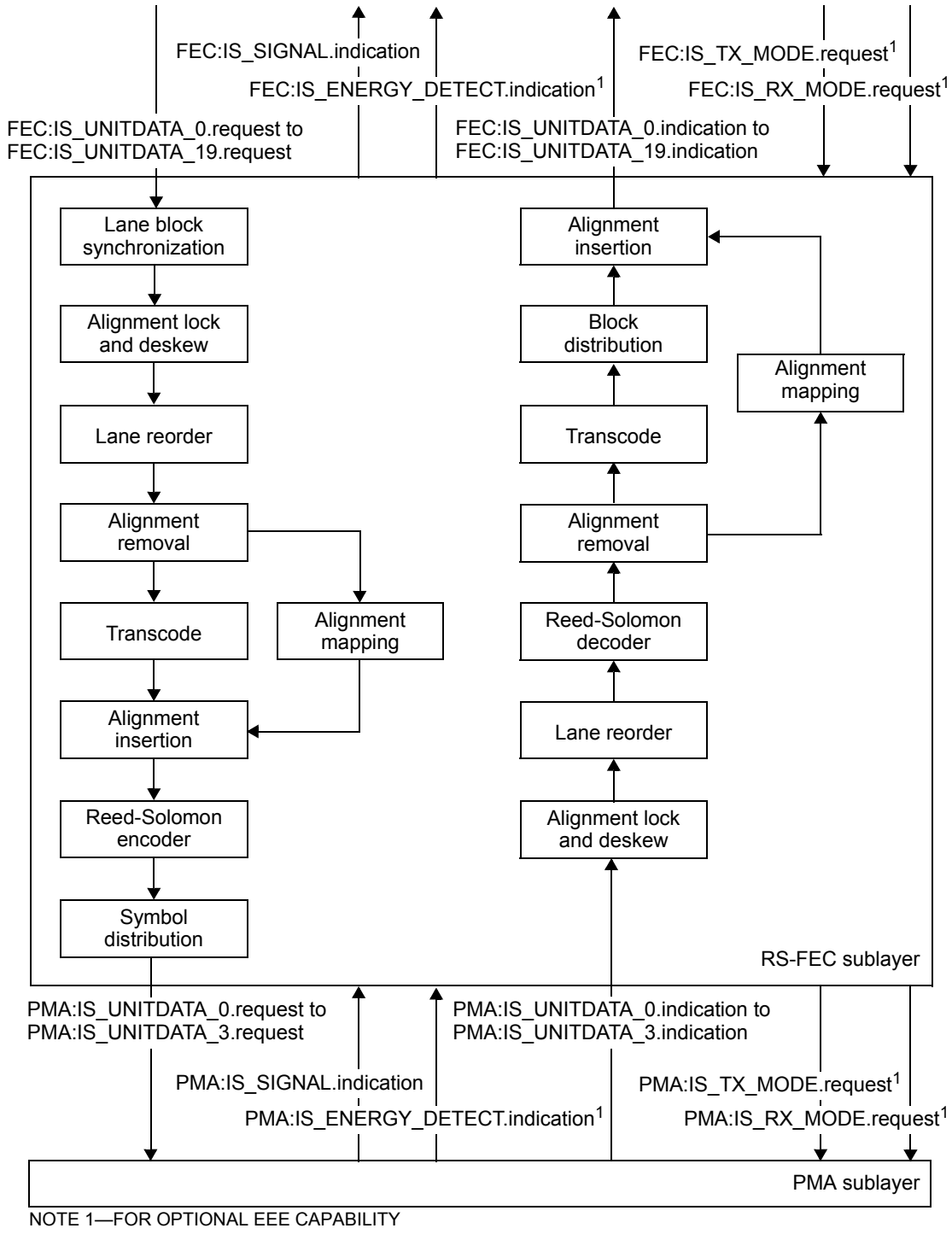


Figure 91–2—Functional block diagram

91.5.2.5 64B/66B to 256B/257B transcoder

The transcoder constructs a 257-bit block, tx_scrambled<256:0>, from a group of four 66-bit blocks, tx_coded_*j*<65:0> where *j*=0 to 3. For each group of four 66-bit blocks, *j*=3 corresponds to the most recently received block. Bit 0 in each 66-bit block is the first bit received and corresponds to the first bit of the synchronization header.

If for all *j*=0 to 3, tx_coded_*j*<0>=0 and tx_coded_*j*<1>=1, tx_xcoded<256:0> shall be constructed as follows.

a) tx_xcoded<0> = 1
b) tx_xcoded<(64*j*+64):(64*j*+1)> = tx_coded_*j*<65:2> for *j*=0 to 3

If for all *j*=0 to 3, tx_coded_*j*<0> ≠ tx_coded_*j*<1> (valid synchronization header) and for any *j*=0 to 3, tx_coded_*j*<0>=1 and tx_coded_*j*<1>=0, tx_xcoded<256:0> shall be constructed as follows.

a) tx_xcoded<0> = 0
b) tx_xcoded<*j*+1> = tx_coded_*j*<1> for *j*=0 to 3
c) Let *c* be the smallest value of *j* such that tx_coded_*c*<0>=1. In other words, tx_coded_*c* is the first 66-bit control block that was received in the current group of four blocks.
d) Let tx_payloads<(64*j*+63):64*j*> = tx_coded_*j*<65:2> for *j*=0 to 3
e) Omit tx_coded_*c*<9:6>, which is the second nibble (based on transmission order) of the block type field for tx_coded_*c,* from tx_xcoded per the following expressions.
   tx_xcoded<(64*c*+8):5> = tx_payloads<(64*c*+3):0>
   tx_xcoded<256:(64*c*+9)> = tx_payloads<255:(64*c*+8)>

If for any *j*=0 to 3, tx_coded_*j*<0> = tx_coded_*j*<1> (invalid synchronization header), tx_xcoded<256:0> shall be constructed as follows.

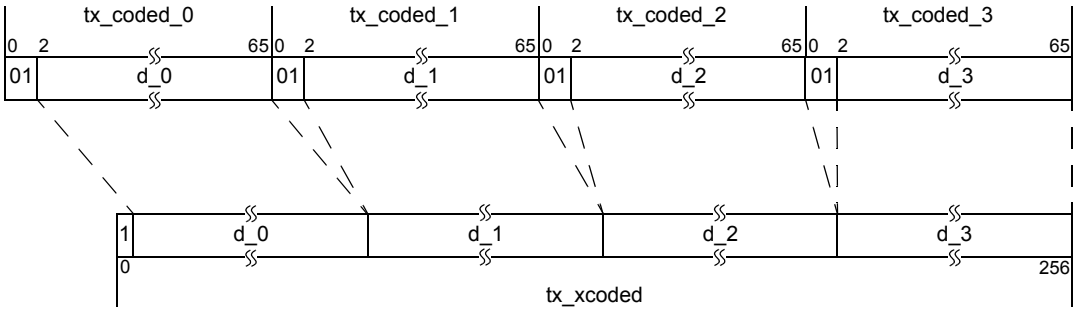
a) tx_xcoded<0> = 0
b) tx_xcoded<*j*+1> = 1 for *j*=0 to 3
c) Let tx_payloads<(64*j*+63):64*j*> = tx_coded_*j*<65:2> for *j*=0 to 3
d) Omit the second nibble (based on transmission order) of tx_coded_0 per the following expressions.
   tx_xcoded<8:5> = tx_payloads<3:0>
   tx_xcoded<256:9> = tx_payloads<255:8>

Several examples of the construction of tx_xcoded<256:0> are shown in Figure 91–3.

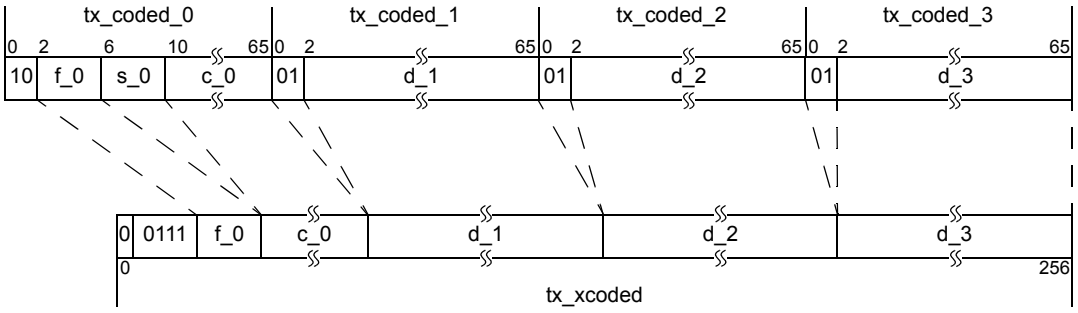
Finally, scramble the first 5 bits, based on transmission order, of tx_xcoded<256:0> to yield tx_scrambled<256:0> as follows.

a) Set tx_scrambled<4:0> to the result of the bit-wise exclusive-OR of the tx_xcoded<4:0> and tx_xcoded<12:8>.
b) Set tx_scrambled<256:5> to tx_xcoded<256:5>

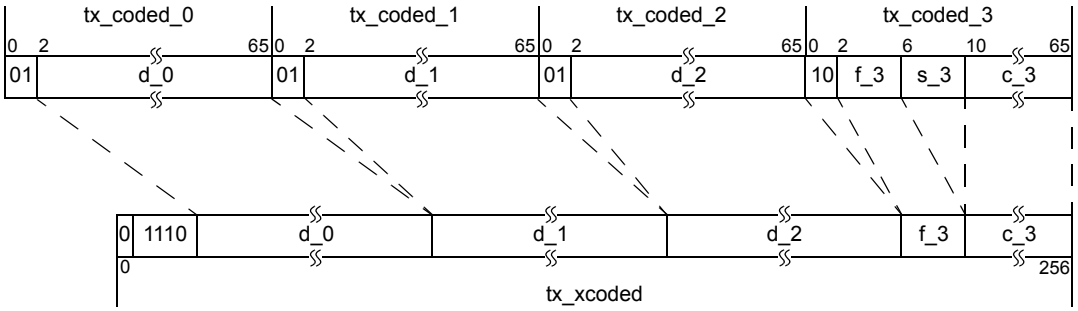
For each 257-bit block, bit 0 shall be the first bit transmitted.



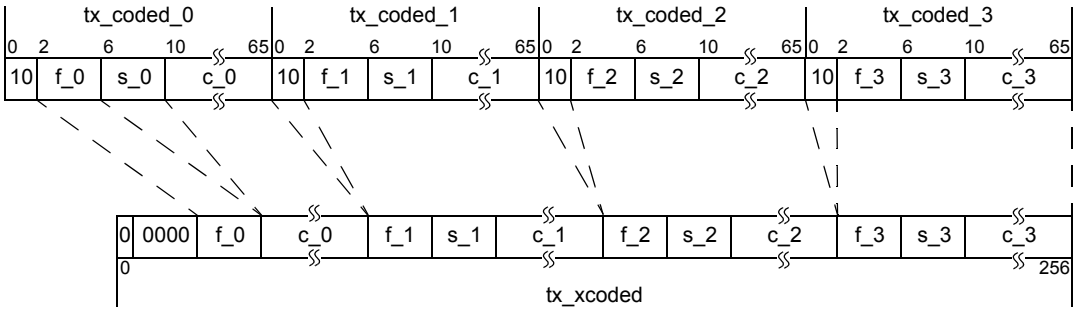
Example 1: All data blocks



Example 2: Control block followed by three data blocks



Example 3: Three data blocks followed by a control block



Example 4: All control blocks

Figure 91–3—Examples of the construction of tx_xcoded

91.5.2.6 Alignment marker mapping and insertion

The alignment markers that were removed per 91.5.2.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 91.5.2.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g. DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization. The RS-FEC receive function uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface, compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of twenty aligned and reordered alignment markers. Let am_tx_*x*<65:0> be the alignment marker for PCS lane *x*, *x*=0 to 19, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_txmapped<1284:0> in a manner that yields the same result as the process defined below.

For *x*=4 to 15, discard the synchronization headers per the following expression.

amp_tx_*x*<63:0> = am_tx_*x*<65:2>

For *x*=0 to 3, amp_tx_*x*<63:0> is constructed as follows.

a) amp_tx_*x*<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–2 for PCS lane number 0. If am_tx_*x* corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–9b).
b) amp_tx_*x*<31:24> = am_tx_*x*<33:26>
c) amp_tx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–2 for PCS lane number 0. If am_tx_*x* corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–9b).
d) amp_tx_*x*<63:56> = am_tx_*x*<65:58>

For *x*=16 to 19, amp_tx_*x*<63:0> is computed using the same procedure except the M_0 through M_6 values for PCS lane number 16 are used.

This process replaces the fixed bytes of the alignment markers corresponding to PCS lanes 1, 2, and 3 with the fixed bytes for the alignment marker corresponding to PCS lane 0. Similarly, it replaces fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16. The variable bytes BIP or CD are unchanged. This process simplifies receiver synchronization since the receiver only needs to search for the fixed bytes corresponding to PCS lane 0 on each FEC lane. When the optional EEE deep sleep capability is supported, the receiver only needs to search for the fixed bytes corresponding to PCS lanes 0 and 16.

Construct a matrix of 4 rows and 320 columns, am_txpayloads, as shown in Figure 91–4. Given *i*=0 to 3, *j*=0 to 4, and *x*=*i*+4*j*, the matrix is derived per the following expression.

am_txpayloads<*i*, (64*j*+63):64*j*> = amp_tx_*x*<63:0>

Given *i*=0 to 3, *k*=0 to 31, and *y*=*i*+4*k*, am_txmapped may then be derived from am_txpayloads per the following expression.

am_txmapped<(10*y*+9):10*y*> = am_txpayloads<*i*, (10*k*+9):10*k*>

A 5-bit pad is appended to the mapped alignment markers to yield the equivalent of five 257-bit blocks. The pad bits, am_txmapped<1284:1280>, shall be set to the binary values 00101 and 11010 (the leftmost bit is

assigned to the highest bit index) in an alternating pattern. In other words, if a pad value of 00101 is used for the current iteration of the mapping function, a value of 11010 will be used in the next iteration and vice versa.

The result of the alignment marker mapping function is a deterministic mapping between alignment marker payloads and FEC lanes. The alignment marker payloads corresponding to PCS lanes 0, 4, 8, 12, and 16 are transmitted on FEC lane 0, the alignment marker payloads corresponding to PCS lanes 0, 5, 9, 13, and 16 are transmitted on FEC lane 1, and so on (see Figure 91–4).

As a result of this process, the BIP_3 and BIP_7 fields from normal alignment markers are carried across the link protected by FEC. It should be noted that these fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, i.e. following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

One group of aligned and reordered alignment markers are mapped every 20 × 16384 66-bit blocks. This corresponds to 4096 Reed-Solomon codewords (refer to 91.5.2.7). The mapped alignment markers, am_txmapped<1284:0> shall be inserted as the first 1285 message bits to be transmitted from every 4096th codeword.

For the optional EEE capability, when tx_lpi_active is true, one group of Rapid Alignment Markers (see 82.2.8a) are mapped every 20 × 8 66-bit blocks. This corresponds to 2 Reed-Solomon codewords. The mapped Rapid Alignment Markers, am_txmapped<1284:0> shall be inserted as the first 1285 message bits to be transmitted from every other codeword.

The first 257-bit block inserted after am_txmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane.

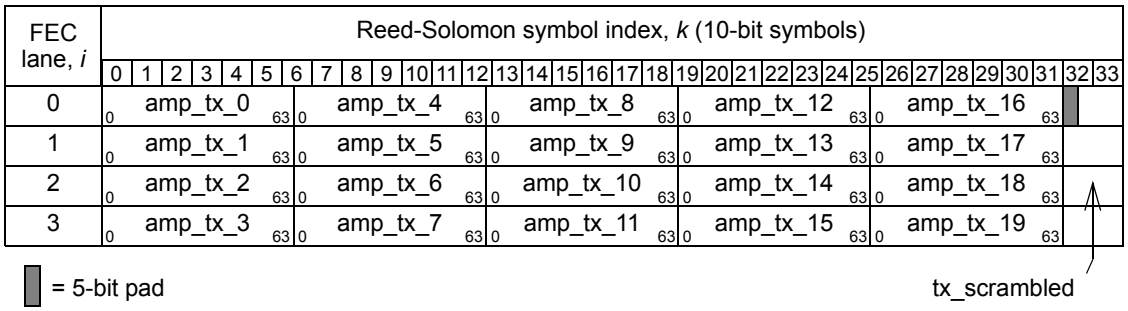


Figure 91–4—Alignment marker mapping to FEC lanes

91.5.2.7 Reed-Solomon encoder

The RS-FEC sublayer employs a Reed-Solomon code operating over the Galois Field GF(2^{10}) where the symbol size is 10 bits. The encoder processes k message symbols to generate $2t$ parity symbols which are then appended to the message to produce a codeword of $n=k+2t$ symbols. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(n,k).

When used to form a 100GBASE-CR4 or 100GBASE-KR4 PHY, the RS-FEC sublayer shall implement RS(528,514). When used to form a 100GBASE-KP4 PHY, the RS-FEC sublayer shall implement RS(544,514). Each k-symbol message corresponds to twenty 257-bit blocks produced by the transcoder. Each code is based on the generating polynomial given by Equation (91–1).

$$g(x) = \prod_{j=0}^{2t-1}(x-\alpha^j) = g_{2t}x^{2t} + g_{2t-1}x^{2t-1} + \ldots + g_1 x + g_0 \quad (91\text{–}1)$$

In Equation (91–1), α is a primitive element of the finite field defined by the polynomial $x^{10}+x^3+1$.

Equation (91–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0.

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1 x^{2t+1} + m_0 x^{2t} \quad (91\text{–}2)$$

Each message symbol m_i is the bit vector $(m_{i,9}, m_{i,8}, \ldots, m_{i,1}, m_{i,0})$ which is identified with the element $m_{i,9}\alpha^9 + m_{i,8}\alpha^8 + \ldots + m_{i,1}\alpha + m_{i,0}$ of the finite field. The message symbols are composed of the bits of the transcoded blocks tx_scrambled (including a mapped group of alignment markers when appropriate) such that bit 0 of the first transcoded block in the message (or am_txmapped<0>) is bit 0 of m_{k-1} and bit 256 of the last transcoded block in the message is bit 9 of m_0. The first symbol input to the encoder is m_{k-1}.

Equation (91–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_{2t-1} to p_0.

$$p(x) = p_{2t-1}x^{2t-1} + p_{2t-2}x^{2t-2} + \ldots + p_1 x + p_0 \quad (91\text{–}3)$$

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This may be computed using the shift register implementation illustrated in Figure 91–5. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{n-1} = m_{k-1}$, is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$, is transmitted last. The first bit transmitted from each symbol is bit 0.

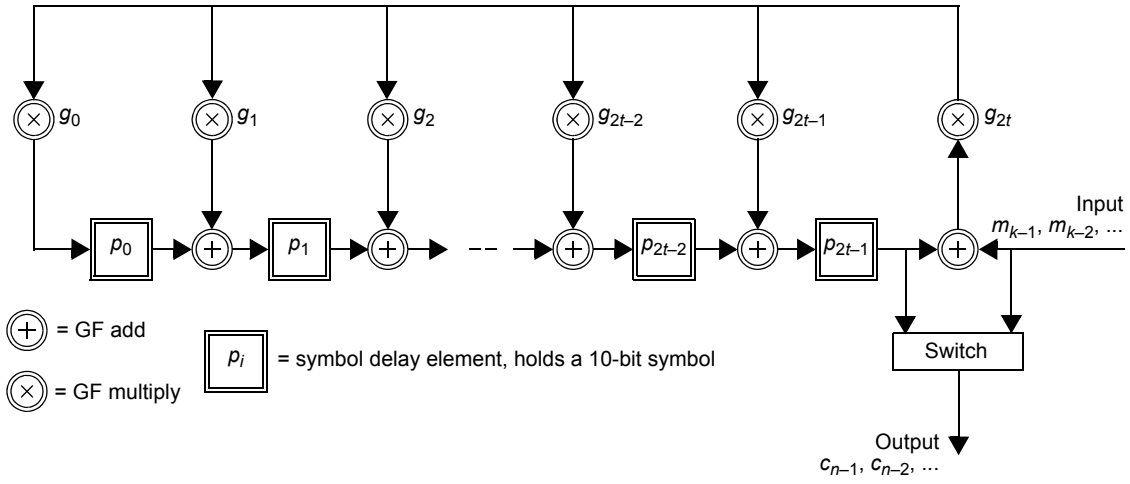


Figure 91–5—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for each code are presented in Table 91–1. Example codewords for each code are provided in Annex 91A.

Table 91–1—Coefficients of the generator polynomial g_i (decimal)

i	RS(528,514)	RS(544,514)	*i*	RS(528,514)	RS(544,514)	*i*	RS(528,514)	RS(544,514)
0	432	523	11	701	883	22		565
1	290	834	12	6	503	23		108
2	945	128	13	904	942	24		1
3	265	158	14	1	385	25		552
4	592	185	15		495	26		230
5	391	127	16		720	27		187
6	614	392	17		94	28		552
7	900	193	18		132	29		575
8	925	610	19		593	30		1
9	656	788	20		249			
10	32	361	21		282			

91.5.2.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it shall be distributed to 4 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane. The distribution process is shown in Figure 91–6.

When used to form a 100GBASE-KP4 PHY, the PMA:IS_UNITDATA_*i*.request primitive is defined to include an additional parameter (refer to 94.2.1.1.1). At the beginning of an FEC codeword, the parameter start=TRUE is asserted for the first bit of the first four symbols of the codeword transferred across the four primitives. Otherwise the parameter start is set to FALSE.

91.5.2.9 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 91–6.

91.5.3 Receive function

91.5.3.1 Alignment lock and deskew

The RS-FEC receive function forms 4 bit streams by concatenating the bits from each of the 4 PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8.

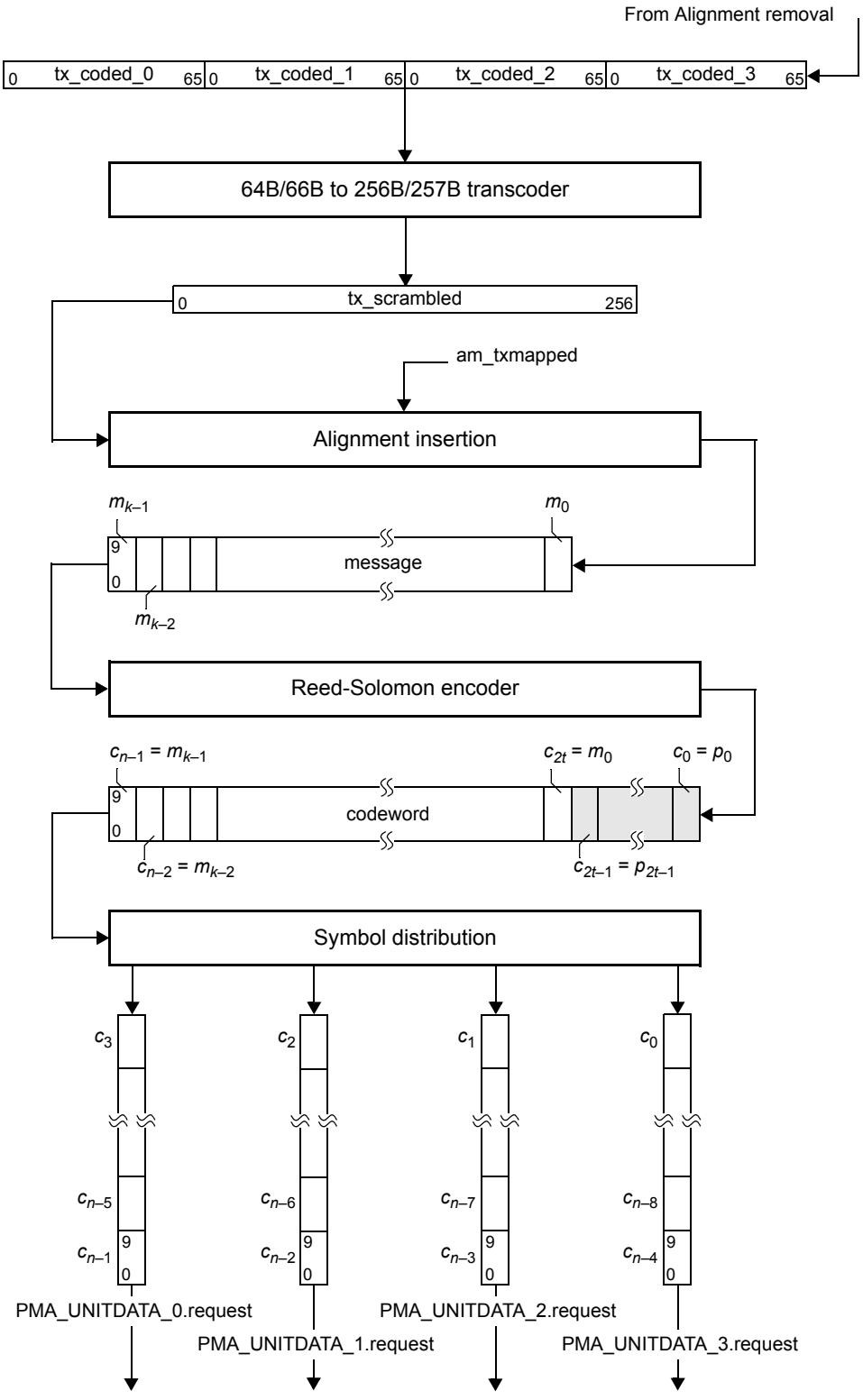


Figure 91–6—Transmit bit ordering

After alignment marker lock is achieved on all 4 lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

The 100GBASE-KP4 PMA transmit function (refer to 94.2.2) inserts PMA-specific overhead that is aligned with the start of a Reed-Solomon codeword. The 100GBASE-KP4 PMA receive function (refer to 94.2.3) synchronizes to this overhead and indicates the first bit of each of the first four symbols in a codeword by setting the PMA:IS_UNITDATA_*i*.indication parameter start=TRUE (see 94.2.1.2).

91.5.3.2 Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 91.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

91.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols. The message symbols correspond to 20 transcoded blocks rx_scrambled.

When used to form a 100GBASE-CR4 or 100GBASE-KR4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=7 symbol errors in a codeword. When used to form a 100GBASE-KP4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_correction_ability variable (see 91.6.3). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 91.6.1).

NOTE—The PHY may rely on the error correction capability of the RS-FEC sublayer to achieve its performance objectives. It is recommended that acceptable performance of the underlying link is verified before error correction is bypassed.

The Reed-Solomon decoder indicates errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled), it shall ensure that, for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword is set to 11. This will cause the PCS to discard all frames 64 bytes and larger that are fully or partially within the codeword.

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 91.6.4). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 91.6.2).

When FEC_bypass_correction_enable is asserted, the decoder shall not bypass error indication and the value of FEC_bypass_indication_enable has no effect.

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet will not be detected. The Reed-Solomon decoder counts the number of symbol errors detected on all four FEC lanes in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds *K*, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS will set hi_ber=true which will inhibit the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber will cause Auto-Negotation to restart.

For the optional EEE capability, the error monitor employed when FEC_bypass_indication_enable is asserted shall be disabled when rx_lpi_active=true. The next block of 8192 codewords considered by the error monitor shall begin on the codeword boundary following the transition of rx_lpi_active from true to false.

When the RS-FEC sublayer is used to form a 100GBASE-CR4 or 100GBASE-KR4 PHY, the symbol error threshold shall be *K*=417. When the RS-FEC sublayer used to form a 100GBASE-KP4 PHY, the symbol error threshold shall be *K*=6380.

91.5.3.4 Alignment marker removal

The first 1285 message bits in every 4096th codeword is the vector am_rxmapped<1284:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (refer to 91.5.3.1).

For the optional EEE capability, transitions between normal alignment markers and Rapid Alignment markers result in changes in the relative position and frequency of am_rxmapped<1284:0>. These transitions are detected by the Receive LPI state diagram (see Figure 91–11) and this information is used by the alignment marker removal function to determine which bits are to be removed. When rx_lpi_active is true, the first 1285 message bits in every other codeword is the vector am_rxmapped<1284:0>.

The vector am_rxmapped shall be removed prior to transcoding.

91.5.3.5 256B/257B to 64B/66B transcoder

The transcoder extracts a group of four 66-bit blocks, rx_coded_*j*<65:0> where *j*=0 to 3, from each 257-bit block rx_scrambled<256:0>. Bit 0 of the 257-bit block is the first bit received.

First, descramble the first 5 bits, based on reception order, of rx_scrambled<256:0> to yield rx_xcoded<256:0> as follows.

a) Set rx_xcoded<4:0> to the result of the bit-wise exclusive-OR of the rx_scrambled<4:0> and rx_scrambled<12:8>.
b) Set rx_xcoded<256:5> to rx_scrambled<256:5>.

If rx_xcoded<0> is 1, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a) rx_coded_*j*<65:2> = rx_xcoded<(64*j*+64):(64*j*+1)> for *j*=0 to 3
b) rx_coded_*j*<0>=0 and rx_coded_*j*<1>=1 for all *j*=0 to 3

If rx_xcoded<0> is 0 and any rx_xcoded<*j*+1>=1 for *j*=0 to 3, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a) Let *c* be the smallest value of *j* such that rx_xcoded<*j*+1>=0. In other words, rx_coded_*c* will be the first 66-bit control block in the resulting group of four blocks.
b) Let rx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions.
rx_payloads<(64*c*+3):0> = rx_xcoded<(64*c*+8):5>
rx_payloads<(64*c*+7):(64*c*+4)> = 0000 (an arbitrary value that is later replaced by s_*c*)
rx_payloads<255:(64*c*+8)> = rx_xcoded<256:(64*c*+9)>
c) rx_coded_*j*<65:2> = rx_payloads<(64*j*+63):64*j*> for *j*=0 to 3
d) Let f_*c*<3:0> = rx_coded_*c*<5:2> be the scrambled first nibble (based on transmission order) of the block type field for rx_coded_*c*.
e) Descramble f_*c*<3:0> to yield g<3:0> per the following expression where "^" denotes the exclusive-OR operation. When *c*=0, rx_coded_(*c*–1) corresponds to rx_coded_3 from the previous 257-bit block.
g<*i*> = f_*c*<*i*> ^ rx_coded_(*c*–1)<*i*+8> ^ rx_coded_(*c*–1)<*i*+27> for *i*=0 to 3
f) The block type field may be uniquely identified by either its most or least significant nibble. Since g<3:0> is the least significant nibble of the block type field (per the transmission order), derive h<3:0> by cross-referencing to g<3:0> using Figure 82–5. For example, if g<3:0> is 0xE then h<3:0> is 0x1. If no match to g<3:0> is found, h<3:0> is set to 0000.
g) if rx_xcoded<*j*+1>=0, rx_coded_*j*<0>=1 and rx_coded_*j*<1>=0 for *j*=0 to 3
h) if rx_xcoded<*j*+1>=1, rx_coded_*j*<0>=0 and rx_coded_*j*<1>=1 for *j*=0 to 3
i) if h<3:0> = 0000, rx_coded_*c*<1>=1 (invalidate synchronization header)

If rx_xcoded<0> is 0 and all rx_xcoded<*j*+1>=1 for *j*=0 to 3, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a) Set *c* = 0 and h<3:0> = 0000.
b) Let rx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions.
rx_payloads<(64*c*+3):0> = rx_xcoded<(64*c*+8):5>
rx_payloads<(64*c*+7):(64*c*+4)> = 0000 (an arbitrary value that is later replaced by s_*c*)
rx_payloads<255:(64*c*+8)> = rx_xcoded<256:(64*c*+9)>
c) rx_coded_*j*<65:2> = rx_payloads<(64*j*+63):(64*j*)> for *j*=0 to 3
d) rx_coded_*j*<0>=0 and rx_coded_*j*<1>=0 for *j*=0 and 2
e) rx_coded_*j*<0>=1 and rx_coded_*j*<1>=1 for *j*=1 and 3

If rx_xcoded<0> is 0, scramble h<3:0> to yield s_*c*<3:0> and assign it to rx_coded_*c* per the following expressions.

a) s_*c*<*i*> = h<*i*> ^ rx_coded_(*c*–1)<*i*+12> ^ rx_coded_(*c*–1)<*i*+31> for *i*=0 to 3
b) rx_coded_*c*<9:6> = s_*c*<3:0>

The 66-bit blocks are transmitted in order from *j*=0 to 3. Bit 0 of each block is the first bit transmitted.

91.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to multiple PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

91.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of lane reorder function (refer to 91.5.3.2) to derive the PCS lane alignment markers, am_rx_*x*<65:0> for *x*=0 to 19, from am_rxmapped<1284:0> (refer to 91.5.3.4).

The alignment markers shall be derived from am_rxmapped<1284:0> in a manner that yields the same result as the process defined below.

Given i=0 to 3, k=0 to 31, and $y=i+4k$, am_rxpayloads may be derived from am_rxmapped per the following expression.

am_rxpayloads<i, (10k+9):10k> = am_rxmapped<(10y+9):10y>

The 5-bit pad am_rxmapped<1284:1280> is ignored. Given i=0 to 3, j=0 to 4, and $x=i+4j$, amp_rx_x may be derived from am_rxpayloads by the following expression.

amp_rx_x<63:0> = am_rxpayloads<i, (64j+63):64j>

For x=0 to 19, am_rx_x<65:0> is constructed as follows.

a) am_rx_x<0>=1 and am_rx_x<1>=0.
b) am_rx_x<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–2 for PCS lane number x. If amp_rx_x corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–9b).
c) am_rx_x<33:26> = amp_rx_x<31:24>.
d) am_rx_x<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–2 for PCS lane number x. If amp_rx_x corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–9b).
e) am_rx_x<65:58> = amp_rx_x<63:56>.

One vector is mapped to 20 alignment markers every 4096 Reed-Solomon codewords (see 91.5.3.4). The alignment markers are simultaneously transmitted on the 20 PCS lanes after every 16383rd column of 20 66-bit blocks.

For the optional EEE capability, when rx_lpi_active is true, one vector is mapped to 20 Rapid Alignment Markers every 2 Reed-Solomon codewords. The Rapid Alignment Markers are simultaneously transmitted on the 20 PCS lanes after every 7th column of 20 66-bit blocks.

The alignment markers am_rx_0 to am_rx_3 shall be inserted so that they are immediately followed by rx_coded_0 to rx_coded_3 respectively as derived from the first 257-bit block following am_rxmapped. Similarly am_rx_4 to am_rx_7 are followed by the 66-bit blocks corresponding to the second 257-bit block following am_rxmapped, and so on.

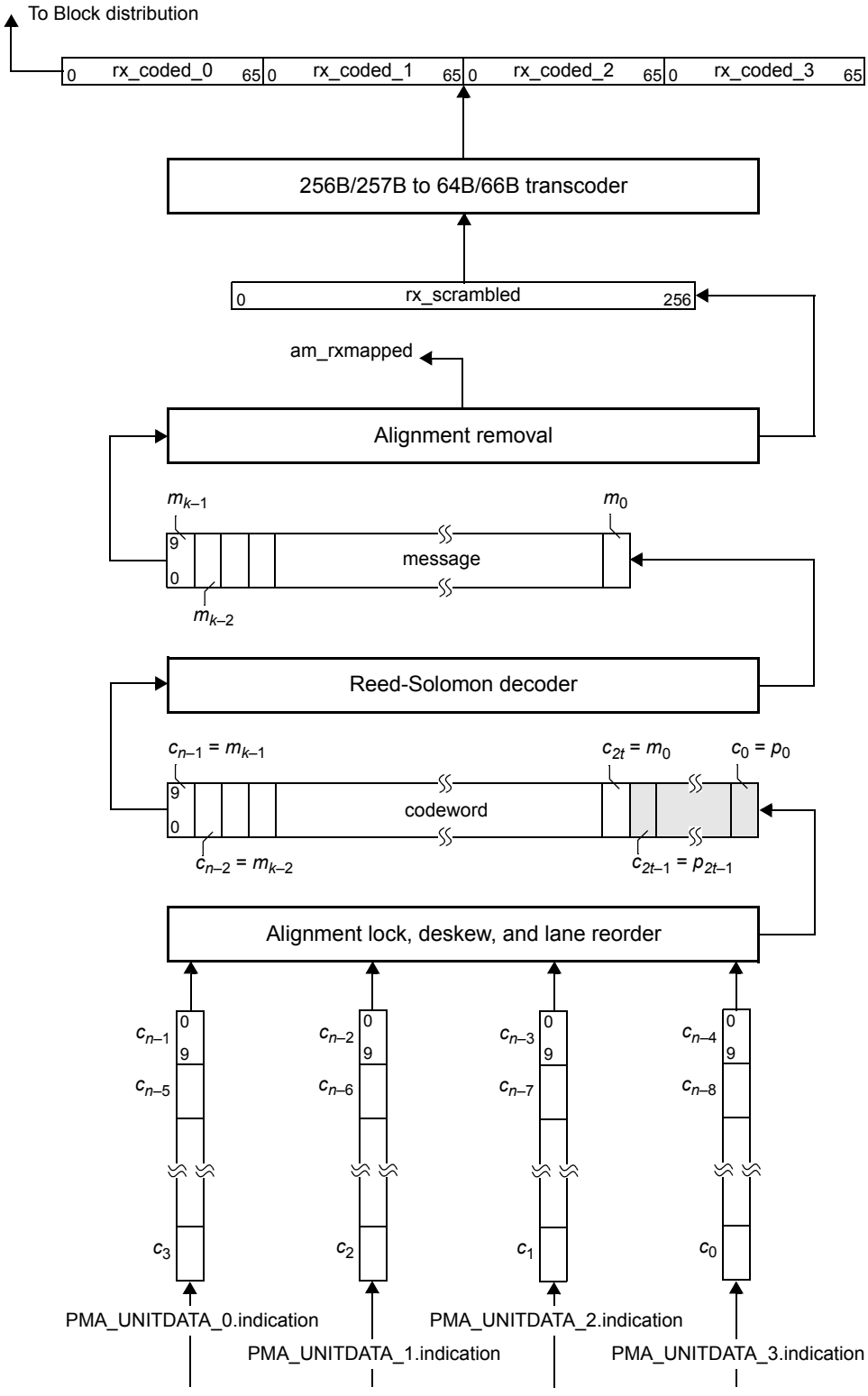


Figure 91–7—Receive bit ordering

91.5.3.8 Receive bit ordering

The receive bit ordering is illustrated in Figure 91–7. This illustration shows the case where the FEC lanes appear across the PMA:IS_UNITDATA_*i*.indication primitives in the correct order.

91.5.4 Detailed functions and state diagrams

91.5.4.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

91.5.4.2 State variables

91.5.4.2.1 Variables

rx_align_status
: Boolean variable that is set by the alignment lock and deskew function (see 91.5.2.2).

all_locked
: A Boolean variable that is set to true when amps_lock<*x*> is true for all *x* and is set to false when amps_lock<*x*> is false for any *x*.

amp_counter_done
: Boolean variable that indicates that amp_counter has reached its terminal count.

amp_match
: Boolean variable that holds the output of the function AMP_COMPARE.

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 91.5.2.6, consists of 48 known bits and 16 variable bits (the BIP_3 or CD_3 field and its complement BIP_7 or CD_7, see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. For the normal mode of operation, each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0. For the optional EEE capability, each FEC lane also compares the candidate block to the alignment marker payload for PCS lane 16 when rx_lpi_active is true.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given FEC lane where *x* = 0:3.

current_pcsl
: A variable that holds the PCS lane number corresponding to the current alignment marker payload that is recognized on a given FEC lane. It is compared to the variable first_pscl to confirm that the location of the alignment marker payload sequence has been detected.

cw_bad
: A Boolean variable that is set to true if the Reed-Solomon decoder (see 91.5.3.3) fails to correct the current FEC codeword and is set to false otherwise.

deskew_done
: A Boolean variable that is set to true when fec_enable_deskew is set to true and the deskew process is completed. Otherwise, this variable is set to false.

fec_align_status
: A variable set by the FEC alignment process to reflect the status of FEC lane-to-lane alignment. Set to true when all lanes are synchronized and aligned and set to false when the deskew process is not complete.

fec_alignment_valid
: Boolean variable that is set to true if all FEC lanes are aligned. FEC lanes are considered to be aligned when amps_lock<*x*> is true for all *x*, each FEC lane is locked to a unique alignment marker payload sequence (see 91.5.2.6), and the FEC lanes are deskewed. Otherwise, this variable is set to false.

fec_enable_deskew
: A Boolean variable that enables and disables the deskew process. Received bits may be discarded whenever deskew is enabled. It is set to true when deskew is enabled and it is set to false when deskew is disabled.

fec_lane
: A variable that holds the FEC lane number (0 to 3) that is derived from the alignment marker payload sequence received on lane *x* of the PMA service interface and the mapping defined in 91.5.2.6 when amps_lock<*x*> = true.

first_pcsl
: A variable that holds the PCS lane number that corresponds to the first alignment marker payload that is recognized on a given FEC lane. It is compared to the PCS lane number corresponding to the second alignment marker payload that is tested.

reset
: Boolean variable that controls the resetting of the RS-FEC sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the RS-FEC sublayer into low-power mode.

restart_lock
: Boolean variable that is set by the FEC alignment process to reset the synchronization process on all FEC lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

signal_ok
: Boolean variable that is set based on the most recently received value of *inst*:IS_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is set to true when the SLIP requested by the synchronization state diagram has been completed indicating that the next candidate 64-bit block position can be tested.

test_amp
: Boolean variable this is set to true when a candidate block position is available for testing and false when the FIND_1ST state is entered.

test_cw
: Boolean variable that is set to true when a new FEC codeword is available for decoding and is set to false when the TEST_CW state is entered.

The following variables are only used for the optional EEE capability. If this capability is not supported, the values of tx_lpi_active and rx_lpi_active are set to false.

1st_ram_counter_done
: Boolean variable that indicates that 1st_ram_counter has reached its terminal count.

1st_ramps_counter_done
: Boolean variable that indicates that 1st_ramps_counter has reached its terminal count.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state diagrams. This variable is set to true when the local PCS is configured to use the Fast Wake mechanism and set to false otherwise.

ram_counter_done
: Boolean variable that indicates that ram_counter has reached its terminal count.

ram_valid
: Boolean variable that is set to true when the 66-bit blocks concurrently received on at least 2 PCS lanes are valid Rapid Alignment Markers with identical values in the Count Down fields and is set to false otherwise.

ram_valid_prev
: Boolean variable that holds the value of ram_valid from the previous expected Rapid Alignment Marker position.

ramps_counter_done
: Boolean variable that indicates that ramps_counter has reached its terminal count.

ramps_valid
: Boolean variable that is set to true when the 66-bit blocks concurrently received on at least 2 FEC lanes are valid Rapid Alignment Marker payloads with identical values in the Count Down fields and is set to false otherwise.

ramps_valid_prev
: Boolean variable that holds that value of ramps_valid from the previous expected Rapid Alignment Marker payload position.

rx_down_count
: The value that results from the bit-wise exclusive-OR of the Count Down (CD_3) byte and the M_0 byte of the current Rapid Alignment Marker payload (see 82.2.8a).

rx_lpi_active
: A Boolean variable that is set to true when the RS-FEC sublayer infers that the Low Power Idle is being received from the link partner and is set to false otherwise.

rx_quiet_timer_done
: A Boolean variable that indicates that rx_quiet_timer has reached its terminal count.

tx_down_count
: The value that results from the bit-wise exclusive-OR of the Count Down (CD_3) byte and the M_0 byte of the current Rapid Alignment Marker (see 82.2.8a).

tx_lpi_active
: A Boolean variable that is set to true when the RS-FEC sublayer infers that the local PCS is transmitting Low Power Idle and is set to false otherwise.

tx_quiet_timer_done
: Boolean variable that indicates that tx_quiet_timer has reached its terminal count.

91.5.4.2.2 Functions

AMP_COMPARE
: This function compares the values of first_pcsl and current_pcsl to determine if a valid alignment marker payload sequence has been detected and returns the result of the comparison using the variable amp_match. When rx_lpi_active is false, if current_pcsl and first_pcsl are 0, amp_match is set to true. When rx_lpi_active is true, the comparison is performed as follows. If first_pcsl is 0 then amp_match is set to true if current_pcsl is 16. If first_pcsl is 16 then amp_match is set to true if current_pcsl is 0. Otherwise, amp_match is set to false.

SLIP
: Causes the next candidate block position to be tested. The precise method for determining the next candidate block position is not specified and is implementation dependent. However, an implementation shall ensure that all possible block positions are evaluated.

91.5.4.2.3 Counters

amp_counter
: When rx_lpi_active is false, this counter counts the 4096 FEC codewords that separate the ends of

two consecutive normal alignment marker payload sequences. An FEC codeword is 1320 bits per FEC lane for 100GBASE-KR4 and 1360 bits per FEC lane for 100GBASE-KP4. When rx_lpi_active is true, then amp_counter is defined as follows. If first_pcsl corresponds to PCS lane 0, it counts the 256 bits to the end of the expected location of the Rapid Alignment Marker payload corresponding to PCS lane 16. If first_pcsl corresponds to PCS lane 16, this counter counts the 2 FEC codewords minus 256 bits to the end of the expected location of the next Rapid Alignment Marker payload corresponding to PCS lane 0.

cw_bad_count
: Counts the number of consecutive uncorrected FEC codewords. This counter is set to zero when an FEC codeword is received and cw_bad is false for that codeword.

The following counters are only used for the optional EEE capability.

1st_ram_counter
: This counter counts 4 66-bit blocks from the end of one candidate RAM position to the end of the next candidate RAM position. The first instance of the counter counts from the end of the last normal alignment marker received.

1st_ramps_counter
: This counter counts one FEC codeword from the end of one candidate RAM payload to the end of the next RAM payload position. An FEC codeword is 1320 bits per FEC lane for 100GBASE-KR4 and 1360 bits per FEC lane for 100GBASE-KP4

ram_counter
: This counter counts 8 66-bit blocks from the end of the current RAM to the end of the next expected RAM position.

ramps_counter
: This counter counts 2 FEC codewords from the end of the current RAM payload to the end of the next expected RAM payload position.

rx_quiet_timer
: This timer limits the maximum time fec_align_status may be deasserted before the Transmit LPI state diagram concludes that the link has failed. The value of this timer is between 2 ms and 2.8 ms.

tx_quiet_timer
: This timer limits the maximum time rx_align_status may be deasserted before the Transmit LPI state diagram concludes that the link has failed. The value of this timer is between 1.8 ms and 2 ms.

91.5.4.3 State diagrams

The FEC shall implement four synchronization processes as shown in Figure 91–8. The synchronization process operates independently on each lane. The synchronization state diagram determines when the FEC has detected the location of the alignment marker payload sequence in the received bit stream for a given lane of the service interface.

The FEC shall implement the alignment process as shown in Figure 91–9.

When the optional EEE capability is supported, the FEC shall also implement the Transmit LPI process as shown in Figure 91–10 and the Receive LPI process as shown in Figure 91–11. The Transmit LPI state diagram infers when Low Power Idle is being transmitted by the local PCS by checking for the presence of Rapid Alignment Markers. The Receive LPI state diagram infers when Low Power Idle is being received from the link partner using a similar mechanism. Monitoring the position and frequency of alignment markers is also critical to the operation of the alignment marker removal function (see 91.5.2.4 and 91.5.3.4).

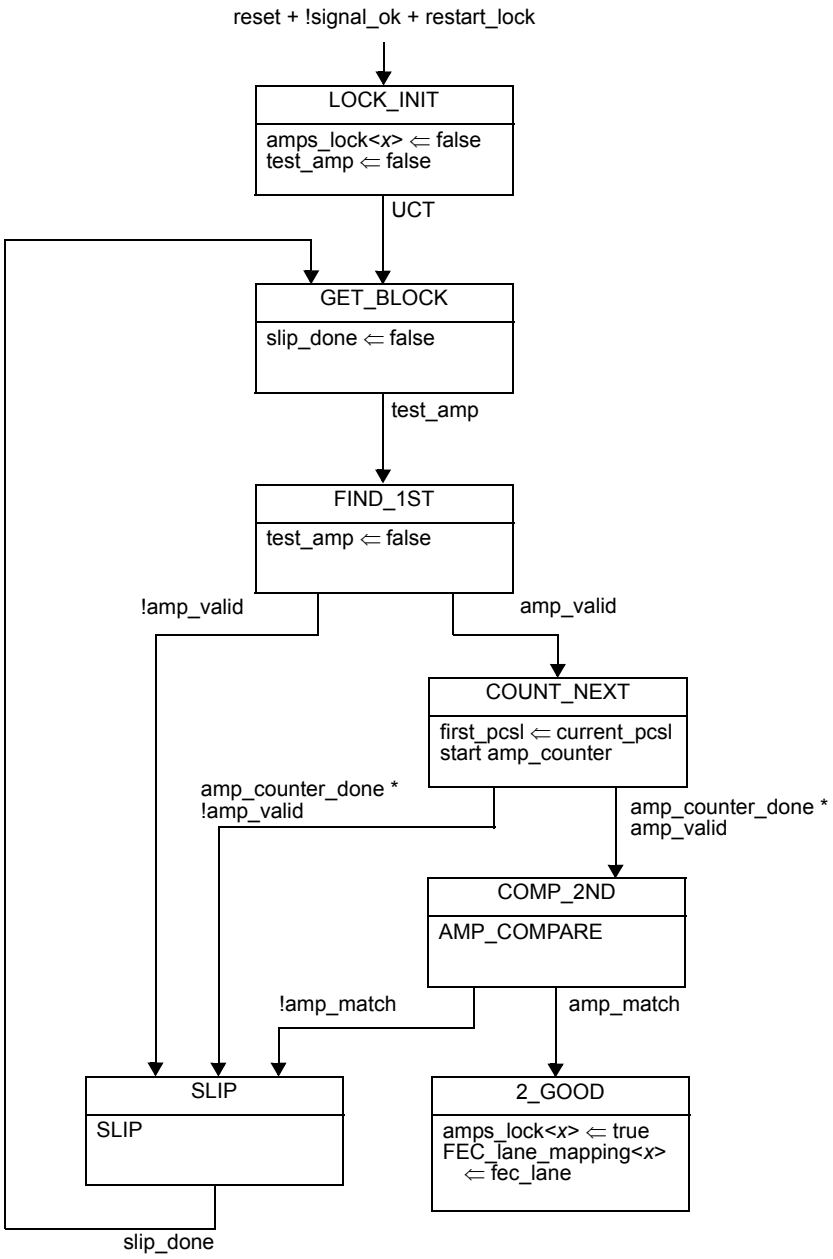


Figure 91–8—FEC synchronization state diagram

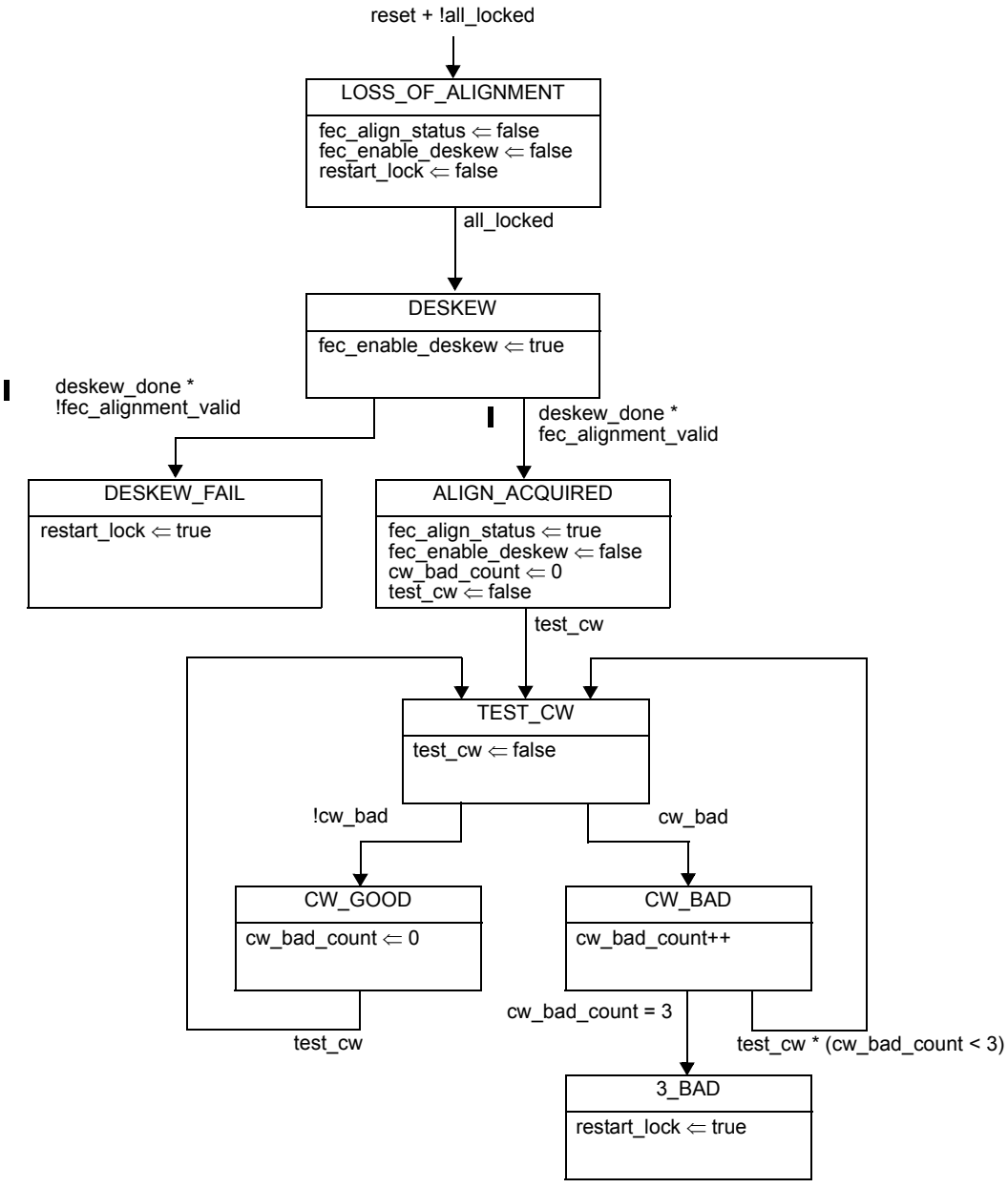


Figure 91–9—FEC alignment state diagram

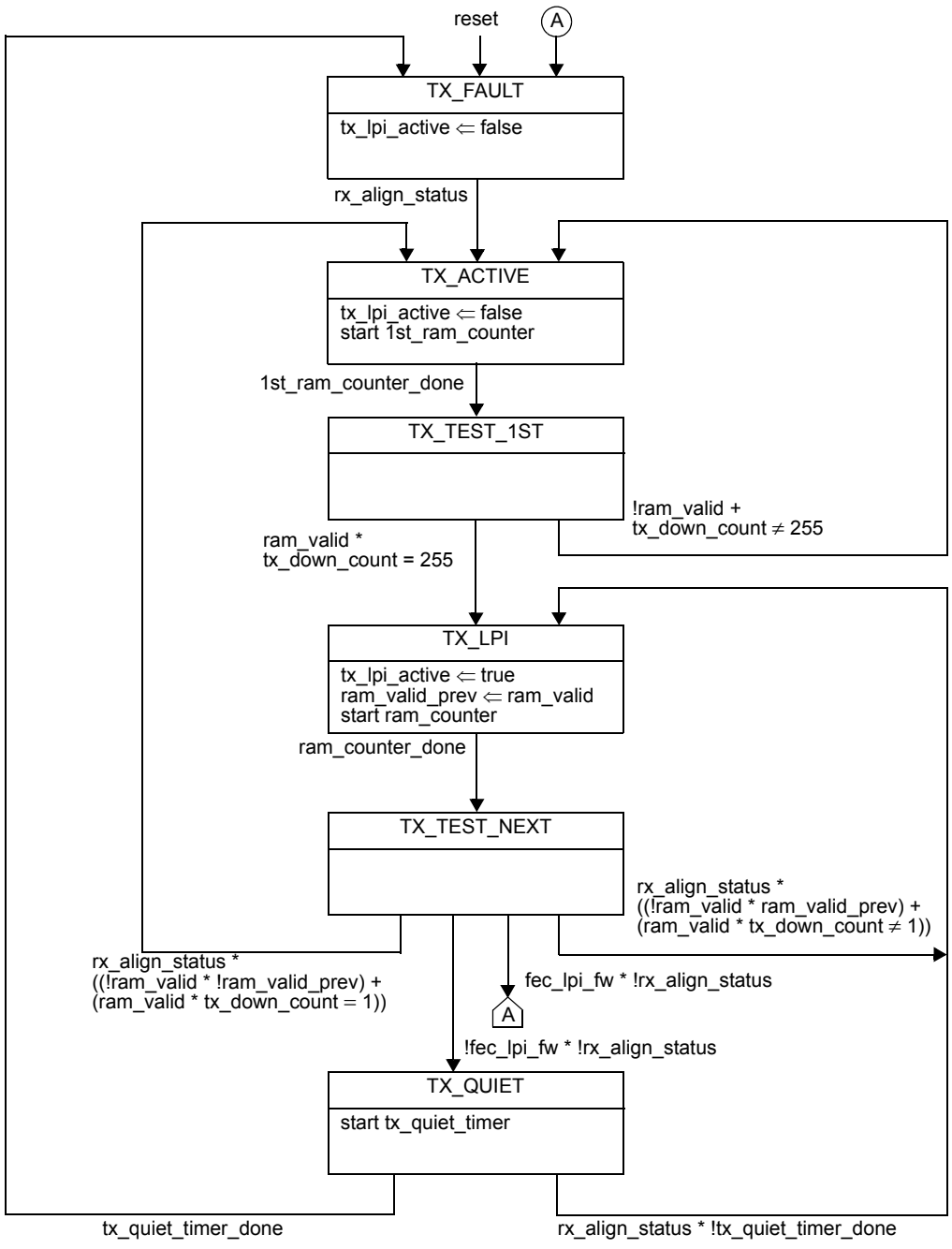


Figure 91–10—Transmit LPI state diagram

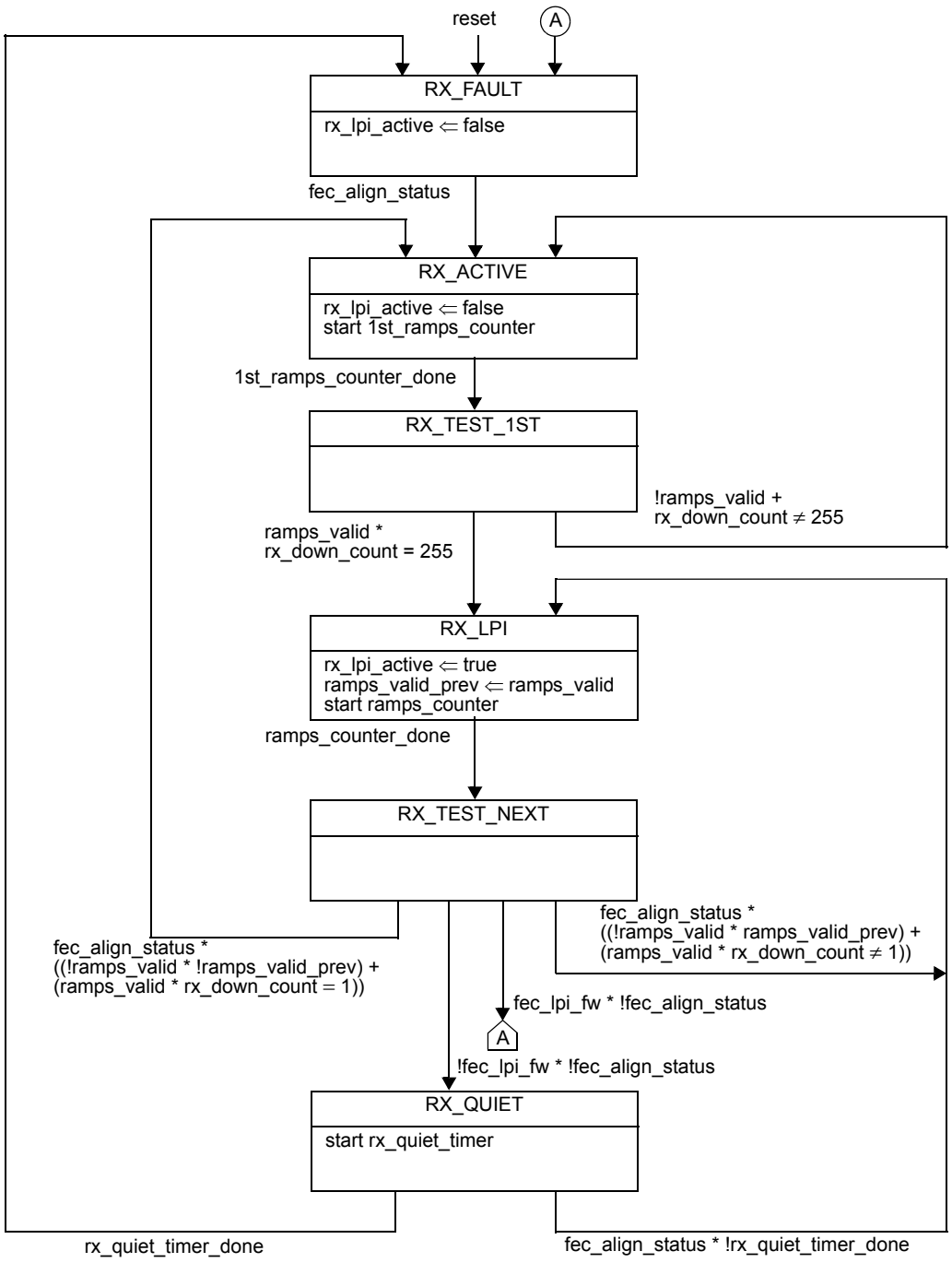


Figure 91–11—Receive LPI state diagram

91.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 91–2, and MDIO status bits to RS-FEC status variables as

shown in Table 91–3, and if a separated PMA (see 45.2.1) is connected to the FEC service interface it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 91–4.

Table 91–2—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction enable	RS-FEC control register	1.200.0	FEC_bypass_correction_enable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable

Table 91–3—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction ability	RS-FEC status register	1.201.0	FEC_bypass_correction_ability
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC corrected codewords	RS-FEC corrected code-words counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected code-words counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC lane alignment status	RS-FEC lane mapping register	1.206.15	fec_align_status
FEC symbol errors, FEC lanes 0 to 3	RS-FEC symbol error coun-ter register, FEC lanes 0 to 3	1.210 to 1.217	FEC_symbol_error_counter_*i*

Table 91–4—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
BIP errors, PCS lanes 0 to 19	RS-FEC BIP error counter register, PCS lanes 0 to 19	1.230 to 1.249	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.269	lane_mapping<*x*>
Block *x* lock	RS-FEC PCS alignment status register	1.280 to 1.281	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status register	1.282 to 1.283	am_lock<*x*>
PCS lane alignment status	RS-FEC PCS alignment status 4 register	1.283.15	align_status

The following subclauses define variables that are not otherwise defined e.g. for use by state diagrams.

91.6.1 FEC_bypass_correction_enable

When this variable is set to one the Reed-Solomon decoder performs error detection without error correction (see 91.5.3.3). When this variable is set to zero, the decoder also performs error correction. The default value of the variable is zero. This variable is mapped to the bit defined in 45.2.1.92a (1.200.0).

91.6.2 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 91.5.3.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. This bit shall have no effect (the decoder shall not bypass error indication) if FEC bypass correction enable (1.200.0) is set to one. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.92a (1.200.1).

91.6.3 FEC_bypass_correction_ability

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error correction. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.92b (1.201.0).

91.6.4 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.92b (1.201.1).

91.6.5 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 91.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.92b (1.201.2).

91.6.6 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.92c (1.202, 1.203).

91.6.7 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors (when the bypass correction feature is supported and enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled).

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.92d (1.204, 1.205).

91.6.8 FEC_lane_mapping<*x*>

When the RS-FEC receive function detects and locks to an alignment marker payload on PMA service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable FEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.92e (1.206).

91.6.9 fec_align_status

This variable assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). It is mapped to the bit defined in 45.2.1.92e (1.206.15).

91.6.10 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i*, where *i*=0 to 3, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.92f and 45.2.1.92g (1.210 to 1.217).

91.6.11 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i*=0 to 19, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC transmit function (see 91.5.2.4). These variables are mapped to the registers defined in 45.2.1.92h and 45.2.1.92i (1.230 to 1.249).

91.6.12 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.92j and 45.2.1.92k (1.250 to 1.269).

91.6.13 block_lock<*x*>

These variables are assigned by the block lock state diagram shown in Figure 82–10 (see 91.5.2.1). They are mapped to the registers defined in 45.2.1.92l and 45.2.1.92m (1.280 to 1.281).

91.6.14 am_lock<*x*>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–11 (see 91.5.2.2). They are mapped to the registers defined in 45.2.1.92n and 45.2.1.92o (1.282 to 1.283).

91.6.15 align_status

This variable is assigned by the PCS deskew state diagram shown in Figure 82–12 (see 91.5.2.2). It is mapped to the bit defined in 45.2.1.92n (1.283.15).

91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs[10]

91.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

91.7.2 Identification

91.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

91.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bj-20XX, Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bj-20XX.)	

Date of Statement	

[10] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

91.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*KR4	100GBASE-CR4 or 100GBASE-KR4		Used to form complete 100GBASE-CR4 or 100GBASE-KR4 PHY	O	Yes [ ] No [ ]
*KP4	100GBASE-KP4		Used to form complete 100GBASE-KP4 PHY	O	Yes [ ] No [ ]
DC	Delay constraints	91.4	Conforms to delay constraints specified in 91.4	M	Yes [ ]
*MD	MDIO capability	91.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEC	Bypass error correction	91.5.3.3	Capability is supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	91.5.3.3	Capability is supported	O	Yes [ ] No [ ]
*EEE	EEE capability	91.5.4.3	Capability is supported	O	Yes [ ] No [ ]

91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	91.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps	M	Yes [ ]
TF2	Lane reorder	91.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	91.5.2.5	tx_xcoded<256:0> constructed per 91.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	91.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	91.5.2.6	Map to am_txmapped<1284:0> per 91.5.2.6	M	Yes [ ]
TF6	Pad value	91.5.2.6	Binary values 00101 and 11010 (the leftmost bit is assigned to the highest bit index) in an alternating pattern	M	Yes [ ]
TF7	Alignment marker insertion	91.5.2.6	First 1285 message bits to be transmitted from every 4096th codeword	M	Yes [ ]
TF8	Alignment marker insertion when tx_lpi_active is true	91.5.2.6	First 1285 message bits to be transmitted from every other codeword	EEE:M	Yes [ ] N/A [ ]
TF9	Alignment marker insertion point	91.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF10	Reed-Solomon encoder for 100GBASE-CR4 or 100GBASE-KR4	91.5.2.7	RS(528,514)	KR4:M	Yes [ ] N/A [ ]
TF11	Reed-Solomon encoder for 100GBASE-KP4	91.5.2.7	RS(544,514)	KP4:M	Yes [ ] N/A [ ]
TF12	Symbol distribution	91.5.2.8	Distributed to 4 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane	M	Yes [ ]

91.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	91.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	91.5.3.2	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for 100GBASE-CR4 or 100GBASE-KR4	91.5.3.3	Corrects any combination of up to t=7 symbol errors in a codeword unless error correction bypassed	KR4:M	Yes [ ] N/A [ ]
RF4	Reed-Solomon decoder for 100GBASE-KP4	91.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword unless error correction bypassed	KP4:M	Yes [ ] N/A [ ]
RF5	Reed-Solomon decoder	91.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF6	Error indication function	91.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords (or errored codewords when correction is bypassed)	M	Yes [ ]
RF7	Error indication when error correction is bypassed	91.5.3.3	Error indication is not bypassed	BEI:M	Yes [ ] N/A [ ]
RF8	Error monitoring while error indication is bypassed	91.5.3.3	When the number of symbols errors in a block of 8192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RF9	Symbol error threshold for 100GBASE-CR4 and 100GBASE-KR4	91.5.3.3	*K*=417	BEI* KR4:M	Yes [ ] N/A [ ]
RF10	Symbol error threshold for 100GBASE-KP4	91.5.3.3	*K*=6380	BEI* KP4:M	Yes [ ] N/A [ ]
RF11	Error monitoring disabled	91.5.3.3	Symbol error monitor is disabled when rx_lpi_active=true	BEI* EEE:M	Yes [ ] N/A [ ]
RF12	Start of error monitoring window	91.5.3.3	Begins on the codeword boundary following the transition of rx_lpi_active from true to false	BEI* EEE:M	Yes [ ] N/A [ ]
RF13	Error monitoring during LPI	91.5.3.3	Error monitor disabled when rx_lpi_active=true	BEI* EEE:M	Yes [ ] N/A [ ]
RF14	Alignment marker removal	91.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF15	256B/257B to 64B/66B transcoder	91.5.3.5	rx_coded_*j*<65:0>, *j*=0 to 3 constructed per 91.5.3.5	M	Yes [ ]
RF16	Block distribution	91.5.3.6	One 66-bit block at a time in a round robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
RF17	Alignment marker mapping	91.5.3.7	Map to am_rx_*x*, *x*=0 to 19 per 91.5.3.7	M	Yes [ ]
RF18	Alignment marker insertion point	91.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-blocks immediately following am_rxmapped	M	Yes [ ]

91.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	91.5.4.2.2	Ensure that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	91.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	91.5.4.3	Per Figure 91–9	M	Yes [ ]
SD4	Transmit LPI process	91.5.4.3	Per Figure 91–10	EEE:M	Yes [ ] N/A [ ]
SD5	Receive LPI process	91.5.4.3	Per Figure 91–11	EEE:M	Yes [ ] N/A [ ]

92. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4

92.1 Overview

This clause specifies the 100GBASE-CR4 PMD and baseband medium. Annex 92A, an associated annex, provides information on parameters with test points that may not be testable in an implemented system.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 92–1, to the appropriate PMA as shown in Table 92–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 92–1—Physical Layer clauses associated with the 100GBASE-CR4 PMD

Associated clause	100GBASE-CR4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R[b]	Required
83A—CAUI	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]There are limitations on the number of PMA lanes that may be used between sublayers, see 83.3.

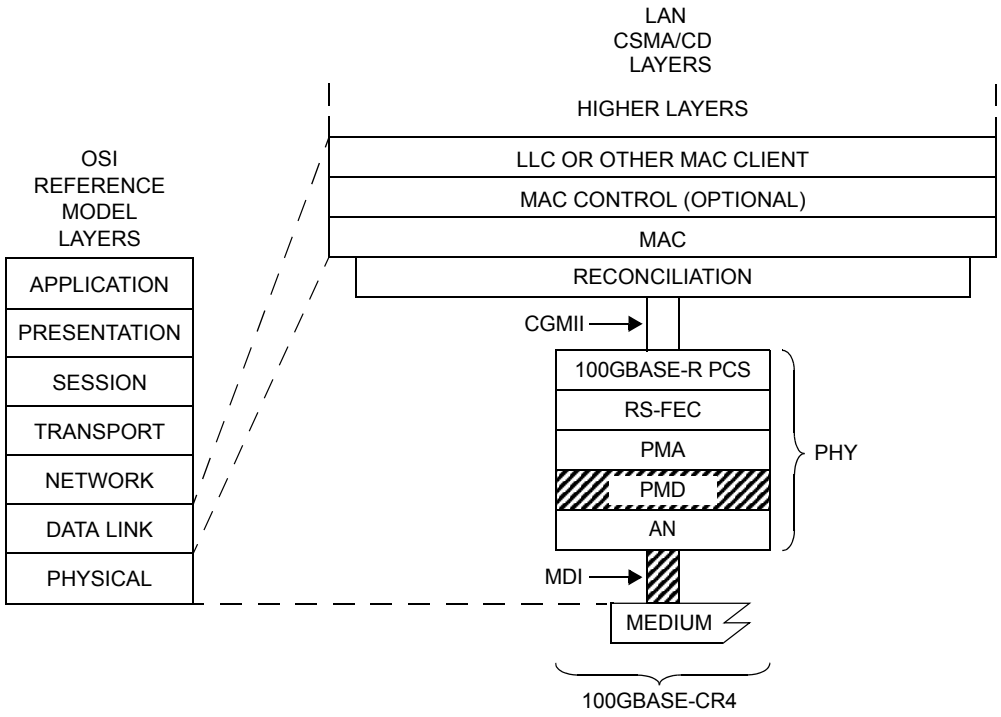
When forming a complete 100GBASE-CR4 Physical Layer, the following guidelines apply.

Differential signals received at the MDI from a transmitter that meets the requirements of 92.8.3 and have passed through the cable assembly specified in 92.10 are received with a BER less than 10^{-5}.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.210a) less than 1.7×10^{-10} for 64-octet frames with minimum inter-packet gap.

A 100GBASE-CR4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

Figure 92–1 shows the relationship of the 100GBASE-CR4 PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.



AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 92–1—100GBASE-CR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

92.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-CR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-CR4 PMD has four parallel bit streams, hence $i = 0$ to 3. The PMA (or the PMD) continuously sends four parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 92.7.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_i.indication parameters are undefined.

If the optional EEE capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

92.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.).

The 100GBASE-CR4 PHY may be extended using CAUI as a physical instantiation of the inter-sublayer service interface between devices. If CAUI is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

92.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 100GBASE-CR4 PMD and AN shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). It is assumed that the one way delay through the medium is no more than 6000 bit times (60 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

92.5 Skew constraints

The Skew (relative delay) between the lanes must be kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–4 and Figure 80–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

92.6 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 92–2, and MDIO status bits to PMD status variables as shown in Table 92–3.

Table 92–2—100GBASE-CR4 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3	PMD training pattern 3	1.1453.12:11	polynomial_3
Seed 3	PMD training pattern 3	1.1453.10:0	seed_3
Polynomial identifier 2	PMD training pattern 2	1.1452.12:11	polynomial_2
Seed 2	PMD training pattern 2	1.1452.10:0	seed_2
Polynomial identifier 1	PMD training pattern 1	1.1451.12:11	polynomial_1
Seed 1	PMD training pattern 1	1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern 0	1.1450.12:11	polynomial_0
Seed 0	PMD training pattern 0	1.1450.10:0	seed_0

92.7 PMD functional specifications

92.7.1 Link block diagram

A 100GBASE-CR4 link in one direction is illustrated in Figure 92–2. For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause. The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 92.8.3 are made at TP2 utilizing the test fixture specified in 92.11.1. Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are performed at TP3 utilizing the test fixture specified in 92.11.1. A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.8.

The 100GBASE-CR4 channel is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 92–2. Annex 92A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable

Table 92–3—100GBASE-CR4 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0
Receiver status 3	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status	1.151.13	frame_lock_3
Start-up protocol status 3	BASE-R PMD status	1.151.14	training_3
Training failure 3	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status	1.151.9	frame_lock_2
Start-up protocol status 2	BASE-R PMD status	1.151.10	training_2
Training failure 2	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status	1.151.5	frame_lock_1
Start-up protocol status 1	BASE-R PMD status	1.151.6	training_1
Training failure 1	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock_0
Start-up protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0

assembly test fixture of Figure 92–15, or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4. Two mated connector pairs and the cable assembly test fixture have been included in the cable assembly specifications defined in 92.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0–TP1 and TP4–TP5 respectively are provided informatively in Annex 92A.

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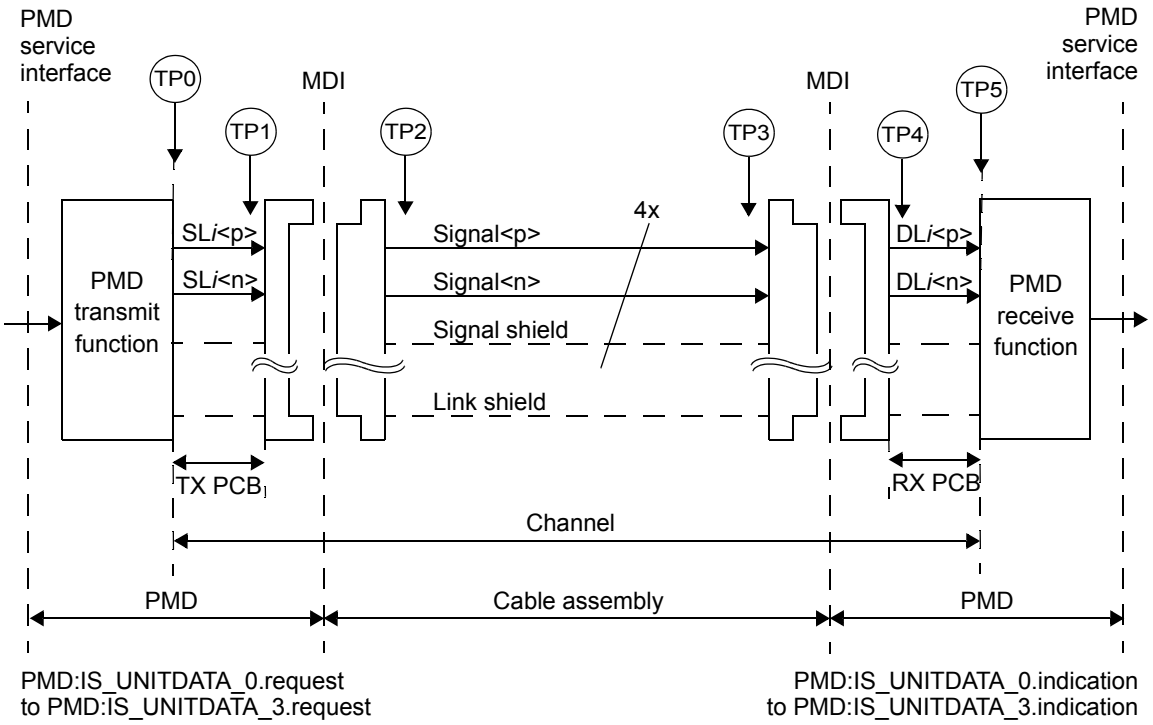


Figure 92–2—100GBASE-CR4 link (one direction is illustrated)

Note that the source lanes (SL), signals SL*i*<p>, and SL*i*<n> are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals, DL*i*<p>, and DL*i*<n> are the positive and negative sides of the receivers differential signal pairs for lane *i* (*i* = 0, 1, 2, 3).

Table 92–4 describes the defined test points illustrated in Figure 92–2.

Table 92–4—100GBASE-CR4 test points

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–15 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.8.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

92.7.2 PMD Transmit function

The PMD transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request (*i*=0 to 3) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 92.8.3. A positive differential output voltage (SL*i*<p> minus SL*i*<n>) shall correspond to tx_bit = one.

If the optional EEE capability is supported, the following requirements apply. When tx_mode is set to ALERT, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane, with the transmit equalizer coefficients set to the preset values (see 92.7.12 and 92.8.3.7). When tx_mode is not set to ALERT, the transmit equalizer coefficients are set to the values determined via the start-up protocol (see 92.7.12).

92.7.3 PMD Receive function

The PMD receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication (*i*=0 to 3). A positive differential input voltage (DL*i*<p> minus DL*i*<n>) shall correspond to rx_bit = one.

92.7.4 Global PMD signal detect function

The variable Global_PMD_signal_detect is the logical AND of the values of PMD_signal_detect_*i* for *i*=0 to 3.

When the MDIO is implemented, this function maps the variable Global_PMD_signal_detect to the register and bit defined in 92.6.

92.7.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the 100GBASE-CR4 PMD to indicate the successful completion of the start-up protocol by the PMD control function (see 92.7.12). PMD_signal_detect_*i* (where *i* represents the lane number in the range 0 to 3) is set to zero when the value of the variable signal_detect is set to false by the Training state diagram for lane *i* (see Figure 72-5). PMD_signal_detect_*i* is set to one when the value of signal_detect for lane *i* is set to true.

If training is disabled by the management variable mr_training_enable (see 92.6), PMD_signal_detect_*i* shall be set to one for *i*=0 to 3.

If the optional EEE capability is supported, the following requirements apply. The value of PMD_signal_detect_*i* (for *i*=0 to 3) is set to zero when rx_mode is first set to QUIET. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall be set to one within 500 ns of the application of the ALERT pattern defined in 92.7.2, with peak-to-peak differential voltage of 720 mV measured at TP2, to the differential pair at the input of the cable assembly that connects the transmitter to the receiver of lane *i*. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall not be set to one when the voltage input to the differential pair of the cable assembly that connects the transmitter to the receiver of lane *i* is less than or equal to 70 mV peak-to-peak differential.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 92.6.

92.7.6 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if EEE deep sleep capability is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 92–6.
b) If a PMD fault (92.7.9) is detected, then the PMD may set Global_PMD_transmit_disable to one.
c) Loopback, as defined in 92.7.8, shall not be affected by Global_PMD_transmit_disable.
d) The following additional requirements apply when the optional EEE capability is supported. The Global PMD transmit disable function shall turn off all of the transmitters as specified in 92.8.3.1 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on all of the transmitters as specified in 92.8.3.1 when tx_mode transitions from QUIET to any other value.

92.7.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0 to 3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 92–6.
b) If a PMD fault (92.7.9) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the electrical transmitter in each lane.
c) Loopback, as defined in 92.7.8, shall not be affected by PMD_transmit_disable_*i*.

92.7.8 Loopback mode

Local loopback mode is provided by the adjacent PMA (see 83.5.8) as a test function. When loopback mode is enabled, transmission requests passed to each transmitter are sent directly to the corresponding receiver, overriding any signal detected by each receiver on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

Control of the loopback function is specified in 83.5.8.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

92.7.9 PMD fault function

If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.1. PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

92.7.10 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then this function shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

92.7.11 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

92.7.12 PMD control function

Each lane of the 100GBASE-CR4 PMD shall use the same control function as 10GBASE-KR, as defined in 72.6.10.

The training frame structure used by the 100GBASE-CR4 PMD control function shall be as defined in 72.6.10 with the exception that 25.78125 GBd symbols replace 10.3125 GBd symbols and 100GBASE-CR4 UI replace 10GBASE-KR UI.

In addition to the coefficient update process specified in 72.6.10.2.5, when frame_lock_*i* is TRUE for lane i (where i represents the lane number in the range 0 to 3), the period from receiving a new request to responding to that request shall be less than 2 ms. The start of the period is the frame marker of the training frame with the new request and the end of the period is the frame marker of the training frame with the corresponding response. A new request occurs when the coefficient update field is different from the coefficient field in the preceding frame. The response occurs when the coefficient status report field is updated to indicated that the corresponding action is complete.

In addition, the training pattern defined in 72.6.10.2.6 is replaced with a set of training patterns designed to minimize the correlation between physical lanes.The training pattern for each lane shall consist of 4094 bits from the output of a pseudo-random bit sequence (PRBS) generator followed by two zeros. The PRBS generator for each lane shall implement each of the four generator polynomials given in Table 92–5 selectable by polynomial_*i* (where i goes from 0 to 3), with default for each lane given in Table 92–5. The state of the generator shall be set to the value in seed_*i*, with default values given in Table 92–5, at the start of the training pattern. An example implementation of the PRBS generator for lane 0 with default settings is given in Figure 92–3. The first 32 bits of the training pattern for a given lane is also provided in Table 92–5.

Table 92–5—PRBS parameters for each physical lane

Lane	Default polynomial, $G(x)$	Default seed bits, S0 is the left most bit	Initial output[a]
0	$1+x^5+x^6+x^{10}+x^{11}$	10101111110	fbf1cb3e
1	$1+x^5+x^6+x^9+x^{11}$	11001000101	fbb1e665
2	$1+x^4+x^6+x^8+x^{11}$	11100101101	f3fdae46
3	$1+x^4+x^6+x^7+x^{11}$	11110110110	f2ffa46b

[a]The first 32 bits of the training pattern are presented in a hexadecimal representation where the hex symbols are transmitted from left to right and the most significant bit of each hex symbol is transmitted first

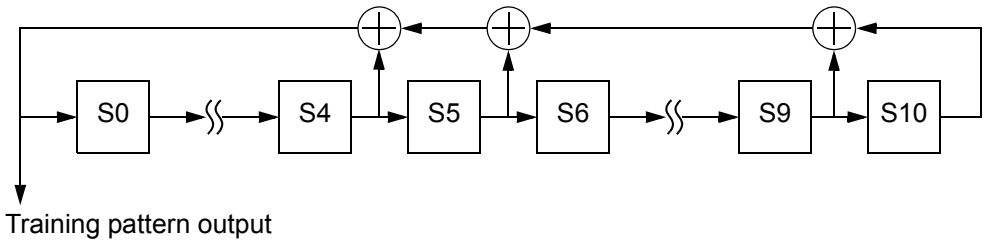


Figure 92–3—Lane 0 PRBS generator

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1.

If the MDIO interface is implemented, then this function shall map the variables polynomial_*i*, seed_*i*, rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* to the registers and bits defined in 92.6.

92.8 100GBASE-CR4 electrical characteristics

92.8.1 Signal levels

The 100GBASE-CR4 MDI is a low-swing AC coupled differential interface. AC coupling within the plug connectors, as defined in 92.12.1, allows for interoperability between components operating from different supply voltages.

92.8.2 Signal paths

The 100GBASE-CR4 MDI signal paths are point-to-point connections. Each path corresponds to a 100GBASE-CR4 MDI lane and comprises two complementary signals, which form a balanced differential pair. For 100GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate on twinaxial cable assemblies ranging from 0.5 m to 5 m in length, as described in 92.10.

92.8.3 Transmitter characteristics

Transmitter characteristics are summarized in Table 92–6. Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixtures specified in 92.11.1. A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified. The transmitter specifications at TP0 are provided informatively in Annex 92A.

Table 92–6—Transmitter characteristics at TP2 summary

Parameter	Subclause reference	Value	Units
Differential peak-to-peak output voltage (max) with Tx disabled	92.8.3.1	35	mV
DC common-mode voltage (max)	92.8.3.1	1.9	V
AC common-mode output voltage, v_{cmi} (max., RMS)	92.8.3.1	30	mV
Differential peak-to-peak voltage, v_{di} (max)	92.8.3.1	1200[a]	mV
Differential output return loss (min)	92.8.3.2	See Equation (92–1)	dB
Common-mode to differential mode output return loss (min)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min)	92.8.3.4	See Equation (92–3)	dB
Transition time (20-80%, min.), no equalization[b]	92.8.3.5	8	ps
Far-end transmit output noise (max) Low insertion loss channel High insertion loss channel	92.8.3.6	 2 1	mV
Transmitter steady-state voltage, v_f	92.8.3.7.1	0.34 min, 0.6 max	V
Linear fit pulse peak (min)	92.8.3.7.1	0.5 × v_f	V
Transmitted waveform max RMS normalized error (linear fit) abs coefficient step size minimum precursor fullscale ratio minimum post cursor fullscale ratio	 92.8.3.7.2 92.8.3.7.4 92.8.3.7.5 92.8.3.7.5	 0.037 0.0083 min, 0.05 max 1.54 4	
Max output jitter (peak-to-peak) Effective deterministic jitter excluding data dependent jitter Effective random jitter Even-odd jitter Total jitter excluding data dependent jitter	92.8.3.9	 0.15 0.15 0.035 0.28	 UI UI UI UI
Signaling rate, per lane	92.8.3.10	25.78125±100 ppm	GBd
Unit interval nominal	92.8.3.10	38.787879	ps

[a]The 100GBASE-CR4 Style-1 connector may support 100GBASE-CR4 or XLPPI interfaces. For implementations that support both interfaces, the transmitter should not exceed the XLPPI voltage maximum until a 100GBASE-CR4 cable assembly has been identified.
[b]Transmit equalization may be disabled by asserting the preset control defined in Table 45–60 and 45.2.1.81.3.

92.8.3.1 Signal levels

The differential output voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode output voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by

Figure 92–4.

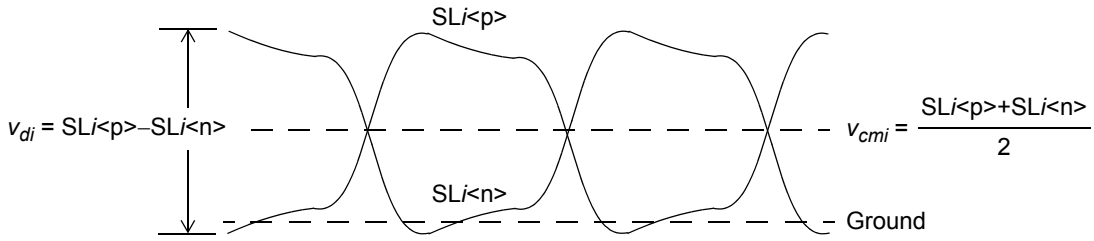


Figure 92–4—Transmitter output voltage definitions

The peak-to-peak differential output voltage shall be less than or equal to 1200 mV regardless of the transmit equalizer setting. The peak-to-peak differential output voltage shall be less than or equal to 35 mV when the transmitter is disabled (refer to 92.7.6 and 92.7.7).

The DC common-mode output voltage shall be between 0 V and 1.9 V with respect to signal ground. The AC common-mode output voltage shall be less than or equal to 30 mV RMS with respect to signal ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

If the optional EEE capability is supported the following requirements also apply. The peak-to-peak differential output voltage shall be less than 35 mV within 500 ns of the transmitter being disabled. When the transmitter is disabled, the peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of the transmitter being enabled. The transmitter is enabled by the assertion of tx_mode=ALERT and the preceding requirement applies when the transmitted symbols are the periodic pattern defined in 92.8.1 and the transmitter equalizer coefficients are assigned their preset values. The transmitter shall meet the requirements of 92.8.3 within 1 μs of the transmitter being enabled. When the transmitter is disabled, the DC common-mode output voltage shall be maintained to within ±150 mV of the value for the enabled transmitter.

Differential and common-mode signal levels are measured with a PRBS9 test pattern.

92.8.3.2 Transmitter differential output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (92–1). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$Return\_loss(f) \geq \begin{cases} 12 - 0.5f & 0.01 \leq f \leq 8 \\ 5.65 - 9.71\log_{10}(f/14) & 8 < f \leq 19 \end{cases} \quad \text{(dB)} \qquad (92\text{–}1)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

92.8.3.3 Common-mode to differential mode output return loss

The common-mode to differential mode output return loss, in dB, of the transmitter shall meet Equation (92–2).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 22 - (20/25.78)f & 0.01 \leq f < 12.89 \\ 15 - (6/25.78)f & 12.89 \leq f \leq 19 \end{array} \right\} \quad \text{(dB)} \qquad (92–2)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

The common-mode to differential mode output return loss is illustrated in Figure 92–5.

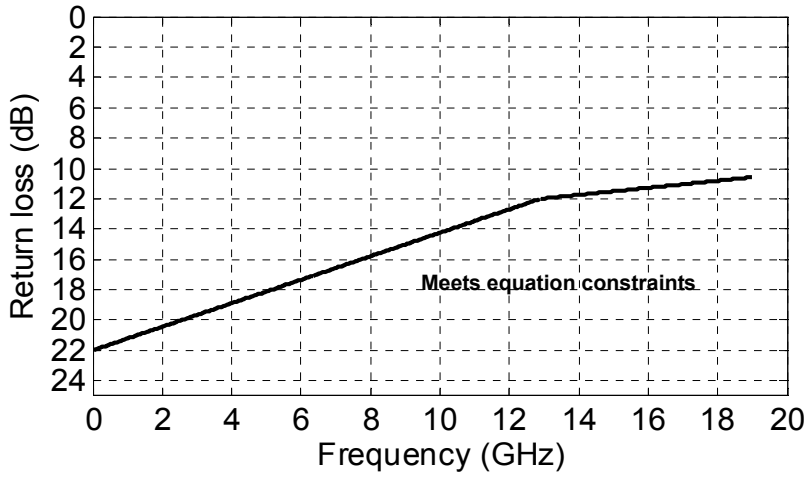


Figure 92–5—Common-mode to differential mode return loss

92.8.3.4 Common-mode to common-mode output return loss

The common-mode to common-mode output return loss, in dB, of the transmitter shall meet Equation (92–3).

$$Return\_loss(f) \geq 2 \quad \text{(dB)} \qquad (92–3)$$

for $0.2 \leq f \leq 19$ GHz

where

f is the frequency in GHz
$Return\_loss(f)$ is the common-mode to common-mode return loss at frequency f

92.8.3.5 Transition time

Transition times (rise and fall times) are defined in 86A.5.3.3. The transition times shall be greater than or equal to 8 ps when transmit equalization is disabled (see 72.6.10.2.3.1).

92.8.3.6 Transmitter noise parameter measurements

The far-end transmitter output noise is an additional source of noise to the cable assembly's integrated crosstalk noise (ICN) specified in 92.10.11. The far-end transmitter output noise parameter is characterized using two reference channels; a "low-loss" cable assembly with insertion loss on the reference pair of 8 dB ± 1.6 dB at 12.8906 GHz and cable assembly integrated crosstalk noise (ICN) meeting the requirements of 92.10.11 and a "high-loss" cable assembly with insertion loss on the reference pair of 20 dB ± 1.5 dB at 12.8906 GHz and cable assembly ICN meeting the requirements of 92.10.11. The far-end transmitter output noise is characterized as a deviation from the cable assembly ICN using the following procedure:

1) Compute the far-end integrated crosstalk noise σ_{fx} into the reference lane of the cable assembly using the methodology of 92.10.11 and the parameters in Table 92–14.
2) Denote σ_l as the far-end ICN for the low-loss cable assembly.
3) Denote σ_h as the far-end ICN for the high-loss cable assembly.
4) The transmitter under test is connected to one end of the reference cable assembly and the other end is connected to the cable assembly test fixture specified in 92.11.2.
5) All lanes of the cable assembly test fixture are terminated in the reference impedance with the reference lane connected to the measuring instrument.
6) The reference lane of the transmitter under test sends a square wave test pattern as specified in 83.5.10 while all other adjacent transmitter lanes send either scrambled idle or PRBS31.
7) A fixed point on the square wave test pattern is chosen and the RMS deviation from the mean voltage at this observation point is measured. The histogram for RMS noise measurement is 1 UI wide.
8) The measurement should not include the measurement system noise. It may be necessary to correct for test system noise.

For the low-loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (92–4).

$$RMSl_{dev} \le \sqrt{\sigma_l^2 + 2^2} \tag{92–4}$$

For the high-loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (92–5).

$$RMSh_{dev} \le \sqrt{\sigma_h^2 + 1^2} \tag{92–5}$$

92.8.3.7 Transmitter output waveform

The 100GBASE-CR4 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model

for the transmit equalizer is the three tap transversal filter shown in Figure 92–6.

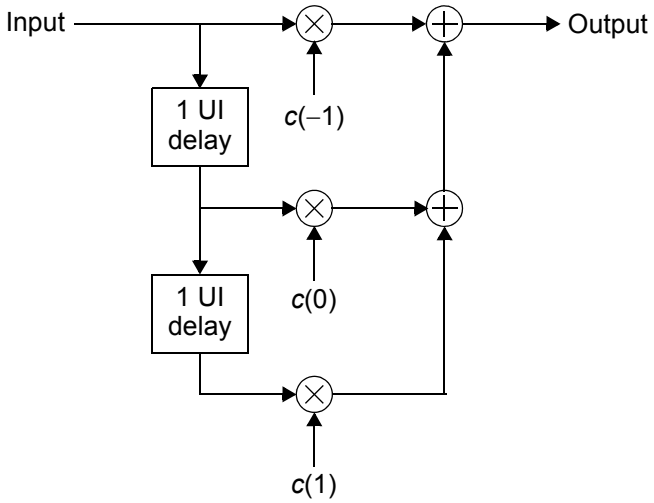


Figure 92–6—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 92.7.12 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

This command set includes instructions to

a) Increment coefficient $c(i)$.
b) Decrement coefficient $c(i)$.
c) Hold coefficient $c(i)$ at its current value.
d) Set the coefficients to a pre-defined value (preset or initialize).

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that

a1) The requested update to coefficient $c(i)$ has completed (updated).
b1) Coefficient $c(i)$ is at its minimum value.
c1) Coefficient $c(i)$ is at its maximum value.
d1) Coefficient $c(i)$ is ready for the next update request (not_updated).

The transmitter output waveform is characterized using the procedure described in 85.8.3.3. The parameters of the linear pulse fit and equalizer are summarized in Table 92–7.

Table 92–7—Linear fit pulse and equalizer parameters

Description	Symbol	Value	Units
Linear fit pulse length	N_p	11	UI
Linear fit pulse delay	D_p	2	UI
Equalizer length	N_w	11	UI
Equalizer delay	D_w	2	UI

92.8.3.7.1 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M (refer to 85.8.3.3 step 3). The steady-state voltage shall be greater than or equal to 0.34 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the "preset" values.

The peak value of $p(k)$ shall be greater than $0.5 \times v_f$ after the transmit equalizer coefficients have been set to the "preset" values.

92.8.3.7.2 Linear fit error

For any configuration of the transmit equalizer, the RMS value of the error between the linear fit and the measured waveform, $e(k)$, normalized to the peak value of the linear fit pulse, $p(k)$, shall be less than or equal to 0.037.

92.8.3.7.3 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72–5) or receives a valid request to “initialize” from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio $(c(0)+c(1)–c(–1))/(c(0)+c(1)+c(–1))$ is $1.29 \pm 10\%$ and the ratio $(c(0)–c(1)+c(–1))/(c(0)+c(1)+c(–1))$ is $2.57 \pm 10\%$. These requirements apply upon the assertion of a coefficient status report of “updated” for all coefficients.

92.8.3.7.4 Coefficient step size

The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to “increment” that coefficient shall be between 0.0083 and 0.05. The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to “decrement” that coefficient shall be between –0.0083 and –0.05.

The change in the normalized amplitude of the coefficient is defined to be the difference in the value measured prior to the assertion of the “increment” or “decrement” request (e.g., the coefficient update request for all coefficients is “hold”) and the value upon the assertion of a coefficient status report of “updated” for that coefficient.

92.8.3.7.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient will reach a lower or upper bound based on the coefficient range or restrictions placed on the minimum steady-state differential output voltage or the maximum peak-to-peak differential output voltage.

With $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0) - c(1))/(c(0) + c(1))$ shall be greater then or equal to 4.

With $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0) - c(-1))/(c(0) + c(-1))$ shall be greater then or equal to 1.54.

Note that a coefficient may be set to zero by first asserting a coefficient preset request and then manipulating the other coefficients as required by the test.

92.8.3.8 Insertion loss TP0 to TP2 or TP3 to TP5

The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is given by Equation (92–6). Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.37 dB at 12.8906 GHz.

$$Insertion\_loss(f) \le \begin{cases} 0.084 + 0.599\sqrt{f} + 0.631f & 0.01 \le f < 14 \\ -20.07 + 2.23f & 14 \le f \le 19 \end{cases} \text{ (dB)} \qquad (92\text{–}6)$$

where

f is the frequency in GHz
$Insertion\_loss(f)$ is the insertion loss at frequency f

The maximum insertion loss of TP0 to TP2 or TP3 to TP5 is illustrated in Figure 92–7.

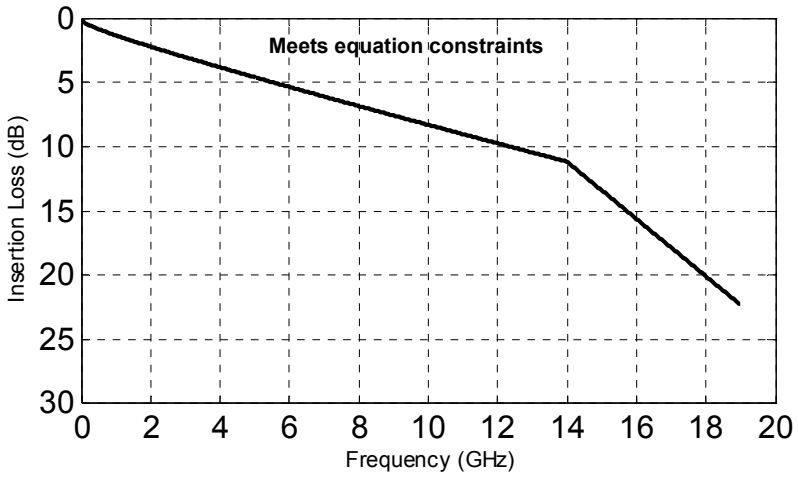


Figure 92–7—Maximum insertion loss TP0 to TP2 or TP3 to TP5

92.8.3.9 Transmitter output jitter

Four components of the transmitter output jitter are defined in this subclause: even-odd jitter, total jitter (TJ), data dependent jitter, and effective random jitter (RJ).

The effect of a single-pole high-pass filter with a 3 dB frequency of 10 MHz is applied to the jitter. The test pattern for TJ and RJ measurements is either PRBS31 (see 83.5.10) or scrambled idle (see 82.2.10). The voltage threshold for the measurement of BER or crossing times is the mid-point (0 V) of the AC-coupled differential signal.

92.8.3.9.1 Even-odd jitter

Even-odd jitter is measured on two repetitions of a repeating pattern with an odd number of bits and at least two transitions between one and zero or zero and one. PRBS9 is such a pattern. The deviation of the time of each transition from an ideal clock at the signaling rate is measured. Even-odd jitter is defined as the magnitude of the difference between the average deviation of all even-numbered transitions and the average deviation of all odd-numbered transitions, where determining if a transition is even or odd is based on possible transitions but only actual transitions are measured and averaged.

Even-odd jitter shall be less than or equal to 0.035 UI regardless of the transmit equalization setting.

NOTE—Even-odd jitter has been referred to as duty cycle distortion by other Physical Layer specifications for operation over electrical backplane or twinaxial copper cable assemblies (see 72.7.1.9). The term even-odd jitter is used here to distinguish it from the duty cycle distortion referred to by Physical Layer specifications for operation over fiber optic cabling.

92.8.3.9.2 Total jitter

The total jitter (TJ) of a signal is defined as the range (the difference between the lowest and highest values) of sampling times around the signal transitions for which the BER at these sampling times is greater than or equal to 10^{-12}.

Total jitter excluding data dependent jitter is the difference between TJ and DDJ and shall be less than or equal to 0.28 UI regardless of the transmit equalization setting.

92.8.3.9.3 Data dependent jitter

Data dependent jitter (DDJ) is defined in 85.8.3.8. The measurement filter and bandwidth defined in 92.8.3 is used in place of the bandwidth defined in 85.8.3.8.

92.8.3.9.4 Effective deterministic and random jitter

The effective random jitter (RJ) of a signal is defined to be the difference between the TJ and effective deterministic jitter (DJ). Effective DJ is derived from the measured jitter distribution as follows.

a) Measure the jitter J*n* which is defined to be the interval that includes all but 10^{-n} of the jitter distribution. If measured by plotting BER vs. decision time, it is the time interval between the two points with a BER of $10^{-n}/4$. Measure two values: J9 and J5.
b) For each J*n* determine the associated Q*n* from the inverse normal cumulative probability distribution adjusted for an assumed transition density of 0.5. Q9 is 5.998 and Q5 is 4.265.
c) Calculate the effective DJ as (Q9×J5 – Q5×J9)/(Q9 – Q5).

Effective deterministic jitter excluding data dependent jitter is the difference between effective DJ and DDJ (see 92.8.3.9.3) and shall be less than or equal to 0.15 UI regardless of the transmit equalization setting.

The effective RJ shall be less than or equal to 0.15 UI regardless of the transmit equalization setting.

92.8.3.10 Signaling rate range

The 100GBASE-CR4 MDI signaling rate shall be 25.78125 GBd ±100 ppm per lane. The corresponding unit interval is approximately 38.787879 ps.

92.8.4 Receiver characteristics

The receiver characteristics are summarized in Table 92–8. Unless specified otherwise, all receiver measurements defined in Table 92–8 are made at TP3 utilizing the test fixtures specified in 92.11.1. Unless otherwise specified, a test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all receiver input signal measurements. The receiver specifications at TP5 are provided informatively in Annex 92A.

Table 92–8—Receiver characteristics at TP3 summary

Parameter	Subclause reference	Value	Units
Receiver input amplitude tolerance	92.8.4.1	1200 mV as measured at TP2	mV
Differential input return loss (min)[a]	92.8.4.2	Equation (92–7)	dB
Differential to common-mode input return loss	92.8.4.3	Equation (92–8)	dB
Bit error ratio	92.8.4.4	10^{-5} or better	
Signaling rate, per lane	92.8.4.6	25.78125 ± 100 ppm	GBd
Unit interval (UI) nominal	92.8.4.6	38.787879	ps

[a]Relative to 100 Ω differential.

92.8.4.1 Receiver input amplitude tolerance

100GBASE-CR4 receiver shall operate at a BER better than 10^{-5} when connected to a compliant transmitter whose peak-to-peak differential output voltage, as defined by 92.8.3.1 using preset equalizer coefficients, is 1200 mV using a compliant cable assembly with the minimum insertion loss defined in 92.10.2. The receiver is allowed to control the transmitter equalizer coefficients, using the protocol defined in 92.7.12 or an equivalent process, to meet this requirement.

92.8.4.2 Receiver differential input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (92–7). This return loss requirement applies at all valid input levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$Return\_loss(f) \geq \begin{cases} 12 - 0.5f & 0.01 \leq f \leq 8 \\ 5.65 - 9.71\log_{10}(f/14) & 8 < f \leq 19 \end{cases} \quad (\text{dB}) \qquad (92\text{–}7)$$

where

f is the frequency in GHz

Return_loss(*f*) is the return loss at frequency *f*

92.8.4.3 Differential to common-mode input return loss

The differential to common-mode input return loss, in dB, of the receiver shall meet Equation (92–8).

$$Return\_loss(f) \geq \begin{cases} 25 - (20/25.78)f & 0.01 \leq f < 12.89 \\ 18 - (6/25.78)f & 12.89 \leq f \leq 19 \end{cases} \quad \text{(dB)} \qquad (92\text{–}8)$$

where

f is the frequency in GHz
Return_loss(*f*) is the return loss at frequency *f*

92.8.4.4 Receiver interference tolerance test

The receiver interference tolerance of each lane shall comply with both test 1 and test 2 using the parameters of Table 92–9 when measured according to the requirements of 92.8.4.4.1 to 92.8.4.4.5.

Table 92–9—100GBASE-CR4 interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
Maximum BER before FEC	10^{-5}	10^{-5}	
Fitted insertion loss coefficients	$a_1 = 1.7$ $a_2 = 0.546$ $a_4 = 0.01$	$a_1 = 4.3$ $a_2 = 0.571$ $a_4 = 0.04$	dB/√GHz dB/GHz dB/GHz^2
Applied SJ[a] (peak-to-peak)	0.115	0.115	UI
Applied RJ[b] (peak-to-peak)	0.13	0.13	UI
Even-odd jitter	0.035	0.035	UI
Calibrated far-end crosstalk (RMS)	6.3	2.2	mV
Calibrated ICN (RMS) – σ_{nx} [c]	3.7	3.7	mV

[a]Applied SJ frequency >100 MHz, specified at TP0.
[b]Applied random jitter at TP0 is specified at 10^{-12}.
[c]σ_{nx} is subtracted from Calibrated ICN (RMS) in square root of the sum of the squares sense.

92.8.4.4.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 92–8. The requirements of this subclause are verified at the pattern generator connection (PGC) or test references in Figure 92–8 and Figure 92–9. The lanes under test (LUT) are illustrated in Figure 92–8 and Figure 92–9. The cable assembly single ended receive lanes are terminated in 50 Ohm to provide 100 Ohm differential termination.

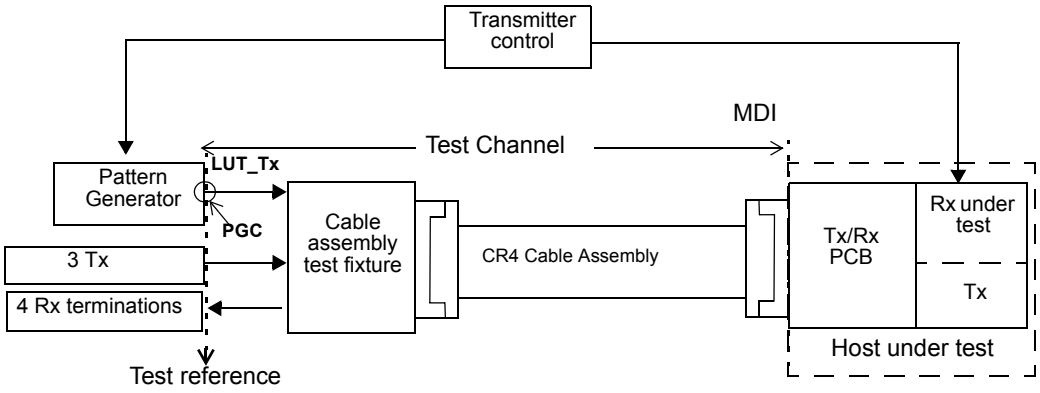


Figure 92–8—Interference tolerance test setup

92.8.4.4.2 Test channel

The test channel consists of the following:

a) A cable assembly
b) A cable assembly test fixture
c) A connecting path from the pattern generator to the cable assembly test fixture

92.8.4.4.3 Test channel calibration

The insertion loss, near-end integrated crosstalk noise, and far-end crosstalk of the test channels are characterized at the test references as illustrated in Figure 92–9 using the cable assembly test fixtures specified in 92.11.2.

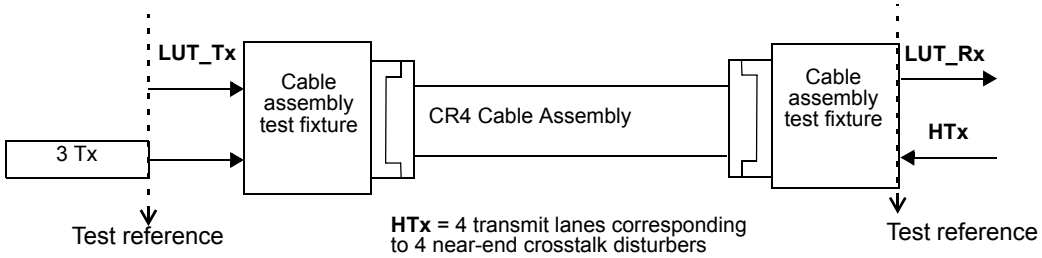


Figure 92–9—Test channel calibration

The fitted insertion loss coefficients of the lane under test (LUT), derived using the fitting procedure in 92.10.2, shall meet the test values in Table 92–9. It is recommended that the deviation between the insertion loss and the fitted insertion loss be as small as practical and that the fitting parameters be as close as practical to the values given in Table 92–9.

The MDNEXT is measured from points HTx to adjacent point LUT_Rx in Figure 92–9. HTx is the set of 4 transmit lanes of the device under test corresponding to the 4 near-end crosstalk disturbers with the parameters given in Table 92–14. The RMS value of the integrated MDNEXT crosstalk noise, determined using Equation (92–23), Equation (92–25), and Equation (92–27), shall meet the test values in Table 92–9.

The far-end crosstalk disturbers consist of 100GBASE-CR4 transmitters. It is recommended that the transition time, equalization setting, and path from the far-end crosstalk disturbers to the cable assembly test fixture emulate the pattern generator as much as practical. For 100GBASE-CR4 test channels, the crosstalk that is coupled into a receive lane is from three transmitters. The disturber transmitters send either scrambled idle codes or PRBS31. The amplitudes of each of the disturbers should not deviate more than 3 dB from the mean of the disturber amplitudes. The amplitudes of the disturbers should be such that the calibrated far-end crosstalk in Table 92–9 is met in the calibration setup at the LUT point with no signal applied at the PGC, and HTx and PGC terminated in 100 Ω differentially.

92.8.4.4.4 Pattern generator

The pattern generator transmits data to the device under test. At the start of transmitter training, the pattern generator output amplitude shall be 800 mV peak-to-peak differential when measured on an alternating one-zero pattern. The output amplitude, measured on an alternating one zero pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The transition times of the pattern generator, as defined in 93.8.1.5, are 19 ps. If the transition times of the pattern generator, T_r, are less than 19 ps, the value of a_4 in Table 92–9 is increased by da_4 from Equation (92–9).

$$da_4 = 6.05 \times 10^{-5}(19^2 - T_r^2) \quad (92–9)$$

where T_r is the rise time in ps.

The pattern generator shall be set to match the jitter specification in Table 92–9. The output waveform of the pattern generator shall comply to 93.8.1.

92.8.4.4.5 Test procedure

For 100GBASE-CR4 testing, the pattern generator is first configured to transmit the training pattern defined in 92.7.12. During this initialization period, the device under test (DUT) configures the pattern generator equalizer, via transmitter control, to the coefficient settings it would select using the protocol described in 72.6.10 and the receiver will be tuned using its optimization method.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to either scrambled idle encoded by RS-FEC or PRBS31. The receiver under test shall meet the target BER listed in Table 92–9. During the tests, the disturbers transmit at their calibrated level and all of the transmitters in the device under test transmit either scrambled idle or PRBS31, with the maximum compliant amplitude and equalization turned off (preset condition).

92.8.4.5 Receiver jitter tolerance

Receiver jitter tolerance is defined by the procedure in this subclause. When measured using the test setup shown in Figure 92–8, or its equivalent, the BER for each lane of the receiver shall be less than or equal to 10^{-5} for each case listed in Table 92–10. The pattern generator meets the requirements of 92.8.4.4.4. The test channel meets the requirements of the interference tolerance test channel using Test 2 values listed in Table 92–9.

The test procedure is as described in 92.8.4.4.5 except that during the test the disturber transmitters are off and the pattern generator jitter is set to the frequency and peak-to-peak amplitude specified in Table 92–10.

Table 92–10—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Jitter frequency	190	940	kHz
Peak-to-peak jitter amplitude	5	1	UI

92.8.4.6 Signaling rate range

A 100GBASE-CR4 receiver shall comply with the requirements of 92.8.4.4 for any signaling rate in the range 25.78125 GBd ± 100 ppm. The corresponding unit interval is approximately 38.787879 ps.

92.9 Channel characteristics

The 100GBASE-CR4 channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 92–2. The channel parameters insertion loss, insertion loss deviation (ILD), insertion loss to crosstalk ratio, and the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane are provided informatively in 92A.4 through 92A.7.

92.10 Cable assembly characteristics

The 100GBASE-CR4 cable assembly contains insulated conductors terminated in a connector at each end for use as a link segment between MDIs. This cable assembly is primarily intended as a point-to-point interface of up to 5 m between network ports using controlled impedance cables. All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in 92.11.2 and illustrated in Figure 92–15. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of 92.10 are met.

Table 92–11 provides a summary of the cable assembly differential characteristics at 12.8906 GHz and references to the subclauses addressing each parameter.

Table 92–11—Cable assembly differential characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 12.8906 GHz	92.10.2	22.48	dB
Minimum insertion loss at 12.8906 GHz	92.10.2	8	dB
Minimum return loss at 12.8906 GHz	92.10.4	6	dB
MDNEXT loss	92.10.9	Equation (92–23)	dB
MDFEXT loss	92.10.10	Equation (92–24)	dB

92.10.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

92.10.2 Cable assembly insertion loss

The fitted cable assembly insertion loss $IL_{fitted}(f)$ as a function of frequency f is defined in Equation (92–10).

$$IL_{\text{fitted}}(f) = a_1\sqrt{f} + a_2 f + a_4 f^2 \quad \text{(dB)} \tag{92–10}$$

where

f is the frequency in GHz
$IL_{\text{fitted}}(f)$ is the fitted cable assembly insertion loss at frequency f

Given the cable assembly insertion loss measured between TP1 and TP4 is at N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 19000 MHz with a maximum frequency spacing of 10 MHz, the coefficients of the fitted insertion loss are determined using Equation (92–11) and Equation (92–12).

Define the frequency matrix F as shown in Equation (92–11).

$$F = \begin{bmatrix} \sqrt{f_1} & f_1 & f_1^2 \\ \sqrt{f_2} & f_2 & f_2^2 \\ \cdots & \cdots & \cdots \\ \sqrt{f_N} & f_N & f_N^2 \end{bmatrix} \tag{92–11}$$

The polynomial coefficients a_1, a_2, and a_4 are determined using Equation (92–12). In Equation (92–12), T denotes the matrix transpose operator and IL is a column vector of the measured insertion loss values, IL_n at each frequency f_n.

$$\begin{bmatrix} a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T IL \tag{92–12}$$

The fitted insertion loss corresponding to one example of the maximum insertion loss at 12.8906 GHz is illustrated in Figure 92–10.

The measured insertion loss of the cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in Equation (92–13) and illustrated in Figure 92–11.

$$IL_{Cabmin}(f) = 0.7\sqrt{f} + 0.3f + 0.01f^2 \ \text{(dB)} \tag{92–13}$$

where

f is the frequency in GHz
$IL_{\text{Cabmin}}(f)$ is the minimum cable assembly insertion loss at frequency f

Table 92–12—Maximum and minimum cable assembly insertion loss characteristics

Description	Value	Unit
Maximum insertion loss at 12.8906 GHz	22.48	dB
Minimum insertion loss at 12.8906 GHz	8	dB

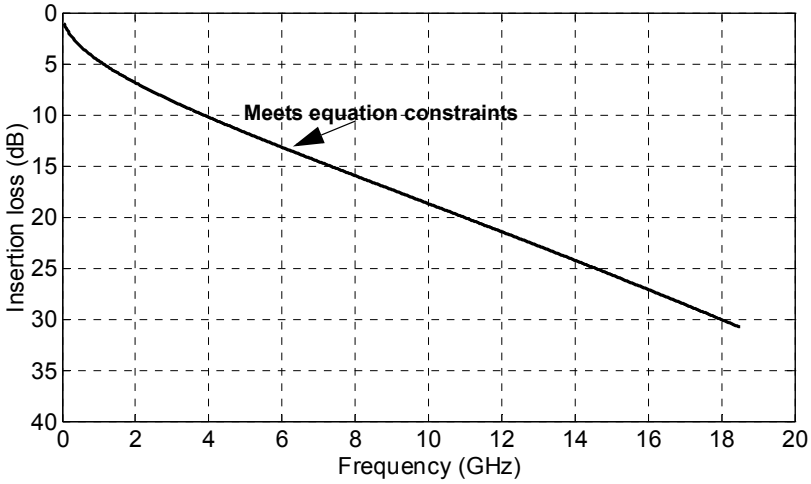


Figure 92–10—Example maximum cable assembly insertion

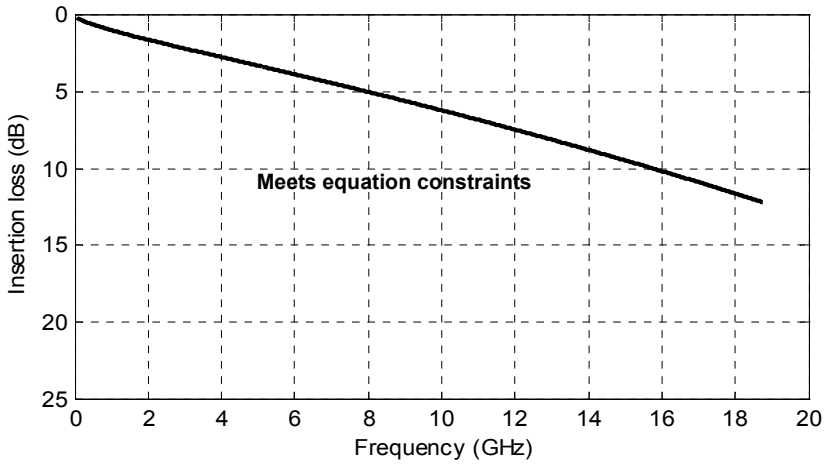


Figure 92–11—Minimum cable assembly insertion loss

92.10.3 Cable assembly insertion loss deviation (ILD)

The cable assembly insertion loss deviation is the difference between the cable assembly insertion loss and the fitted cable assembly insertion loss determined using Equation (92–14).

$$ILD(f) = IL(f) - IL_{\text{fitted}}(f) \quad (92–14)$$

where

f is the frequency in GHz
$ILD(f)$ is the cable assembly insertion loss deviation at frequency f

92.10.4 Cable assembly return loss

The return loss of each pair of the 100GBASE-CR4 cable assembly shall meet the values determined using Equation (92–15).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 16.5 - 2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66 - 14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{array} \right\} \text{ (dB)} \quad (92–15)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

The minimum cable assembly return loss is illustrated in Figure 92–12.

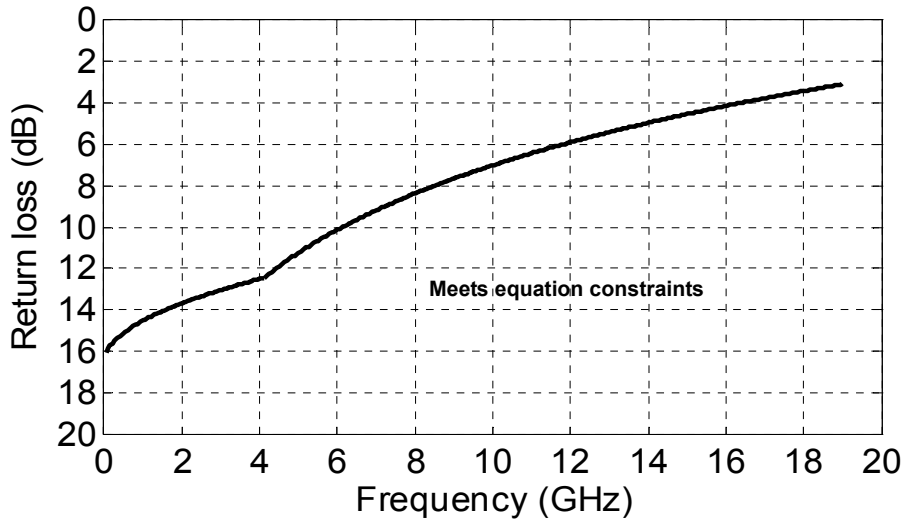


Figure 92–12—Minimum cable assembly return loss

92.10.5 Differential to common-mode return loss

The differential to common-mode return loss, in dB, of the cable assembly shall meet Equation (92–16).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 25 - (20/25.78)f & 0.01 \leq f < 12.89 \\ 18 - (6/25.78)f & 12.89 \leq f \leq 19 \end{array} \right\} \quad \text{(dB)} \qquad (92\text{–}16)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

The differential to common-mode cable assembly return loss is illustrated in Figure 92–13.

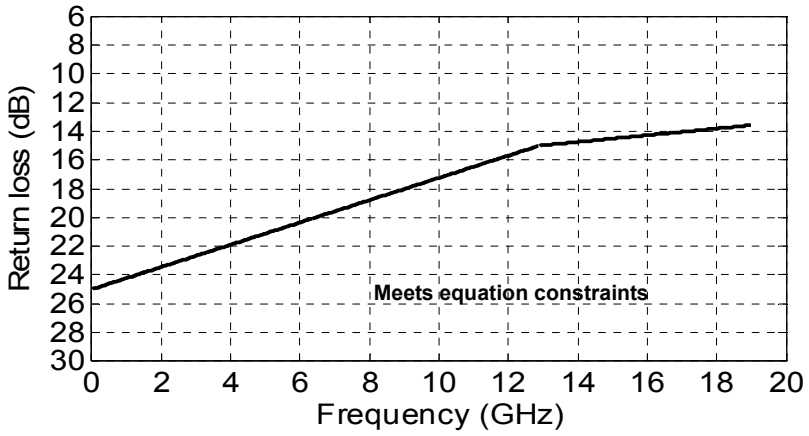


Figure 92–13—Differential to common-mode cable assembly return loss

92.10.6 Differential to common-mode conversion loss

The difference between the cable assembly differential to common-mode conversion loss and the cable assembly insertion loss shall meet Equation (92–17)

$$Conversion\_loss(f) - IL(f) > 10 \quad (92–17)$$

where

f is the frequency in GHz
$Conversion\_loss(f)$ is the cable assembly differential to common-mode conversion loss
$IL(f)$ is the cable assembly insertion loss

92.10.7 Common-mode to common-mode return loss

The common-mode to common-mode return loss, in dB, of the cable assembly shall meet Equation (92–18).

$$Return\_loss(f) \geq 2 \quad (\text{dB}) \quad (92–18)$$

for $0.2 \leq f \leq 19$ GHz

where

f is the frequency in GHz
$Return\_loss(f)$ is the common-mode to common-mode return loss at frequency f

92.10.8 Cable assembly channel operating margin

The performance of the cable assembly is evaluated using the channel operating margin (COM) procedure in 93A.1 and the parameters in Table 93–9 plus the additional PCB loss parameters. The cable assembly COM

is derived from the cable assembly scattering parameter measurements of the insertion loss of a receive lane and the four individual pair-to-pair differential NEXT losses and three individual pair-to-pair differential FEXT losses that can couple into a receive lane.

The channel insertion loss between TP0 and TP5 for the cable assembly (COM) consists of the cable assembly insertion loss measurement and an insertion loss allocation of 6.26 dB for TP0 to MDI and 6.26 dB for TP5 to MDI to account for the transmitter and receiver PCB insertion losses and the additional MDI insertion loss.

The transmitter or receiver PCB insertion losses or return losses (TP0 to MDI or TP5 to MDI) are calculated using the method defined in 93A.1.2.3. A 1 mm section of the PCB is defined by Equation (93A–9), Equation (93A–10), and the parameters values in Table 92–13. The PCB model consists of one hundred and eighty five 1 mm sections.

Table 92–13—Transmission line model parameters

Parameter	Real	Imaginary	Units
ρ_0	5.63643×10^{-4}	0	—
ρ_1	1.111×10^{-18}	2.654×10^{-3}	1/GHz
ρ_2	9.975×10^{-5}	7.218×10^{-20}	$1/GHz^2$
ρ_3	4.718×10^{-21}	2.252×10^{-6}	$1/GHz^3$
ρ_4	-4.404×10^{-8}	-4.404×10^{-8}	$1/GHz^4$
γ_0	-6.69×10^{-4}	0	—
γ_1	-5.8×10^{-4}	-1.572×10^{-4}	$1/GHz^{1/2}$
γ_2	-1.297×10^{-6}	-37.203×10^{-3}	1/GHz
γ_4	-6.78×10^{-6}	-1.514×10^{-6}	$1/GHz^2$

The channel insertion loss signal path to be used in COM (93A.1.2) is the concatenation of the cable assembly insertion loss measurement and the PCB insertion losses (derived above) using the cascade function defined in 93A.1.2.1 given in Equation (92–19).

$$S_p^{(CHILp)} = \text{cascade}(\text{cascade}(S^{(HILp)}, S^{(CAILp)}), S^{(HILp)}) \quad (92–19)$$

where

$S^{(CHILp)}$ *C*hannel insertion loss between TP0 and TP5

$S^{(HILp)}$ Insertion loss allocation of 6.26 dB for TP0 to MDI or TP5 to MDI

$S^{(CAILp)}$ Cable assembly insertion loss

The channel return loss signal path to be used in COM (93A.1.2) is the concatenation of the cable assembly return loss measurement and the PCB return losses (derived above) using the cascade function defined in

93A.1.2.1 given in Equation (92–20).

$$S_p^{(CHRLp)} = \text{cascade}(\text{cascade}(S^{(HRLp)}, S^{(CARLp)}), S^{(HRLp)}) \quad (92–20)$$

where

$S^{(CHRLp)}$ Channel return loss
$S^{(HRLp)}$ Return loss of PCB for TP0 to MDI or TP5 to MDI
$S^{(CARLp)}$ Cable assembly return loss

The channel structure includes three far-end and four near-end crosstalk paths. The MDI is the significant contributor to the channel crosstalk. The MDI crosstalk contribution is included in and characterized by the cable assembly crosstalk measurements. The cable assembly crosstalk signal paths to be used in COM (93A.1.2) are four individual pair-to-pair differential NEXT losses and three individual pair-to-pair differential FEXT losses adjusted by the PCB insertion losses (derived above) using the cascaded function defined in 93A.1.2.1 given in Equation (92–21) and Equation (92–22).

$$S_p^{(CHNXTip)} = \text{cascade}(\text{cascade}(S^{(HILp)}, S^{(CANXTip)}), S^{(HILp)}) \quad (92–21)$$

where

$S^{(CHILp)}$ Channel near-end crosstalk loss adjusted by the PCB insertion losses
$S^{(HILp)}$ Insertion loss allocation of 6.26 dB for TP0 to MDI or TP5 to MDI
$S^{(CANXTip)}$ Cable assembly near-end crosstalk loss
i is the 0 to 3 (pair-to-pair combination)

$$S_p^{(CHFXTip)} = \text{cascade}(\text{cascade}(S^{(HILp)}, S^{(CAFXTip)}), S^{(HILp)}) \quad (92–22)$$

where

$S^{(CHFXTip)}$ Channel far-end crosstalk loss adjusted by the PCB insertion losses
$S^{(HILp)}$ Insertion loss allocation of 6.26 dB for TP0 to MDI or TP5 to MDI
$S^{(CAFXTip)}$ Cable assembly far-end crosstalk loss
i is the 0 to 2 (pair-to-pair combination)

The cable assembly COM shall be greater than or equal to 4 dB.

92.10.9 Cable assembly multiple disturber near-end crosstalk (MDNEXT) loss

Since four lanes are used to transfer data between PMDs, the NEXT that is coupled into a receive lane will be from the four transmit lanes. Multiple Disturber Near-End Crosstalk (MDNEXT) loss is determined using the individual NEXT losses.

MDNEXT loss is determined from the four individual pair-to-pair differential NEXT loss values using Equation (92–23).

$$MDNEXT\_loss(f) = -10\log_{10}\left(\sum_{i=0}^{i=3} 10^{-NLi(f)/10}\right) \text{ (dB)} \quad (92\text{–}23)$$

for 0.05 GHz ≤ f ≤ 19 GHz

where

$MDNEXT\_loss(f)$ is the MDNEXT loss at frequency f
$NL_i(f)$ is the NEXT loss at frequency f of pair combination i, in dB
f is the frequency in GHz
i is the 0 to 3 (pair-to-pair combination)

92.10.10 Cable assembly multiple disturber far-end crosstalk (MDFEXT) loss

Since four lanes are used to transfer data between PMDs, the FEXT that is coupled into a data carrying lane will be from the three other lanes in the same direction. MDFEXT loss is specified using the individual FEXT losses. MDFEXT loss is determined from the three individual pair-to-pair differential FEXT loss values using Equation (92–24).

$$MDFEXT\_loss(f) = -10\log_{10}\left(\sum_{i=0}^{i=2} 10^{-NLi(f)/10}\right) \text{ (dB)} \quad (92\text{–}24)$$

for 0.05 GHz ≤ f ≤ 19 GHz

where

$MDFEXT\_loss(f)$ is the MDFEXT loss at frequency f
$NL_i(f)$ is the FEXT loss at frequency f of pair combination i, in dB
f is the frequency in GHz
i is the 0 to 2 (pair-to-pair combination)

92.10.11 Cable assembly integrated crosstalk noise (ICN)

In order to limit multiple disturber crosstalk noise at a receiver, the cable assembly integrated crosstalk noise (ICN) is specified in relationship to the measured insertion loss. ICN is calculated from the MDFEXT and MDNEXT. Given the multiple disturber near-end crosstalk loss $MDNEXT\_loss(f)$ and multiple disturber far-end crosstalk loss $MDFEXT\_loss(f)$ measured over N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 19000 MHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated crosstalk noise shall be determined using Equation (92–25) through Equation (92–29). The RMS crosstalk noise is characterized at the output of a specified receive filter utilizing a specified transmitter waveform and the measured multiple disturber crosstalk transfer functions. The transmitter and receiver filters are defined in Equation (92–25) and Equation (92–26) as weighting functions to the multiple disturber crosstalk in Equation (92–27) and Equation (92–28). The sinc function is defined by $\text{sinc}(x) = \sin(\pi x)/(\pi x)$.

Define the weight at each frequency f_n using Equation (92–25) and Equation (92–26).

$$W_{nt}(f_n) = (A_{nt}^2/f_b)\text{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{nt})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (92\text{–}25)$$

$$W_{ft}(f_n) = (A_{ft}^2/f_b)\mathrm{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{ft})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (92–26)$$

where the equation parameters are given in Table 92–14.

Note that the 3 dB transmit filter bandwidths f_{nt} and f_{ft} are inversely proportional to the 20% to 80% rise and fall times T_{nt} and T_{ft} respectively. The constant of proportionality is 0.2365 (e.g., $T_{nt}f_{nt} = 0.2365$; with f_{nt} in hertz and T_{nt} in seconds). In addition, f_r is the 3 dB reference receiver bandwidth, which is set to 18.75 GHz.

The near-end integrated crosstalk noise σ_{nx} is calculated using Equation (92–27).

$$\sigma_{nx} = \left[2\Delta f\sum_n W_{nt}(f_n)10^{-MDNEXT_{loss}(f_n)/10}\right]^{1/2} \quad (92–27)$$

The far-end integrated crosstalk noise σ_{fx} is calculated using Equation (92–28).

$$\sigma_{fx} = \left[2\Delta f\sum_n W_{ft}(f_n)10^{-MDFEXT_{loss}(f_n)/10}\right]^{1/2} \quad (92–28)$$

where Δf is the uniform frequency step of f_n.

The total integrated crosstalk noise σ_x is calculated using Equation (92–29).

$$\sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2} \quad (92–29)$$

The total integrated crosstalk noise for the cable assembly shall be computed using the parameters shown in Table 92–14.

Table 92–14—Cable assembly integrated crosstalk parameters

Description	Symbol	Value	Units
Symbol rate	f_b	25.78125	GBd
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.6	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	9.6	ps

92.11 Test Fixtures

Transmitter and receiver measurements are made at TP2 or TP3 utilizing the test fixture specified in 92.11.1. and illustrated in Figure 92–14. All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in 92.11.2 and illustrated in Figure 92–15. The test fixtures of Figure 92–14 and Figure 92–15 are specified in a mated state, illustrated in Figure 92–16, to enable connections to measurement equipment. The requirements in this section are not MDI connector specifications for an implemented design.

92.11.1 TP2 or TP3 Test fixture

The test fixture (also known as Host Compliance Board) of Figure 92–14, or its equivalent, is required for measuring the transmitter specifications in 92.8.3 at TP2 and the receiver return loss at TP3. The TP2 and TP3 test points are illustrated in Figure 92–2. Figure 92–14 illustrates the test fixture attached to TP2 or TP3.

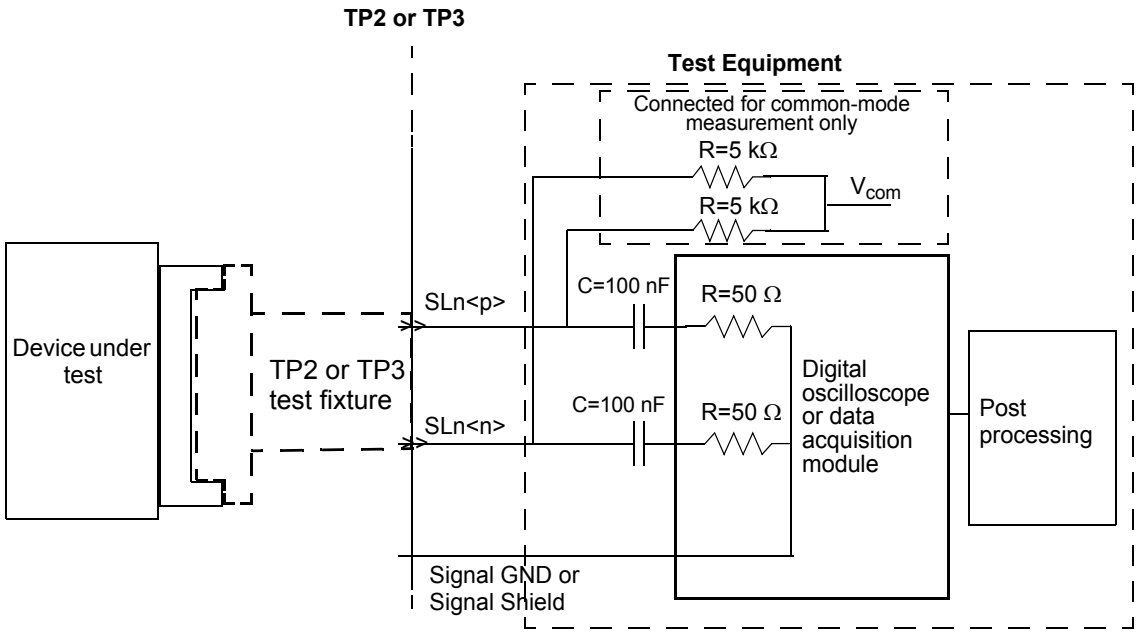


Figure 92–14—Transmitter and receiver test fixture

92.11.1.1 Test fixture return loss

The differential return loss, in dB, of the test fixture is specified in a mated state and shall meet the requirements of 92.11.3.2.

92.11.1.2 Test fixture insertion loss

The test fixture printed circuit board insertion loss values determined using Equation (92–30) shall be used as the reference test fixture insertion loss. The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

$$IL_{tfref}(f) = -0.002 + 0.192\sqrt{f} + 0.092f \text{ (dB)} \quad (92–30)$$

for $0.01 \le f \le 25$ GHz

where

f is the frequency in GHz

$IL_{tfref}(f)$ is the reference test fixture PCB insertion loss at frequency f

92.11.2 Cable assembly test fixture

The test fixture of Figure 92–15 or its equivalent, is required for measuring the cable assembly

specifications in 92.10 at TP1 and TP4. The TP1 and TP4 test points are illustrated in Figure 92–2 and Figure 92–15. The test fixture return loss is equivalent to the test fixture return loss specified in 92.11.3.2. The test fixture printed circuit board insertion loss values determined using Equation (92–31) shall be used as the reference test fixture insertion loss. The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

$$IL_{\text{catf}}(f) = -0.00125 + 0.12\sqrt{f} + 0.0575f \text{ (dB)} \quad (92\text{–}31)$$

for $0.01 \text{ GHz} \le f \le 25 \text{ GHz}$

where

f is the frequency in GHz
$IL_{\text{catf}}(f)$ is the reference test fixture printed circuit board insertion loss at frequency f

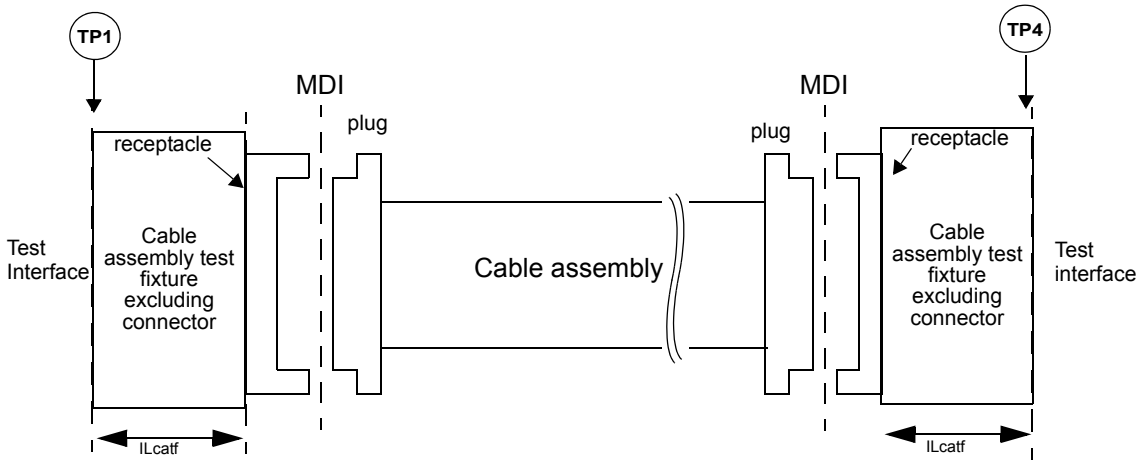


Figure 92–15—Cable assembly test fixtures

92.11.3 Mated test fixtures

The test fixtures of Figure 92–14 and Figure 92–15 are specified in a mated state illustrated in Figure 92–16.

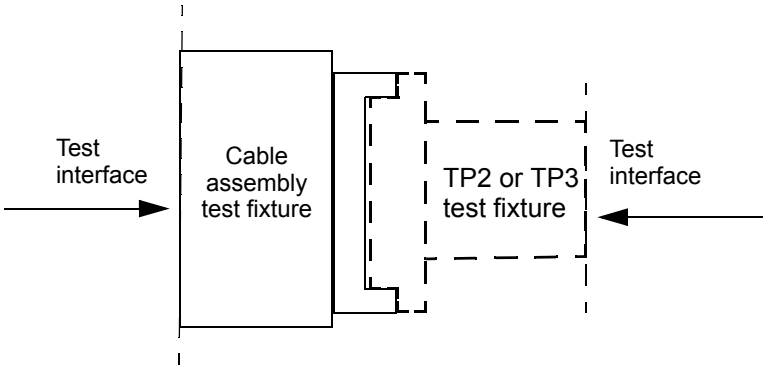


Figure 92–16—Mated test fixtures

The mated test fixtures specifications shall be verified in both directions indicated by the arrows illustrated in Figure 92–16 except insertion loss which shall be verified at either test interface illustrated in

Figure 92–16.

92.11.3.1 Mated test fixtures insertion loss

The insertion loss of the mated test fixtures shall meet the values determined using Equation (92–32) and Equation (92–33).

$$IL(f) \le IL_{MTFmax}(f) = \left\{ \begin{array}{ll} 0.12 + 0.475\sqrt{f} + 0.221f & 0.01 \le f \le 14 \\ -4.25 + 0.66f & 14 < f \le 25 \end{array} \right\} \text{ (dB)} \quad (92–32)$$

$$IL(f) \ge IL_{MTFmin}(f) = 0.08\sqrt{f} + 0.2f \quad 0.01 \le f \le 25 \text{ (dB)} \quad (92–33)$$

where

f is the frequency in GHz
$IL(f)$ is the mated test fixture insertion loss at frequency f

The mated test fixtures insertion loss limits are illustrated in Figure 92–17.

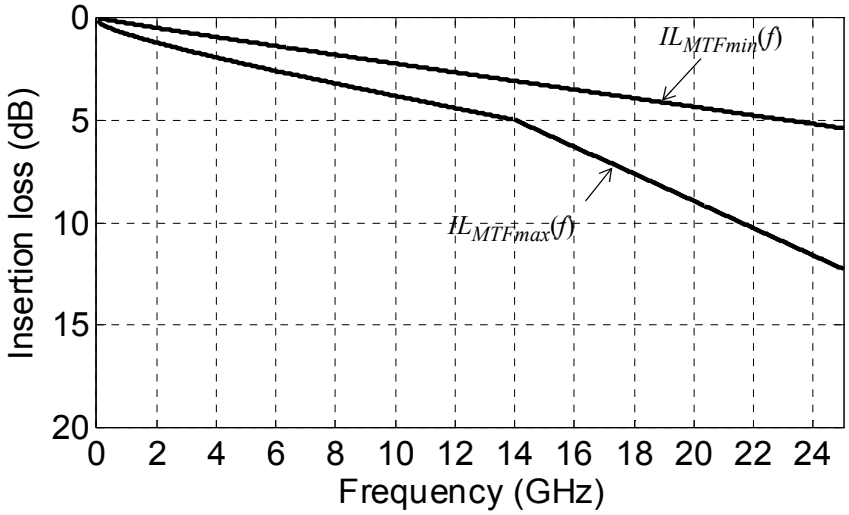


Figure 92–17—Mated test fixtures Insertion loss

92.11.3.2 Mated test fixtures return loss

The return loss of the mated test fixtures measured at each test fixture interface shall meet the values determined using Equation (92–34).

$$Return\_loss(f) \ge \left\{ \begin{array}{ll} 20 - f & 0.01 \le f < 4 \\ 18 - 0.5f & 4 \le f \le 25 \end{array} \right\} \text{ (dB)} \quad (92–34)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

The mated test fixtures return loss is illustrated in Figure 92–18.

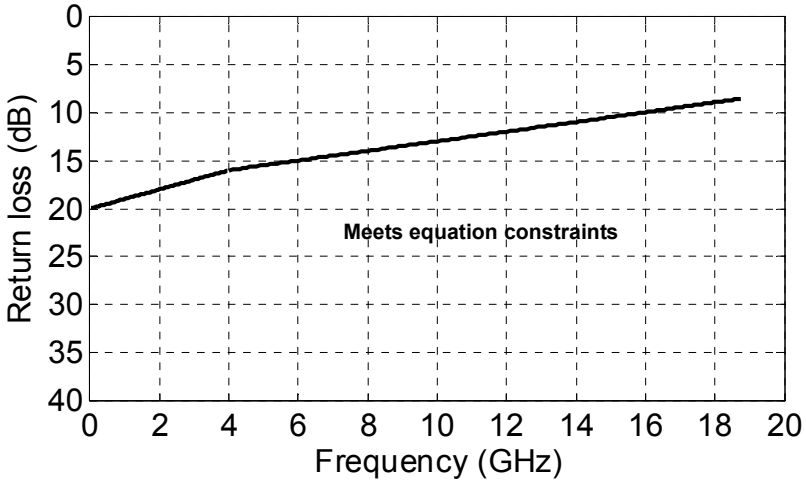


Figure 92–18—Mated test fixtures return loss

92.11.3.3 Mated test fixtures common-mode conversion insertion loss

The common-mode conversion insertion loss of the mated test fixtures measured at either test fixture test interface shall meet the values determined using Equation (92–35).

$$Conversion\_loss(f) \geq \left\{ \begin{array}{ll} 30 - 1.143f & 0.01 \leq f < 14 \\ 14 & 14 \leq f \leq 25 \end{array} \right\} \text{ (dB)} \quad (92–35)$$

where

f is the frequency in GHz
$Conversion\_loss(f)$ is the conversion insertion loss at frequency f

The mated test fixtures common-mode conversion insertion loss is illustrated in Figure 92–19.

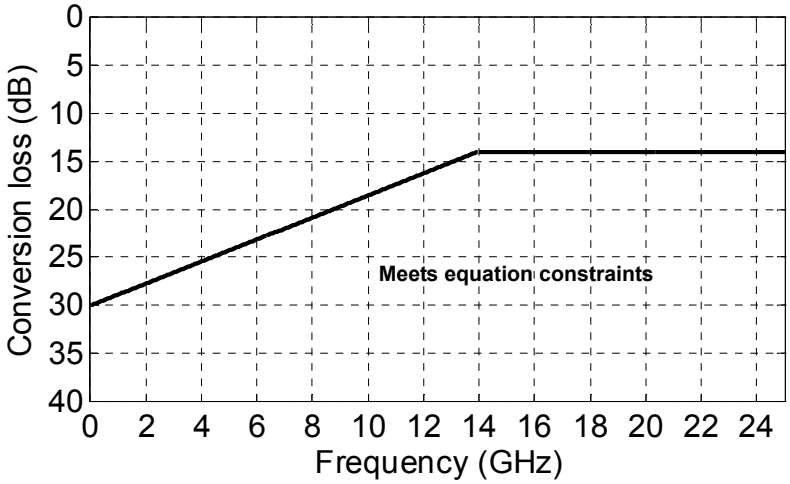


Figure 92–19—Common-mode conversion loss

92.11.3.4 Mated test fixtures common-mode return loss

The common-mode return loss of the mated test fixtures measured at each test fixture test interface shall meet the values determined using Equation (92–36).

$$Common\_mode\_return\_loss(f) \geq \left\{ \begin{array}{ll} 12 - 9f & 0.01 \leq f < 1 \\ 3 & 1 \leq f \leq 25 \end{array} \right\} \text{ (dB)} \qquad (92–36)$$

where

f is the frequency in GHz
$Common\_mode\_return\_loss(f)$ is the common-mode return loss at frequency f

The mated test fixtures common-mode return loss is illustrated in Figure 92–20.

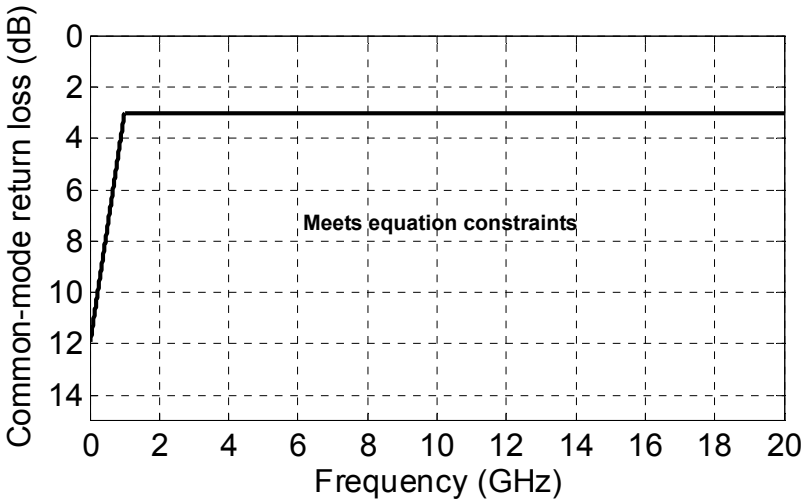


Figure 92–20—Common-mode return loss

92.11.3.5 Mated test fixtures common-mode to differential mode return loss

The common-mode to differential mode return loss of the mated test fixtures measured at each test fixture test interface shall meet the values determined using Equation (92–37).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 30 - (5/7)f & 0.01 \leq f < 14 \\ 25 - (5/14)f & 14 \leq f \leq 25 \end{array} \right\} \text{ (dB)} \qquad (92–37)$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the common-mode to differential mode return loss at frequency f

The mated test fixtures common-mode to differential mode return loss is illustrated in Figure 92–21.

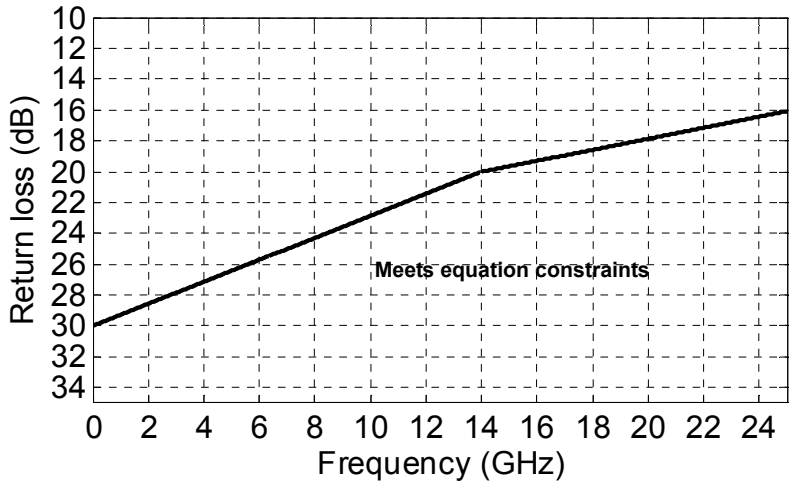


Figure 92–21—Common-mode to differential return loss

92.11.3.6 Mated test fixtures integrated crosstalk noise

The values of the mated test fixtures integrated crosstalk RMS noise voltages determined using Equation (92–25) through Equation (92–29) for the multiple disturber near-end crosstalk loss, and the multiple disturber far-end crosstalk loss shall meet the specifications in Table 92–15.

Table 92–15—Mated test fixtures integrated crosstalk noise

Parameter	100GBASE-CR4	Units
MDNEXT integrated crosstalk noise voltage	less than 1.8	mV
MDFEXT integrated crosstalk noise voltage	less than 4.8	mV

92.12 MDI specification

This subclause defines the Media Dependent Interface (MDI). The 100GBASE-CR4 PMD, as per 92.7, is coupled to the cable assembly, as per 92.10, by the MDI.

92.12.1 100GBASE-CR4 MDI connectors

Connectors meeting the requirements of 92.12.1.1 (Style-1) or 92.12.1.2 (Style-2) are used as the mechanical interface between the PMD of 92.7 and the cable assembly of 92.10. The plug connector is used on the cable assembly and the receptacle on the PHY. Style-1 or Style-2 connectors may be used as the MDI.

For Style-1 and Style 2 100GBASE-CR4 plug connectors the receive lanes are AC coupled; the AC coupling shall be within the plug connectors. It should be noted that there may be various methods for AC coupling in actual implementations. The low-frequency 3 dB cutoff of the AC coupling shall be less than 50

kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor will limit the inrush charge and baseline wander.

92.12.1.1 Style-1 100GBASE-CR4 MDI connectors

The plug connector for each end of the cable assembly shall be the QSFP+ 28 Gb/s 4X Pluggable (QSFP28) plugs defined in SFF-8665 and illustrated in Figure 92–22. The MDI connector shall be the QSFP+ 28 Gb/s 4X Pluggable (QSFP28) receptacle with the mechanical mating interface defined in SFF-8665 and illustrated in Figure 92–23. These connectors have contact assignments that are listed in Table 92–16 and electrical performance consistent with the signal quality and electrical requirements of 92.8 and 92.9.

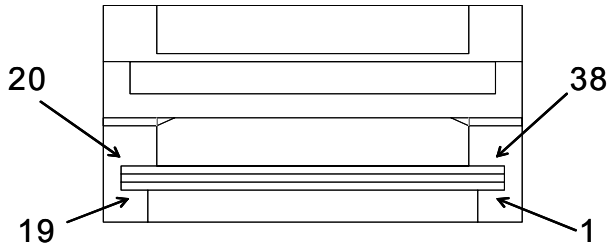


Figure 92–22—Style-1 example cable assembly

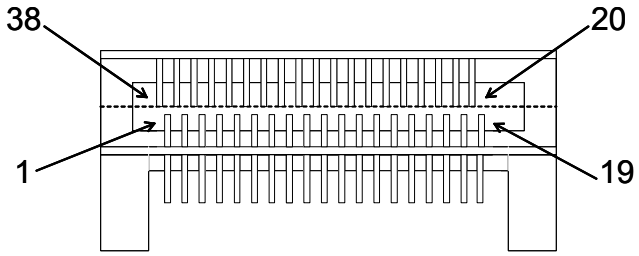


Figure 92–23—Style-1 example MDI board receptacle

The Style-1 MDI connector of the 100GBASE-CR4 PMD comprises 38 signal connections. The Style-1 100GBASE-CR4 MDI connector contact assignments shall be as defined in Table 92–16.

Table 92–16—100GBASE-CR4 lane to MDI connector contact mapping

Tx lane	MDI connector contact	Rx lane	MDI connector contact
signal gnd	S1	signal gnd	S13
SL1<n>	S2	DL2<p>	S14
SL1<p>	S3	DL2<n>	S15
signal gnd	S4	signal gnd	S16
SL3<n>	S5	DL0<p>	S17
SL3<p>	S6	DL0<n>	S18
signal gnd	S7	signal gnd	S19
SL2<p>	S33	DL1<n>	S21
SL2<n>	S34	DL1<p>	S22
signal gnd	S35	signal gnd	S23
SL0<p>	S36	DL3<n>	S24
SL0<n>	S37	DL3<p>	S25
signal gnd	S38	signal gnd	S26

92.12.1.2 Style-2 100GBASE-CR4 MDI connectors

The connector for each end of the cable assembly shall be the 100G Form Factor Pluggable 4 (CFP4) with the mechanical mating interface defined in CFP4 MSA HW Specification and illustrated in Figure 92–24. The MDI connector shall be the 100G Form Factor Pluggable (CFP4) receptacle with the mechanical mating interface defined by CFP4 MSA HW Specification and illustrated in Figure 92–25. These connectors have contact assignments that are listed in Table 92–17, and electrical performance consistent with the signal quality and electrical requirements of 92.8 and 92.9.

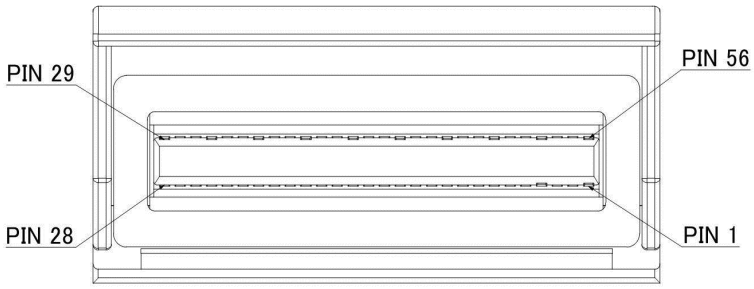


Figure 92–24—Style-2 example cable assembly

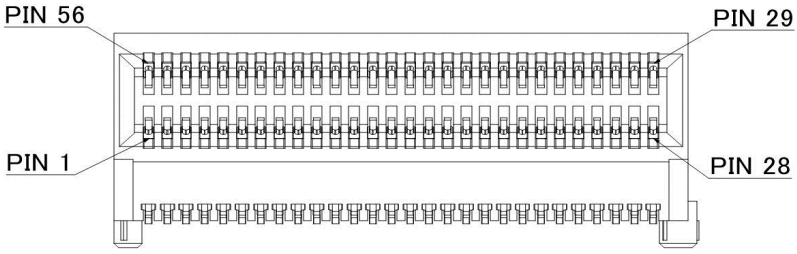


Figure 92–25—Style-2 example MDI board receptacle

The Style-2 MDI connector of the 100GBASE-CR4 PMD comprises 56 signal connections. The Style-2 100GBASE-CR4 MDI connector contact assignments shall be as defined in Table 92–17. Note that the source lanes (SL), signals SLi<p>, and SLi<n> are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals, DLi<p>, and DLi<n> are the positive and negative sides of the receivers differential signal pairs for lane i (i = 0, 1, 2, 3).

Table 92–17—100GBASE-CR4 lane to MDI connector contact mapping

Tx lanes	MDI connector contact	Rx lanes	MDI connector contact
signal gnd	44	signal gnd	29
SL0<p>	45	DL0<p>	30
SL0<n>	46	DL0<n>	31
signal gnd	47	signal gnd	32
SL1<p>	48	DL1<p>	33
SL1<n>	49	DL1<n>	34
signal gnd	50	signal gnd	35
SL2<p>	51	DL2<p>	36
SL2<n>	52	DL2<n>	37
signal gnd	53	signal gnd	38
SL3<p>	54	DL3<p>	39
SL3<n>	55	DL3<n>	40
signal gnd	56	signal gnd	41

92.13 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

92.14 Protocol implementation conformance statement (PICS) proforma for Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4[11]

92.14.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

92.14.2 Identification

92.14.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

92.14.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bj-20XX, Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bj-20XX.)	

Date of Statement	

[11] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

92.14.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
CGMII	CGMII	92.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100GBASE-R PCS	92.1		M	Yes [ ]
RS-FEC	100GBASE-R RS-FEC	92.1		M	Yes [ ]
PMA	100GBASE-R PMA	92.1		M	Yes [ ]
CAUI	CAUI	92.1	Interface is supported	O	Yes [ ] No [ ]
CR4	100GBASE-CR4 PMD	92.1	Can operate as 100GBASE-CR4 PMD	M	Yes [ ]
AN	Auto-negotiation	92.1	Device implements Auto-Negotiation	M	Yes [ ]
DC	Delay constraints	92.4	Device conforms to delay constraints specified in 92.4	M	Yes [ ]
DSC	Skew constraints	92.5	Device conforms to Skew and Skew Variation constraints specified in 92.5	M	Yes [ ]
*MD	MDIO capability	92.6	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE deep sleep capability	92.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	92.7.6	Function is supported	EEE:M	Yes [ ] No [ ]
*LTD	PMD lane-by-lane transmit disable function	92.7.7	Function is supported	O	Yes [ ] No [ ]
*CBL	Cable assembly	92.10	Items marked with CBL include cable assembly specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CAST1	100GBASE-CR4 Style-1 cable assembly	92.10	Cable assembly supports 100GBASE-CR4 Style-1	CBL:O.1	Yes [ ] No [ ]
CAST2	100GBASE-CR4 Style-2 cable assembly	92.10	Cable assembly supports 100GBASE-CR4 Style-2	CBL:O.1	Yes [ ] No [ ]
MDIST1	Style-1 MDI connector	92.12.1.1	100GBASE-CR4 device uses Style-1 MDI	O:2	Yes [ ] N/A [ ]
MDIST2	Style-2 MDI connector	92.12.1.2	100GBASE-CR4 device uses Style-2 MDI	O:2	Yes [ ] N/A [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

92.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4

92.14.4.1 PMD functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
PF1	Transmit function	92.7.2	Converts four logical bit streams from the PMD service interface into four electrical signals and delivers them to the MDI	M	Yes [ ]
PF2	Transmitter signal	92.7.2	A positive differential voltage corresponds to tx_bit = one	M	Yes [ ]
PF3	ALERT signal	92.7.2	Transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane when tx_mode is set to ALERT	EEE:M	Yes [ ] N/A [ ]
PF4	Receive function	92.7.3	Converts four electrical signals from the MDI into four logical bit streams delivers them to the PMD service interface	M	Yes [ ]
PF5	Receiver signal	92.7.3	A positive differential voltage corresponds to rx_bit = one	M	Yes [ ]
PF6	Training disabled by management	92.7.5	PMD_signal_detect_*i* set to one for *i*=0 to 3	M	Yes [ ]
PF7	PMD_signal_detect_*i* asserted, rx_mode=QUIET	92.7.5	Set to one within 500 ns following the application of the signal defined in 92.7.5 to the input of the channel corresponding to the receiver of lane *i*	EEE:M	Yes [ ]
PF8	PMD_signal_detect_*i* not asserted, rx_mode=QUIET	92.7.5	Not set to one when the signal applied to the input of the channel corresponding to the receiver of lane *i* is less than or equal to 70 mV peak-to-peak differential	EEE:M	Yes [ ]
PF9	Global_PMD_transmit_disable	92.7.6	Disables all transmitters by forcing a constant output level	GTD:M	Yes [ ] N/A [ ]
PF10	Global_PMD_transmit_disable affect on loopback	92.7.6	No effect	GTD:M	Yes [ ] N/A [ ]
PF11	Global PMD transmit disable function, tx_mode transition to QUIET	92.7.6	Turn off all transmitters when tx_mode transitions to QUIET from any other value	EEE:M	Yes [ ] N/A [ ]
PF12	Global PMD transmit disable function, tx_mode transition from QUIET	92.7.6	Turn on all transmitters when tx_mode transitions from QUIET to any other value	EEE:M	Yes [ ] N/A [ ]

Item	Feature	Sub clause	Value/Comment	Status	Support
PF13	PMD_transmit_disable_*i* variable	92.7.7	When set to one, the transmitter for lane *i* satisfies the requirements of Table 92–6	LTD:M	Yes [ ] N/A [ ]
PF14	PMD lane-by-lane transmit disable function affect on loopback	92.7.7	No effect	LTD:M	Yes [ ] N/A [ ]
PF15	PMD_fault variable mapping to MDIO	92.7.9	Mapped to the fault bit as specified in 45.2.1.2.1	MD:M	Yes [ ] N/A [ ]
PF16	PMD_transmit_fault variable mapping to MDIO	92.7.10	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
PF17	PMD_receive_fault variable mapping to MDIO	92.7.11	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
PF18	PMD control function	92.7.12	Defined in 72.6.10	M	Yes [ ]
PF19	Training frame structure	92.7.12	Defined in 72.6.10 but adjusted for 100GBASE-CR4 signaling rate and use of uncorrelated training patterns	M	Yes [ ]
PF20	Training pattern	92.7.12	4094 bits from the output of a pseudo-random bit sequence (PRBS) generator defined in Table 92–5 followed by two zeros	M	Yes [ ]
PF21	Training pattern seed	92.7.12	Set to the value in Table 92–5 at the start of the training pattern	M	Yes [ ]
PF22	PMD control function variable mapping	92.7.12	Map variables to the appropriate bits as specified in 45.2.1.80	MD:M	Yes [ ] N/A [ ]

92.14.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Global_PMD_signal_detect	92.7.4	Set to the value described in 45.2.1.9.7	O	Yes [ ]
MF2	Global_PMD_signal_detect	92.7.4	Set defined by the training state diagram in Figure 72–5	O	Yes [ ] No [ ]
MF3	Lane-by-Lane Signal Detect function	92.7.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 92.7.5	MD:M	Yes [ ] N/A [ ]
MF4	Lane-by-Lane Signal Detect function	92.7.5	If training is disabled by management, PMD_signal_detect_*i* shall be set to one for i=0 to 3.	MD:M	Yes [ ] N/A [ ]
MF5	Lane-by-Lane Signal Detect function	92.7.5	If the optional EEE capability is supported, apply optional requirements as specified in 92.7.5.	O	Yes [ ] N/A [ ]
MF6	Global_PMD_transmit_disable	92.7.6	If the optional EEE capability is supported, apply optional requirements as specified 92.7.6.	O	Yes [ ]
MF7	PMD_fault function	92.7.9	Mapped to the fault bit as specified in 45.2.1.2.1	MD:M	Yes [ ] N/A [ ]
MF8	PMD_transmit_fault function	92.7.10	Mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF9	PMD_receive_fault function	92.7.11	Contributes to the PMA/PMD receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
MF10	PMD_receive_fault function	92.7.11	Contributes to the PMA/PMD receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
MF11	PMD control function	92.7.12	Each lane shall use the same control function as 10GBASE-KR, as defined in 72.6.10.	MD:M	Yes [ ] N/A [ ]
MF12	PMD control response time	92.7.12	Response time less than 2 ms.	M	Yes [ ]

92.14.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture return loss	92.11.1.1	Meets equation constraints	M	Yes [ ]
TC2	Test fixture insertion loss	92.11.1.2	Meets equation constraints	M	Yes [ ]
TC3	Signaling rate per lane	92.8.3.10	25.78125 GBd ± 100 ppm	M	Yes [ ]
TC4	Peak-to-peak differential output voltage	92.8.3.1	Less than or equal to 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC5	Peak-to-peak differential output voltage, transmitter disabled	92.8.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC6	DC common-mode output voltage	92.8.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC7	AC common-mode output voltage	92.8.3.1	Less than or equal to 30 mV RMS with respect to signal ground	M	Yes [ ]
TC8	The peak-to-peak differential output voltage	92.8.3.1	If the optional EEE capability is supported, less than 30 mV within 500 ns of the transmitter being disabled.	EEE:M	Yes [ ]
TC9	The peak-to-peak differential output voltage	92.8.3.1	If the optional EEE capability is supported, when the transmitter is disabled, the peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of the transmitter being enabled .	EEE:M	Yes [ ]
TC10	The peak-to-peak differential output voltage	92.8.3.1	If the optional EEE deep sleep capability is supported, when the transmitter is disabled, it shall meet the requirements of 92.8.3 within 1 μs of the transmitter being enabled.	EEE:M	Yes [ ]
TC11	The peak-to-peak differential output voltage	92.8.3.1	If the optional EEE deep sleep capability is supported, when the transmitter is disabled, the DC common-mode output voltage shall be maintained to within +/-150 mV of the value for the enabled transmitter.	EEE:M	Yes [ ]
TC12	Common-mode output voltage requirements	92.8.3.1	Met regardless of the transmit equalizer setting	M	Yes [ ]
TC13	Differential output return loss (min)	92.8.3.2	Meets equation constraints	M	Yes [ ]
TC14	Reference impedance for differential return loss measurements	92.8.3.2	100 Ω	M	

Item	Feature	Subclause	Value/Comment	Status	Support
TC15	Common-mode to differential mode output return loss	92.8.3.3	Meets equation constraints	M	Yes [ ]
TC16	Steady-state voltage, v_f	92.8.3.7.1	0.34 min, 0.6 max	M	Yes [ ]
TC17	Linear fit pulse peak (min)	92.8.3.7.1	$0.52 \times v_f$	M	Yes [ ]
TC18	Normalized linear fit error (max)	92.8.3.7.2	0.037	M	Yes [ ]
TC19	Coefficient initialization	92.8.3.7.3	Satisfies the requirements of 92.8.3.7.3.	M	Yes [ ]
TC20	Normalized coefficient step size for “increment”	92.8.3.7.4	Between 0.0083 and 0.05	M	Yes [ ]
TC21	Normalized coefficient step size for “decrement”	92.8.3.7.4	Between –0.05 and –0.0083	M	Yes [ ]
TC22	Maximum post-cursor equalization ratio	92.8.3.7.5	Greater than or equal to 4	M	Yes [ ]
TC23	Maximum pre-cursor equalization ratio	92.8.3.7.5	Greater than or equal to 1.54	M	Yes [ ]
TC24	Transmitter far-end output noise, low-loss channel	92.8.3.6	Less than or equal to 2 mV RMS	M	Yes [ ]
TC25	Transmitter far-end output noise, high-loss channel	92.8.3.6	Less than or equal to 1 mV RMS	M	Yes [ ]
TC26	Even-odd jitter	92.8.3.9	Less than or equal to 0.035 UI regardless of the transmit equalization setting	M	Yes [ ]
TC27	The total jitter, excluding data dependent jitter	92.8.3.9	less than or equal to 0.28 UI regardless of the transmit equalization setting	M	Yes [ ]
TC28	Effective random jitter	92.8.3.9	Shall be less than or equal to 0.15 UI regardless of the transmit equalization setting	M	Yes [ ]

92.14.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture return loss	92.11.1.1	Meets the requirements of 92.11.3.2	M	Yes [ ]
RC2	Test fixture insertion loss	92.11.1.2	Meets equation constraints	M	Yes [ ]
RC3	Receiver input amplitude tolerance	92.8.4.1	1200 mV measured at TP2	M	Yes [ ]
RC4	Differential input return loss	92.8.4.2	Meets equation constraints	M	Yes [ ]
RC5	Reference impedance for differential return loss measurements	92.8.4.2	100 Ω	M	Yes [ ]
RC6	Common-mode input return loss	92.8.4.3	Meets equation constraints	M	Yes [ ]
RC7	Interference tolerance	92.8.4.4	Satisfy requirements summarized in Table 92–9	M	Yes [ ]
RC8	Interference tolerance	92.8.4.4.4	Pattern generator output amplitude	M	Yes [ ]
RC9	Interference tolerance	92.8.4.4.4	Pattern generator jitter specification	M	Yes [ ]
RC10	Receiver jitter tolerance	92.8.4.5	BER less than or equal to 10^{-5} for each case listed in Table 92–10	M	Yes [ ]
RC11	Signaling rate, per lane	92.8.4.6	25.78125 GBd ± 100 ppm	M	Yes [ ]

92.14.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	92.10.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Insertion loss	92.10.2	Per Equation (92–10) and Table 92–12	CBL:M	Yes [ ] N/A [ ]
CA3	Return loss	92.10.4	Per Equation (92–15)	CBL:M	Yes [ ] N/A [ ]
CA4	Differential to common-mode input and output return loss	92.10.5	Per Equation (92–16)	CBL:M	Yes [ ] N/A [ ]
CA5	Differential to common-mode conversion loss	92.10.6	Per Equation (92–17)	CBL:M	Yes [ ] N/A [ ]
CA6	Common-mode to common-mode return loss	92.10.7	Per Equation (92–18)	CBL:M	Yes [ ] N/A [ ]
CA7	Cable assembly COM.	92.10.8	Greater than 4 dB.	CBL:M	Yes [ ] N/A [ ]
CA8	Test fixture reference printed circuit board insertion loss	92.11.2	Per Equation (92–31)	CBL:M	Yes [ ] N/A [ ]
CA9	Mated test fixture specifications	92.11.3	Verified in both directions illustrated in Figure 92–16 except insertion loss verified at either test interface in directions illustrated in Figure 92–16.	CBL:M	Yes [ ] N/A [ ]
CA10	Mated test fixture insertion loss	92.11.3.1	Per Equation (92–32) and Equation (92–33)	CBL:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CA11	Mated test fixture return loss	92.11.3.2	Per Equation (92–34)	CBL:M	Yes [ ] N/A [ ]
CA12	Mated test fixture common-mode conversion loss	92.11.3.3	Per Equation (92–35)	CBL:M	Yes [ ] N/A [ ]
CA13	Mated test fixture common-mode return loss	92.11.3.4	Per Equation (92–36)	CBL:M	Yes [ ] N/A [ ]
CA14	Mated test fixture common-mode to differential mode return loss	92.11.3.5	Per Equation (92–37)	CBL:M	Yes [ ] N/A [ ]
CA15	Mated test fixtures integrated crosstalk noise	92.11.3.6	Per Equation (92–25), through Equation (92–29) and Table 92–15	CBL:M	Yes [ ] N/A [ ]
CA16	Cable assembly connector type	92.12.1.1	100GBASE-CR4 Style-1 plug (SFF-8665 plug)	CAST1:M	Yes [ ] N/A [ ]
CA17	Pin assignments	92.12.1.1	Per Table 92–16	CAST1:M	Yes [ ] N/A [ ]
CA18	Cable assembly connector type	92.12.1.2	100GBASE-CR4 Style-2 plug (CFP4)	CAST2:M	Yes [ ] N/A [ ]
CA19	Pin assignments	92.12.1.2	Per Table 92–17	CAST2:M	Yes [ ] N/A [ ]
CA20	AC coupling	92.12.1	3 dB cutoff	CBL:M	Yes [ ]

92.14.4.6 MDI connector specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDC1	MDI connector type	92.12.1.1	100GBASE-CR4 Style-1 receptacle (SFF-8665 receptacle)	MDIST1:M	Yes [ ] N/A [ ]
MDC2	MDI connector type	92.12.1.2	100GBASE-CR4 Style-2 receptacle (CFP4 receptacle)	MDIST2:M	Yes [ ]

92.14.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	92.13		M	Yes [ ]

93. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4

93.1 Overview

This clause specifies the 100GBASE-KR4 PMD and baseband medium. There are two associated annexes. Annex 93A defines characteristics of electrical backplanes and Annex 93B extends the electrical backplane reference model with additional informative test points.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 93–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 93–1—Physical Layer clauses associated with the 100GBASE-KR4 PMD

Associated clause	100GBASE-KR4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R[b]	Required
83A—CAUI	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]There are limitations on the number of PMA lanes that may be used between sublayers, see 83.3.

A 100GBASE-KR4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

Figure 93–1 shows the relationship of the 100GBASE-KR4 PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

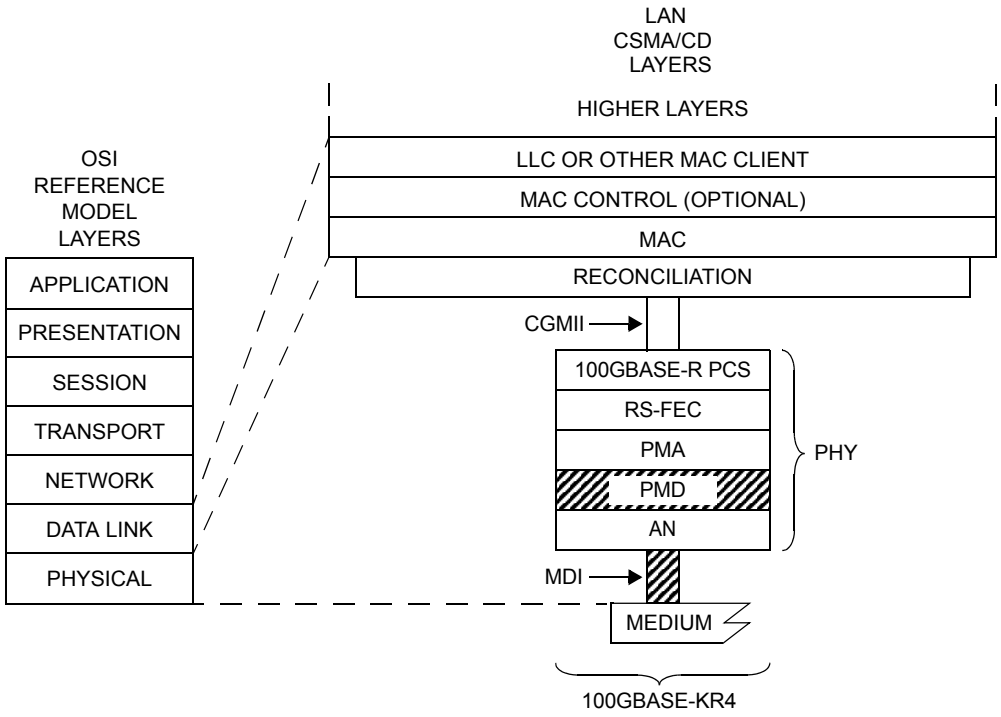


Figure 93–1—100GBASE-KR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The receive path of the RS-FEC sublayer may have the option to perform error detection without correction to reduce the data delay (see 91.5.3.3). When the receive path of the RS-FEC sublayer performs error correction, the link is required to operate with a BER of 10^{-5} or better. When the RS-FEC sublayer is configured to bypass error correction, the link is required to operate with a BER of 10^{-12} or better. In this context, a link consists of a compliant PMD transmitter, a compliant PMD receiver, and a channel meeting the requirements of 93.9.1.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.210a) of less than 1.7×10^{-10} for 64-octet frames with minimum inter-packet gap.

93.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-KR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-KR4 PMD has four parallel bit streams, hence $i = 0$ to 3. The PMA (or the PMD) continuously sends four parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 93.7.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_*i*.indication parameters are undefined.

If the optional EEE capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

93.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 100GBASE-KR4 PHY may be extended using CAUI as a physical instantiation of the inter-sublayer service interface between devices. If CAUI is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

93.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 100GBASE-KR4 PMD, AN, and the medium in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). It is assumed that the one way delay through the medium is no more than 800 bit times (8 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

93.5 Skew constraints

The Skew (relative delay) between the lanes must be kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–4 and Figure 80–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

93.6 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 93–2, and MDIO status bits to PMD status variables as shown in Table 93–3.

Table 93–2—100GBASE-KR4 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3	PMD training pattern 3	1.1453.12:11	polynomial_3
Seed 3	PMD training pattern 3	1.1453.10:0	seed_3
Polynomial identifier 2	PMD training pattern 2	1.1452.12:11	polynomial_2
Seed 2	PMD training pattern 2	1.1452.10:0	seed_2
Polynomial identifier 1	PMD training pattern 1	1.1451.12:11	polynomial_1
Seed 1	PMD training pattern 1	1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern 0	1.1450.12:11	polynomial_0
Seed 0	PMD training pattern 0	1.1450.10:0	seed_0

Table 93–3—100GBASE-KR4 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0
Receiver status 3	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status	1.151.13	frame_lock_3
Start-up protocol status 3	BASE-R PMD status	1.151.14	training_3
Training failure 3	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status	1.151.9	frame_lock_2
Start-up protocol status 2	BASE-R PMD status	1.151.10	training_2
Training failure 2	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status	1.151.5	frame_lock_1
Start-up protocol status 1	BASE-R PMD status	1.151.6	training_1
Training failure 1	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock_0
Start-up protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0

93.7 PMD functional specifications

93.7.1 Link block diagram

One direction for one lane of a 100GBASE-KR4 link is shown in Figure 93–2.

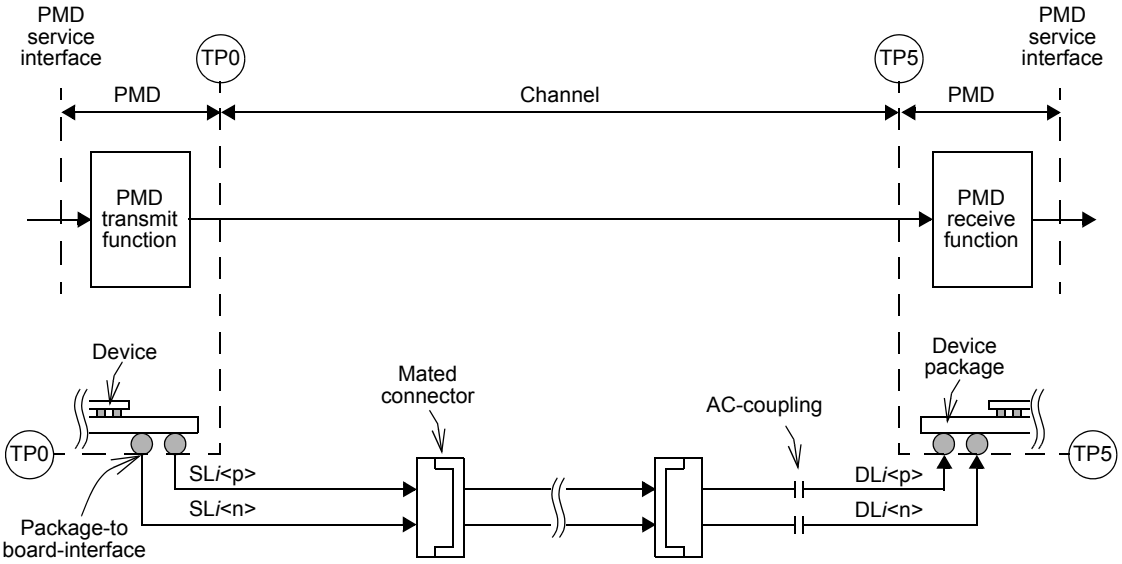


Figure 93–2—100GBASE-KR4 link (one direction for one lane is illustrated)

93.7.2 PMD Transmit function

The PMD transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request (*i*=0 to 3) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 93.8.1. A positive differential output voltage (SL*i*<p> minus SL*i*<n>) shall correspond to tx_bit = one.

If the optional EEE capability is supported, the following requirements apply. When tx_mode is set to ALERT, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane, with the transmit equalizer coefficients set to the preset values (see 93.7.12 and 93.8.1.6). When tx_mode is not set to ALERT, the transmit equalizer coefficients are set to the values determined via the start-up protocol (see 93.7.12).

93.7.3 PMD Receive function

The PMD receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication (*i*=0 to 3). A positive differential input voltage (DL*i*<p> minus DL*i*<n>) shall correspond to rx_bit = one.

93.7.4 Global PMD signal detect function

The variable Global_PMD_signal_detect is the logical AND of the values of PMD_signal_detect_*i* for *i*=0 to 3.

When the MDIO is implemented, this function maps the variable Global_PMD_signal_detect to the register and bit defined in 93.6.

93.7.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the 100GBASE-KR4 PMD to indicate the successful completion of the start-up protocol by the PMD control function (see 93.7.12). PMD_signal_detect_*i* (where *i* represents the lane number in the range 0 to 3) is set to zero when the value of the variable signal_detect is set to false by the Training state diagram for lane *i* (see Figure 72–5). PMD_signal_detect_*i* is set to one when the value of signal_detect for lane *i* is set to true.

If training is disabled by the management variable mr_training_enable (see 93.6), PMD_signal_detect_*i* shall be set to one for *i*=0 to 3.

If the optional EEE capability is supported, the following requirements apply. The value of PMD_signal_detect_*i* (for *i*=0 to 3) is set to zero when rx_mode is first set to QUIET. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall be set to one within 500 ns of the application of the ALERT pattern defined in 93.7.2, with peak-to-peak differential voltage of 720 mV as measured at TP0a, to the differential pair at the input of the channel that connects the transmitter to the receiver of lane *i*. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall not be set to one when the voltage applied to the input of the differential pair of the channel that connects the transmitter to the receiver of lane *i* is less than or equal to 60 mV peak-to-peak differential.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 93.6.

93.7.6 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if the EEE deep sleep capability is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 93–4.
b) If a PMD fault (93.7.9) is detected, then the PMD may set Global_PMD_transmit_disable to one.
c) Loopback, as defined in 93.7.8, shall not be affected by Global_PMD_transmit_disable.
d) The following additional requirements apply when the optional EEE capability is supported. The Global PMD transmit disable function shall turn off all of the transmitters as specified in 93.8.1.3 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on all of the transmitters as specified in 93.8.1.3 when tx_mode transitions from QUIET to any other value.

93.7.7 PMD lane-by-lane transmit disable function

The PMD transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0 to 3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 93–4.
b) If a PMD fault (93.7.9) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the electrical transmitter in each lane.
c) Loopback, as defined in 93.7.8, shall not be affected by PMD_transmit_disable_*i*.

93.7.8 Loopback mode

Local loopback mode is provided by the adjacent PMA (see 83.5.8) as a test function to the device. When loopback mode is enabled, transmission requests passed to each transmitter are sent directly to the corresponding receiver, overriding any signal detected by each receiver on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

Control of the loopback function is specified in 83.5.8.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

93.7.9 PMD fault function

PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.1.

93.7.10 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

93.7.11 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit specified in 45.2.1.7.5.

93.7.12 PMD control function

Each lane of the 100GBASE-KR4 PMD shall use the same control function as 10GBASE-KR, as defined in 72.6.10. The training frame structure used by the 100GBASE-KR4 PMD control function shall be as defined in 72.6.10 with the exception that 25.78125 GBd symbols replace 10.3125 GBd symbols and 100GBASE-KR4 UI replace 10GBASE-KR UI.

In addition to the coefficient update process specified in 72.6.10.2.5, when frame_lock_*i* is TRUE for lane *i* (where *i* represents the lane number in the range 0 to 3), the period from receiving a new request to responding to that request shall be less than 2 ms. The start of the period is the frame marker of the training frame with the new request and the end of the period is the frame marker of the training frame with the corresponding response. A new request occurs when the coefficient update field is different from the coefficient field in the preceding frame. The response occurs when the coefficient status report field is updated to indicate that the corresponding action is complete.

In addition, the training pattern defined in 72.6.10.2.6 is replaced with the set of training patterns defined in 92.7.12 which are designed to minimize the correlation between physical lanes.

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1.

If the MDIO interface is implemented, then this function shall map these variables to the appropriate bits in the BASE-R PMD status register (Register 1.151) as specified in 45.2.1.80.

93.8 100GBASE-KR4 electrical characteristics

93.8.1 Transmitter characteristics

Transmitter characteristics measured at TP0a are summarized in Table 93–4.

93.8.1.1 Transmitter test fixture

Unless otherwise noted, measurements of the transmitter are made at the output of a test fixture (TP0a) as shown in Figure 93–4.

The insertion loss of the test fixture shall be between 1.2 dB and 1.6 dB at 12.89 GHz. The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.1 dB from 0.05 to 13 GHz.

The differential return loss of the test fixture, in dB, shall meet Equation (93–1) where *f* is the frequency in GHz.

$$RL_d(f) \geq \begin{cases} 20 - f & 0.05 \leq f \leq 5 \\ 15 & 5 < f \leq 13 \\ 20.57 - 0.4286f & 13 < f \leq 25 \end{cases} \text{ dB} \qquad (93\text{–}1)$$

The return loss limit is illustrated by Figure 93–3.

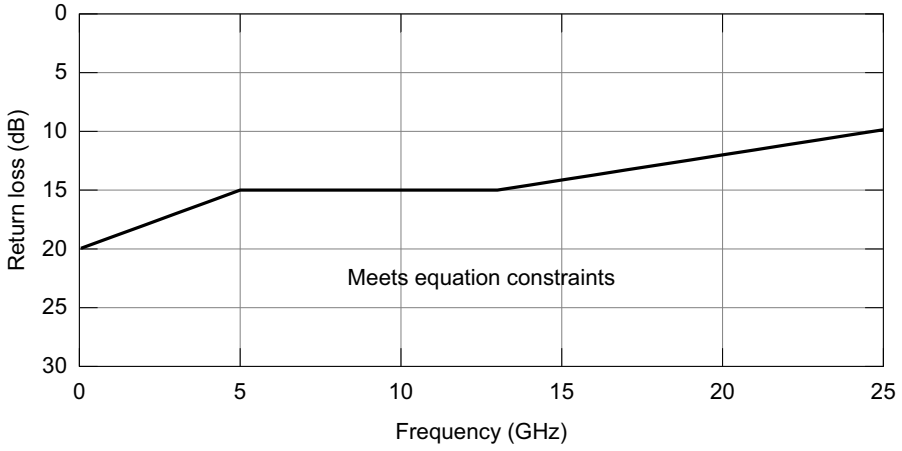


Figure 93–3—Test fixture differential return loss limit

Table 93–4—Summary of transmitter characteristics at TP0a

Parameter	Subclause reference	Value	Units
Signaling rate	93.8.1.2	25.78125±100 ppm	GBd
Differential peak-to-peak output voltage (max.) Transmitter disabled[a] Transmitter enabled	93.8.1.3	 30 1200	 mV mV
DC common-mode output voltage (max.)	93.8.1.3	1.9	V
DC common-mode output voltage (min.)	93.8.1.3	0	V
AC common-mode output voltage (RMS, max.)	93.8.1.3	12	mV
Differential output return loss (min.)	93.8.1.4	Equation (93–2)	dB
Common-mode output return loss (min.)	93.8.1.4	Equation (93–3)	dB
Transition time (20-80%, min.), no equalization[b]	93.8.1.5	8	ps
Output waveform Steady-state voltage v_f(max.) Steady-state voltage v_f(min.) Linear fit pulse peak (min.) Normalized RMS linear fit error (max.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	93.8.1.6	 0.6 0.4 0.8 × v_f 0.037 0.0083 0.05 1.54 4	 V V V — — — — —
Far-end output noise (max.) Low insertion loss channel High insertion loss channel	93.8.1.7	 2 1	 mV mV
Output jitter (max.) Even-odd jitter Effective deterministic jitter excluding data dependent jitter Effective random jitter Total jitter excluding data dependent jitter	93.8.1.8	 0.035 0.15 0.15 0.28	 UI UI UI UI

[a]The transmitter for lane *i* is disabled when either Global_PMD_transmit_disable or PMD_transmit_disable_*i* is set to one.
[b]Transmit equalization may be disabled by asserting the preset control defined in Table 45–60 and 45.2.1.81.3.

The common-mode return loss of the test fixture shall be greater than or equal to 10 dB from 0.05 to 13 GHz.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

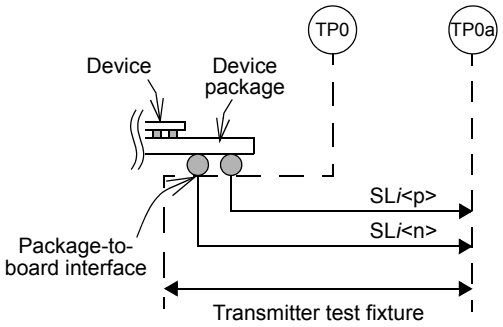


Figure 93–4—Transmitter test fixture and test points

93.8.1.2 Signaling rate and range

The 100GBASE-KR4 signaling rate shall be 25.78125 GBd ± 100 ppm per lane.

93.8.1.3 Signal levels

The differential output voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode output voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 93–5.

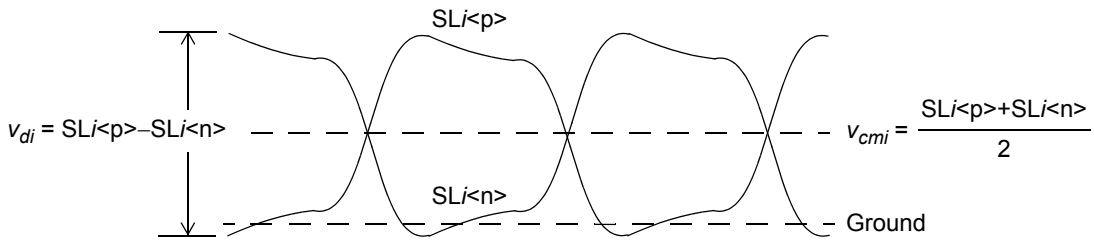


Figure 93–5—Transmitter output voltage definitions

The peak-to-peak differential output voltage shall be less than or equal to 1200 mV regardless of the transmit equalizer setting. The peak-to-peak differential output voltage shall be less than or equal to 30 mV when the transmitter is disabled (refer to 93.7.6 and 93.7.7).

The DC common-mode output voltage shall be between 0 V and 1.9 V with respect to signal ground. The AC common-mode output voltage shall be less than or equal to 12 mV RMS with respect to signal ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

If the optional EEE capability is supported the following requirements also apply. The peak-to-peak differential output voltage shall be less than 30 mV within 500 ns of the transmitter being disabled. When the transmitter is disabled, the peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of the transmitter being enabled. The transmitter is enabled by the assertion of tx_mode=ALERT and the preceding requirement applies when the transmitted symbols are the periodic pattern defined in 93.7.2 and the transmitter equalizer coefficients are assigned their preset values. The transmitter shall meet the requirements of 93.8.1 within 1 μs of the transmitter being enabled. When the transmitter is disabled, the DC common-mode output voltage shall be maintained to within ±150 mV of the value for the enabled transmitter.

Differential and common-mode signal levels are measured with a PRBS9 test pattern.

93.8.1.4 Transmitter output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (93–2) where f is the frequency in GHz. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω

$$RL_d(f) \geq \begin{cases} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.45 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB} \quad (93\text{–}2)$$

The return loss limit is illustrated by Figure 93–6.

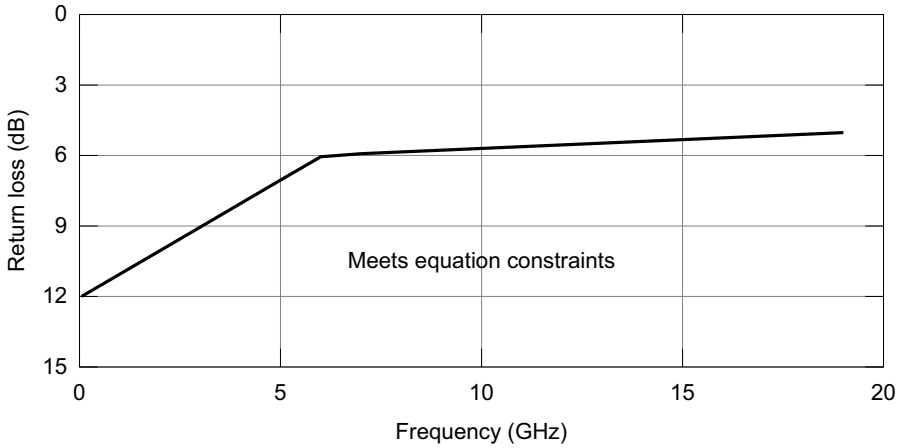


Figure 93–6—Differential return loss limit

The common-mode output return loss, in dB, of the transmitter shall meet Equation (93–3) where f is the frequency in GHz. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL_{cm}(f) \geq 6 \text{ dB}, \ 0.05 \leq f \leq 19 \text{ GHz} \quad (93\text{–}3)$$

93.8.1.5 Transition time

Transition times (rise and fall times) are defined in 86A.5.3.3. The transition times shall be greater than or equal to 8 ps when transmit equalization is disabled. Transmit equalization may be disabled by asserting the preset control defined in Table 45–60 and 45.2.1.81.3.

93.8.1.6 Transmitter output waveform

The 100GBASE-KR4 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for

the transmit equalizer is the three tap transversal filter shown in Figure 93–7.

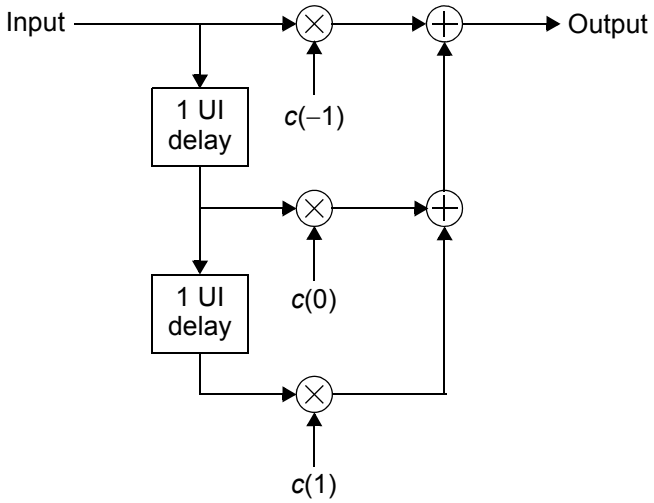


Figure 93–7—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 93.7.12 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

This command set includes instructions to:

Increment coefficient $c(i)$.
Decrement coefficient $c(i)$.
Hold coefficient $c(i)$ at its current value.
Set the coefficients to a pre-defined value (preset or initialize).

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that:

The requested update to coefficient $c(i)$ has completed (updated).
Coefficient $c(i)$ is at its minimum value.
Coefficient $c(i)$ is at its maximum value.
Coefficient $c(i)$ is ready for the next update request (not_updated).

The transmitter output waveform is characterized using the procedure described in 85.8.3.3. The parameters of the linear pulse fit and equalizer are summarized in Table 93–5.

Table 93–5—Linear fit pulse and equalizer parameters

Description	Symbol	Value	Units
Linear fit pulse length	N_p	8	UI
Linear fit pulse delay	D_p	2	UI
Equalizer length	N_w	8	UI
Equalizer delay	D_w	2	UI

93.8.1.6.1 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M (refer to 85.8.3.3 step 3). The steady-state voltage shall be greater than or equal to 0.4 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the "preset" values.

The peak value of $p(k)$ shall be greater than $0.8 \times v_f$ after the transmit equalizer coefficients have been set to the "preset" values.

93.8.1.6.2 Linear fit error

For any configuration of the transmit equalizer, the RMS value of the error between the linear fit and the measured waveform, $e(k)$, normalized to the peak value of the linear fit pulse, $p(k)$, shall be less than or equal to 0.037.

93.8.1.6.3 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72–5) or receives a valid request to “initialize” from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio $(c(0)+c(1)–c(–1))/(c(0)+c(1)+c(–1))$ is 1.29±10% and the ratio $(c(0)–c(1)+c(–1))/(c(0)+c(1)+c(–1))$ is 2.57±10%. These requirements apply upon the assertion a coefficient status report of “updated” for all coefficients.

93.8.1.6.4 Coefficient step size

The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to “increment” that coefficient shall be between 0.0083 and 0.05. The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to “decrement” that coefficient shall be between –0.05 and –0.0083.

The change in the normalized amplitude of the coefficient is defined to be the difference in the value measured prior to the assertion of the “increment” or “decrement” request (e.g., the coefficient update request for all coefficients is “hold”) and the value upon the assertion of a coefficient status report of “updated” for that coefficient.

93.8.1.6.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient will reach a lower or upper bound based on the coefficient range or restrictions placed on the minimum steady-state differential output voltage or the maximum peak-to-peak differential output voltage.

With $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)–c(1))/(c(0)+c(1))$ shall be greater than or equal to 4.

With $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)–c(-1))/(c(0)+c(-1))$ shall be greater than or equal to 1.54.

Note that a coefficient may be set to zero by first asserting the preset control and then manipulating the other coefficients as required by the test.

93.8.1.7 Transmitter far-end output noise

The transmitter far-end output noise is defined in 85.8.3.2.

The far-end transmitter output noise is measured using two reference channels:

A "low-loss" channel with insertion loss that satisfies the requirements of Test 1 in Table 93–7 and far-end integrated crosstalk noise, computed per 85.10.7, denoted as σ_l.
A "high-loss" channel with insertion loss that satisfies the requirements of Test 4 in Table 93–7 and far-end integrated crosstalk noise, computed per 85.10.7, denoted as σ_h.

For the low-loss channel, $RMSl_{dev}$ shall be less than or equal to the value given by Equation .(93–4)

$$RMSl_{dev} = \sqrt{\sigma_l^2 + 2^2} \text{ mV} \quad (93–4)$$

For the high-loss channel, $RMSh_{dev}$ shall be less than or equal to the value given by Equation (93–5).

$$RMSh_{dev} = \sqrt{\sigma_h^2 + 1^2} \text{ mV} \quad (93–5)$$

93.8.1.8 Transmitter output jitter

The conditions for the measurement of transmitter output jitter (jitter filter, test pattern, etc.) are defined in 92.8.3.7.

Even-odd jitter is defined in 92.8.3.9.1. Even-odd jitter shall be less than or equal to 0.035 UI regardless of the transmit equalization setting.

Total jitter is defined in 92.8.3.9.2. Data dependent jitter is defined in 92.8.3.9.3. The difference between total jitter and data dependent jitter shall be less than or equal to 0.28 UI regardless of the transmit equalization setting.

The effective deterministic jitter and effective random jitter are defined in 92.8.3.9.4. The difference between the effective deterministic jitter and data dependent jitter shall be less than or equal to 0.15 UI regardless of the transmit equalization setting. The effective random jitter shall be less than or equal to 0.15 UI regardless of the transmit equalization setting.

93.8.2 Receiver characteristics

Receiver characteristics measured at TP5a are summarized in Table 93–6.

Table 93–6—Summary of receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min.)	93.8.2.2	Equation (93–2)	dB
Differential to common-mode return loss (min.)	93.8.2.2	Equation (93–6)	dB
Interference tolerance	93.8.2.3	Table 93–7	—
Jitter tolerance	93.8.2.4	Table 93–8	—

93.8.2.1 Receiver test fixture

Unless otherwise noted, measurements of the receiver are made at the input to a test fixture as shown in Figure 93–8.

The insertion loss of the test fixture shall be between 1.2 dB and 1.6 dB at 12.89 GHz. The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.1 dB from 0.05 to 13 GHz.

The differential return loss of the test fixture, in dB, shall meet Equation (93–1) where *f* is the frequency in GHz. The return loss limit is illustrated by Figure 93–3.

The common-mode return loss of the test fixture shall be greater than or equal to 10 dB from 0.05 to 13 GHz.

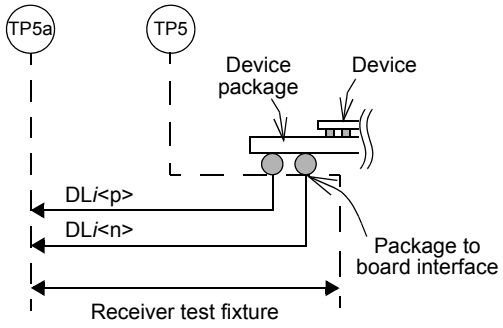


Figure 93–8—Receiver test fixture and test points

93.8.2.2 Receiver input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (93–2) where *f* is the frequency in GHz. The reference impedance for differential return loss measurements shall be 100 Ω. The differential input return loss limit is illustrated by Figure 93–6.

The differential to common-mode return loss, in dB, of the receiver shall meet Equation (93–6).

$$RL_{cd}(f) = \left\{ \begin{array}{ll} 25 - 1.44f & 0.05 \le f \le 6.95 \\ 15 & 6.95 < f \le 19 \end{array} \right\} \text{dB} \quad (93\text{–}6)$$

The differential to common-mode return loss limit is illustrated by Figure 93–9.

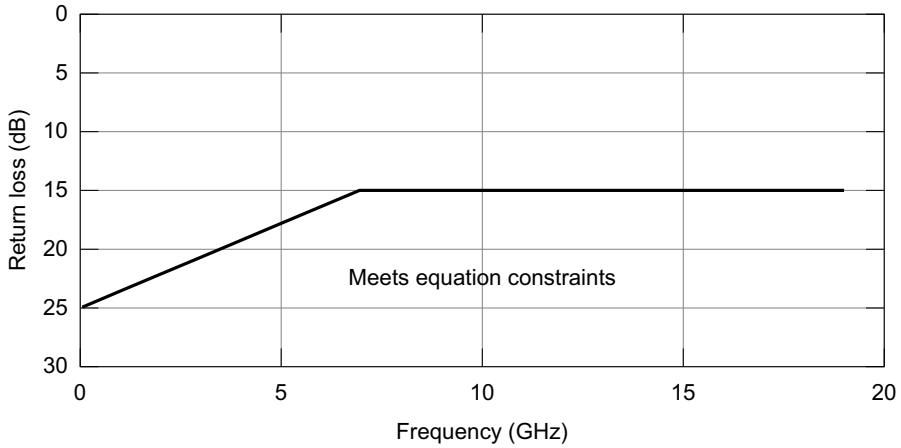


Figure 93–9—Receiver differential to common-mode return loss limit

93.8.2.3 Receiver interference tolerance

Editor's note (to be removed prior to final publication):

The receiver interference tolerance test was modified per moore_3bj_02a_0513.pdf as prescribed by the response to comment #90. However, the contribution left some parameters undefined and the editor has included values for these parameters based on an understanding of the method. The parameters in question are the transmitter noise parameter to be calibrated by the transmit noise source, the transmitter jitter values to be measured and their mapping to COM parameters, the target RS-FEC symbol erorr ratio, and the minimum value for RSS_DFE4.

The receiver interference tolerance test setup and method are defined in Annex 93C. The receiver on each lane shall meet the RS-FEC symbol error ratio requirement with the channel defined for each test listed in Table 93–7. The parameter RSS_DFE4 is a figure of merit for the test channel that is defined in 93A.2.

The following considerations apply to the interference tolerance test. The test transmitter meets the specifications in 93.8.1 as measured at TPta (see Figure 93C–2). The test transmitter is constrained such that for any transmit equalizer setting the differential peak-to-peak voltage (see 93.8.1.3) is less than or equal to 800 mV and the pre- and post-cursor equalization ratios (see 93.8.1.6.5) are less than or equal to 1.54 and 4 respectively. If the test transmitter far-end output noise (see 93.8.1.7) is less than the maximum compliant value, the amplitude of transmit noise source shown in Figure 93C–2 is increased until the maximum compliant far-end noise amplitude is achieved. The lowest frequency f_{NSD1} for constraints on the noise spectral density is 1 GHz.

The values of the parameters required for the calculation of COM are given in Table 93–9 with the following exceptions. The COM parameter σ_{RJ} is set to the measured value of effective random jitter divided by 14.07 and the COM parameter A_{DD} is set to half the measured value of effective deterministic jitter exclud-

ing data dependent jitter (see 93.8.1.8). Tests 1 and 2 are for the case when error correction is bypassed in the RS-FEC sublayer (see 91.5.3.3) and for these cases COM is computed with a DER_0 value of 10^{-12}. The test pattern to be used is either PRBS31 or the scrambled idles test pattern.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

Table 93–7—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Test 3 values		Test 4 values		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
RS-FEC symbol error ratio[a]	—	10^{-11}	—	10^{-11}	—	10^{-4}	—	10^{-4}	—
Insertion loss at 12.89 GHz[b]	—	16	30	—	—	30	35	—	dB
Coefficients of fitted insertion loss[c]									
a_0	–0.9	0.9	–0.9	0.9	–0.9	0.9	–0.9	0.9	dB
a_1	0	3.3	0	3.3	0	3.3	0	3.3	dB/GHz$^{1/2}$
a_2	0	—	0	—	0	—	0	—	dB/GHz
a_4	0	0.022	0	0.03	0	0.03	0	0.043	dB/GHz^2
RSS_DFE4	0.05	—	0.05	—	0.05	—	0.05	—	—
COM, including effects of broadband noise	—	1.5	—	1.5	—	1.5	—	1.5	dB

[a]The FEC symbol error ratio is measured in step 11 of the receiver interference tolerance method defined in 93C.2.
[b]Measured between TPt and TP5 (see Figure 93C–4).
[c]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with f_{min} = 0.05 GHz, f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz.

93.8.2.4 Receiver Jitter Tolerance

Receiver jitter tolerance is measured using the test setup shown in Figure 93–10, or its equivalent, for the receiver of each lane.

The test transmitter meets the specifications of 93.8.1. It is constrained so that its differential peak-to-peak output voltage does not exceed 800 mV at TP0a regardless of the transmitter equalizer setting (see 93.8.1.3). It is further constrained so that its maximum pre-cursor equalization ratio is 1.54 and its maximum post-cursor equalization ratio is 4 (see 93.8.1.6.5).

The test channel meets the requirements of the interference tolerance test channel using Test 4 values (see 93.8.2.3). No broadband noise is added for this test.

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 93–8. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0a. The output of the ISI channel is connected to the input of the receiver under test at TP5a. The link is initialized and the PMD start-up protocol is allowed to complete thereby optimizing the test transmitter equalizer. The test transmitter then transmits either PRBS31 or scrambled idle (subsequently encoded by the

RS-FEC sublayer). The BER at the output of the receiver under test, and prior to error correction by the RS-FEC sublayer, is measured.

The BER shall be less than or equal to 10^{-5} for each case listed in Table 93–8.

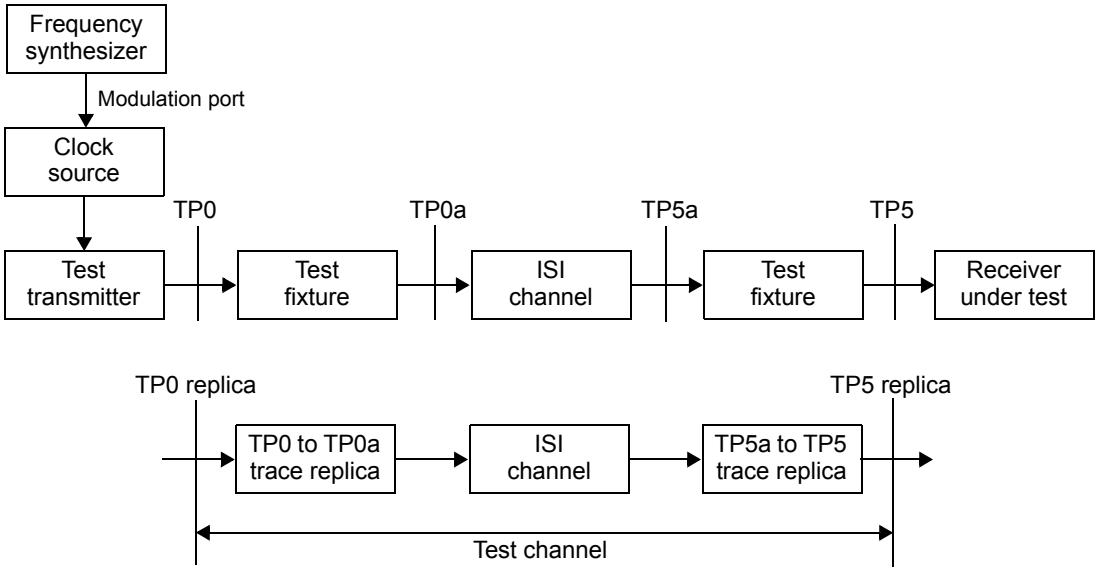


Figure 93–10—Jitter tolerance test setup

Table 93–8—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Jitter frequency	190	940	kHz
Peak-to-peak jitter amplitude	5	1	UI

93.9 Channel characteristics

93.9.1 Channel operating margin

The channel operating margin (COM) computed using the procedure in 93A.1 and the parameters in Table 93–9 shall be greater than or equal to 3 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

The receive path of the RS-FEC sublayer may have the option to perform error detection without correction to reduce the data delay (see 91.5.3.3). Channels that are compatible with this mode of operation shall meet this COM requirement with the value of DER_0 set to 10^{-12}.

Table 93–9—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_d z_p C_b	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	 dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	14	UI
Normalized DFE coefficient magnitude limit	$b_{\max}(n)$	1 for $n = 1$ to N_b	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.07	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-5}	—

93.9.2 Insertion loss

The insertion loss, in dB, of the channel is recommended to meet Equation (93–7).

$$IL(f) \le \left\{ \begin{array}{ll} 1.5 + 4.6\sqrt{f} + 1.318f & 0.05 \le f \le f_b/2 \\ -12.71 + 3.7f & f_b/2 < f \le f_b \end{array} \right\} \text{ (dB)} \qquad (93\text{–}7)$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$IL(f)$ is the insertion loss at frequency f

The insertion loss limit is illustrated by Figure 93–11.

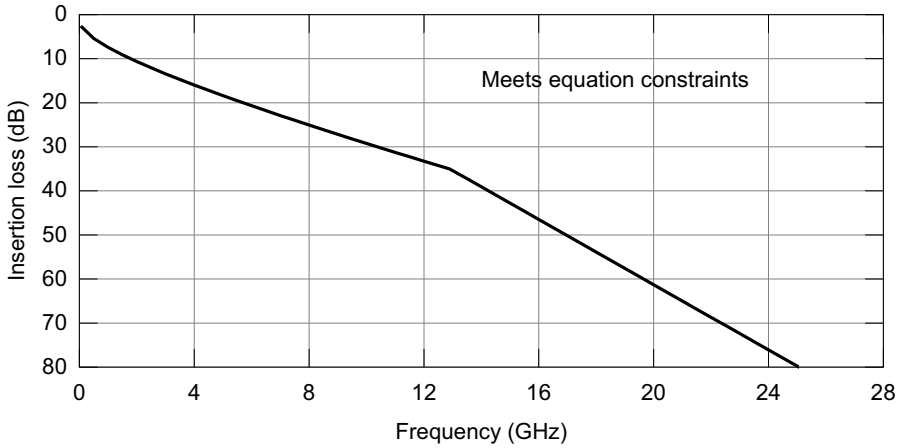


Figure 93–11—Insertion loss limit

93.9.3 Return loss

The return loss, in dB, of the channel is recommended to meet Equation (93–8).

$$RL_d(f) \ge \left\{ \begin{array}{ll} 12 & 0.05 \le f \le f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \le f_b \end{array} \right\} \text{ dB} \qquad (93\text{–}8)$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$RL(f)$ is the return loss at frequency f

The differential return loss limit is illustrated by Figure 93–12.

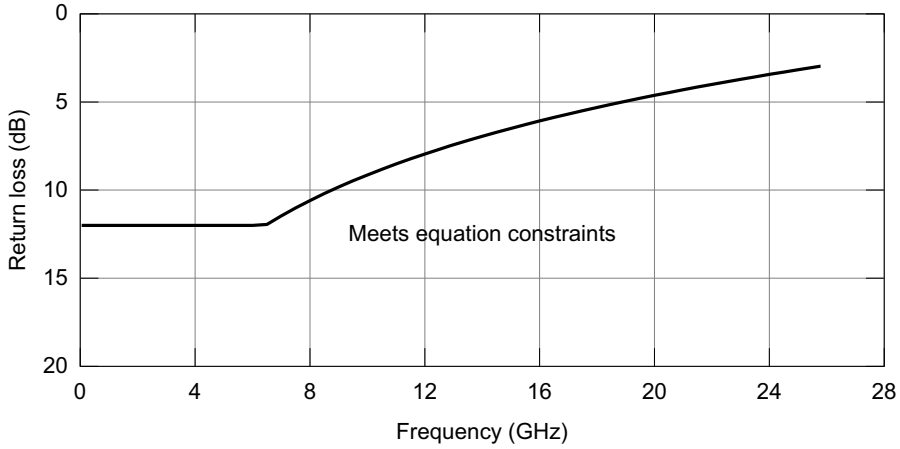


Figure 93–12—Differential return loss limit

93.9.4 AC-coupling

The 100GBASE-KR4 transmitter shall be AC-coupled to the receiver. Common-mode specifications are defined as if the DC-blocking capacitor is implemented between TP0 and TP5. Should the capacitor be implemented outside TP0 and TP5, the common-mode specifications in Table 93–4 may not be appropriate.

The impact of a DC-blocking capacitor implemented between TP0 and TP5 is accounted for within the channel specifications. Should the capacitor be implemented outside TP0 and TP5, it is the responsibility of implementors to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance.

The low-frequency 3 dB cutoff of the AC coupling shall be less than 50 kHz.

93.10 Environmental specifications

93.10.1 General safety

All equipment subject to this clause shall conform to applicable sections (including isolation requirements) of IEC 60950-1.

93.10.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

93.10.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

93.10.4 Electromagnetic compatibility

A system integrating the 100GBASE-KR4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

93.10.5 Temperature and humidity

A system integrating the 100GBASE-KR4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

93.11 Protocol implementation conformance statement (PICS) proforma for Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4[12]

93.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

93.11.2 Identification

93.11.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

93.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bj-20XX, Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bj-20XX.)	

Date of Statement	

[12] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

93.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CGMII	CGMII	93.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100GBASE-R PCS	93.1		M	Yes [ ]
RS-FEC	100GBASE-R RS-FEC	93.1		M	Yes [ ]
PMA	100GBASE-R PMA	93.1		M	Yes [ ]
CAUI	CAUI	93.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-negotiation	93.1		M	Yes [ ]
DC	Delay constraints	93.4	Conforms to delay constraints specified in 93.4	M	Yes [ ]
DSC	Skew constraints	93.5	Conforms to the Skew and Skew Variation constraints specified in 93.5	M	Yes [ ]
*MD	MDIO capability	93.6	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE capability	93.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	93.7.6	Function is supported	EEE:M	Yes [ ] No [ ]
*LTD	PMD lane-by-lane transmit disable function	93.7.7	Function is supported	O	Yes [ ] No [ ]

93.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4

93.11.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	PMD transmit function	93.7.2	Converts four logical bit streams from the PMD service interface into four electrical signals and delivers them to the MDI	M	Yes [ ]
FS2	Mapping of logical signals to electrical signals	93.7.2	Positive differential output voltage corresponds to tx_bit=one	M	Yes [ ]
FS3	ALERT signal	93.7.2	Transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane when tx_mode is set to ALERT	EEE:M	Yes [ ] N/A [ ]
FS4	PMD receive function	93.7.3	Converts four electrical signals from the MDI into four logical bit streams delivers them to the PMD service interface	M	Yes [ ]
FS5	Mapping of eletrical signals to logical signals	93.7.3	Positive differential input voltage corresponds to rx_bit=one	M	Yes [ ]
FS6	SIGNAL_OK mapping	93.2	Set to OK when Global_PMD_signal_detect is one and set to FAIL when Global_PMD_signal_detect is zero	M	Yes [ ]
FS7	Training disabled by variable mr_training_enable	93.7.5	PMD_signal_detect_*i* set to one for *i*=0 to 3	M	Yes [ ]
FS8	PMD_signal_detect_*i* asserted, rx_mode=QUIET	93.7.5	Set to one within 500 ns following the application of the signal defined in 93.7.5 to the input of the channel corresponding to the receiver of lane *i*	EEE:M	Yes [ ] N/A [ ]
FS9	PMD_signal_detect_*i* not asserted, rx_mode=QUIET	93.7.5	Not set to one when the signal applied to the input of the channel corresponding to the receiver of lane *i* is less than or equal to 60 mV peak-to-peak differential	EEE:M	Yes [ ] N/A [ ]
FS10	Global_PMD_transmit_disable variable	93.7.6	When set to one, all transmitters satisfy the requirements of 93.7.6	GTD:M	Yes [ ] N/A [ ]
FS11	Global PMD transmit disable function affect on loopback	93.7.6	No effect	GTD:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
FS12	Global PMD transmit disable function, tx_mode transition to QUIET	93.7.6	Turn off all transmitters when tx_mode transitions to QUIET from any other value	EEE:M	Yes [ ] N/A [ ]
FS13	Global PMD transmit disable function, tx_mode transition from QUIET	93.7.6	Turn on all transmitters when tx_mode transitions from QUIET to any other value	EEE:M	Yes [ ] N/A [ ]
FS14	PMD_transmit_disable_*i* variable	93.7.7	When set to one, the transmitter for lane *i* satisfies the requirements of 93.8.1.3	LTD:M	Yes [ ] N/A [ ]
FS15	PMD lane-by-lane transmit disable function affect on loopback	93.7.7	No effect	LTD:M	Yes [ ] N/A [ ]
FS16	PMD_fault variable mapping to MDIO	93.7.9	Mapped to the fault bit as specified in 45.2.1.2.1	MD:M	Yes [ ] N/A [ ]
FS17	PMD_transmit_fault variable mapping to MDIO	93.7.10	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
FS18	PMD_receive_fault variable mapping to MDIO	93.7.11	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
FS19	PMD control function	93.7.12	Defined in 72.6.10	M	Yes [ ]
FS20	Training frame structure	93.7.12	Defined in 72.6.10 but adjusted for 100GBASE-KR4 signaling rate and use of uncorrelated training patterns	M	Yes [ ]
FS21	PMD control function variable mapping to MDIO	93.7.12	Map variables as specified in 93.7.12	MD:M	Yes [ ] N/A [ ]
FS22	PMD control response time	93.7.12	Response time less than 2 ms.	M	Yes [ ]

93.11.4.2 Transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture insertion loss	93.8.1.1	Between 1.2 dB and 1.6 dB at 12.89 GHz.	M	Yes [ ]
TC2	Test fixture insertion loss deviation	93.8.1.1	Magnitude less than 0.1 dB	M	Yes [ ]
TC3	Test fixture differential return loss	93.8.1.1	Meets equation constraints	M	Yes [ ]
TC4	Test fixture common-mode return loss	93.8.1.1	Greater than or equal to 10 dB from 0.05 to 13 GHz	M	Yes [ ]
TC5	Signaling rate per lane	93.8.1.2	25.78125 GBd ± 100 ppm	M	Yes [ ]
TC6	Peak-to-peak differential output voltage	93.8.1.3	Less than or equal to 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC7	Peak-to-peak differential output voltage, transmitter disabled	93.8.1.3	Less than or equal to 30 mV	M	Yes [ ]
TC8	DC common-mode output voltage	93.8.1.3	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC9	AC common-mode output voltage	93.8.1.3	Less than or equal to 12 mV RMS with respect to signal ground	M	Yes [ ]
TC10	Common-mode output voltage requirements	93.8.1.3	Met regardless of the transmit equalizer setting	M	Yes [ ]
TC11	Transmitter disable timing	93.8.1.3	Peak-to-peak differential output voltage less than 30 mV within 500 ns of the transmitter being disabled	EEE:M	Yes [ ] N/A [ ]
TC12	Transmitter enable timing	93.8.1.3	Peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of the transmitter being enabled and meet all requirements of 93.8.1 within 1 μs	EEE:M	Yes [ ] N/A [ ]
TC13	Common-mode output voltage, transmitter disabled	93.8.1.3	Maintained to within ±150 mV of the value for the enabled transmitter	EEE:M	Yes [ ] N/A [ ]
TC14	Differential input return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC15	Reference impedance for differential return loss measurements	93.8.1.4	100 Ω	M	Yes [ ]
TC16	Common-mode output return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC17	Reference impedance for common-mode return loss measurements	93.8.1.4	25 Ω	M	Yes [ ]
TC18	Transition times	93.8.1.5	Greater than or equal to 8 ps when transmit equalization is disabled	M	Yes [ ]
TC19	Steady-state voltage, v_f	93.8.1.6.1	Greater than or equal to 0.4 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the "preset" values	M	Yes [ ]
TC20	Linear fit pulse peak	93.8.1.6.1	Greater than $0.8 \times v_f$ after the transmit equalizer coefficients have been set to the "preset" values	M	Yes [ ]
TC21	Normalized linear fit error	93.8.1.6.2	Less than or equal to 0.037	M	Yes [ ]
TC22	Coefficient initialization	93.8.1.6.3	Satisfies the requirements of 93.8.1.6.3.	M	Yes [ ]
TC23	Normalized coefficient step size for “increment”	93.8.1.6.4	Between 0.0083 and 0.05	M	Yes [ ]
TC24	Normalized coefficient step size for “decrement”	93.8.1.6.4	Between –0.05 and –0.0083	M	Yes [ ]
TC25	Maximum post-cursor equalization ratio	93.8.1.6.5	Greater than or equal to 4	M	Yes [ ]
TC26	Maximum pre-cursor equalization ratio	93.8.1.6.5	Greater than or equal to 1.54	M	Yes [ ]
TC27	Transmitter far-end output noise, low-loss channel	93.8.1.7	Meets equation constraints	M	Yes [ ]
TC28	Transmitter far-end output noise, high-loss channel	93.8.1.7	Meets equation constraints	M	Yes [ ]
TC29	Even-odd jitter	93.8.1.8	Less than or equal to 0.035 UI regardless of the transmit equalization setting	M	Yes [ ]
TC30	Total jitter, excluding data dependent jitter	93.8.1.8	Less than or equal to 0.28 UI regardless of the transmit equalization setting	M	Yes [ ]
TC31	Effective deterministic jitter, excluding data dependent jitter	93.8.1.8	Less than or equal to 0.15 UI regardless of the transmit equalization setting	M	Yes [ ]
TC32	Effective random jitter	93.8.1.8	Less than or equal to 0.15 UI regardless of the transmit equalization setting	M	Yes [ ]

93.11.4.3 Receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture insertion loss	93.8.2.1	Between 1.2 dB and 1.6 dB at 12.89 Ghz.	M	Yes [ ]
RC2	Test fixture insertion loss deviation	93.8.2.1	Magnitude less than 0.1 dB	M	Yes [ ]
RC3	Test fixture differential return loss	93.8.2.1	Meets equation constraints	M	Yes [ ]
RC4	Test fixture common-mode return loss	93.8.2.1	Greater than or equal to 10 dB from 0.05 to 13 GHz	M	Yes [ ]
RC5	Differential input return loss	93.8.2.2	Meets equation constraints	M	Yes [ ]
RC6	Reference impedance for differential return loss measurements	93.8.2.2	100 Ω	M	Yes [ ]
RC7	Differential to common-mode return loss	93.8.2.2	Meets equation constraints	M	Yes [ ]
RC8	Receiver interference tolerance	93.8.2.3	Satisfy requirements summarized in Table 93–7	M	Yes [ ]
RC9	Receiver jitter tolerance	93.8.2.4	BER less than or equal to 10^{-5} for each case listed in Table 93–8	M	Yes [ ]

93.11.4.4 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel operating margin (COM)	93.9.1	Greater than or equal to 3 dB	M	Yes [ ]
CC2	COM when error correction is bypassed by the RS-FEC sublayer	93.9.1	Greater than or equal to 3 dB but with $DER_0 = 10^{-12}$	M	Yes [ ]
CC3	AC-coupling	93.9.4	Channel AC couples the transmitter to the receiver	M	Yes [ ]
CC4	AC-coupling 3 dB cut-off frequency	93.9.4	Less than 50 kHz	M	Yes [ ]

93.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Generate safety	93.10.1	Conform to applicable sections of IEC 60950-1	M	Yes [ ]
ES2	Electromagnetic compatibility	93.10.4	Comply with applicable local and national codes	M	Yes [ ]

94. Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 100GBASE-KP4

94.1 Overview

This clause specifies the Physical Medium Attachment (PMA) sublayers, Physical Medium Dependent (PMD) sublayer, and medium for the 100GBASE-KP4 PHY.

When forming a complete Physical Layer, the PMA shall be connected to the RS-FEC, the PMD shall be connected to the medium through the MDI as shown in Figure 94-1, and the PMA and PMD shall be connected to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 94–1—Physical Layer clauses associated with the 100GBASE-KP4 PMD

Associated clause	100GBASE-KP4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
83—PMA for 100GBASE-R	Optional
83A—CAUI	Optional
91—RS-FEC	Required
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

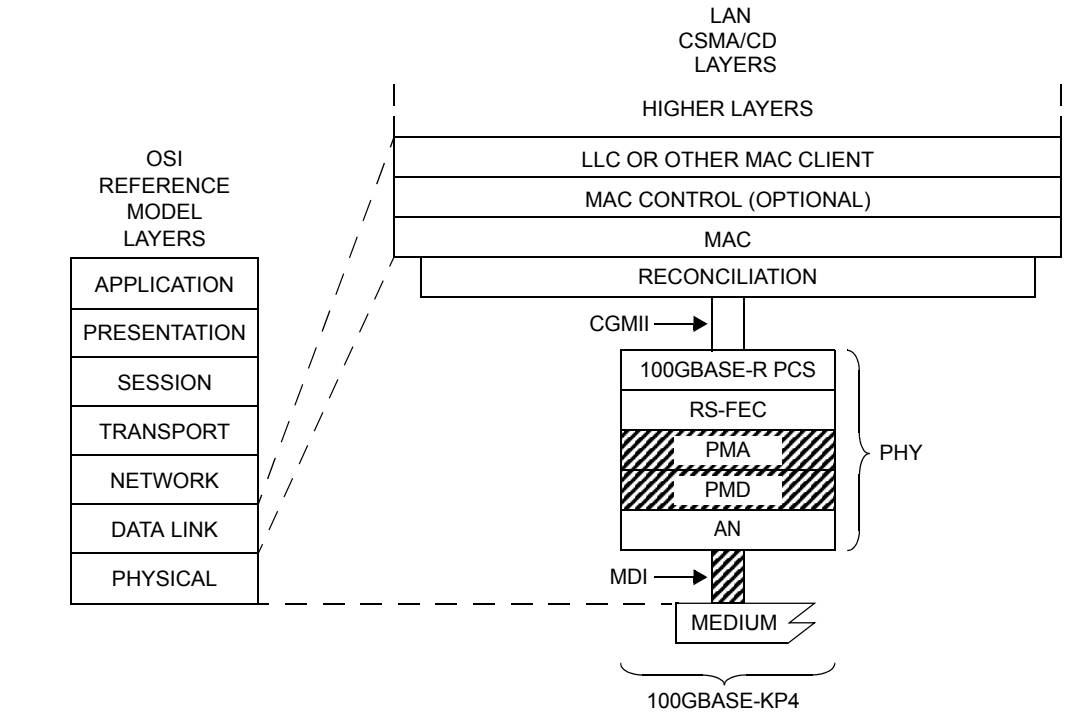
[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.

Figure 94–1 shows the relationship of the 100GBASE-KP4 PMA and PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

Differential signals received at the MDI from a transmitter that meets the requirements of 94.2.2 and 94.3.12 and have passed through the channel specified in 94.4 are received with a BER less than 10^{-5} as measured at the PMA service interface.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.210a) of less than 1.7×10^{-10} for 64-octet frames with minimum inter-packet gap.

A 100GBASE-KP4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.



AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 94–1—100GBASE-KP4 PMA and PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

94.2 Physical Medium Attachment (PMA) Sublayer

94.2.1 PMA Service Interface

The PMA service interface for 100GBASE-KP4 PMA is based on the inter-sublayer service interface defined in 80.3. This interface is defined in an abstract manner and does not imply any particular implementation.

The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication
PMA:IS_SIGNAL.indication

If the optional EEE deep sleep capability is supported (see Clause 78, 78.3) then the PMA service interface includes three additional primitives as follows:

PMA:IS_TX_MODE.request
PMA:IS_RX_MODE.request
PMA:IS_ENERGY_DETECT.indication

94.2.1.1 PMA:IS_UNITDATA_i.request

The PMA:IS_UNITDATA_*i*.request (where *i*=0 to 3) primitive is used to define the transfer of four streams of data units from the PMA client to the PMA.

94.2.1.1.1 Semantics of the service primitive

PMA:IS_UNITDATA_0.request(tx_bit,start)
PMA:IS_UNITDATA_1.request(tx_bit,start)
PMA:IS_UNITDATA_2.request(tx_bit,start)
PMA:IS_UNITDATA_3.request(tx_bit,start)

The data conveyed by PMA:IS_UNITDATA_0.request to IS_UNITDATA_3.request consists of four parallel continuous streams of encoded bits, one stream for each lane. Each of the tx_bit parameters can take one of two values: one or zero. The start parameter is TRUE to indicate that the concurrent tx_bit is the first bit of the first, second, third, or fourth FEC symbol in a FEC codeword and is otherwise FALSE.

94.2.1.1.2 When generated

The PMA client continuously sends four parallel bit streams PMA:IS_UNITDATA_*i*.request(tx_bit,start) to the PMA, each at a nominal signaling rate of 26.5625 Gb/s.

94.2.1.1.3 Effect of receipt

Upon receiving each instance of PMA:IS_UNITDATA_*i*.request, the tx_bit and start parameters are passed to the PMA framing process corresponding to each stream.

94.2.1.2 PMA:IS_UNITDATA_i.indication

The PMA:IS_UNITDATA_*i*.indication (where $i = 0$ to 3) primitive is used to define the transfer of four streams of data units from the PMA to the PMA client.

94.2.1.2.1 Semantics of the service primitive

PMA:IS_UNITDATA_0.indication(rx_bit, start)
PMA:IS_UNITDATA_1.indication(rx_bit, start)
PMA:IS_UNITDATA_2.indication(rx_bit, start)
PMA:IS_UNITDATA_3.indication(rx_bit, start)

The data conveyed by PMA:IS_UNITDATA_0.indication to PMA:IS_UNITDATA_3.indication consists of 4 parallel continuous streams of encoded bits, one stream for each lane. Each of the rx_bit parameters can take one of two values: one or zero. The start parameter is TRUE to indicate that the concurrent rx_bit is the first bit of the first, second, third, or fourth FEC symbol in the FEC codeword and is otherwise FALSE.

94.2.1.2.2 When generated

The PMA continuously sends four parallel bit streams PMA:IS_UNITDATA_*i*.indication(rx_bit,start) to the PMA client, each at a nominal signaling rate of 26.5625 Gb/s.

94.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is defined by the PMA client.

94.2.1.3 PMA:IS_SIGNAL.indication

The PMA:IS_SIGNAL.indication primitive is generated by the PMA to the PMA client to indicate the status of the receive process. This primitive is generated by the receive process to propagate the detection of severe error conditions (e.g., loss of synchronization) to the PMA client.

94.2.1.3.1 Semantics of the service primitive

PMA:IS_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take on one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented (rx_bit parameters undefined) by the PMA to the PMA client. A value of OK does not guarantee valid data is being presented by the PMA to the PMA client.

94.2.1.3.2 When generated

The PMA generates the PMA:IS_SIGNAL.indication primitive to the PMA client whenever there is a change in the value of the SIGNAL_OK parameter.

94.2.1.3.3 Effect of receipt

The effect of receipt of this primitive is defined by the PMA client.

94.2.1.4 PMA:IS_TX_MODE.request

The PMA:IS_TX_MODE.request primitive communicates the tx_mode parameter generated by the PCS LPI transmit process to invoke the appropriate PMA, FEC and PMD transmit EEE states. Without EEE deep sleep capability, this primitive is never invoked and the sublayers behave as if tx_mode = DATA.

94.2.1.4.1 Semantics of the service primitive

PMA:IS_TX_MODE.request(tx_mode)

The tx_mode parameter takes on one of up to six values: DATA, SLEEP, QUIET, FW, ALERT or BYPASS.

94.2.1.4.2 When generated

This primitive is generated to indicate the state of the PCS LPI transmit function.

94.2.1.4.3 Effect of receipt

When this primitive is received, PMD:IS_TX_MODE.request(tx_mode) is generated with the value received in PMA:IS_TX_MODE.request(tx_mode).

If the value is DATA, SLEEP, FW, BYPASS or ALERT, the PMA operates normally.

If the value is QUIET, the PMA may be go into a low power mode.

94.2.1.5 PMA:IS_RX_MODE.request

The PMA:IS_RX_MODE.request primitive communicates the rx_mode parameter generated by the PCS LPI receive process. Without EEE deep sleep capability, this primitive is never invoked and the sublayers behave as if rx_mode = DATA.

94.2.1.5.1 Semantics of the service primitive

PMA:IS_RX_MODE.request(rx_mode)

The rx_mode parameter takes on one of two values: DATA or QUIET.

94.2.1.5.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function.

94.2.1.5.3 Effect of receipt

When this primitive is received, PMD:IS_RX_MODE.request(rx_mode) is generated with the value received in PMA:IS_RX_MODE.request(rx_mode).

If the value is DATA, the PMA operates normally.

If the value is QUIET, the PMA may be go into a low power mode.

94.2.1.6 PMA:IS_ENERGY_DETECT.indication

The PMA:IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the presence of energy on the interface following a period of quiescence. Without EEE deep sleep capability, this primitive is never invoked and has no effect.

94.2.1.6.1 Semantics of the service primitive

PMA:IS_ENERGY_DETECT.indication(energy_detect)

The parameter energy_detect is Boolean.

94.2.1.6.2 When generated

This primitive is generated by the PMA, reflecting the state of PMD:IS_SIGNAL.indication(SIGNAL_OK) received from the PMD (see 94.3.1.3). When SIGNAL_OK indicates OK, energy detect indicates TRUE. When SIGNAL_OK indicates FAIL, energy_detect indicates FALSE.

94.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is defined by the PMA client sublayers that receive it.

94.2.2 PMA Transmit Functional Specifications

In the transmit direction, the role of the 100GBASE-KP4 PMA is to adapt the signal from the FEC (the PMA client) to a PAM4 encoded signal to be passed to the PMD for transfer over the attached medium. The adaptation processes shown in Figure 94–2 include insert overhead, insert termination bits, apply Gray coding, apply 1/(1+D) mod 4 precoding, and apply PAM4 encoding.

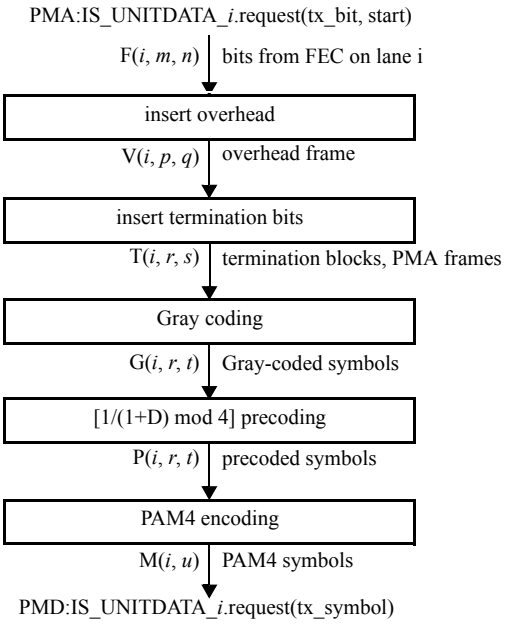


Figure 94–2—Transmit adaptation process diagram

94.2.2.1 FEC Interface

The PMA transmit process receives FEC bits via the PMA:IS_UNITDATA_*i*(tx_bit, start) primitive (see 94.2.1.1). The index *i* indicates the PMA lane number: 0, 1, 2, or 3.

On each transaction, tx_bit is assigned to F(*i*, *m*, *n*), where

i is the lane number
m is an index indicating the FEC codeword number and increments at the start of each codeword
n is an index indicating the bit number within a codeword with a range 1 to 1360

The start of a codeword is determined by the start parameter associated with the tx_bit parameter being equal to TRUE.

94.2.2.2 Overhead Frame

The PMA transmit process shall create a sequence of overhead frames by inserting 40 overhead bits for every 31280 FEC bits as specified in this subclause.

The FEC bits, F(i, m, n) are mapped into a continuous sequence of overhead frames. The overhead frame is 31320 bits in length.

Each bit in the overhead frame is denoted V(i, p, q), where:

i is the lane number
p is an index that indicates the frame number and increments at the start of each frame
q is an index that indicates the bit number within a frame with a range 1 to 31320

The first 40 bits of the frame, V(i, p, 1) to V(i, p, 40) are the overhead bits (see 94.2.2.3). The next 31280 bits, V(i, p, 41) to V(i, p, 31320) are composed of the bits from 23 consecutive FEC codewords.

The overhead bits are inserted in the frame as follows:

V(i, p, 1) = H(i, p, 1)
V(i, p, 2) = H(i, p, 2)
V(i, p, ...) = H(i, p, ...)
V(i, p, 40) = H(i, p, 40)

The FEC codeword bits are aligned such that V(i, p, 41) is the first bit of a codeword, e.g., V(i, p, 41) = F(i, m, 1). The FEC bits are inserted into the frame in the order in which they were received from the FEC, e.g., V(i, p, 42) = F(i, m, 2), V(i, p, 43) = F(i, m, 3), and so on. The method for aligning the FEC codeword with the start of the overhead frame is outside the scope of this standard.

94.2.2.3 Overhead

The PMA transmit process shall form the overhead bits in each overhead frame as specified in this subclause.

The overhead bits are denoted H(i, p, k), where

i is the lane number
p is an index that indicates the frame number and increments at the start of each frame
k is an index that indicates the header bit number with a range 1 to 40.

Bits are mapped to the overhead in a sequence of five groups of 8 bits each. Each 8-bit group takes on the value A or An. The values of the 8 bits in A are such that A(7:0) = TX_OH_pattern(7:0). The values of the 8 bits in An are such that each bit is the inverse of the corresponding bit in A. For each lane i, the sequence of 8-bit groups is according to the bits in TX_OH_sequence_i(4:0) such that H(i,p,((a+1)*8):(a*8+1)) is equal to A(7:0) or An(7:0) if TX_OH_sequence_i(a) is equal to 0 or 1, respectively, where a $\in$ {0,1,2,3,4}.

If the optional Clause 45 MDIO is implemented, the overhead function maps the TX_OH_pattern and TX_OH_sequence_i status variables to the registers and bits defined in 94.2.10. The default values for each of the variables are summarized in Table 94–2.

94.2.2.4 Termination Blocks

The PMA transmit process shall create a sequence of termination blocks by inserting two termination bits for every 90 overhead frame bits as specified in this subclause. The termination block is 92 bits in length. The overhead frame mapped into 348 consecutive termination blocks forms a PMA frame.

Table 94–2—Default overhead configuration values

Parameter	Values (binary)
TX_OH_pattern(7:0)	01100110
TX_OH_sequence_0(4:0)	00110
TX_OH_sequence_1(4:0)	01010
TX_OH_sequence_2(4:0)	10101
TX_OH_sequence_3(4:0)	11001

Each bit in a termination block is denoted T(*i*, *r*, *s*), where:

i is the lane number
r is an index indicating block number and increments at the start of each block
s is an index indicating the bit number within a termination block with a range 1 to 92

The first two bits in each termination block, T(*i*, *r*, 1) and T(i, r, 2), are populated with the output of a PRBS13 generator of the form specified in 94.3.10.8. For each termination block, the PRBS13 generator generates a block of 92 pseudo-random bits, R(i,1:92). The first two bits are used for the termination bits such that T(i, r, 1)=R(i, 1) and T(i, r, 2)=R(i,2). The PRBS13 generator is initialized during training (94.3.10.8). Upon the transition from the last training frame to the first PMA frame the PRBS13 generator used during training advances without re-seeding (see 94.3.10.7.2) and without inversion, and the output is used to generate the termination bits. The PRBS13 generator continues to advance without re-seeding and without inversion.

The remaining 90 bits of each termination block, T(*i*, *r*, 3) to T(*i*, *r*, 92), are overhead frame bits (see 94.2.2.2). The overhead frame bits are aligned with the termination blocks such that the first overhead bit, V(*i*, *p*, 1), corresponds to the third bit of a termination block, T(*i*, *r*, 3).

Overhead frame bits are mapped to the termination blocks in order of location within the overhead frame, e.g., T(*i*, *r*, 4) = V(*i*, *p*, 2), T(*i*, *r*, 5) = V(*i*, *p*, 3), and so on.

The termination bit PRBS13 generator is initialized during the training process. When training is complete the state of the termination bit PRBS13 generator is retained and the resulting output is used for the termination bits in the PMA frame.

94.2.2.5 Gray Mapping

The PMA transmit process shall map consecutive pairs of bits to one of four Gray-coded symbols as specified in this subclause.

Each pair of bits, {A, B}, of each termination block are converted to a Gray-coded symbol with one of the four Gray-coded levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

Gray-coded symbols corresponding to each termination block are denoted G(*i*, *r*, *t*), where:

i is the lane number

r is an index indicating the termination block number
t is an index indicating the symbol number within a termination block with a range 1 to 46.

Pairing of bits is such that the first two bits of each termination block, T(*i*, *r*, 1) and T(*i*, *r*, 2), form a pair. Each bit pair {T(*i*, *r*, 2*t*–1), T(*i*, *r*, 2*t*)} maps to {A, B} and the Gray-coded result is assigned to G(*i*, *r*, t). The gray-coded symbol G(*i*, *r*, 1) is formed from the first two bits of a termination block, the termination bits, thus forming a termination symbol.

94.2.2.6 Precoding

The PMA transmit process shall precode the Gray-coded symbols as specified in this subclause.

The precoder output symbols are denoted, P(*i*, *r*, *t*), where:
i is the lane number
r is an index indicating the termination block number
t is an index indicating the symbol number within a termination block with a range 1 to 46.

For each Gray-coded symbol G(*i*, *r*, *t*), a precoded symbol, P(*i*, *r*, *t*) is determined by the following algorithm:

If *t* = 1 then
    P(*i*, *r*, *t*) = G(*i*, *r*, *t*)
Else
    P(*i*, *r*, *t*) = (G(*i*, *r*, *t*) – P(*i*, *r*, *t*–1)) mod 4
End If

The bits contributing to the Gray-coded termination symbol, G(*i*, *r*, 1), are the termination bits. The precoding algorithm applies this symbol directly to the output rather than combining it with the previous non-deterministic symbols and thus this termination symbol is always deterministic.

94.2.2.7 PAM4 encoding

The PMA transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this subclause.

The PAM4 encoded symbols are denoted M(*i*, *u*), where
i is the lane number
u is an index indicating the symbol number.

Each consecutive precoder output symbol, P(*i*, *r*, *t*), is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output M(*i*, u).

Mapping from the precoder output symbol P(*i*, *r*, *t*) to a PAM4 encoded symbol M(*i*, *u*) is as follows:
0 maps to –1,
1 maps to –1/3,
2 maps to +1/3, and
3 maps to +1.

94.2.2.8 PMD Interface

The PMA transmit process shall transmit each PAM4 encoded symbol, M(*i*, *u*) to the PMD via the PMD:IS_UNITDATA_*i*(tx_symbol) primitive at a symbol transfer rate of 13.59375 GBd.

94.2.3 PMA Receive Functional Specifications

The receive process shall recover the data encoded by the transmit process meeting the performance requirements specified in 94.1 after the overhead and termination bits have been removed.

The process by which the receiver recovers the data to meet this requirement is outside the scope of this standard. The signal structure encoded by the transmitter process including the overhead bits, gray coding, and termination symbols may be leveraged by the receiver implementation at the discretion of the implementor. The remainder of this subclause specifies the receiver processes to reverse the transmitter encoding and report status.

In the received direction, the role of the 100GBASE-KP4 PMA is to adapt the PAM4 encoded signal from the PMD to a FEC encoded signal to be passed to the FEC for further processing. The adaptation processes shown in Figure 94–3 include PAM4 decoding, (1+D) mod 4 decoding, inverse Gray coding, remove termination bits, and remove overhead.

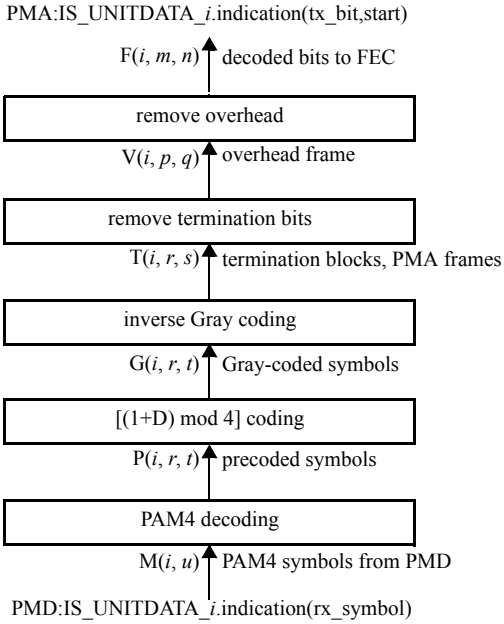


Figure 94–3—Receive adaptation process diagram

94.2.3.1 Overhead

The PMA receive process shall decode the overhead bits in each overhead frame as specified in this subclause. The format of the overhead bits is specified in 94.2.2.3.

The receive process decodes the received overhead bits in a sequence of five groups of 8 bits each into a sequence of 5 bits. Each group of 8 bits is compared with A and An, where A(7:0) = RX_OH_pattern(7:0) and the values of the 8 bits in An are such that each bit is the inverse of the corresponding bit in A. A match of each 8-bit group with A or An results in a decoded value of 0 or 1, respectively. The decoded value when the 8-bit group matches neither A or An is not specified. The decoded values from H(i,p,((a+1)*8):(a*8+1)) are assigned to RX_OH_sequence_i(a), where a ∈ {0,1,2,3,4}. If all of the 8-bit groups match either A or An, the RX_OH_sequence_i(5) is set to 1 and is otherwise set to 0.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the RX_OH_pattern and RX_OH_sequence_i variables to the registers and bits defined in 94.2.10. The default values for each of the control variables are summarized in Table 94–2.

Table 94–3—Default overhead control values

Parameter	Values (binary)
RX_OH_pattern(7:0)	01100110

94.2.4 Skew constraints

Skew considerations for the 100GBASE-KP4 PMA, PMD, and AN are specified in 94.3.4.

94.2.5 Delay constraints

Delay considerations for the 100GBASE-KP4 PMA, PMD, AN, and medium are specified in 94.3.3.

94.2.6 Link status

The PMA shall provide link status information to the PMA client using the PMA:IS_SIGNAL.indication primitive (see 94.2.1.3). The PMA continuously monitors the link status reported by the PMD from the PMD:IS_SIGNAL.indication primitive, and uses this as input to Signal Indication Logic (SIL) to determine the link status to report to the PMA client. Other inputs to the SIL may include status of clock and data recovery on the lanes from the PMD and frame synchronization.

94.2.7 PMA local loopback mode

PMA local loopback shall be provided. This function involves looping back each input lane from the PMA service interface to the corresponding output lane on the PMA service interface. Each received instance of the PMA:IS_UNITDATA_*i*.request(tx_bit,start) primitive is looped back in the direction of the PMA client using the PMA:IS_UNITDATA_*i*.indication(rx_bit,start) primitive.

During local loopback, the PMA performs normal framing and precoding onto the lanes in the Tx direction toward the PMD service interface.

Ability to perform this function is indicated by the Local_loopback_ability status variable. The Local_loopback_ability status variable is always set to 1. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15). A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

94.2.8 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

Remote loopback, if provided, should be implemented close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each bit received over a lane of the service interface below the PMA via PMD:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via PMD:IS_UNITDATA_*i*.request.

During remote loopback, the PMA performs normal bit processing operation in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the Remote_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (45.2.1.12.1). A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one, and removed from remote loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

94.2.9 PMA test patterns

94.2.9.1 JP03A test pattern

A 100GBASE-KP4 PHY shall include a JP03A test pattern generator as specified in this subclause.

The JP03A test pattern is generated prior to PAM4 encoding. When the JP03A test pattern is enabled, it replaces the signal from the precoder. The JP03A test pattern is a repeating {0,3} sequence.

The JP03A test pattern is enabled by the test_pattern_enable and JP03A_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.9.2 JP03B test pattern

A 100GBASE-KP4 PHY shall include a JP03B test pattern generator as specified in this subclause.

The JP03B test pattern is generated prior to PAM4 encoding. When the JP03B test pattern is enabled, it replaces the signal from the precoder. The JP03B test pattern is a repeating sequence of {0,3} repeated 15 times followed by {3,0} repeated 16 times. The entire 62-symbol pattern is shown in Equation (94–1).

$$03030303030303030303030303033030303030303030303030303030303030 \quad (94–1)$$

The JP03B test pattern is enabled by the test_pattern_enable and JP03B_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.9.3 Quaternary PRBS13 test pattern

A 100GBASE-KP4 PHY shall include a quaternary PRBS13 (QPRBS13) pattern generator as specified in this subclause.

The QPRBS13 test pattern is a repeating 15548-symbol (338 training frame words) sequence equivalent to the training pattern specified in 94.3.10.8.

The PRBS13 pattern generator is re-initialized for each repetition of QPRBS13 with the same seeds specified in Table 94–11.

The QPRBS13 test pattern is enabled by the test_pattern_enable and QPRBS13_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.10 PMA MDIO function mapping

Clause 45 specifies the optional MDIO capability that describes several registers that provide control and status information for and about the PMA. 45.2.1 describes the Management Data Input/Output (MDIO) Manageable Device (MMD) addresses. If MDIO is implemented, it shall map MDIO control bits to PMA control variables as shown in Table 94–4, and MDIO status bits to PMA status variables as shown in Table 94–5.

Table 94–4—100GBASE-KP4 MDIO/PMA control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMA control variable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
PMA remote loopback	PMA/PMD status 2	1.0.1	Remote_loopback_enable
PMA Tx generator enable	PRBS pattern testing control	1.1501.3	test_pattern_enable
JP03A pattern enable	PRBS pattern testing control	1.1501.8	JP03A_enable
JP03B pattern enable	PRBS pattern testing control	1.1501.9	JP03B_enable
QPRBS13 pattern enable	PRBS pattern testing control	1.1501.10	QPRBS13_enable
PMA transmit overhead pattern	PMA overhead control 1	1.162.7:0	TX_OH_pattern
PMA transmit overhead sequence 0	PMA overhead control 1	1.162.12:8	TX_OH_sequence_0
PMA transmit overhead sequence 1	PMA overhead control 2	1.163.4:0	TX_OH_sequence_1
PMA transmit overhead sequence 2	PMA overhead control 2	1.163.9:5	TX_OH_sequence_2
PMA transmit overhead sequence 3	PMA overhead control 2	1.163.14:10	TX_OH_sequence_3
PMA receive overhead pattern	PMA overhead control 3	1.164.7:0	RX_OH_pattern

94.3 Physical Medium Dependent (PMD) Sublayer

94.3.1 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-KP4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is based on the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

Table 94–5—100GBASE-KP4 MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PMA remote loopback ability	40G/100G PMA/PMD extended ability	1.13.15	Remote_loopback_ability
PMA receive overhead sequence 0	PMA overhead status 1	1.165.5:0	RX_OH_sequence_0
PMA receive overhead sequence 1	PMA overhead status 1	1.165.11:6	RX_OH_sequence_1
PMA receive overhead sequence 2	PMA overhead status 2	1.166.5:0	RX_OH_sequence_2
PMA receive overhead sequence 3	PMA overhead status 2	1.166.11:6	RX_OH_sequence_3

If the optional EEE capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

94.3.1.1 PMD:IS_UNITDATA_i.request

The PMD:IS_UNITDATA_*i*.request (where *i*=0 to 3) primitive is used to define the transfer of four streams of data units from the PMA to the PMD.

94.3.1.1.1 Semantics of the service primitive

PMD:IS_UNITDATA_0.request(tx_symbol)
PMD:IS_UNITDATA_1.request(tx_symbol)
PMD:IS_UNITDATA_2.request(tx_symbol)
PMD:IS_UNITDATA_3.request(tx_symbol)

The data conveyed by PMD:IS_UNITDATA_i.request consists of four parallel continuous streams of encoded symbols, tx_symbol, one stream for each lane. Each of the tx_symbol parameters can take one of four values: –1, –1/3, +1/3, or +1.

94.3.1.1.2 When generated

The PMA continuously sends four parallel symbol streams PMD:IS_UNITDATA_*i*.request(tx_symbol) to the PMD, each at a nominal signaling rate of 13.59375 GBd.

94.3.1.1.3 Effect of receipt

Upon receiving each instance of PMD:IS_UNITDATA_*i*.request, the tx_symbol parameter is passed to the PMD transmit process corresponding to each stream.

94.3.1.2 PMD:IS_UNITDATA_i.indication

The PMD:IS_UNITDATA_*i*.indication (where *i*=0 to 3) primitive is used to define the transfer of four streams of data units from the PMD to the PMA.

94.3.1.2.1 Semantics of the service primitive

PMD:IS_UNITDATA_0.indication(rx_symbol)
PMD:IS_UNITDATA_1.indication(rx_symbol)
PMD:IS_UNITDATA_2.indication(rx_symbol)
PMD:IS_UNITDATA_3.indication(rx_symbol)

The data conveyed by PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication consists of 4 parallel continuous streams of encoded symbols, one stream for each lane. Each of the rx_symbol parameters can take one of four values: –1, –1/3, +1/3, or +1.

94.3.1.2.2 When generated

The PMD continuously sends four parallel bit streams PMD:IS_UNITDATA_*i*.indication(rx_symbol) to the PMD client, each at a nominal signaling rate of 13.59375 GBd.

94.3.1.2.3 Effect of receipt

The effect of receipt of this primitive is undefined by the PMD.

94.3.1.3 PMD:IS_SIGNAL.indication

The PMD:IS_SIGNAL.indication primitive is generated by the PMD to the PMA to indicate the status of the PMD receive process. This primitive is generated by the PMD receive process to propagate the detection of severe error conditions (e.g., loss of synchronization) to the PMA.

94.3.1.3.1 Semantics of the service primitive

PMD:IS_SIGNAL.indication(SIGNAL_OK).

The SIGNAL_OK parameter corresponds to the variable Global_PMD_signal_detect as defined in 94.3.6.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_DETECT = FAIL, the PMD:IS_UNITDATA_*i*.indication parameters are undefined.

94.3.1.3.2 When generated

The PMD generates the PMD:IS_SIGNAL.indication primitive to the PMD client whenever there is change in the value of the Global_PMD_signal_detect parameter.

94.3.1.3.3 Effect of receipt

The effect of receipt of this primitive is undefined by the PMD.

94.3.2 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 100GBASE-KP4 PHY may be extended using CAUI as a physical instantiation of the inter-sublayer service interface between devices. If CAUI is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementor. As examples, the implementor may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

94.3.3 Delay constraints

The sum of the transmit and the receive delays contributed by the 100GBASE-KP4 PMA, PMD, AN, and the medium in one direction shall be no more than 8192 bit times (16 pause_quanta or 81.92 ns). It is assumed that the one way delay through the medium is no more than 800 bit times (8 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

94.3.4 Skew constraints

The Skew (relative delay) between the lanes must be kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–4 and Figure 80–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 0.4 ns.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 0.6 ns.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

94.3.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 94–6, and MDIO status bits to PMD status variables as shown in Table 94–7.

Table 94–6—100GBASE-KP4 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable

Table 94–7—100GBASE-KP4 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0
Receiver status 3	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status	1.151.13	frame_lock_3
Start-up protocol status 3	BASE-R PMD status	1.151.14	training_3
Training failure 3	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status	1.151.9	frame_lock_2
Start-up protocol status 2	BASE-R PMD status	1.151.10	training_2
Training failure 2	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status	1.151.5	frame_lock_1
Start-up protocol status 1	BASE-R PMD status	1.151.6	training_1
Training failure 1	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock_0
Start-up protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0

94.3.6 PMD functional specifications

94.3.6.1 Link block diagram

One direction for one lane of a 100GBASE-KP4 link is shown in Figure 94–4.

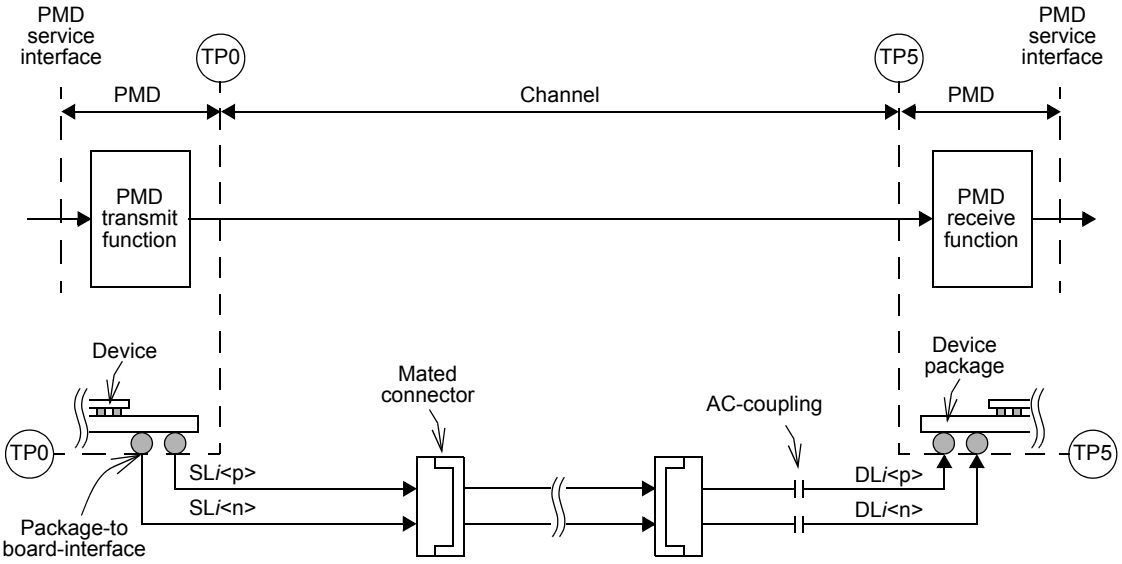


Figure 94–4—100GBASE-KP4 link (one direction for one lane is illustrated)

94.3.6.2 PMD Transmit function

The PMD transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_i.request (i=0 to 3) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 94.3.12. A positive differential output voltage (SL*i*<p> minus SL*i*<n>) shall correspond to a positive tx_symbol value.

If the optional EEE capability is supported, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence is an ALERT frame (see 94.3.11.1) when tx_mode is set to ALERT. Regardless of tx_mode the transmit equalizer coefficients shall be set to the values determined via the start-up protocol (see 94.3.10).

94.3.6.3 PMD Receive function

The PMD receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_i.indication (i=0 to 3). A positive differential input voltage of (DL*i*<p> minus DL*i*<n>) shall correspond to a positive rx_symbol value.

94.3.6.4 Global PMD signal detect function

The variable Global_PMD_signal_detect is the logical AND of the values of PMD_signal_detect_i for i=0 to 3.

When the MDIO is implemented, this function maps the variable Global_PMD_signal_detect to the register and bit specified in 94.3.5.

94.3.6.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the 100GBASE-KP4 PMD to indicate the successful completion of the start-up protocol by the PMD control function (see 94.3.10). PMD_signal_detect_i (where i represents the lane number in the range 0 to 3) is set to zero when the value of the variable signal_detect is set to false by the Training state diagram for lane i (see Figure 72-5). PMD_signal_detect_i is set to one when the value of signal_detect for lane i is set to true.

If training is disabled by the management variable mr_training_enable (see 94.3.5), PMD_signal_detect_i shall be set to one for i=0 to 3.

If the optional EEE capability is supported, the following requirements apply. The value of PMD_signal_detect_i (for i=0 to 3) is set to zero when rx_mode is first set to QUIET. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall be set to one within 500 ns of the application of the ALERT pattern defined in 94.3.6.2 and meeting the EEE transmit-enabled amplitude requirement of 94.3.12.3. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall not be set to one when the output of the transmitter on the same lane meets the EEE transmit-disabled amplitude requirement of 94.3.12.3.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 94.3.5.

94.3.6.6 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if EEE deep sleep capability is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 94–13.

b) If a PMD fault (94.3.7) is detected, then the PMD may set Global_PMD_transmit_disable to one.

c) Loopback, as defined in 94.3.6.8, shall not be affected by Global_PMD_transmit_disable.

d) The following additional requirements apply when the optional EEE capability is supported. The Global PMD transmit disable function shall turn off all of the transmitters as specified in 94.3.12.3 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on all of the transmitters as specified in 94.3.12.3 when tx_mode transitions from QUIET to any other value.

94.3.6.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where i represents the lane number in the range 0 to 3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 94–13.

b) If a PMD_fault (94.3.7) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the electrical transmitter in each lane.

c) Loopback, as defined in 94.3.6.8, shall not be affected by PMD_transmit_disable_*i*.

94.3.6.8 Loopback mode

Local loopback mode is provided by the PMA (94.2.7). Loopback shall not affect the state of the transmitter, which continues to send data unless disabled (94.3.6.7).

NOTE 1—Placing a network port into loopback mode can be disruptive to a network.

94.3.7 PMD fault function

PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.1.

94.3.8 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault. A fault is indicated by setting the variable PMD_transmit_fault to one.

If PMD_transmit_fault is asserted, then Global_PMD_transmit_disable should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

94.3.9 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall contribute to the Receive fault bit as specified in 45.2.1.7.5.

94.3.10 PMD control function

94.3.10.1 Overview

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner.

The PMD control function is based upon the 10GBASE-KR start-up protocol. This protocol facilitates timing recovery and equalization while also providing a mechanism through which the receiver can tune the transmit equalizer to optimize performance over the backplane interconnect. The protocol supports these mechanisms through the continuous exchange of fixed-length training frames.

Each lane of the 100GBASE-KP4 PMD shall have an independent control function as defined in this subclause.

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1. If the MDIO interface is implemented, then this function shall map these variables to the appropriate bits in the BASE-R PMD status register (Register 1.151) as specified in 45.2.1.80.

94.3.10.2 Training frame structure

The training frame is a fixed length structure that is sent continuously during training. The training frame, shown in Figure 94–5, is 348 training frame words (94.3.10.3) in length and contains a frame marker, a control channel and training pattern. The frame marker delimits the beginning of a training frame. The control channel provides a means for the each receiver to control the taps on the link partner transmitter and communicate status. The training pattern provides content rich pattern for receiver convergence.

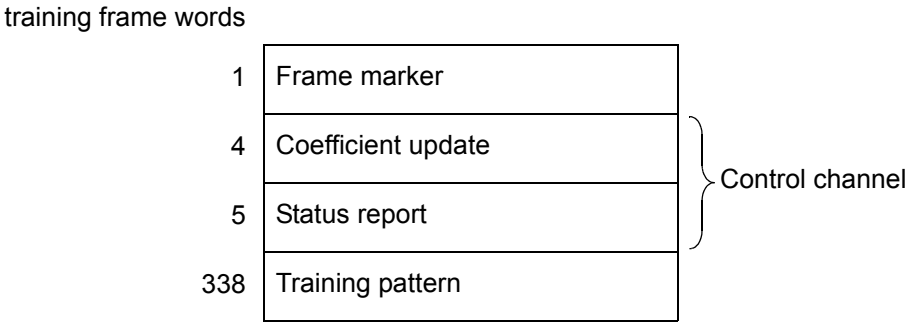


Figure 94–5—Training frame structure

94.3.10.3 Training Frame Words

Each training frame is composed of a series of 348 training frame words. Each training frame word is 46 symbols in length, equivalent in size to a termination block described in 94.2.2.4.

94.3.10.4 Frame marker

Each training frame shall be delimited by a frame marker as described in this subclause. The frame marker is a training frame word composed of a 46-symbol pattern of 23 +1 symbols followed by 23 -1 symbols. This pattern does not appear in the control channel or the training pattern and therefore serves as a unique indicator of the start of a training frame.

94.3.10.5 Control Channel Encoding

94.3.10.5.1 Differential Manchester Encoding

The control channel shall be transmitted using differential Manchester encoding (DME). DME guarantees transition density and DC balance while the reduced rate of transmission facilitates reception over non-optimally equalized channels.

DME cells shall be encoded using the following rules:

a) Each DME cell represents one bit of information.
b) The upper value is represented by a series of PAM4 +1 symbols.
c) The lower value is represented by a series of PAM4 -1 symbols.
d) A data transition occurs at each cell boundary.
e) A mid-cell data transition is used to signal a logical one.

f) The absence of a mid-cell data transition is used to signal a logical zero.

If a coding violation is detected within the bounds of the control channel in a given training frame, the contents of the control channel for that frame shall be ignored.

94.3.10.5.2 Control Channel Structure

The control channel shall be constructed of a series of DME cells as described in this subclause.

The control channel is composed of a series of 9 training frame words. Each training frame word is composed of 4 10-symbol control channel DME cells and a 6-symbol control overhead DME cell.

The control overhead cell is always transmitted as a one following the DME rules. In other words, the control overhead cell is transmitted as either three +1 symbols followed by three -1 symbols or vice versa depending on the previously transmitted control channel cell.

The coefficient update field is transmitted in the first 16 control channel DME cells. The status report field is transmitted in the next 24 control channel DME cells. The structure of the frame marker and control channel are shown in Table 94–8.

Table 94–8—Frame marker and control channel structure

Training frame word	Symbols 1:10	Symbols 11:20	Symbols 21:30	Symbols 31:40	Symbols 41:46	Training frame fields
1	cell 15	cell 14	cell 13	cell 12	overhead	coefficient update
2	cell 11	cell 10	cell 9	cell 8	overhead	
3	cell 7	cell 6	cell 5	cell 4	overhead	
4	cell 3	cell 2	cell 1	cell 0	overhead	
5	cell 19	cell 18	cell 17	cell 16	overhead	status report
6	cell 15	cell 14	cell 13	cell 12	overhead	
7	cell 11	cell 10	cell 9	cell 8	overhead	
8	cell 7	cell 6	cell 5	cell 4	overhead	
9	cell 3	cell 2	cell 1	cell 0	overhead	

94.3.10.6 Coefficient update field

The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer. The field consists of preset controls, initialization controls, coefficient updates for three transmit equalizer taps, and parity. The coefficient update field is mapped into the first 16 control channel DME

The format of the coefficient update field shall be as shown in Table 94–9. Cell 15 of the coefficient update field shall be transmitted first. The preset, initialize, and coefficient update fields are set by the receiver adaptation process. The algorithm employed by the receiver adaptation process is beyond the scope of this standard.

Table 94–9—Coefficient update field

Cell(s)	Name	Description
15:14	Reserved	Transmitted as 0, ignored on reception.
13	Preset	1 = Preset coefficients 0 = Normal operation
12	Initialize	1 = Initialize coefficients 0 = Normal operation
11:7	Reserved	Transmitted as 0, ignored on reception.
6	Parity	Even parity of all other coefficient update cells.
5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold

94.3.10.6.1 Preset

The behavior in response to the preset field shall be as specified in 72.6.10.2.3.1.

94.3.10.6.2 Initialize

The behavior in response to the initialize field shall be as specified in 72.6.10.2.3.2, except that the conditions for the INITIALIZE state are specified in 94.3.12.6.4 instead of 72.6.10.4.2.

94.3.10.6.3 Parity

The parity bit shall be set so that all bits in the coefficient update field including the parity bit exhibit even parity. The parity bit protects against acceptance of errored control messages and preserves DC balance. If a parity violation is detected within a received coefficient update field, that field shall not be used to update the transmitter coefficients.

94.3.10.6.4 Coefficient (k) update

The coefficient update fields shall be encoded as described in this subclause.

Each coefficient, identified by the index k, is assigned a 2-bit field describing a requested update, where $k \in \{-1, 0, 1\}$ denoting the pre-cursor, main, and post-cursor taps, respectively. The encoding of the coefficient update fields are as shown in Table 94–9.

Three request encodings are defined: increment, decrement, and hold. The default state of each tap is hold, which corresponds to no change in the coefficient. The increment or decrement encodings are transmitted to request that the corresponding coefficient be increased or decreased. The amount of change implemented by the transmitter in response to the coefficient update request meets the requirements of 94.3.12.6.5. An increment or decrement request is transmitted continuously until the update status (94.3.10.7.4) for that tap indicates updated, maximum, or minimum. At that point, the outgoing requests for that tap may be set to hold. The hold setting must be maintained until the incoming status message for that tap reverts to not_updated. A new request to increment or decrement a tap may be sent only when the incoming status message for that tap is not_updated.

Coefficient increment and decrement update requests must not be sent in combination with initialize or preset.

94.3.10.7 Status report field

The status report field is used to signal state information from the local PMD to the link partner. The format of the status report field of training frames shall be as shown in Table 94–10. Cell 19 of the status report field shall be transmitted first.

Table 94–10—Status report field for training and alert frames

Cell(s)	Name	Description
19	Parity	Set to achieve even parity for status report field.
18	Mode	0: Training 1: EEE
17:16	Frame countdown	Number of frames remaining before transition to data mode.
15:13	PMA alignment offset	Relative location of the next alert frame within the PMA frame (set to zero for training frames).
12:7	Reserved	Transmitted as zeros.
6	Receiver ready	1 = The local receiver has determined that training is complete and is prepared to receive data. 0 = The local receiver is requesting that training continue.
5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated (and for EEE alert frames)
3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated (and for EEE alert frames)
1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated (and for EEE alert frames)

94.3.10.7.1 Parity

The parity cell shall be set so that all bits in the status report field including the parity bit exhibit even parity. The parity bit protects against acceptance of errored status messages and preserves DC balance. If a parity violation is detected within a received status field, that field shall not be used to determine the link partner status.

94.3.10.7.2 Training frame countdown

The training frame countdown cell shall signal the transition from training to data mode as described in this subclause. When training begins, countdown is set to the value 3 and remains so until all receivers have completed training. When the received status report receiver ready is 1 in all four received lanes and the transmitted status report receiver ready is 1 in all four transmitted lanes, the transmitter on each transmitted lane will decrement the countdown in three successive frames. The countdown values will be equal in all four lanes. In other words, in the last three training frames countdown will contain 2, 1, and 0, respectively. Immediately after the last training frame word of the last training frame is sent, transmission of the PMA frame will begin starting with the termination block containing the PMA overhead (see 94.3.10.9).

94.3.10.7.3 Receiver Ready

The receiver ready bit shall signal the local receiver state to the link partner as described in this subclause. When training begins the receiver ready bit will be de-asserted and remain so until the receiver has concluded training. The receiver ready bit will be asserted to indicate that the local receiver has concluded training and is prepared to receive data. The encoding of the receiver ready bit is as shown in Table 94–10.

94.3.10.7.4 Coefficient (k) status

The behavior of the coefficient (k) status fields shall be as specified in 72.6.10.2.4.5.

94.3.10.7.5 Coefficient update process

The coefficient update process shall behave as specified in 72.6.10.2.5.

In addition, when frame_lock_i is TRUE for lane i (where i represents the lane number in the range 0 to 3), the period from receiving a new request to responding to that request shall be less than 2 ms. The start of the period is the frame marker of the training frame with the new request and the end of the period is the frame marker of the training frame with the corresponding response. A new request occurs when the coefficient update field is different from the coefficient field in the preceding frame. The response occurs when the coefficient status report field is updated to indicated that the corresponding action is complete.

94.3.10.8 Training Pattern

The training pattern shall be encoded as specified in this subclause.

The training pattern is mapped into a series of 338 training frame words. Each training frame words is encoded as a PMA signal as specified in 94.2.2 with the exception that the input is from a PRBS13 generator rather than from the PMA service interface and no PMA overhead (94.2.2.2) is inserted.

For each training frame, the PRBS13 generator is used to produce 31096 bits. Three full cycles of 8191 bits and one truncated cycle of 6523 bits are concatenated to form the 31096 bit sequence, R(1:31096). Bits in the first and third cycle, R(1:8191) and R(16383:24573), are not inverted and bits in the second and fourth cycles, R(8192:16382) and R(24574:31096), are inverted.

The PRBS13 pattern generator produces the same result as the implementation shown in Figure 94–6, which implements the generator polynomial shown in Equation (94–2). The PRBS13 pattern generator is initialized for each frame using a unique seed for each lane. The 13-bit seed and the initial 16 bits for each lane are annotated in Table 94–11.

$$G(x) = 1 + x + x^2 + x^{12} + x^{13} \quad (94–2)$$

The PRBS13 pattern is mapped into the 92 bits of each training frame word. The first 2 bits of each training frame word form the termination bits (94.2.2.4) and each training frame word in the training pattern is equivalent to a termination block (94.2.2.4). The resulting termination blocks are gray-mapped (94.2.2.5), precoded (94.2.2.6), and mapped to PAM4 levels (94.2.2.7).

The outputs of PRBS13 generator, gray mapper, and precoder for the first two training frame words are provided in Table 94–12.

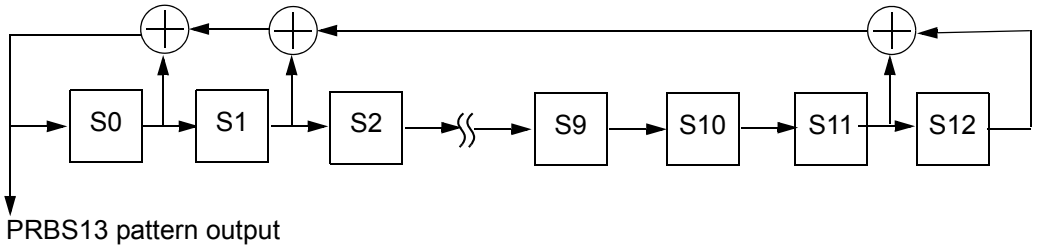


Figure 94–6—PRBS13 pattern generator

Table 94–11—PRBS13 seeds and initial output

PMD Lane	Seed bits (leftmost bit in S0, rightmost in S12)	Initial 16 bits (in order of transmission)
0	0000010101011	0100100110110011
1	0011101000001	1101111101010100
2	1001000101100	1100101111000011
3	0100010000010	0110111101000111

94.3.10.9 Transition from training to data

The transmitted signal shall transition from the training signal to normal data as described in this subclause.

The transition from the training signal to normal data occurs when the training countdown is complete, as indicated by the a training frame countdown being equal to 0 (94.3.10.7.2). Immediately after the last bit of the last training frame, transmission of the first PMA frame (94.2.2.4) begins with the termination block containing the overhead, T(i,1,1:92). The PRBS13 generator used during training to generate the training pattern is used to generate the termination bits in data mode. The state of the training PRBS13 generator is retained and 92 new bits are generated without re-seeding or inverting. Termination bits are assigned and the

Table 94–12—Training pattern initial sequences

PMD Lane	Output of	Contents of first (top) and second (bottom) training frame words transmitted left to right
0	PRBS13	0100100110110011110001010101100001001001110111100111010000011 10100110111010011100110010101 11 00011111110101110110111111010001011011111010011111011001010110 01110010011100001111000011101011
	Gray code	10313202201111301031212312100121021210231311 12 01222112132221011322331232033202310230123013 32
	Precoder	13012002001010310032011233222332201100210323 20 01111011033332232111210211303311231122330012 11
1	PRBS13	11011111010101000000100100110110011111000101010110000100100111 01111001110100000111010011011 10 10011100110010101110001111111010111011011111101000101101111 10 10011110110010101100111001001 11
	Gray code	21221110003102131230333200310232202330023313 23 31202033230222332321223303212210221311131203 12
	Precoder	23332322221002301122121131231120220300021230 21 32002212031111211201112130233322023010123312 33
2	PRBS13	11001011110000111110111011101100110011001100111000111000110000110 00011101110000011001100000001 110 00110110000110001010110001100100111010101000110010010000111 00 11110111010101100110010010101 01
	Gray code	20322002232323202020230230200200232300202000 23 02130130332013102333302031002312323332020311 11
	Precoder	22111311120330220022031122000222033000220000 21 02300122120012311212133123133011203033113010 10
3	PRBS13	01101111010001111011111010110011011111100011110110101110111 10 01000010110001011001010111 1000 10010110101111001010010110001001111100001010110101100100111 11 10001010110111010010001011111 00
	Gray code	13221012322332021223022133232203011303203322 30 31133220331130312200332113102220111323310112 20
	Precoder	12023102111211332021333212033312232130222120 213 32303331210122102000302321002022323021231011 13

PRBS13 generator continues to operate as specified in 94.2.2.4. The transition from training to data mode and mapping of the PRBS13 to training frame and termination bits is depicted in Figure 94–7.

94.3.10.10 Frame lock state diagram

The 10GBASE-KP4 PMD shall implement the Frame Lock state diagram as depicted in Figure 72–4 including compliance with the associated state variables, timers, counters, and functions specified in 72.6.10.3. The frame lock state diagram determines when the PMD control function has detected the frame boundaries in the received data stream.

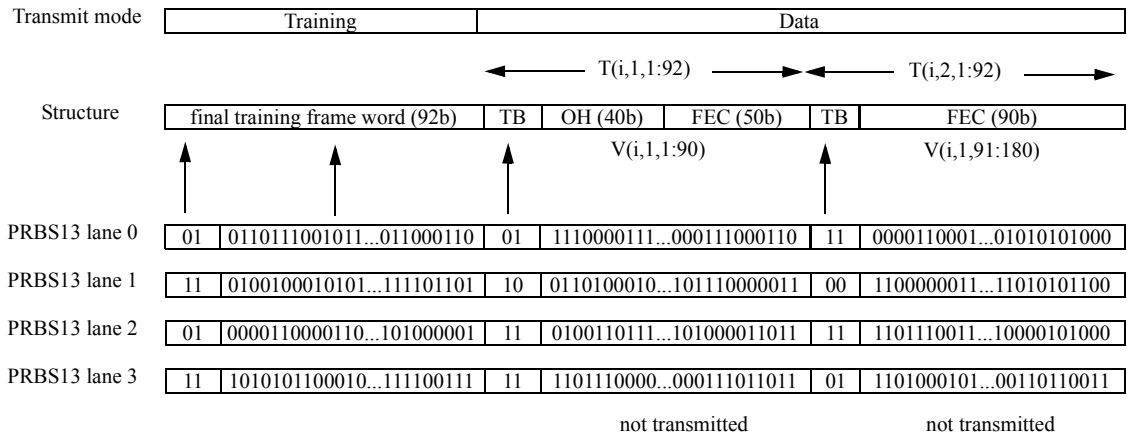


Figure 94–7—Transition from training to data mode

94.3.10.11 Training state diagram

The 10GBASE-KP4 PMD shall implement the Training state diagram as depicted in Figure 72–5 including compliance with the associated state variables specified in 72.6.10.3. The training state diagram defines the operation of the 100GBASE-KP4 start-up protocol.

When the training state diagram enters the INITIALIZE state, the transmitter equalizer shall be configured such that the output meets the requirements of 94.3.12.6.4.

94.3.10.12 Coefficient update state diagram

For each tap, the 100GBASE-KP4 PMD shall implement an instance of the coefficient update state diagram in Figure 72–6 including compliance with the associated state variables as specified in 72.6.10.3. The coefficient update state diagram defines the process for updating transmit equalizer coefficients in response to requests from the link partner and also defines the coefficient update status to be reported in outgoing training frames.

94.3.11 PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD:IS_TX_MODE.request and PMD:IS_RX_MODE.request. Implementation of the function is optional. EEE capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in 45.2.7.13. The transmitter on the local device will inform the link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the link partner's transmitter and can change independent of the local transmitter states and transitions.

94.3.11.1 Alert Signal

During refresh and wake, to enable effective detection and quick receiver synchronization an alert frame is sent prior to sending normal PMA frames. The alert signal is a series of repeating alert frames.

The alert frame shall be composed of a frame marker, control channel, and training pattern as depicted in Figure 94–8. The alert frame is based on the training frame specified in 94.3.10.2. The distinguishing

differences are that the training pattern is truncated to 48 training frame words (4320 bits) and the coefficient update and status report fields are encoded differently. The alert frame is a total of 58 training frame words in length.

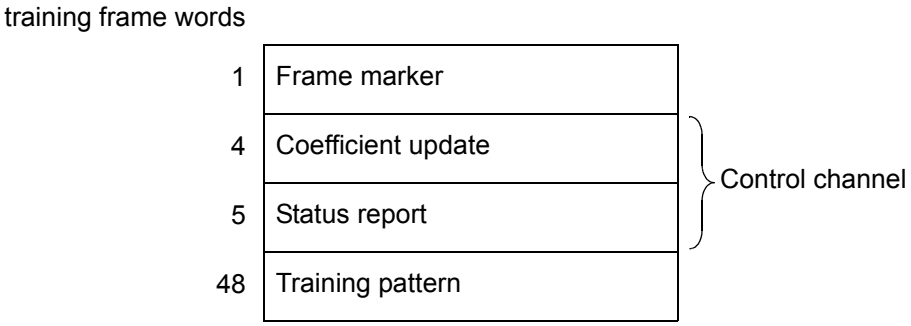


Figure 94–8—Alert frame structure

94.3.11.1.1 Frame marker

The frame marker shall be implemented as specified in 94.3.10.4.

94.3.11.1.2 Coefficient update field

The coefficient update field is unused in the alert frame. All bits in the coefficient update field are reserved and shall be transmitted as zeros.

94.3.11.1.3 Status report field

The status report field is used to signal state information from the local PMD to the link partner. The format of the status report field of alert frames shall be as shown in Table 94–10. Cell 19 of the status report field shall be transmitted first.

94.3.11.1.4 Parity

The parity field shall have the same behavior and purpose as specified for the training frame in 94.3.10.7.1.

94.3.11.1.5 Mode

The mode field indicates whether the frame is a training frame (mode = 0) or an alert frame (mode = 1). This field differentiates the alert frame from a training frame. The mode field in the alert frame shall always indicate 1.

94.3.11.1.6 Alert frame countdown

The alert frame countdown field shall be updated as specified for the training frame in 94.3.10.7.2. The alert frame countdown may be used by the receiver to determine when the signal will transition from the alert frame to the PMA frame (see 94.3.11.1.9).

94.3.11.1.7 PMA Alignment Offset

The PMA alignment offset (PAO) shall indicate the relative position in the PMA frame in relation to the beginning of the next alert frame as described in this subclause. The PMA alignment offset may be used by

the receiver to synchronize to the PMA frame without an additional frame synchronization process (see 94.3.11.1.9). The beginning of the PMA frame is defined as the termination block containing the PMA overhead (94.2.2.2).

The PMA frame length is exactly 6 times the alert frame length. The PMA alignment offset field indicates one of six offsets for the next alert frame within the PMA frame. The offset in number of training frame words of the next alert frame is determined by multiplying PMA alignment offset by 32. As a reference point, a PMA alignment offset of zero indicates that the start of the next alert frame is aligned with the start of a PMA frame. Valid values for the PMA alignment offset are {0,1,2,3,4,5}. The values {6,7} are not valid.

94.3.11.1.8 Receiver ready

The receiver ready cell shall always be set to 1 to indicate training is complete and the link is up.

94.3.11.1.9 Transition from alert to data

The transmitted signal shall transition from the alert signal to normal data as described in this subclause.

The transition from the alert signal to normal data occurs when the alert countdown is complete, as indicated by the alert frame countdown being equal to 0 (94.3.11.1.6). Immediately after the last bit of the last alert frame, transmission of the first PMA frame (94.2.2.4) begins with the termination block indicated by the PMA alignment offset, T(i,32*PAO,1:92). The PRBS13 generator used during alert to generate the training pattern is used to generate the termination bits in data mode. The state of the training PRBS13 generator is retained and 92 new bits are generated without re-seeding or inverting. Termination bits are assigned and the PRBS13 generator continues to operate as specified in 94.2.2.4. The transition from alert to data mode and mapping of the PRBS13 to alert frame and termination bits is depicted in Figure 94–9. The values for the PRBS13 in Figure 94–9 are specific to a transition with a PAO of zero. The values are different for other PAO values.

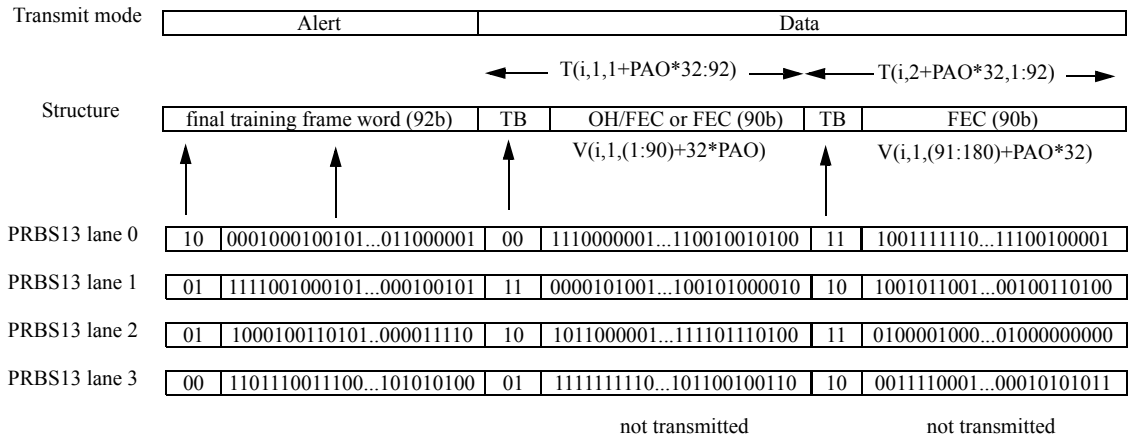


Figure 94–9—Transition from alert to data mode

94.3.12 PMD Transmitter electrical characteristics

Transmitter characteristics measured at TP0a are summarized in Table 94–13.

Table 94–13—Summary of transmitter characteristics at TP0a

Parameter	Subclause reference	Value	Units
Signaling rate	94.3.12.2	13.59375 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.) Transmitter disabled[a] Transmitter enabled	94.3.12.3	 30 1200	 mV mV
DC common-mode output voltage (max.)	94.3.12.3	1.9	V
DC common-mode output voltage (min.)	94.3.12.3	0	V
AC common-mode output voltage (RMS, max.)	94.3.12.3	30	mV
Differential output return loss (min.)	94.3.12.4	Equation (94–5)	dB
Common-mode output return loss (min.)	94.3.12.4	Equation (94–6)	dB
Transition time (20-80%, min.), no equalization[b]	94.3.12.5	18	ps
Output waveform Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized RMS linear fit error (max.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	94.3.12.6	 0.6 0.4 0.85 × v_f 0.025 0.0083 0.05 1.54 4	 V V V — — — — —
Far-end output noise (max.) Low insertion loss channel High insertion loss channel	94.3.12.7	 Equation (94–7) Equation (94–8)	 mV mV
Output jitter and linearity Clock random jitter, RMS Clock deterministic jitter, peak-to-peak Even-odd jitter Signal-to-noise-and-distortion ratio	 94.3.12.8.1 94.3.12.8.1 94.3.12.8.2 94.3.12.9	 0.005 0.05 0.03 19	 UI UI UI dB

[a]The transmitter for lane *i* is disabled when either Global_PMD_transmit_disable or PMD_transmit_disable_*i* is set to one.
[b]Transmit equalization may be disabled by asserting the preset control defined in Table 45–60 and 45.2.1.81.3.

94.3.12.1 Test Fixture

The test fixture of Figure 94–10 or its equivalent, is required for measuring the transmitter specifications described in 94.3.12.

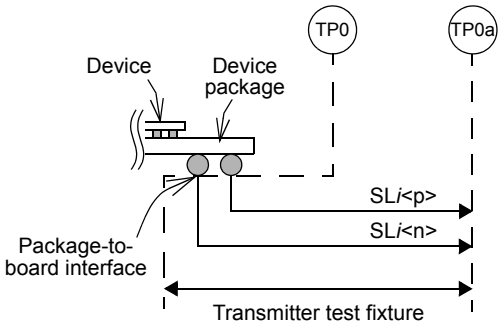


Figure 94–10—Transmitter test fixture and test points

94.3.12.1.1 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 94–10 shall be 100 Ω.

The differential return loss, in dB with f in GHz, of the test fixture shall meet the requirement of Equation (94–3).

$$RL(f) \geq \begin{cases} 20 - f & 0.05 \leq f \leq 5 \\ 15 & 5 < f \leq 13 \\ 20.57 - 0.4286f & 13 < f \leq 14 \end{cases} \quad (94–3)$$

The common-mode return loss, in dB with f in GHz, of the test fixture shall meet the requirement of Equation (94–4).

$$RL(f) \geq RL_{\max}(f) = 10 \qquad 0.05 \leq f \leq 14 \quad (94–4)$$

94.3.12.1.2 Test fixture insertion loss

The insertion loss of the test fixture measured at 12.89 GHz shall be between 1.2 dB and 1.6 dB.

The insertion loss deviation of the test fixture from 0.05 GHz to 10 GHz shall be less than 0.1 dB.

A test system with a fourth-order Bessel-Thomson low-pass response with 17 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

94.3.12.2 Signaling rate and range

The 100GBASE-KP4 signaling rate shall be 13.59375 GBd ± 100 ppm per lane.

94.3.12.3 Signal levels

The differential output voltage v_{di} is defined to be SLi<p> minus SLi<n>. The common-mode output voltage v_{cmi} is defined to be one half of the sum of SLi<p> and SLi<n>. These definitions are illustrated by Figure 94–11.

For a QPRBS13 test pattern (94.2.9.3), the peak-to-peak differential output voltage shall be less than or equal to 1200 mV regardless of the transmit equalizer setting. The peak-to-peak differential output voltage shall be less than or equal to 30 mV when the transmitter is disabled (refer to 94.3.6.6 and 94.3.6.7).

The DC common-mode output voltage shall be between 0 V and 1.9 V with respect to signal ground. The AC common-mode output voltage shall be less than or equal to 30 mV RMS with respect to signal ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

If the optional EEE capability is supported, the following requirements also apply. The peak-to-peak differential output voltage shall be less than 30 mV within 500 ns of the transmitter being disabled.

When the transmitter transitions from disabled to enabled: (a) The amplitude of the frame marker of the third complete alert frame (see 94.3.11.1) after the transmitter is enabled shall be greater than 90% of the steady-state value (see 94.3.12.6.2), and (b) the transmitter output shall meet the requirements of 94.3.12 within 1 us of the transmitter being enabled.

When the transmitter is disabled, the DC common-mode output voltage shall be maintained to within ±150 mV of the value for the enabled transmitter.

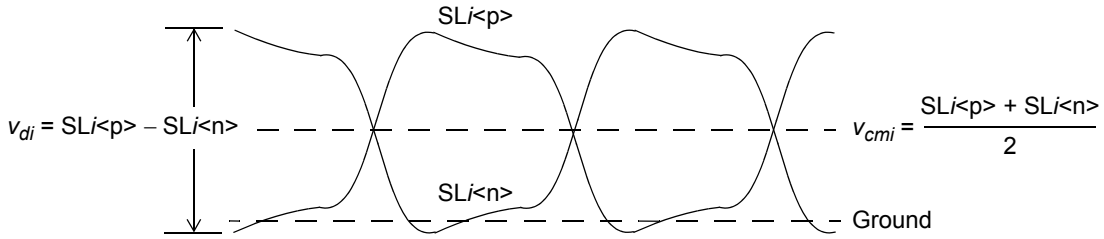


Figure 94–11—Transmitter output voltage definitions

94.3.12.4 Transmitter output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (94–5). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω

$$RL(f) \geq \left\{ \begin{array}{ll} 12.05 - f & 0.05GHz \leq f \leq 6GHz \\ 6.45 - 0.075f & 6GHz < f \leq 10GHz \end{array} \right\} \quad (94–5)$$

The common-mode output return loss, in dB, of the transmitter shall meet Equation (94–6). This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω

$$RL(f) \geq 6 \qquad 0.05GHz \leq f \leq 10GHz \quad (94–6)$$

94.3.12.5 Transition time

Transition times (rise and fall times) are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated edges.

The test pattern is QPRBS13 (see 94.2.9.3). The transitions within sequences of three –1 PAM4 symbols followed by three +1 PAM4 symbols and three +1 PAM4 symbols followed by three –1 PAM4 symbols are measured. The 0% level and the 100% level are as defined by the OMA measurement procedure (see 52.9.5) with the exception that differential voltage is measured rather than optical power and the test pattern has a shorter run length.

NOTE—This definition is not the same as the rise and fall times typically reported by an oscilloscope from an eye diagram, which take all the edges into account.

The transition times shall be greater than or equal to 18 ps when transmit equalization is disabled. Transmit equalization may be disabled by asserting the preset control defined in Table 45–60 and 45.2.1.81.3.

94.3.12.6 Transmitter output waveform

The 100GBASE-KP4 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 94–12.

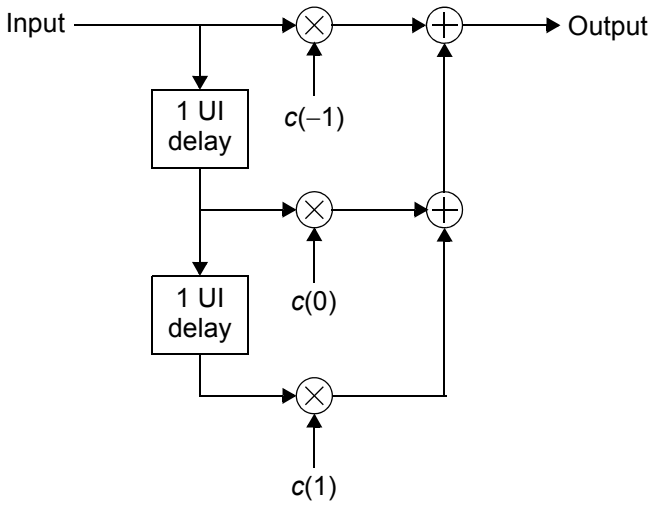


Figure 94–12—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 94.3.10 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

This command set includes instructions to:

Increment coefficient $c(i)$.
Decrement coefficient $c(i)$.
Hold coefficient $c(i)$ at its current value.
Set the coefficients to a pre-defined value (preset or initialize).

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that:

The requested update to coefficient $c(i)$ has completed (updated).
Coefficient $c(i)$ is at its minimum value.

Coefficient $c(i)$ is at its maximum value.
Coefficient $c(i)$ is ready for the next update request (not_updated).

94.3.12.6.1 Linear fit to the measured waveform

The following test procedure shall be followed to determine the linear fit pulse response, linear fit error, and normalized transmitter coefficient values.

1) The transmitter under test is preset as specified in 72.6.10.2.3.1 such that c(–1) and c(1) are zero and c(0) is its maximum value.
2) Configure the transmitter to transmit the QPRBS13 test pattern (94.2.9.3) and capture at least one complete cycle of the test pattern per 85.8.3.3.4 with the exception that the waveform should not be averaged.
3) Compute the linear fit to the captured waveform and the linear fit pulse response p(k) per 85.8.3.3.5. For aligned symbol values x(n) use -1, -1/3, 1/3, and 1 to represent symbol values of 0, 1, 2, and 3, respectively. The parameters of the pulse fit and the equalizing filter are given in Table 94–14.
4) Define t_x to be the time where the rising edge of p(k) from step 3 crosses 50% of its peak amplitude.
5) Sample p(k) at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the symbol-sampled pulse p_i.
6) Use p_i to compute the vector of coefficients, w, of a N_w-tap symbol-spaced transversal filter that equalizes for the transfer function from the transmit function to TP0a per 85.8.3.3.6.
7) Configure the transmitter equalizer with the next equalizer setting.
8) Same as step 2.
9) Same as step 3.
10) Same as step 4.
11) Same as step 5.
12) Equalize the sampled pulse p_i using the coefficient vector, w, computed in step 6 to yield the equalized pulse q_i. The normalized amplitude of coefficient c(–1) is the value of q_i at time $t_0 + (D_p - 1)$ UI. The normalized amplitude of coefficient c(0) is the value of q_i at time $t_0 + D_p$ UI. The normalized amplitude of coefficient c(1) is the value of q_i at time $t_0 + (D_p + 1)$ UI.
13) Repeat steps 7 and 12 for each supported transmitter equalizer setting.

Table 94–14—Linear fit pulse and equalizer parameters

Description	Symbol	Value	Units
Linear fit pulse length	N_p	8	UI
Linear fit pulse delay	D_p	2	UI
Equalizer length	N_w	8	UI
Equalizer delay	D_w	2	UI

94.3.12.6.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, p(k), is determined according to the linear fit procedure in 94.3.12.6.1. The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M, determined in step 3 of the linear fit procedure.

The steady-state voltage shall be greater than or equal to 0.4 V and less than or equal to 0.6 V.

The peak value of $p(k)$ shall be greater than $0.85 \times v_f$.

94.3.12.6.3 Linear fit error

The linear fit pulse peak, p(k), and the error between the linear fit and the measured waveform, e(k), are determined according to the linear fit procedure in 94.3.12.6.1.

For any configuration of the transmit equalizer, the RMS value of $e(k)$ normalized to the peak value of the linear fit pulse, $p(k)$, shall be less than or equal to 0.025.

94.3.12.6.4 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72-5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio (c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1)) is 1.29 ±10%, the ratio (c(0)-c(1)+c(-1))/(c(0)+c(1)+c(-1)) is 2.57 ±10%, and the steady-state voltage, v_f, (see 94.3.12.6) is greater than or equal to 140 mV. These requirements apply upon the assertion of a coefficient status report of "updated" for all coefficients.

94.3.12.6.5 Coefficient step size

The normalized amplitude of each coefficient c(i) is determined according to step 12 of the linear fit procedure in 94.3.12.6.1.

The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to "increment" that coefficient shall be between 0.0083 and 0.05. The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to "decrement" that coefficient shall be between –0.05 and –0.0083.

The change in the normalized amplitude of the coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (e.g., the coefficient update request for all coefficients is "hold") and the value upon the assertion of a coefficient status report of "updated" for that coefficient.

94.3.12.6.6 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient will reach a lower or upper bound based on the coefficient range or restrictions placed on the minimum steady-state differential output voltage or the maximum peak-to-peak differential output voltage.

With $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)–c(1))/(c(0)+c(1))$ shall be greater than or equal to 4.

With $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)–c(-1))/(c(0)+c(-1))$ shall be greater than or equal to 1.54.

Note that a coefficient may be set to zero by first asserting the preset control and then manipulating the other coefficients as required by the test.

94.3.12.7 Transmitter far-end output noise

The transmitter far-end output noise is a source of noise in addition to the channel integrated crosstalk noise (ICN) specified in 94.4.3. The transmitter far-end output noise is characterized using the procedure defined in 85.8.3.2.

The far-end transmitter output noise is measured using two reference channels:

A "low-loss" channel with insertion loss that satisfies the requirements of Test 1 in Table 94–16 and far-end integrated crosstalk noise, computed per 85.10.7, denoted as σ_l.
A "high-loss" channel with insertion loss that satisfies the requirements of Test 2 in Table 94–16 and far-end integrated crosstalk noise, computed per 85.10.7, denoted as σ_h.

For the low-loss channel, $RMSl_{dev}$ shall be less than or equal to the value given by Equation (94–7).

$$RMSl_{dev} = \sqrt{\sigma_l^2 + 0.67^2} \quad \text{mV} \tag{94–7}$$

For the high-loss channel, $RMSh_{dev}$ shall be less than or equal to the value given by Equation (94–7).

$$RMSh_{dev} = \sqrt{\sigma_h^2 + 0.33^2} \ \text{mV} \tag{94–8}$$

94.3.12.8 Transmitter output jitter

94.3.12.8.1 Clock Random Jitter and Clock Deterministic Jitter

Clock random jitter (CRJrms) measured at the transmitter output using the methodology described in this subclause shall be less than 0.005 UI RMS regardless of transmit equalization setting.

Clock deterministic jitter (CDJ) measured at the transmitter output using the methodology described in this subclause shall be less than 0.05 UI peak-to-peak regardless of transmit equalization setting.

CRJrms and CDJ are determined using the following procedure:

1) CRJrms and CDJ are measured using the JP03A test pattern (94.2.9.1).
2) Using appropriate test equipment and procedure capture the zero-crossing times, $T_{ZC}(i)$, of a pattern of length, N, of 10^7 symbols or greater.
3) Determine the average pulse width ΔT_{Avg} using Equation (94–9).
4) Determine the jitter series, $\tau(j)$, using Equation (94–10).
5) Apply the effect of a single-pole high-pass filter (20 dB per decade low-frequency response) with –3 dB gain at 1.6 MHz and peak gain of 3 dB at 6 MHz to the jitter samples to obtain $\tau_{HPF}(j)$.
6) Create a CDF as a function of $\tau_{HPF}(j)$.
7) From the CDF determine J_5 as the difference between τ_{HPF} at the $(1–0.5 \times 10^{-5})$ and 0.5×10^{-5} probabilities, respectively, and J_6 as the difference between τ_{HPF} at the $(1–0.5 \times 10^{-6})$ and 0.5×10^{-6} probabilities, respectively.
8) Calculate CRJrms and CDJ using the relationship in Equation (94–11).

$$\Delta T_{Avg} = \frac{T_{ZC}(N) - T_{ZC}(1)}{N - 1} \tag{94–9}$$

$$\tau(j) = T_{ZC}(j) - (j-1) \cdot \Delta T_{Avg} - T_{ZC}(1) \qquad j = 2, 3, \ldots N \tag{94–10}$$

$$\begin{bmatrix} CRJrms \\ CDJ \end{bmatrix} = \begin{bmatrix} 1.0538 & -1.0538 \\ -9.3098 & 10.3098 \end{bmatrix} \begin{bmatrix} J_6 \\ J_5 \end{bmatrix} \tag{94–11}$$

94.3.12.8.2 Even-Odd Jitter

Even-odd jitter (EOJ) measured at the transmitter output using the methodology described in this subclause shall be less than 0.03 UI peak-to-peak regardless of transmit equalization setting.

EOJ is determined using the following procedure:

1) EOJ is measured using the JP03B test pattern (94.2.9.2).
2) Using appropriate test equipment and procedure, capture the time for each of the 60 transitions.
3) Averaging of the vertical waveform or of each zero-crossing time is recommended to mitigate the contribution of uncorrelated noise and jitter.
4) Denote the averaged zero-crossing times as $T_{ZC}(i)$, where i = {1,2,...60} and where i = 1 designates the transition from 3 to 0 after the consecutive pair of symbols {3,3}.
5) The set of 40 pulse widths, $\Delta T(j)$, isolated from the double-width pulses are determined using the relationship in Equation (94–12).
6) EOJ is calculated using the relationship in Equation (94–13).

$$\Delta T(j) = \begin{cases} T_{ZC}(j+10) - T_{ZC}(j+9) & 1 \le j \le 20 \\ T_{ZC}(j+19) - T_{ZC}(j+18) & 21 \le j \le 40 \end{cases} \quad (94–12)$$

$$EOJ = \frac{\left| \sum_{j=1}^{20} \Delta T(2 \cdot j) - \sum_{j=1}^{20} \Delta T(2 \cdot j - 1) \right|}{40} \quad (94–13)$$

94.3.12.9 Transmitter output noise and distortion

Signal-to-noise-and-distortion ratio (SNDR) measured at the transmitter output using the methodology described in this subclause shall be greater than 19 dB for any allowable transmit equalizer setting.

1) Compute the linear fit to the captured waveform and the linear fit pulse response, $p(k)$, and error, $e(k)$, according to 94.3.12.6.1.
2) Calculate the standard deviation, $\sigma_e(m)$, for each phase, m={1, 2,...,M}, of the error $e(m+jM)$. This is the output noise and distortion error.
3) Calculate SNDR according to Equation (94–14).

$$SNDR = \frac{\max(p(k))}{3 \cdot \max(\sigma_e(m))} \quad (94–14)$$

94.3.13 PMD Receiver electrical characteristics

Receiver characteristics measured at TP5a are summarized in Table 94–15.

Table 94–15—Summary of receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min.)	94.3.13.2	Equation (94–5)	dB
Differential to common-mode return loss (min.)	94.3.13.2	Equation (94–15)	dB
Interference tolerance	94.3.13.3	Table 94–16	N/A
Jitter tolerance	94.3.13.4	Table 94–17	N/A

94.3.13.1 Test Fixture

The test fixture of Figure 94–13 or its equivalent is required for measuring the receiver specifications described in 94.3.13. The test fixture shall meet the requirements for insertion loss, insertion loss deviation, differential return loss, and common-mode return loss in 94.3.12.1.

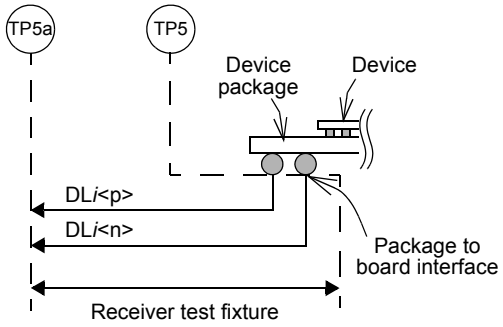


Figure 94–13—Receiver test fixture and test points

94.3.13.2 Receiver input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (94–5). The reference impedance for differential return loss measurements shall be 100 Ω

The differential to common-mode return loss, in dB, of the receiver shall meet Equation (94–15).

$$RL(f) \geq RL_{\max}(f) = \begin{cases} 25 - 1.44f & 0.05 \leq f \leq 6.95\,GHz \\ 15 & 6.95 \leq f \leq 10\,GHz \end{cases} \quad (94\text{–}15)$$

94.3.13.3 Receiver interference tolerance

Receiver interference tolerance is defined by the procedure in Annex 93C. The receiver on each lane shall meet the FEC symbol error ratio requirement with channels matching the COM and loss parameters for Test 1 and Test 2 in Table 94–16. Example fitted-insertion-loss curves for Test 1 and Test 2, as well as bounds resulting from the constraints on the fitted-insertion-loss coefficients with insertion loss at the limit specified for each test, are shown in Figure 94–14 and Figure 94–15 respectively. The parameter RSS_DFE4 in Table 94–16 is a figure of merit for the test channel that is defined by Equation (93A–47) (see 93A.2).

The following considerations apply to the interference tolerance test. The transmitter noise parameter is SNDR (see 94.3.12.9). The test transmitter meets the specifications in 94.3.12. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage (see 94.3.12.3) is less than 800 mV, the pre-cursor peaking ratio (see 94.3.12.6.6) is less than 1.54, and the post-cursor peaking ratio (see 94.3.12.6.6) is less than 4. The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz. The jitter parameters to be measured are CRJrms and CDJ (see 94.3.12.8.1). The COM parameter σ_{RJ} is set to the measured value of CRJrms and the COM parameter A_{DD} is set to half the measured value of CDJ. Other COM parameters are set according to the values in Table 94–18. The test pattern to be used is the scrambled idles test pattern. A test system with a fourth-order Bessel-Thomson low-pass response with 17 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

Table 94–16—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
FEC symbol error ratio[a]		3.3×10^{-3}		3.3×10^{-3}	
Test channel parameters:					
COM, including effects of broadband noise		1.5		1.5	dB
Insertion loss at 7 GHz[b]		14.4	33		dB
a_0[c]	–1.5	1	–1.5	2	dB
a_1	0	1.6	0	3.8	dB/√GHz
a_2	0	1.6	0	4.2	dB/GHz
a_4	0	0.03	0	0.065	dB/GHz^2
RSS_DFE4	0.05	—	0.05	—	—

[a]The FEC symbol error ratio is measured in step 11) of the interference tolerance test method in 93C.2.
[b]Measured between TPt and TP5 (see Figure 93C-4).
[c]Coefficients are determined from insertion loss measured between TPt and TP5 (see Figure 93C-4) using the methodology in 93A.3 with f_{min} of 0.05 GHz, f_{max} of 13.59375 GHz, and maximum Δf of 0.01 GHz.

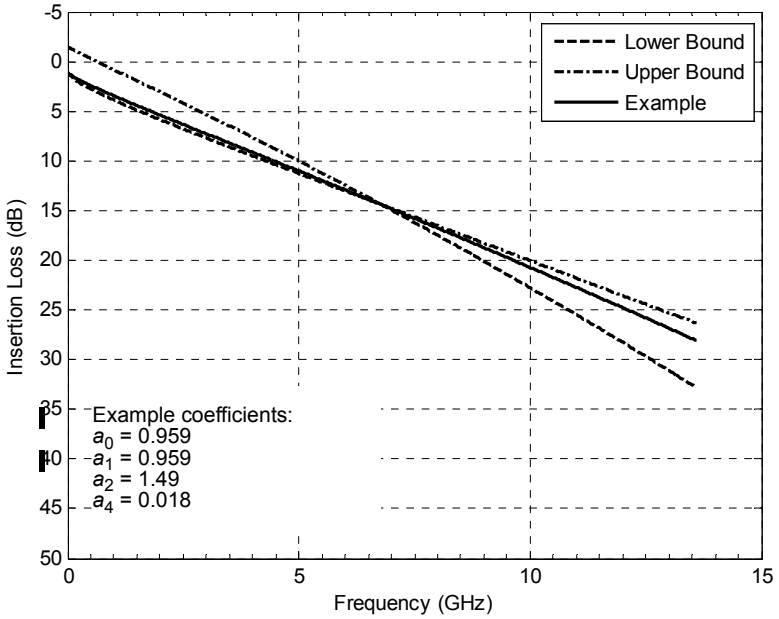


Figure 94–14—Insertion loss example and bounds for Test 1 channel

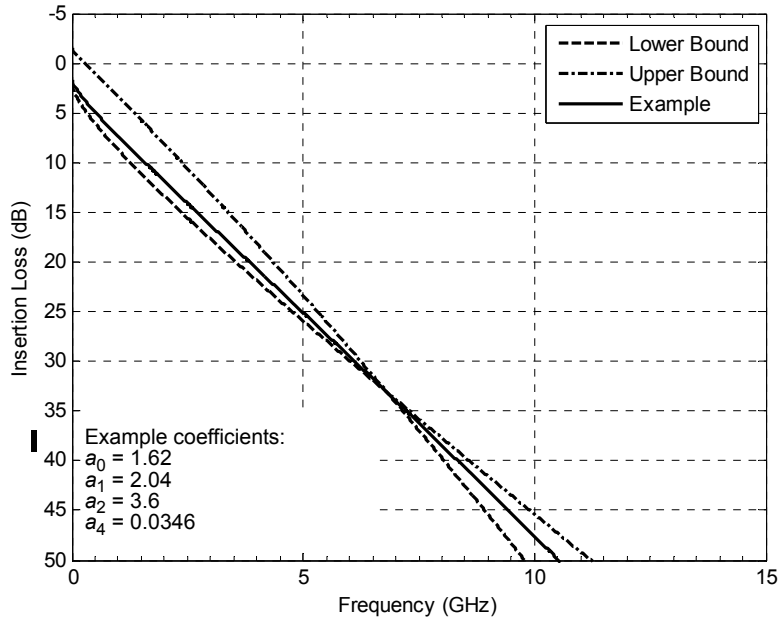


Figure 94–15—Insertion loss example and bounds for Test 2 channel

94.3.13.4 Receiver Jitter Tolerance

Receiver jitter tolerance is defined by the procedure defined in 94.3.13.4.2. The receiver FEC symbol error ratio shall be less than the maximum value for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 94–17.

Table 94–17—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Maximum FEC symbol error ratio[a]	3.3×10^{-3}	3.3×10^{-3}	
Jitter frequency	16	160	kHz
Jitter amplitude	5	0.5	UI

[a]The FEC symbol error ratio is measured in step 3) of the jitter tolerance test method in 94.3.13.4.2.

94.3.13.4.1 Test setup

Jitter tolerance is measured using the test setup in Figure 93C–2 on each lane. The transmitter output is constrained as described in 93C.1. The Tx and channel noise sources are disabled. The test channel (TPt to TP5 replica) meets the requirements for the channel used for Test 2 in 94.3.13.3. The low-frequency jitter specified in Table 94–17 is applied to the output of the transmitter and is measured at TPta.

94.3.13.4.2 Test method

The following jitter tolerance test method is repeated for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 94–17.

1) Configure the transmitter with the corresponding jitter frequency and amplitude from Table 94–17.
2) Initiate training on the receiver under test and allow training to complete.
3) Measure the FEC symbol error ratio on each lane using the errored symbol counter, FEC_symbol_error_*i*, where *i* is the lane under test.

94.4 Channel characteristics

94.4.1 Channel operating margin

The channel operating margin (COM) computed using the procedure in Annex 93A and the parameters in Table 94–18 shall be greater than or equal to 3 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

Table 94–18—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	13.59375	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_d z_p C_b	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02	 — — —

Table 94–18—Channel operating margin parameters

Parameter	Symbol	Value	Units
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	 dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	 0.4 0.4 0.6	 V V V
Number of signal levels	L	4	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	16	UI
Normalized DFE coefficient magnitude limit	$b_{max}(n)$	1 for n = 1 0.2 for n = 2 to N_b	—
Random jitter, RMS	σ_{RJ}	0.005	UI
Dual-Dirac jitter, peak	A_{DD}	0.025	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	3×10^{-4}	—

94.4.2 Channel insertion loss

The insertion loss, in dB, of the channel is recommended to meet Equation (94–16). The insertion loss limit is shown Figure 94–16.

$$IL(f) \le IL_{\max}(f) = \begin{cases} a_0 + a_1 \cdot \sqrt{f} + a_2 \cdot f + a_3 \cdot f^2 + a_4 \cdot f^3 & f_{\min} \le f \le f_2 \\ a_5 + a_6 \cdot (f - f_2) & f_2 < f \le f_{\max} \end{cases} \quad (94\text{–}16)$$

where

IL(f) is the insertion loss at frequency f
IL_{max}(f) is the maximum allowable insertion loss at frequency f
f is the measurement frequency in Hz
f_{min} = 0.05 GHz
f_2 = 7 GHz
f_{max} = 15 GHz
a_0 = 0.8
$a_1 = 1.7372 \times 10^{-4}$
$a_2 = 1.1554 \times 10^{-9}$
$a_3 = 2.7795 \times 10^{-19}$
$a_4 = -1.0423 \times 10^{-29}$
a_5 = 33.467
$a_6 = 1 \times 10^{-8}$

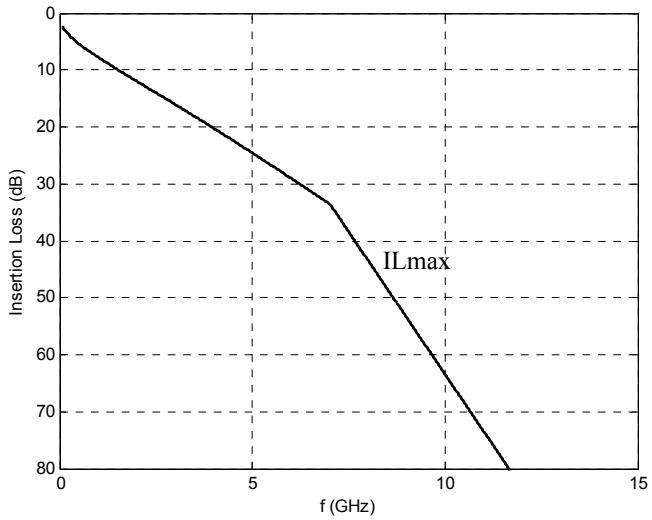


Figure 94–16—Channel Insertion Loss limit

94.4.3 Channel Return Loss

The return loss, in dB, of the channel is recommended to meet Equation (94–17). The return loss limit $RL_{max}(f)$ is shown Figure 94–17.

$$RL(f) \geq RL_{\min}(f) = \begin{cases} 12 & 0.05 \leq f \leq f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \leq f_b \end{cases} \quad (94–17)$$

where

RL(f) is the return loss at frequency f in dB
$RL_{min}(f)$ is the minimum allowable return loss in dB
f is the measurement frequency in GHz
f_b is the signalling rate (13.59375) in GHz

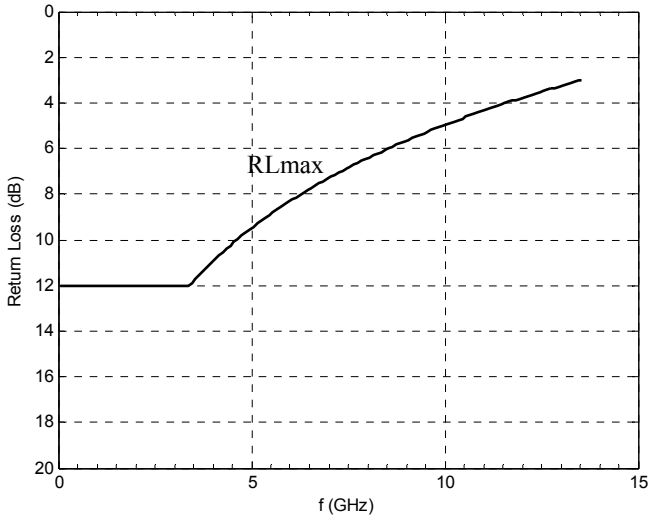


Figure 94–17—Channel Return Loss limit

94.4.4 Channel AC-coupling

The 100GBASE-KP4 transmitter shall be AC-coupled to the receiver. Common-mode specifications are defined as if the DC-blocking capacitor is implemented between TP0 and TP5. Should the capacitor be implemented outside TP0 and TP5, the common-mode specifications in Table 94–13 may not be appropriate.

The impact of a DC-blocking capacitor implemented between TP0 and TP5 is accounted for within the channel specifications. Should the capacitor be implemented outside TP0 and TP5, it is the responsibility of implementors to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance.

The low-frequency 3 dB cutoff of the AC coupling shall be less than 50 kHz.

94.5 Environmental specifications

94.5.1 General safety

All equipment subject to this clause shall conform to applicable sections (including isolation requirements) of IEC 60950-1.

94.5.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

94.5.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

94.5.4 Electromagnetic compatibility

A system integrating the 100GBASE-KP4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

94.5.5 Temperature and humidity

A system integrating the 100GBASE-KP4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

94.6 Protocol implementation conformance statement (PICS) proforma for Clause 94., Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KP4[13]

94.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 94, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KP4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

94.6.2 Identification

94.6.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

94.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bj-20XX, Clause 94, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KP4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bj-20XX.)	

Date of Statement	

[13] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

94.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CGMII	CGMII	94.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100GBASE-R PCS	94.1		M	Yes [ ]
RS-FEC	100GBASE-R RS-FEC	94.1		M	Yes [ ]
PMA	100GBASE-R PMA	94.1		O	Yes [ ] No [ ]
CAUI	CAUI	94.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-negotiation	94.1		M	Yes [ ]
*MD	MDIO capability	94.3.5	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE capability	94.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	94.3.6.6	Function is supported	O	Yes [ ] No [ ]
*LTD	PMD lane-by-lane transmit disable function	94.3.6.7	Function is supported	O	Yes [ ] No [ ]
*PDI	Physically instantiated PMD service interface	94.3.4	Interface is supported	O	Yes [ ] No [ ]

94.6.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KP4

94.6.4.1 PMA functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
AFS1	Overhead frame	94.2.2.2	Transmitter maps FEC bits to overhead frame	M	Yes [ ]
AFS2	Overhead	94.2.2.3	Transmitter maps sequence overhead bits	M	Yes []
AFS3	Termination blocks	94.2.2.4	Transmitter maps overhead frame bits to termination blocks.	M	Yes [ ]
AFS4	Gray mapping	94.2.2.5	Transmitter maps each pair of termination block bits to Gray-mapped symbols	M	Yes [ ]
AFS5	Precoder	94.2.2.6	Transmitter precodes each Gray-mapped symbol	M	Yes [ ]
AFS6	PAM4 encoder	94.2.2.7	Transmitter maps each pre-coded symbol to PAM4 levels	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
AFS7	Transmit symbols	94.2.2.8	Transmitter sends each PAM4 symbol to the PMD.	M	Yes [ ]
AFS8	Recover data	94.2.3	Receiver recovers data, meet performance requirements, and removes termination bits and overhead.	M	Yes [ ]
AFS9	Overhead	94.2.3.1	Recover overhead sequence	M	Yes []
AFS10	Link status	94.2.6	Provide link status to PMA client via PMA:IS_SIGNAL.indication primitive.	M	Yes [ ]
AFS11	PMA local loopback	94.2.7	Provide loopback from PMA SI input to PMA SI output.	M	Yes [ ]
AFS12	PMA remote loopback	94.2.8	Provide loopback from PMA SI output to PMA SI input.	O	Yes [ ] No [ ]
AFS13	JP03A pattern	94.2.9.1	Provide JP03A test pattern.	M	Yes [ ]
AFS14	JP03B pattern	94.2.9.2	Provide JP03B test pattern.	M	Yes [ ]
AFS15	QPRBS13 test pattern	94.2.9.3	Provide QPRBS13 test pattern	M	Yes [ ]
AFS16	PMA control variables	94.2.10	Map PMA control variables to MDIO per Table 94–4.	MD:M	Yes [ ] N/A [ ]
AFS17	PMA status variables	94.2.10	Map PMA status variables to MDIO per Table 94–5.	MD:M	Yes [ ] N/A [ ]

94.6.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DFS1	SIGNAL_OK assignment	94.3.1.3.1	Set SIGNAL_OK based on Global_PMD_signal_detect	M	Yes[]
DFS2	Sum of receive and transmit delays in one direction for PMA, PMD, and AN.	94.3.3	Less than 8192 bit times.	M	Yes [ ]
DFS3	Skew at SP2	94.3.4	Less than 43 ns	PDI:M	Yes [ ]
DFS2	Skew variation at SP2	94.3.4	Less than 0.4 ns	PDI:M	Yes [ ]
DFS3	Skew at SP3	94.3.4	Less than 54 ns	M	Yes [ ]
DFS4	Skew variation at SP3	94.3.4	Less than 0.6 ns	M	Yes [ ]
DFS5	Skew at SP4	94.3.4	Less than 134 ns	M	Yes [ ]
DFS6	Skew variation at SP4	94.3.4	Less than 3.4 ns	M	Yes [ ]
DFS7	Skew at SP5	94.3.4	Less than 145 ns	PDI:M	Yes [ ]
DFS8	Skew variation at SP5	94.3.4	Less than 3.6 ns	PDI:M	Yes [ ]
DFS9	PMD control variables	94.3.5	Map PMD control variables to MDIO per Table 94–6.	MD:M	Yes [ ] N/A [ ]
DFS10	PMD status variables	94.3.5	Map PMD status variables to MDIO per Table 94–7.	MD:M	Yes [ ] N/A [ ]
DFS11	Transmit function	94.3.6.2	Convert 4 bit streams from PMD SI to 4 electrical streams at the MDI.	M	Yes [ ]
DFS12	Transmit symbol value	94.3.6.2	A positive value for SLi<p> minus SLi<n> corresponds to a positive symbol value.	M	Yes [ ]
DFS13	Transmit EEE alert signal	94.3.6.2	Send ALERT frame	EEE:M	Yes [ ] N/A [ ]
DFS14	Transmit EEE alert transmitter setting	94.3.6.2	Using coefficients determined during start-up	EEE:M	Yes [ ] N/A [ ]
DFS15	Receive function	94.3.6.3	Convert 4 electrical bit streams from MDI to 4 bit streams at the PMD SI.	M	Yes [ ]
DFS16	Receive symbol value	94.3.6.3	A positive value for DLi<p> minus DLi<n> corresponds to a positive symbol value.	M	Yes [ ]
DFS17	Signal detect parameter	94.3.6.4	Continuously send SIGNAL_DETECT to PMD SI.	M	Yes [ ]
DFS18	PMD_signal_detect_i when training is disabled by management	94.3.6.5	Set to one for all lanes.	M	Yes []
DFS19	PMD_signal_detect_i assertion time	94.3.6.5	Within 500 ns of compliant signal.	EEE:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
DFS20	PMD_signal_detect_i when transmitter is disabled	94.3.6.5	Not asserted when transmitter output meets requirements for disabled state.	EEE:M	Yes [ ] N/A [ ]
DFS22	Global_PMD_transmit_disable variable	94.3.6.6	When set to one, all transmitters satisfy the requirements of 94.3.12.3.	GTD:M	Yes [ ] N/A [ ]
DFS21	Loopback when transmitter disabled	94.3.6.6	Loopback not affected.	GTD:M	Yes [ ] N/A [ ]
DFS22	Transmitter output on transition to QUIET	94.3.6.6	Turn off and meet requirements in 94.3.12.3.	EEE:M	Yes [ ] N/A [ ]
DFS23	Transmitter output on transition from QUIET	94.3.6.6	Turn on and meet requirements in 94.3.12.3.	EEE:M	Yes [ ] N/A [ ]
DFS24	PMD_transmit_disable_*i* variable	94.3.6.7	When set to one, the transmitter for lane *i* satisfies the requirements of 94.3.12.3	LTD:M	Yes [ ] N/A [ ]
DFS25	PMD lane-by-lane transmit disable function affect on loopback	94.3.6.7	No effect	LTD:M	Yes [ ] N/A [ ]
DFS26	Loopback mode	94.3.6.8	Provided in adjacent PMA.	M	Yes [ ]
DFS27	Loopback effect	94.3.6.8	Does not affect transmitter.	M	Yes [ ]
DFS28	PMD_fault variable mapping to MDIO	94.3.7	Mapped to the fault bit as specified in 45.2.1.2.1	MD:M	Yes [ ] N/A [ ]
DFS29	PMD_transmit_fault variable mapping to MDIO	94.3.8	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
DFS30	PMD_receive_fault variable mapping to MDIO	94.3.9	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
DFS31	Control function	94.3.10.1	Independent per lane	M	Yes [ ]
DFS32	Training variables	94.3.10.1	Map to MDIO bits per 45.2.1.80.	MD:M	Yes [ ] N/A [ ]
DFS33	Training frame marker	94.3.10.4	Frame marker encoded per 94.3.10.4.	M	Yes [ ]
DFS34	Training frame control channel encoding	94.3.10.5.1	Differential manchester encoding	M	Yes [ ]
DFS35	Training frame control channel DME	94.3.10.5.1	Encoded based on rules in 94.3.10.5.1.	M	Yes [ ]
DFS36	Training frame coding violation	94.3.10.5.1	Discard control channel if there is any coding violation.	M	Yes [ ]
DFS37	Training frame control channel structure	94.3.10.5.2	Series of DME cells specified in 94.3.10.5.2.	M	Yes [ ]
DFS38	Training frame coefficient update field	94.3.10.6	Format per Table 94–9.	M	Yes [ ]
DFS39	Training frame coefficient transmission order.	94.3.10.6	Cell 15 first.	M	Yes [ ]
DFS40	Training frame preset	94.3.10.6.1	Response per 72.6.10.2.3.1.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
DFS41	Training frame initialize	94.3.10.6.2	Response per 72.6.10.3.2 and conditions per 94.3.12.6.4.	M	Yes [ ]
DFS42	Training frame coefficient update parity	94.3.10.6.3	Set for even parity in coefficient update field.	M	Yes [ ]
DFS43	Training frame coefficient update parity violation	94.3.10.6.3	Discard control channel if parity violation.	M	Yes [ ]
DFS44	Training frame coefficient (k) update	94.3.10.6.4	Encoded per 94.3.10.6.4.	M	Yes [ ]
DFS45	Training and alert frame status report field	94.3.10.7	Format per Table 94–10.	M	Yes [ ]
DFS46	Training frame status transmission order.	94.3.10.7	Cell 19 first.	M	Yes [ ]
DFS47	Training frame status report parity	94.3.10.7.1	Set for even parity in status report field.	M	Yes [ ]
DFS48	Training frame status report parity violation	94.3.10.7.1	Discard control channel if parity violation.	M	Yes [ ]
DFS49	Training frame countdown.	94.3.10.7.2	Indicate transition per 94.3.10.7.2.	M	Yes [ ]
DFS50	Training frame receiver ready	94.3.10.7.3	Signal local receiver state per 94.3.10.7.3.	M	Yes [ ]
DFS51	Training frame coefficient status	94.3.10.7.4	Behavior per 72.6.10.2.4.5.	M	Yes [ ]
DFS52	Training frame coefficient update process	94.3.10.7.5	Update coefficients per 72.6.10.2.5.	M	Yes [ ]
DFS53	Coefficient update response time	94.3.10.7.5	Respond in less than 2 ms.	M	Yes [ ]
DFS54	Training frame training pattern	94.3.10.8	Encode per 94.3.10.8.	M	Yes [ ]
DFS55	Signal on transition from training mode to data mode	94.3.10.9	Signal according to 94.3.10.9.	M	Yes [ ]
DFS56	Training frame lock state diagram	94.3.10.10	Implement per Figure 72–4 and 72.6.10.3.	M	Yes [ ]
DFS57	Training state diagram	94.3.10.11	Implement per Figure 72–5 and 72.6.10.3.	M	Yes [ ]
DFS58	Transmitter setting in INITIALIZE state	94.3.10.11	Transmitter configured according to 94.3.12.6.4.	M	Yes [ ]
DFS59	Coefficient update state diagram.	94.3.10.12	Implement per Figure 72–6 and 72.6.10.3.	M	Yes [ ]
DFS60	Alert frame	94.3.11.1	Structure per Figure 94–8.	EEE:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
DFS61	Alert frame marker	94.3.11.1.1	Implement per 94.3.10.4.	EEE:M	Yes [ ] N/A [ ]
DFS62	Alert frame coefficient update field	94.3.11.1.2	Transmitted as all zeros.	EEE:M	Yes [ ] N/A [ ]
DFS63	Alert frame status report field	94.3.11.1.3	Format per Table 94–10.	EEE:M	Yes [ ] N/A [ ]
DFS64	Alert frame status report field order of transmission	94.3.11.1.3	Transmit cell 19 first.	EEE:M	Yes [ ] N/A [ ]
DFS65	Alert frame status report parity	94.3.11.1.4	Behavior per 94.3.10.7.1.	EEE:M	Yes [ ] N/A [ ]
DFS66	Alert frame mode	94.3.11.1.5	Always set to 1.	EEE:M	Yes [ ] N/A [ ]
DFS67	Alert frame countdown	94.3.11.1.6	Indicate transition per 94.3.10.7.2.	EEE:M	Yes [ ] N/A [ ]
DFS68	Alert frame PMA alignment offset	94.3.11.1.7	Indicate relative position of PMA frame and encoded per 94.3.11.1.7.	EEE:M	Yes [ ] N/A [ ]
DFS69	Alert frame receiver ready	94.3.11.1.8	Always set to 1.	EEE:M	Yes [ ] N/A [ ]
DFS70	Signal on transition from alert to data mode	94.3.11.1.9	Signal according to 94.3.11.1.9.	M	Yes [ ]

94.6.4.3 PMD transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture impedance	94.3.12.1.1	100 Ω	M	Yes [ ]
TC2	Test fixture differential return loss	94.3.12.1.1	Equation (94–3)	M	Yes [ ]
TC3	Test fixture common-mode return loss	94.3.12.1.1	Equation (94–4)	M	Yes [ ]
TC4	Test fixture differential insertion loss	94.3.12.1.2	≥ 1.2 dB and ≤ 1.6 dB at 12.89 Ghz.	M	Yes [ ]
TC5	Test fixture insertion loss deviation	94.3.12.1.2	Magnitude < 0.1 dB	M	Yes [ ]
TC6	Signaling rate per lane	94.3.12.2	13.59375 GBd ± 100 ppm	M	Yes [ ]
TC7	Peak-to-peak differential output voltage	94.3.12.3	≤ 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC8	Peak-to-peak differential output voltage, transmitter disabled	94.3.12.3	≤ 30 mV	M	Yes [ ]
TC9	DC common-mode output voltage	94.3.12.3	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC10	AC common-mode output voltage	94.3.12.3	≤ 30 mV RMS regardless of transmit equalizer setting	M	Yes [ ]
TC11	EEE transmitter output level when disabled	94.3.12.3	< 35 mV peak-to-peak differential within 500 ns.	EEE:M	Yes [ ] N/A [ ]
TC12	EEE transmitter output level when enabled	94.3.12.3	90% of steady-state voltage by third alert frame marker and meet requirements of 94.3.12 with 1 us	EEE:M	Yes [ ] N/A [ ]
TC13	Transmitter output DC common-mode voltage when disabled	94.3.12.3	Within ±150 mV of value when transmitter is enabled.	M	Yes [ ]
TC14	Differential output return loss	94.3.12.4	Equation (94–5) with 100 Ω reference impedance	M	Yes [ ]
TC15	Common-mode output return loss	94.3.12.4	Equation (94–6) with 25 Ω reference impedance.	M	Yes [ ]
TC16	Transition times	94.3.12.5	≥ 18 ps when transmit equalization is disabled	M	Yes [ ]
TC17	Steady-state voltage, v_f	94.3.12.6.2	≥ 0.4 V and ≤ 0.6 V after the transmit equalizer coefficients have been set to the “preset” values	M	Yes [ ]
TC18	Linear fit pulse peak	94.3.12.6.2	> 0.85 × v_f after the transmit equalizer coefficients have been set to the “preset” values	M	Yes [ ]
TC19	Normalized linear fit error	94.3.12.6.3	≤ 0.025	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC20	Coefficient initialization	94.3.12.6.4	Satisfies the requirements of 94.3.12.6.4.	M	Yes [ ]
TC21	Normalized coefficient step size for “increment”	94.3.12.6.5	Between 0.0083 and 0.05	M	Yes [ ]
TC22	Normalized coefficient step size for “decrement”	94.3.12.6.5	Between –0.05 and –0.0083	M	Yes [ ]
TC23	Maximum post-cursor equalization ratio	94.3.12.6.6	≥ 4	M	Yes [ ]
TC24	Maximum pre-cursor equalization ratio	94.3.12.6.6	≥ 1.54	M	Yes [ ]
TC25	Transmitter far-end output noise, low-loss channel	94.3.12.7	< Equation (94–7)	M	Yes [ ]
TC26	Transmitter far-end output noise, high-loss channel	94.3.12.7	< Equation (94–8)	M	Yes [ ]
TC27	Clock random jitter RMS	94.3.12.8.1	≤ 0.005 UI RMS regardless of the transmit equalization setting	M	Yes [ ]
TC28	Clock deterministic jitter	94.3.12.8.1	≤ 0.05 UI regardless of the transmit equalization setting	M	Yes [ ]
TC29	Even-odd jitter	94.3.12.8.2	≤ 0.03 UI regardless of the transmit equalization setting	M	Yes [ ]
TC30	SNDR	94.3.12.9	≥ 19 dB	M	Yes [ ]

94.6.4.4 PMD receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture insertion loss	94.3.13.1	Meet requirements in 94.3.12.1.	M	Yes [ ]
RC2	Differential input return loss	94.3.13.2	Meets Equation (94–5) measured with a reference impedance of 100 Ω.	M	Yes [ ]
RC3	Differential to common-mode return loss	94.3.13.2	Meets Equation (94–15).	M	Yes [ ]
RC4	Interference tolerance	94.3.13.3	Satisfy requirements in Table 94–16	M	Yes [ ]
RC5	Jitter tolerance	94.3.13.4	Satisfy requirements in Table 94–17.	M	Yes []

94.6.4.5 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel operating margin (COM)	94.4.1	Greater than or equal to 3 dB	M	Yes [ ]
CC2	AC-coupling	94.4.4	Channel AC couples the transmitter to the receiver	M	Yes [ ]
CC3	AC-coupling 3 dB cut-off frequency	94.4.4	Less than 50 kHz	M	Yes [ ]

94.6.4.6 Environment specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	94.5.1	Complies with application section of IEC 60950-1	M	Yes [ ]
ES2	Electromagnetic interference	94.5.4	Complies with applicable local and national codes.	M	Yes [ ]

Annex 83A

(normative)

40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s Attachment Unit Interface (CAUI)

Insert the following after 83A.3.2:

83A.3.2a EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.3) then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI shutdown.

If the EEE capability includes XLAUI/CAUI shutdown (see 78.5.2) then when tx_mode is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the XLAUI/CAUI. When tx_mode is QUIET, the transmit direction XLAUI/CAUI transmitter is disabled as specified in 83A.3.3.1.1. Similarly when the received tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the XLAUI/CAUI. When the received tx_mode is QUIET, the receive direction XLAUI/CAUI transmitter is disabled as specified in 83A.3.3.1.1.

Insert the following at the end of 83A.3.3.1:

83A.3.3.1.1 Amplitude and swing

For EEE capability with XLAUI/CAUI shutdown, the XLAUI/CAUI transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_mode changing to QUIET in the relevant direction. Furthermore, the XLAUI/CAUI transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_mode ceasing to be QUIET in the relevant direction.

Insert the following after 83A.3.3.5 for the CAUI shutdown:

83A.3.3.6 Global transmit disable function

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction XLAUI/CAUI if PEASE is asserted and tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction XLAUI/CAUI if PIASE is asserted and the received tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction tx_mode changes to any state other than QUIET within a time and voltage level specified in 83A.3.3.1.1.

83A.3.4.7 Global energy detect function

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and XLAUI/CAUI shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the XLAUI/CAUI for the ingress direction SIGNAL_DETECT is set to FAIL following a tran-

sition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input detects an ALERT signal driven from the XLAUI/CAUI link partner. While rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is applied to the channel.

83A.7 Protocol implementation conformance statement (PICS) proforma for Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s Attachment Unit Interface (CAUI)[14]

Insert the following row at the end of the table in 83A.7.3:

83A.7.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Support for CAUI shutdown	83A.3.2a		O	Yes [ ] No [ ]

Insert the following rows at the end of the table in 83A.7.4:

83A.7.4 XLAUI/CAUI transmitter requirements

Item	Feature	Subclause	Value/Comment	Status	Support
TC11	Amplitude & swing for XLAUI/CAUI shutdown	83A.3.3.1.1		LPI:M	Yes [ ]
TC12	Transmit disable for XLAUI/CAUI shutdown	83A.3.3.6		LPI:M	Yes [ ]

Insert the following rows at the end of the table in 83A.7.5:

83A.7.5 XLAUI/CAUI receiver requirements

Item	Feature	Subclause	Value/Comment	Status	Support
RC8	Signal detect for XLAUI/CAUI shutdown	83A.3.4.7		LPI:M	Yes [ ]

[14]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

Annex 83C

(informative)

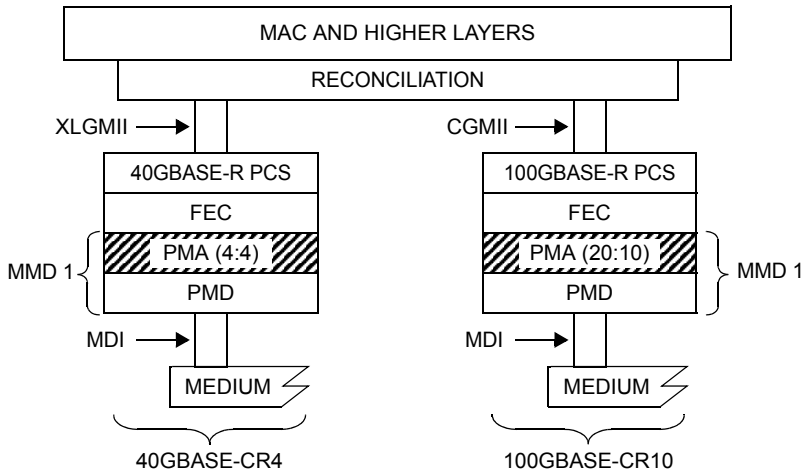
PMA sublayer partitioning examples

Change 83C.1 as follows:

83C.1 Partitioning examples with FEC

The example of BASE-R FEC (See Clause 74) implemented in a separate device from either the PCS or the PMD is illustrated in Figure 83–2.

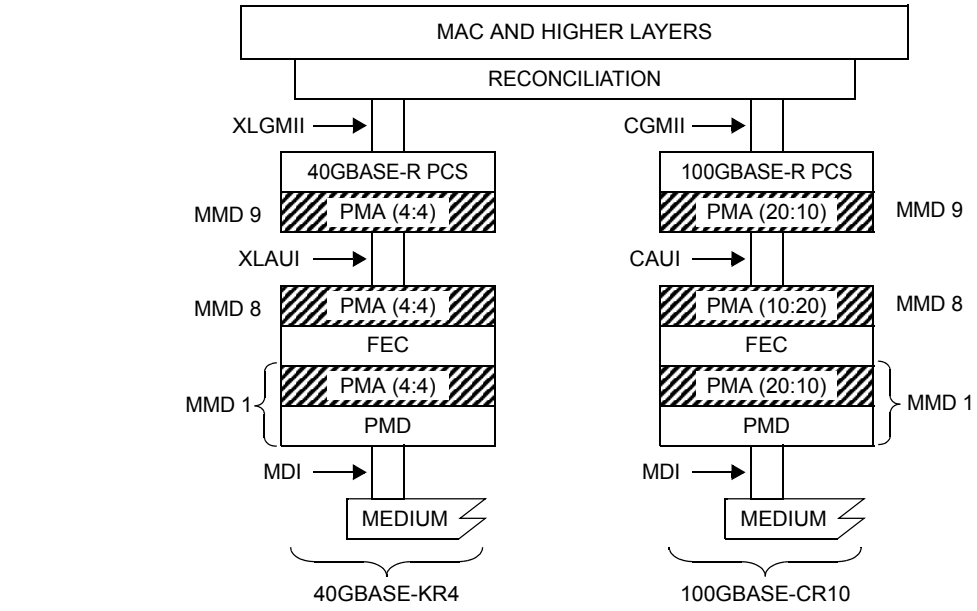
83C.1.1 FEC implemented with PCS



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–1—Example FEC implemented with PCS

83C.1.2 FEC implemented with PMD



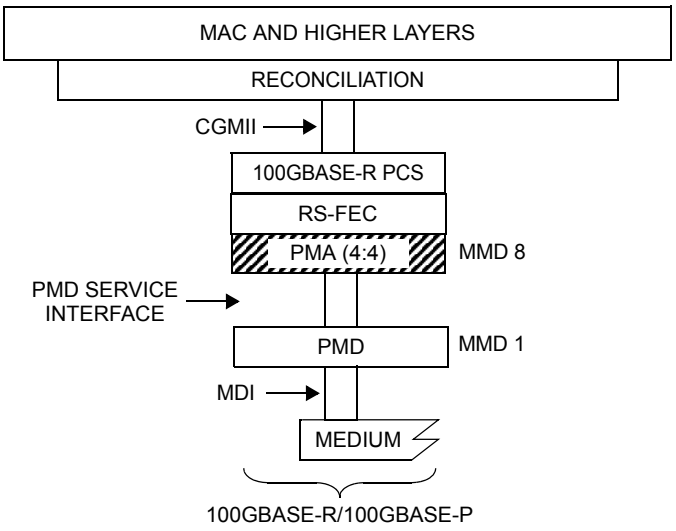
CAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–2—Example FEC implemented with PMD

Insert 83C.1a after 83C.1 as follows:

83C.1a Partitioning examples with RS-FEC

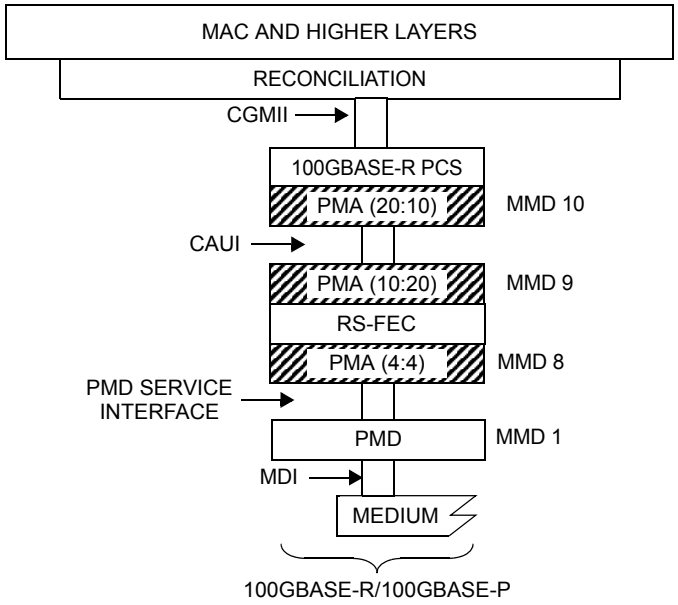
83C.1a.1 Single PMA sublayer with RS-FEC



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83C–2a—Example single PMA sublayer with RS-FEC

83C.1a.2 Single CAUI with RS-FEC



CAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83C–2b—Example single CAUI with RS-FEC

Annex 91A

(informative)

RS-FEC codeword examples

This annex provides example RS-FEC codewords produced by the 64B/66B to 256B/257B transcoding and Reed-Solomon encoding defined in Clause 91. This annex presents data in a tabular form. The contents of the tables are transmitted from left to right within each row starting from the top row and ending at the bottom row. The tables contain both binary and hexadecimal representations of the data. For the hexadecimal representation, the most significant bit of each hex symbol is transmitted first.

91A.1 Input to the 64B/66B to 256B/257B transcoder

Table 91A–1 contains a sequence of 80 66-bit blocks corresponding to the PCS transmission of Idle control characters. The initial value of the scrambler was set to bits 6 to 63 of the first 64-bit payload in the first row of Table 74A–2. Bit 6 is assigned to S57 and bit 63 is assigned to S0 (see 49.2.6).

Table 91A–1—64B/66B to 256B/257B transcoder input

Sync <0:1>	64-bit payload, hex <2:65>	Sync <0:1>	64-bit payload, hex <2:65>	Sync <0:1>	64-bit payload, hex <2:65>	Sync <0:1>	64-bit payload, hex <2:65>
10	ad5a3bf86d9acf5c	10	de55cb85df0f7ca0	10	e6ccff8e8212b1c6	10	d63bc6c309000638
10	70e3b0ce30e0497d	10	dc8df31ec3ab4491	10	66fb9139c81cd37b	10	b57477d4f05e3602
10	8cfd495012947a31	10	e7777cf0c6d06280	10	44529cf4b4900528	10	85ce1d27750ad61b
10	456d5c71743f5c69	10	c1bf62e5dc5464b5	10	dc6011be7ea1ed54	10	1cf92c450042a75f
10	cc4b940eaf3140db	10	77bb612a7abf401f	10	c22d341e90545d98	10	ce6daf1f248bbd6d
10	dd22d0b3f9551ed6	10	574686c3f9e93898	10	2e52628f4a1282ce	10	f20c86d71944aab1
10	55133c9333808a2c	10	1aa825d8b817db4d	10	637959989f3021eb	10	976806641b26aae9
10	6a37d4531b7ed5f2	10	53c3e96d3b12fb46	10	528c7eb8481bc969	10	ab8f9980d5a54559
10	9a4d2abfda65cc33	10	94fe646efe5af02d	10	9a65ae5fcd88c03a	10	5ef08673168def9b
10	220c871a953fffc6	10	ce0bb95ac263e6c1	10	4f6a917d1a676571	10	5890918c7b687d75
10	44d2b3e43096f836	10	84cdd4fc48b79608	10	b3e4503e3c824a8c	10	fd6d0b1a39687929
10	1730167c08302a69	10	4c15ff56de92b1ad	10	d0c2f0d4ff0dee95	10	e1422ee2e8b92125
10	ed5acaf86592fcee	10	de799be0b903c880	10	2714ffbf40bc09f6	10	c3be97c3c285009f
10	1020faf19f606631	10	93007cabbb3f8c9d	10	ef6955f7f43df5d0	10	4dbd0616afe60e1f
10	3a1e49b7c7f7bb5d	10	901d828746ceec61	10	71ed3c097158c224	10	11adb3d81e13d263
10	a350d1a343b2394b	10	eab30ca27b5b34e3	10	90359ef711ed53d9	10	9b446763c8627ea8
10	6e891c0f4842b823	10	c4d786a25727a7fc	10	094fe7da31fb60cd	10	9f9a004de5e70767
10	054bdd77b7cb4e7b	10	c598cb710558af67	10	fc386d1f99d3a925	10	4928e0b43e781893
10	5a44dd3eb8b2ad6c	10	94462af4f583d770	10	8061ba9381f51f55	10	476d4eded7c90fcc
10	1efc25aa6a7e0b4c	10	93dd968c06a56809	10	9768e9d1ba74d3b6	10	014e9dc9f13670bb

91A.2 Output of the RS(528,514) encoder

Table 91A–2 contains a RS(528,514) codeword. Each row of Table 91A–1 is a set of 4 66-bit blocks that is converted to one 257-bit block using the procedure defined in 91.5.2.5. The resulting set of 20 257-bit blocks constitute the message portion of the codeword. The parity is computed using the encoder defined in 91.5.2.7 and is appended to the message to complete the codeword.

Table 91A–2—RS(528,514) codeword

Header <0:4>	Payload, hex <5:64>	Payload, hex <65:128>	Payload, hex <129:192>	Payload, hex <193:256>
00101	a5a3bf86d9acf5c	de55cb85df0f7ca0	e6ccff8e8212b1c6	d63bc6c309000638
11110	7e3b0ce30e0497d	dc8df31ec3ab4491	66fb9139c81cd37b	b57477d4f05e3602
01111	8fd495012947a31	e7777cf0c6d06280	44529cf4b4900528	85ce1d27750ad61b
00110	46d5c71743f5c69	c1bf62e5dc5464b5	dc6011be7ea1ed54	1cf92c450042a75f
00100	c4b940eaf3140db	77bb612a7abf401f	c22d341e90545d98	ce6daf1f248bbd6d
10010	d22d0b3f9551ed6	574686c3f9e93898	2e52628f4a1282ce	f20c86d71944aab1
10001	5133c9333808a2c	1aa825d8b817db4d	637959989f3021eb	976806641b26aae9
00011	637d4531b7ed5f2	53c3e96d3b12fb46	528c7eb8481bc969	ab8f9980d5a54559
10100	94d2abfda65cc33	94fe646efe5af02d	9a65ae5fcd88c03a	5ef08673168def9b
00000	20c871a953fffc6	ce0bb95ac263e6c1	4f6a917d1a676571	5890918c7b687d75
01101	4d2b3e43096f836	84cdd4fc48b79608	b3e4503e3c824a8c	fd6d0b1a39687929
10011	130167c08302a69	4c15ff56de92b1ad	d0c2f0d4ff0dee95	e1422ee2e8b92125
00101	e5acaf86592fcee	de799be0b903c880	2714ffbf40bc09f6	c3be97c3c285009f
10010	120faf19f606631	93007cabbb3f8c9d	ef6955f7f43df5d0	4dbd0616afe60e1f
10001	31e49b7c7f7bb5d	901d828746ceec61	71ed3c097158c224	11adb3d81e13d263
00101	a50d1a343b2394b	eab30ca27b5b34e3	90359ef711ed53d9	9b446763c8627ea8
01000	6891c0f4842b823	c4d786a25727a7fc	094fe7da31fb60cd	9f9a004de5e70767
00100	04bdd77b7cb4e7b	c598cb710558af67	fc386d1f99d3a925	4928e0b43e781893
10100	544dd3eb8b2ad6c	94462af4f583d770	8061ba9381f51f55	476d4eded7c90fcc
11111	1fc25aa6a7e0b4c	93dd968c06a56809	9768e9d1ba74d3b6	014e9dc9f13670bb
Parity, hex <0:63>	**Parity, hex <64:127>**	**Parity, hex <128:139>**		
ed0e78f1734bc808	a38c0c417bd68f36	825		

91A.3 Output of the RS(544,514) encoder

Table 91A–3 contains a RS(544,514) codeword. Each row of Table 91A–1 is a set of 4 66-bit blocks that is converted to one 257-bit block using the procedure defined in 91.5.2.5. The resulting set of 20 257-bit blocks constitute the message portion of the codeword. The parity is computed using the encoder defined in 91.5.2.7 and is appended to the message to complete the codeword.

Table 91A–3—RS(544,514) codeword

Header <0:4>	Payload, hex <5:64>	Payload, hex <65:128>	Payload, hex <129:192>	Payload, hex <193:256>
00101	a5a3bf86d9acf5c	de55cb85df0f7ca0	e6ccff8e8212b1c6	d63bc6c309000638
11110	7e3b0ce30e0497d	dc8df31ec3ab4491	66fb9139c81cd37b	b57477d4f05e3602
01111	8fd495012947a31	e7777cf0c6d06280	44529cf4b4900528	85ce1d27750ad61b
00110	46d5c71743f5c69	c1bf62e5dc5464b5	dc6011be7ea1ed54	1cf92c450042a75f
00100	c4b940eaf3140db	77bb612a7abf401f	c22d341e90545d98	ce6daf1f248bbd6d
10010	d22d0b3f9551ed6	574686c3f9e93898	2e52628f4a1282ce	f20c86d71944aab1
10001	5133c9333808a2c	1aa825d8b817db4d	637959989f3021eb	976806641b26aae9
00011	637d4531b7ed5f2	53c3e96d3b12fb46	528c7eb8481bc969	ab8f9980d5a54559
10100	94d2abfda65cc33	94fe646efe5af02d	9a65ae5fcd88c03a	5ef08673168def9b
00000	20c871a953fffc6	ce0bb95ac263e6c1	4f6a917d1a676571	5890918c7b687d75
01101	4d2b3e43096f836	84cdd4fc48b79608	b3e4503e3c824a8c	fd6d0b1a39687929
10011	130167c08302a69	4c15ff56de92b1ad	d0c2f0d4ff0dee95	e1422ee2e8b92125
00101	e5acaf86592fcee	de799be0b903c880	2714ffbf40bc09f6	c3be97c3c285009f
10010	120faf19f606631	93007cabbb3f8c9d	ef6955f7f43df5d0	4dbd0616afe60e1f
10001	31e49b7c7f7bb5d	901d828746ceec61	71ed3c097158c224	11adb3d81e13d263
00101	a50d1a343b2394b	eab30ca27b5b34e3	90359ef711ed53d9	9b446763c8627ea8
01000	6891c0f4842b823	c4d786a25727a7fc	094fe7da31fb60cd	9f9a004de5e70767
00100	04bdd77b7cb4e7b	c598cb710558af67	fc386d1f99d3a925	4928e0b43e781893
10100	544dd3eb8b2ad6c	94462af4f583d770	8061ba9381f51f55	476d4eded7c90fcc
11111	1fc25aa6a7e0b4c	93dd968c06a56809	9768e9d1ba74d3b6	014e9dc9f13670bb
Parity, hex <0:63>	**Parity, hex <64:127>**	**Parity, hex <128:191>**	**Parity, hex <192:255>**	**Parity, hex <256:299>**
d6983839edc3e5ac	c3cb45691ddba6cb	c26d756ea6f5b73d	249e30f415aa60b1	5743dc81c21

91A.4 Reed-Solomon encoder model

This annex also includes a model of the Reed-Solomon encoder defined in 91.5.2.7 written in the C programming language. To emulate the RS(528,514) encoder, declare global variables per 91A.4.1. To emulate the RS(544,514) encoder, declare global variables per 91A.4.2. The generic components of the model are defined in 91A.4.3 to 91A.4.6.

91A.4.1 Global variable declarations for RS(528,514)

These global variables define the codeword size (in symbols) and generator polynomial coefficients (see Table 91–1) for the RS(528,514) code. Elements of GF(2^{10}) are presented as decimal values.

```
long n_symbols = 528;
unsigned long generator_polynomial[1024] =
   {904,6,701,32,656,925,900,614,391,592,265,945,290,432};
```

91A.4.2 Global variable declarations for RS(544,514)

These global variables define the codeword size and generator polynomial coefficients for the RS(544,514) code.

```
long n_symbols = 544;
unsigned long generator_polynomial[1024] =
   {575,552,187,230,552,1,108,565,282,249,593,132,94,720,495,385,942,503,883,36
   1,788,610,193,392,127,185,158,128,834,523};
```

91A.4.3 Other global variable declarations

The following global variables are declared for both RS(528,514) and RS(544,514). The field polynomial is assigned its decimal representation (1033 corresponds to $x^{10}+x^3+1$).

```
long polynomial = 1033;
long k_symbols = 514;
long check_symbols;
unsigned long codeword[1024];
```

91A.4.4 GF(2^{10}) multiplier function

This function implements multiplication over GF(2^{10}) using the expansion and reduction algorithm.

```
unsigned long multiply(long aa, long bb)
{
   unsigned long expand = 0;
   long k;

   for (k = 0; k < 10; k++)
   {
      if (bb & (1 << k))
         expand = expand ^ (aa << k);
   }

   for (k = 0; k < 9; k++)
   {
      if ((expand >> (18-k)) & 1)
         expand = expand ^ (polynomial << (8-k));
   }

   return expand;
}
```

91A.4.5 Reed-Solomon encoder function

This function implements the Reed-Solomon encoder. It uses the multiply() function.

```
void encode()
{
   long k, j;
   unsigned long multiplier;
   unsigned long generator_vector[1024];
   unsigned long encoder_divide[1024];

   for (k = 0; k < check_symbols; k++)
      encoder_divide[k] = 0;

   for (k = 0; k < k_symbols; k++)
   {
      multiplier = codeword[k] ^ encoder_divide[0];

      for (j = 0; j < check_symbols; j++)
         generator_vector[j] = multiply(multiplier, generator_polynomial[j]);

      for (j = 0; j < check_symbols-1; j++)
         encoder_divide[j] = generator_vector[j] ^ encoder_divide[j+1];

      encoder_divide[check_symbols-1] = generator_vector[check_symbols-1];

      for (j = 0; j < check_symbols; j++)
         codeword[j+k_symbols] = encoder_divide[j];
   }
}
```

91A.4.6 Main function

This sample main function defines a hypothetical message consisting of a countdown from 1023 to 510 (514 Reed-Solomon symbols). It then computes the parity and produces a codeword using the encode() function. The resulting codeword is printed to the console.

```
void main()
{
   long k;
   check_symbols = n_symbols-k_symbols;

   //*** Generate simple message symbols ***
   for (k = 0; k < k_symbols; k++)
      codeword[k] = 1023-k;

   encode();

   for (k = 0; k < n_symbols; k++)
      printf("%ld ", codeword[k]);
}
```

Annex 92A

(informative)

100GBASE-CR4 TP0 and TP5 test point parameters and channel characteristics

92A.1 Overview

Annex 92A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 100GBASE-CR4 link block diagram of Figure 92–2. It also provides information on channel characteristics.

92A.2 Transmitter characteristics at TP0

The transmitter characteristics at TP0 are constrained at TP0a by 93.8.1.

92A.3 Receiver characteristics at TP5

The receiver characteristics at TP5 are constrained at TP5a by 93.8.2.

92A.4 Transmitter and receiver differential printed circuit board trace loss

The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is determined using Equation (92A–1) and illustrated in Figure 92A–1. Note that the recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 6.81 dB at 12.9806 GHz. The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is consistent with the insertion loss TP0 to TP2 or TP3 to TP5 given in 92.8.3.8 and an assumed mated connector loss of 1.69 dB.

$$IL_{\mathrm{PCB}}(f) \le IL_{\mathrm{PCBmax}}(f) = 0.5(0.0694 + 0.4248\sqrt{f} + 0.9322f) \text{ (dB)} \quad (92A–1)$$

for 0.01 GHz $\le f \le$ 19 GHz.

where

f	is the frequency in GHz
$IL_{\mathrm{PCB}}(f)$	is the insertion loss for the transmitter and receiver PCB
$IL_{\mathrm{PCBmax}}(f)$	is the recommended maximum insertion loss for the transmitter and receiver PCB

The minimum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the minimum value of the sum of the insertion losses from TP0 to MDI receptacle or TP5 to MDI receptacle) are determined using Equation (92A–2) and illustrated in Figure 92A–1.

$$IL_{PCB}(f) \geq IL_{PCBmin}(f) = 0.086(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)} \qquad (92A–2)$$

for 0.01 GHz ≤ f ≤ 19 GHz.

where

f is the frequency in GHz
$IL_{PCB}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmin}(f)$ is the minimum insertion loss for the transmitter and receiver PCB

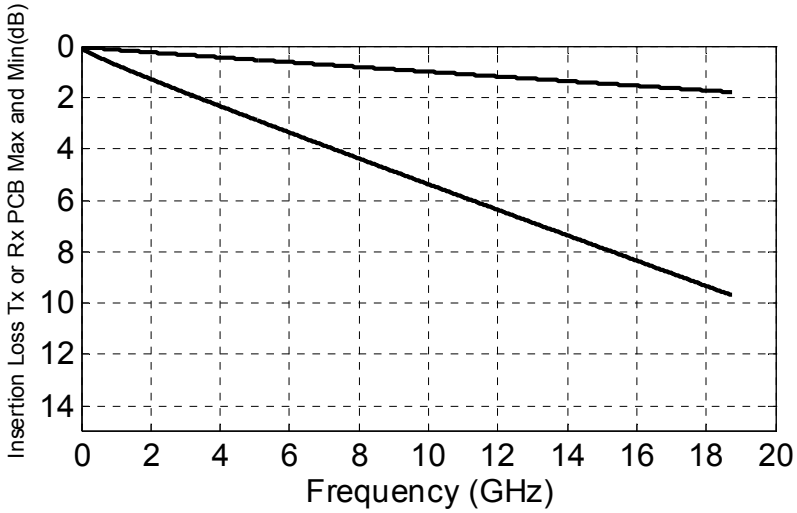


Figure 92A–1—Insertion Loss Tx or Rx PCB Max and Min

92A.5 Channel insertion loss

This subclause provides information on channel insertion losses for intended topologies ranging from 0.5 m to 5 m in length. The maximum channel insertion loss associated with the 5 m topology is determined using Equation (92A–3). The channel insertion loss associated with the 0.5 m topology and a maximum host channel is determined by Equation (92A–5). The channel insertion loss budget at 12.8906 GHz for the 5 m topology is illustrated in Figure 92A–2.

The maximum channel insertion loss for the 5 m topology is determined using Equation (92A–3). The maximum channel insertion loss is 35 dB at 12.8906 GHz.

$$IL_{Chmax35dB}(f) = IL_{Camax5m}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \text{ (dB)} \qquad (92A–3)$$

for 0.05 GHz ≤ f ≤ 19 GHz.

where

f is the frequency in GHz

$IL_{Chmax35dB}(f)$ is the maximum channel insertion loss between TP0 and TP5 representative of a 5 m cable assembly and a maximum host channel

$IL_{Camax5m}(f)$ is the maximum 5 m cable assembly insertion loss.

$IL_{Host}(f)$ is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–6)

$IL_{MatedTF}(f)$ is the nominal insertion loss of the mated test fixture using Equation (92A–4)

The nominal insertion loss of the mated test fixture is determined using Equation (92A–4).

$$IL_{MatedTF}(f) = 0.1148\sqrt{f} + 0.287f \text{ (dB)} \quad \text{(92A–4)}$$

for 0.01 GHz ≤ f ≤ 25 GHz.

where

f is the frequency in GHz

$IL_{MatedTF}(f)$ is the nominal insertion loss of the mated test fixture.

The channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel is determined using Equation (92A–5).

$$IL_{Ch0.5m}(f) = IL_{Camin0.5m}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \text{ (dB)} \quad \text{(92A–5)}$$

for 0.05 GHz ≤ f ≤ 19 GHz.

where

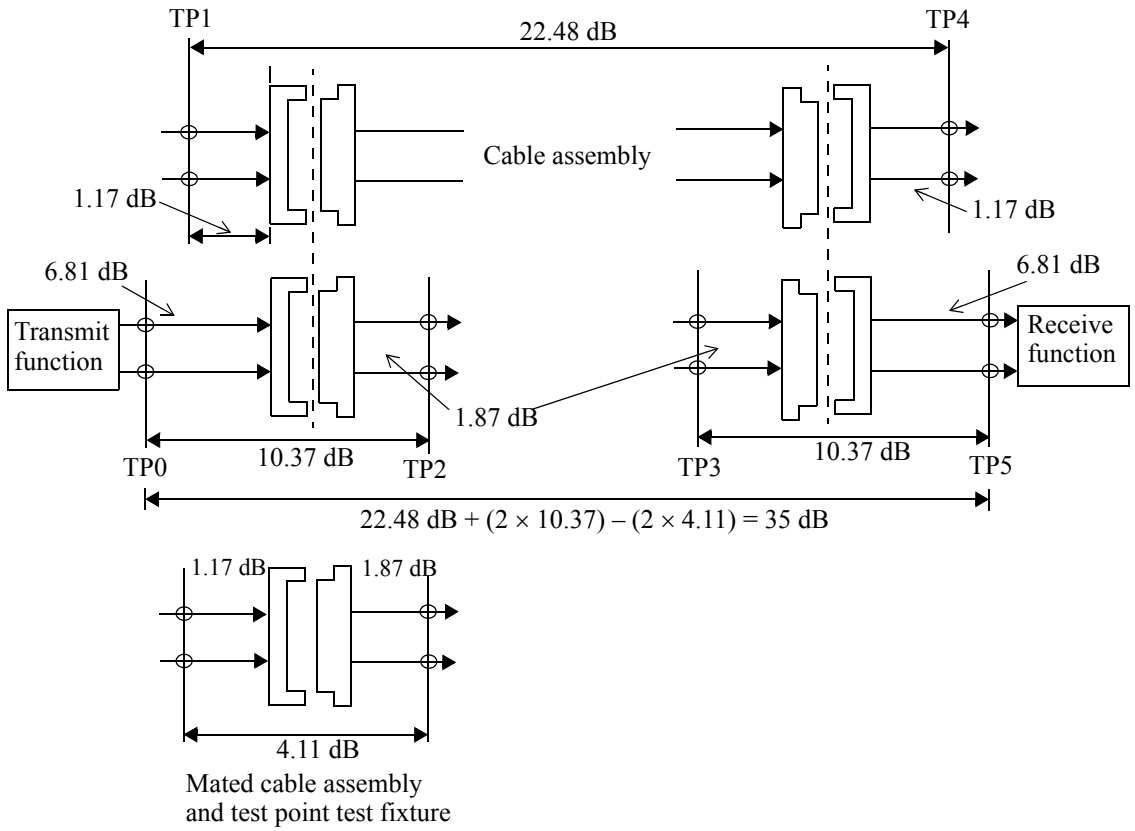
f is the frequency in GHz

$IL_{Ch0.5m}(f)$ is the channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel

$IL_{Camin0.5m}(f)$ is the minimum 0.5 m cable assembly insertion loss given in Equation (92–13) and illustrated in Figure 92–11.

$IL_{Host}(f)$ is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–6)

$IL_{MatedTF}(f)$ is the nominal insertion loss of the mated test fixture using Equation (92A–4)



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 92A–2—35 dB channel insertion loss budget at 12.8906 GHz

92A.6 Channel return loss

The return loss of each lane of the 100GBASE-CR4 channel is recommended to meet the values determined using Equation (92–15).

92A.7 Channel operating margin (COM)

The channel operating margin (COM) for the channel between TP0 and TP5, computed using the procedure in 93A.1 and the parameters in Table 93–9, is recommended to be greater than or equal to 3 dB.

Annex 93A

(normative)

Specification methods for electrical channels

93A.1 Channel operating margin

Editor's note (to be removed prior to final publication):

This annex contains a mathematical description of the channel operating margin computation. A sample implementation of this calculation, in the MATLAB(R) computational language, may be found at the following URL (http://www.ieee802.org/3/bj/public/tools.html).

The channel operating margin (COM) is a figure of merit for a channel derived from a measurement of its scattering parameters. COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude as defined by Equation (93A–1).

$$COM = 20\log_{10}(A_s/A_n) \quad \text{(93A–1)}$$

COM shall be calculated using the method described in this annex. The signal amplitude A_s is defined in 93A.1.6 and the noise amplitude A_n is defined in 93A.1.7.

Figure 93A–1 illustrates the reference model that is the basis for the calculation for COM. The parameters used to calculate COM are summarized in Table 93A–1. The values assigned to these parameters are defined by the Physical Layer specification that invokes the method.

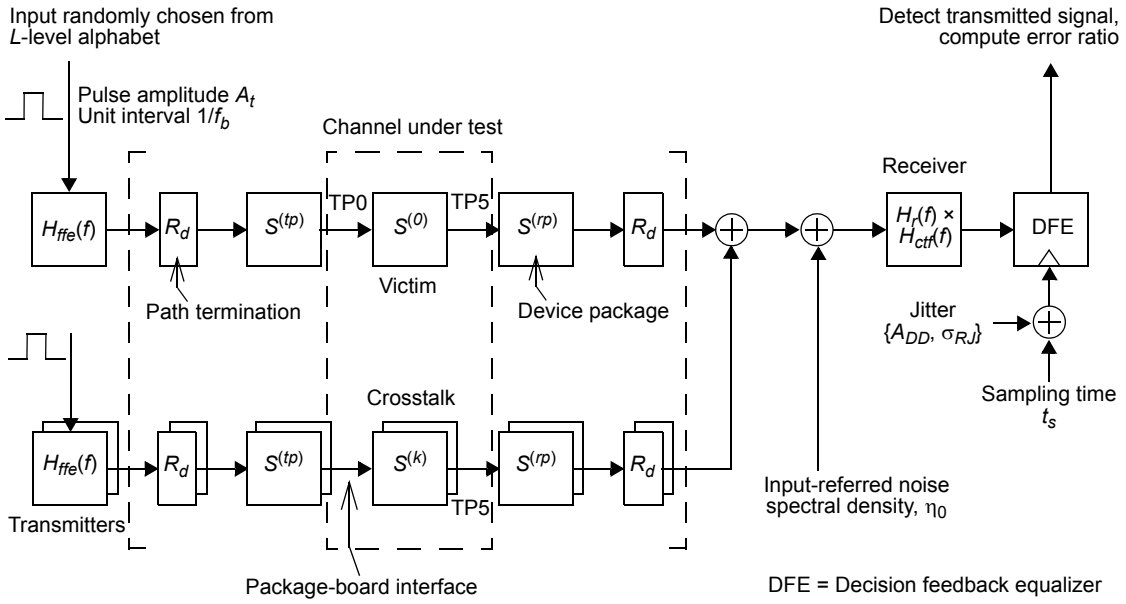


Figure 93A–1—Channel operating margin reference model

Table 93A–1—Summary of parameters

Parameter	Reference	Symbol	Units
Signaling rate	93A.1.1	f_b	GBd
Maximum start frequency	93A.1.1	$f_{\min}$	GHz
Maximum frequency step	93A.1.1	Δf	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended board capacitance	93A.1.2	 C_d z_p C_b	 nF mm nF
Single-ended reference resistance	93A.1.2	R_0	Ω
Single-ended termination resistance	93A.1.3	R_d	Ω
Receiver 3 dB bandwidth	93A.1.4.1	f_r	GHz
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	93A.1.4.2	$c(-1)$	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	93A.1.4.2	$c(1)$	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	93A.1.4.3	g_{DC}	 dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	93A.1.5	 A_v A_f A_n	 V V V
Number of signal levels	93A.1.6	L	—
Number of samples per unit interval	93A.1.6	M	—
Decision feedback equalizer (DFE) length	93A.1.6	N_b	UI
Normalized DFE coefficient magnitude limit	93A.1.6	$b_{\max}(n)$	—
Random jitter, RMS	93A.1.6	σ_{RJ}	UI
Dual-Dirac jitter, peak	93A.1.6	A_{DD}	UI
One-sided noise spectral density	93A.1.6	η_0	V^2/GHz
Target detector error ratio	93A.1.7	DER_0	—

93A.1.1 Measurement of the channel

The channel consists of a victim signal path plus some number of far-end and near-end crosstalk paths. The total number of paths for a given channel is denoted as K and, by convention, the path index k=0 corresponds to the victim path. The number of crosstalk paths is a function of the structure of the system. All significant contributors to the channel crosstalk should be included in the calculation of COM.

Each signal path is represented by a set of frequency-dependent scattering parameters. For the purpose of the calculation of COM, references to scattering parameters correspond to the differential-mode scattering parameters. The scattering parameters measured at frequency f are presented as the 2 x 2 matrix $S(f)$ as defined by Equation (93A–2).

$$S(f) = \begin{bmatrix} s_{11}(f) & s_{12}(f) \\ s_{21}(f) & s_{22}(f) \end{bmatrix} \quad \text{(93A–2)}$$

The relationship between $S(f)$ and other commonly cited characteristics is as follows. The insertion loss is the magnitude in dB of either $1/s_{12}(f)$ or $1/s_{21}(f)$. The input and output return loss are the magnitude in dB of $1/s_{11}(f)$ and $1/s_{22}(f)$ respectively.

The scattering parameters for the victim signal path are measured from TP0 to TP5. The scattering parameters for each crosstalk path are measured from the package-to-board interface of the aggressor transmitter to TP5. The frequency-dependent scattering matrix for signal path k is denoted as $S^{(k)}(f)$. The reference impedance for scattering parameter measurements is 100 Ω.

It is recommended that the scattering parameters be measured with uniform frequency step no larger than Δf from a start frequency no larger than $f_{\min}$ to a stop frequency of at least the signaling rate f_b.

93A.1.2 Transmitter and receiver device package models

Each signal path in the channel is augmented to reflect the likely influence of transmitter and receiver device packages. The device package models are two-port networks defined by their scattering parameters. The scattering parameters are calculated using the method defined in 93A.1.2.1 through 93A.1.2.4.

Each signal path in the channel is represented by the scattering matrix $S^{(k)}$. The augmented signal path is denoted as $S_p^{(k)}$ and is defined by Equation (93A–3).

$$S_p^{(k)} = \text{cascade}(\text{cascade}(S^{(tp)}, S^{(k)}), S^{(rp)}) \quad \text{(93A–3)}$$

The function cascade() is defined in 93A.1.2.1. $S^{(tp)}$ and $S^{(rp)}$ are defined in 93A.1.2.4. If k corresponds to a near-end crosstalk path, $S^{(tp)}$ is calculated with C_d and C_b values that are half of the values specified by the clause that invokes this method.

93A.1.2.1 Cascade connection of two-port networks

The connection of a pair of two-port networks x and y such that port 2 of network x is connected to port 1 of network y may be represented by an equivalent two-port network z. Port 1 of network z corresponds to port 1 of network x and port 2 network z corresponds to port 2 of network y. The scattering parameters of network z are given in terms of the scattering parameters of networks x and y by Equation (93A–4) through Equation (93A–7).

$$s_{11}^{(z)} = s_{11}^{(x)} + \frac{s_{21}^{(x)} s_{11}^{(y)} s_{12}^{(x)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \quad \text{(93A–4)}$$

$$s_{12}^{(z)} = \frac{s_{12}^{(x)} s_{12}^{(y)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \quad \text{(93A–5)}$$

$$s_{21}^{(z)} = \frac{s_{21}^{(x)} s_{21}^{(y)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \quad (93A–6)$$

$$s_{22}^{(z)} = s_{22}^{(y)} + \frac{s_{12}^{(y)} s_{22}^{(x)} s_{21}^{(y)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \quad (93A–7)$$

For the purpose of this annex, this set of operations will be referred to using the shorthand notation $S^{(z)} = \text{cascade}(S^{(x)}, S^{(y)})$.

93A.1.2.2 Two-port network for a shunt capacitance

The scattering parameters for a shunt capacitance with value C are defined by Equation (93A–8) where $j = \sqrt{-1}$ and $\omega = 2\pi f$.

$$S(C) = \frac{1}{2 + j\omega CR_0} \begin{bmatrix} -j\omega CR_0 & 2 \\ 2 & -j\omega CR_0 \end{bmatrix} \quad (93A–8)$$

The scattering parameters for the device capacitance C_d are denoted as $S^{(d)} = S(C_d)$ and the scattering parameters for the board capacitance C_b are denoted as $S^{(b)} = S(C_b)$.

93A.1.2.3 Two-port network for the package transmission line

The scattering parameters for a 1 mm section of the package transmission line model are defined by Equation (93A–9), Equation (93A–10), and the parameters values in Table 93A–2.

$$s_{11} = s_{22} = \rho_0 + \rho_1 f + \rho_2 f^2 + \rho_3 f^3 + \rho_4 f^4 \quad (93A–9)$$

$$s_{12} = s_{21} = \exp(\gamma_0 + \gamma_1 \sqrt{f} + \gamma_2 f + \gamma_4 f^2) \quad (93A–10)$$

The scattering parameters for a package transmission line whose length z_p is an integer multiple of 1 mm are derived from the scattering parameters of the 1 mm section using Equation (93A–11) and Equation (93A–12).

$$s_{11}^{(l)} = s_{22}^{(l)} = s_{11} \sum_{i=1}^{z_p} s_{21}^{2i-2} \quad (93A–11)$$

$$s_{12}^{(l)} = s_{21}^{(l)} = s_{21}^{z_p} \quad (93A–12)$$

The transmission line scattering parameter matrix is then denoted as $S^{(l)}$.

93A.1.2.4 Assembly of transmitter and receiver device package models

The scattering parameters for the transmitter device package model $S^{(tp)}$ are the result of the cascade connection of the device capacitance, package transmission line, and board capacitance as defined by Equation (93A–13).

$$S^{(tp)} = \text{cascade}(\text{cascade}(S^{(d)}, S^{(l)}), S^{(b)}) \quad (93A–13)$$

Table 93A–2—Transmission line model parameters

Parameter	Real	Imaginary	Units
ρ_0	11.007×10^{-4}	0	—
ρ_1	3.679×10^{-18}	-8.124×10^{-3}	1/GHz
ρ_2	-3.235×10^{-4}	-3.544×10^{-20}	$1/GHz^2$
ρ_3	-1.021×10^{-20}	7.434×10^{-6}	$1/GHz^3$
ρ_4	1.722×10^{-7}	-1.78×10^{-21}	$1/GHz^4$
γ_0	-10.037×10^{-4}	0	—
γ_1	-3.538×10^{-4}	-3.355×10^{-3}	$1/GHz^{1/2}$
γ_2	-1.027×10^{-3}	-3.818×10^{-2}	1/GHz
γ_4	-1.178×10^{-5}	3.363×10^{-5}	$1/GHz^2$

Similarly, the scattering parameters for the receiver device package model $S^{(rp)}$ are the result of the cascade connection of the board capacitance, package transmission line, and device capacitance as defined by Equation (93A–14).

$$S^{(rp)} = \text{cascade}(\text{cascade}(S^{(b)}, S^{(l)}), S^{(d)}) \quad (93A–14)$$

93A.1.3 Path terminations

The input to each signal path is terminated by an impedance defined by the reflection coefficient Γ_1. The output of each signal path is terminated by an impedance defined by the reflection coefficient Γ_2.

The reflection coefficients Γ_1 and Γ_2 are defined by Equation (93A–15).

$$\Gamma_1(f) = \Gamma_2(f) = \frac{R_d - R_0}{R_d + R_0} \quad (93A–15)$$

The voltage transfer function of the terminated signal path is defined by Equation (93A–16) where $\Delta S(f) = s_{11}(f)s_{22}(f) - s_{12}(f)s_{21}(f)$.

$$H_{21}(f) = \frac{s_{21}(f)(1-\Gamma_1)(1+\Gamma_2)}{1 - s_{11}(f)\Gamma_1(f) - s_{22}(f)\Gamma_2(f) + \Gamma_1(f)\Gamma_2(f)\Delta S(f)} \quad (93A–16)$$

The voltage transfer function for the signal path represented by $S_p^{(k)}(f)$ is denoted $H_{21}^{(k)}(f)$.

93A.1.4 Filters

The voltage transfer function for each signal path $H_{21}^{(k)}(f)$ (see 93A.1.3) is multiplied by a set of filter transfer functions to yield $H^{(k)}(f)$ as shown in Equation (93A–17).

$$H^{(k)}(f) = H_{ffe}(f)H_{21}^{(k)}(f)H_r(f)H_{ctf}(f) \quad (93A–17)$$

The receiver noise filter $H_r(f)$ is defined in 93A.1.4.1, the transmitter equalizer $H_{ffe}(f)$ is defined in 93A.1.4.2, and the receiver equalizer $H_{ctf}(f)$ is defined in 93A.1.4.3.

The filtered voltage transfer function $H^{(k)}(f)$ is used to compute the pulse response (see 93A.1.5).

93A.1.4.1 Receiver noise filter

$H_r(f)$ is a noise filter defined by Equation (93A–18).

$$H_r(f) = \frac{1}{1 - 3.414214(f/f_r)^2 + (f/f_r)^4 + j2.613126(f/f_r - (f/f_r)^3)} \quad (93A–18)$$

93A.1.4.2 Transmitter equalizer

$H_{ffe}(f)$ is defined by Equation (93A–19) and is intended to represent the transmitter equalizer. If k corresponds to a near-end crosstalk path, then $c(-1)$ and $c(1)$ are zero regardless of the values used for the other paths. The value of the "cursor" coefficient $c(0)$ is set to $1 - |c(-1)| - |c(1)|$ for any value of $c(-1)$ and $c(1)$.

$$H_{ffe}(f) = \sum_{i=-1}^{1} c(i)\exp(-j2\pi(i+1)(f/f_b)) \quad (93A–19)$$

93A.1.4.3 Receiver equalizer

$H_{ctf}(f)$ is defined by Equation (93A–20).

$$H_{ctf}(f) = \frac{10^{g_{DC}/20} + j(4f/f_b)}{(1 + j(f/f_b))(1 + j(4f/f_b))} \quad (93A–20)$$

93A.1.5 Pulse response

The pulse response of a signal path is defined to be the output of the path following the application of rectangular pulse one unit interval in duration at its input. First define the function $X(f)$ per Equation (93A–21) where $\mathrm{sinc}(x) = \sin(\pi x)/(\pi x)$ and $T_b = 1/f_b$ is the unit interval.

$$X(f) = A_t T_b \mathrm{sinc}(fT_b) \quad (93A–21)$$

$X(f)$ is a function of A_t which in turn is based on the path index k. If k=0, i.e. the victim path, then $A_t = A_v$. If k corresponds to a far-end crosstalk path then $A_t = A_f$. If k corresponds to a near-end crosstalk path then $A_t = A_n$.

The pulse response $h^{(k)}(t)$ is derived from the voltage transfer function $H^{(k)}(f)$ (see 93A.1.4) using Equation (93A–22).

$$h^{(k)}(t) = \int_{-\infty}^{\infty} X(f)H^{(k)}(f)\exp(j2\pi ft)dt \quad (93A–22)$$

NOTE 1—It is expected that COM will be computed from measurements at discrete frequencies that cover a limited span (see 93A.1.1). The inverse Fourier transform depicted in Equation (93A–22) will likely be implemented as a discrete Fourier transform and the filtered voltage transfer function may need to be extrapolated (both to DC and to one half

of the sampling frequency) for this computation. The extrapolation method and sampling frequency must be chosen carefully to limit the error in the COM computation.

NOTE 2—The time span of the pulse response in unit intervals, N, is limited in practice by frequency step Δf ($N = f_b/\Delta f$) but in general should be set to include all significant components of the pulse response.

93A.1.6 Signal amplitude

COM is a function of the variables $c(-1)$, $c(1)$, and g_{DC}. The following procedure is used to determine the values of these variables that will be used to calculate COM.

a) Compute the pulse response $h^{(k)}(t)$ of each signal path k for a given $c(-1)$, $c(1)$, and g_{DC} using the procedure defined in 93A.1.5.
b) Define t_s to be the time that satisfies Equation (93A–23). If there are multiple values of t_s that satisfy the equation, then the first value prior to the peak of $h^{(0)}(t)$ is selected. The coefficients of the decision feedback equalizer $b(n)$ are computed as shown in Equation (93A–24). If N_b is 0, then the $b(n)$ is considered to be zero for all n.
c) Define A_s to be $h^{(0)}(t_s)/(L-1)$.
d) Compute $h_{ISI}(n)$ per Equation (93A–25). This represents the residual intersymbol interference (ISI) after decision feedback equalization. The corresponding ISI amplitude variance σ_{ISI}^2 is computed per Equation (93A–28) and Equation (93A–27).
e) Compute the slope of the pulse response of the victim path $h_J(n)$ as shown in Equation (93A–26). The variance of the amplitude error due to timing jitter σ_J^2 is computed per Equation (93A–29) and Equation (93A–27).
f) The variance of the amplitude for path k is given by Equation (93A–30) where the phase index m can assume any integer value from 0 to $M-1$. Denote the value of m that maximizes the variance for path k as i. The variance of the amplitude for the combination of all crosstalk paths σ_{XT}^2 is then computed using Equation (93A–31) which is the sum of the maximum variances for the individual paths k=1 to $K-1$.
g) Compute the variance of the noise at the output of the receive equalizer σ_N^2 based on the one-sided spectral density η_0 referred to the receiver noise filter input per Equation (93A–32).
h) Compute the figure of merit (FOM) per Equation (93A–33).

$$h^{(0)}(t_s - T_b) = h^{(0)}(t_s + T_b) - h^{(0)}(t_s)b(1) \tag{93A–23}$$

$$b(n) = \begin{cases} -b_{\max}(n) & h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) < -b_{\max}(n) \\ b_{\max}(n) & h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) > b_{\max}(n) \\ h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) & \text{otherwise} \end{cases} \tag{93A–24}$$

$$h_{ISI}(n) = \begin{cases} 0 & n = 0 \\ h^{(0)}(t_s + nT_b) - h^{(0)}(t_s)b(n) & 1 \le n \le N_b \\ h^{(0)}(t_s + nT_b) & \text{otherwise} \end{cases} \tag{93A–25}$$

$$h_J(n) = \frac{h^{(0)}(t_s + (n + 1/M)T_b) - h^{(0)}(t_s + (n - 1/M)T_b)}{2/M} \tag{93A–26}$$

$$\sigma_X^2 = \frac{L^2 - 1}{3(L-1)^2} \quad (93A–27)$$

$$\sigma_{ISI}^2 = \sigma_X^2 \sum_n h_{ISI}^2(n) \quad (93A–28)$$

$$\sigma_J^2 = (A_{DD}^2 + \sigma_{RJ}^2)\sigma_X^2 \sum_n h_J^2(n) \quad (93A–29)$$

$$[\sigma_m^{(k)}]^2 = \sigma_X^2 \sum_n [h^{(k)}((m/M + n)T_b)]^2 \quad (93A–30)$$

$$\sigma_{XT}^2 = \sum_{k=1}^{K-1} [\sigma_i^{(k)}]^2 \quad (93A–31)$$

$$\sigma_N^2 = \eta_0 \int_0^\infty |H_r(f)H_{ctf}(f)|^2 df \quad (93A–32)$$

$$FOM = 10\log_{10}\left(\frac{A_s^2}{\sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right) \quad (93A–33)$$

The FOM is calculated for each permitted combination of $c(-1)$, $c(1)$, and g_{DC} values per Table 93A–1. The combination of values that maximizes the FOM, including the corresponding value of t_s, is used for the calculation of the interference and noise amplitude in 93A.1.7 and the calculation of COM in 93A.1.

93A.1.7 Interference and noise amplitude

Given the values of $c(-1)$, $c(1)$, g_{DC}, and t_s derived in 93A.1.6, compute the combined interference and noise distribution $p(y)$ per 93A.1.7.3. The corresponding cumulative distribution function is $P(y)$ as defined by Equation (93A–34).

$$P(y) = \int_{-\infty}^{y} p(y)dy \quad (93A–34)$$

The noise amplitude, A_n, is the magnitude of the value of y_0 that satisfies the relationship $P(y_0) = DER_0$ where DER_0 is the target detector error ratio. The detector error ratio is the probability that the detector fails to identify the signal level that was transmitted.

In 93A.1.7.1 through 93A.1.7.3, "*" denotes convolution which is defined by Equation (93A–35).

$$f(t) * g(t) = \int_{-\infty}^{\infty} f(\tau)g(t-\tau)d\tau \quad (93A–35)$$

93A.1.7.1 Interference amplitude distribution

The interference amplitude distribution is computed from the sampled pulse response $h(n)$ with the assumption that the transmitted symbols are independent, identically distributed random variables and that the sym-

bols are uniformly distributed across the set of L possible values. For the purpose of this subclause, $h(n)$ is a general notation that corresponds to $A_{DD}h_f(n)$ (see 93A.1.7.2), $h_{ISI}(n)$, or $h^{(k)}((i / M + n)T_b)$ (see 93A.1.7.3).

Equation (93A–36) defines the nth component of the interference amplitude distribution function where $\delta(y)$ is the Dirac delta function.

$$p_n(y) = \frac{1}{L}\sum_{l=0}^{L-1}\delta\left(y-\left(\frac{2l}{L-1}-1\right)h(n)\right) \quad (93A–36)$$

The set of N such components are combined via convolution to obtain the complete interference amplitude distribution. Initialize $p(y)$ to $\delta(y)$ and then evaluate Equation (93A–37) sequentially for n=0 to N–1.

$$p(y) = p(y) * p_n(y) \quad (93A–37)$$

NOTE—It is expected that COM will be numerically computed using a quantized amplitude axis y. The amplitude step Δy will introduce quantization error in the calculated distribution function that will be compounded by subsequent convolutions with other quantized distribution functions. It is recommended that Δy be no larger than 0.1 mV in order to limit the error.

93A.1.7.2 Noise amplitude distribution

The calculation of COM includes two noise terms that are described in terms of their distribution function. The first term has a Gaussian amplitude distribution function with zero mean and variance σ_G^2. The variance is defined by Equation (93A–38) where $H_r(f)$ is defined in 93A.1.4.1, $H_{ctf}(f)$ is defined in 93A.1.4.3, and σ_X^2 and $h_f(n)$ are defined in 93A.1.6.

$$\sigma_G^2 = \sigma_{RJ}^2\sigma_X^2\sum_n h_f^2(n) + \eta_0\int_0^\infty \left|H_r(f)H_{ctf}(f)\right|^2 df \quad (93A–38)$$

The amplitude distribution of the Gaussian noise term is defined by Equation (93A–39).

$$p_G(y) = \frac{\exp(-y^2/(2\sigma_G^2))}{\sqrt{2\pi\sigma_G^2}} \quad (93A–39)$$

The second term is denoted as p_{DD} and is related to the amplitude noise resulting from dual-Dirac jitter. It is computed using the procedure defined in 93A.1.7.1 with $h(n) = A_{DD}h_f(n)$.

The components are combined using convolution to yield the overall noise amplitude distribution function as defined in Equation (93A–40).

$$p_n(y) = p_G(y) * p_{DD}(y) \quad (93A–40)$$

93A.1.7.3 Combination of interference and noise distributions

Compute the intersymbol interference amplitude distribution using the procedure defined in 93A.1.7.1 with $h(n) = h_{ISI}(n)$ as defined by Equation (93A–25) and denote the result as $p(y)$.

The contributions of the K–1 crosstalk paths to the total interference are included as follows. Determine the phase index $m = i$ that maximizes the variance of the amplitude for path k as defined by Equation (93A–30). Compute the interference amplitude distribution using the procedure defined in 93A.1.7.1 with $h(n) = h^{(k)}((i / M + n)T_b)$ and denote the result as $p^{(k)}(y)$.

Compute $p^{(k)}(y)$ and evaluate Equation (93A–41) sequentially for integer values k=1 to K–1.

$$p(y) = p(y) * p^{(k)}(y) \quad (93A–41)$$

The noise distribution $p_n(y)$ defined in 93A.1.7.2 is then included to yield the combined interference and noise amplitude distribution as shown in Equation (93A–42).

$$p(y) = p(y) * p_n(y) \quad (93A–42)$$

93A.2 Test channel calibration using channel operating margin (COM)

A generalized block diagram of the interference tolerance test channel is shown in Figure 93A–2.

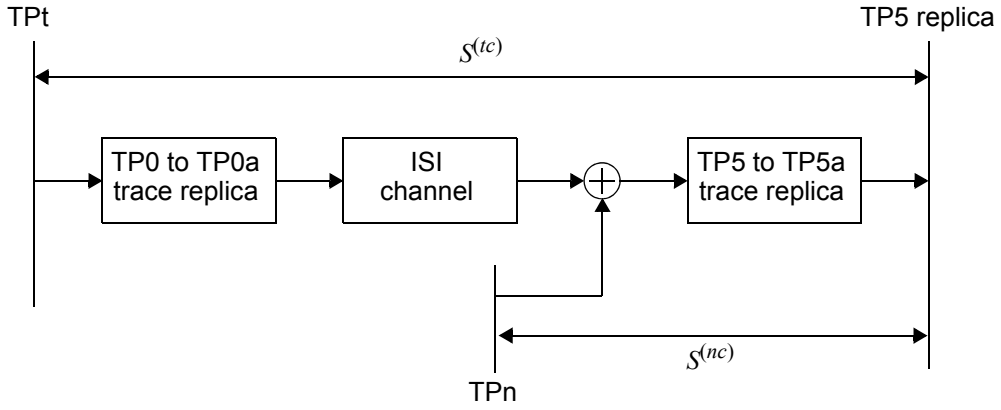


Figure 93A–2—Generalized interference tolerance test channel

The signal path from the test transmitter connected at TPt to the receiver under test connected at TP5 consists of replicas of the test fixture traces, a controlled ISI channel, and the means by which additive broadband noise is coupled into the path. This path is represented by the scattering parameters $S^{(tc)}$ measured from TPt to the TP5 replica. The signal path from the broadband noise source connected at TPn to the receiver consists of the means of broadband noise coupling and a replica of TP5 to TP5a test fixture trace. This path is represented by scattering parameters $S^{(nc)}$ measured from TPn to the TP5 replica.

Channel operating margin (COM) is used to calibrate the interference tolerance test channel. The values assigned to the parameters listed in Table 93A–1 are defined by the Physical Layer specification that invokes this method.

The calculations defined in 93A.1 are evaluated for $S^{(tc)}$ with the following exceptions.

If the test transmitter presents a high-quality termination, e.g. it is a piece of test equipment, the transmitter device package model $S^{(tp)}$ is omitted from the calculation of $S_p^{(k)}$. Instead, the voltage transfer function is multiplied by the filter $H_t(f)$ defined by Equation (93A–43) where T_r is the 20 to 80% transition time (see 93.8.1.5) of the signal as measured at TPta.

$$H_t(f) = \exp(-(\pi f T_r / 1.6832)^2) \quad (93A–43)$$

The approximate voltage transfer function for the path from TPn to the output of the receiver equalizer is defined by Equation (93A–44).

$$H^{(ne)}(f) = s_{21}^{(nc)}(f)\, s_{21}^{(rp)}(f)\, H_r(f)\, H_{ctf}(f) \tag{93A–44}$$

The broadband noise source applies noise at TPn that has a Gaussian amplitude distribution with zero mean and standard deviation σ_{bn}. The power spectral density of the noise is flat from $-f_b / 2$ to $f_b / 2$ and is zero elsewhere. The standard deviation of the noise at the receiver equalizer output σ_{ne} is defined by Equation (93A–45).

$$\sigma_{ne}^2 = \frac{2\sigma_{bn}^2}{f_b} \int_0^{f_b/2} \left|H^{(ne)}(f)\right|^2 df \tag{93A–45}$$

Equation (93A–38) defines the standard deviation of the Gaussian noise amplitude distribution function. When COM is used to calibrate the interference tolerance test channel, this definition is replaced by Equation (93A–46). The value of σ_{bn} is adjusted until the target COM value is achieved.

$$\sigma_G^2 = \sigma_{RJ}^2 \sigma_X^2 \sum_n h_J^2(n) + \eta_0 \int_0^{\infty} \left|H_r(f) H_{ctf}(f)\right|^2 df + \sigma_{ne}^2 \tag{93A–46}$$

An additional figure of merit for the test channel is the root-sum-square of the magnitude terms n_1 to n_2 of the equalized pulse response where n_2 is less than or equal to N_b. This measure of the relative usage of the decision feedback equalizer is defined by Equation (93A–47).

$$u_b(n_1, n_2) = \frac{1}{A_s} \sqrt{\sum_{i=n_1}^{n_2} \left(h^{(0)}(n)\right)^2} \tag{93A–47}$$

The shorthand notation RSS_DFE4 is used to represent $u_b(4, N_b)$.

93A.3 Fitted insertion loss

The fitted insertion loss as a function of frequency is given by Equation (93A–48).

$$IL_{fitted}(f) = a_0 + a_1\sqrt{f} + a_2 f + a_4 f^2 \tag{93A–48}$$

Denote the insertion loss, in dB, measured at frequency f_n as $IL(f_n)$. Given the insertion loss measured at N uniformly-spaced frequencies from start frequency $f_{\min}$ to stop frequency $f_{\max}$ with step no larger than Δf, the coefficients for the fitted insertion loss shall be calculated as follows.

Define the weighted frequency matrix F using Equation (93A–49).

$$F = \begin{bmatrix} 10^{-IL(f_1)/20} & \sqrt{f_1}10^{-IL(f_1)/20} & f_1 10^{-IL(f_1)/20} & f_1^2 10^{-IL(f_1)/20} \\ 10^{-IL(f_2)/20} & \sqrt{f_2}10^{-IL(f_2)/20} & f_2 10^{-IL(f_2)/20} & f_2^2 10^{-IL(f_2)/20} \\ \cdots & \cdots & \cdots & \cdots \\ 10^{-IL(f_N)/20} & \sqrt{f_N}10^{-IL(f_N)/20} & f_N 10^{-IL(f_N)/20} & f_N^2 10^{-IL(f_N)/20} \end{bmatrix} \quad \text{(93A–49)}$$

Define the weighted insertion loss vector L using Equation (93A–50).

$$L = \begin{bmatrix} IL(f_1)10^{-IL(f_1)/20} \\ IL(f_2)10^{-IL(f_2)/20} \\ \cdots \\ IL(f_N)10^{-IL(f_N)/20} \end{bmatrix} \quad \text{(93A–50)}$$

The fitted insertion loss coefficients are then given by Equation (93A–51).

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T L \quad \text{(93A–51)}$$

The values assigned to $f_{\min}$, $f_{\max}$, and Δf are defined by the Physical Layer specification that invokes this method.

Annex 93B

(informative)

Electrical backplane reference model

This annex describes additional informative test points that may used to partition the electrical backplane channel.

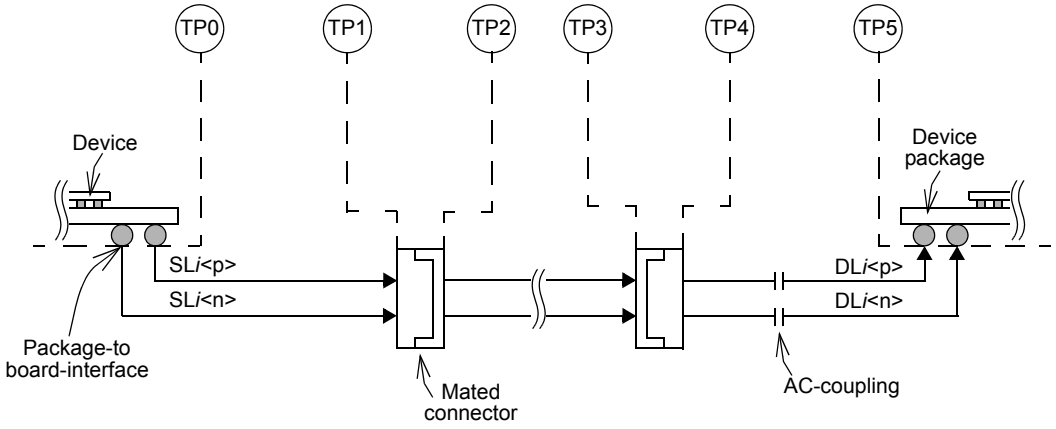


Figure 93B–1—Reference model (one direction from one lane is illustrated)

Table 93B–1—Description of channel components

Test points	Description
TP0 to TP1	The printed circuit board between the transmitter and the separable connector closest to the transmitter. TP1 is defined to be the interface between the board and connector plug.
TP2 to TP3	The electrical path from the separable connector closest to the transmitter to the separable connector closest to the receiver. TP2 and TP3 are defined to be the interface between connector receptacle and the printed circuit board.
TP4 to TP5	The printed circuit board between the receiver and the separable connector closest to the receiver. TP4 is defined to be the interface between the board and connector plug. It is recommended that the AC-coupling capacitors are implemented between TP4 and TP5
TP0 to TP5	The electrical backplane channel as defined in 93.9 and 94.4. TP0 and TP5 are defined to be the interface between the device package and the printed circuit board.

Annex 93C

(informative)

(normative)

Receiver interference tolerance

This annex defines a test setup (see 93C.1) and method (see 93C.2) for testing receiver interference tolerance. The PMD clause that invokes this method specifies for the following items:

a) the relevant noise parameter and target value for test setup,
b) constraint limit values for peak-to-peak voltage, the pre-cursor peaking ratio, and the post-cursor peaking ratio for test setup,
c) the lower frequency bound for the noise spectral density constraints (f_{NSD1}),
d) the noise parameter and target value for test method step 3,
e) the jitter parameters to be measured in test method step 5,
f) the target COM and RSSDFE4 values for the test system in test method step 8,
g) the COM parameter table in test method step 8,
h) the jitter transformation method in test method step 8,
i) the test pattern in test method step 10, and
j) the test system frequency response.

93C.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 93C–2 or its equivalent. Calibration and characterization of the various elements in the test setup is accomplished using the test configurations in Figure 93C–3, Figure 93C–4, Figure 93C–5, and Figure 93C–6.

The transmitter is functionally and parametrically compliant to the requirements of the invoking PMD clause. The transmit noise source is used to degrade the transmitter output so that it exhibits the worst-case noise characteristics specified by the invoking PMD clause as measured at TPta. The transmit noise source and summer may be excluded from the test setup if the transmitter can provide the correct noise characteristics. The ISI channel emulates the frequency dependent loss of a backplane channel. The channel noise source emulates crosstalk and unequalizable signal distortions introduced by a channel.

The transmitter output, as measured at TPta, meets all transmitter specifications as indicated by the invoking PMD clause. In addition, the transmitter output, as measured at TPta, is constrained such that for any transmitter equalizer setting the maximum differential peak-to-peak voltage, the pre-cursor peaking ratio, and the post-cursor peaking ratio are constrained as indicated by the PMD clause that invokes this method.

The transmit and channel noise sources have adjustable outputs such that the levels may be set according to the test procedure. The noise produced by the transmit and channel noise sources are measured directly at the output of each noise source (see Figure 93C–6). The noise is Gaussian with a crest factor of at least 4. The noise spectral density, $NSD(f)$, is normalized and constrained according to the relations in Equation (93C–1), where f_b is the symbol rate and f_{NSD1} is specified by the PMD clause that invokes this

method. $NSD(f)$ is in units of V^2/Hz. The average noise spectral density, NSD_{average}, is determined according Equation (93C–2). An example constraint template with f_{NSD1} equal to $0.08f_b$ is illustrated in Figure 93C–1.

$$\left.\begin{aligned} 10\log_{10}\left(\frac{NSD(f)}{NSD_{average}}\right) &< 3 \\ 10\log_{10}\left(\frac{NSD(f)}{NSD_{average}}\right) &> -3(1-1.2f/f_b) \end{aligned}\right\} f_{NSD1} \le f \le f_b/2 \qquad \text{(93C–1)}$$

$$NSD_{average} = \frac{\int_{f_{NSD1}}^{f_b/2} NSD(f)df}{f_b/2 - f_{NSD1}} \qquad \text{(93C–2)}$$

The receiver on one lane at a time is tested for compliance. The input to the receiver on each of the other lanes is generated by a transmitter with similar levels and equalization settings and transmitted through a similar channel, such that the input signals are similar to the input signal on the lane under test. During the test, the transmitters of the PMD under test transmit the pattern specified by the PMD clause that invokes this method, with the transmitters in the preset condition.

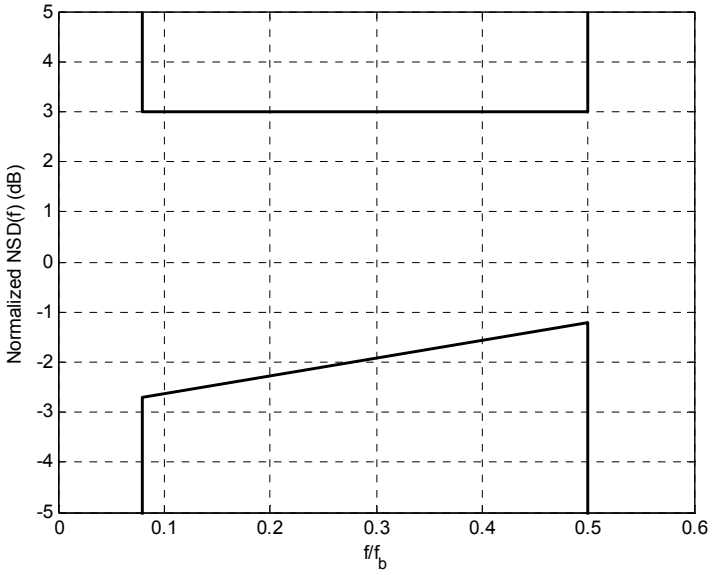


Figure 93C–1—Example NSD(f) constraint template

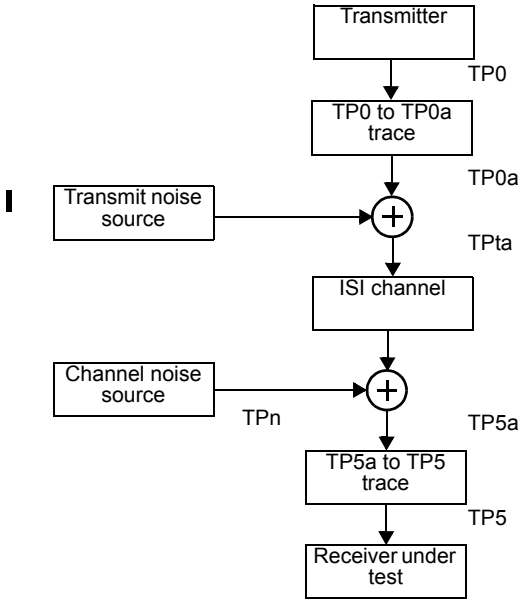


Figure 93C–2—Interference tolerance test setup

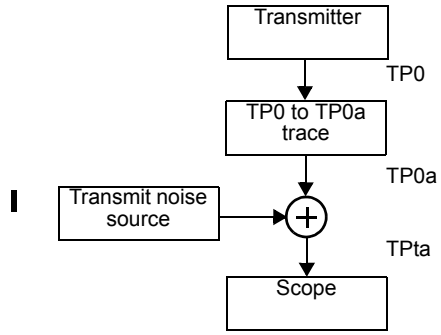


Figure 93C–3—Interference tolerance transmitter test setup

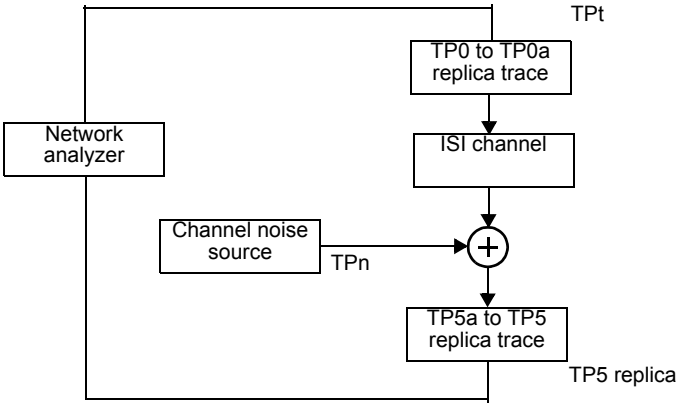


Figure 93C–4—Interference tolerance channel s-parameter test setup

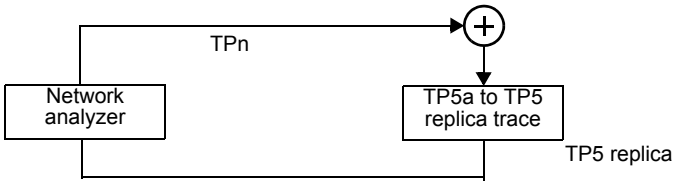


Figure 93C–5—Interference tolerance channel noise path test setup

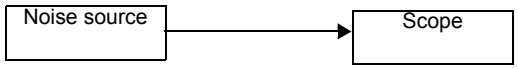


Figure 93C–6—Interference tolerance channel noise level test setup

93C.2 Test method

The following method is repeated for each lane for Test 1 and Test 2.

1) Set the transmit noise source and channel noise source to zero.
2) Using the test setup in Figure 93C–2, initiate the training sequence, allow the training sequence to complete, and retain the resulting transmitter tap coefficients.
3) Enable the transmit noise source (if not already enabled) and adjust the noise level to give the worst case noise allowable by the PMD clause that invokes this method as measured at TPta.
4) Iterate steps 2 and 3 until the transmitter taps have converged.
5) Measure the jitter parameters relevant to the PMD clause that invokes this method that are to be used to set the value of σ_{RJ} and A_{DD} in step 8.
6) Using the test setup in Figure 93C–4 (also see Figure 93A–2), measure the scattering parameters, $S^{(tc)}$, of the test channel (TPt to TP5 replica).
7) Using the test setup in Figure 93C–5 (also see Figure 93A–2), measure the scattering parameters, $S^{(nc)}$, of the noise addition network (TPn to TP5 replica).
8) Using the procedure defined in 93A.2: (a) determine the receiver noise level, σ_{bn}, required to achieve the COM value specified in the PMD clause that invokes this method and (b) verify that RSS_DFE4 is greater than or equal to the value specified in the PMD clause that invokes this method. The procedure is based on the calculation of COM which uses the parameters defined in the COM parameter table in the PMD clause that invokes this method with the following exceptions. The value of σ_{RJ} and A_{DD} are set based on a transformation of measured parameters as specified in the PMD clause that invokes this method. In the COM computation the transmitter package model is included only if a compliant transmitter with a similar termination is used. If a transmitter with high quality termination is used, in the COM calculation, the termination is modeled as ideal and a Gaussian low pass filter is added to equation 93A-17 which has the same 20%-80% transition time as the transmitter measured at TPta.
9) Using the test setup in Figure 93C–6, measure the channel noise voltage σ_{bnm} and adjust it so that it equals σ_{bn} determined in step 8. The channel noise voltage is determined from the measured $NSD(f)$ according to Equation (93C–3).
10) Using the test setup in Figure 93C–2, the transmitter taps and transmit noise as determined in step 4, and the channel noise as determined in step 8, configure the transmitter PCS to transmit the test pattern specified in the PMD clause that invokes this method.

11) Measure the FEC symbol error ratio on the receiver under test using the errored symbol counter, FEC_symbol_error_*i*, where *i* is the lane number of the receiver under test.

$$\sigma_{bnm} = \sqrt{\int_0^{f_b/2} NSD(f)df} \qquad (93C–3)$$

A test system with frequency response specified in the PMD clause that invokes this method is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.