IEEE P802.3az™/D1.2, Mar 2009
(Draft Amendment of IEEE Std 802.3-2008)

IEEE *Draft* P802.3az™/D1.2

Draft Standard for Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—
Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment:
Media Access Control parameters, Physical Layers and management parameters for Energy-Efficient Ethernet

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2008 and includes a new clause, Clause 78, which provides an overview of changes required to enable energy efficient operation of several existing physical layers. Changes to the specifications of these physical layers are also included in this draft. Draft D1.2 is prepared by the IEEE 802.3az Energy Efficient Task Force for Task Force Review. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

IEEE Standards Activities Department

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Abstract: This amendment to IEEE Std 802.3–2008 specifies changes to several existing physical layers to enable energy efficient operation of Ethernet. Changes to 10BASE-T include a reduction in transmit voltage requirements. Changes to 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KX4 and 10GBASE-KR include the definition of a low power idle mode and mechanisms to communicate and manage the entry and exit into and out of low power idle and the operation of this mode. New LLDP TLVs are defined for negotiating system level energy efficiency parameters.
Keywords: 802.3az, 10BASE-T, 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, Backplane Ethernet, Energy Efficient Ethernet, Low Power Idle Mode, TLV, LLDP

Introduction

Editor's Note (to be removed prior to publication):

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

One exceptions to IEEE style that is consciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecutively with arabic page numbers.

This introduction is not part of IEEE Std 802.3az-2010, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements, Part 3: CSMA/CD Access Method and Physical Layer Specifications, Amendment: Energy Efficient Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE 802.3an-2006). A historical listing of all projects that have added to or modified IEEE Std 802.3 follows as a part of this introductory material. The listing is in chronological order of project initiation and for each project describes: subject, clauses added (if any), approval dates, and committee officers.

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in, and are superceded by, IEEE Std 802.3-2008 and are not maintained as separate documents.

At the date of IEEE Std 802.3az-2010 publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2008

Section One -- Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two -- Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s physical layer specifications.

Section Three -- Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s physical layer specifications.

Section Four -- Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s physical layer specifications.

Section Five -- Includes Clause 56 through Clause 74 and Annex 57A through Annex 74A. Clause 56 through Clause 67 and associated annexes specify subscriber access physical layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s physical layer specification. Clause 69 through 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

IEEE Std 802.3at™–200X

This amendment includes changes to IEEE Std 802.3–2008 to augment the capabilities of IEEE Std 802.3 with higher power levels and improved power management information.

IEEE Std 802.3av™–200X

This amendment includes changes to IEEE Std 802.3–2008 and adds Clauses 91 through 93 and Annex 91A. This amendment adds new Physical Layers for 10 Gb/s operation on point-to-multipoint passive optical networks.

IEEE 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Notice to users

Errata

Errata, if any, for this and all other standards can be accessed at the following URL:
http://standards.ieee.org/reading/ieee/updates/errata/index.html.
Users are encouraged to check this URL for errata periodically.

Downloads

Portions of this standard can be downloaded from the Internet. Materials include PICS tables, data tables, and code. URLs are listed in the text in the appropriate sections.

Interpretations

Current interpretations can be accessed at the following URL:
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Participants

The following individuals were members of the IEEE 802.3 working group at the beginning of the P802.3xx working group ballot. Individuals may have not voted, voted for approval, disapproval, or abstained on this amendment.

David J. Law, *Working Group Chair*
Wael William Diab, *Working Group Vice Chair*

Adam Healey, *Working Group Secretary*
Steven B. Carlson, *Working Group Executive Secretary*
Bradley Booth, *Working Group Treasurer*

Michael J. Bennett, *Chair, Energy Efficient Task Force*
Sanjay Kasturia, *Chief Editor, Energy Efficient Task Force*

xxx

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

xxx

xxx

When the IEEE–SA Standards Board approved this standard on 15 September 200X, it had the following membership:

xxx, *Chair*
xxx, *Vice Chair*
xxx, *Past Chair*
xxx, *Secretary*

xxx

*Member Emeritus

Also included are the following nonvoting IEEE–SA Standards Board liaisons:

NRC Representative
DOE Representative
NIST Representative

Michelle Turner
IEEE Standards Program Manager, Document Development

Michael D. Kipness
IEEE Standards Program Manager, Technical Program Development

List of special symbols

For the benefit of those who have received this document by electronic means, what follows is a list of special symbols and operators. If any of these symbols or operators fail to print out correctly on your machine, the editors apologize, and hope that this table will at least help you to sort out the meaning of the resulting funny-shaped blobs and strokes.

Special symbols and operators

Printed character	Meaning	Keystrokes	Character code	Font
*	Boolean AND	*	ALT-042	Symbol
+	Boolean OR, arithmetic addition	+	ALT-043	Symbol
^	Boolean XOR	^	ALT-094	Times New Roman
!	Boolean NOT	!	ALT-033	Symbol
×	Multiplication	Ctrl-q 4	ALT-0180	Symbol
<	Less than	<	ALT-060	Symbol
≤	Less than or equal to	Ctrl-q #	ALT-0163	Symbol
>	Greater than	>	ALT-062	Symbol
≥	Greater than or equal to	Ctrl-q 3	ALT-0179	Symbol
=	Equal to	=	ALT-061	Symbol
≠	Not equal to	Ctrl-q 9	ALT-0185	Symbol
⇐	Assignment operator	Ctrl-q \	ALT-0220	Symbol
∈	Indicates membership	Ctrl-q Shift-n	ALT-0206	Symbol
∉	Indicates nonmembership	Ctrl-q Shift-o	ALT-0207	Symbol
±	Plus or minus (a tolerance)	Ctrl-q 1	ALT-0177	Symbol
°	Degrees	Ctrl-q 0	ALT-0176	Symbol
∑	Summation	Esc ^ Shift-a	ALT-0229	Symbol
√	Square root	Ctrl-q Shift-v	ALT-0214	Symbol
—	Big dash (em dash)	Ctrl-q Shift-q	ALT-0151	Times New Roman
–	Little dash (en dash), subtraction	Ctrl-q Shift-p	ALT-0150	Times New Roman
|	Vertical bar	|	ALT-0124	Times New Roman
†	Dagger	Ctrl-q Space	ALT-0134	Times New Roman
‡	Double dagger	Ctrl-q ‘	ALT-0135	Times New Roman
α	Lower case alpha	a	ALT-097	Symbol
β	Lower case beta	b	ALT-098	Symbol
γ	Lower case gamma	g	ALT-103	Symbol
δ	Lower case delta	d	ALT-100	Symbol
ε	Lower case epsilon	e	ALT-101	Symbol
λ	Lambda	l	ALT-0108	Symbol
μ	Micro	Ctrl-q 5	ALT-0181	Times New Roman
Ω	Omega	W	ALT-087	Symbol
Π	Upper case Pi	Shift-p		Symbol

Revisions to IEEE Std 802.3-2008, Clause 1

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: To be removed prior to final publication.
We have dropped plans to move TPPMD into 802.3. It is currently specified in an external reference.
References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	**Intial draft for IEEE P802.3az Task Force review.**

1. Introduction

1.3 Normative references

Editors' Notes: To be removed prior to final publication.

Check status of ANSI X3.263-1995, Revision 2.2 (1 March 1995), FDDI Twisted Pair—Physical Medium Dependent (TPPMD).

1.4 Definitions

Editors' Notes: To be removed prior to final publication.

Need to check if more EEE related terms need to be added to the list of definitions.

Insert the following defintion(s) in alphanumeric order:

10BASE-Te	IEEE 802.3 Physical Layer specification for an Energy Efficient version of 10BASE-T for a 10Mb/s CSMA/CD local area network over two pairs of Category 5 or better balanced cabling. (See IEEE 802.3, Clause 14.)

1.5 Abbreviations

Editors' Notes: To be removed prior to final publication.

Check to see if any addtional EEE related abbreviations need to be added here.

1.1 Abbreviations

Insert the following abbreviations in alphanumeric order:

LPI	label to indicate "Low Power Idle"

Revisions to IEEE Std 802.3-2008, Clause 14

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Intial draft for IEEE P802.3az Task Force review.

Change the clause heading as shown below:

14.Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T and type 10BASE-Te

14.1 Scope

14.1.1 Overview

Change the first paragraph of 14.1.1 as shown below:

Clause 14 defines the functional, electrical, and mechanical characteristics of the type 10BASE-T MAU and one specific medium for use with that MAU. This clause also specifies characteristics of the Energy Efficient version of 10BASE-T (type 10BASE-Te) MAU. The relationship of this clause to the entire ~~ISO/IEC 8802-3~~IEEE Std 802.3 LAN International Standard is shown in Figure 14–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Clause 1 through Clause 7 and Clause 9 of this standard.

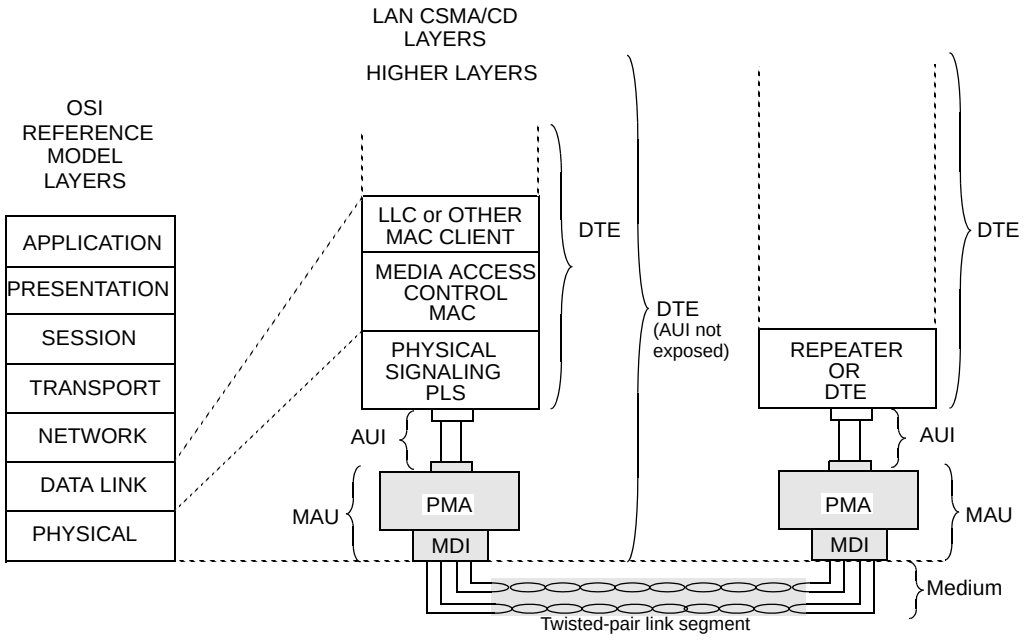


Figure 14–1—10BASE-T relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

14.1.1.1 Medium Attachment Unit (MAU)

Change item (c) as shown below and insert item (i) into the list of general characteristics as shown below:

The MAU has the following general characteristics:

a) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Clause 14.
b) Supports message traffic at a data rate of 10 Mb/s.
c) Provides for operating over 0 m to at least 100 m of twisted pair without the use of a repeater. The 10BASE-T PHY provides for operating over 0 m to at least 100 m of twisted pair cabling meeting or exceeding the simplex link segment specification found in 14.4. This specification is generally met by 0.5 mm telephone twisted pair. The 10BASE-Te PHY provides for operation over 0 m to at least 100 m of ISO/IEC 11801:1995 Class D or better cabling.
d) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.
e) Supports network configurations using the CSMA/CD access method defined in this standard with baseband signaling.
f) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.
h) Allows for either half duplex operation, full duplex operation, or both.
i) Provides for operation with reduced transmit amplitude for a type 10BASE-Te MAU (optional).

14.1.1.2 Twisted-pair media

Insert paragraph as shown below:

The medium for 10BASE-T is twisted-pair wire. The performance specifications of the simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter [26 AWG to 22 AWG] unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

The medium for 10BASE-Te is a channel meeting or exceeding the requirements of the Class D channel specified by ISO/IEC 11801:1995.

14.3 MAU electrical specifications

Change the first paragraph of 14.3 as shown below:

This subclause defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Clause 7 when the AUI is implemented. This subclause also defines the electrical characteristics of the type 10BASE-Te MAU at the MDI and the AUI.

Additional information relative to conformance testing is given in B.4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

14.3.1 MAU-to-MDI interface characteristics

14.3.1.2 Transmitter specifications.

The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this subclause.

Where a load is not specified, the transmitter shall meet requirements of this subclause when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

Change the third paragraph onwards of 14.3.1.2 to read as shown below:

Some tests in this subclause require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Figure 14–7 for a type 10BASE-T MAU and according to Figure 14–7a for a type 10BASE-Te MAU with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to section 1 and the signal measured across a load connected to section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit. Also, the value of the resistor that is in series with the inductors includes the series resistance of the inductor itself. The actual value of the resistor that is used is computed by subtracting the series resistance of the inductor from the resistor value shown in the figure.

~~The~ For a type 10BASE-T MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.

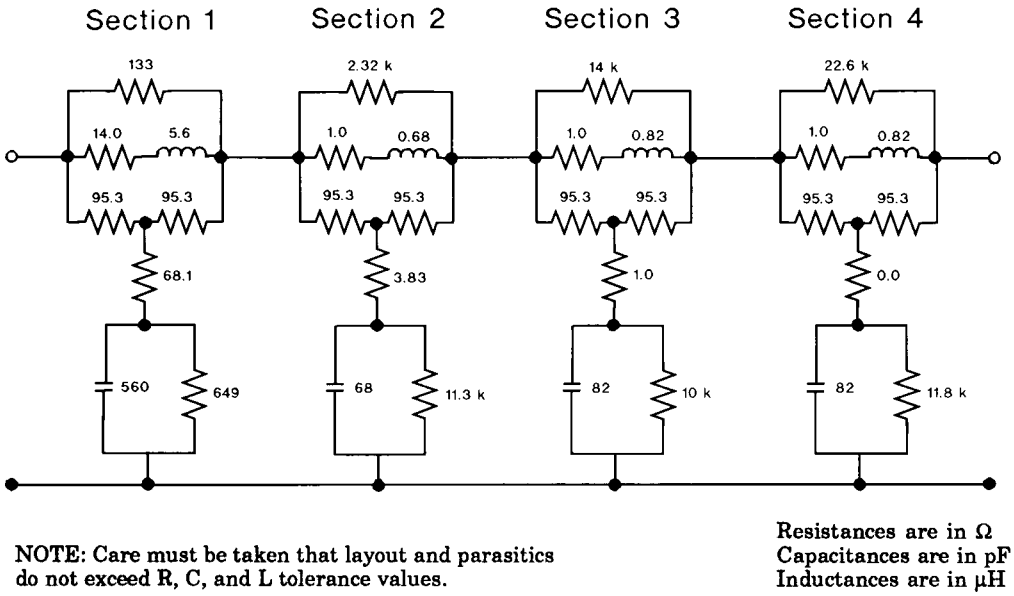
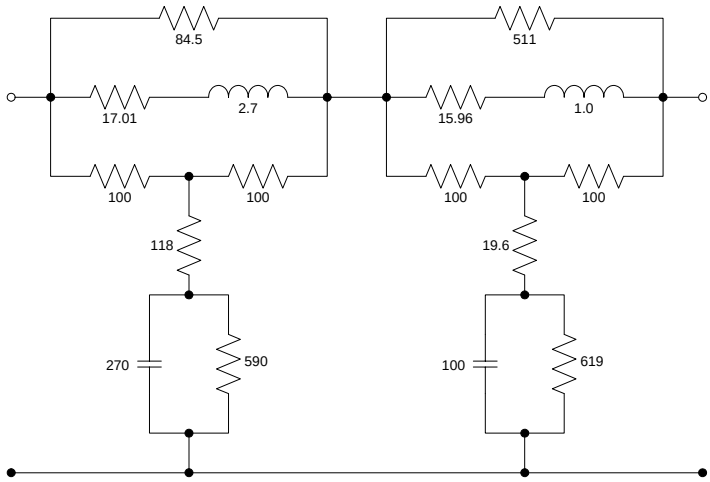


Figure 14–7—Twisted-pair model for 10BASE-T

Insert Figure 14–7a ***showing new twisted-pair model after Figure 14.7 (which shows the existing twisted-pair model) and renumber subsequent figures appropriately.***

For a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 6.8 dB and 7.4 dB at 10 MHz, and between 4.75 dB and 5.25 dB at 5 MHz so that it matches the worst case insertion loss for a Class D channel as specified in ISO/IEC 11801:1995.



NOTE: Care must be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

Figure 14–7a—Twisted-pair model for 10BASE-Te

14.3.1.2.1 Differential output voltage

Some of the text and figures of this subclause describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

Change the second and third paragraphs of 14.3.1.2.1 (Differential output voltage) to read as shown below:

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences for a type 10BASE-T MAU. For a type 10BASE-Te MAU, the peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 1.54V and 1.96V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal V_o, is defined at the output of the twisted-pair model as shown in Figure 14–8. The specific twisted-pair model used in Figure 14–8 shall be the equivalent circuit shown in Figure 14–7 for 10BASE-T and shall be the equivalent circuit shown in Figure 14–7a for 10BASE-Te. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Figure 14–9 for all data sequences. Voltage and time coordinates for inflection points on Figure 14–9 are given in Table 14–1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Figure 14–9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in B.4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output

waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

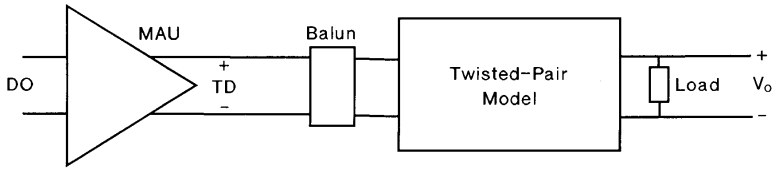


Figure 14–8—Differential output voltage test

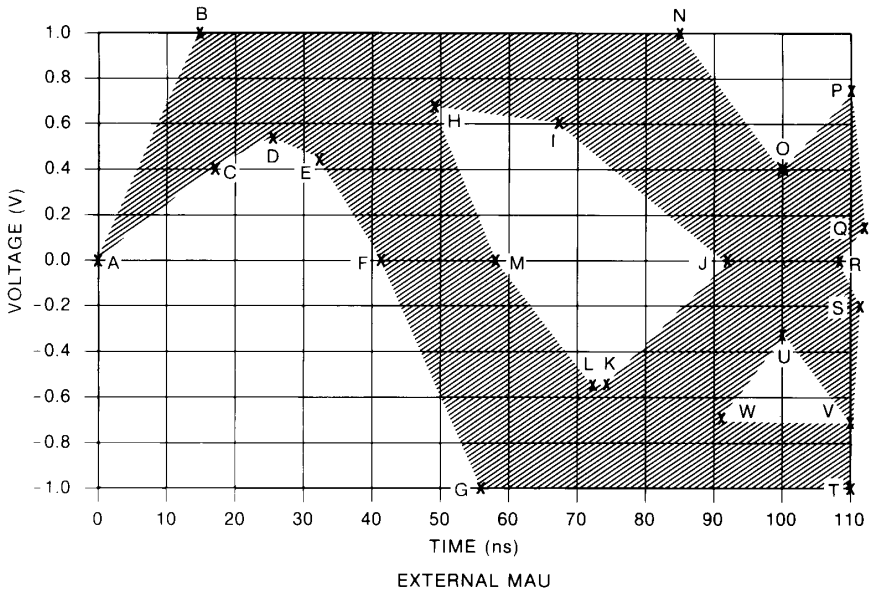


Figure 14–9—Voltage template

Table 14–1—Voltage template values for Figure 14–9

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
A	0	0	0
B	15	15	1.0
C	15	15	0.4
D	25	25	0.55
E	32	32	0.45
F	42	39	0
G	57	57	–1.0
H	48	48	0.7
I	67	67	0.6
J	92	89	0
K	74	74	–0.55
L	73	73	–0.55
M	58	61	0
N	85	85	1.0
O	100	100	0.4
P	110	110	0.75

Table 14–1—Voltage template values for Figure 14–9 *(continued)*

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
Q	111	111	0.15
R	108	111	0
S	111	111	–0.15
T	110	110	–1.0
U	100	100	–0.3
V	110	110	–0.7
W	90	90	–0.7

This test shall be repeated with the template inverted about the time axis. In that case, t = 0 on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See B.4.3.3 for modification of the template to test jitter.)

The TP_IDL shall always start with a positive waveform when a waveform conforming to Figure 7–12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14–10. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Figure 14–10 shall be met when measured across each of the test loads defined in Figure 14–11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8.

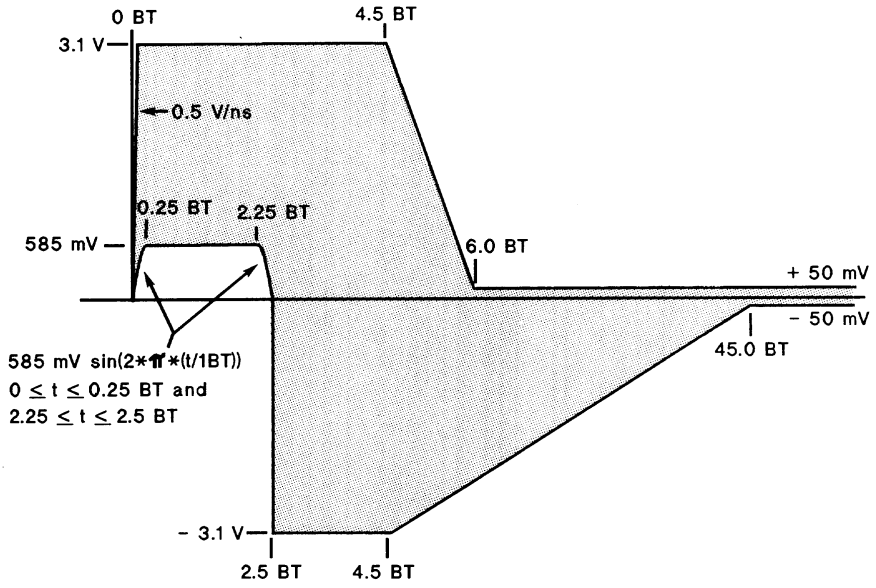
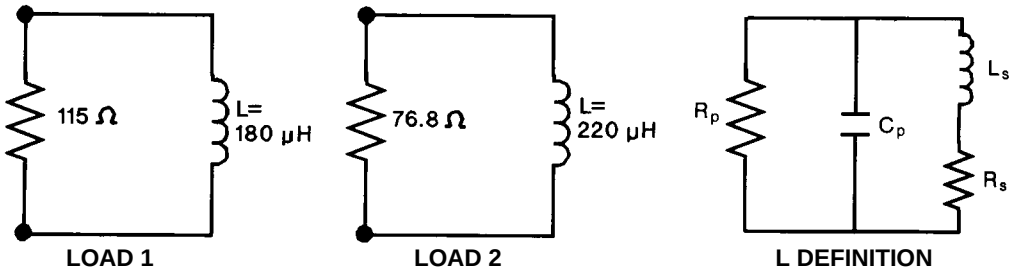


Figure 14–10—Transmitter waveform for start of TP_IDL

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Figure 14–12. Once the differential output voltage has become more negative than –50 mV, it

shall remain less than +50 mV. The template requirements of Figure 14–12 shall be met when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8.



All parameters are defined over the frequency range of 250 kHz to 6 MHz.

$L_s = L \pm 1\%$ $R_p \geq 2\ k\Omega$
$C_p = 12\ pF \pm 20\%$ $R_s \leq 0.5\ \Omega$

Figure 14–11—Start-of-TP_IDL test load

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the template requirements of Figure 14–12 when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8.

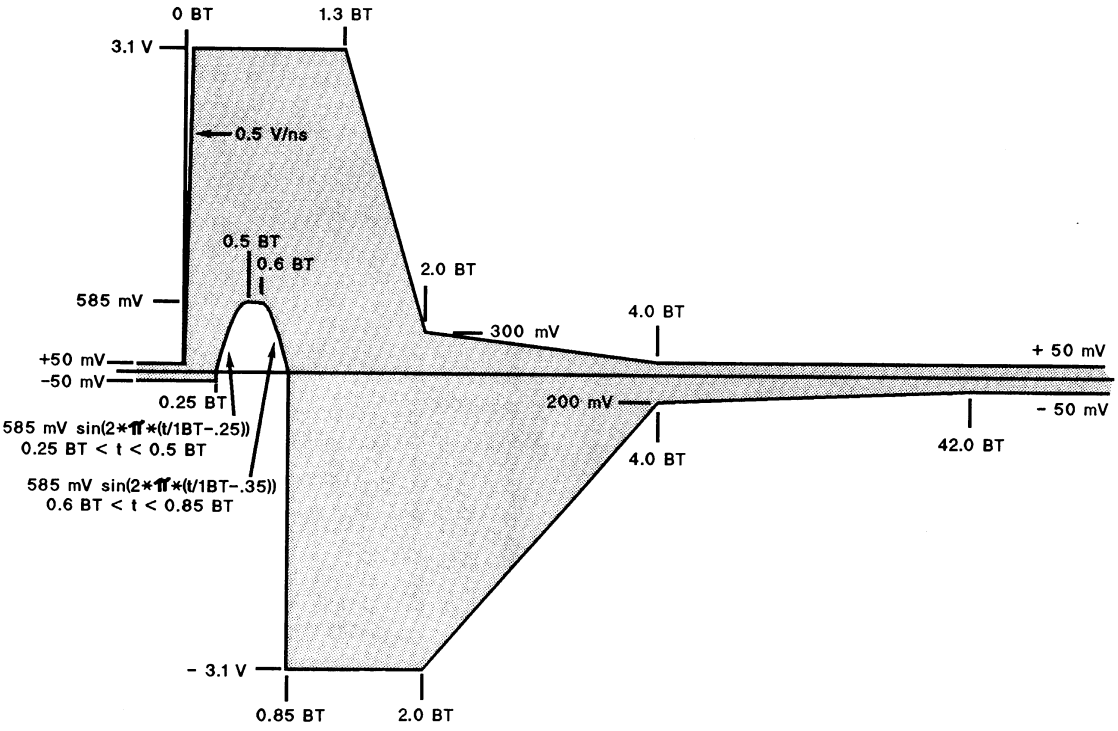


Figure 14–12—Transmitter waveform for link test pulse

14.4 Characteristics of the simplex link segment

Editor's Notes: *To be removed prior to publication.*
Check if the various specifications of the link segment need any changes to account for the introduction of 10BASE-Te. Currently on the overview and the insertion loss sections have been modified.

Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

14.4.1 Overview

Insert sentence as shown after the first paragraqh of 14.4.1

The medium for 10BASE-T is twisted-pair wiring. Since a significant number of 10BASE-T networks are expected to be installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

The medium for 10BASE-Te is a channel meeting or exceeding the requirements of the Class D channel specified by ISO/IEC 11801:1995.

NOTE—ISO/IEC 11801:2002 provides a specification for media that exceeds the minimum requirements of this standard.

14.4.2.1 Insertion loss

Insert sentence as shown below in first paragraph of 14.4.2.1

The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 and 10 MHz for a 10BASE-T MAU. For a 10BASE-Te MAU, the insertion loss of a simplex link segment shall be no more than 8.5 dB at all frequencies between 5.0 MHz and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE—Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

14.8 MAU labeling

Insert item (e) in list as shown below:

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s,
b) Power level in terms of maximum current drain (for external MAUs),
c) Any applicable safety warnings,
d) Duplex capabilities, and
e) 10BASE-T or 10BASE-Te support.

See also 14.5.2.

Change section 14.10 header to read as shown below:

14.10 Protocol implementation conformance statement (PICS) proforma for Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T and type 10BASE-Te[1]

14.10.4.5.12 Transmitter specification

Change TS1 to read as shown below. Insert TS2 and renumber subsequent entries in the PICS:.

	Parameter	Subclause	Req	Imp	Value/Comment
TS1	Peak differential output voltage on TD circuit for a type 10BASE-T MAU	14.3.1.2.1	C~~M~~		Conditional on whether it is a type 10BASE-T MAU. 2.2 to 2.8 V
TS2	Peak differential ouput voltage on TD circuit for a type 10BASE-Te MAU	14.3.1.2.1	C		Conditional on whether it is a type 10BASE-Te MAU. 1.54 to 1.96 V

14.10.4.5.12 10BASE-T link segment characteristics

Change LS4 to read as shown below. Insert LS5 and renumber subsequent entries in the PICS:

Editor's Notes: *To be removed prior to publication.*
Check if 10BASE-Tee will require changes to the PICS relating to the Insertion Loss specifications.

	Parameter	Subclause	Req	Imp	Value/Comment
LS4	Insertion loss, 5.0 to 10 MHz for a type 10BASE-T MAU	14.4.2.1	C		Conditional on whether it is a type 10BASE-T MAU. ≤ 11.5 dB
LS5	Insertion loss, 5.0 to 10 MHz for a type 10BASE-Te MAU	14.4.2.1	C		Conditional on whether it is a type 10BASE-Te MAU. ≤ 8.5 dB

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 22

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Intial draft for IEEE P802.3az Task Force review.

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

Editors' Notes: *To be removed prior to publication.*
Changes to MII interface for EEE operation.

Change 22.2.1 for LPI function:

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2. The mapping changes slightly when low power idle signaling is in operation, this is described in 22.7a. The definition of low power idle signaling assumes the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in low power idle mode.

Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the station management entity (STA).

Editors' Notes: *To be removed prior to publication.*
Figure 22-3 is changed to correct an error in 802.3-2008/2005.

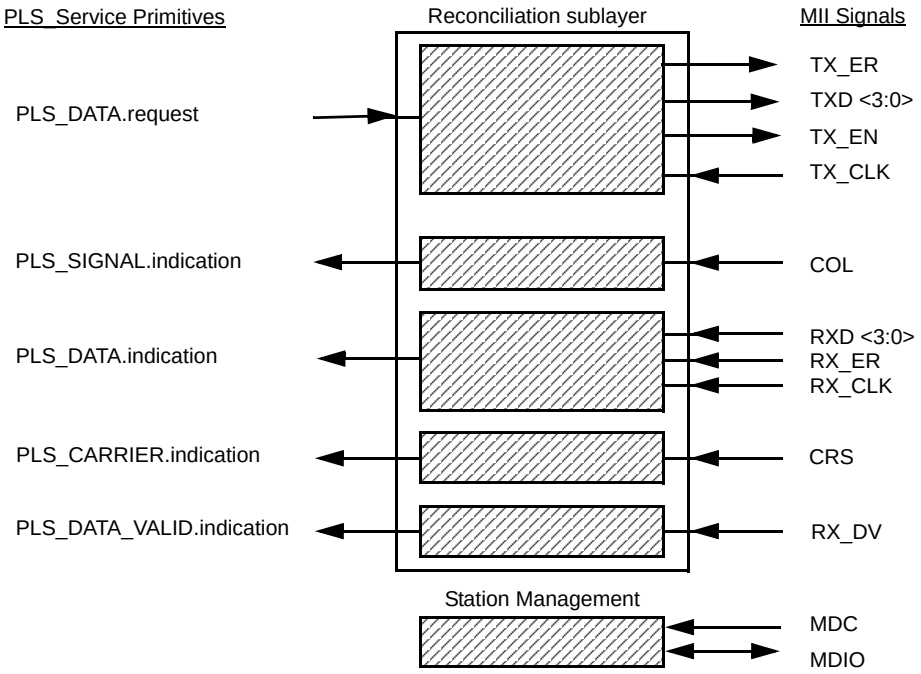


Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

Change 22.2.1.3 for PLS_CARRIER.indication:

22.2.1.3 Mapping of PLS_CARRIER.indication

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the MII signal CRS.

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signal CRS and from the transmit LPI state machine.

22.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value. Any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the receiveDataValid variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC processBitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

For LPI operation, in full duplex mode RX_DV and CRS have no influence on CARRIER_STATUS, a transition to the LPI_ASSERTED state in the transmit LPI state machine shall cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and a transition to the LPI_DEASSERTED state in the transmit LPI state machine shall cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

Change 22.2.2 to show LPI signaling:

22.2.2 MII signal functional specifications

Change NOTE in 22.2.2.2 for clock definitions:

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5 and 22.2.2.9a.

Change 22.2.2.4 for TXD definition:

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is

asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN and TX_ER are both ~~is~~ de-asserted, TXD<3:0> shall have no effect upon the PHY.

The PHY shall interpret the combination of TX_EN, TX_ER and TXD<3:0> as shown in Table 22–1 as an assertion of low power idle. Transition into and out of the low power idle state is shown in Figure 22–6a. Other values of TXD<3:0> shall have no effect upon the PHY.

Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
~~0~~	~~1~~	~~0000 through 1111~~	~~Reserved~~
0	1	0000	Reserved
0	1	0001	Assert low power idle
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Insert 22.2.2.6a for transmit low power idle transition:

22.2.2.6a Transmit direction low power idle transition

When the transmit LPI state machine is in state LPI_ASSERTED, the MAC device asserts that it wishes the PHY to transition to the low power idle state by deasserting TX_EN, asserting TX_ER and setting TXD<3:0> to 0001. The MAC device maintains the same state for these signals for the entire time that it wishes the PHY to remain in the low power idle state.

When the MAC device wishes the PHY to transition out of the low power idle state it deasserts TX_EN and TX_ER. The MAC device should not assert TX_EN for valid transmit data until after the wake up time specified for the PHY.

Figure 22–6a shows the behavior of TX_EN, TX_ER and TXD<3:0> during the transition into and out of the low power idle state.

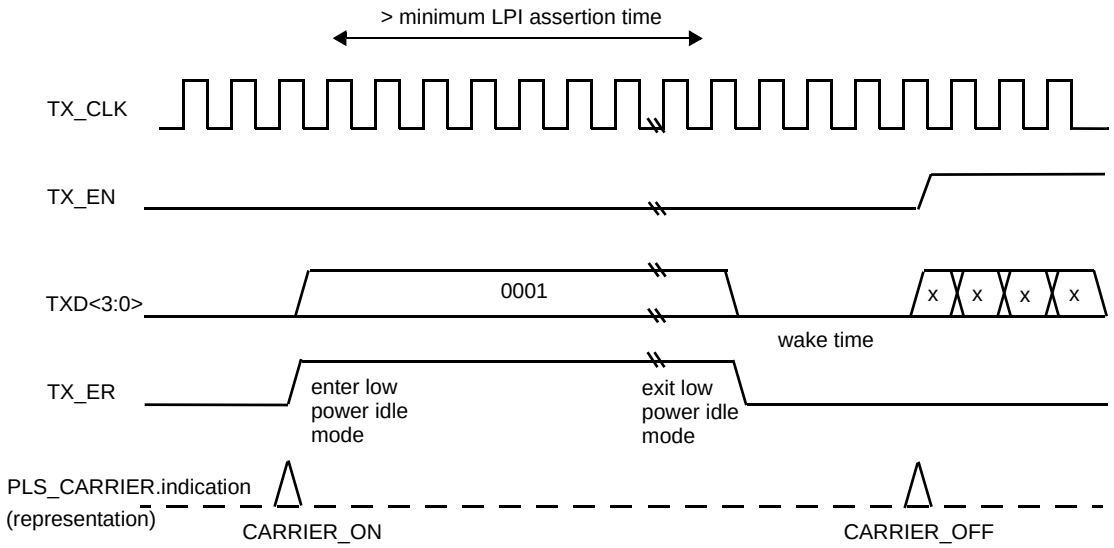


Figure 22–6a—Low power idle transition

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Change 22.2.2.7 for RXD definition:

22.2.2.7 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RX_DV is de-asserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 22.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

While RX_DV is de-asserted, a PHY that supports low power idle operation shall indicate that it is receiving low power idle by asserting the RX_ER signal while driving the value 0001 onto RXD<3:0>.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <3:0> must not be looped back to RXD <3:0> unless the loopback mode of operation is selected.

Figure 22–6 shows the behavior of RXD<3:0> during frame reception.

Table 22–2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
~~0~~	~~1~~	~~0001 through 1101~~	~~Reserved~~
0	1	0001	Receive low power idle
0	1	0010 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

Insert 22.2.2.9a for receive low power idle transition:

22.2.2.9a Receive direction low power idle transition

When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the MAC device by asserting RX_ER and setting RXD<3:0> to 0001 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power idle state. When the PHY receives signals from the link partner to indicate transition out of the low power idle state it indicates this to the MAC device by deasserting RX_ER and returning to a normal inter-frame state.

While the PHY device is indicating low power idle it may halt the RX_CLK at any time more than 9 clock cycles after the start of the low power idle state as shown in [figure 22–9a] if and only if the RX_CLK_stoppable bit is asserted [45.2.3.1.3a].

Figure 22–9a shows the behavior of RX_ER, RX_DV and RXD<3:0> during low power idle transitions.

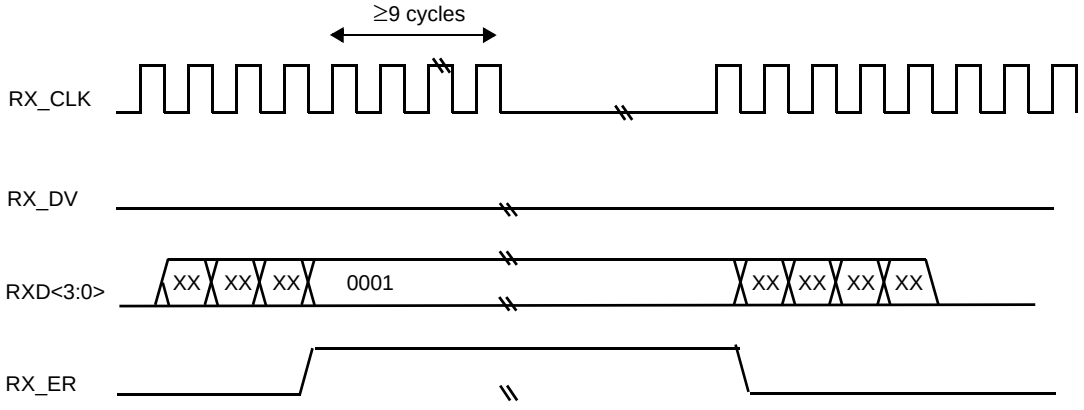


Figure 22–9a—Low power idle transitions (receive)

Insert a new section, 22.7a for Low Power Idle assertion and detection:

22.7a Low Power Idle Assertion and Detection

Low Power Idle signaling allows the MAC device to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the MAC device to understand that the link partner has sent such an indication.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the MII signals as shown in Figure 22–20a. The definition of TX_EN, TX_ER and TXD<3:0> is derived from

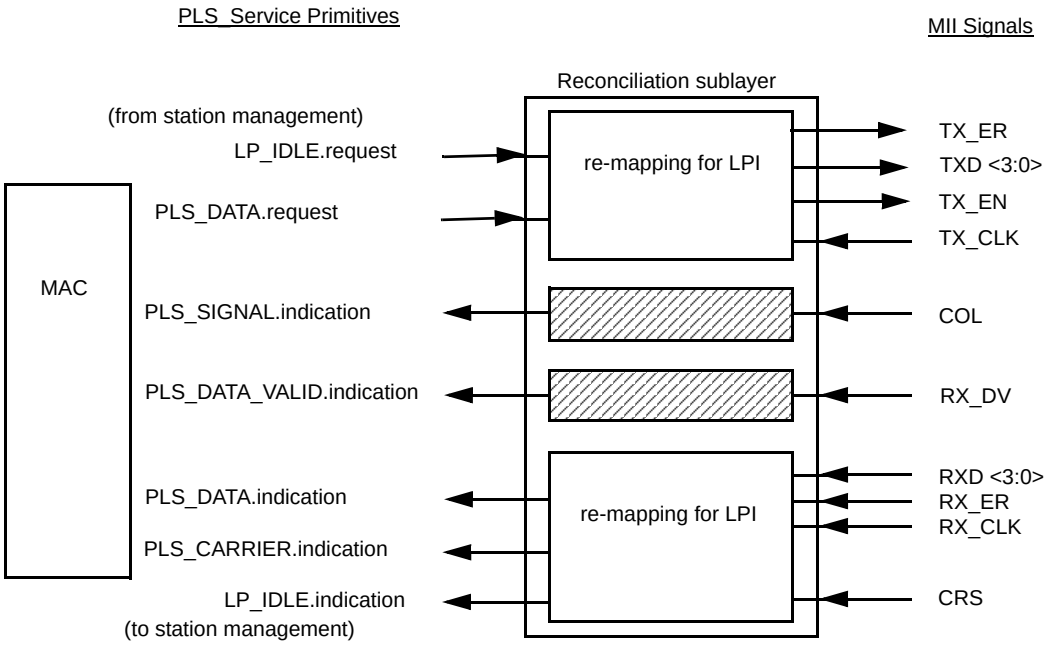


Figure 22–20a—LPI assertion and detection mechanism

the state of PLS_DATA.request (22.2.1.1), except when it is overridden by an assertion of LP_IDLE.request. Similarly, RX_ER and RXD<3:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected and CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire.

22.7a.1 LPI messages

LP_IDLE.indication

A primitive that indicates to the station management entity that the PHY has detected the assertion or deassertion of low power idle from the link partner.

Values: DEASSERT: The link partner is operating with normal idle behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request

A primitive that is used by the station management entity to signal that it wishes to assert or deassert low power idle.

Values: DEASSERT: The system wishes to operate with normal idle behavior (default).
ASSERT: The system wishes to assert LPI and signal this to the link partner.

22.7a.2 Transmit LPI state machine

The operation of low power idle in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by Resolved Transmit Tw defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state machine and the rules mapping CARRIER_SENSE.indication defined in 22.2.1.3. The implementation shall conform to the behavior described by the transmit LPI state machine shown in Figure 22–21.

22.7a.2.1 Conventions

The notation used in the state diagram follows the conventions of 21.5. The notation ++ after a counter indicates it is to be incremented.

22.7a.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

reset

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values: FALSE: The device is completely powered and has not been reset (default).
TRUE: The device has not been completely powered or has been reset.

li_timer

A timer that counts, in microseconds, the time expired since the assertion of LPI. The terminal count of the timer is the value of the minimim LPI assertion time for the PHY in use. Signal li_timer_done is asserted on reaching its terminal count. If the minimum LPI assertion time is zero for the PHY in use then li_timer_done is always true.

tw_timer

A timer that counts, in microseconds, the time expired since the deassertion of LPI. The terminal count of the timer is the value of the Resolved Transmit Tw as defined in 78.4.2.3. Signal tw_timer_done is asserted on reaching its terminal count.

22.7a.2.3 State Diagram

22.7a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least Resolved Transmit Tw time, in microseconds, after it requests the deassertion of LPI. Buffering and queue management should be designed to accommodate this.

22.7a.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the MII. The receive system should be aware that data frames may arrive at the MII following the deassertion of LP_IDLE.indicate with a delay corresponding to the link partner's Resolved Transmit Tw (as specified in 78.4.2.3) time, in microseconds.

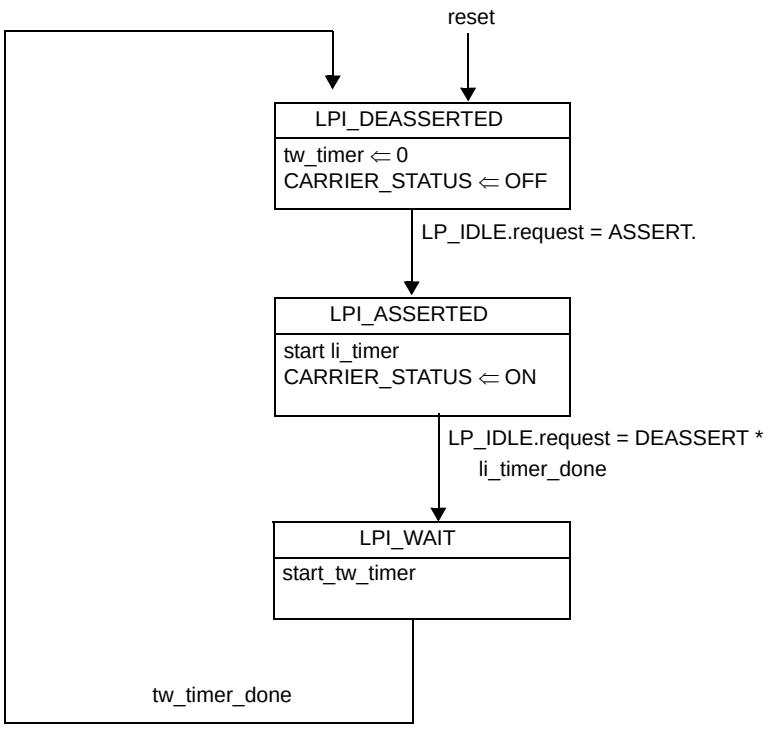


Figure 22–21—Transmit LPI State Diagram

22.7 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[1]

[Editor's note (to be removed prior to publication) - changes and additions to PICS for LPI]

Add the following row into table 22.7.2.3:

22.7.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*LPI	Implementation of LPI	22.7a	O		

Add new subclause 22.7.3.4a:

22.7.3.4a Low power idle functions

Item	Feature	Subclause	Status	Support	Value/Comment
L1	Transitions to LPI_ASSERTED and LPI_DEASSERTED reflected in CARRIER_STATUS	22.2.1.3	LPI:M		
L2	Assertion of LPI as defined in Table 22–1	22.2.2.4	LPI:M		
L3	RX_CLK stoppable during LPI	22.2.2.9a	LPI:O		At least 9 cycles after LPI assertion
L4	RS shall continue to indicate IDLE on PLS_DATA.indicate	22.7a.3.1	LPI:M		
L5	Behavior matches the transmit LPI state machine	22.7a.2.3	LPI:M		

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 24

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: To be removed prior to final publication.

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:
Draft 0.1, July 2008Initial draft for IEEE P802.3az Task Force review.
Draft 0.9, August 2008Initial draft for IEEE P802.3az Task Force review.

24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.1.1 Scope

Insert a new paragraph as shown below after the second paragraph:

The 100BASE-X may support the capability of Energy Efficient Ethernet as described in Clause 78. When this capability is implemented and utilized, the PHY enters the low power idle mode during periods of low link utilization. Energy is conserved by deactivating some or all functional blocks. The transmit and receive paths can enter and exit low power states independently. The only 100BASE-X PHY that supports this capability is 100BASE-TX.

24.1.2 Objectives

Insert item (g) as the last item in the objective list in 24.1.2:

The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC in the half duplex and the full duplex modes of operation.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 UTP, 150 Ω STP or optical fiber, compliant with ISO/IEC 11801.
e) Allow for a nominal network extent of 200–400 m, including
    1) Unshielded twisted-pair links of 100 m;
    2) Two repeater networks of approximately 200 m span;
    3) One repeater network of approximately 300 m span (using fiber); and
    4) DTE/DTE links of approximately 400 m (half duplex mode using fiber) and 2 km (full duplex mode using multimode fiber).
f) Preserve full duplex behavior of underlying PMD channels.
g) Support Energy Efficient Ethernet with the optional function of Low Power Idle as described in Clause 78 for the embodiment of 100BASE-TX.

24.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Media Independent Interface (MII) that provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations (e.g., 100BASE-X and 100BASE-T4). 100BASE-X, as other 100BASE-T PHYs, is modeled as providing services to the MII. This is similar to the use of an AUI interface.

Insert item (e) after item (d) in the list of services required as shown below:

The 100BASE-X PCS realizes all services required by the MII, including:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B);
b) Generating Carrier Sense and Collision Detect indications;
c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA~~, and~~;
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA~~.~~,and
e) Optionally, interpreting and generating MII opcodes to enable or disable the low power idle mode.

24.1.4.2 Physical Medium Attachment (PMA) sublayer

Insert item (e) after item (d) in the list of PMA functions as shown below and renumber the items:

The PMA provides a medium-independent means for the PCS and other bit-oriented clients (e.g., repeaters) to support the use of a range of physical media. The 100BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD;
b) Generating a control signal indicating the availability of the PMD to a PCS or other client, also synchronizing with Auto-Negotiation when implemented;
c) Optionally, generating indications of activity (carrier) and carrier errors from the underlying PMD;
d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication; ~~and~~
e) Optionally, receiving and processing low power idle state control signals from the PCS; and
f) Recovery of clock from the NRZI data supplied by the PMD.

24.1.6 Functional block diagram

Replace Figure 24–4 with the new Figure 24–4

Figure 24–4 provides a functional block diagram of the 100BASE-X PHY. Signals or functions shown with dashed lines are optional.

24.2 Physical Coding Sublayer (PCS)

24.2.2 Functional requirements

Insert two new paragraphs as shown after the third paragraph of 24.2.2 Functional requirements:

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates RXD <3:0>, RX_DV and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

The Receive process may support the low power idle by deactivating all or part of receive functional blocks of PCS, PMA, and PMD to conserve energy during low link utilization upon receiving proper code-groups via rx_code bits from the link partner as described in 24.2.2.1.6, and generate proper commands (RX_LP_IDLE) sending through MII as described in 22.2.2.7. By interacting with Link Monitor of PMA, a link failure detection mechanism is included to differentiate two conditions of link failure due to signal off: the loss of channel signal during normal operation and the loss of refresh signal in low power idle.

The Transmit process generates continuous code-groups based upon the TXD <3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA.request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Transmit process may support the low power idle by deactivating all or part of transmit functional blocks of PCS, PMA, and PMD to conserve energy for low link utilization upon receiving the proper command (TX_LP_IDLE) from MII as described in 22.2.2.4. In this mode, the Transmit process is periodically activated to transmit refresh signal through tx_code_bits in order to allow remote receiver to keep track of the long term variation of channel characteristics and the clock drift between link partners.

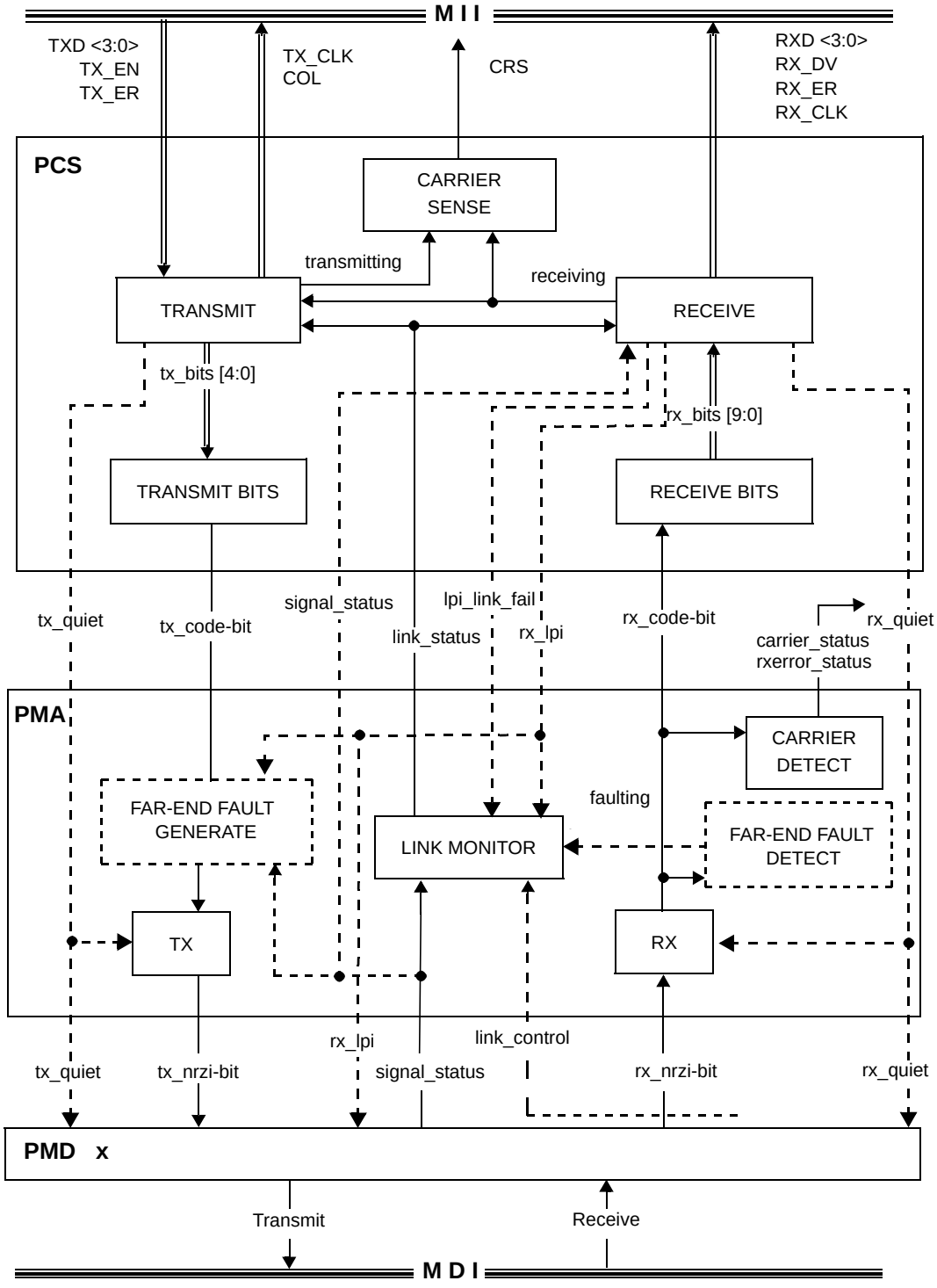


Figure 24–4—Functional block diagram

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

24.2.2.1 Code-groups

Change 24.2.2.1 as shown below:

The PCS maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme. A code-group is a consecutive sequence of five code-bits interpreted and mapped by the PCS. Implicit in the definition of a code-group is an establishment of code-group boundaries by an alignment function within the PCS Receive process. It is important to note that, with the sole exception of the SSD, which is used to achieve alignment, code-groups are undetectable and have no meaning outside the 100BASE-X physical protocol data unit, called a "stream."

The coding method used, derived from ISO/IEC 9314-1, provides

a) Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups;
b) Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel as provided by FDDI PMDs; and
c) Sufficient transition density to facilitate clock recovery (when not scrambled).

Table 24–1 specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories, as shown.

For clarity in the remainder of this clause, code-group names are shown between /slashes/. Code-group sequences are shown in succession, e.g., /1/2/....

The indicated code-group mapping is identical to ISO/IEC 9314-1:1989, with ~~four~~five exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.
e) The /P/ code-group is used to start a low power state and to refresh the link during the LPI mode.

24.2.2.1.1 Data code-groups

A Data code-group conveys one nibble of arbitrary data between the MII and the PCS. The sequence of Data code-groups is arbitrary, where any Data code-group can be followed by any other Data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of Data code-groups depends on proper receipt of the Start-of-Stream Delimiter sequence, as defined in Table 24–1.

Change Table 24–1 as shown by inserting a row redefining the 00000 code group to be the SLEEP code group right after the row defining the 11111 code group. Delete the row defining the 00000 code group as an invalid code group.

Insert 24.2.2.1.6 to define the sleep code-group after 24.2.2.1.5

Table 24–1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
	0 0 0 0 0	P	undefined	SLEEP; Low Power Idle code
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

24.2.2.1.6 SLEEP code-groups (/P/)

The SLEEP code-group (/P/) is used to delineate the boundary of a low power idle sequence and to deliver a refresh signal to maintain clock synchronization and verify the link status. The SLEEP code-groups are emitted from, and interpreted by, the PCS.

Insert 24.2.2.5 after 24.2.2.4 Mapping between MII and PMA as shown below:

24.2.2.5 Low Power Idle

Editor's Notes: **To be removed prior the final publication.**

In Table 24-2, all timing parameters are modified by adding the range of value to cover the implementation variations. This technical change is added in D1.1.

The 100BASE-X PCS accepts LPI commands from the Reconciliation Sublayer and MII (TX_LP_IDLE, Table 22–1) to start low power transmit state. The PCS returns to the normal state when it detects the termination of the LPI command. Upon receiving LPI command, it replaces the continuous IDLE code-groups with a signal stream comprising several intermediate line states as described below and shown in Table 24–2. The timing parameter of each line state is defined with a fixed value within a specified range.

Table 24–2—Timing Parameters and Signals of Low Power Idle line state

Line State	Symbol	Timing Parameters (TX)	Timing Parameters (RX)	Line Signal
Sleep	Ts	100 us - 120 us	100 us - 120 us	4b5b code-group /P/
Quiet	Tq	20 ms - 22 ms	24 ms - 26 ms	Differential DC zero volt
Wake	Tw	30 us - 36 us	30 us - 36 us	4b5b code-group /I/
Refresh	Tr	100 us - 120 us	Not Applicable	4b5b code-group /P/

a) *Sleep state.* The start of a LPI state is indicated by a series of SLEEP code-groups for fixed amount of time denoted by Ts as defined inTable 24–2. Upon reception, SLEEP is interpreted by the PCS as a request to transit to low power idle mode.

b) *Quiet state.* Following SLEEP code-groups, the PCS sends a control signal to indicate the start of the Quiet state, which is consuming less power than the normal state. During the Quiet state, the PMD may cease the transmission by turning the output to a low power steady level (DC 0 volt). This state is not allowed to last longer than a fixed amount of time Tq before a Refresh or Wake state must present.

c) *Wake state.* At the end of the LPI state, the stream is terminated by a series of IDLE code-groups for default or negotiated amount of time denoted by Tw. Upon reception, IDLE is triggering the wakeup process of PMD and is interpreted by the PCS as a request to exit the low power idle mode.

d) *Refresh state.* In low power idle mode of 100BASE-X, the Refresh state is similar to a concatenation of a Wake state followed by a Sleep state except that it uses the same code-group as a Sleep state. Therefore, the duration of the Refresh state Tr on the receiver side is limited by the sum of Tw and Ts.

Upon successfully receiving SLEEP code-groups, the 100BASE-X PCS enters low power receive state. It then sends LPI commands to the Reconciliation Sublayer and MII (RX_LP_IDLE, Table 22–2) to notify the upper layer the change of operation mode. It returns to normal mode and ceases the transmission of LPI commands on MII if consecutive IDLE code-groups are received. The Refresh signal is used to maintain some internal parameters of the receiver, such as those necessary for timing recovery and signal equalization. It shares the SLEEP code-groups with Sleep signal and does not cause the PCS to exit the low power receive state.

24.2.3 State variables

24.2.3.1 Constants

Insert two new Constants in alphabetical order in the list below:

SLEEP

The SLEEP code-group (/P/) used for Low Power Idle state delineator, as specified in 24.2.2.1.

TX_LP_IDLE

A value of transmit nibble-wide Data signals (TXD) combining with proper value of TX_EN and TX_ER on the MII used to communicate the status or request of low power transmit state, as specified in 24.2.2.

RX_LP_IDLE

A value of receive nibble-wide Data signals (RXD) combining with proper value of RX_DV and RX_ER on the MII used to communicate the status or request of low power receive state, as specified in 24.2.2.

24.2.3.2 Variables

Insert new variable in the variables list of 24.2.3.2 in alphabetic order as shown below:

lpi_link_fail

A Boolean set by the Receive process to control the transition to a Link Down state during the low power receive state. Used by the Link Monitor process of PMA as communicated through the PMA_LPILINKFAIL.request primitive.

Values: TRUE; Local receiver has detected a link failure status during low power idle state
FALSE; Local receiver is functioning normally during low power idle state

rx_lpi

A Boolean set by the Receive process to indicate the low power receive state. Used by the Link Monitor process of PMA as communicated through the PMA_RXLPI.request primitive. This parameter is used to alter the signal detection time as shown in Table 25–3. It can also be used to halt the clock RXC of MII as described in Clause 22.

Values: TRUE; Local receiver is in low power receive state
FALSE; Local receiver is in normal state

rx_quiet

A Boolean set by the Receive process to indicate the quiet line state of low power receive state as communicated through PMD_RXQUIET.request primitive. Also may be used to control the power saving function of various receiver blocks (PCS, PMA, and PMD).

Values: TRUE; The local receiver is in Quiet state
FALSE; The local receiver is not in Quiet state

tx_quiet

A Boolean set by the Transmit process to indicate the quiet line state of low power transmit state as communicated through PMD_TXQUIET.request primitive. Also may be used to control the power saving function of various transmit blocks (PCS, PMA, and PMD).

Values: TRUE; The local transmitter is in Quiet state
FALSE; The local transmitter is not in Quiet state

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

24.2.3.4 Timers

Insert new timers in the timer list in 24.2.3.4 as shown below:

lpi_rx_ti_timer

In low power receive state, the receiver can move to Idle state when it receives consecutive IDLE symbols. In order to distinguish the intended IDLE symbols sent by link partner from ones falsely decoded during the transition from Sleep state to Quiet state before the signal status is deasserted, this receiver timer counts the minimum duration of received IDLE symbols. During this period of time, the receiver stays in an intermediate state. The timer shall have a period between 1.0 us to 1.2 us.

lpi_rx_tq_timer

In low power receive state, this receiver timer counts the maximum duration PHY stays in Quiet state before it expects a Refresh signal. If the PHY fails to receive a valid Refresh signal or Wake signal before this timer expires, the receiver shall assume a link failure when the timer has expired. The timer shall have a period between 24 ms to 26 ms.

lpi_rx_ts_timer

In low power receive state, this receiver timer counts the minimum duration PHY stays in Sleep state before going into Quiet state. The timer shall have a period between 100 us to 120 us.

lpi_rx_tw_timer

In low power receive state, the receiver in Quiet state is woken up by the receiving signal. This receiver timer counts the maximum duration for PHY to identify if valid SLEEP symbols for Refresh state or valid IDLES for Wake state have been properly received. If none of the SLEEP or IDLE symbols are received when the timer is expired, the receiver shall assume a link failure. The timer shall have a period between 30 us to 36 us.

lpi_tx_tq_timer

In low power transmit state, this transmitter timer counts the duration PHY remains in Quiet state before it must wake for refresh signal. The timer shall have a period between 20 ms to 22 ms.

lpi_tx_ts_timer

In low power transmit state, this transmitter timer counts the duration PHY is sending continuous SLEEP symbols in Sleep state before going into Quiet state. The timer shall have a period between 100 us to 120 us.

lpi_tx_tr_timer

In low power transmit state, the transmitter is woken up to send Refresh signal periodically. This timer counts the duration for PHY in Refresh state to continuously send Sleep signal to refresh the receiver for clock synchronization and necessary coefficients update. The timer shall have a period

between 100 us to 120 us.

24.2.4.2 Transmit

Replace the transmit state diagram (Figure 24–8) with the new Figure 24–8 which now includes the state transitions for energy efficient operation:.

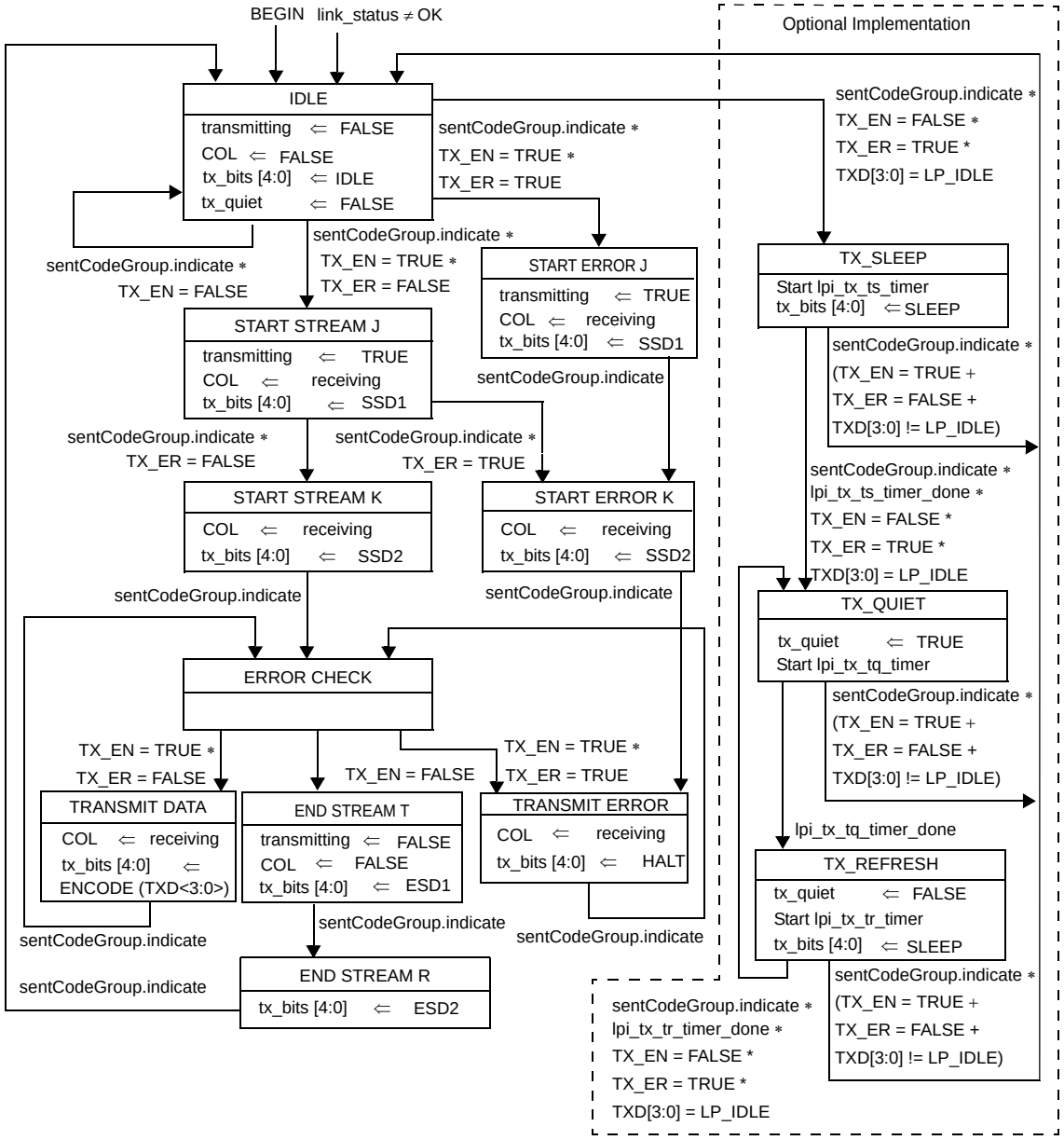


Figure 24–8—Transmit state diagram

24.2.4.4 Receive

Replace the receive state diagram (Figure 24–11b) with the new Figure 24–11b and which now includes the state transitions for energy efficient operation.

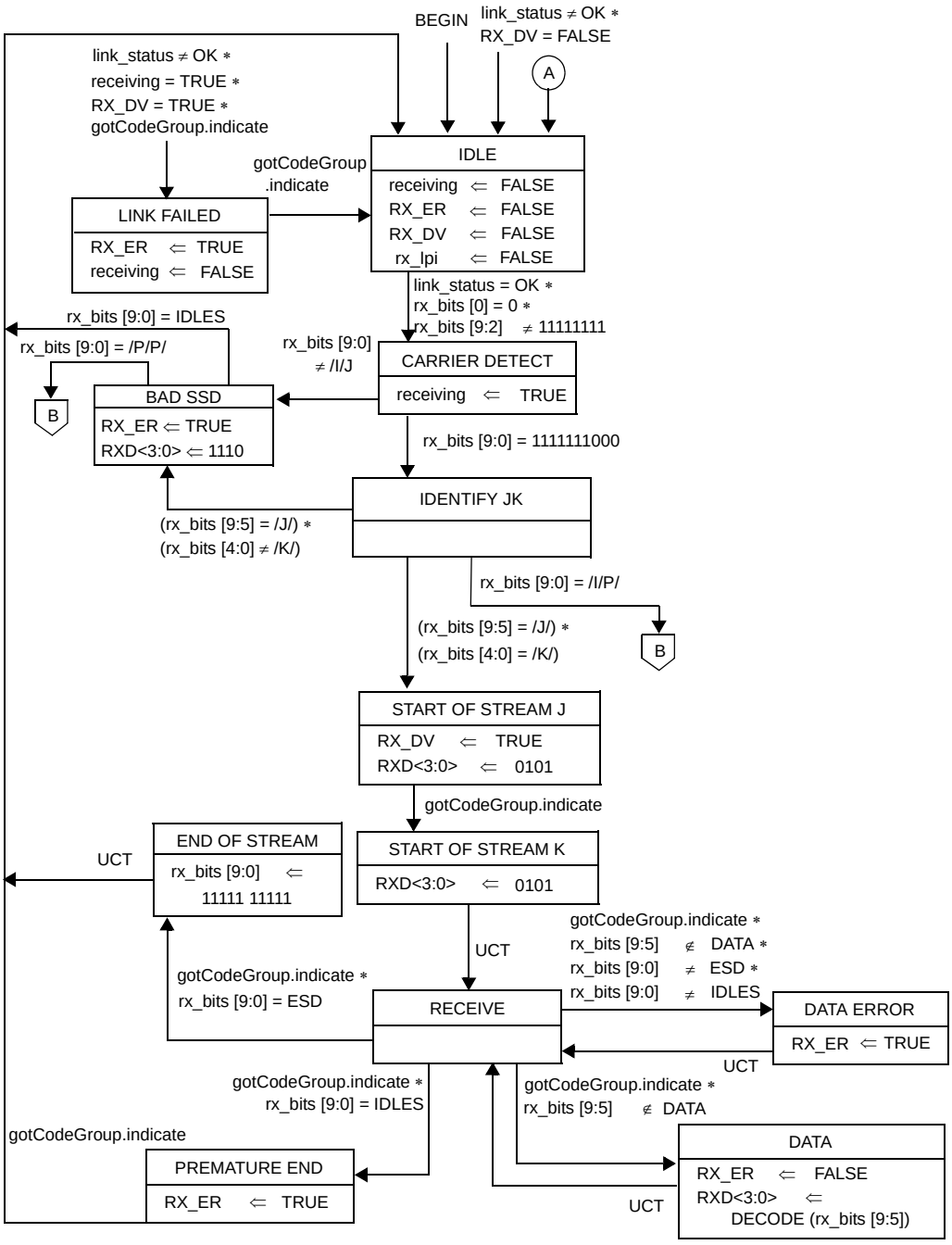


Figure 24–11a—Receive state diagram, part a

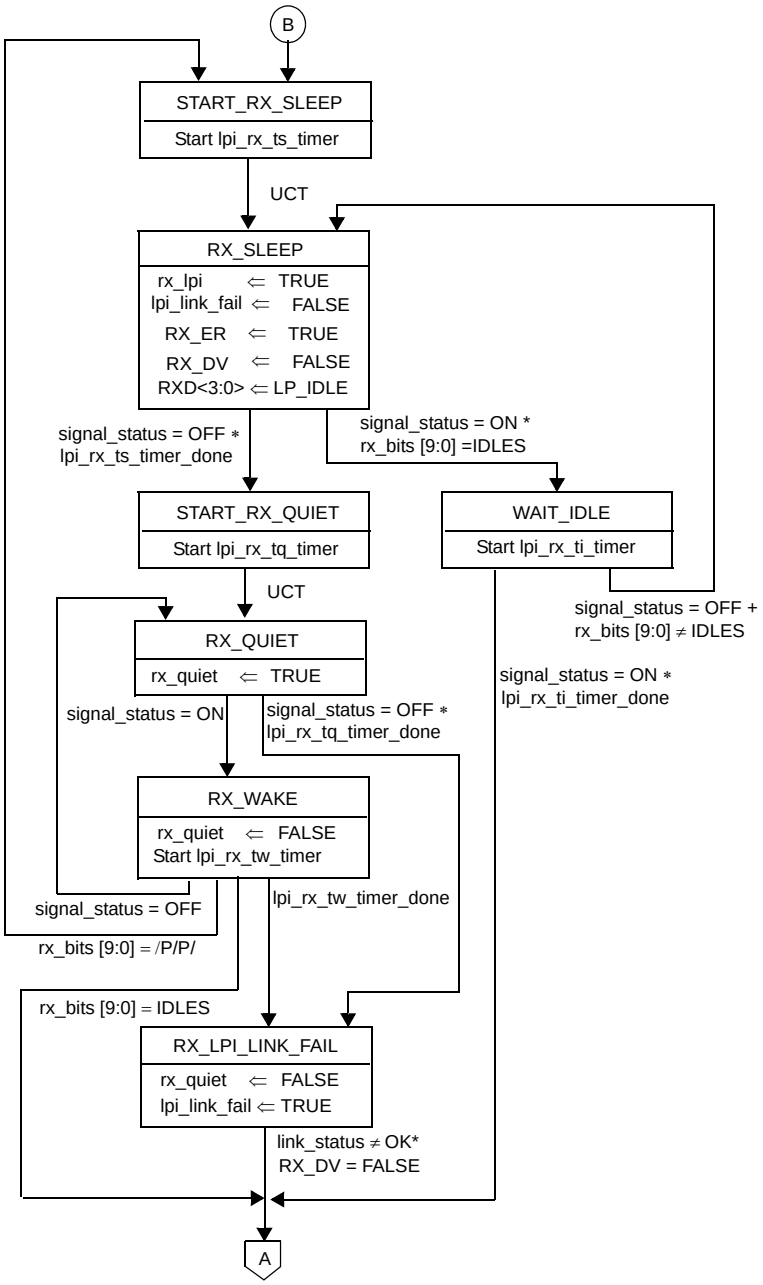


Figure 24–11b—Receive state diagram, part b (optional)

24.3 Physical Medium Attachment (PMA) sublayer

24.3.1 Service Interface

Insert the two new primitive as shown below at the end of the third paragraph:

PMA_LPILINKFAIL.request

PMA_RXLPI.request

Insert the following new primitive definitions following existing primitives as shown below at the end of clause 24.3.1.7.3:

24.3.1.8 PMA_LPILINKFAIL.request

This primitive is generated by the Receive Process of PCS, when Low Power Idle mode is implemented, to control one of link failure conditions of the Link Monitor of the PMA. See Clause 24.2.4.4 and Figure 24–11b. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMA behaves as if lpi_link_fail = FALSE.

24.3.1.8.1 Semantics of the service primitive

PMA_LPILINKFAIL.request (lpi_link_fail)

The lpi_link_fail parameter takes on one of two values: TRUE or FALSE. The value of TRUE during low power receive state sets link_status of Link Monitor to FAIL. See Clause 24.3.4.4 and Figure 24–15.

24.3.1.8.2 When generated

The PCS generates this primitive to indicate a link failure condition caused by the loss of Refresh signal during low power receive state.

24.3.1.8.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in Clause 24.3.4.4.

24.3.1.9 PMA_RXLPI.request

This primitive is generated by the Receive Process of PCS, when LPI mode is implemented, to indicate that the receiver is in low power state. See Clause 24.2.4.4 and Figure 24–11b. When LPI mode is not implemented, the primitive is never invoked and the PMA behaves as if rx_lpi = FALSE.

24.3.1.9.1 Semantics of the service primitive

PMA_RXLPI.request (rx_lpi)

The rx_lpi parameter takes on one of two values: TRUE or FALSE.

24.3.1.9.2 When generated

The PCS generates this primitive to indicate the low power receive state.

24.3.1.9.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4. Other use of receipt of this primitive by the client is unspecified by the PMA sublayer.

Change the sixth paragraph of 24.3.2.1 Far-End fault as shown below:

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF during normal operation) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status. Far-End fault is not generated during the low power idle mode.

24.3.3.2 Variables

Insert new variable in the variables list in 24.3.3.2 in alphabetic order as shown below:

lpi_link_fail

The lpi_link_fail parameter is communicated by the PMA_LPILINK.request primitive. When low power idle mode is executed, this variable is generated by the Receive process of PCS to control the transition to a Link Down state during the low power receive state.

Values: TRUE; Local receiver has detected a link failure status during low power idle state
FALSE; Local receiver is functioning normal during low power idle state

rx_lpi

The rx_lpi parameter is communicated by the PMA_RXLPI.request primitive. This variable is from the Receive process of PCS to control the transition to indicate the low power receive state.

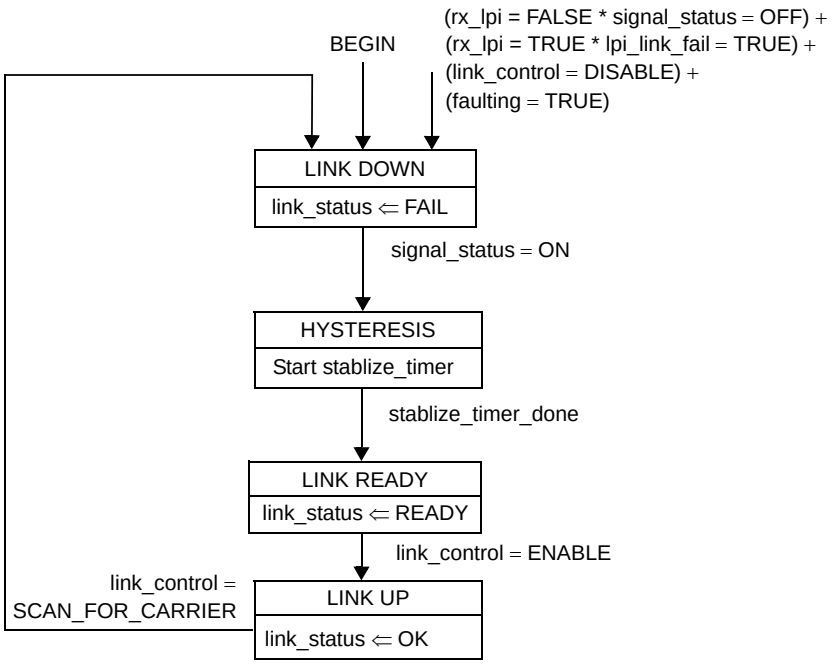
Values: TRUE; Local receiver is in low power receive state
FALSE; Local receiver is in normal Active state

24.3.4.4 Link Monitor

Change the second paragraph of 24.3.4.4 Link Monitor as shown below:

The Link Monitor process monitors signal_status, setting link_status to FAIL whenever signal_status is OFF during normal operation or when Auto-Negotiation sets link_control to DISABLE. If the low power idle mode is implemented and the receiver is in low power state the assertion of lpi_link_fail sets the link_status to FAIL and eventually exits the low power idle mode. The link is deemed to be reliably operating when signal_status has been continuously ON for a period of time. This period is implementation dependent but not less than 330 µs or greater than 1000 µs. If so qualified, Link Monitor sets link_status to READY in order to synchronize with Auto-Negotiation, when implemented. Auto-Negotiation permits full operation by setting link_control to ENABLE. When Auto-Negotiation is not implemented, Link Monitor operates with link_control always set to ENABLE.

Replace the Link Monitor diagram (Figure 24–15) with the new Figure 24–15 which now takes energy efficient operation into consideration.



NOTE—The variables link_control and link_status are designated as link_control_[TX] and link_status_[TX], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 24–15—Link Monitor State Diagram

24.3.4.5 Far-End Fault Generation

Change the first paragraph of 24.3.4.5 Far-End Fault Generation as shown below:

Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON. When signal_status=OFF and not in the low power receive state, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted.

Replace the Far-End fault diagram (Figure 24–16) with the new Figure 24–16 which now takes energy efficient operation into consideration.

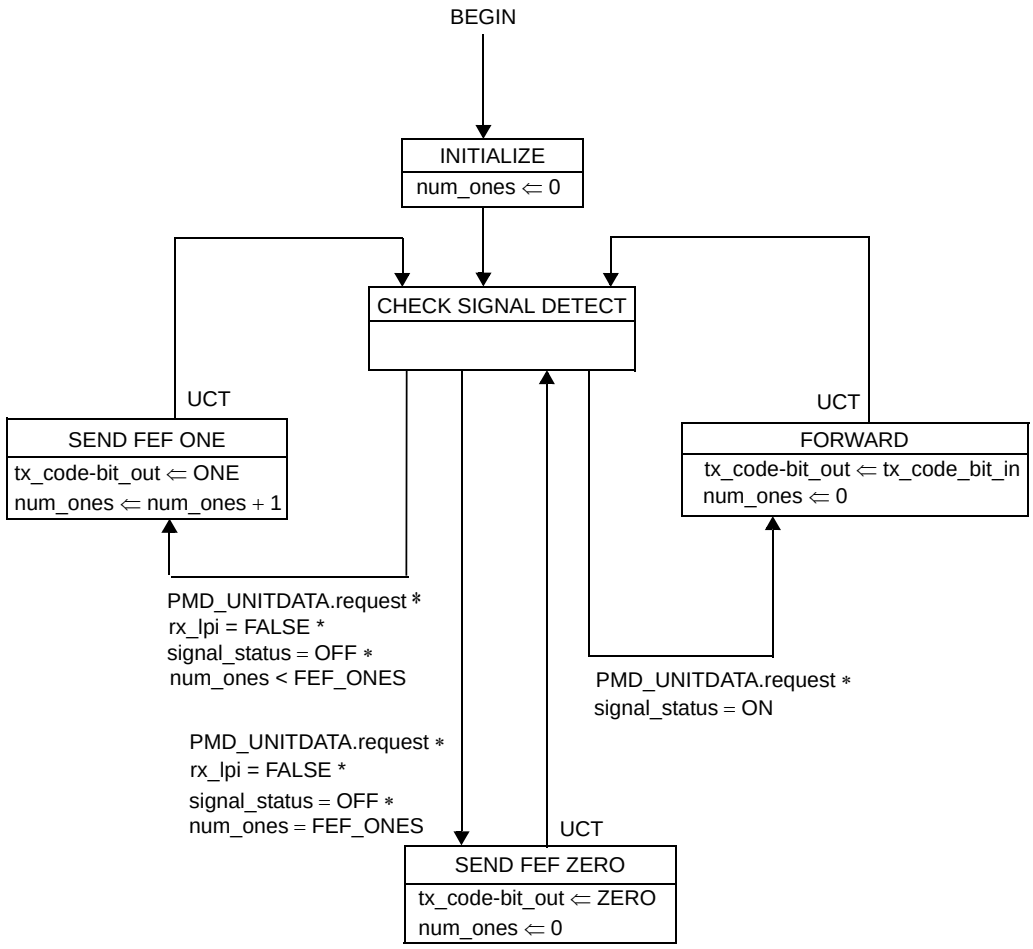


Figure 24–16—Far-End Fault Generation state diagram

24.4 Physical Medium Dependent (PMD) sublayer

24.4.1 PMD Service Interface

Change the first two paragraph of subclause 24.4.1 as shown by inserting a new exception item.

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3:1990 and ANSI X3.263-1995, with ~~two~~ three exceptions:

a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3:1990 and ANSI X3.263-1995.
b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.
c) 100BASE-X supports Low Power Idle mode if the Energy Efficient Ethernet is implemented and low power idle mode is utilized.

Insert the two new primitive as shown below at the end of subclause 24.4.1:

PMD_RXQUIET.request

PMD_TXQUIET.request

Insert the following new primitive definitions as shown below at the end of clause 24.4.1.3.3:

24.4.1.4 PMD_RXQUIET.request

This primitive is generated by the Receive Process of PCS, when low power idle mode is implemented, to indicate that the receiver is in low power receive state and the line is in Quiet state. See Clause 24.2.4.4 and Figure 24–11b. When low power idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

24.4.1.4.1 Semantics of the service primitive

PMD_RXQUIET.request(rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

24.4.1.4.2 When generated

The PCS generates this primitive to indicate the Quiet line of low power receive state.

24.4.1.4.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in Clause 25.4.11.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.5 PMD_TXQUIET.request

This primitive is generated by the Transmit Process of PCS, when low power idle mode is implemented, to indicate that the transmitter is in low power transmit state and the line is in Quiet state. See Clause 24.2.4.2 and 4Figure 24–8. When low power idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

24.4.1.5.1 Semantics of the service primitive

PMD_TXQUIETrequest(tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

24.4.1.5.2 When generated

The PCS generates this primitive to indicate the Quiet line of low power transmit state.

24.4.1.5.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in Clause 25.4.11.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.8 Protocol implementation conformance statement (PICS) proforma for Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X[1]

24.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

24.8.2 Identification

24.8.2.2 Protocol summary

Editor's Notes: *To be removed prior to publication.*
Check if EEE 100BASE-TX will require changes to the PICS relating to identification of protocol support or labeling.

Identification of protocol standard	IEEE Std 802.3-2005, Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2005.)	

Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Editor's Notes: *To be removed prior to publication.*

changes and additions to PICS for LPI.

24.8.2.3 Major capabilities/options

Add the following row into table of Clause 24.8.2.3:

Item	Feature	Subclause	Status	Support	Value/Comment
*LPI	Supports LPI function	24.2.2.5	O		

24.8.3 PICS proforma tables for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

Add new subclause 24.8.3.5:

24.8.3.5 LPI timers

Item	Feature	Subclause	Status	Support	Value/Comment
LT1	lpi_rx_ti_timer	24.2.3.4	LPI:M		Expired between 1.0-1.2 us after being started
LT2	lpi_rx_tq_timer	24.2.3.4	LPI:M		Expired between 24-26 ms after being started
LT3	lpi_rx_ts_timer	24.2.3.4	LPI:M		Expired between 100-120 us after being started
LT4	lpi_rx_tw_timer	24.2.3.4	LPI:M		Expired between 30-36 us after being started
LT5	lpi_tx_tq_timer	24.2.3.4	LPI:M		Expired between 20-22 ms after being started
LT6	lpi_tx_ts_timer	24.2.3.4	LPI:M		Expired between 100-120 us after being started
LT7	lpi_tx_tr_timer	24.2.3.4	LPI:M		Expired between 100-120 us after being started

Revisions to IEEE Std 802.3-2008, Clause 25

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: To be removed prior to final publication.

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	**Initial draft for IEEE P802.3az Task Force review.**
Draft 0.9, August 2008	**Initial draft for IEEE P802.3az Task Force review.**

25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.3 General exceptions

Insert item (e) following item (d) and change the original item (e) to item (f) as shown below:

Editor's Note: To be removed prior to final publication.

The primitive PMA_RXLPI.request (rx_lpi) generated by PCS is intended to pass to PMD sublayer and is used to control the duration of Signal_Detect assertion and deassertion time. The modifications will be furnished when the Editor is submitting comments to D1.0. It includes the change of Table 25-1, subclause 25.4.11.3, and 25.4.11.4.

Editor's Note: To be removed prior to final publication.

In item d), "...(UTP) of TP-PMD 11.1 are replaced by those specified in 25.4.7", while what it refers to (subclause 25.4.7) seems incorrect, it is actually referring to Draft rev 9 of 802.3ay instead of IEEE Std 802.3-2005 of which the TP-PMD cable plant is in clause 25.4.6.

d) The cable plant specifications for untwisted shielded pair (UTP) of TP-PMD 11.1 are replaced by those specified in 25.4.7.

e) 100BASE-TX supports optional capability of Energy Efficient Ethernet as described in Clause 78. The way to implement this feature is through the Low Power Idle. Two new service primitives PMD_RXQUIET.request(rx_quiet) (see 24.4.1.4) and PMD_TXQUIET.request(tx_quiet) (see 24.4.1.5) are generated to pass the energy saving requests from the PCS.

f) There are minor terminology differences between this standard and TP-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 25–1

Change Table 25–1 as shown by inserting two rows defining PMD.RXQUIET.request and PMD.TXQUIET.request at the end of table:

Table 25–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-TX
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 3062 code-groups
PHY (or PHY-2)	PMA; i.e., PMD client

Table 25–1—Interpretation of general FDDI terms and concepts *(continued)*

FDDI term or concept	Interpretation for 100BASE-TX
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indication (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indication (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request(Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group
<no comparable entity>	PMD_RXQUIET.request (rx_quiet)
<no comparable entity>	PMD_TXQUIET.request (tx_quiet)
<no comparable entity>	PMA_RXLPI.request (rx_lpi)

25.4 Specific requirements and exceptions

Insert a new subclause 25.4.11 at the end of Clause 25.4 to include the optional capability of Energy Efficient Ethernet as shown below:

Editors' Notes: To be removed prior to final publication.

Editor tries to make this subclause effective only if the Energy Efficient Ethernet capability is implemented. Otherwise, the original TP-PMD specification is still applicable to legacy 100BASE-TX phy.

25.4.11 Energy Efficient Ethernet capability

TP-PMD does not have an option to support Energy Efficient Ethernet. In order to add this capability to existing TP-PMD specification, TP-PMD 7.1.2, 7.2.2, 10.1.2, 10.1.3, and Table 4 are modified to incorporate the Low Power Idle function. This clause takes effect only if the option of low power idle is implemented.

25.4.11.1 Change to TP-PMD 7.1.2 "Encoder"

The Encoder receives the scrambled NRZ data stream from the Scrambler and encodes the stream into MLT3 code for presentation to the Driver. MLT3 coding is similar to NRZI coding, but three instead of two levels are transmitted. The Encoder can be deactivated during the low power transmit state.

The PMD in low power idle mode shall implement the Encoder as depicted in Figure 25–1.

25.4.11.1.1 State Variables

25.4.11.1.1.1 Variables

encoder_input
Indicates the value of each scrambled NRZ bit to be encoded.

Values: ZERO; the nrz bit from Scrambler process (TP-PMD 7.1.1) has a logical value 0
ONE; the nrz bit from Scrambler process (TP-PMD 7.1.1) has a logical value 1

encoder_output
Indicates the value from the encoder for each MLT-3 encoded bit.

Values: POSITIVE_VOLTAGE; the output indicates a positive value of voltage to TP-TMD Driver (TP-PMD 7.1.3)
ZERO_VOLTAGE; the output indicates a zero value of voltage to TP-TMD Driver (TP-PMD 7.1.3)
NEGATIVE_VOLTAGE; the output indicates a negative value of voltage to TP-TMD Driver (TP-PMD 7.1.3)

link_status
The link_status parameter as communicated by the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact
READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

tx_quiet
The tx_quiet parameter as communicated by the PMD_TXQUIET.request (tx_quiet) primitive. This variable is from the Transmit process of PCS to control the power saving function of local transmitter. It is also used to set the initial state of Encoder state diagram.

Values: TRUE; The local transmitter is in Quiet state
FALSE; The local transmitter is not in Quiet state

le_flag
A Boolean set by the Encoder process to indicate whether the last non-zero value of encoder_output was POSITIVE_VOLTAGE. The flag le_flag is set upon entry to PLUS_V state and is cleared upon entry to MINUS_V state.

Values: ONE; The encoder is in PLUS_V state
ZERO; The encoder is in MINUS_V state

25.4.11.1.1.2 Messages

gotNRZbit.indicate

A signal sent to the Encoder process by the Scrambler process after a scrambled nrz text bit has been generated using recursive linear function by the scrambler from plaintext bit stream and is

ready to transmit.

Insert Figure 25-1 as depicted in Figure 25-1 at the end of subclause 25.4.11.1:

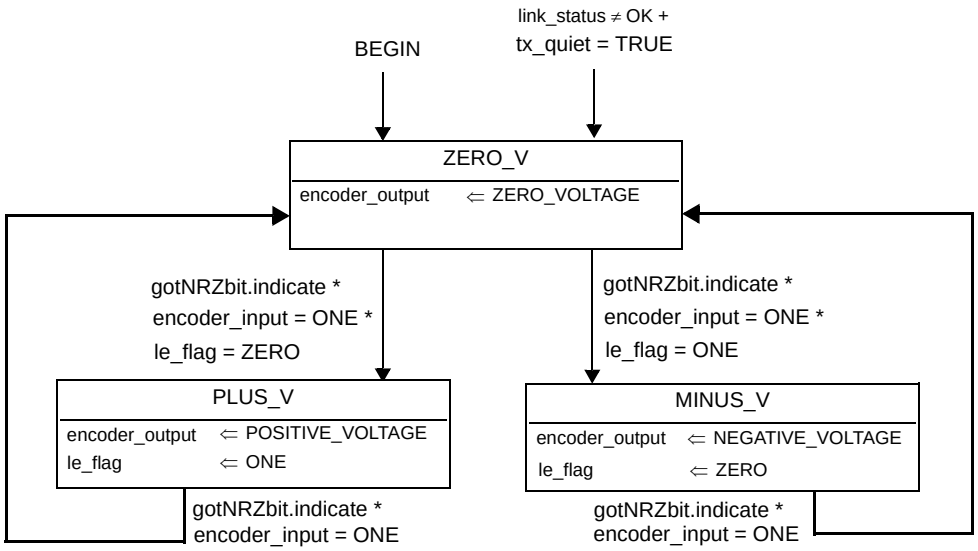


Figure 25–1—Encoder state diagram

25.4.11.2 Change to TP-PMD 7.2.2 "Decoder"

The Decoder receives the MLT3 encoded bit stream from the Receiver, and decodes it into a NRZ encoded bit stream for presentation to the Descrambler. The Decoder can be deactivated during the low power receive state.

The PMD in low power idle mode shall implement the Decoder as depicted in Figure 25–2.

25.4.11.2.1 State Variables

25.4.11.2.1.1 Variables

decoder_input
: Indicates the value of the MLT-3 encoded bit from the Receiver.

  Values: ZERO; the MLT3 bit from Receiver process (TP-PMD 7.2.1) has a logical value 0
  NONZERO; the MLT3 bit from Receiver process (TP-PMD 7.2.1) has a non-zero logical value

decoder_output
: Indicates the value of the NRZ encoded bit.

  Values: ZERO; the output indicates a logical value of 0 to TP-TMD Descrambler process
  ONE; the output indicates a logical value of 1 to TP-TMD Descrambler process

link_status

The link_status parameter as communicated by the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact
READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

rx_quiet

The rx_quiet parameter as communicated by the PMD_RXQUIET.request (rx_quiet) primitive. This variable is from the Receive process of PCS to control the power saving function of local receiver. It is also used to set the initial state of Decoder state diagram.

Values: TRUE; The local receiver is in Quiet state
FALSE; The local receiver is not in Quiet state

prev_data

Indicates whether the last value of decoder_input was ZERO or NONZERO.

Values: ZERO; the last value of MLT3 bit of decoder_input has a logical value 0
NONZERO; the last value of MLT3 bit of decoder_input has a non-zero logical value

25.4.11.2.1.2 Messages

sentNRZbit.indicate

A signal sent to the Decoder process by the Descrambler process after an nrz bit from ciphertext bit stream has been processed using recursive linear function and is ready to process the next bit from Decoder.

Insert Figure 25-2 as depicted in Figure 25-2 at the end of Clause 25.4.11.2:

Editors' Notes: To be removed prior to final publication.

The requirement of signal detection time is different between normal operation mode and low power idle mode. In order to share one signal_detect, the timing characteristics are qualified by the LPI signal rx_lpi from PCS.

Editors' Notes: To be removed prior to final publication.

The requirement of signal detection threshold and hysteresis are different between normal operation mode and low power idle mode. Due to the significant shortening of signal detection time, the threshold need to be reduced to allow the proper detection of short pulses.
Further analysis of hysteresis is required from task force to make sure that transients of signal turning off do not trigger the thresholds.

25.4.11.3 Changes to 10.1.1.1 "Signal_Detect assertion threshold"

The TP-PMD 10.1.1.1 is applicable during the normal operation. During the low power idle mode, when rx_lpi as communicated by the PMA_RXLPI.request primitive is asserted, Signal_Detect shall be asserted per 25.4.11.5 for any valid peak to peak signal, VSDA, of greater than 400 mV.

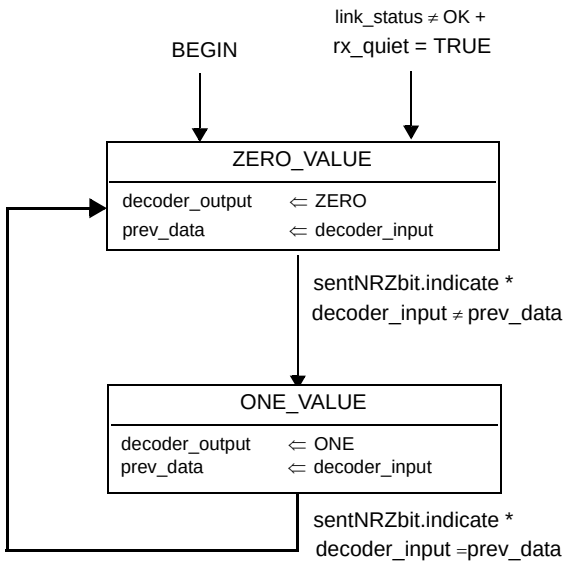


Figure 25–2—Decoder state diagram

25.4.11.4 Changes to 10.1.1.2 “Signal_Detect deassertion threshold”

The TP-PMD 10.1.1.2 is applicable during the normal operation. During the low power idle mode, when rx_lpi is deasserted, Signal_Detect shall be deasserted per 25.4.11.6 for any valid peak to peak signal, VSDA, of smaller than 200 mV.

25.4.11.5 Change to 10.1.2 “Signal_Detect timing requirements on assertion”

The TP-PMD 10.1.2 is applicable during the normal operation mode. When the Low Power Idle mode is implemented, the following paragraph is included:

During the low power idle mode, when rx_lpi is asserted, Signal_Detect output shall be asserted within 5 µs instead of 1000 µs under the same quality requirement of received signal as in normal operation. The new definition of conditional parameter AS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.4.11.6 Change to 10.1.3 “Signal_Detect timing requirements on deassertion”

The TP-PMD 10.1.3 is applicable during the normal operation mode. When the Low Power Idle mode is implemented, the following paragraph is included:

During the low power idle mode, when rx_lpi is asserted, Signal_Detect output shall be deasserted within 5 µs instead of 350 µs under the same quality requirement of received signal as in normal operation. The new definition of conditional parameter ANS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.4.11.7 Changes to TP-PMD 10.2 "Transmitter"

During the low power idle mode, when tx_quiet as communicated by PMD_TXQUIET.request primitive is deasserted, the transmitter output shall deliver a signal that exceeds Signal_Detect assertion threshold within 2 us, and at the same starting time, deliver a fully compliant 100BASE-TX signal within 5 us.

25.4.11.8 Replace TP-PMD Table 4 "Signal_Detect summary" with Table 25-3

.

Table 25–3—Signal_Detect summary

Characteristic	Minimum	Maximum	Units
Assert time Normal operation mode		1000	us
Deassert time Normal operation mode		350	us
Assert time Low Power Idle mode		5	us
Deassert time Low Power Idle mode		5	us
Assert threshold VSDA 100 ohm balanced cable Normal operation mode		1000	mV peak to peak
Deassert threshold VSDD 100 ohm balanced cable Normal operation mode	200		mV peak to peak
Assert threshold VSDA 150 ohm balanced shielded cable Normal operation mode		1225	mV peak to peak
Deassert threshold VSDD 150 ohm balanced shielded cable Normal operation mode	245		mV peak to peak
Assert threshold VSDA Low Power Idle mode		400	mV peak to peak
Deassert threshold VSDD Low Power Idle mode	200		mV peak to peak

25.5 Protocol implementation conformance statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[1]

25.5.1 Introduction

Editor's Notes: *To be removed prior to publication.*

changes and additions to PICS for LPI.

The supplier of a protocol implementation that is claimed to conform to Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

25.5.3 Major capabilities/options

Add the following row into table of Clause 25.5.3:

Item	Feature	Subclause	Status	Support	Value/Comment
*LPI	Supports LPI function	25.4.11	O		

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 30

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.

30. Management

[Editor's note (to be removed prior to publication) - The LLDP framework required for this will be undertaken by Task Force P802.3bc but the actual MIB object definitions will be provided by this task force]

30.5 Layer management for medium attachment units (MAUs)

Add new objects for LPI:

30.5.1.1.21 aEEESupportList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
100BASE-TX	Clause 24, Clause 24 MLT-3
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
1000BASE-KX	Clause 36, Clause 70 1000 Mb/s 8B/10B
10GBASE-KX4	Clause 48, Clause 71 10 Gb/s 4 lane 8B/10B
10GBASE-KR	Clause 49, Clause 72 10 Gb/s 64B/66B
10GBASE-T	Clause 55 10 Gb/s DSQ128

BEHAVIOUR DEFINED AS:

A read-only list of the possible PHY types that could support Energy Efficient Ethernet as defined in Clause 78. If Clause 28 or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local device.;

Revisions to IEEE Std 802.3-2008, Clause 35

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

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Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.

35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

Editors' Notes: *To be removed prior to publication.*
changes to GMII interface for EEE operation.

Change 35.1.1 for major concepts:

35.1.1 Summary of major concepts

a) The GMII is based on the MII defined in Clause 22.
b) Each direction of data transfer is serviced by Data (an eight-bit bundle), Delimiter, Error, and Clock signals.
c) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
d) The GMII uses the MII management interface composed of two signals that provide access to management parameters and services as specified in Clause 22.
e) MII signal names have been retained and the functions of most signals are the same, but additional valid combinations of signals have been defined for 1000 Mb/s operation.
f) The Reconciliation sublayer maps the signal set provided at the GMII to the PLS service primitives provided to the MAC.
g) GMII signals are defined such that an implementation may multiplex most GMII signals with the similar PMA service interface defined in Clause 36.
h) The GMII may also support low power idle signaling as defined for Energy Efficient Ethernet for some PHY types (see Clause 78).

Change 35.2.1 for LPI function:

35.2.1 Mapping of GMII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The mapping changes slightly when optional Low Power Idle signaling is in operation. This behavior and restrictions are the same as described in 22.7a, with the details of the signaling described in 35.2.2.

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the station management entity (STA).

Change 35.2.2 to show LPI signaling:

35.2.2 GMII signal functional specifications

Add NOTE in 35.2.2.1 for clock definitions:

NOTE—GTX_CLK may be halted during periods of low utilization according to 35.2.2.6a.

Add NOTE in 35.2.2.1 for clock definitions:

NOTE—RX_CLK may be halted during periods of low utilization according to 35.2.2.9a.

Change 22.2.2.4 for TXD definition:

35.2.2.4 TXD (transmit data)

TXD is a bundle of eight data signals (TXD<7:0>) that are driven by the Reconciliation sublayer. TXD<7:0> shall transition synchronously with respect to the GTX_CLK. For each GTX_CLK period in which TX_EN is asserted and TX_ER is de-asserted, data are presented on TXD<7:0> to the PHY for transmission. TXD<0> is the least significant bit. While TX_EN and TX_ER are both de-asserted, TXD<7:0> shall have no effect upon the PHY.

While TX_EN is de-asserted and TX_ER is asserted, TXD<7:0> are used to request the PHY to generate an assertion of low power idle; Carrier Extend or Carrier Extend Error code-groups. The use of TXD<7:0> during the transmission of a frame with carrier extension is described in 35.2.2.5 and low power idle transitions are described in 35.2.2.6a. Carrier extension shall only be signalled immediately following the data portion of a frame.

The PHY shall interpret the combination of TX_EN, TX_ER and TXD<7:0> as shown in Table 35–1 as an assertion of low power idle. Transition into and out of the low power idle state is shown in Figure 35–6a.

Table 35–1 specifies the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

Table 35–1—Permissible encodings of TXD<7:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00	Reserved	—
0	1	01	Assert low power idle	—
0	1	02 through 0E	Reserved	—
~~0~~	~~1~~	~~00 through 0E~~	~~Reserved~~	~~—~~
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter
NOTE—Values in TXD<7:0> column are in hexadecimal.				

Insert 35.2.2.6a for transmit low power idle transition:

35.2.2.6a Transmit direction low power idle transition

The MAC device asserts that it wishes the PHY to transition to the low power idle state by asserting TX_ER and setting TXD<7:0> to 01. The MAC device maintains the same state for these signals for the entire time that it wishes the PHY to remain in the low power idle state.

The MAC device may halt GTX_CLK at any time more than 9 clock cycles after the start of the low power idle state as shown in Figure 35–6a if and only if the Clock stoppable bit is asserted [45.2.3.1.3a].

When the MAC device wishes the PHY to transition out of the low power idle state it deasserts TX_ER. The MAC device should not assert TX_EN for valid transmit data until after the wake up time specified for the PHY.

Figure 35–6a shows the behavior of TX_EN, TX_ER and TXD<7:0> during the transition into and out of the low power idle state..

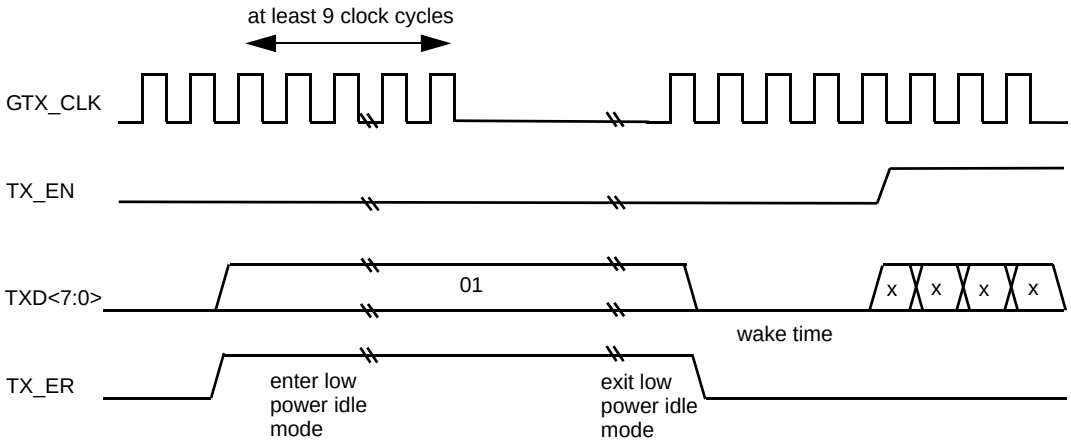


Figure 35–6a—Low power idle transition

Table 35–1 summarizes the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

Change 35.2.2.4 for RXD definition:

35.2.2.7 RXD (receive data)

RXD is a bundle of eight data signals (RXD<7:0>) that are driven by the PHY. RXD<7:0> shall transition synchronously with respect to RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD<7:0> transfer eight bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. Figure 35–8 shows the behavior of RXD<7:0> during frame reception.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication or assert low power idle by asserting the RX_ER signal while driving the specific value listed in Table 35–2 onto RXD<7:0>. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication and low power idle transitions are described in 35.2.2.9a.

While RX_DV is de-asserted, the PHY may indicate that it is receiving low power idle by asserting the RX_ER signal while driving the value <01> onto RXD<7:0>.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the GMII.

In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<7:0> back to RXD<7:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <7:0> shall not be looped back to RXD <7:0> unless the loop-back mode of operation is selected.

While RX_DV is de-asserted and RX_ER is asserted, a specific RXD<7:0> value is used to transfer recovered Carrier Extend from the PHY to the Reconciliation sublayer. A Carrier Extend Error is indicated by

another specific value of RXD<7:0>. Figure 35–7 shows the behavior of RX_DV during frame reception with carrier extension. Carrier extension shall only be signalled immediately following frame reception.

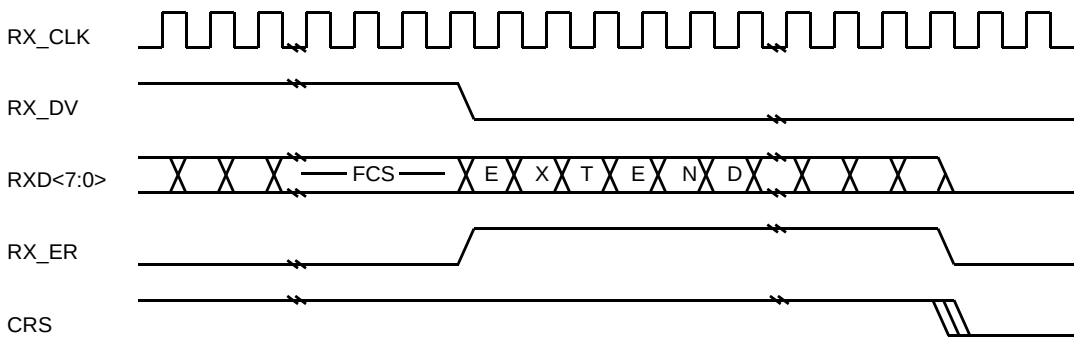


Figure 35–7—Frame reception with carrier extension

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–8 shows the behavior of RX_ER and RX_DV during burst reception.

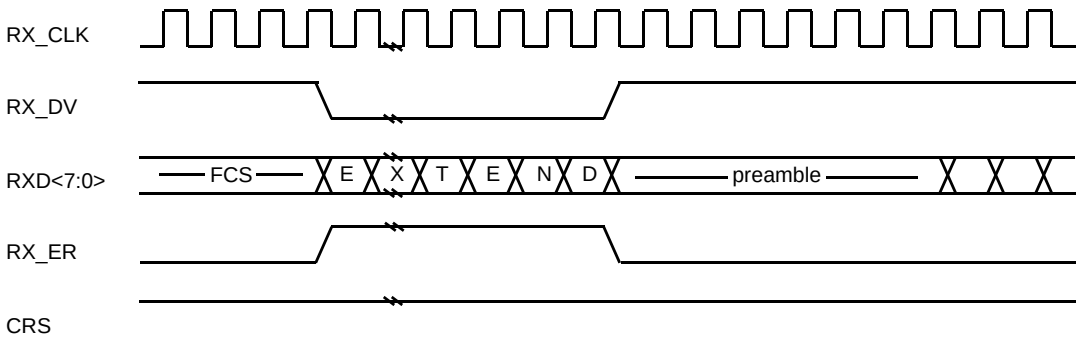


Figure 35–8—Burst reception

Table 35–2 specifies the permissible encoding of RXD<7:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Insert 35.2.2.9a for receive low power idle transition:

35.2.2.9a Receive direction low power idle transition

When the PHY receives signals from the link partner (RX_LP_IDLE) to indicate transition into the low power state it indicates this to the MAC device by asserting RX_ER and setting RXD<7:0> to 01 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power idle state. When the PHY receives signals from the link partner to indicate transition out of the low power idle state it indicates this to the MAC device by deasserting RX_ER and returning to a normal inter-frame state.

While the PHY device is indicating low power idle the PHY device may halt the RX_CLK as shown in [figure 35-9a] if and only if the Clock stoppable bit is asserted [45.2.3.1.3a].

Figure 35–9a shows the behavior of RX_ER, RX_DV and RXD<7:0> during low power idle transitions.

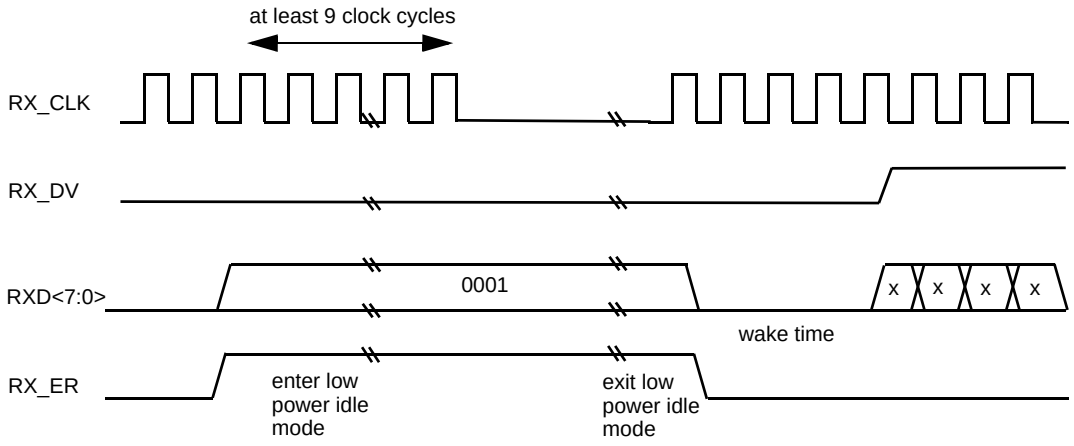


Figure 35–9a—Low power idle transitions (receive)

Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01	Assert low power idle	No applicable parameter
~~0~~	~~1~~	~~01 through 0D~~	~~Reserved~~	~~—~~
0	1	02 through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicable parameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE (eight bits)
NOTE—Values in RXD<7:0> column are in hexadecimal.				

35.5 Protocol implementation conformance statement (PICS) proforma for Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)[1]

[Editor's note (to be removed prior to publication) - changes and additions to PICS for LPI]

Add the following row into table 35.5.2.3:

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

35.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	35.2.2		O	Yes [ ] No [ ]

Add the new subclause 35.5.3.3a for LPI functions:

35.5.3.3a Low power idle functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI as defined in Table 35–1	35.2.2.4		LPI:M	Yes [ ]
L2	TX_CLK stoppable during LPI	35.2.2.6a	At least 9 cycles after LPI assertion	LPI:O	Yes [ ]
L3	RX_CLK stoppable during LPI	35.2.2.9a		LPI:O	Yes [ ]

Revisions to IEEE Std 802.3-2008, Clause 36

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 1.1, December 2008	The decision to adopt a consistent architectural model for Low Power Idle operation (see Motion #5 from the Nov 2008 meeting) across all PHYs and several issues with implementing this for backplane PHYs without violating the layering model let us to a decision to move some material from the backplane Clauses (70, 71, 72) to the 1000BASE-X (36), 10GBASE-T (48) and 10GBASE-R (49) clauses. See koenen_01_1108.pdf and healey_02_1108.pdf for more background on this. This is a substantial change and the editors suggest it be reviewed carefully.

36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

Editors' Notes: *To be removed prior to publication.*
changes to BASE-X signaling for EEE operation.

Change 36.2.4.7 for LPI signaling:

36.2.4.7 TXD (transmit data)

Eight ordered_sets, consisting of a single special code-group or combinations of special and data code-groups are specifically defined. Ordered_sets which include /K28.5/ provide the ability to obtain bit and code-group synchronization and establish ordered_set alignment (see 36.2.4.9 and 36.3.2.4). Ordered_sets provide for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. Table 36–3 lists the defined ordered_sets. The ability to transmit or receive /LI/, /LI1/ and /LI2/ is an option for certain PHYs to support Energy Efficient Ethernet (see Clause 78).

Change Table 36-3 for LPI signaling:

Table 36–3—Defined ordered_sets

Code	TXD<7:0>	Number of Code-Groups	Encoding
/C/	**Configuration**		Alternating /C1/ and /C2/
/C1/	Configuration 1	4	K28.5/D21.5/Config_Reg
/C2/	Configuration 2	4	K28.5/D2.2/Config_Reg
/I/	**IDLE**		Correcting /I1/, Preserving /I2/
/I1/	IDLE 1	2	K28.5/D5.6
/I2/	IDLE 2	2	K28.5/D16.2
/LI/	**Low Power Idle**		Correcting /LI1/, Preserving /LI2/
/LI1/	Low Power Idle 1	2	K28.5/D6.5
/LI2/	Low Power Idle 2	2	K28.5/D26.4
	Encapsulation		
/R/	Carrier_Extend	1	K23.7
/S/	Start_of_Packet	1	K27.7
/T/	End_of_Packet	1	K29.7
/V/	Error_Propagation	1	K30.7

Insert 36.2.4.12a (after 36.2.4.12) to describe Low Power Idle signaling:

36.2.4.12a Low Power Idle

Low Power Idle is transmitted in the same manner as IDLE to reflect TX_LP_IDLE or RX_LP_IDLE. See 35.2.2.6a and 35.2.2.9a for corresponding GMII definitions.

Add new constants into 36.2.5.1.2, new variables into 36.2.5.1.3, new timers into 36.2.5.1.5 and new messages into 36.2.5.1.6 to support state machine changes

36.2.5.1.2 Constants

/LI/
: The LP_IDLE ordered_set group, comprising either the /LI1/ or /LI2/ ordered_sets, as specified in 36.2.4.12a.

36.2.5.1.3 Variables

assert_lpidle
: Alias used for the optional Low Power Idle function, consisting of the following terms: (xmit=DATA * TX_OSET.indicate * TX_EN=FALSE * TX_ER=TRUE * (TXD<7:0> =01))

code_sync_status
: Variable used to by the synchronization state machine to indicate that receiver is synchronized to code-group boundaries. If the optional Low Power Idle function is implemented then this is overriden by the LPI receive state machine, otherwise this is identical to sync_status. The definition is the same as sync_status.

detect_idle
: Alias for the following terms: (xmit≠DATA * SUDI(∈[/D/] * ![/D21.5/] * ![/D2.2/])) + (xmit=DATA * SUDI(![/D21.5/] * ![/D2.2/])) that uses an alternate form to support the optional Low Power Idle function: (xmit≠DATA * SUDI(∈[/D/] * ![/D21.5/] * ![/D2.2/])) + (xmit=DATA * SUDI(![/D21.5/] * ![/D2.2/]) * SUDI(![/D26.4/] * ![/D6.5/]))

detect_lpidle
: Alias used for the optional Low Power Idle function, consisting of the following terms: (xmit=DATA * SUDI([/D26.4/] + [/D6.5/]))

rx_lpi_fail
: A boolean variable that is set to TRUE when the receiver fails to recover from a low power idle state to an Active state.

rx_lpi_mode
: An enumerated variable that is set to ON when the PMD's receiver is in a low power state and set to OFF when it is in an active state and capable of receiving data.

tx_lpi_mode
: An enumerated variable that is set to ON when the PMD's transmitter is in a low power state and set to OFF when it is in an active state and capable of transmitting data.

rx_quiet
: A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise

tx_quiet
: A boolean variable set to TRUE when the transmitter is in the TX_QUIET state and is set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 70.6.5

36.2.5.1.5 Counters

rx_deact_timer
: This timer is started when the PMD's receiver enters the RX_DEACT state. The timer terminal count is set to T_{DA}. When the timer reaches terminal count it will set the rx_deact_timer_done = TRUE.

rx_tq_timer
: This timer is started when the PMD's receiver enters the RX_QUIET state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
: This timer is started when the PMD's receiver enters the RX_WAKE state. The timer terminal count is set to T_{WR}. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PMD's receiver enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
: This timer is started when the PMD's receiver enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer
: This timer is started when the PMD's receiver enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

36.2.5.1.6 Message

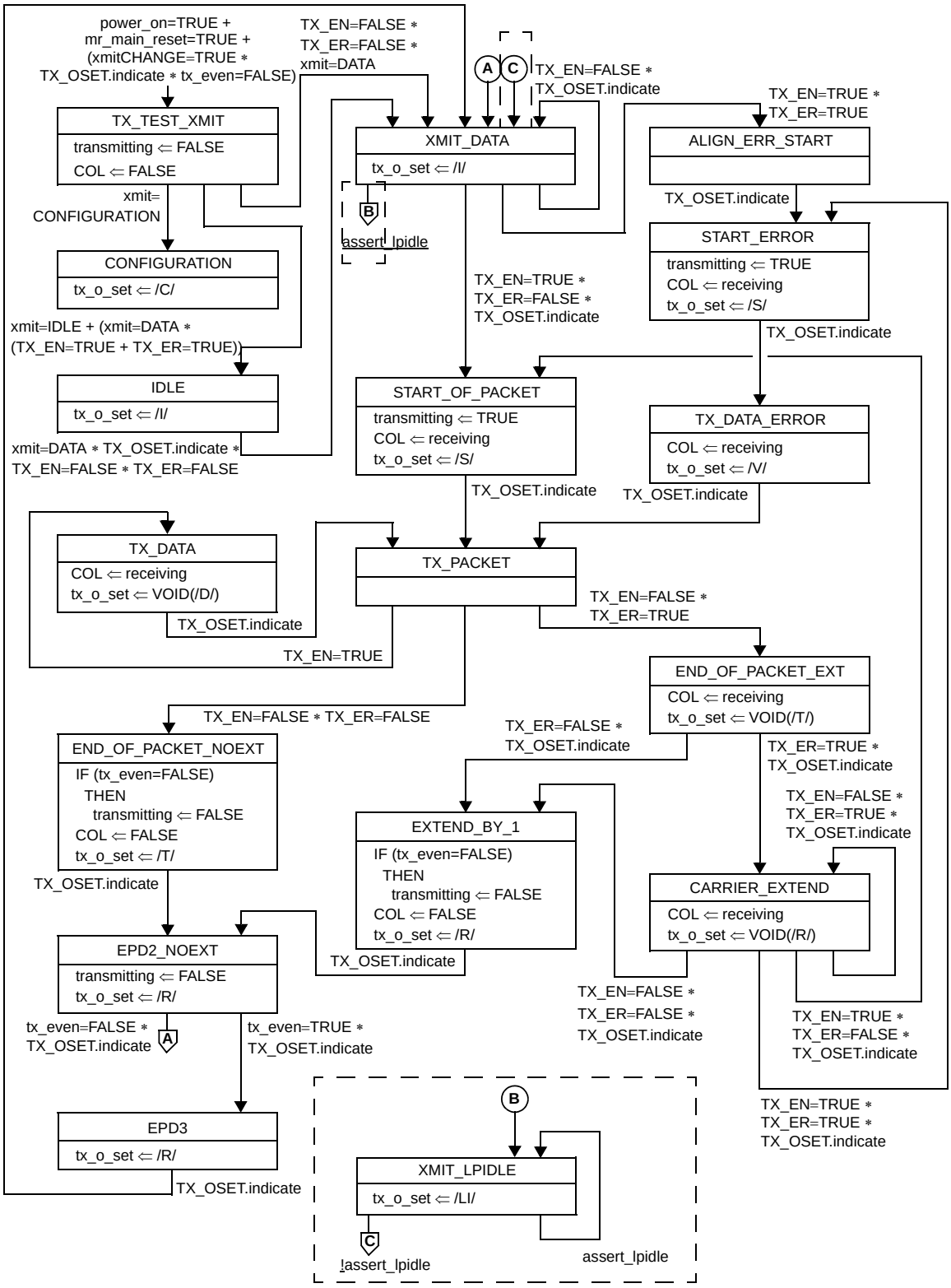
PMD_RXQUIET.request(rx_quiet)
: A signal sent by the PCS/PMA LPI receive state machine to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data. Note that this message is ignored by devices that do not support the optional LPI mechanism.

PMD_TXQUIET.request(tx_quiet)
: A signal sent by the PCS/PMA LPI transmit state machine to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium. Note that this message is ignored by devices that do not support the optional LPI mechanism.

Change 36.2.5.2.1 and 2, transmit and receive state machines for LPI:

36.2.5.2.1 Transmit

The PCS Transmit process is depicted in two state diagrams: PCS Transmit ordered_set and PCS Transmit code-group. The PCS shall implement its Transmit process as depicted in Figures 36–1 and 36–2, including compliance with the associated state variables as specified in 36.2.5.1.



Change Figure 36-1, new states and transitions in dotted boxes

Figure 36–1—PCS transmit ordered_set state diagram

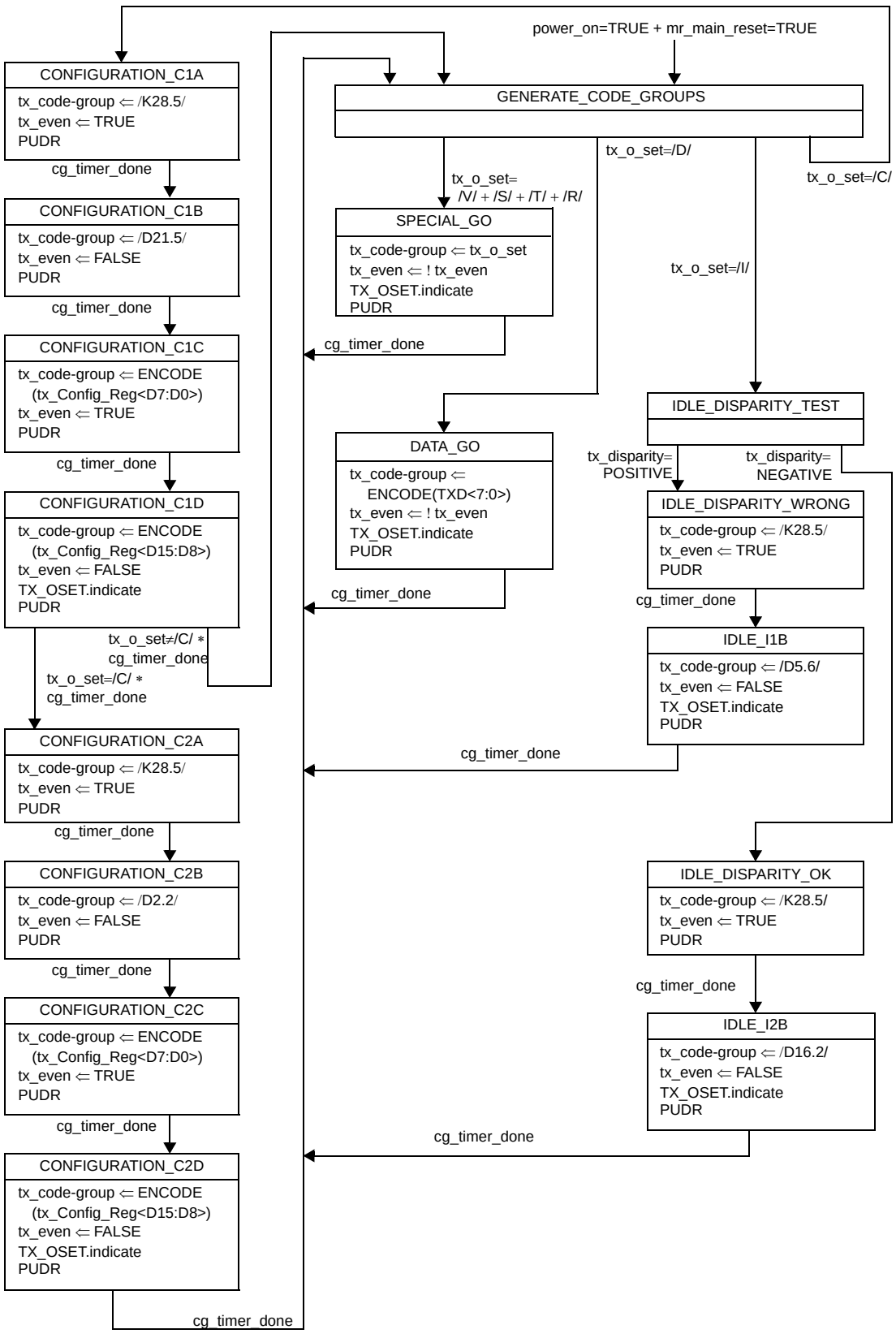
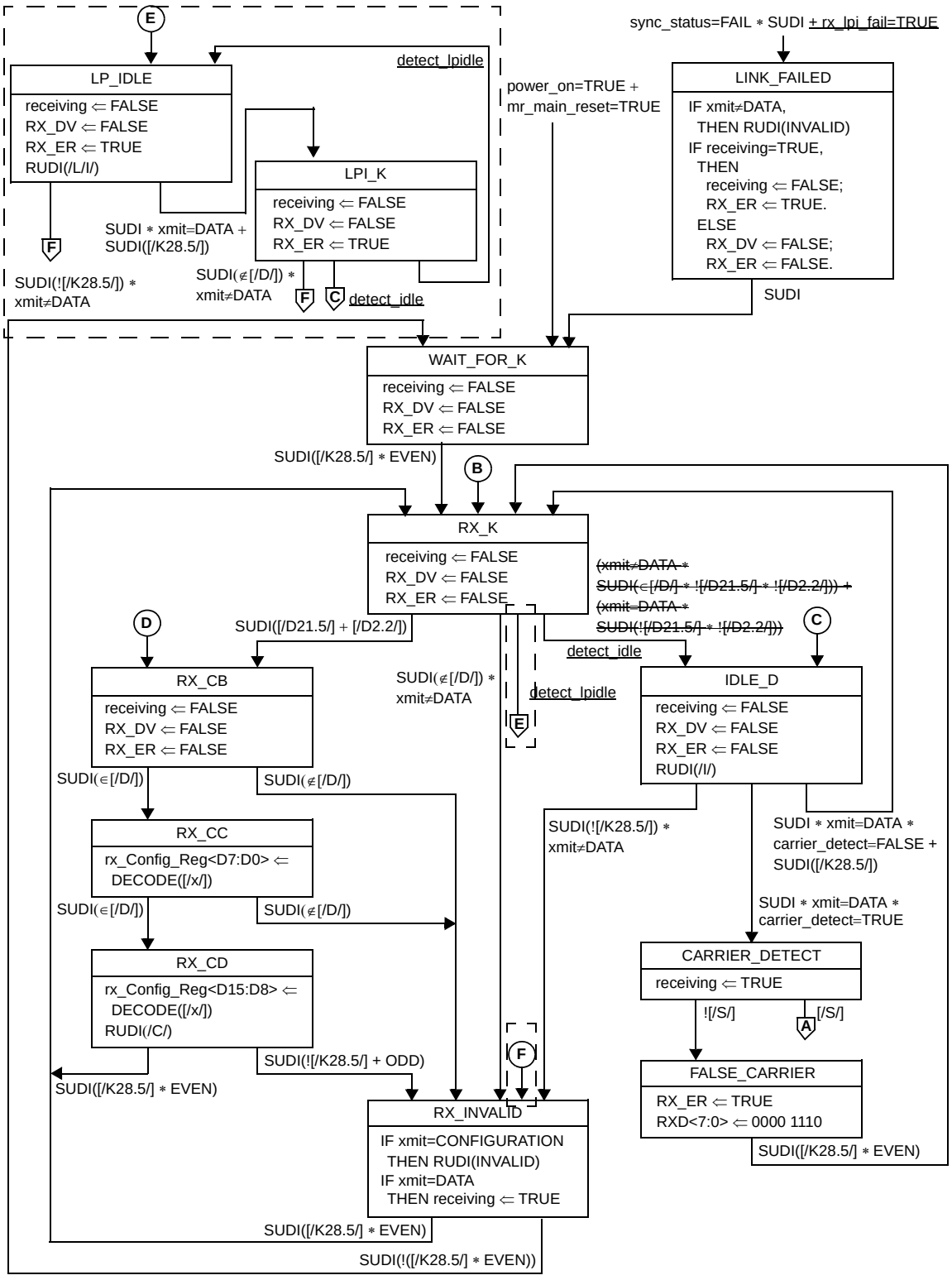


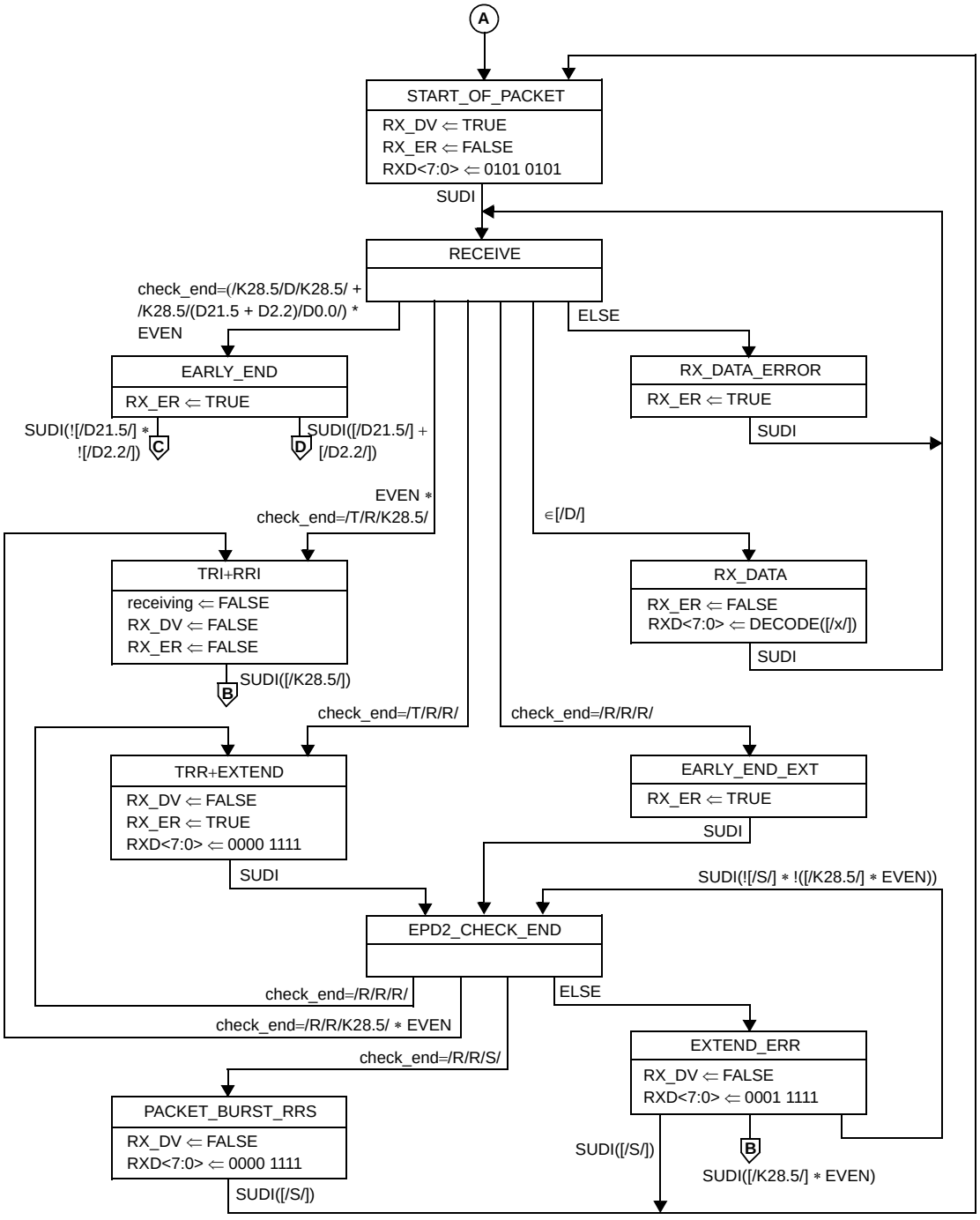
Figure 36–6—PCS transmit code-group state diagram



Change Figure 36-7a, new states and transitions in dotted boxes

NOTE—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7b, and vice versa.

Figure 36–7a—PCS receive state diagram, part a



NOTE 1—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

NOTE 2—In the transition from RECEIVE to RX_DATA state the transition condition is a test against the code-group obtained from the SUDI that caused the transition to RECEIVE state.

Figure 36–7b—PCS receive state diagram, part b

The Transmit ordered_set process continuously sources ordered_sets to the Transmit code-group process. When initially invoked, and when the Auto-Negotiation process xmit flag indicates CONFIGURATION, the Auto-Negotiation process is invoked. When the Auto-Negotiation process xmit flag indicates IDLE, and between packets (as delimited by the GMII), /I/ is sourced. Upon the assertion of TX_EN by the GMII when the Auto-Negotiation process xmit flag indicates DATA, the SPD ordered_set is sourced. Following the SPD, /D/ code-groups are sourced until TX_EN is deasserted. Following the de-assertion of TX_EN, EPD ordered_sets are sourced. If TX_ER is asserted when TX_EN is deasserted and carrier extend error is not indicated by TXD, /R/ ordered_sets are sourced for as many GTX_CLK periods as TX_ER is asserted with a delay of two GTX_CLK periods to first source the /T/ and /R/ ordered sets. If carrier extend error is indicated by TXD during carrier extend, /V/ ordered_sets are sourced. If TX_EN and TX_ER are both de-asserted, the /R/ ordered_set may be sourced, after which the sourcing of /I/ is resumed. If, while TX_EN is asserted, the TX_ER signal is asserted, the /V/ ordered_set is sourced except when the SPD ordered set is selected for sourcing.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the models of 10BASE-T and 100BASE-X.

The Transmit code-group process continuously sources tx_code-group<9:0> to the PMA based on the ordered_sets sourced to it by the Transmit ordered_set process. The Transmit code-group process determines the proper code-group to source based on even/odd-numbered code-group alignment, running disparity requirements, and ordered_set format.

36.2.5.2.2 Receive

The PCS shall implement its Receive process as depicted in Figure 36–7a and Figure 36–7b, including compliance with the associated state variables as specified in 36.2.5.1.

The PCS Receive process continuously passes RXD<7:0> and sets the RX_DV and RX_ER signals to the GMII based on the received code-group from the PMA.

When the Auto-Negotiation process xmit flag indicates CONFIGURATION or IDLE, the PCS Receive process continuously passes /C/ and /I/ ordered sets and rx_Config_Reg<D15:D0> to the Auto-Negotiation process.

Change 36.2.5.2.6 for synchronization:

36.2.5.2.6 Synchronization

The PCS shall implement the Synchronization process as depicted in Figure 36–9 including compliance with the associated state variables as specified in 36.2.5.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions.

A receiver that is in the LOSS_OF_SYNC state and that has acquired bit synchronization attempts to acquire code-group synchronization via the Synchronization process. Code-group synchronization is acquired by the detection of three ordered_sets containing commas in their leftmost bit positions without intervening invalid code-group errors. Upon acquisition of code-group synchronization, the receiver enters the SYNC_ACQUIRED_1 state. Acquisition of synchronization ensures the alignment of multi-code-group ordered_sets to even-numbered code-group boundaries.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states.

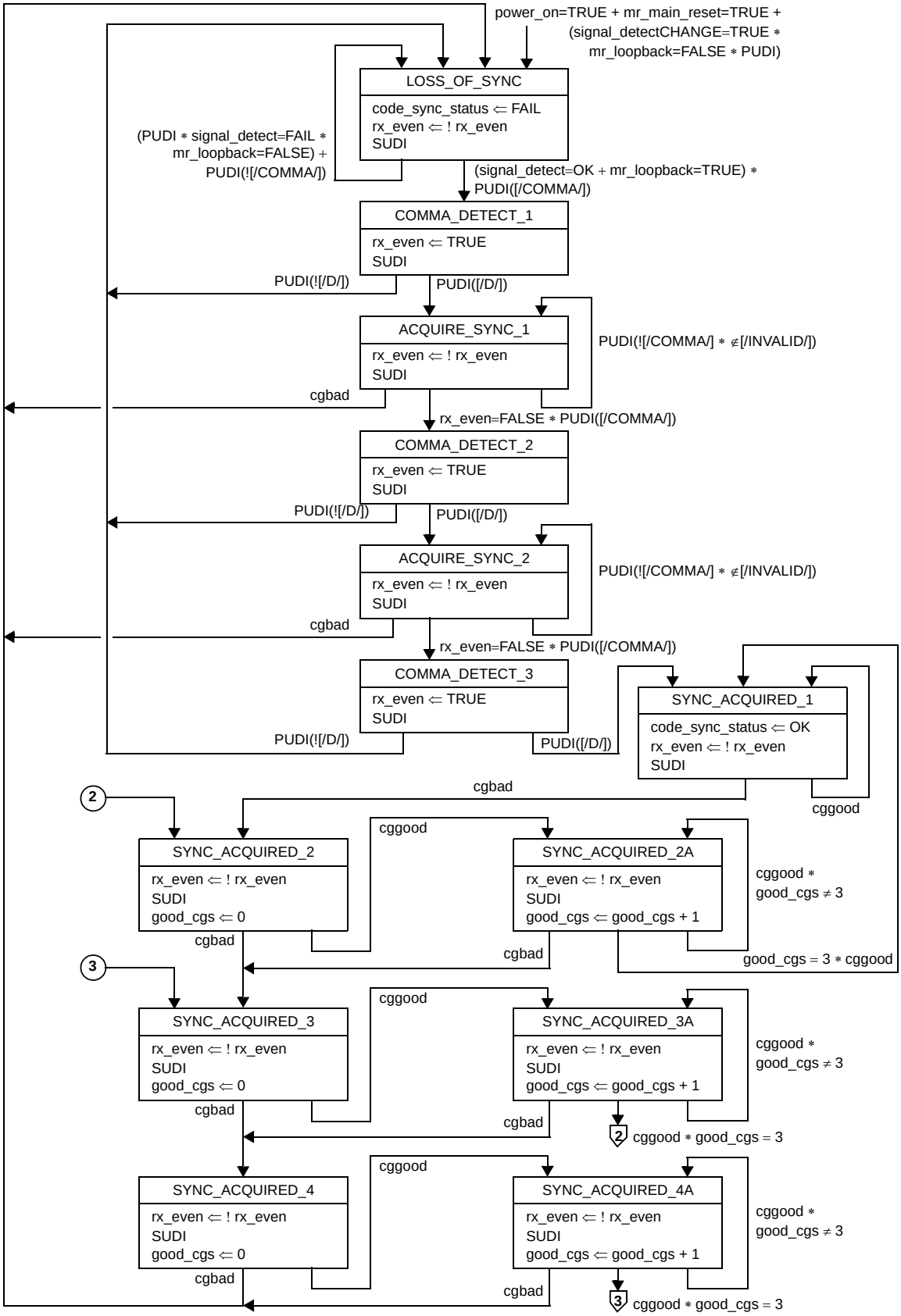


Figure 36–9—Synchronization state diagram

If the optional Low Power Idle function is not implemented then sync_status is identical to code_sync_status. Otherwise the relationship between sync_status and code_sync_status is given by 36-9b the LPI receive state diagram.

The condition sync_status=FAIL existing for ten ms or more causes the PCS Auto-Negotiation process to begin and the PCS Transmit process to begin transmission of /C/. Upon reception of three matching /C/s from the link partner, the PCS Auto-Negotiation process begins. The internal signal receiving is de-asserted in the PCS Receive process LINK_FAILED state when sync_status=FAIL and a code-group is received.

Insert 36.2.5.2.8 for LPI state machines:

36.2.5.2.8 LPI state diagrams

If the optional Low Power Idle function is implemented the transmit and receive functions are modified as shown in Figures 36–9a and 36–9b.

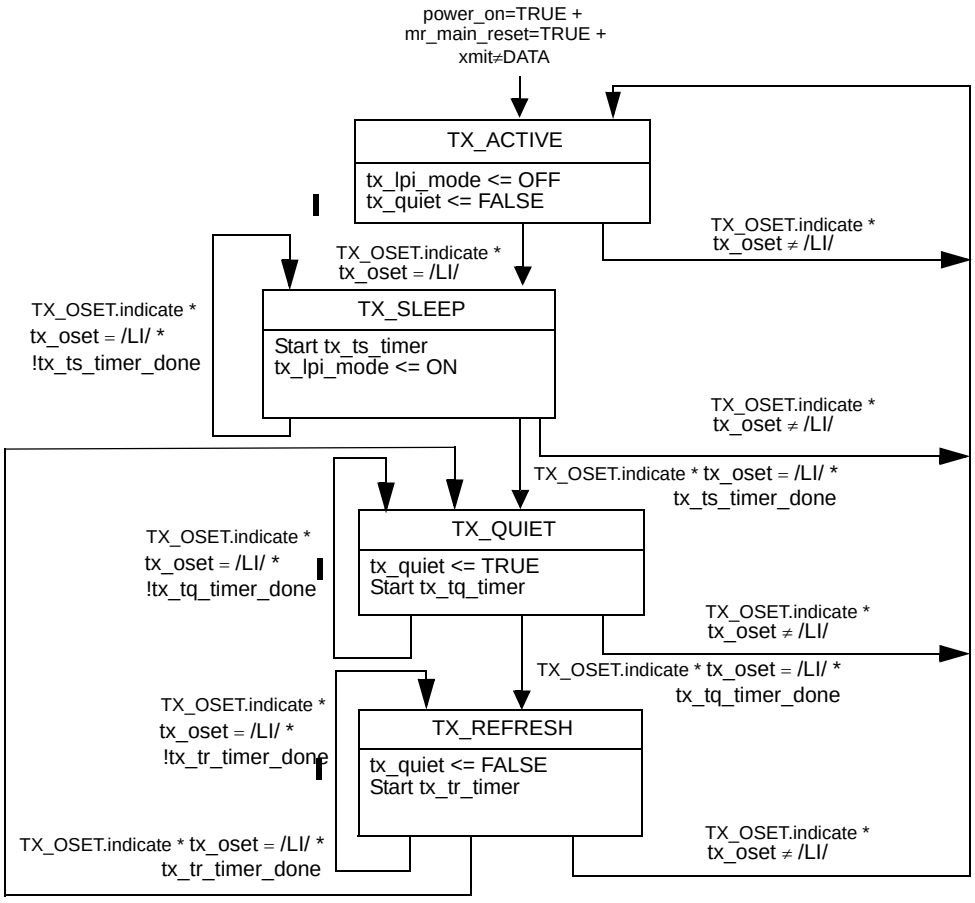


Figure 36–9a—LPI Transmit state diagram

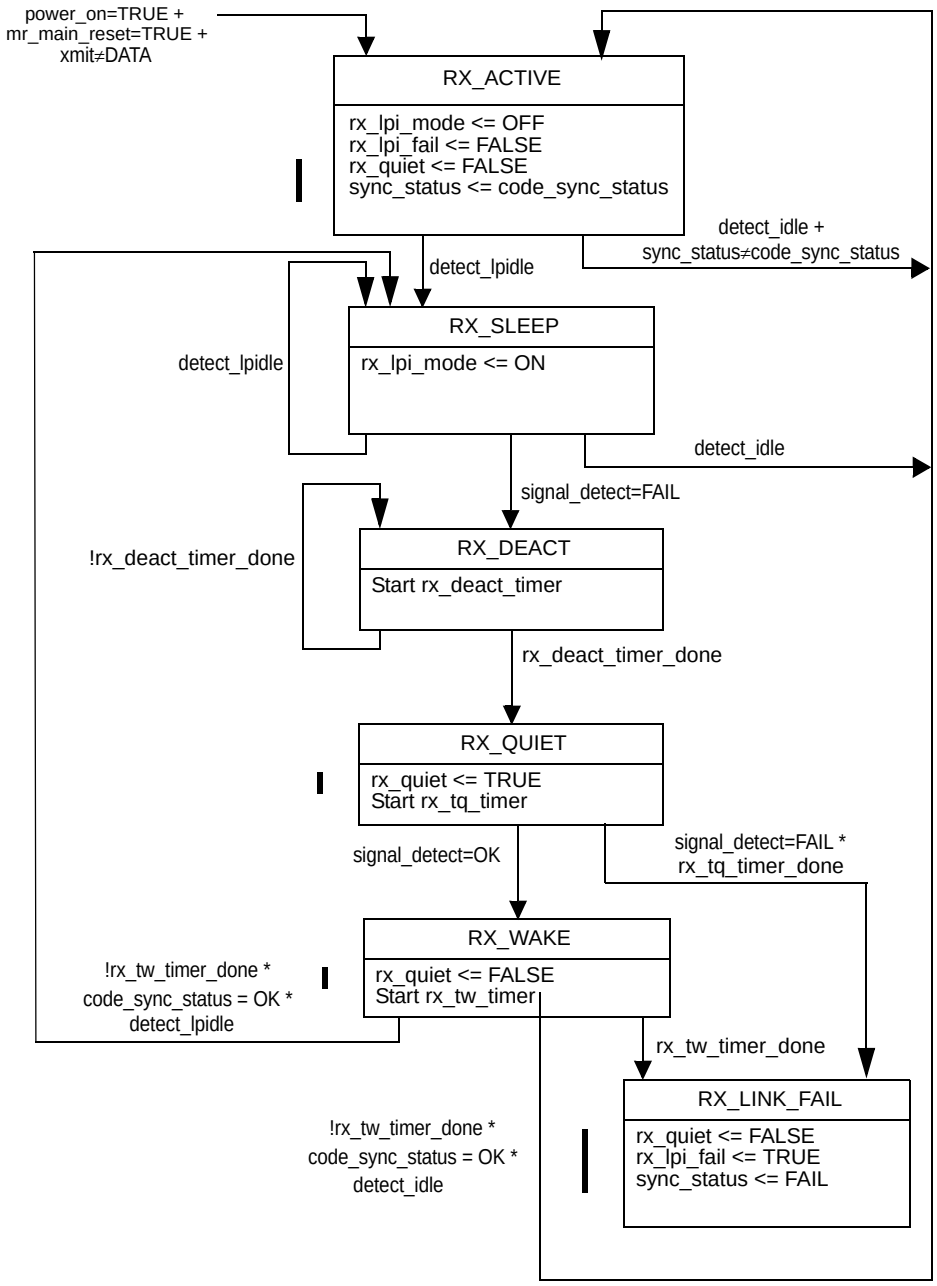


Figure 36–9b—LPI Receive state diagram

The timer values for these state machines are shown in Table 36–3a for transmit and Table 36–3b for receive.

Table 36–3a—Transmitter LPI timing parameters

Parameter	Description	Value	Units
T_{SL}	Local Sleep Time from entering TX_SLEEP state to transmit disable	20	μs
T_{QL}	Local Quiet Time from Transmitter disabled to start of TX_REFRESH state	2.5	ms
T_{UL}	Local Refresh Time from transmitter activated to TX_QUIET state	20	μs

Table 36–3b—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect while in the RX_QUIET state before asserting a rx_fault	3	4	ms
T_{WR}	Time to wake remote link partner's receiver. T_{WR} is set by the remote link partner during Auto-negotiation.	10	20[a]	μs
T_{DA}	Time to deactivate receiver to handle debounce	1	2	μs

[a]Remote receiver can ask for four T_{WR} values: 10μs, 13μs, 17μs and 20μs.

Insert 36.2.5.2.9 for LPI status:

36.2.5.2.9 LPI status and management

If the optional Low Power Idle function is implemented the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variable shown in Table 36-3c.

Table 36–3c—MDIO status indications

MDIO status variable	Register name	Register address	Note
Tx LP idle received	PCS status register 1	3.1.11	Latched version of 3.1.9
Rx LP idle received	PCS status register 1	3.1.10	Latched version of 3.1.8
Tx LP idle indication	PCS status register 1	3.1.9	TRUE when not in state TX_ACTIVE
Rx LP idle indication	PCS status register 1	3.1.8	TRUE when not in state RX_ACTIVE

36.7 Protocol implementation conformance statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X[1]

[Editor's note (to be removed prior to publication) - changes and additions to PICS for LPI]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Add the following row into table 36.7.3:

36.7.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	36.2.4.12a		O	Yes [ ] No [ ]

Revisions to IEEE Std 802.3-2008, Clause 40

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: To be removed prior to final publication.

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:
Draft 0.1, July 2008: Intial draft for IEEE P802.3az Task Force review.
Draft 1.0, November 2008: Incorporates responses to comments agreed at the September 2008 interim meeting.
Draft 1.1, January 2009: Incorporates responses to comments agreed at the November 2008 plenary meeting.
Draft 1.2, March 2009: Incorporates responses to comments agreed at the January 2009 interim meeting.

40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

40.1.3 Operation of 1000BASE-T

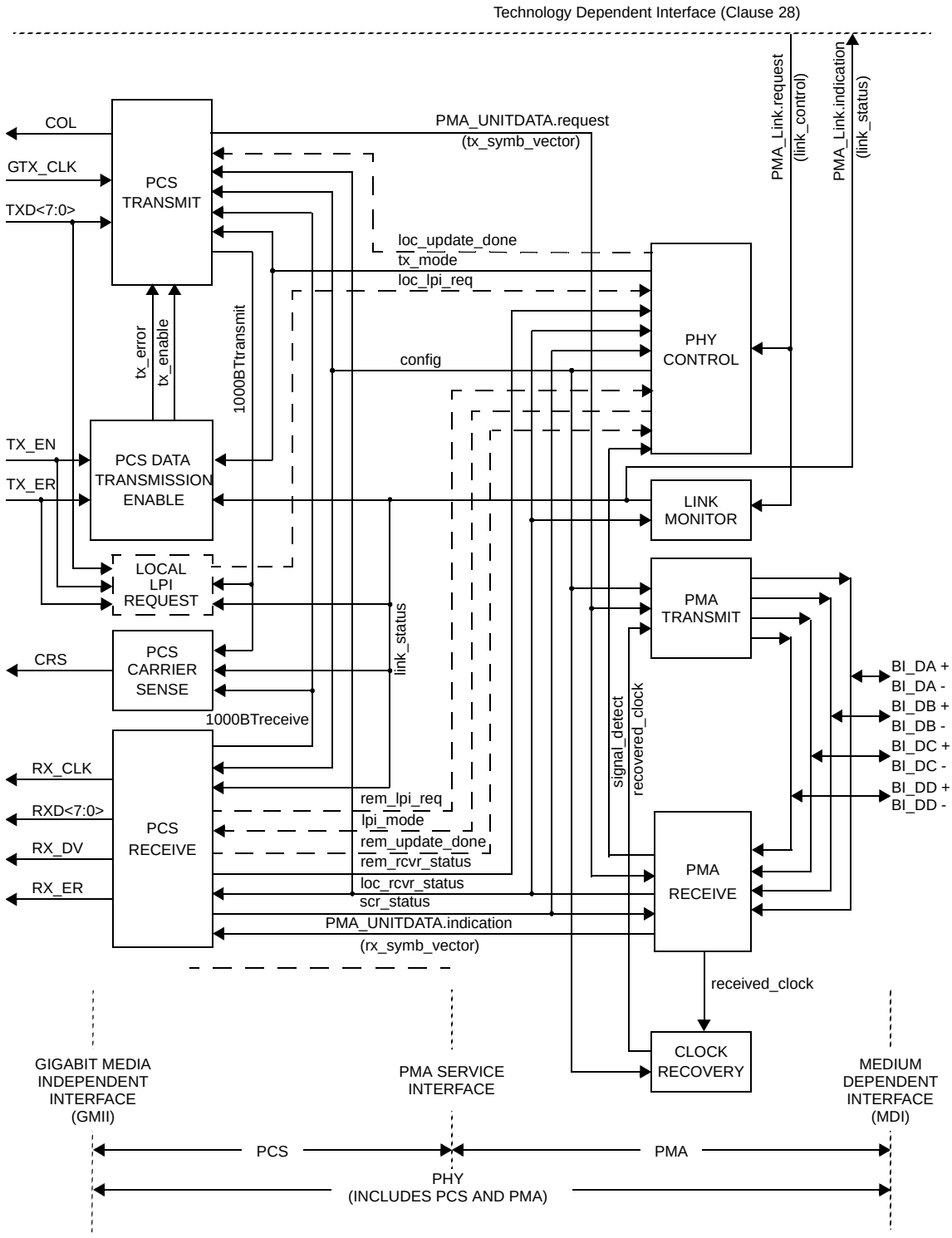
Insert paragraph as shown before the last paragraph of 40.1.3:

A 1000BASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 40.5, and Annex 28C). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 40–3. In a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

A 1000BASE-T PHY may optionally enter a low power mode to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The "Assert low power idle" request at the GMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as "Assert low power idle" at the GMII. When low power idle is simultaneously transmitted and received, an Energy Efficient 1000BASE-T PHY ceases transmission and deactivates transmit and receive functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the GMII, the PHY re-activates transmit and receive functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power mode.

The PCS and PMA subclauses of this document are summarized in 40.1.3.1 and 40.1.3.2. Figure 40–3 shows the functional block diagram.

Replace the existing Functional block diagram figure (Figure 40–3) with the new Functional block diagram figure shown in Figure 40–3.



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are optional.

Figure 40–3—Functional block diagram

40.1.3.1 Physical Coding Sublayer (PCS)

Insert text shown below after the fourth paragraph is 40.1.3.1 as shown below:

Between frames, a special subset of code-groups using only the symbols {2, 0, –2} is transmitted. This is called idle mode. Idle mode encoding takes into account the information of whether the local PHY is operating reliably or not (see 40.4.2.4) and allows this information to be conveyed to the remote station. During normal operation, idle mode is followed by a data mode that begins with a Start-of-Stream delimiter.

When the PHY supports Energy Efficient Ethernet, Idle mode encoding also conveys to the remote PHY information of whether the local PHY is requesting entry into the low power mode or not. Such requests are a direct translation of the assertion of low power idle at the GMII. In addition, Idle mode encoding conveys to the remote PHY whether the local PHY has completed the update of its receiver state or not, as indicated by the PMA PHY Control function.

Further patterns are used for signaling a transmit error and other control functions during transmission of a data stream.

40.1.3.2 Physical Medium Attachment (PMA) sublayer

Insert the following text before the last paragraph of 40.1.3.2:

When the PHY supports Energy Efficient Ethernet, the PMA PHY Control function also coordinates transitions between the low power mode and the normal operating mode.

PMA functions and state diagrams are specified in 40.4. PMA electrical specifications are given in 40.6.

40.1.4 Signaling

Insert new items j) and k) into the list of signaling scheme objectives as shown below and renumber subsequent items in list:

a) Forward Error Correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping and inverse mapping from octet data to a quartet of quinary symbols and back.
c) Uncorrelated symbols in the transmitted symbol stream.
d) No correlation between symbol streams traveling both directions on any pair combination.
e) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
f) Idle mode uses a subset of code-groups in that each symbol is restricted to the set {2, 0, –2}to ease synchronization, start-up, and retraining.
g) Ability to rapidly or immediately determine if a symbol stream represents data or idle or carrier extension.
h) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
i) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
j) Optionally, ability to signal to the remote PHY a request to enter the low power mode and to exit the low power mode and return to normal operation.
k) Optionally, ability to signal to the remote PHY that the update of the local receiver state (e.g. timing recovery, adaptive filter coefficients) has completed.
l) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
m) Ability to automatically detect and correct for incorrect polarity in the connections.
n) Ability to automatically correct for differential delay variations across the wire-pairs.

Change the last paragraph of 40.1.4 as shown below:

The PHY ~~operates~~ may operate in ~~two~~ three basic modes, normal ~~mode~~mode, training mode, or ~~training~~an optional low power mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA. In training mode, the PCS is directed to generate only idle code-groups for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. In low power mode, the PCS is directed to generate only idle code groups encoded with low power request and update status indications, or zeros as dictated by the PMA PHY Control function. (See the PCS reference diagram in 40.2.).

40.2.2 PMA Service Interface

Insert three new items in the list of service primitives as shown below:

PMA_LPIMODE.indication(lpi_mode)

PMA_LPIREQ.request(loc_lpi_req)

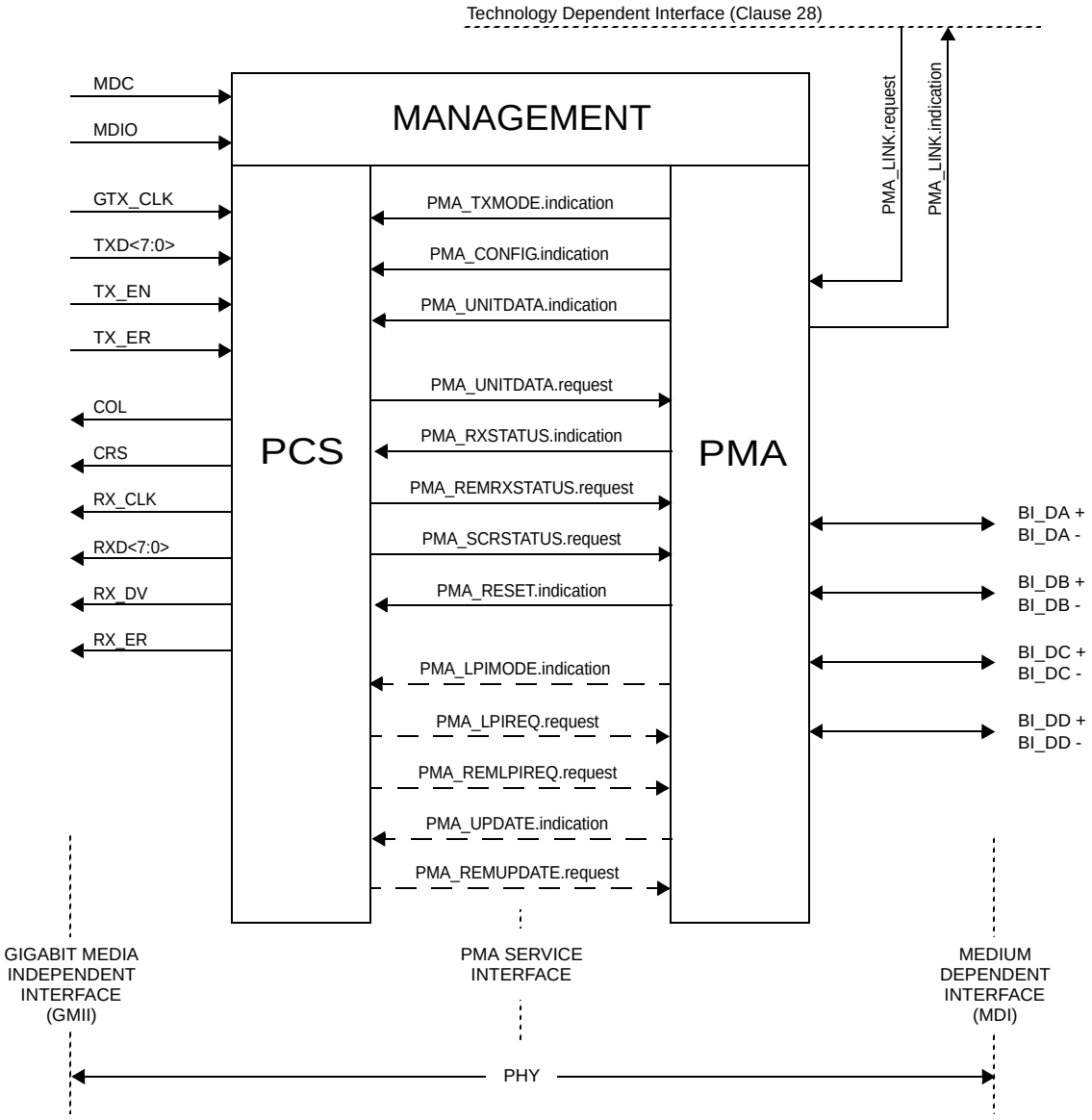
PMA_REMLPIREQ.request(rem_lpi_req)

PMA_UPDATE.indication(loc_update_done)

PMA_REMUPDATE.request(rem_update_done)

The use of these primitives is illustrated in Figure 40–4.

Replace Figure 40–4 with the new Figure 40–4 shown below:



NOTE—Service interface primitives shown with dashed lines are optional.

Figure 40–4—1000BASE-T service interfaces

Insert the following text after 40.2.10 PMA_RESET.indication:

40.2.11 PMA_LPIMODE.indication

This primitive is generated by the PMA to indicate that the PHY has entered the low power mode of operation.

40.2.11.1 Semantics of the primitive

PMA_LPIMODE.indication(lpi_mode)

PMA_LPIMODE.indication specifies to the PCS Receive function, via the parameter lpi_mode, whether or not the PHY has entered low power mode. The parameter lpi_mode can take on one of the following values of the form:

ON	This value is asserted with then PHY is operating in low power mode.
OFF	This value is asserted during normal operation.

40.2.11 PMA_LPIREQ.request

This primitive is generated by the PCS to indicate a request to enter the low power mode.

40.2.11.1 Semantics of the primitive

PMA_LPIREQ.request (loc_lpi_req)

PMA_LPIREQ.request specifies to the PMA PHY Control, via the parameter loc_lpi_req, whether or not the PHY is requested to enter the low power mode. The parameter loc_lpi_req can take on one of the following values of the form:

TRUE	This value is continuously asserted when “Assert low power idle” is present on the GMII. Note “Assert low power idle” at the GMII implies that no frame transmission is in progress hence 1000BTtransmit (refer to 40.3.3.1) will also be FALSE.
FALSE	This value is continuously asserted when “Assert low power idle” is not present at the GMII.

40.2.11.2 When generated

The PCS Local LPI Request function generates PMA_LPIREQ.request messages continuously.

40.2.11.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.2.12 PMA_REMLPIREQ.request

This primitive is generated by the PCS to indicate a request to enter low power mode as communicated by the remote PHY via its encoding of its loc_lpi_req parameter.

40.2.12.1 Semantics of the primitive

PMA_REMLPIREQ.request (rem_lpi_req)

PMA_REMLPIREQ.request specifies to the PMA PHY Control, via the parameter rem_lpi_req, whether or not the remote PHY is requesting entry into low power mode. The parameter rem_lpi_req can take on one of the follow values of the form:

TRUE	This value is continuously asserted when low power idle is encoded in the received symbols.
FALSE	This value is continuously asserted when low power idle is not encoded in the received symbols.

40.2.12.2 When generated

The PCS Receive function generates PMA_REMLPIREQ.request messages continuously on the basis of the signals received at the MDI.

40.2.12.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.2.13 PMA_UPDATE.indication

This primitive is generated by the PMA to indicate that the PHY has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients).

40.2.13.1 Semantics of the primitive

PMA_UPDATE.indication(loc_update_done)

PMA_UPDATE.indication specifies to the PCS Transmit functions, via the parameter loc_update_done, whether or not the PHY has completed the update of its receiver state. The parameter loc_update_done can take on one of the following values of the form:

ON	This value is asserted when the PHY has completed the current update.
OFF	This value is asserted when the PHY is ready for the next update or when the current update is still in progress.

40.2.13.2 When generated

The PMA PHY Control function generates PMA_UPDATE.indication messages continuously.

40.2.13.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3 and 40.3.1.4.

40.2.14 PMA_REMUPDATE.request

This primitive is generated by the PCS to indicate that the remote PHY has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients).

Semantics of the primitive

PMA_REMUPDATE.request(rem_update_done)

PMA_REMUPDATE.indication specifies to the PMA_PHY_Control function, via the parameter rem_update_done, whether or not the remote PHY has completed the update of its receiver state. The parameter rem_update_done can take on one of the following values of the form:

ON	This value is asserted when the remote PHY has completed the current update.
OFF	This value is asserted to when the remote PHY is ready for the next update or when the current update is still in progress.

40.2.14.1 When generated

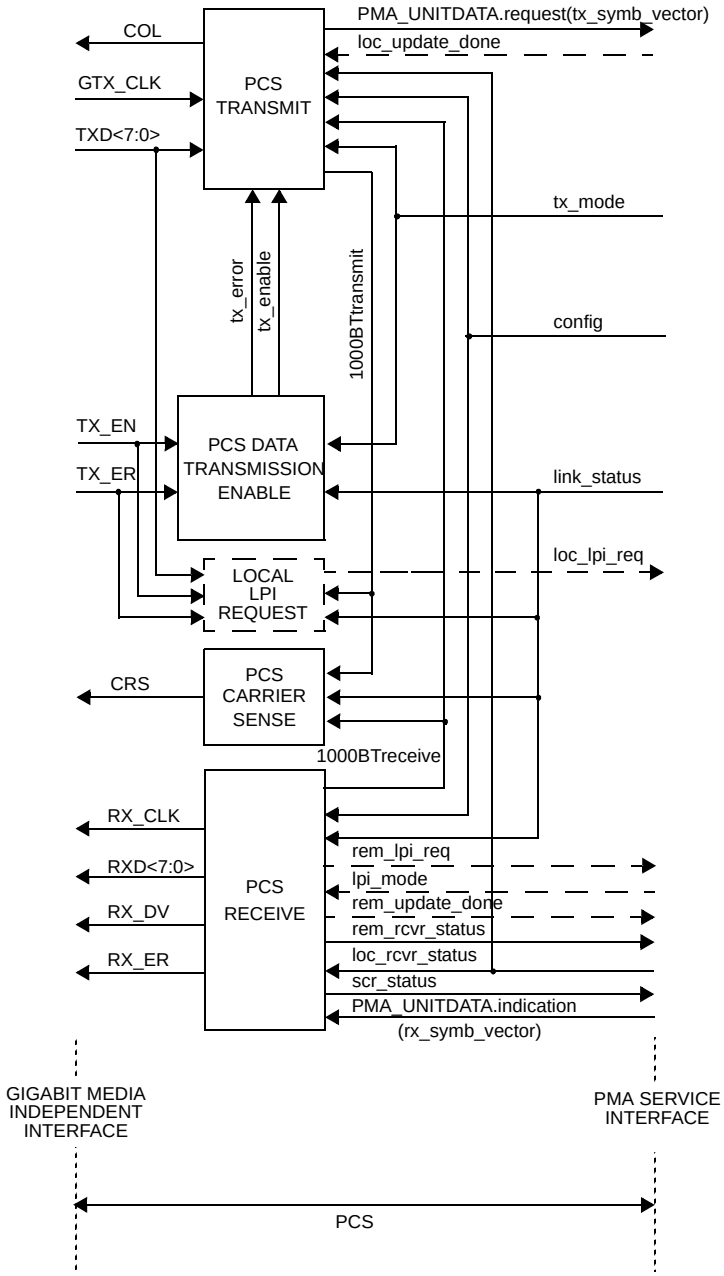
The PCS Receive function generates PMA_REMUDPATE.request messages continuously.

40.2.14.2 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.3 Physical Coding Sublayer (PCS)

Replace the existing PCS reference diagram, Figure 40–5 with the new Figure 40–5 shown below:



NOTE—Signals and functions shown with dashed lines are optional.

Figure 40–5—PCS reference diagram

40.3.1.3 PCS Transmit function

Insert the text shown below between paragraphs five and six as shown below:

If a PMA_TXMODE.indication message has the value SEND_I, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values {+2, 0, –2} are transmitted in this case. Training mode encoding also takes into account the value of the

parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner during idle transmission.

When the PHY supports Energy Efficient Ethernet, the low power mode encoding also takes into account the value of the parameter loc_lpi_req. By this mechanism, the PHY indicates whether it requests to operate in low power mode or return to the normal mode of operation. In addition, low power mode encoding takes into account the value of loc_update_done. By this mechanism, the PHY indicates whether it has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients) or not, as indicated by the PMA PHY Control function.

In the normal mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses an 8B1Q4 coding technique to generate at each symbol period code-groups that represent data, control or idle based on the code-groups defined in Table 40–1 and Table 40–2. During transmission of data, the TXD<7:0> bits are scrambled by the PCS using a side-stream scrambler, then encoded into a code-group of quinary symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a three-state convolutional encoder.

40.3.1.3.4 Generation of bits $Sd_n[8:0]$

Change the definition of $Sd_n[5:3]$ as shown below:

The bits Sd_n[5:4]~~[5:3]~~ are derived from the bits Sc_n[5:4]~~[5:3]~~ and the GMII data bits TXD_n[5:4]~~[5:3]~~ as

$$Sd_n[5:4\text{~~3~~}] = \begin{cases} Sc_n[5:4]\text{~~[5:3]~~} \wedge TXD_n[5:4]\text{~~[5:3]~~} & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[5:4]\text{~~[5:3]~~} & \text{else} \end{cases}$$

The bit Sd_n[3] is used to scramble the GMII data bit TXD_n[3] during data mode and to encode loc_lpi_req otherwise. It is defined as

$$Sd_n[3] = \begin{cases} Sc_n[3] \wedge TXD_n[3] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[3] \wedge 1 & \text{else if } ((loc\_lpi\_req = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[3] & \text{else} \end{cases}$$

Change the definition of $Sd_n[2]$ as shown below:

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } ((loc\_rcvr\_status = \text{OK}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[2] & \text{else} \end{cases}$$

Change the definition of $Sd_n[1]$ as shown below:

The bits Sd_n[1:0] are used to transmit carrier extension information during tx_mode=SEND_N and are thus dependent upon the bits $cext_n$ and $cext\_err_n$. In addition, bit Sd_n[1] is used to encode loc_update_done. These bits are dependent on the variable tx_error_n, which is defined in Figure 40–8. These bits are defined as

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] \text{ if } (tx\_enable_{n-2} = 1) \\ \underline{Sc_n[1] \wedge 1 \text{ else if } ((loc\_update\_done = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z}))} \\ Sc_n[1] \wedge cext\_err_n \text{ else} \end{cases}$$

40.3.1.4 PCS Receive function

Insert the text below following the second paragraph:

When the PHY supports Energy Efficient Ethernet, the PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode to derive the values of the variables rem_lpi_req and rem_update_done.

Insert the text below as 40.3.1.6 following 40.3.1.5 PCS Carrier Sense function:

40.3.1.6 PCS Local LPI Request function

The PCS Local LPI Request function generates the signal loc_lpi_req, which indicates to the PMA_PHY_Control function whether or not the local PHY is requested to enter the low power mode. For a PHY that supports Energy Efficient Ethernet, the PCS shall conform to the Local LPI Request state diagram as depicted in Figure 40–9 including compliance with the associated state variables as specified in 40.3.3.

40.3.3 State variables

40.3.3.1 Variables

Change the following variable definition as shown:

1000BTtransmit

A Boolean used by the PCS Transmit Process to indicate whether a frame transmission is in progress. Also ~~U~~used by the Carrier Sense and Local LPI Request processes.

Values: TRUE: The PCS is transmitting a stream
FALSE: The PCS is not tranmsitting a stream

Insert the following variables/variable definitions in alphabetical order in the existing list of variables:

loc_lpi_req

The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the low power mode. It is passed to the PMA_PHY_Control function via the PMA_LPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE.

Values: TRUE or FALSE

lpi_mode

The lpi_mode variable is generated by the PMA_PHY_Control function and indicates whether or not the local PHY has entered low power mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. When Energy Efficient Ethernet is not implemented, this variable is set to OFF,

Values: ON or OFF

rem_lpi_req

The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not

the remote PHY is requesting entry into low power mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this value shall be set to FALSE.
Values: ON or OFF

40.3.4 State diagrams

Insert the PCS Local LPI Request state diagram (Figure 40-9) after Figure 40-8 and renumber subsequent figures:

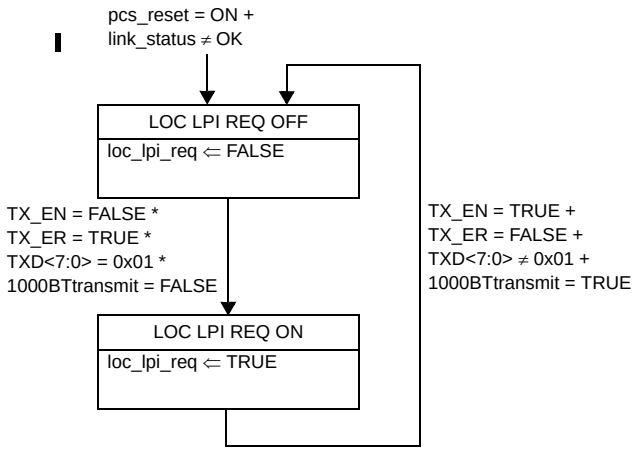


Figure 40–9—PCS Local LPI Request state diagram (optional)

Replace existing PCS Receive state diagrams, part a (Figure 40-10a) with new PCS Receive state part a

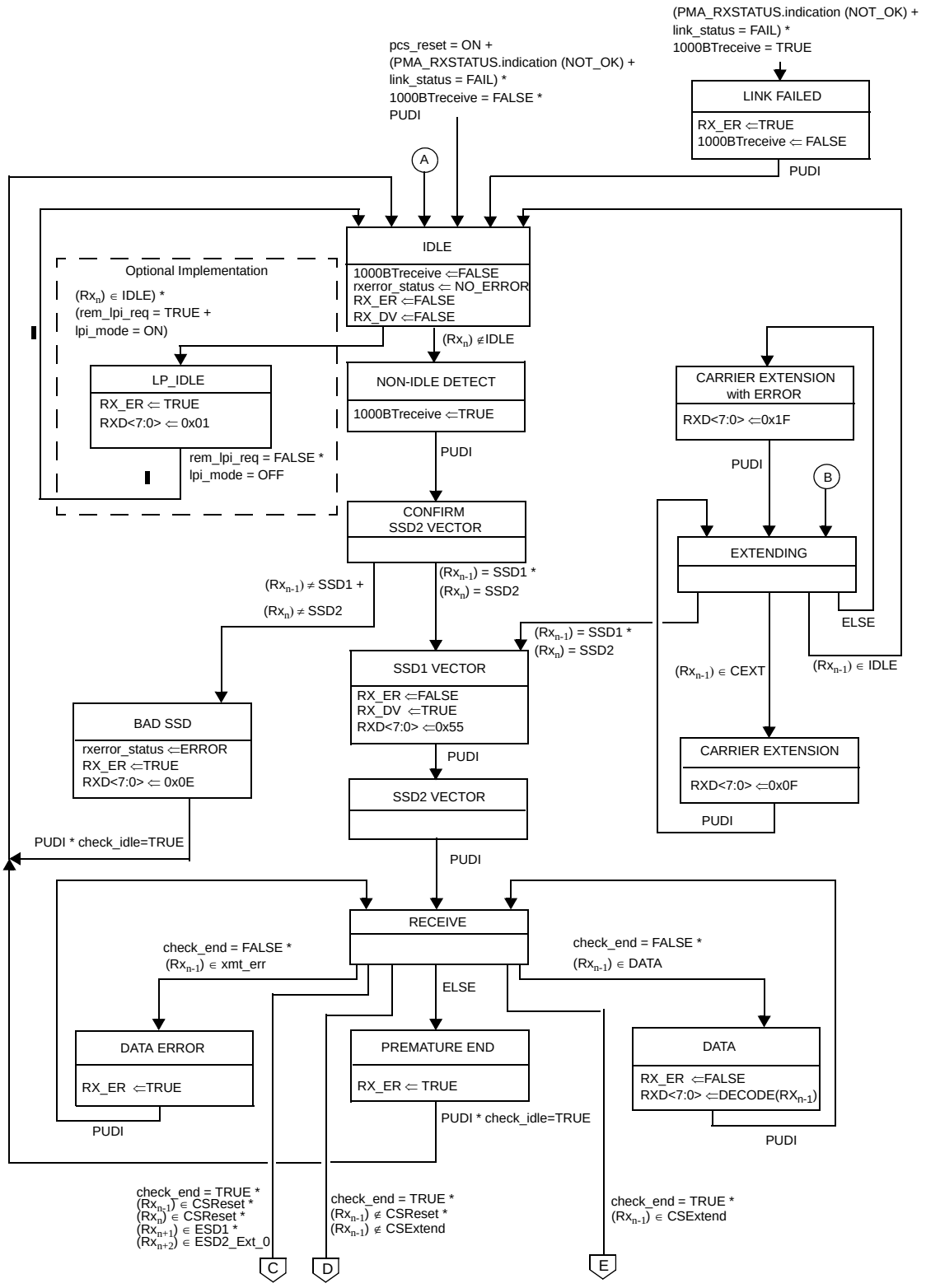
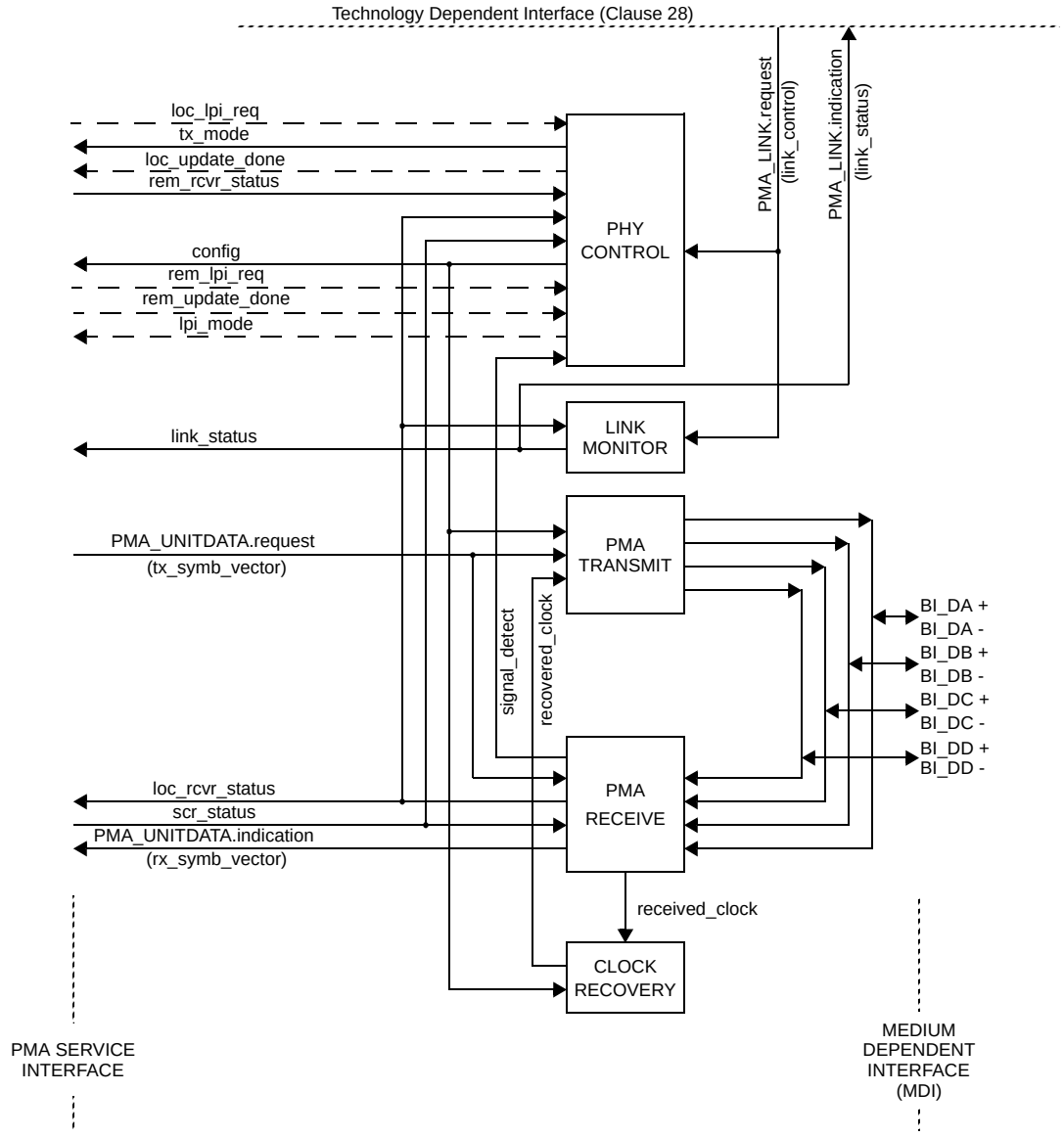


Figure 40–10a—PCS Receive state diagram, part a

40.4 Physical Medium Attachment (PMA) sublayer

40.4.2 PMA functions

Replace the existing PMA reference diagram (Figure 40-13) with the new PMA reference diagram Figure 40–14—:



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are optional.

Figure 40–14—PMA reference diagram

40.4.2.4 PHY Control function

Change the last sentence in the first paragraph of 40.4.2.4 as shown below:

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 40–15a and Figure 40–15b~~Figure 40-15~~.

Insert the following text before the last paragraph of 40.4.2.4 as shown below:

When the PHY supports Energy Efficient Ethernet, PHY Control will transition to a low power mode in response to concurrent requests for low power operation from the local PHY (loc_lpi_req = TRUE) and remote PHY (rem_lpi_req = TRUE).

Upon activation of the low power mode, the PHY Control asserts tx_mode = SEND_I for period of time defined by lpi_update_timer which allows the remote PHY to prepare for cessation of transmission. When lpi_update_timer expires, PHY Control transitions to the POST_UPDATE state, signals to the remote PHY that is has completed the update by setting loc_update_done = TRUE, and starts the lpi_postupdate_timer. When lpi_postupdate timer expires, PHY Control transitions to the WAIT_QUIET state. If there is a request to wake (loc_lpi_req = FALSE or rem_lpi_req = FALSE) while in the POST_UPDATE state, PHY Control will wait for confirmation that the remote PHY has completed the update (rem_update_done = TRUE) and is prepared for cessation of transmission before proceeding to the WAIT_QUIET state.

Upon entry into the WAIT_QUIET state, PHY Control asserts tx_mode = SEND_Z and transmission ceases. During the WAIT_QUIET and QUIET states, the PHY may deactivate transmit and receive functions in order to conserve energy. However, in the WAIT_QUIET state, the PHY shall be capable of correctly decoding rem_lpi_req. The PHY will remain in the QUIET state no longer than the time implied by lpi_quiet_timer.

When lpi_quiet_timer expires, the PHY intiates a wake sequence. The wake sequence begins with a transition to the WAKE state where the PHY will transmit (tx_mode = SEND_I) for period lpi_waketx_timer and simultaneously start a parallel timer, lpi_wakemz_timer. Since it is likely that transmit circuits were deactivated while in the QUIET state, this transmission is not expected to be compliant 1000BASE-T signaling, but rather of sufficient quality and duration to be detected by the remote PHY receiver and initiate the wake sequence in the remote PHY.

Upon expiration of lpi_waketx_timer, the PHY will enter the WAKE_SILENT state and cease transmission (tx_mode = SEND_Z). The PHY will remain in the WAKE_SILENT state until lpi_wakemz_timer has expired, at which point it is assumed transmitter circuits have stabilized and compliant 1000BASE-T signaling can be transmitted. At this point the MASTER transitions to the WAKE_TRAINING state and transmits to the SLAVE PHY.

The remaining wake sequence is essentially an accelerated training mode sequence leading to entry into the UPDATE state.

Once scrambler synchronization is acheived, the incoming value of rem_lpi_req can be determined. If low power operation is no longer requested by either the local or remote PHY, then both PHYs return to the SEND IDLE OR DATA state and the normal mode of operation (tx_mode = SEND_N). If both PHYs continue to request low power operation, then both PHYs remain in the UPDATE state and continue to transmit for time defined by lpi_update_timer. This time is intended to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If lpi_update_timer expires and both PHYs continue to request low power operation, then the PHY transitions to the POST_UPDATE state.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 40.3.1.1.

40.4.5 State variables

40.4.5.1 State diagram variables

Change definition of scr_status as shown:

scr_status

The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.

Values: OK: The descrambler has acheived synchronization.
NOT_OK: The descrambler is not synchronized. Note that when the PHY supports Energy Efficient Ethernet, when signal_detect is FALSE, scr_status is set to NOT_OK.

Insert the new variable definitions shown below in the exisiting variable list in alphabetical order:

loc_lpi_req

The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the low power mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this variable is set to FALSE.

Values: TRUE: "Assert low power idle" is present at the GMII.
FALSE: "Assert low power idle" is not present at the GMII.

loc_udpate_done

The loc_update_done variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has completed the update of its receiver state. It is passed to the PCS Transmit function via the PMA_UPDATE.indication primitive. When Energy Efficient Ethernet is not implemented, this value shall be set to FALSE.

Values: TRUE: The PHY has completed the current update.
FALSE: The PHY is ready for the next update or the current update is still in progress.

lpi_mode

The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered low power mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. When Energy Efficient Ethernet is not implemented, this variable shall be set to OFF.

Values: ON: The PHY is operating in low power mode.
OFF: The PHY is in normal operation.

rem_lpi_req

The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into low power mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this variable is set to FALSE.

Values: TRUE: Low power idle is encoded in the received symbols.
FALSE: Low power idle is not encoded in the received symbols.

rem_update_done

The rem_update_done variable is generated by the PCS Receive function and indicates whether or not the remote PHY is has completed the update of its receiver state. It is passed to the PMA PHY Control function via the PMA_REMUPDATE.request primitive. When Energy Efficient Ethernet is not implemented, this value shall be set to FALSE.

Values: TRUE: The remote PHY has completed the current update.
FALSE: The remote PHY is ready for the next update or the current update is still in progress.

signal_detect

The signal_detect variable is set by the PMA Receive function and indicates the presence of a signal at the MDI as defined in 40.6.1.3.5.

Values: TRUE: There is a signal present at the MDI.
FALSE: There is no signal present at the MDI.

40.4.5.2 Timers

Insert the following new timer definitions into the existing list in alphabetical order:

lpi_link_fail_timer

This timer defines the maximum time the PHY will allow between entry into the WAKE state and subsequent entry into the UPDATE or SEND IDLE OR DATA states before forcing the link to restart.

Values: The condition lpi_link_fail_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 90 μs and 110 μs.

lpi_postupdate_timer

This timer defines the maximum time the PHY will dwell in the POST_UPDATE state before proceeding to the WAIT_QUIET state.

Values: The condition lpi_postupdate_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 2.0 μs and 2.2 μs.

lpi_quiet_timer

This timer defines the maximum time the PHY will remain quiet before initiating transmission to refresh the remote PHY.

Values: The condition lpi_quiet_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 20 ms and 24 ms.

lpi_waitwq_timer

This timer defines the maximum time the PHY will dwell in the WAIT_QUIET state before forcing the link to restart.

Values: The condition lpi_waitwq_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 10 μs and 12 μs.

lpi_wake_timer

This timer defines the expected time for the PHY to transition from low power mode to normal operation.

Values: The condition lpi_wake_timer_done becomes true upon timer expiration. For each transition of lpi_wake_timer_done from false to true, the wake error counter (refer to 40.5.1.1) shall be incremented.
Duration: This timer is shall have a period of 16 μs.

lpi_waketx_timer

This timer defines the time the PHY will transmit to ensure detection by the remote PHY receiver and trigger an exit from the low power state.

Values: The condition lpi_waketx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between1.2 μs and 1.4 μs.

lpi_wakemz_timer

This timer defines the time allowed for the PHY transmitter to acheive compliant operation following activation.

Values: The condition lpi_wakemz_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period of 5 µs.

lpi_update_timer

This timer defines the time the PHY will transmit to facilitate a refresh of the remote PHY receiver.

Values: The condition lpi_update_timer_done becomes true upon timer expiration.
Duration: For a PHY configured as the MASTER, this timer shall have a period between 0.23 ms and 0.25 ms. For a PHY configured as the SLAVE, this timer shall have a period between 0.18 ms and 0.20 ms.

40.4.6 State Diagrams

40.4.6.1 PHY Control state diagram

Replace existing PHY Control state diagram (Figure 40-15) with new PHY Control state diagram, part a labled Figure 40–15a

Also insert new PHY control state diagram (Phy Control state diagram, part b labled Figure 40–15b) after Phy Control state diagram part a.

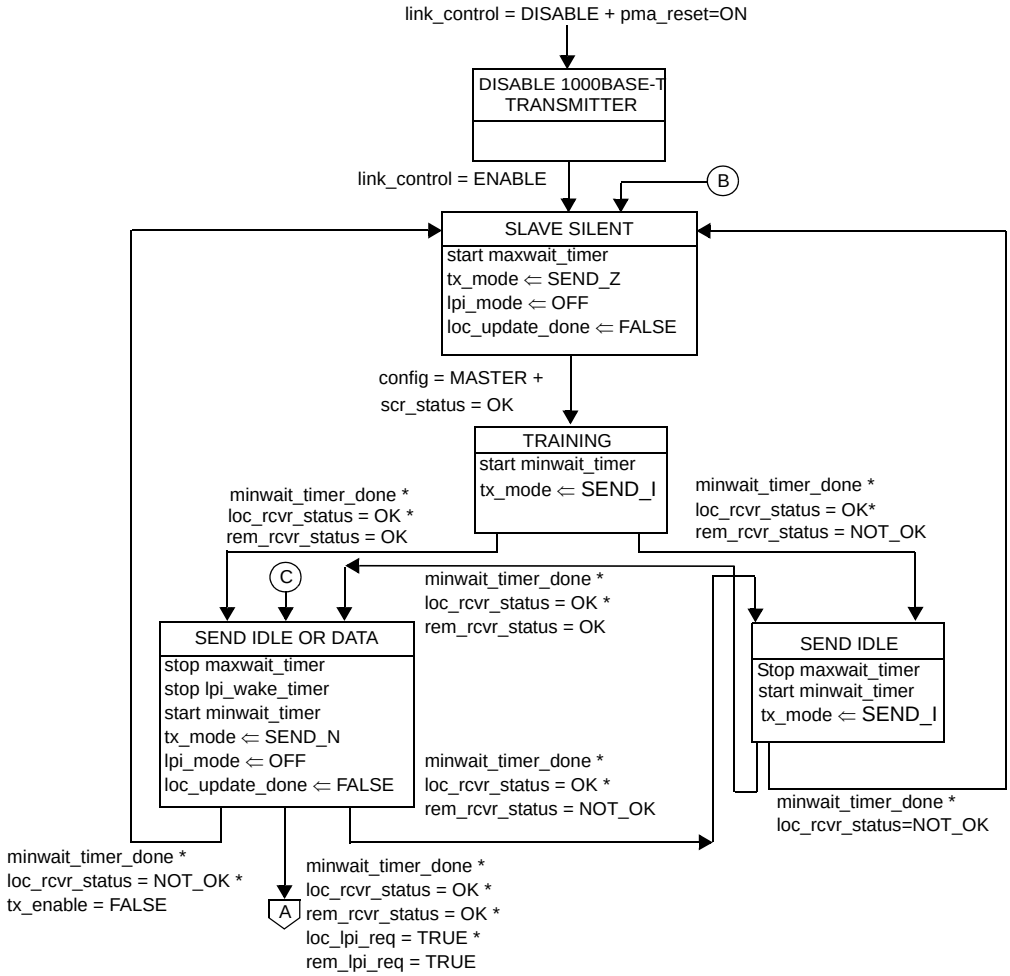


Figure 40–15a—PHY Control state diagram, part a

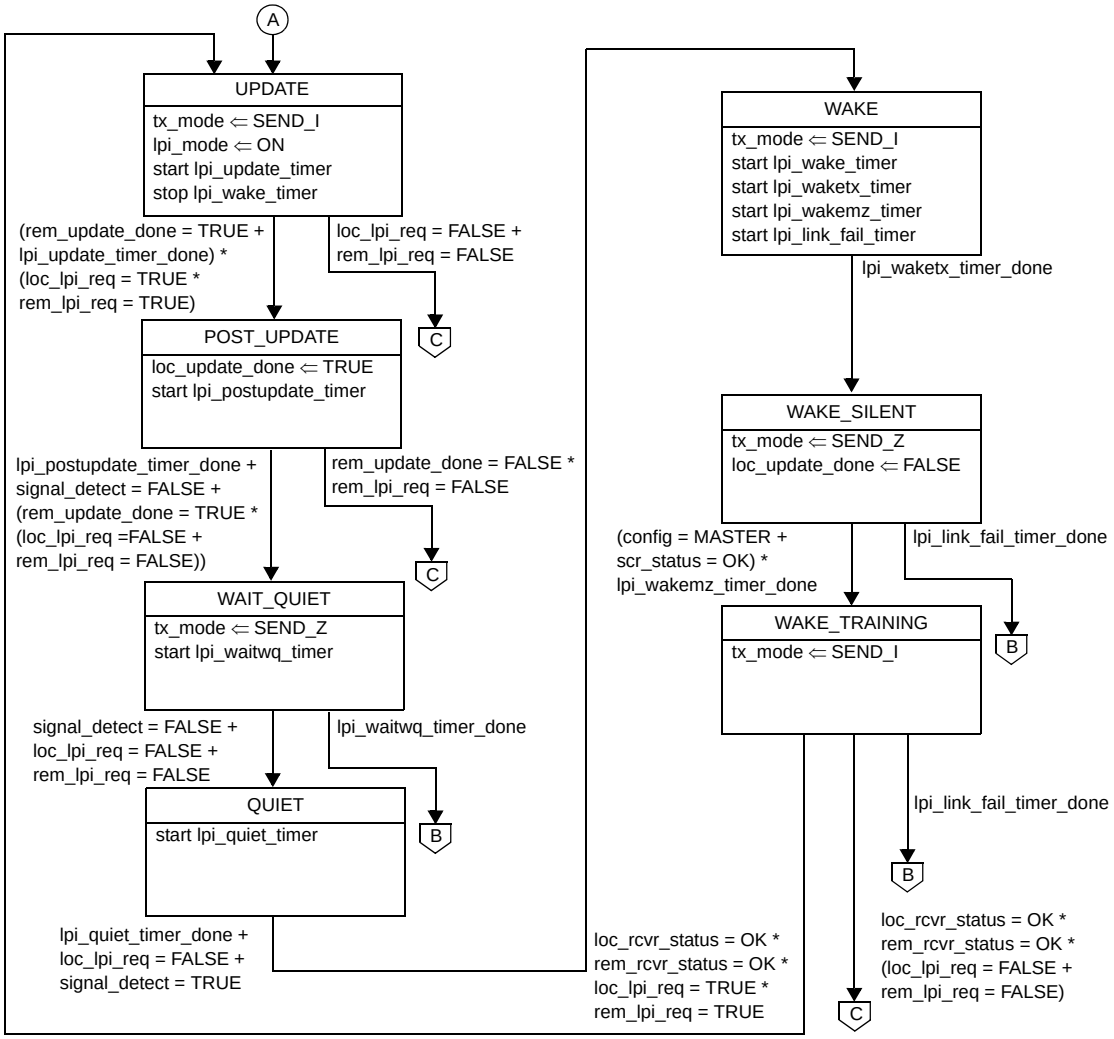
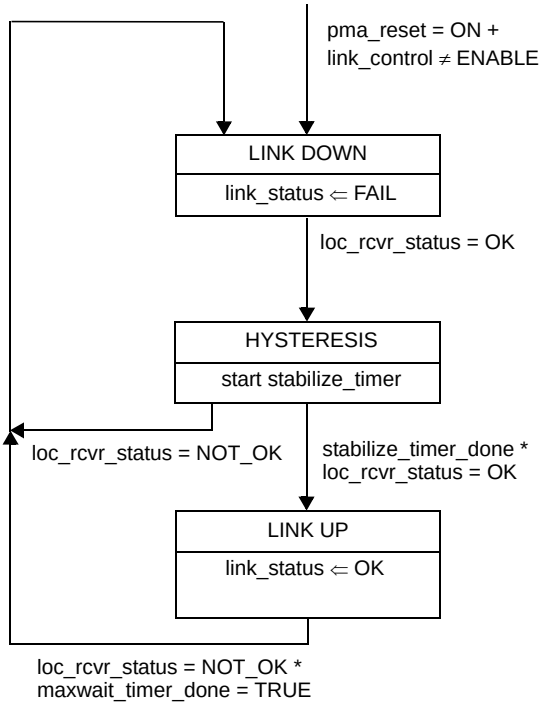


Figure 40–15b—PHY Control state diagram, part b (optional)

40.4.6.2 Link Monitor state diagram

Change Figure reference in NOTE 1 of the Link Monitor state diagram to point to new Phy Control state diagram part a (*Figure 40–15a****):***



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 40–15a).
NOTE 2—The variables link_control and link_status are designated as link_control_(1GigT) and link_status_(1GigT), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 40–16—Link Monitor state diagram

40.5 Management interface

1000BASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28).

40.5.1 Support for Auto-Negotiation

Insert the following below bullet item b):

c) To negotiate Energy Efficient Ethernet capabilities as specified in 28C.12.

40.5.1.1 1000BASE-T use of registers during Auto-Negotiation

A 1000BASE-T PHY shall use the management register definitions and values specified in Table 40–3.

Insert rows in Table 40–3 following Register 15, "Extended status register " as shown:

Table 40–3—1000BASE-T Registers

Register	Bit	Name	Description	Type[a]
15	15.15:12	Extended status register	See 22.2.4.4	RO
3.0[b]	3.0.10	Clock stoppable	Defined in 45.2.3.1.3a. A 1000BASE-T PHY that supports EEE may stop the derived GMII receive clock while it is signaling low power idle in the receive direction. If this bit is set to 1 then the PHY may stop the receive GMII clock while it is signaling low power idle otherwise it keeps the clock active.	R/W
3.1	3.1.11	Transmit low power idle received	Defined in 45.2.3.2.1a.	RO/LH
3.1	3.1.10	Receive low power idle received	Defined in 45.2.3.2.1b.	RO/LH
3.1	3.1.9	Transmit low power idle indication	Defined in 45.2.3.2.1c.	RO
3.1	3.1.8	Receive low power idle indication	Defined in 45.2.3.2.1d.	RO
3.20	3.20.2	1000BASE-T EEE supported	If the local device supports EEE operation for 1000BASE-T, this bit is set to 1.	RO
3.22	3.22.15:0	1000BASE-T wake error counter	This counter is incremented for each transition of lpi_wake_timer_done from FALSE to TRUE (refer to 40.4.5.2).	RO, NR
7.60	7.60.2	1000BASE-T EEE advertisement	If the local device supports EEE operation for 1000BASE-T and EEE operation is desired, this bit is set to 1	R/W
7.61	7.61.2	LP 1000BASE-T EEE advertisement	If the link partner supports EEE operation for 1000BASE-T and EEE operation is desired, this bit is set to 1	RO

[a] R/W = Read/Write, RO = Read only, SC = Self-clearing, LH = Latch High
[b] This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

40.5.1.2 1000BASE-T Auto-Negotiation page use

1000BASE-T PHYs shall exchange one Auto-Negotiation base page, a 1000BASE-T formatted next page, and two 1000BASE-T unformatted next pages in sequence, without interruption, as specified in Table 40–4. Additional next pages can be exchanged as described in Annex 40C.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 1000BASE-T message page exchange.

Insert rows in Table 40–4 following "PAGE 2 (Unformatted next page)" as shown:

Insert the following subclause after 46.6.1.2.6:

40.6.1.2.7 Transmitter operation during WAKE

When the PHY supports Energy Efficient Ethernet, it is required to transmit a signal to wake the remote PHY upon entry into the WAKE state (refer to the PHY Control state diagram, Figure 40–15b). This signal

Table 40–4—1000BASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
PAGE 2 (Unformatted next page)		
U10	1000BASE-T MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value (10:0)
U9	1000BASE-T MASTER-SLAVE Seed Bit 9 (SB9)	
U8	1000BASE-T MASTER-SLAVE Seed Bit 8 (SB8)	
U7	1000BASE-T MASTER-SLAVE Seed Bit 7 (SB7)	
U6	1000BASE-T MASTER-SLAVE Seed Bit 6 (SB6)	
U5	1000BASE-T MASTER-SLAVE Seed Bit 5 (SB5)	
U4	1000BASE-T MASTER-SLAVE Seed Bit 4 (SB4)	
U3	1000BASE-T MASTER-SLAVE Seed Bit 3 (SB3)	
U2	1000BASE-T MASTER-SLAVE Seed Bit 2 (SB2)	
U1	1000BASE-T MASTER-SLAVE Seed Bit 1 (SB1)	
U0	1000BASE-T MASTER-SLAVE Seed Bit 0 (SB0)	
PAGE 3 (Unformatted next page)		
U10:U3	As specified in 45.2.7.13a.	
U2	1000BASE-T EEE (1 = EEE is supported for 1000BASE-T, 0 = EEE is not supported for 1000BASE-T)	Management register 7.60.2[a]
U1:U0	As specified in 45.2.7.13a.	
PAGE 4 (Unformatted next page)		
U10:U0	As specified in 45.2.7.15a.	

[a]This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

may be transmitted during reactivation of the PHY analog front-end and is not guaranteed or intended to be a compliant idle signal.

The wake signal shall be between 50 and 75% of the nominal idle levels with a symbols ratio within 10% of a nominal idle signal. These requirements shall be met within 700 ns following entry into the WAKE state.

The PHY shall acheive compliant operation within lpi_wakemz_timer, as defined in 40.4.5.2.

Insert the following subclause after 46.6.1.3.4:

40.6.1.3.5 Signal_detect

When the PHY supports Energy Efficient Ethernet, the PMA Receive function shall convey an indicator of signal presense, referred to as signal_detect, to the PMA PHY Control function. The value of signal_detect shall be set to TRUE within 0.5 µs of the receipt of a wake signal meeting the requirements of 46.6.1.2.7. The value of signal_detect shall be set to FALSE within 0.5 µs of the receipt of a continuous sequence of zeros.

40.12 Protocol implementation conformance statement (PICS) proforma for Clause 40—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 1000BASE-T[1]

40.12.2 Major capabilities/options

Insert *EEE option into the table as follows;

Item	Feature	Subclause	Status	Support	Value/Comment
*EEE	Energy Efficient Ethernet	40.1.3	O	Yes [ ] No [ ]	

40.12.4 Physical Coding Sublayer (PCS)

Insert PCT18 and PCT19 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PCT18	PCS Local LPI Request function	40.3.1.6	EEE:M	Yes [ ]	The PCS shall conform to the Local LPI Request state diagram as depicted in Figure 40–9 including compliance with the associated state variables specified in 40.3.3.
PCT19	loc_lpi_req	40.3.3.1	!EEE:M	Yes [ ]	When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE

40.12.4.1 PCS receive functions

Insert PCR5 and PCR6 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PCR5	rem_lpi_req	40.3.3.1	!EEE:M	Yes [ ]	When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE.

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

40.12.5 Physical Medium Attachment (PMA)

Insert PMF24 through PMF32 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PMF24	Energy Efficient Ethernet PHY Control extensions	40.4.2.4	EEE:M	Yes [ ]	PHY Control shall comply with the state diagram description given in Figure 40–15a and Figure 40–15b.
PMF25	Decoding of rem_lpi_req and in the WAIT_QUIET state	40.4.2.4	EEE:M	Yes [ ]	In the WAIT_QUIET state, the PHY shall be capable of correctly decoding rem_lpi_req.
PMF26	loc_update_done	40.4.5.1	EEE:M	Yes [ ]	When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE.
PMF27	lpi_mode	40.4.5.1	EEE:M	Yes [ ]	When Energy Efficient Ethernet is not implemented, this variable shall be set to OFF.
PMF28	rem_update_done	40.4.5.1	EEE:M	Yes [ ]	When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE.
PMF29	lpi_link_fail_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period between 90 μs and 110 μs.
PMF30	lpi_postupdate_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period between 2.0 μs and 2.2 μs.
PMF31	lpi_quiet_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period between 20 ms and 24 ms.
PMF32	lpi_waitwq_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period between 10 μs and 12 μs.
PMF33	1000BASE-T wake error counter	40.4.5.2	EEE:M	Yes [ ]	For each transition of lpi_wake_timer_done from false to true, the wake error counter shall be incremented.
PMF34	lpi_wake_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period of 16 μs.
PMF35	lpi_waketx_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period between 1.2 μs and 1.4 μs.
PMF36	lpi_wakemz_timer	40.4.5.2	EEE:M	Yes [ ]	This timer shall have a period of 5 μs.
PMF37	lpi_update_timer	40.4.5.2	EEE:M	Yes [ ]	For a PHY configured as the MASTER, this timer shall have a period between 0.23 ms and 0.25 ms. For a PHY configured as the SLAVE, this timer shall have a period between 0.18 ms and 0.20 ms.

40.12.6 PMA Electrical Specifications

Insert PME71 through PME75 as shown:

Item	Feature	Subclause	Status	Support	Value/Comment
PME71	Transmitter operation during WAKE	40.6.1.2.7	EEE:M	Yes [ ]	The wake signal shall be between 50 and 75% of the nominal idle levels with a symbols ratio within 10% of a nominal idle signal. These requirements shall be met within 700 ns following entry into the WAKE state.
PME72	Acheive compliant operation following WAKE.	40.6.1.2.7	EEE:M	Yes [ ]	The PHY shall acheive compliant operation within lpi_wakemz_timer, as defined in 40.4.5.2.
PME73	Signal presence indicator	40.6.1.3.5	EEE:M	Yes [ ]	PMA Receive function shall convey an indicator of signal presense, referred to as signal_detect, to the PMA PHY Control function.
PME74	Assertion of signal_detect	40.6.1.3.5	EEE:M	Yes [ ]	The value of signal_detect shall be set to TRUE within 0.5 µs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7.
PME75	De-assertion of signal_detect	40.6.1.3.5	EEE:M	Yes [ ]	The value of signal_detect shall be set to FALSE within 0.5 µs of the receipt of a continuous sequence of zeros.

Revisions to IEEE Std 802.3-2008, Clause 45

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.

45. Management Data Input/Output (MDIO) Interface

Editors' Notes: *To be removed prior to publication.*
Insert new registers, or add bits to existing registers, or add new tables, for new PMA/PMD, PCS, and Auto-Neg for EEE operation.

Editors' Notes: *To be removed prior to publication.*
There are no changes to PMA registers at present, this not is a placeholder.

45.2.3 PCS registers

Change Table 45-82 to add EEE capability register:

Table 45–1—PCS registers

Register address	Register name	Clause
3.20	EEE capability register	TBD
3.21	EEE reduced energy capability register	TBD

45.2.3.1 PCS control 1 register (Register 3.0)

Change Table 45-83 for LPI clock control:

Table 45–2—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.12	Reserved	Value always 0, writes ignored	R/W
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10	Clock stoppable	1 = Clock stoppable during LPI 0 = Clock not stoppable	R/W
3.0.~~10~~9:7	Reserved	Value always 0, writes ignored	R/W
3.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self-clearing

Insert 45.2.3.1.3a as follows:

45.2.3.1.3a Clock stoppable (3.0.10)

A PHY that supports low power idle signaling may stop the derived xMII receive clock while it is signaling low power idle in the receive direction. Similarly the MAC may stop the xMII transmit clock while it is asserting low power idle in the transmit direction. If bit 3.0.10 is set to 1 then the PHY may stop the receive xMII clock while it is signaling low power idle otherwise it shall keep the clock active. Also if this bit is set, the MAC may stop the transmit xMII clock while it is asserting low power idle. If the PHY does not support

low power idle signaling or is not able to stop the receive clock then this bit has no effect (see 22.2.2.9a, 35.2.2.9a, 46.3.2.4a).

45.2.3.2 PCS status 1 register (Register 3.1)

Change Table 45-84 for LPI status:

.

Table 45–84—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:~~8~~12	Reserved	Ignore when read	RO
3.1.11	Tx LP idle received	1 = Tx PCS has received LP idle 0 = LP Idle not received	RO/LH
3.1.10	Rx LP idle received	1 = Rx PCS has received LP idle 0 = LP Idle not received	RO/LH
3.1.9	Tx LP idle indication	1 = Tx PPCS is currently receiving LP idle 0 = PCS is not currently receiving LP idle	RO
3.1.8	Rx LP idle indication	1 = Rx PCS is currently receiving LP idle 0 = PCS is not currently receiving LP idle	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6:3	Reserved	Ignore when read	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Ignore when read	RO

[a]RO = Read only, LL = Latching low

Insert 45.2.3.2.1a, b, c and d as follows:

45.2.3.2.1a Transmit low power idle received (3.1.11)

When read as a one, bit 3.1.11 indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. When read as a zero, bit 3.1.11 indicates that the PCS has not received low power idle signaling. This bit shall be implemented with latching high behavior.

45.2.3.2.1b Receive low power idle received (3.1.10)

When read as a one, bit 3.1.10 indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. When read as a zero, bit 3.1.10 indicates that the PCS has not received low power idle signaling. This bit shall be implemented with latching high behavior.

45.2.3.2.1c Transmit low power idle indication (3.1.9)

When read as a one, bit 3.1.9 indicates that the transmit PCS is currently receiving low power idle signals. When read as a zero, bit 3.1.9 indicates that the PCS is not currently receiving low power idle signals. The behavior if read during a state transition is undefined.

45.2.3.2.1d Receive low power idle indication (3.1.8)

When read as a one, bit 3.1.8 indicates that the receive PCS is currently receiving low power idle signals. When read as a zero, bit 3.1.8 indicates that the PCS is not currently receiving low power idle signals. The behavior if read during a state transition is undefined.

Insert 45.2.3.9a and b as follows:

45.2.3.9a EEE capability (Register 3.20)

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE capability register is shown in Table 45–88a.

Table 45–88a—EEE capability register (Register 3.20) bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15:7	Reserved	Ignore on read	RO
3.20.6	10GBASE-KR EEE	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	RO
3.20.5	10GBASE-KX4 EEE	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	RO
3.20.4	1000BASE-KX EEE	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	RO
3.20.3	10GBASE-T EEE	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	RO
3.20.2	1000BASE-T EEE	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	RO
3.20.1	100BASE-TX EEE	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	RO
3.20.0	Reserved	Ignore on read	RO

[a] RO = Read only

45.2.3.9a.1 10GBASE-KR EEE supported (3.20.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.3a this bit shall be set to 1.

45.2.3.9a.2 10GBASE-KX4 EEE supported (3.20.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.3a this bit shall be set to 1.

45.2.3.9a.3 1000BASE-KX EEE supported (3.20.4)

If the device supports EEE operation for 1000BASE-KX as defined in TBD this bit shall be set to 1.

45.2.3.9a.4 10GBASE-T EEE supported (3.20.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3 this bit shall be set to 1.

45.2.3.9a.5 1000BASE-T EEE supported (3.20.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.2.11 this bit shall be set to 1.

45.2.3.9a.6 100BASE-TX EEE supported (3.20.1)

If the device supports EEE operation for 100BASE-TX as defined in 25.4.11 this bit shall be set to 1.

45.2.7 Auto-Negotiation registers

Change Table 45-133 for EEE AN registers:

.

Table 45–133— Auto-Negotiation MMD registers

Register address	Register name
~~7.49 through 7.32 767~~	~~Reserved~~
7.49 through 7.59	Reserved
7.60	EEE advertisement
7.61	EEE LP advertisement
7.62, 7.63	Reserved
7.64	EEE backplane timer mode
7.65	EEE LP backplane timer mode
7.66 through 7.32 767	Reserved

Insert 45.2.7.13a through 45.2.7.16a for register definitions:

45.2.7.13a EEE advertisement (Register 7.60)

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code as defined in 28C.12. The 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to the bits in the unformatted next page. For PHYs that negotiate extended next page support the

11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to bits U10 to U0 respectively of the extended next page unformatted code field. The assignment of bits in the EEE advertisement register is shown in Table 45–145.

Table 45–145—EEE advertisement register (Register 7.60) bit definitions

Bit(s)	Name	Description	R/W[a]
7.60.15:7	Reserved	Ignore on read	RO
7.60.6	10GBASE-KR EEE	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	R/W
7.60.5	10GBASE-KX4 EEE	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	R/W
7.60.4	1000BASE-KX EEE	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	R/W
7.60.3	10GBASE-T EEE	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	R/W
7.60.2	1000BASE-T EEE	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	R/W
7.60.1	100BASE-TX EEE	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	R/W
7.60.0	Reserved	Ignore on read	RO

[a]R/W = Read/Write, RO = Read only

45.2.7.13a.1 10GBASE-KR EEE supported (7.60.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.3a, and EEE operation is desired, this bit shall be set to 1.

45.2.7.13a.2 10GBASE-KX4 EEE supported (7.60.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.3a, and EEE operation is desired, this bit shall be set to 1.

45.2.7.13a.3 1000BASE-KX EEE supported (7.60.4)

If the device supports EEE operation for 1000BASE-KX as defined in TBD70.3, and EEE operation is desired, this bit shall be set to 1.

45.2.7.13a.4 10GBASE-T EEE supported (7.60.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3, and EEE operation is desired, this bit shall be set to 1.

45.2.7.13a.5 1000BASE-T EEE supported (7.60.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.2.11, and EEE operation is desired, this bit shall be set to 1.

45.2.7.13a.6 100BASE-TX EEE supported (7.60.1)

If the device supports EEE operation for 100BASE-TX as defined in 25.4.11, and EEE operation is desired, this bit shall be set to 1.

45.2.7.14a EEE link partner advertisement (Register 7.61)

All of the bits in the EEE LP advertisement register are read only. A write to the EEE LP advertisement register shall have no effect. When the AN process has been completed, this register shall reflect the contents of th link partner's EEE advertisement register. The definitions are the same as for the EEE advertisement register (45.2.7.13a).

45.2.7.15a EEE backplane timer mode (Register 7.64)

This register defines the EEE backplane mode control that is sent in the unformatted next page following the EEE technology message code as defined in 28C.12 and the EEE advertisement. The 12 (7.64.11 to 7.64.0) bits in the EEE backplane timer mode register correspond to the bits in the unformatted next page. The assignment of bits in the EEE backplane timer mode register is shown in Table 45–146.

Table 45–146—EEE backplane timer mode register (Register 7.64) bit definitions

Bit(s)	Name	Description	R/W[a]
7.64.15:12	Reserved	Ignore on read	RO
7.64.11:8	10GBASE-KR wake timer	4 through F - reserved 3 = 40 training frames 2 = 35 training frames 1 = 30 training frames 0 = 26 training frames	R/W
7.64.7:4	10GBASE-KX4 wake timer	4 through F - reserved 3 = 18μs 2 = 15μs 1 = 11μs 0 = 8μs	R/W
7.64.3:0	1000BASE-KX wake timer	4 through F - reserved 3 = 20μs 2 = 17μs 1 = 13μs 0 = 10μs	R/W

[a]R/W = Read/Write, RO = Read only

45.2.7.15a.1 10GBASE-KR local Tw (7.64.11:8)

For 10GBASE-KR, the local device advertises the smallest wakeup time (Tw) that the PHY can support. This is compared with the link partner's advertised value and resolves to the largest of the two. The resolved Tw is used as the variable lpi_wake_timer (see 40.4.5.2).

45.2.7.15a.2 10GBASE-KX4 local Tw (7.64.8:4)

For 10GBASE-KX4, the local device advertises the smallest wakeup time (Tw) that the PHY can support. This is compared with the link partner's advertised value and resolves to the largest of the two. The resolved Tw is used as the variable lpi_wake_timer (see 40.4.5.2).

45.2.7.15a.3 1000BASE-KX local Tw (7.64.3:0)

For 1000BASE-KX, the local device advertises the smallest wakeup time (Tw) that the PHY can support. This is compared with the link partner's advertised value and resolves to the largest of the two. The resolved Tw is used as the variable lpi_wake_timer (see 40.4.5.2).

45.2.7.15b EEE link partner backplane timer mode (Register 7.65)

All of the bits in the EEE LP backplane timer mode register are read only. A write to the EEE LP backplane timer mode register shall have no effect. When the AN process has been completed, this register shall reflect the contents of the link partner's EEE backplane timer mode register. The definitions are the same as for the EEE backplane timer mode register (45.2.7.15a).

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface[1]

[Editor's note (to be removed prior to publication) - Insert corresponding PICS, for new PMA/PMD, PCS, and Auto-Neg for EEE]

Add the following rows into table 45.5.3.7:

45.5.3.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM30a	EEE capability indicated for each port type	45.2.3.9a		M	Yes [ ] N/A [ ]
RM30b	EEE reduced energy capability indicated for each port type	45.2.3.9b		M	Yes [ ] N/A [ ]

Add the following rows into table 45.5.3.9:

45.5.3.9 Auto-Negotiation management functions

Item	Feature	Subclause	Value/Comment	Status	Support
AM58	EEE capability in advertisement register for each port type	45.2.7.13a		AN:M	Yes [ ] N/A [ ]
AM59	EEE LP advertisement register reflects link partner's capabilities	45.2.7.14a		AN:M	Yes [ ] N/A [ ]
AM60	Writes to EEE LP advertisement register have no effect	45.2.7.14a		AN:M	Yes [ ] N/A [ ]
AM61	EEE mode control register operates as specified	45.2.7.15a		AN:M	Yes [ ] N/A [ ]
AM62	EEE LP mode control register reflects link partner's mode control register	45.2.7.15b		AN:M	Yes [ ] N/A [ ]
AM63	Writes to EEE LP mode control register have no effect	45.2.7.15b		AN:M	Yes [ ] N/A [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 46

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.

46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII))

Editors' Notes: *To be removed prior to publication.*
changes to GMII interface for EEE operation.

Change 46.1.1 for major concepts (add item h at he end of the list) :

h) The XGMII may also support low power idle signaling as defined for Energy Efficient Ethernet for some PHY types (see Clause 78).

Change 46.1.7 for LPI function:

46.1.7 Mapping of XGMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the XGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 10 Gb/s; therefore, PLSservice primitives supporting CSMA/CD operation are not mapped through the RS to the XGMII. The mapping changes slightly when Low Power Idle signaling is in operation. This behavior and restrictions are the same as described in 22.7a, with the details of the signaling described in 46.3.

Mappings for the following primitives are defined for 10 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

Change 46.3 to show LPI signaling:

46.3 XGMII functional specifications

Add NOTE in 46.3.1.1 for clock definitions:

NOTE—TX_CLK may be halted during periods of low utilization according to 46.3.1.5a.

Change NOTE in 46.3.2.1 for clock definitions:

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. RX_CLK may be halted during periods of low utilization according to 46.3.2.4a.

Change 46.3.1.2 for TXC<3:0> definition:

46.3.1.2 TXC<3:0> (transmit control)

TXC<3:0> indicate that the RS is presenting either data or control characters on the XGMII for transmission. The TXC signal for a lane shall be de-asserted when a data octet is being sent on the corresponding lane and asserted when a control character is being sent. In the absence of errors, the TXC signals are de-asserted by the RS for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be transmitted are presented on the lanes of the XGMII. TXC<3:0> are driven by the RS and shall transition synchronously with respect to both the rising and falling

edges of TX_CLK. Table 46–3 specifies the permissible encodings of TXD and TXC for a XGMII transmit lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Table 46–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
~~1~~	~~00 through 06~~	~~Reserved~~	~~—~~
1	00 through 05	Reserved	—
1	06	assert low power idle (in all lanes)	No applicable parameter (Normal inter-frame)
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, replaces first eight ZERO, ONE of a frame (preamble octet)
1	FC	Reserved	—
1	FD	Terminate	DATA_COMPLETE
1	FE	Transmit error propagation	No applicable parameter
1	FF	Reserved	—

NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).

The PHY shall interpret the combination of TXC and TXD as shown in Table 46–3 as an assertion of low power idle. Transition into and out of the low power idle state is shown in Figure 46–7a.

Insert 46.3.1.5a for transmit low power idle transition:

46.3.1.5a Transmit direction low power idle transition

The MAC device asserts that it wishes the PHY to transition to the low power idle state by asserting TXC and setting TXD<7:0> to 06 (in all lanes). The MAC device maintains the same state for these signals for the entire time that it wishes the PHY to remain in the low power idle state.

The MAC device may halt TX_CLK at any time more than 128 clock cycles after the start of the low power idle state as shown in Figure 46–7a if and only if the clock stoppable bit is asserted [45.2.3.1.3a].

The MAC device deasserts TXC and asserts IDLE on lanes 0-3 in order to make the PHY transition out of the low power idle state. The MAC device should not present a start code for valid transmit data until after the wake up time specified for the PHY.

Figure 46–7a shows the behavior of TXC and TXD<7:0> during the transition into and out of the low power idle state..

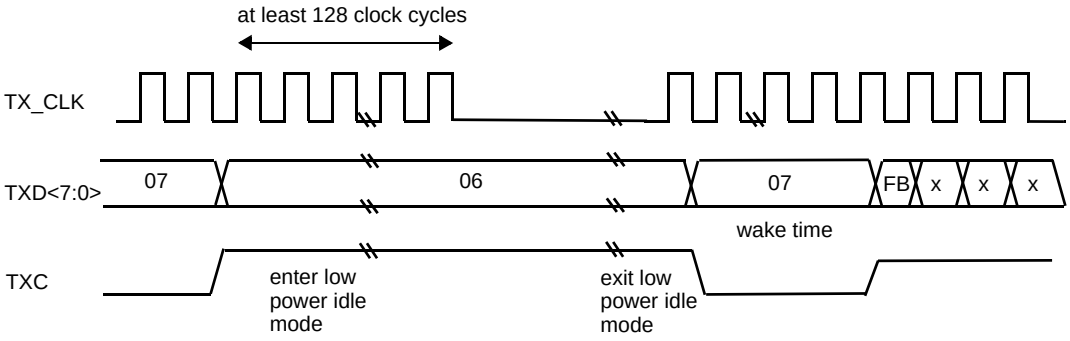


Figure 46–7a—Low power idle transition

Table 46–3 summarizes the permissible encodings of TXD<31:0>, TXC<3:0>.

Change 46.3.2.2 for RXC definition:

46.3.2.2 RXC<3:0> (receive control)

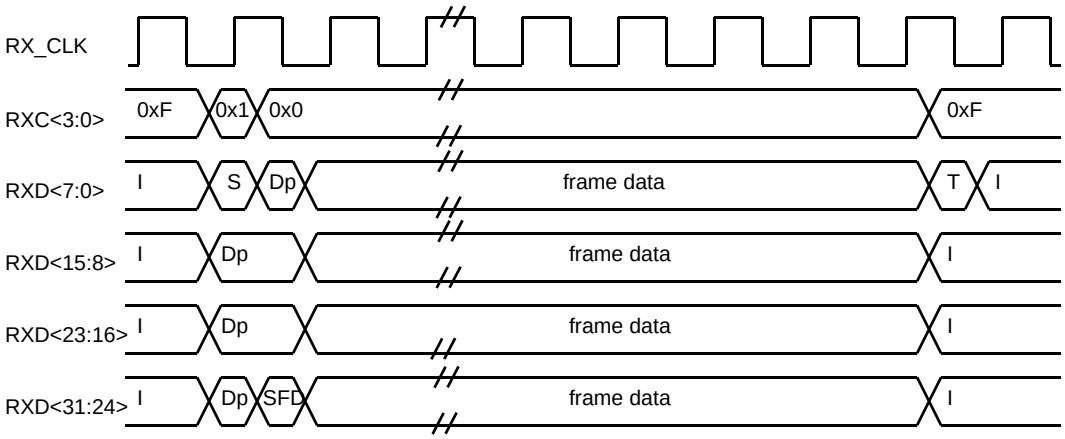
RXC<3:0> indicate that the PHY is presenting either recovered and decoded data or control characters on the XGMII. The RXC signal for a lane shall be de-asserted when a data octet is being received on the corresponding lane and asserted when a control character is being received. In the absence of errors, the RXC signals are de-asserted by the PHY for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be received are presented on the lanes of the XGMII. RXC<3:0> are driven by the PHY and shall transition synchronously with respect to both the rising and falling edges of RX_CLK. Table 46–4 specifies the permissible encodings of RXD and RXC for a XGMII receive lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Figure 46–7 shows the behavior of RXC<3:0> during an example frame reception with no errors.

Table 46–4—Permissible lane encodings of RXD and RXC

RXC	RXD	Description	PLS_DATA.indication parameter
0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
~~1~~	~~00 through 06~~	~~Reserved~~	~~—~~
1	00 through 05	Reserved	—
1	06	assert low power idle (in all lanes)	No applicable parameter (Normal inter-frame)
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, replaces first eight ZERO, ONE of a frame (a pre-amble octet)
1	FC	Reserved	—
1	FD	Terminate	No applicable parameter (Start of inter-frame)
1	FE	Receive error	No applicable parameter
1	FF	Reserved	—

NOTE—Values in RXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–7—~~Basic f~~Frame reception without error

Insert 45.3.2.4a for receive low power idle transition:

46.3.2.4a Receive direction low power idle transition

When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the MAC device by asserting RXC and setting RXD<7:0> to 06 (in all lanes). The PHY maintains these signals in this state while it remains in the low power idle state. When the PHY receives signals from the link partner to indicate transition out of the low power idle state it indicates this to the MAC device by deasserting RXC and returning to a normal inter-frame state.

The PHY may halt RX_CLK at any time more than 128 clock cycles after the start of the low power idle state as shown in Figure 46–8a if and only if the clock stoppable bit is asserted [45.2.3.1.3a].

Figure 46–8a shows the behavior of RXC and RXD<7:0> during low power idle transitions.

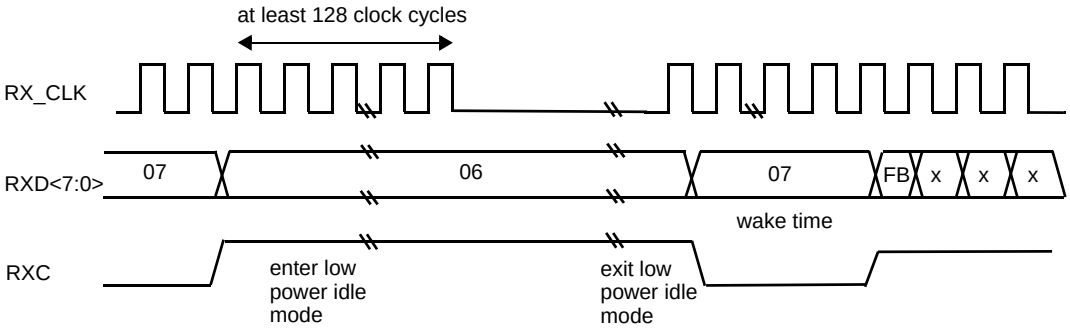


Figure 46–8a—Low power idle transition

46.5 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[1]

[Editor's note (to be removed prior to publication) - changes and additions to PICS for LPI]

Add the following row into table 46.5.2.3:

46.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	46.1.7		O	Yes [ ] No [ ]

Add the new subclause 46.5.3.3a for LPI functions:

46.5.3.3a Low power idle functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI as defined in Table 46–3	46.3.1.2		LPI:M	Yes [ ] N/A [ ]
L2	TX_CLK stoppable during LPI	46.3.1.5a	At least 128 cycles after LPI assertion	LPI:O	Yes [ ] N/A [ ]
L3	RX_CLK stoppable during LPI	46.3.2.4a		LPI:O	Yes [ ] N/A [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 48

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 1.1, December 2008	The decision to adopt a consistent architectural model for Low Power Idle operation (see Motion #5 from the Nov 2008 meeting) across all PHYs and several issues with implementing this for backplane PHYs without violating the layering model let us to a decision to move some material from the backplane Clauses (70, 71, 72) to the 1000BASE-X (36), 10GBASE-T (48) and 10GBASE-R (49) clauses. See koenen_01_1108.pdf and healey_02_1108.pdf for more background on this. This is a substantial change and the editors suggest it be reviewed carefully.

48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X)

Editors' Notes: *To be removed prior to publication.*
changes to XAUI interface and BASE-X encoding for EEE operation.

Change 48.2.3 for LPI code groups

48.2.3 Use of code-groups

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 36.2.4. A 10GBASE-X PCS shall meet the requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. PCS lanes are independent of one another. All code-group rules specified in 36.2.4 are applicable to each lane. The mapping of XGMII characters to PCS code-groups is specified in Table 48–2. The mapping of PCS code-groups to XGMII characters is specified in Table 48–3. The ability to transmit or receive Low Power Idle is an option for certain PHYs to support Energy Efficient Ethernet (see Clause 78).

Figure 48–3 illustrates the mapping of an example XGMII character stream into a PCS code-group stream. Figure 48-3a illustrates the mapping during Low Power Idle.

The relationship of code-group bit positions to XGMII, PCS and PMA constructs and PMD bit transmission order, exemplified for lane 0, is illustrated in Figure 48–4.

Insert Figure 48-3a as shown

wake time

XGMII																		
T/RXD<7:0>	I	I	LI	LI	LI	LI	LI	---	LI	LI	LI	I	I	---	I	S	Dp	D
T/RXD<15:8>	I	I	I	I	I	I	I	---	I	I	I	I	I	---	I	Dp	Dp	D
T/RXD<23:16>	I	I	I	I	I	I	I	---	I	I	I	I	I	---	I	Dp	Dp	D
T/RXD<31:24>	I	I	I	I	I	I	I	---	I	I	I	I	I	---	I	Dp	Ds	D

PCS																		
LANE 0	K	R	R	K	R	A	K	---	LL	R	K	K	A	---	R	S	Dp	D
LANE 1	K	R	LL	K	R	A	K	---	R	R	K	K	A	---	R	Dp	Dp	D
LANE 2	K	R	R	K	LL	A	LL	---	R	R	LL	K	A	---	R	Dp	Dp	D
LANE 3	K	R	R	LL	R	A	K	---	R	LL	K	K	A	---	R	Dp	Ds	D

Legend:
LI represents the data character containing the XGMII LPI pattern (06)
LL represents the LPI indication codegroup /D20.5/
Dp represents a data character containing the preamble pattern
Ds represents a data character containing the SFD pattern

Figure 48–3a—XGMII and PCS mapping example with optional LPI

Change 48.2.4, Tables 48-2 and 48-3 for LPI encoding:

48.2.4 Ordered_sets and special code-groups

.

Change 48.2.4.2 for Low Power Idle definitions

48.2.4.2 Idle (||I||) and Low Power Idle

Idle ordered_sets (||I||) are transmitted in full columns continuously and repetitively whenever the XGMII is idle (TXD <31:0>=0x07070707 and TXC <3:0>=0xF). ||I|| provides a continuous fill pattern to establish and maintain lane synchronization, perform lane-to-lane deskew and perform PHY clock rate compensation. ||I|| is emitted from, and interpreted by, the PCS.

A sequence of ||I|| ordered_sets consists of one or more consecutively transmitted ||K||, ||R|| or ||A|| ordered_sets, as defined in Table 48–4. Rules for ||I|| ordered_set sequencing shall be as follows:

a) ||I|| sequencing starts with the first column following a ||T||.
b) The first ||I|| following ||T|| alternates between ||A|| or ||K|| except if an ||A|| is to be sent and less than *r* [see item d)] columns have been sent since the last ||A||, a ||K|| is sent instead.

Table 48–2—XGMII character to PCS code-group mapping

XGMII TXC	XGMII TXD	PCS code group	Description
0	00 through FF	Dxx.y	Normal data transmission
1	06	K28.0 or K28.3 or K28.5[a]	Low Power Idle
1	07	K28.0 or K28.3 or K28.5	Idle in **||I||**
1	07	K28.5	Idle in **||T||**
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Other value in Table 36-2	See Table 36-2	Reserved XGMII character
1	Any other value	K30.7	Invalid XGMII character
NOTE—Values in TXD column are in hexadecimal			

[a]Insertion of /D20.5/ is per the rules described below

Table 48–3—PCS code-group to XGMII character mapping

XGMII RXC	XGMII RXD	PCS code group	Description
0	00 through FF	Dxx.y	Normal data reception
1	06	K28.0 or K28.3 or K28.5[a]	Low Power Idle
1	07	K28.0 or K28.3 or K28.5	Idle in **||I||**
1	07	K28.5	Idle in **||T||**
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code-group	Received code-group
1	See Table 36-2	Other valid code-group	Received reserved code-group
NOTE—Values in RXD column are in hexadecimal			

[a]Detection of /D20.5/ is per the rules described below

c) ||R|| is chosen as the second ||I|| following ||T||.

d) Each ||A|| is sent after *r* non-||A|| columns where *r* is a randomly distributed number between 16 and 31, inclusive. The corresponding minimum spacing of 16 non-||A|| columns between two ||A|| columns provides a theoretical 85-bit deskew capability.

e) When not sending an ||A||, either ||K|| or ||R|| is sent with a random uniform distribution between the two.

f) Whenever sync_status=OK, all ||I|| received during idle are translated to XGMII Idle control characters for transmission over the XGMII. All other !||I|| received during idle are mapped directly to XGMII data or control characters on a lane by lane basis, with the exception of /D20.5/ (Low Power Idle) being detected in any row and the rest of the rows in the same column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE in all lanes.

The purpose of randomizing the ||I|| sequence is to reduce 10GBASE-X electromagnetic interference (EMI) during idle. The randomized ||I|| sequence produces no discrete spectrum. Both ||A|| spacing as well as ||K||, ||R||, or ||A|| selection shall be based on the generation of a random integer *r* generated by a PRBS based on one of the 7th order polynomials listed in Figure 48–5. ||A|| spacing is set to the next generated value of *r*. The rate of generation of *r* is once per column, 312.5 MHz ± 100 ppm. Once the ||A|| spacing count goes to zero (A_CNT=0), ||A|| is selected for transmission at the next opportunity during the Idle sequence. ||K|| and ||R|| selection follows the value of code_sel, which is continuously set according to the even or odd value of *r*. The method of generating the random integer *r* is left to the implementer. PCS Idle randomizer logic is illustrated in Figure 48-5.

Low Power Idle is indicated by inserting /D20.5/ with a random uniform distribution in one row of each column during ||I|| to replace ||K|| or ||R|| (not ||A||). Insertion of /D20.5/ does not alter the distribution of ||A||, ||K|| or ||R||.

Add new constants in 48.2.6.1.2, new variables into 48.2.6.1.3, new timers into 48.2.6.1.5 and new messages into 48.2.6.1.6 for LPI state diagrams

48.2.6.1.2 Constants

||LPIDLE||
: Alias for ||I|| during Low Power Idle.

48.2.6.1.3 Variables

deskew_align_status
: Variable used to by the deskew state machine to reflect the status of the lane-to-lane code-group alignment. If the optional Low Power Idle function is implemented then this is overriden by the LPI receive state machine, otherwise this is identical to align_status. The definition is the same as align_status.

rx_lpi_fail
: A boolean variable that is set to TRUE when the receiver fails to recover from a low power idle state to an Active state.

rx_lpi_mode
: An enumerated variable that is set to ON when the PMD's receiver is in a low power state and set to OFF when it is in a Active state and capable of receiving data.

tx_lpi_mode
: An enumerated variable that is set to ON when the PMD's transmitter is in a low power state and set to OFF when it is in a Active state and capable of transmitting data.

rx_quiet
: A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise

tx_quiet

A boolean variable set to TRUE when the transmitter is in the TX_QUIET state and is set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 70.6.5

48.2.6.1.5 Counters

LPI_fail_timer

This timer is started when the LPI receive state machine enters the RX_LINK_FAIL state. The timer terminal count is set to 250 μs. When the timer reaches terminal count it will set the LPI_fail_timer_done = TRUE.

rx_deact_timer

This timer is started when the PMD's receiver enters the RX_SLEEP state. The timer terminal count is set to T_{DA}. When the timer reaches terminal count it will set the rx_deact_timer_done = TRUE.

rx_tq_timer

This timer is started when the PMD's receiver enters the RX_QUIET state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer

This timer is started when the PMD's receiver enters the RX_WAKE state. The timer terminal count is set to T_{WR}. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

tx_ts_timer

This timer is started when the PMD's receiver enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer

This timer is started when the PMD's receiver enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer

This timer is started when the PMD's receiver enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

48.2.6.1.6 Message

PMD_RXQUIET.request(rx_quiet)

A signal sent by the PCS/PMA LPI receive state machine to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data.

PMD_TXQUIET.request(tx_quiet)

A signal sent by the PCS/PMA LPI transmit state machine to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium.

48.2.6.2 State diagrams

Change Figure 48-6 for LPI transmit state diagram and 48-9 for LPI receive state diagram

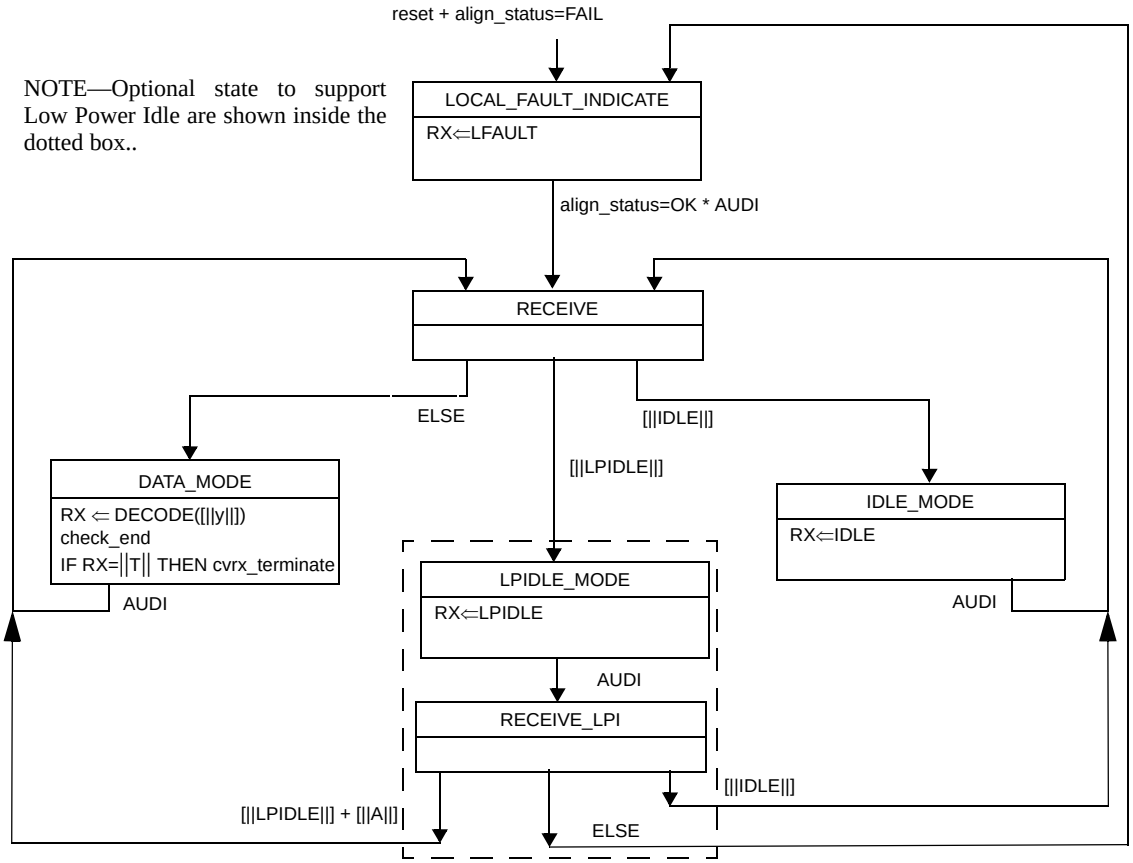


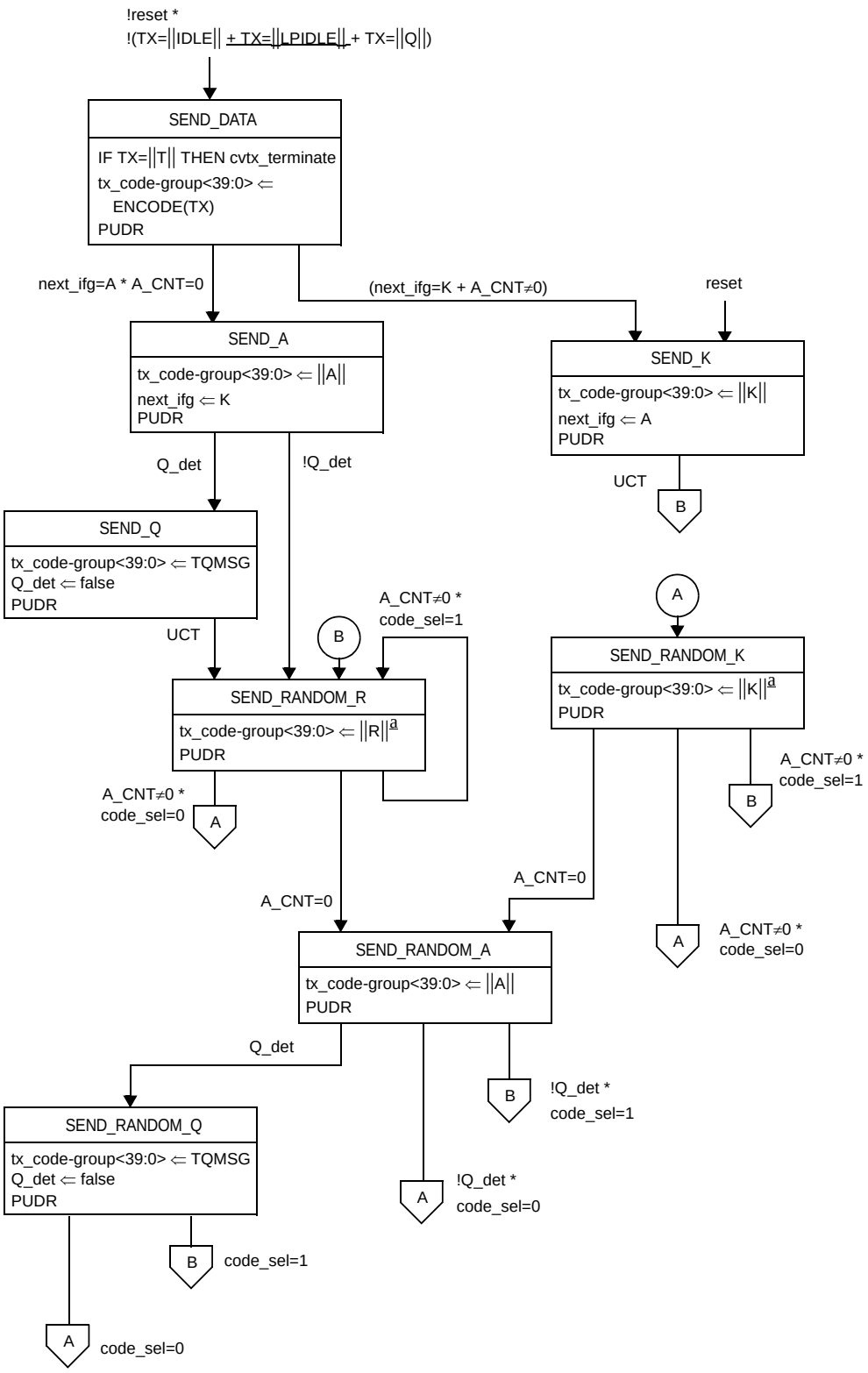
Figure 48–9—PCS receive state diagram

Change 48.2.6.2.2 and 48.6.2.3 and Figure 48-8 for synchronization and deskew

48.2.6.2.1 Synchronization

The PCS shall implement four Synchronization processes as depicted in Figure 48–7 including compliance with the associated state variables as specified in 48.2.6.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions. A Synchronization process operates independently on each lane, and synchronization is complete only when synchronization is acquired on all lanes. The synchronization process described in the following paragraphs applies to each lane.

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indication primitive and conveys received code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message.



[a] If TX=||LPIDLE|| one column is replaced by /D20.5/ as defined in 48.2.4.2.

NOTE—The state diagram makes exactly one transition for each transmit code-group processed.

Figure 48–6—PCS transmit source state diagram

When in the LOSS_OF_SYNC state, the PCS may attempt to realign its current code-group boundary to one which coincides with the code-group boundary defined by a comma (see 36.2.4.9). This process is referred to in this document as code-group alignment.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states. The Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis). Whenever any PMA lane is not operating dependably, as indicated by the setting of lane_sync_status <3:0>, the ~~align_status~~ deskew_align_status flag is set to FAIL

48.2.6.2.2 Deskew

The PCS shall implement the Deskew process as depicted in Figure 48–8 including compliance with the associated state variables as specified in 48.2.6.1. The Deskew process is responsible for determining whether the underlying receive channel is capable of presenting coherent data to the XGMII. The Deskew process asserts the deskew_align_status ~~align_status~~ flag to indicate that the PCS has successfully deskewed and aligned code-groups on all lanes. The Deskew process attempts deskew and alignment whenever the deskew_align_status ~~align_status~~ flag is de-asserted. The Deskew process is otherwise idle. If the optional Low Power Idle function is not implemented then align_status is identical to deskew_align_status. Otherwise the relationship between align_status and deskew_align_status is given by Figure 48-9b the LPI receive state diagram. Whenever the align_status flag is set to FAIL the condition is indicated as a link_status=FAIL condition in the status register bit 4.1.2 or 5.1.2.

Once alignment is acquired, the Deskew process tests received columns and employs multiple sub-states, effecting hysteresis, to move between the ALIGN_ACQUIRED_1 and LOSS_OF_ALIGNMENT states. These states monitor the link for continued alignment, tolerate alignment inconsistencies due to a reasonably low BER, and restart the Deskew process if alignment can not be reliably maintained.

Insert 48.2.6.2.5 for LPI state machines:

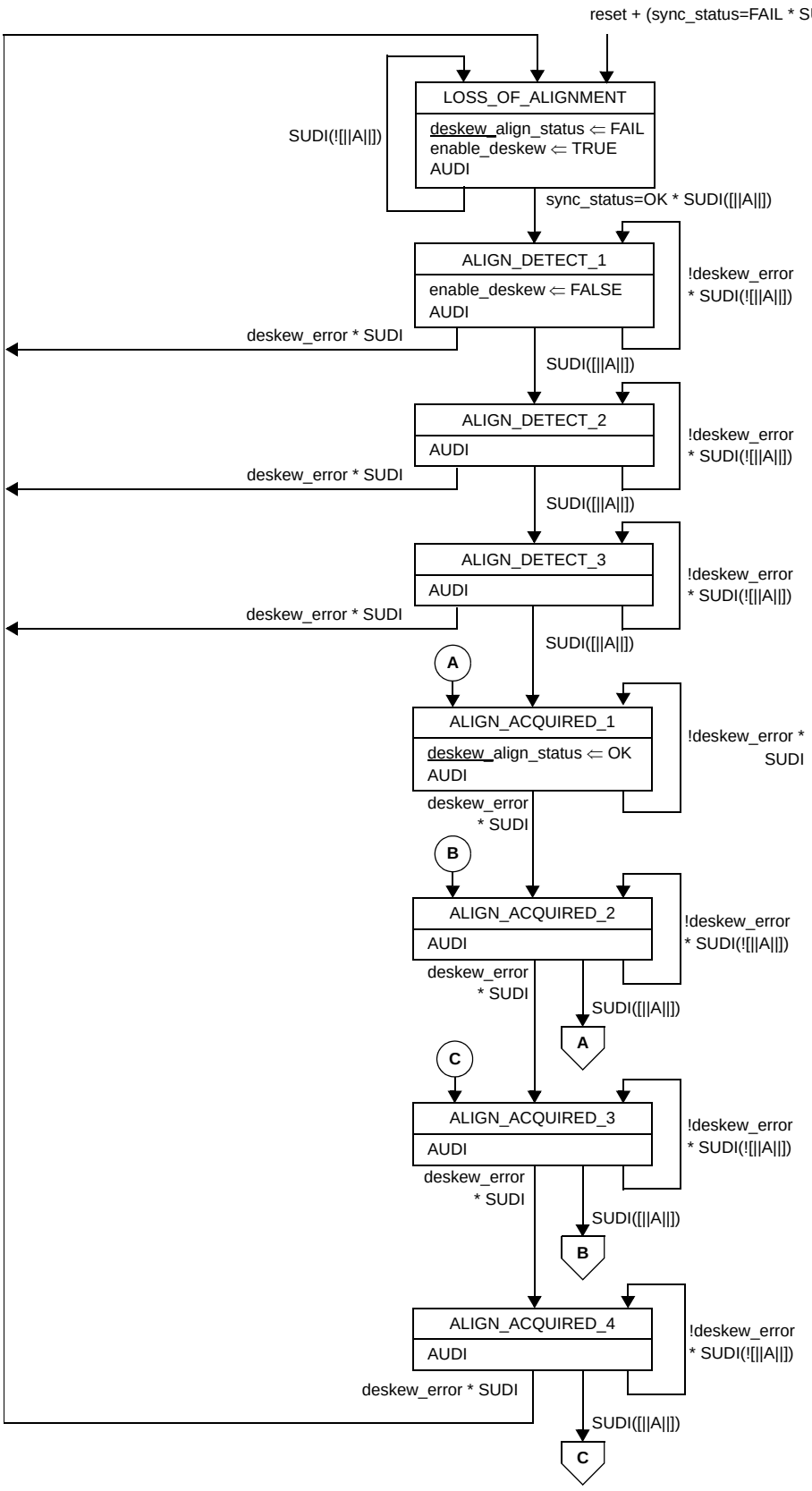


Figure 48–8—PCS deskew state diagram

48.2.6.2.5 LPI state diagrams

If the optional Low Power Idle function is implemented the transmit and receive functions are modified as shown in Figures 48–9a and 48–9b.

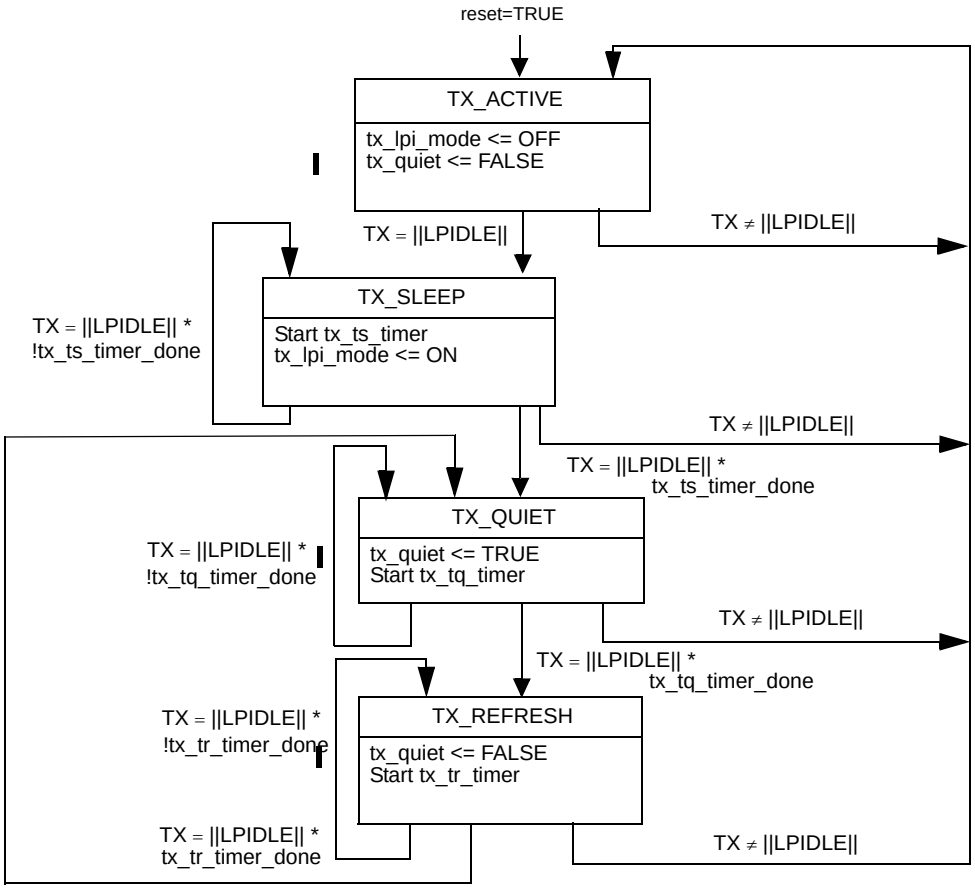


Figure 48–9a—LPI Transmit state diagram

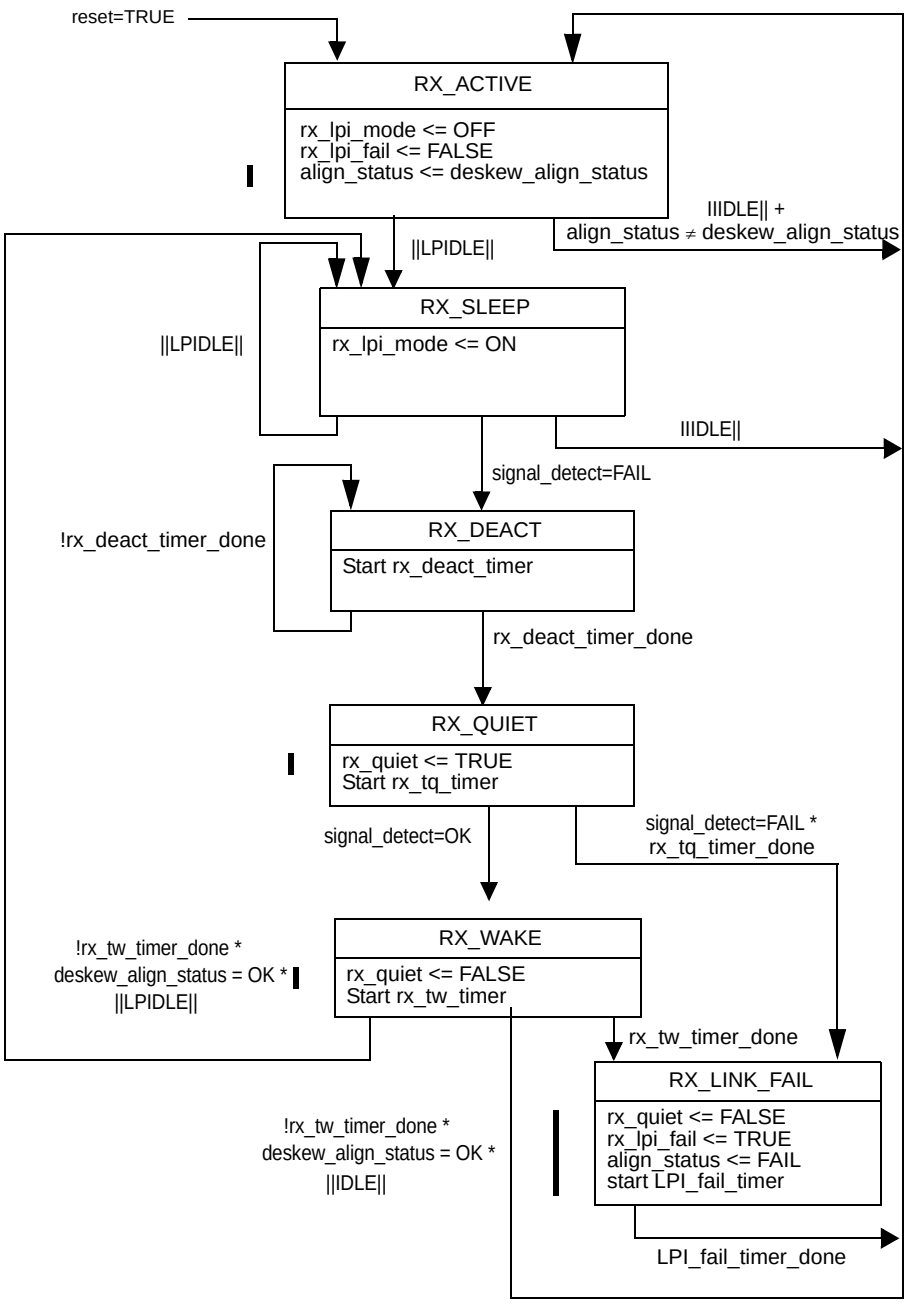


Figure 48–9b—LPI Receive state diagram

The timer values for these state machines are shown in Table 48–9a for transmit and Table 48–10b for receive.

Table 48–9—Transmitter LPI timing parameters

Parameter	Description	Value	Units
T_{SL}	Local Sleep Time from entering TX_SLEEP state to transmit disable	20	μs
T_{QL}	Local Quiet Time from Transmitter disabled to start of TX_REFRESH state	2.5	ms
T_{UL}	Local Refresh Time from Signal_Detect asserted to TX_QUIET state	20	μs

Table 48–10—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect while in the RX_QUIET state before asserting rx_fault	3	4	ms
T_{WR}	Time to wake remote link partner's receiver. T_{WR} is set by the remote link partner during Auto-negotiation.	8	18[a]	μs
T_{DA}	Time to deactivate receiver to handle debounce	1	2	μs

[a]Remote receiver can ask for four T_{WR} values: 8μs, 11μs, 15μs and 18μs

Insert 48.2.6.2.6 for LPI status:

48.2.6.2.6 LPI status and management

If the optional Low Power Idle function is implemented the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variable shown in Table 48-11.

Table 48–11—MDIO status indications

MDIO status variable	Register name	Register address	Note
Tx LP idle received	PCS status register 1	3.1.11	Latched version of 3.1.9
Rx LP idle received	PCS status register 1	3.1.10	Latched version of 3.1.8
Tx LP idle indication	PCS status register 1	3.1.9	TRUE when not in state TX_ACTIVE
Rx LP idle indication	PCS status register 1	3.1.8	TRUE when not in state RX_ACTIVE

48.7 Protocol implementation conformance statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X[1]

[Editor's note (to be removed prior to publication) - changes and additions to PICS for LPI]

Add the following row into table 48.7.3:

48.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	48.2.3		O	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 49

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.9, August 2008	Intial draft for IEEE P802.3az Task Force review.
Draft 1.1, December 2008	The decision to adopt a consistent architectural model for Low Power Idle operation (see Motion #5 from the Nov 2008 meeting) across all PHYs and several issues with implementing this for backplane PHYs without violating the layering model let us to a decision to move some material from the backplane Clauses (70, 71, 72) to the 1000BASE-X (36), 10GBASE-T (48) and 10GBASE-R (49) clauses. See koenen_01_1108.pdf and healey_02_1108.pdf for more background on this. This is a substantial change and the editors suggest it be reviewed carefully.

49. Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R)

Editors' Notes: *To be removed prior to publication.*
changes to BASE-R encoding for EEE operation.

Change 49.2.4.4 for LPI function:

49.2.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-R PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-R PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-R PCS encodes the ordered_set control codes using a combination of the block type field and a 4-bit O code for each ordered_set. The 10GBASE-R PCS encodes each of the other control characters into a 7-bit C code).

The control characters and their mappings to 10GBASE-R control codes and XGMII control codes are specified in Table 49–1. All XGMII and 10GBASE-R control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received. The ability to transmit or receive Low Power Idle is an option for certain PHYs to support Energy Efficient Ethernet (see Clause 78). If this option is not supported Low Power Idle shall not be transmitted and shall be treated as an error if received.

49.2.4.5 Ordered sets

Change Table 49-1 for LPI encoding, insert row:

Table 49–1—Control codes

Control character	Notation	XGMII control code	10GBASE-R control code	10GBASE-R O code	8B/10B code[a]
Idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
Low Power Idle	/LI/	0x06	0x07		K28.0 or K28.3 or K28.5 with D20.5 in one row[b]
Start	/S/	0xfb	Encoded by block type field		K27.7

[a]For information only.The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48
[b]See 48.2.4.2

Change 49.2.4.7 for Low Power Idle definitions

49.2.4.7 Idle /I/ and Low Power Idle /LI/

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

To communicate Low Power Idle, idle control code 0x00 is replaced with 0x07.

Change 49.2.9 and Fig 49-12 for LPI override of synchronization

49.2.9 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 16-bit PMA_UNITDATA.request or WIS_UNITDATA.request primitives. It shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state diagram shown in Figure 49–12.

If the optional Low Power Idle function is not implemented then block_lock is identical to rx_block_lock. Otherwise the relationship between block_lock and rx_block_lock is given by 49-15 the LPI receive state diagram.

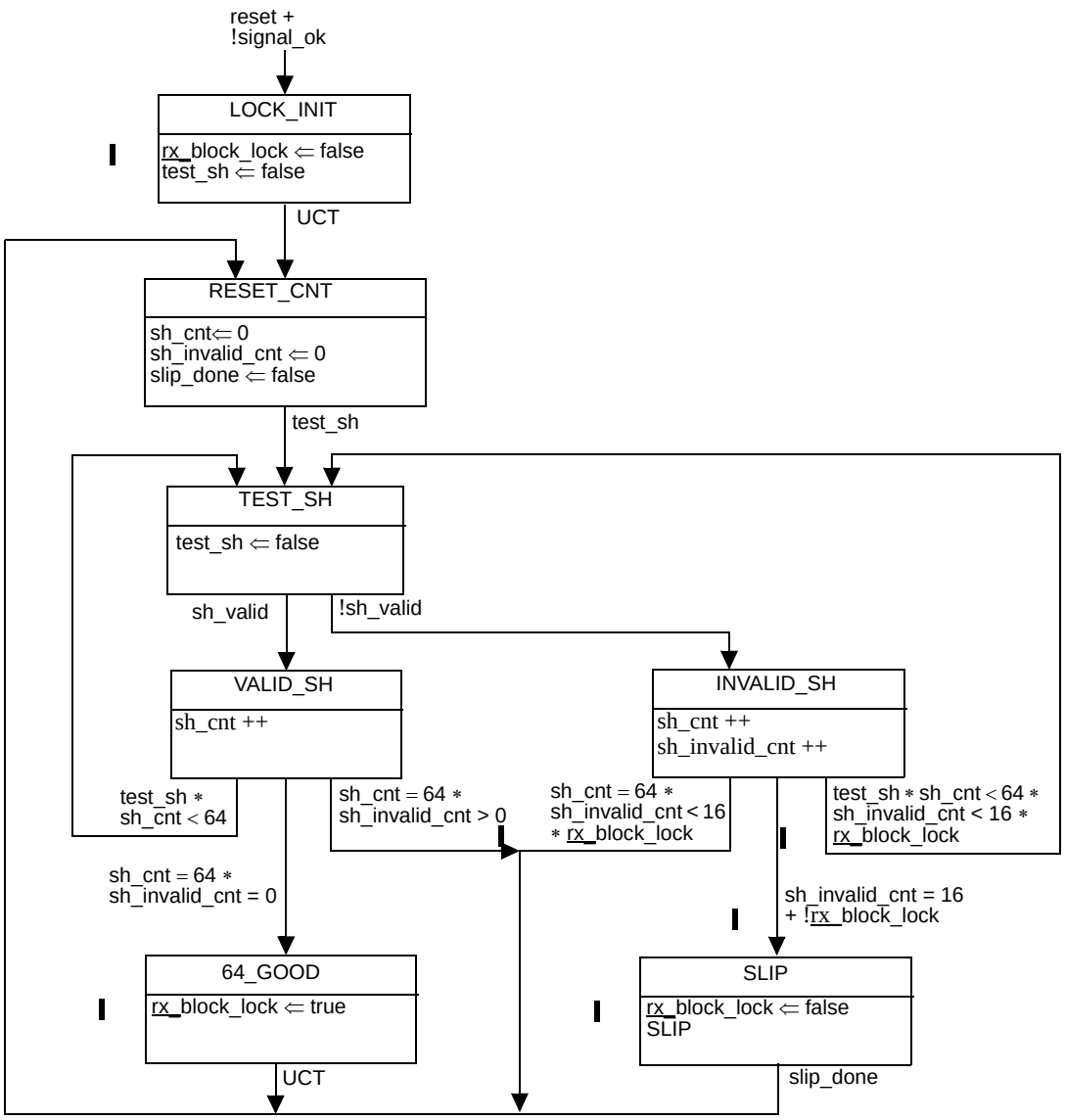


Figure 49–12—Lock state diagram

Change 49.2.13.2.3 function definitions for LPI block types

49.2.13.2.3 Functions

DECODE(rx_coded<65:0>)

Decodes the 66-bit vector returning rx_raw<71:0> which is sent to the XGMII. The DECODE function shall decode the block as specified in 49.2.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<63:0> is sent to the scrambler. The two high order sync bits bypass the scrambler. The ENCODE function shall encode the block as specified in 49.2.4.

R_BLOCK_TYPE = {C, S, T, D, E, LI}

This function classifies each 66-bit rx_coded vector as belonging to one of the five or six types depending on its contents.

Values: C; The vector contains a sync header of 10 and one of the following:

a) A block type field of 0x1e and eight valid control characters other than /E/ and /LI/ (note that /LI/ is only excluded if the optional Low Power Idle function is supported);

b) A block type field of 0x2d or 0x4b, a valid O code, and four valid control characters;

c) A block type field of 0x55 and two valid O codes.

LI; If the optional Low Power Idle function is supported then LI type is a special case of the C type where the vector contains a sync header of 10, a block type field of 0x1e and eight control characters of 0x07 (/LI/).

S; The vector contains a sync header of 10 and one of the following:

a) A block type field of 0x33 and four valid control characters;

b) A block type field of 0x66 and a valid O code;

c) A block type field of 0x78.

T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xaa, 0xb4, 0xcc, 0xd2, 0xe1 or 0xff and all control characters are valid.

D; The vector contains a sync header of 01.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-R control code specified in Table 49–1. A valid O code is one containing an O code specified in Table 49–1.

R_TYPE(rx_coded<65:0>)

Returns the R_BLOCK_TYPE of the rx_coded<65:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP

Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E, LI}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains one of the following:

a) eight valid control characters other than /O/, /S/, /T/, /E/ and /LI/ (note that /LI/ is only excluded if the optional Low Power Idle function is supported);

b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;

c) two valid ordered sets.

LI; If the optional Low Power Idle function is supported then LI type is a special case of the C type where the vector contains a sync header of 10, a block type field of 0x1e and eight control characters of 0x07 (/LI/).

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 49–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 49–1.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

Add new constants in 49.2.13.2.1, new variables into 49.2.13.2.2, new timers into 49.2.13.2.5 and messages into a new subclause 49.2.13.2.6 in support of the LPI state diagrams

49.2.13.2.1 Constants

||LPIDLE||
Alias for ||I|| during Low Power Idle.

49.2.13.2.2 Variables

rx_block_lock
Variable used to by the lock state machine to reflect the status of the code-group delineation. If the optional Low Power Idle function is implemented then this is overriden by the LPI receive state machine, otherwise this is identical to block_lock. The definition is the same as block_lock.

rx_lpi_fail
A boolean variable that is set to TRUE when the receiver fails to recover from a low power idle state to an Active state.

rx_lpi_mode
An enumerated variable that is set to ON when the PMD's receiver is in a low power state and set to OFF when it is in a Active state and capable of receiving data.

tx_lpi_mode
An enumerated variable that is set to ON when the PMD's transmitter is in a low power state and set to OFF when it is in a Active state and capable of transmitting data.

rx_quiet
A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise

tx_quiet
An enumerated variable set to TRUE when the transmitter is in the TX_QUIET state, set to REFRESH when the transmitter is to send refresh signaling, set to WAKE when the transmitter is to send wake signaling and set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 71.6.6. When set to REFRESH or WAKE the PMD will send training signals as described in 71.6.12.

49.2.13.2.5 Timers

LPI_fail_timer
This timer is started when the LPI receive state machine enters the RX_LINK_FAIL state. The timer terminal count is set to 250 μs. When the timer reaches terminal count it will set the LPI_fail_timer_done = TRUE.

rx_deact_timer

This timer is started when the PMD's receiver enters the RX_SLEEP state. The timer terminal count is set to T_{DA}. When the timer reaches terminal count it will set the rx_deact_timer_done = TRUE.

rx_tq_timer

This timer is started when the PMD's receiver enters the RX_QUIET state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer

This timer is started when the PMD's receiver enters the RX_WAKE state. The timer terminal count is set to T_{WR}. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

tx_ts_timer

This timer is started when the PMD's receiver enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer

This timer is started when the PMD's receiver enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer

This timer is started when the PMD's receiver enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

tx_tw_timer

This timer is started when the PMD's receiver enters the TX_WAKE state. The timer terminal count is set to TWL. When the timer reaches terminal count it will set the tx_tw_timer_done = TRUE.

49.2.13.2.6 Messages

PMD_RXQUIET.request(rx_quiet)

A signal sent by the PCS/PMA LPI receive state machine to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data.

PMD_TXQUIET.request(tx_quiet)

A signal sent by the PCS/PMA LPI transmit state machine to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium. When REFRESH or WAKE this indicates that the transmitter must send specific signals to support LPI operation.

Change Figure 49-14 for LPI transmit state diagram and 49-15 for LPI receive state diagram

Editors' Notes: *To be removed prior to publication.*
Changes may be required for lock and BER.state diagrams (49-12 & 49-13)

49.2.13.3 State diagrams

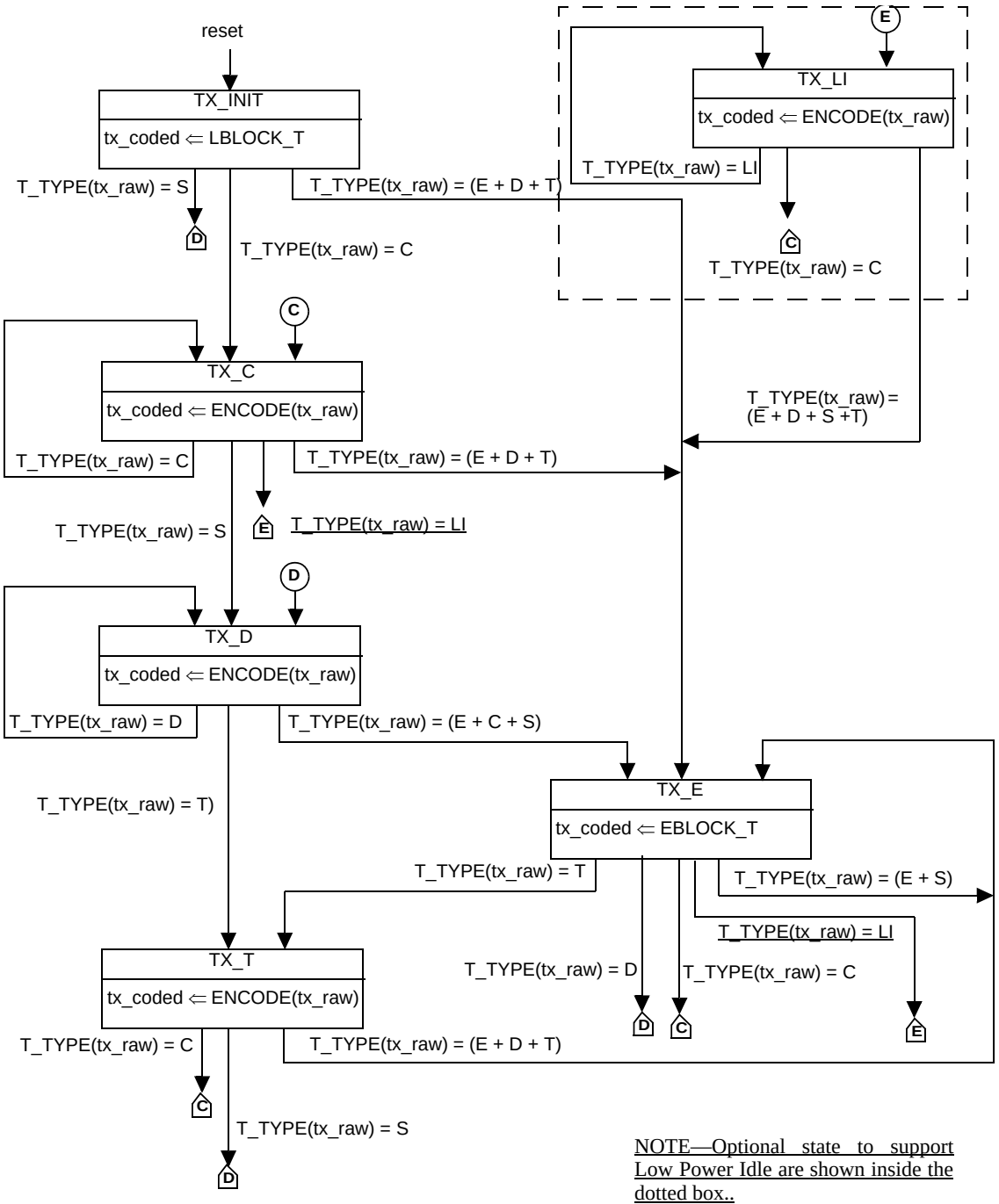


Figure 49–14—Transmit state diagram

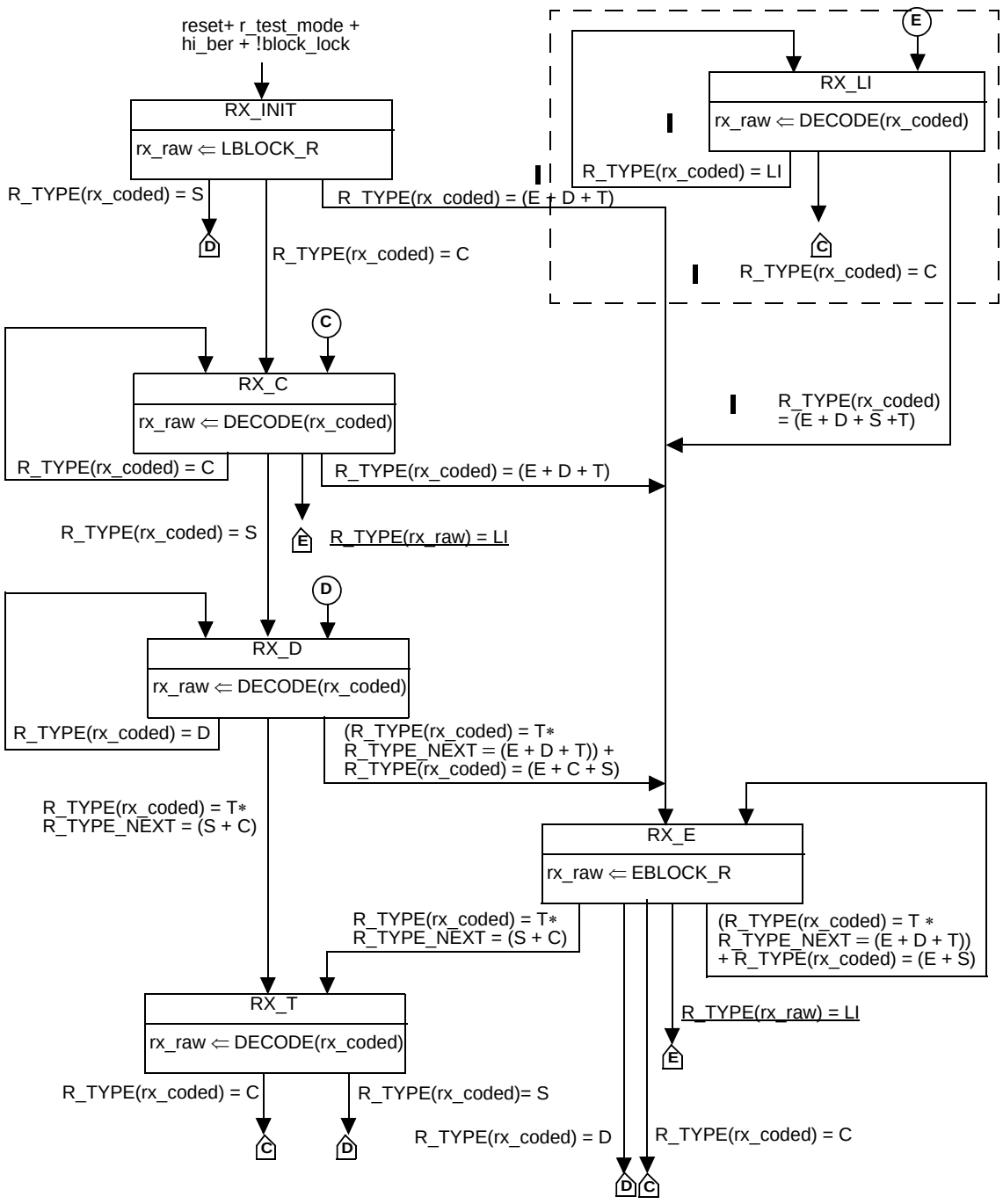


Figure 49–15—Receive state diagram

49.2.13.3.1 LPI state diagrams

If the optional Low Power Idle function is implemented the transmit and receive functions are modified as shown in Figures 49–16 and 49–17.

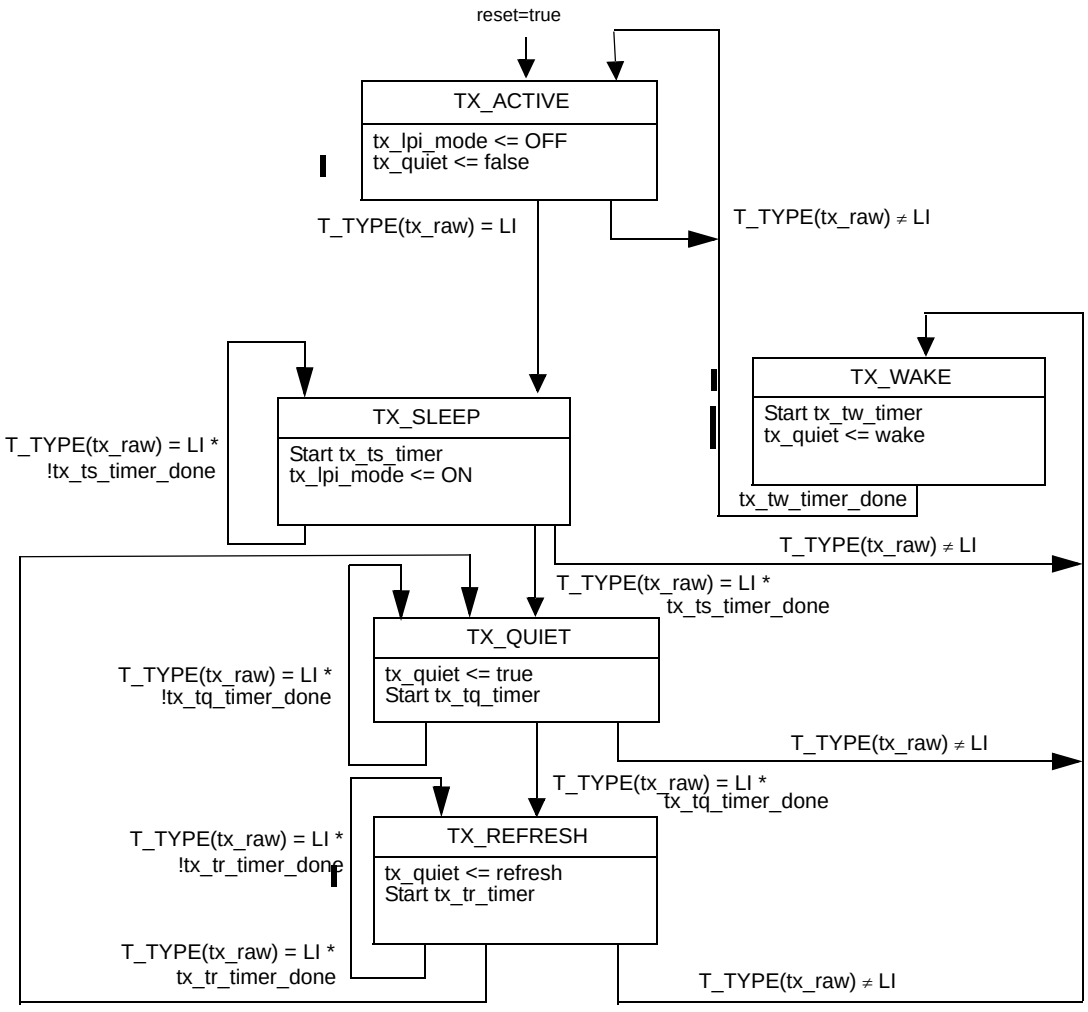


Figure 49–16—LPI Transmit state diagram

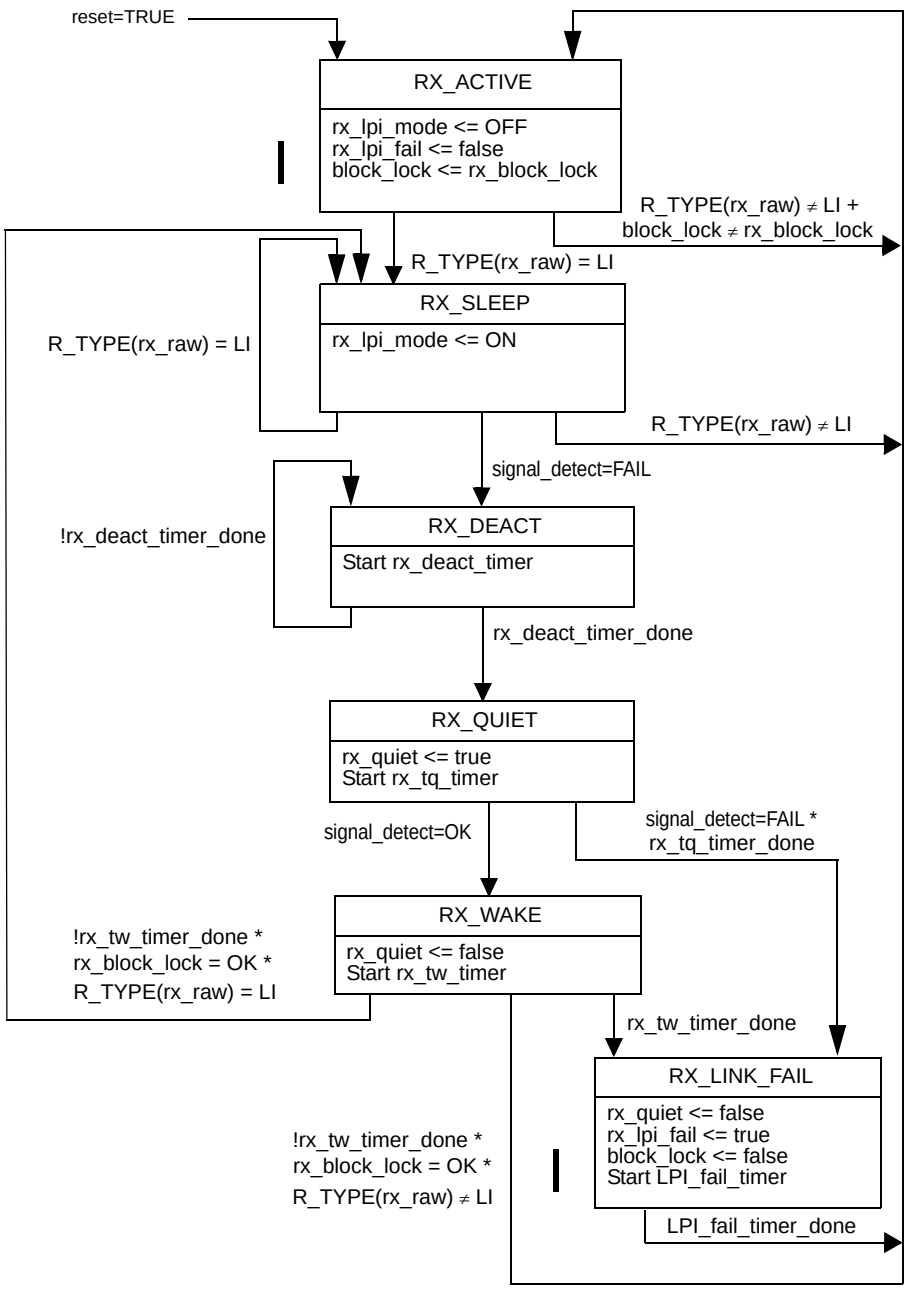


Figure 49–17—LPI Receive state diagram

The timer values for these state machines are shown in Table 49–2a for transmit and Table 49–3b for receive.

Table 49–2—Transmitter LPI timing parameters

Parameter	Description	Value	Units
T_{SL}	Local Sleep Time from entering TX_SLEEP state to transmit disable	5	μs
T_{QL}	Local Quiet Time from Transmitter disabled to start of TX_REFRESH state	1.7	ms
T_{UL}	Local Refresh Time from Signal_Detect asserted to TX_QUIET state	17	μs
T_{WL}	Local Wake Time from LPI deasserted to TX_ACTIVE state	17	μs

Table 49–3—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect while in the RX_QUIET state before asserting rx_fault	2	3	ms
T_{WR}	Time to wake remote link partner's receiver. T_{WR} is set by the remote link partner during Auto-negotiation.	11	17[a]	μs
T_{DA}	Time to deactivate receiver to handle debounce	1	2	μs

[a]Remote receiver can ask for four T_{WR} values: 11μs, 13μs, 15μs and 17μs.

Change 49.2.14.1 for LPI status:

49.2.14.1 Status

PCS_status:

Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_ber is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_ber:

Indicates the state of the hi_ber variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LP idle indication:

If the optional LPI function is implemented, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the LPI receive state machine is in any state other than RX_ACTIVE. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LP idle received).

Tx LP idle indication:

If the optional LPI function is implemented, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the LPI transmit state machine is in any state other than TX_ACTIVE. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LP idle received).

49.3 Protocol implementation conformance statement (PICS) proforma for Clause 49, Physical Coding Sublayer (PCS) type 10GBASE-R[1]

[Editor's note (to be removed prior to publication) - changes and additions to PICS for LPI]

Add the following row into table 49.3.3:

49.3.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	49.2.4.4		O	Yes [ ] No [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Revisions to IEEE Std 802.3-2008, Clause 55

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: *To be removed prior to final publication.*

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.1, July 2008	Initial draft for IEEE P802.3az Task Force review.
Draft 0.9, August 2008	Second draft for IEEE P802.3az Task Force review.
Draft 1.0, October 2008	
Draft 1.1 December 2008	
Draft 1.2 February 2009	First draft of PICS, editor's notes for testmodes

55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.1 Overview

Insert the following text as the last paragraph of 55.1

This clause also specifies a 10GBASE-T Low Power Idle (LPI) capability as part of Energy Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78.

55.1.1 Objectives

Insert item (l) in the list of objectives as shown below:

The objectives of 10GBASE-T are as follows:

a) Support full duplex operation only
b) Support star-wired local area networks using point-to-point links and structured cabling topologies
c) Support a speed of 10 Gb/s at the MAC/PLS service interface
d) Support copper medium from ISO/IEC 11801:2002, with appropriate augmentation as specified in 55.7
e) Support operation over 4-connector structured 4-pair, twisted copper cabling for all supported distances and Classes
f) Define a single 10 Gb/s PHY that would support links of up to 100 m on 4-pair balanced copper cabling as specified in 55.7
g) Preserve the IEEE 802.3/Ethernet frame format at the MAC client service interface
h) Preserve minimum and maximum frame size of the current IEEE 802.3 standard
i) Support Auto-Negotiation (Clause 28)
j) Meet CISPR/FCC Class A EMC requirements
k) Support a BER of less than or equal to 10^{-12} on all supported distances and Classes
l) Support a low-power idle (LPI) capability as part of Energy Efficient Ethernet (Clause 78)

55.1.3 Operation of 10GBASE-T

Insert the following text before the last paragraph of 55.1.3

10GBASE-T PHYs optionally provide support for Low Power Idle (LPI) as part of Energy Efficient Ethernet (see Clause 78). This extension allows PHYs to enter a low-power idle mode of operation when either the local or link system requests low power operation. The transmit and receive functions may enter and leave the lower power mode independently so that both symmetric and asymmetric operation is supported. While the PHY is in the lower power mode the PHY periodically transmits a refresh signal to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. An easily detectable alert signal is used to signal an end to the lower power mode. The alert signal is followed by a wake signal to enable a rapid transition back to the normal operational mode.

Insert the sentence as shown in the last paragraph of 55.1.3

The PCS and PMA subclauses of this document are summarized in 55.1.3.1 and 55.1.3.2. The LPI capability is summarized in 55.1.3.3. Figure 55–3 shows the functional block diagram.

Remove Figure 55-3 and replace it with the figure shown below

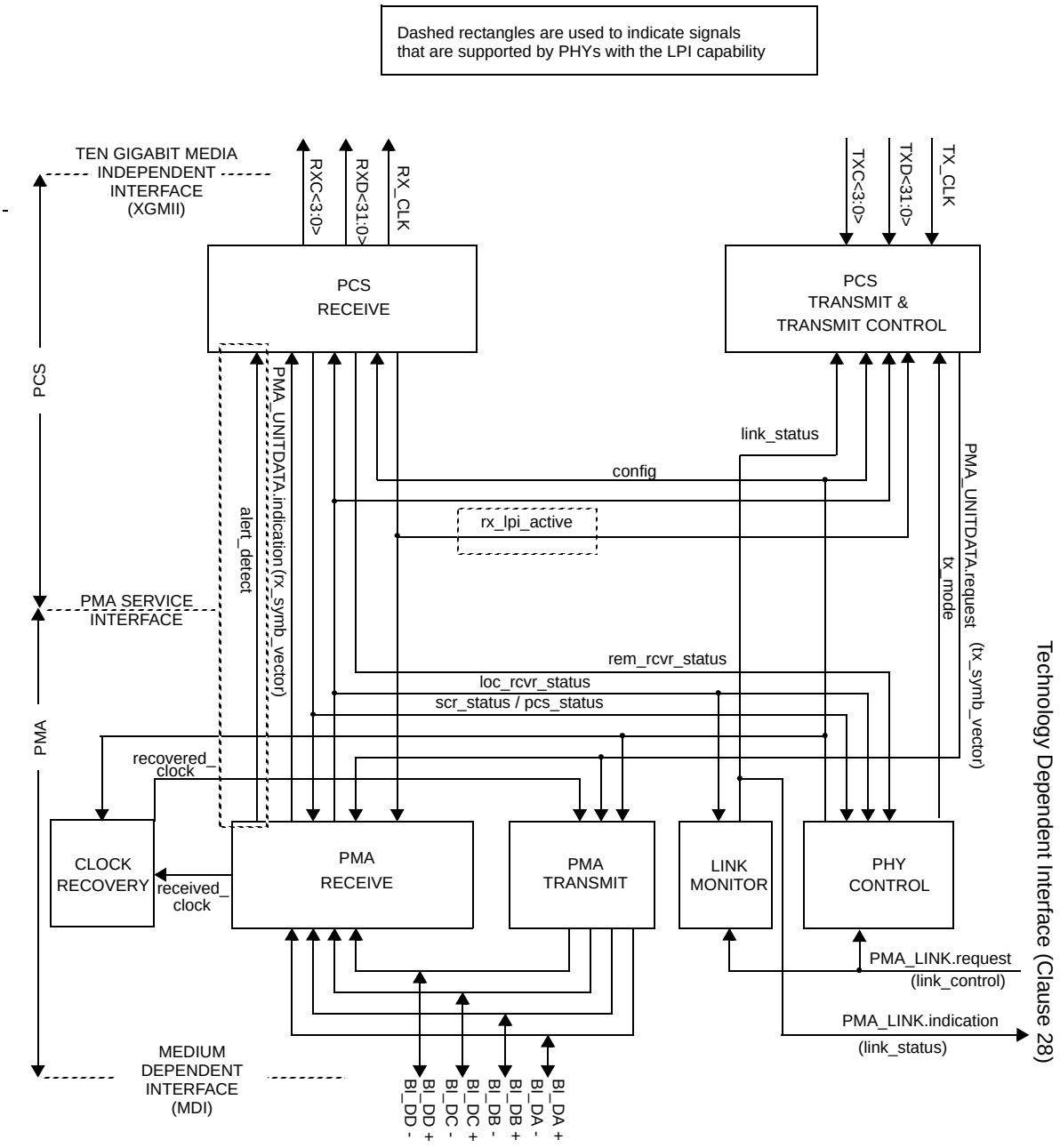


Figure 55–3—Functional block diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

Edit the first paragraph of clause 55.1.3.1 as shown below:

The 10GBASE-T PCS couples a Ten Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 10GBASE-T Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. When the PHY supports EEE the PCS also supports a low power mode . Furthermore, the PCS contains a management interface.

55.1.3.1 Physical Medium Attachment (PMA) sublayer

Insert the following text after the last paragraph of 55.1.3.2

When the PHY supports EEE the PMA also supports a low power transmit mode and a low power receive mode.

Insert 55.1.3.3 after 55.1.3.2 as shown below:

55.1.3.3 Low Power Idle (LPI) capability

A 10GBASE-T PHY may optionally support a LPI capability as part of EEE (Energy Efficient Ethernet). The LPI capability is a mechanism by which 10GBASE-T PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after reaching PCS data mode. Each side of the full duplex link is able to enter and exit the lower power mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full-duplex link is in a period of low utilization. No data frames are lost or corrupted during the transition to or from the lower power mode.

In the transmit direction the transition to the lower power transmit mode begins when the PCS transmit function detects an LPI control character in Lane 0 of two consecutive transfers of TXD[31:0] that will be mapped into a single 64B/65B block. Following this event a sleep signal, encoded into LDPC frames, is transmitted by the PMA. The sleep signal is composed of repeated LP_IDLE 64B/65B blocks. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the lower power transmit mode. Immediately after the transmission of the sleep frames the transmit function of the local PHY enters the lower power transmit mode. While the transmit function is in the lower power mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. This quiet-refresh cycle continues until the PCS function detects IDLE characters on the XGMII interface. These characters signal to the PHY that the lower power transmit mode should end. The PMA Transmit function in the PHY then sends an alert message to the link partner. The alert signal begins on a LDPC frame boundary, but has no fixed relationship to the quiet/refresh cycle. The alert signal wakes the link partner from sleep. The alert signal is followed by a wake signal, composed of IDLE characters. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the lower power mode is triggered when the PCS Receive function detects LP_IDLE characters within received LDPC frames. This indicates that the link partner is about to enter the lower power receive mode. Following these frames the link partner ceases transmission and is quiet. During this quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the full data rate. The alert signal is detected in the PMA and signals that normal data frames will follow. After the alert signal is a wake signal that allows the local receiver time to prepare for the full 10G data-rate. The wake signal is composed of repeated IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

Support for the LPI capability is advertised during Auto-Negotiation. Transitions to and from the lower power transmit mode are controlled via XGMII signaling. Transitions to and from the lower power receive mode are controlled by the link partner through sleep, alert and wake signaling across the channel.

The PCS 64/65B Transmit state diagram includes additional states for EEE as specified in Figure 55–15 and Figure 55–16. The PCS 64/65B Receive state diagram includes additional states for EEE as specified in Figure 55–17 and Figure 55–18. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 55–19. The EEE Receive state diagram is contained in the PMA Receive function and is specified in Figure 55–24.

55.1.4 Signaling

Insert item (l) as the last item in the list of objectives of the signaling scheme as shown below:

10GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to four-dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four-dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation

Insert the following text at the end of the last paragraph in 55.1.4 as shown below:

PHYs may also support the LPI capability as described in 55.1.3.3. Transitions to the lower power mode are supported after reaching normal mode.

Insert the following text at the end of the last paragraph in 55.2.2 as shown below:

PMA_REMRXSTATUS.request (rem_rcvr_status)

EEE capable PHYs additionally support the following service primitives:

PMA_ALERTDETECT.indication (alert_detect)

PCS_RX_LPI_STATUS.indication (rx_lpi_active)

Replace the existing Figure 55-4 with the figure shown below.

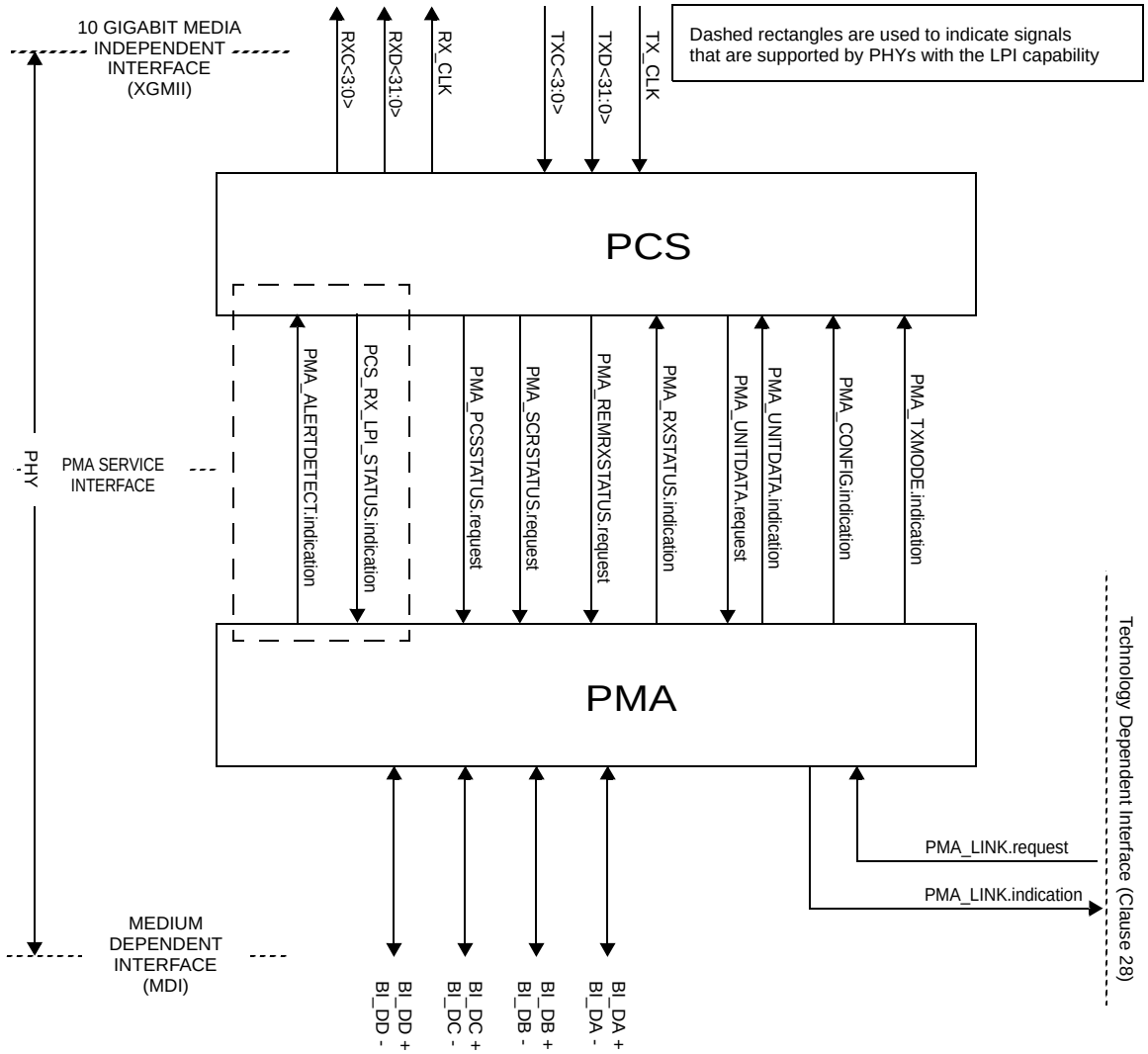


Figure 55–4—10GBASE-T service interfaces

55.2.2.3.1 Semantics of the primitive

Edit the tx_sym_vector parameter options in 55.2.2.3.1 as shown below :

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D	A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. In normal operation each symbol may take on one of the values in the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The symbols may additionally take the value 0 when zeros are to be

	transmitted in the two cases: i) when PMA_TXMODE.indication is SEND_Z during PMA training ii) after data mode is reached, the transmit function is in the lower power transmit mode and lpi_tx_mode is QUIET
ALERT)	A vector used to indicate that the PMA should transmit the Alert sequence. ALERT will be asserted for a time equal to 4 LDPC frames.

Insert 55.2.2.9 and 55.2.2.10 after section 55.2.2.8 as shown below:

55.2.2.9 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is ACTIVE. The parameter alert_detect conveys to the PCS receive function information regarding the detection of the LPI Alert signal by the PMA receive function. The criterion for setting the parameter alert_detect is left to the implementor.

55.2.2.9.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of two values of the form:

DETECTED	The alert signal has been reliably detected at the local receiver
NOT_DETECTED	The alert signal at the local receiver has not been detected.

55.2.2.9.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

55.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Clause 55.3.2.3, Figure 55–17 and Figure 55–18.

55.2.2.10 PCS_RX_LPI_STATUS.indication

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PCS_RX_LPI_STATUS.indication conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the lower power receive mode. The parameter is generated by the EEE Receive state diagram.

55.2.2.10.1 Semantics of the primitive

PCS_RX_LPI_STATUS.indication (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

ACTIVE	The receive function is in the lower power receive mode
NOT_ACTIVE	The receive function is not in the lower power receive mode

55.2.2.10.2 When generated

The PCS generates PCS_RX_LPI_STATUS.indication messages to indicate a change in the rx_lpi_active status.

55.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.3.2.3 and Figure 55–24.

Replace the existing Figure 55-5 with the figure shown below.

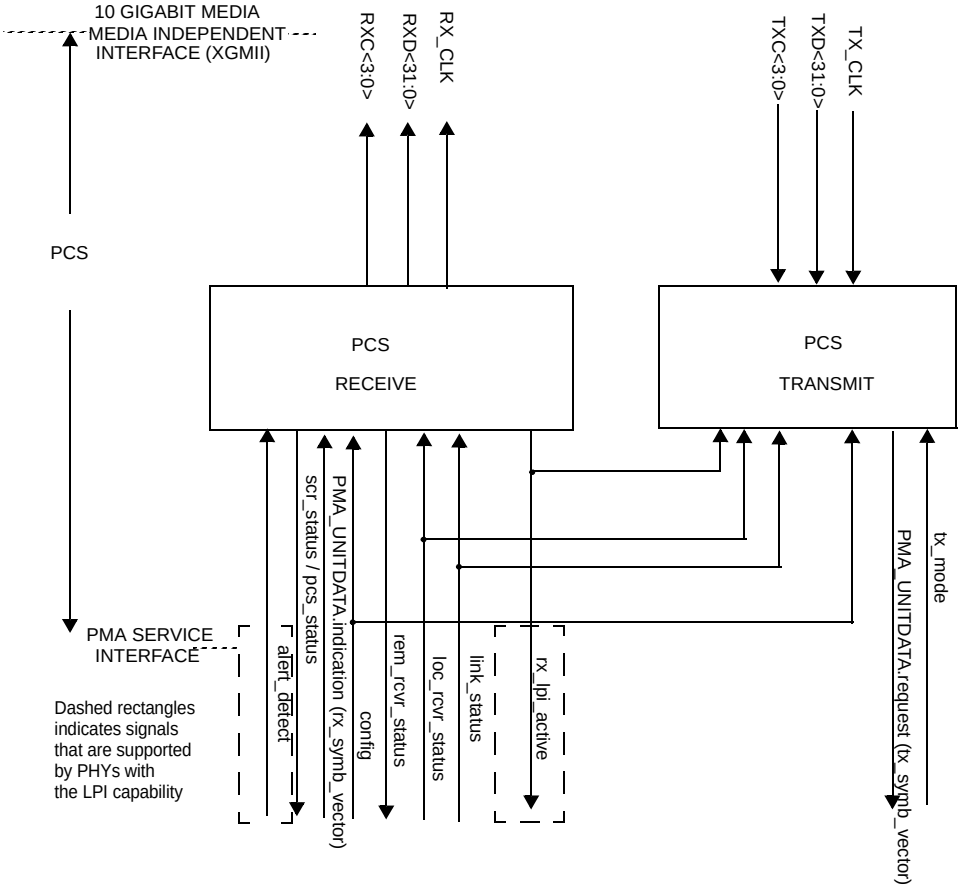


Figure 55–5—PCS reference diagram

55.3.2.2 PCS Transmit function

Insert the following text after the first paragraph in 55.3.2.2

A dashed rectangle in Figure 55–15 and Figure 55–16 is used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the LPI capability. PHYs without the LPI capability do not support these transitions.

Insert the following text after the last paragraph in 55.3.2.2

After reaching the normal mode of operation, LPI-capable PHYs may enter the lower power transmit mode under the control of the MAC across the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The LPI capability is described in 55.3.2.2.21

55.3.2.2.1 Use of blocks

Change text in 55.2.2.9.4 as shown below:

The PCS maps XGMII signals into 65-bit blocks inserted into an LDPC frame, and vice versa, using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Outside the lower power mode blocks ~~Blocks~~ and frames are unobservable and have no meaning outside the PCS. During the lower power mode LDPC frames are used to delimit sleep, wake, refresh, quiet and alert times. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 55.3.2.2.6.

55.3.2.2.2 Idle (/I/)

Change the Control Codes table (55-1) by inserting a row for lp_idle after the first row (idle):.

Table 55–1—Control Codes

Control character	Notation	XGMII Control codes	10GBASE-T Control codes	10GBASE-T O code	8B/10B code[a]
lp_idle	/LI/	0x06	0x06		TBD

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.

Insert 55.3.3.3.10 LP_idle as shown and renumber subsequent sections:

55.3.2.2.10 LP_idle (/LI/)

When preceded by idle control characters (/I/), low power idle control characters (/LI/) on the XGMII indicate that the MAC is requesting a transition to the lower power transmit mode. A continuous stream of low power idle characters (/LI/) is used to maintain a link in the lower power transmit mode. Idle control characters (/I/) are used to transition from the lower power transmit mode to the normal mode. EEE compliant PHYs respond to the low power idle XGMII control characters using the procedure outlined in 55.1.3.3. Low power idle characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of 4. /LI/s may be added following low power idle. They shall not be added while data is being received.

Insert text shown as a new subclause 55.3.2.2.21 after the existing subclause 55.3.2.2.20:

55.3.2.2.21 LPI Capability

The optional LPI 10GBASE-T capability allows compliant PHYs to transition to a lower power mode of operation when link utilization is low.

EEE compliant PHYs shall implement the EEE transmit state diagram, shown in Figure 55–19, within the PCS.

When PCS_Reset is asserted the state diagram enters the TX_NORMAL state.

When a complete 64B/65B block of LPI characters is generated by the PCS transmit function, the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the lower power transmit mode. The sleep signal comprises 9 full LDPC frames composed of LP_IDLE 64/65B blocks encoded using the 65B-LDPC coding technique. The 9 full frames may be preceded by a partial frame of LP_IDLE XGMII characters.

Following the transmission of the sleep signal, quiet/refresh signaling begins, as described in Clause 55.3.5.

After the sleep signal is transmitted LP_IDLE characters shall be input to the PCS scrambler continuously until the PCS Transmit Function exits the lower power transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive as described below:

During PMA training the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH_A and the PMA asserts SEND_N the PCS passes the PMA training signal to the PMA on pair A, to allow both the local and remote PHY to refresh adaptive filters and timing loops. The PCS passes zeros to all other pairs in this condition. REFRESH_B, REFRESH_C and REFRESH_D operate in a analogous manner for the other pairs.

The quiet-refresh cycle is repeated until IDLE codewords are detected at the XGMII. These characters indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request message is set to the value ALERT. The alert signal is not synchronized with respect to the refresh/quiet cycle but shall be synchronized so that the alert signal from the PMA begins on a LDPC frame boundary.

The PHY will also transition back to the normal operation mode if an error condition occurs. This error condition is defined as the detection of any characters other than LP_IDLE or IDLE at the XGMII.

After the Alert message the PCS completes the transition from low power idle mode to normal mode by sending a Wake signal which is composed of lpi_wake_time /I/ 64B/65B blocks if an error condition has not been detected, or lpi_wake_time repeated local fault blocks if an error condition has been detected.

lpi_wake_time is a fixed parameter that is defined as 9 LDPC frames as shown in Table 55–2 below. The maximum PHY wake time, lpi_wake_timer, is 7.63us (lpi_wake_timer=Tw_phy as defined by Clause 78), which occurs only when wake is requested before sleep has been transmitted. Typically, wake will be requested after the sleep signal is transmitted and in this case the maximum PHY wake time value is 4.16 us.

Table 55–2—LPI wake time

lpi_tx_wake_time	lpi_wake_timer during sleep		lpi_wake_timer after sleep	
(frames)	(frames)	(usec)	(frames)	(usec)
9	23	7.36	13	4.16

55.3.2.3 PCS Receive function

Insert the following text after the existing text in 55.3.2.3:

PHYs with the EEE capability support transition to the lower power mode after PCS_Status=OK is asserted. Transitions to and from low power idle operation are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the lower power receive state and indicating these transitions using signals defined in subclause 55.2.2.

The link partner signals a transition to the lower power mode of operation by transmitting /LI/ blocks. When /LI/ blocks are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive XGMII. The link partner will transmit 9 LDPC frames composed entirely of repeated /LI/ blocks. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses LDPC frame counters to maintain synchronization with the remote PHY, and receives periodic refresh signals that are used to update coefficients so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in subclause 55.3.5. The quiet/refresh cycle continues until the PMA asserts alert_detect to indicate that the alert signal has been reliably detected. After the alert signal the link partner transmits repeated /I/ characters, representing a wake signal. The /LI/ codeword at the receive XGMII is deasserted. The PCS receive function decodes the /I/ characters to the XGMII and resumes normal operation.

55.3.5 LPI signaling

Insert the following clause after the existing 55.3.4.3 subclause, and renumber subsequent clauses appropriately

PHYs with the LPI capability have transmit and receive functions that can enter and leave the lower power mode independently. The PHY can transition to the lower power mode after PCS_status=OK is asserted by the PHY Control state diagram. The transmit function of the PHY initiates a transition to the lower power transmit mode when LP_IDLE blocks are generated as described in 55.3.2.2.21. The transmit function of the link partner signals the transition using the sleep signal. Following the sleep signal the transmit function asserts tx_lpi_active and the transmit function enters the lower power transmit mode.

Within the lower power mode PHYs use a repeating quiet-refresh cycle. The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 124 LDPC frames. The quiet period is defined in 55.3.5.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 4 LDPC frames. The refresh period is defined in 55.3.5.3. A cycle composed of one quiet period and one refresh period is known as an single pair LPI cycle and lasts for a time lpi_qr_time equal to 128 LDPC frames. The time taken to complete a quiet-refresh cycle for all four pairs is known as a complete LPI cycle and lasts for a time lpi_allpairs_qr_time = 4 x lpi_qr_time.

lpi_offset, lpi_quiet_time, lpi_refresh_time, lpi_qr_time and lpi_allpairs_qr_time are timing parameters that are integer multiples of the LDPC frame time. lpi_offset is a fixed value equal to lpi_qr_time/2 that is used to ensure refresh signals are appropriately offset by the link partners.

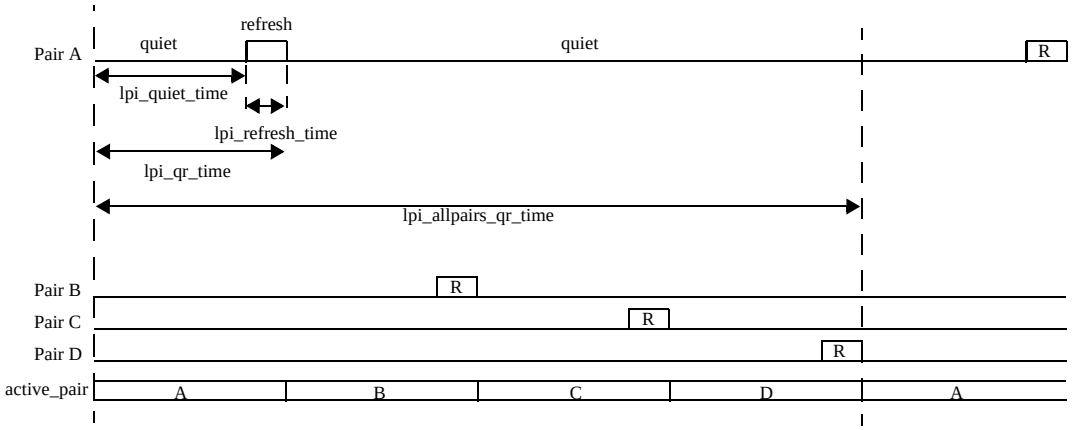


Figure 55–6—Timing periods for LPI signals

Table 55–3—Values of quiet and refresh time parameters

lpi_refresh_time	lpi_quiet_time
4	124

PHYs begin the transition from the lower power receive mode when the alert signal is detected by the PMA as defined in 55.4.2.4 and Figure 55–24.

55.3.5.1 LPI Synchronization

Editor's note: To be removed prior to publication
This synchronization method works well for loop-timed links. Non-loop-timed links require further attention.

To maximise power savings, maintain link integrity and ensure interoperability, LPI capable PHYs must synchronize refresh intervals during the lower power mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting LDPC frames from the transition to PCS_Test.

As in normal training the master signals the time it will transition to PCS_Test using the transition counter following the procedure described in 55.4.2.5.14. **(Editor's note: Insert active cross reference)**.

When both PHYs support the EEE capability, the slave PHY is responsible for initializing its transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master PHY's transition to PCS_Test, measured at the slave PHY's MDI on pair A. The slave PHY shall initialize its transition counter so that the slave PHY's transition to PCS_Test occurs during the PHY frame when the slave PHY's transition counter = 0. The master PHY is responsible for detecting the slave PHY's transition to PAM16. The master PHY counts the slave PHY's LDPC frames from this point.

This mechanism ensures that the refresh offset is bounded to a small value at both MDI interfaces, thus ensuring there is no overlap of master and slave signals during the symmetric lower power mode.

Following the transition to PCS_Test, the PCS counts transmitted and received LDPC frames, and uses these counters to generate refresh and pair control signals for the transmit and receive functions. The transmitted LDPC frame count is named tx_ldpc_frame_cnt. The received LDPC frame count is named rx_ldpc_frame_cnt.

The master and slave derive the active pair and refresh_active signals from the LDPC frame counters as shown in Table-55–4 and Table 55–5 below.

Table 55–4—Synchronization logic derived from master signal LDPC frame count

Master-side Variable	Slave-side Variable	for master v=tx_ldpc_frame_cnt for slave v=rx_ldpc_frame_cnt
tx_refresh_active=true	rx_refresh_active=true	lpi_offset-lpi_refresh_time ≤ mod(v,lpi_qr_time) < lpi_offset
tx_active_pair=PAIR_A	rx_active_pair=PAIR_A	lpi_offset + lpi_qr_time ≤ v < lpi_offset + 2 x lpi_qr_time
tx_active_pair=PAIR_B	rx_active_pair=PAIR_B	lpi_offset + 2 x lpi_qr_time ≤ v < lpi_offset + 3 x lpi_qr_time
tx_active_pair=PAIR_C	rx_active_pair=PAIR_C	lpi_offset + 3 x lpi_qr_time ≤ v < 4 x lpi_qr_time OR 0 ≤ v < lpi_offset
tx_active_pair=PAIR_D	rx_active_pair=PAIR_D	lpi_offset ≤ v < lpi_offset + lpi_qr_time

Table 55–5—Synchronization logic derived from slave signal LDPC frame count

Master-side Variable	Slave-side Variable	for master u=rx_ldpc_frame_cnt for slave u=tx_ldpc_frame_cnt
rx_refresh_active=true	tx_refresh_active=true	lpi_quiet_time ≤ mod(u,lpi_qr_time)
rx_active_pair=PAIR_A	tx_active_pair=PAIR_A	0 ≤ u < lpi_qr_time
rx_active_pair=PAIR_B	tx_active_pair=PAIR_B	lpi_qr_time ≤ u < 2 x lpi_qr_time
rx_active_pair=PAIR_C	tx_active_pair=PAIR_C	2 x lpi_qr_time ≤ u < 3 x lpi_qr_time
rx_active_pair=PAIR_D	tx_active_pair=PAIR_D	3 x lpi_qr_time ≤ u < 4 x lpi_qr_time

55.3.5.2 Quiet period signaling

During the quiet period the transmitters on all four pairs should be turned off. Average Launch Power (as measured from 28 LDPC frames after a Refresh period to 28 LDPC frames before the next Refresh period on the same lane) for each Transmitter shall be less than -41dBm. This requirement does not apply to the periods when the alert signal is transmitted as defined in Clause 55.4.2.2.1

55.3.5.3 Refresh period signaling

During the lower power mode 10GBASE-T PHYs use staggered, out-of-phase refresh signaling to maximize power savings. 2-level PAM refresh symbols are generated using the PMA side-stream scrambler polynomials described in subclause 55.3.4. The long training sequence described in 55.3.4 shall be used during the lower power mode, with the scramblers free-running from PCS Reset. If scrambler reinitialization was used for initial training, it shall be disabled after the PHY Control state diagram reaches the PCS_Data state.

Refresh signals shall be sent using the THP filter as described in subclause Clause 55.4.3.1. At the start of each refresh signal the THP feedback delay line shall be initialized with zeros.

While a transmit function is in the lower power transmit mode only one of the transmit pairs will be active during a refresh period, except when the tx_symb_vector has the value ALERT. When tx_symb_vector has the value ALERT and the PHY is the master the transmitter on pair A shall be active and all other pairs shall be quiet. When tx_symb_vector has the value ALERT and the PHY is slave the transmitter on pair C shall be active and all other pairs shall be quiet. If lpi_tx_mode=REFRESH_A and tx_symb_vector has the value ALERT then the alert shall be transmitted in place of the refresh. tx_symb_vector for all transmit pairs that are not active shall be set to zero.

Insert the following variable definitions after all existing variable definitions in the existing 55.3.5.2.2

tx_lpi_active

Set to ON when the PHY transmit function is operating in a lower power transmit mode and set to OFF otherwise. The lower power transmit mode begins immediately after the sleep signal is transmitted and lasts until the alert signal is transmitted completely.

rx_lpi_active

Set to ON when the PHY receive function is operating in a lower power receive mode and set to OFF otherwise. The lower power receive mode begins when the sleep signal is detected and lasts until the alert signal is detected.

tx_lpi_req

Set to TRUE when the MAC indicates that it is requesting a transition to the lower power transmit mode via the XGMII and set to FALSE otherwise.

rx_lpi_req

Set to TRUE when the 64B/65B decoder output signal indicates the link partner is requesting that the PHY operate in the lower power receive mode and set to FALSE otherwise.

pma_alert_indicate

Indicates that an alert signal from the link partner has been received at the MDI. This signal will be set to TRUE when the PHY detects that the link partner is sending the alert signal and is set to FALSE otherwise.

tx_active_pair

A vector indicating the transmit active pair during the lower power transmit mode. The vector may take the values PAIR_A, PAIR_B, PAIR_C, PAIR_D. This variable is defined in 55.3.5.1,

tx_lpi_error

A boolean value. TRUE indicates that an error has been detected at the XGMII interface on exit from the lower power transmit mode.

lpi_tx_mode

A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb_vector) interface.

lpi_tx_mode controls tx_symb_vector only when tx_mode is set to SEND_N.

The variable is set to NORMAL when tx_lpi_active is false, indicating that the PCS is in the normal mode of operation and will encode code-groups from the XGMII as described in 55.3.2.2.

The variable is set to REFRESH_A when tx_lpi_active * tx_active_pair==PAIR_A * tx_refresh active.

The variable is set to REFRESH_B when tx_lpi_active * tx_active_pair==PAIR_B * tx_refresh active.

The variable is set to REFRESH_C when tx_lpi_active * tx_active_pair==PAIR_C * tx_refresh active.

The variable is set to REFRESH_D when tx_lpi_active * tx_active_pair==PAIR_D * tx_refresh active.

The variable is set to QUIET when tx_lpi_active * !tx_refresh_active.

tx_refresh_active

A boolean value. This variable is set to true following the logic described in 55.3.5.1.

55.3.5.2.3 Timers

Insert 7 additional timers after existing timer definitions in 55.3.5.2.3:

lpi_tx_sleep_timer
This timer defines the time the local transmitter sends the sleep signal to the link partner
Values: The condition lpi_tx_sleep_timer_done becomes true upon timer expiration
Duration: This timer has a period equal to 9 LDPC frames

lpi_tx_quiet_timer
This timer defines the time the local transmitter is quiet. The timer is synchronized with respect to the transition to PCS_Test as described in Clause 55.3.5.1.
Values: The condition lpi_tx_quiet_timer_done becomes true upon timer expiration
Duration: This timer has a period equal to lpi_quiet_time LDPC frames

lpi_tx_refresh_timer
This timer defines the time the local transmitter transmits the refresh signal. The timer is synchronized with respect to the transition to PCS_Test as described in Clause 55.3.5.1.
Values: The condition lpi_tx_refresh_timer_done becomes true upon timer expiration.
Duration: This timer has a period equal to lpi_refresh_time LDPC frames.

lpi_tx_alert_timer
This timer defines the time the local transmitter transmits the alert signal, in order to alert the link partner that the PHY will transition from the lower power transmit mode back to the normal data mode.
Values: The condition lpi_tx_alert_timer_done becomes true upon timer expiration.
Duration: This timer has a period equal to 4 LDPC frames.

lpi_wake_timer:
This timer defines the time the local transmitter transmits IDLE control characters to allow the remote PHY to return to data mode.
Values: The condition lpi_wake_timer_done becomes true upon timer expiration.
Duration: This timer has a period equal to lpi_wake_time LDPC frames.

lpi_rx_wake_timer:
This timer defines the time the receiver waits to receive IDLE or LF control characters following an alert indication, before it is able to report an error condition
Values: The condition lpi_rx_wake_timer_done becomes true upon timer expiration.
Duration: This timer has a period equal to lpi_wake_time LDPC frames.

lpi_tx_wake_timer:
This timer defines the minimum time the PHY remains in the lower power mode before it can resume transmitting XGMII data.
Values: The condition lpi_tx_wake_timer_done becomes true upon timer expiration.
Duration: This timer has a period equal to the value shown in table Table 55–2, selected from the appropriate column depending upon whether the PHY has finished transmitting the sleep signal.

55.3.5.2.5 .Counters

Insert the following text after the existing text in subclause 55.3.5.2.4

tx_ldpc_frame_cnt
An integer value that counts transmitted LDPC frames. tx_ldpc_frame_cnt is reset to 0 when tx_ldpc_frame_cnt = lpi_qr_time x 4. It is incremented every time ldpc_frame_done comes true.
The counter is reset when the first symbol of the first LDPC frame crosses the MDI interface on pair A in the transmit direction after initial training.

rx_ldpc_frame_cnt

An integer value that counts received LDPC frames. tx_ldpc_frame_cnt is reset to 0 when rx_ldpc_frame_cnt = lpi_qr_time x 4. The counter is reset when the first symbol of the first LDPC frame crosses the MDI interface on pair A in the receive direction after initial training.

55.3.5.4 State diagrams

States and transitions surrounded by dashed rectangles indicate requirements for 10GBASE-T EEE-compliant implementations.

Add the figures shown below and renumber figures appropriately.

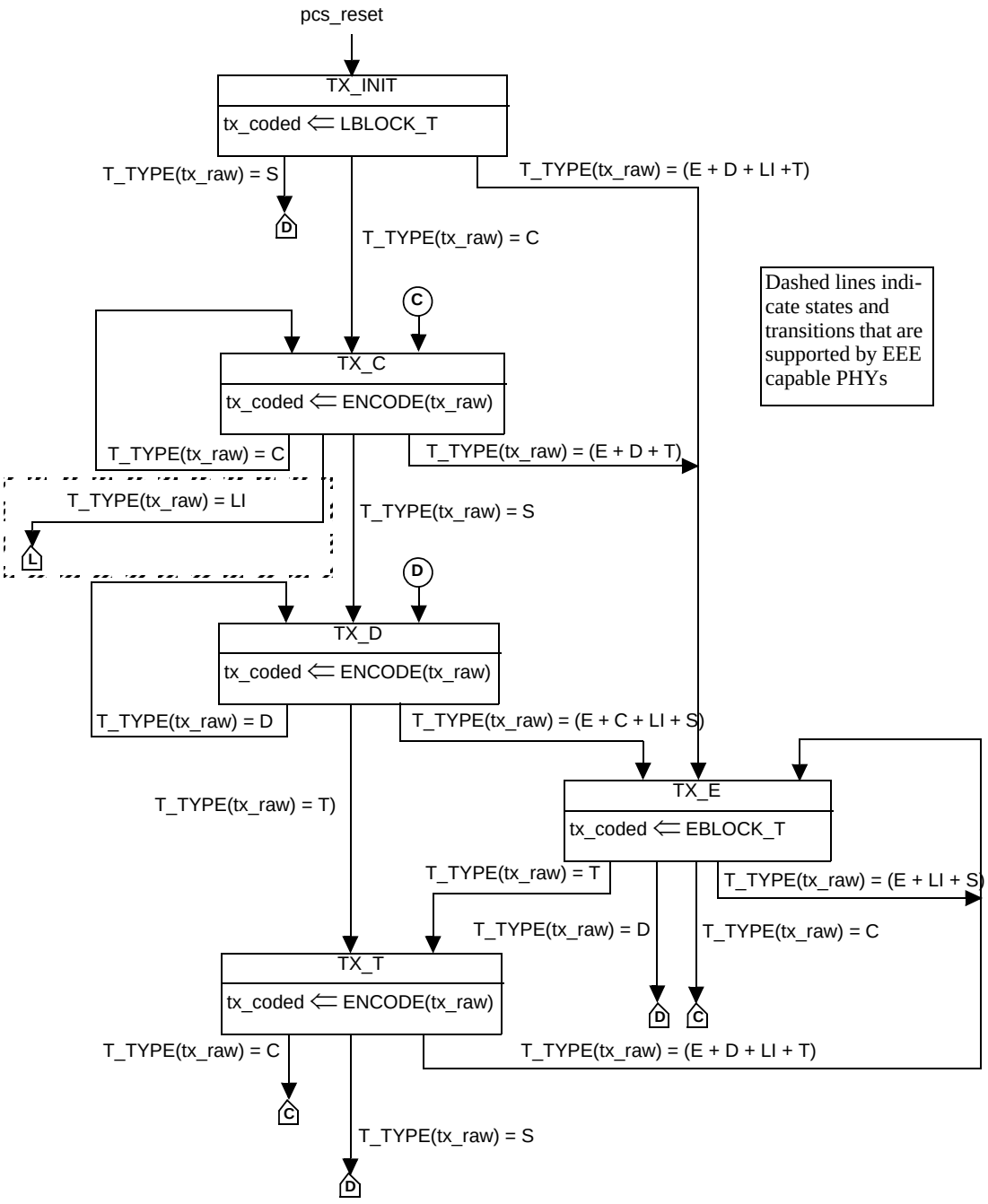


Figure 55–15—PCS 64B/65B Transmit state diagram part a)

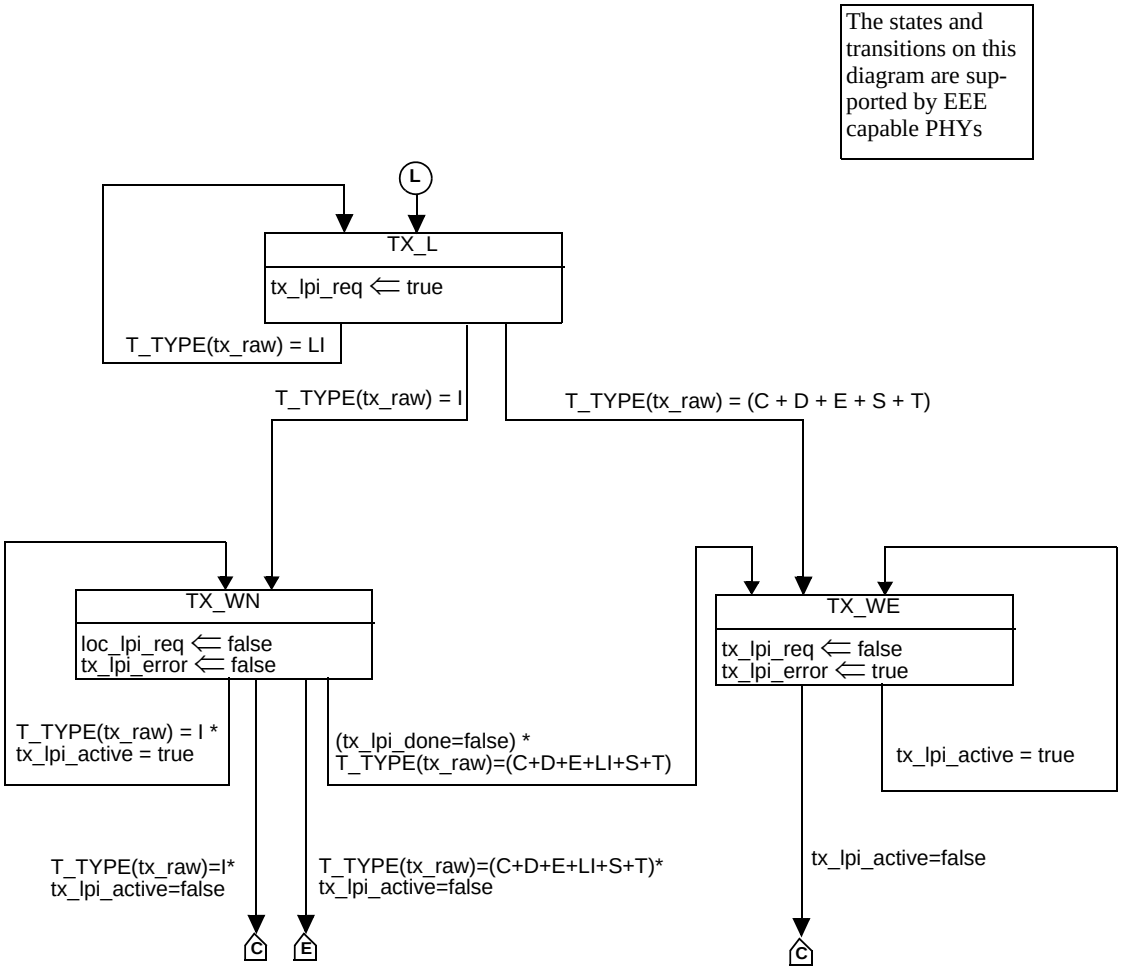


Figure 55–16—PCS 64B/65B Transmit state diagram part b)

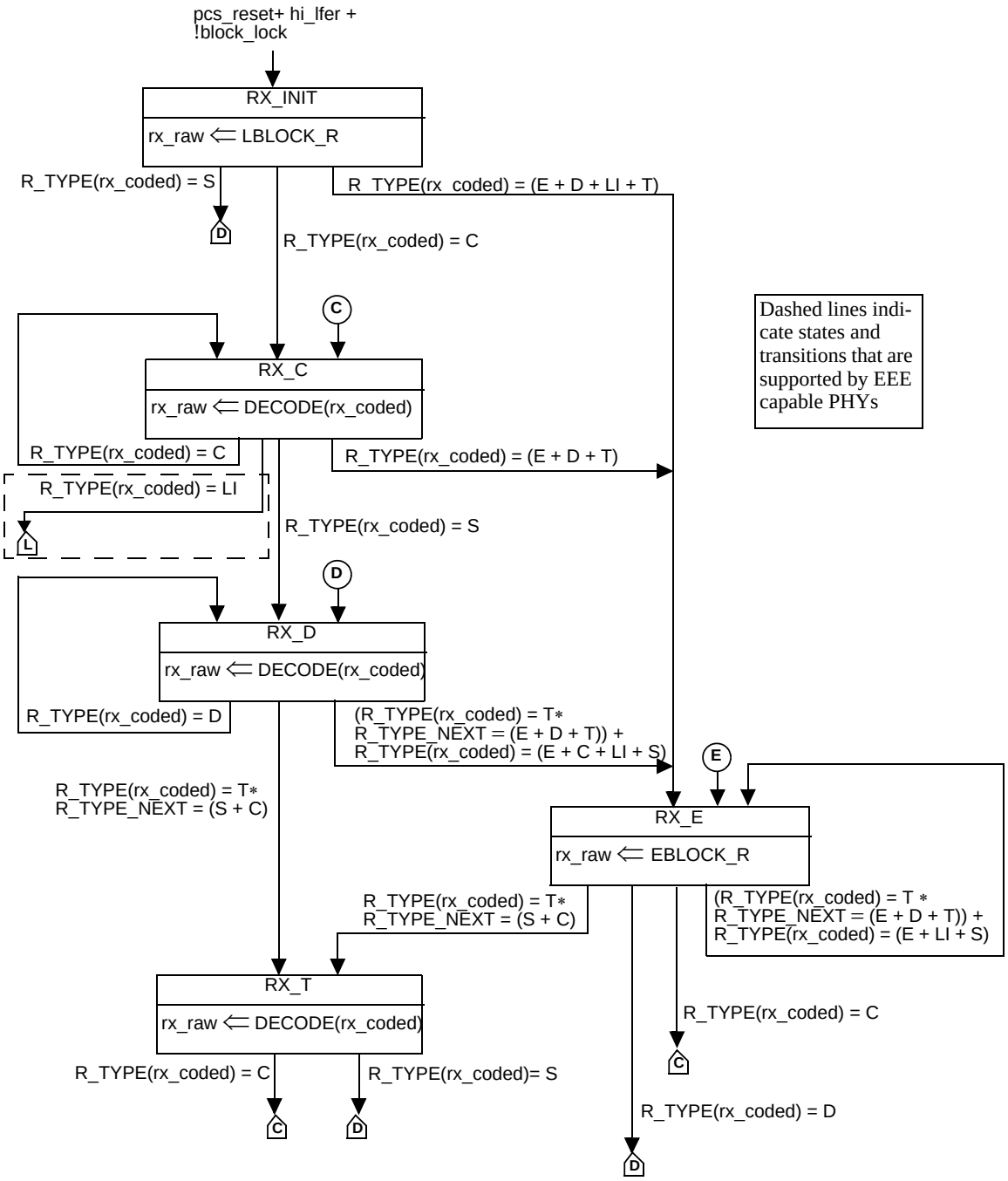


Figure 55–17—PCS 64B/65B Receive state diagram, part a)

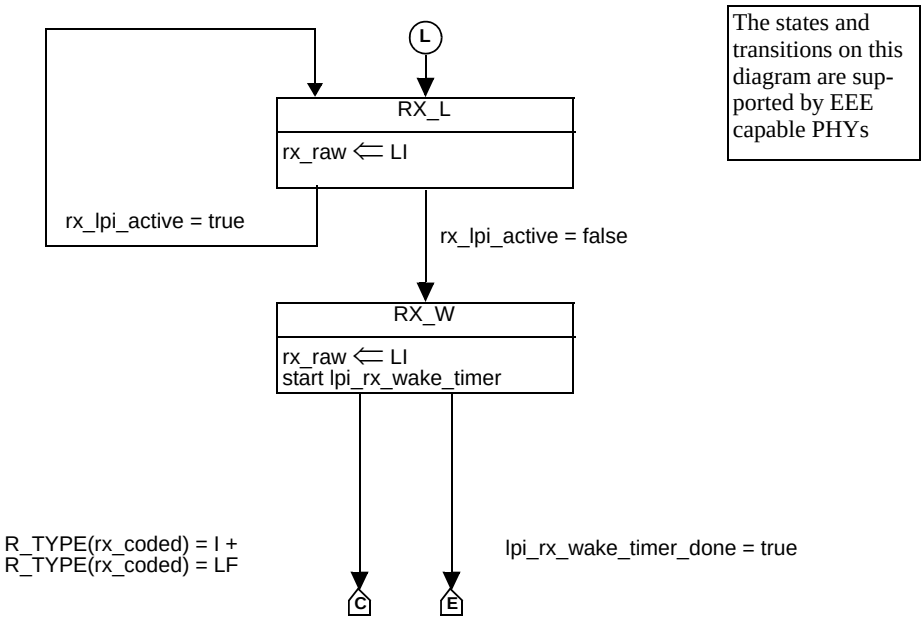


Figure 55–18—PCS 64B/65B Receive state diagram, part b)

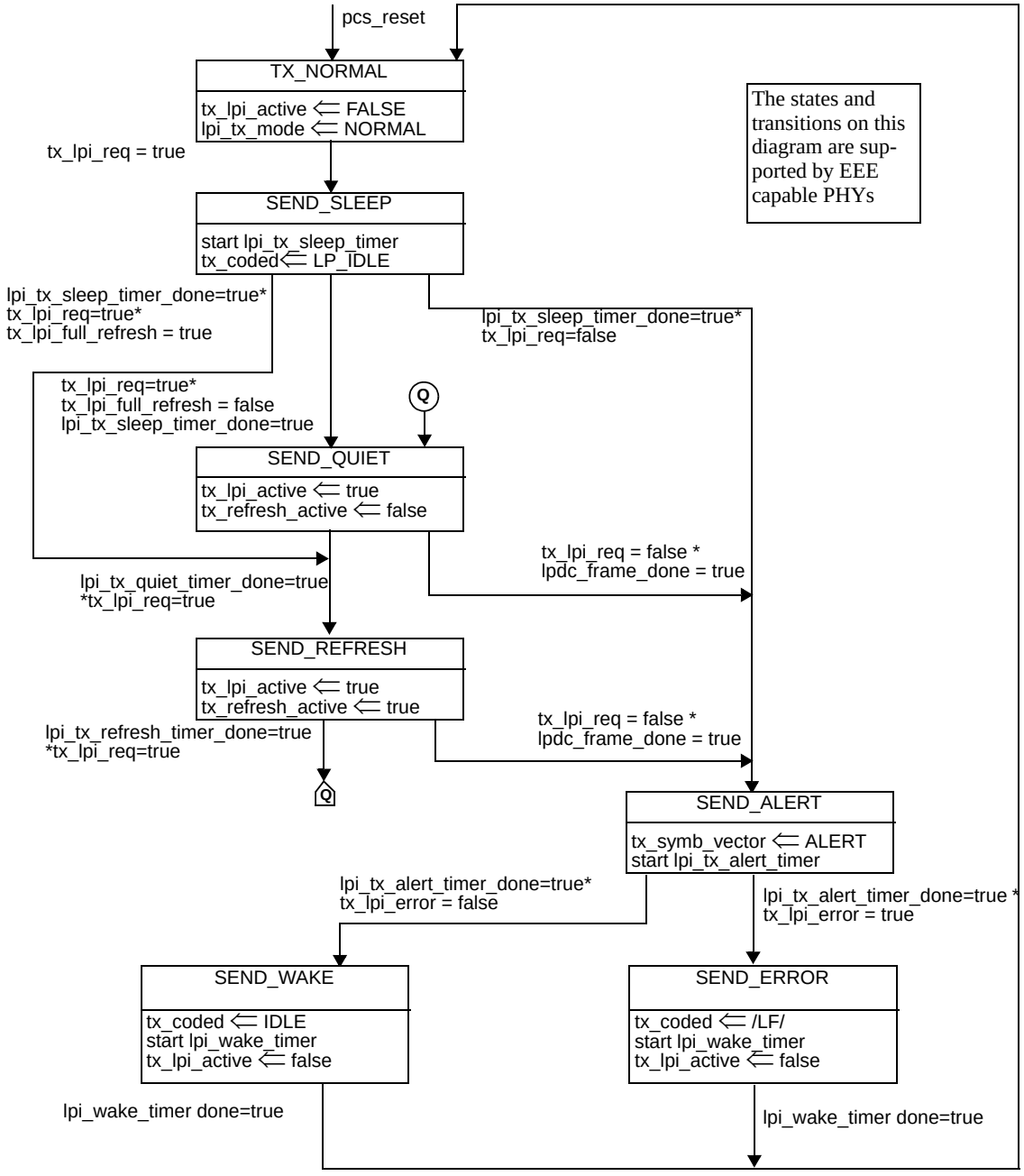


Figure 55–19—EEE transmit state diagram

55.4 Physical Medium Attachment (PMA) sublayer

55.4.1 PMA functional specifications

Replace Figure 55-17 with the figure shown below

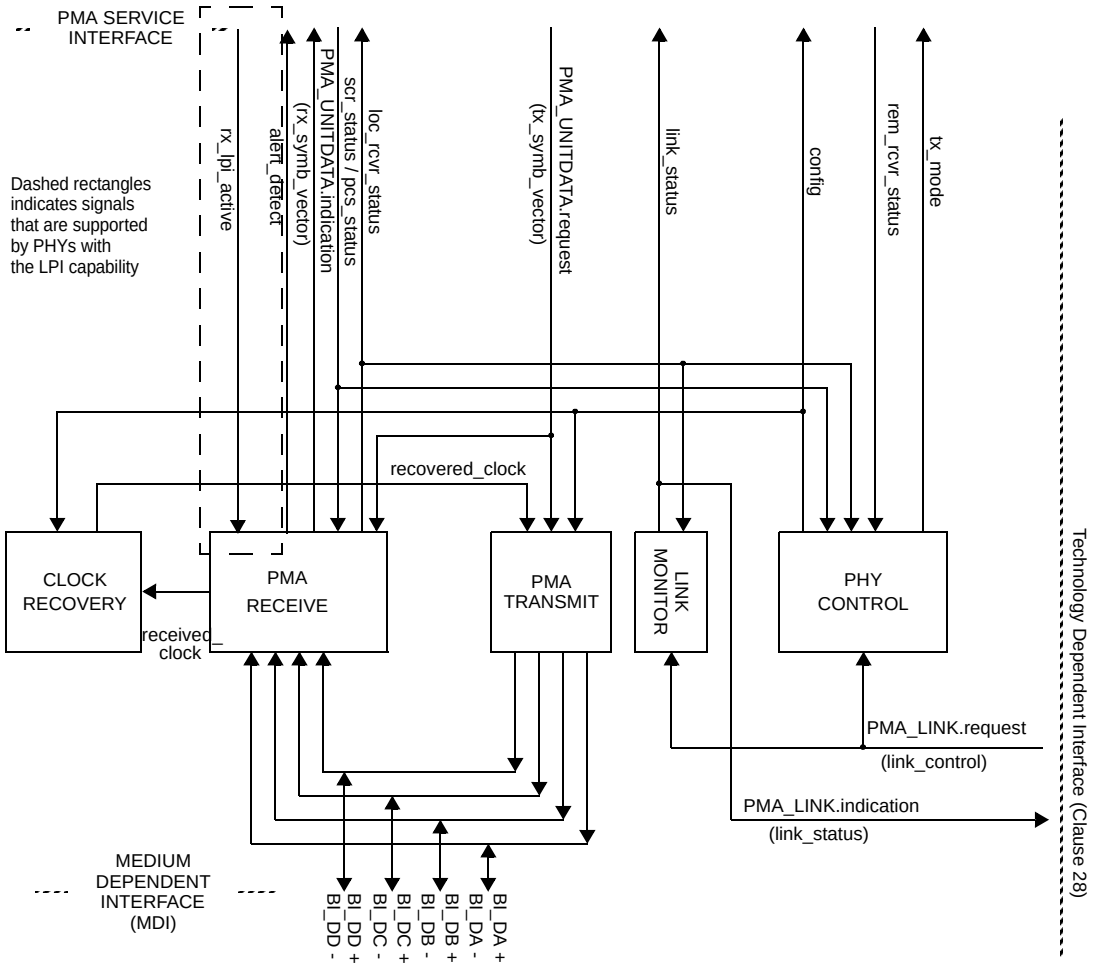


Figure 55-20 -- PMA reference diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

55.4.2.2 PMA Transmit function

Change text in 55.4.2.2 PMA Transmit function as shown below:

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. When ALERT is not indicated by tx_symb_vector then PMA transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively after processing with the THP, optional transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. The four transmitters shall be driven by the same

transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 55.4.3.1, and shall comply with the electrical specifications given in 55.5.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 55.5.3.3. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented and the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 55.4.2.7 while meeting the jitter requirements of 55.5.3.3. If loop timing is not implemented, the SLAVE PHY transmit clocking is identical to the MASTER PHY transmit clocking.

Insert the following text after the existing text in 55.4.2.2 PMA Transmit function:

EEE capable PHYs shall implement a PMA Transmit function that is able to generate the alert signal defined in 55.4.2.2.1.

Insert a new clause 55.4.2.2.1 after existing text in 55.4.2.2 PMA Transmit function as shown below:

55.4.2.2.1 Alert signal

PHYs that support the optional LPI capability will transmit the following PAM2 sequence when the PMA_UNITDATA.request parameter is set to ALERT. The alert signal is sent for a total of 4 LDPC frames and begins on a LDPC frame boundary. The alert signal is transmitted without THP filtering. The alert signal is transmitted on pair A when the PHY operates as a MASTER. The Alert signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in subclause 55.3.5.

When the PMA_CONFIG.indication parameter config is MASTER the Alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xPR_Master =

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 -9 -9

-9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9

When the PMA_CONFIG.indication parameter config is SLAVE the Alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xPR_Slave =

-9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9

-9 -9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

The alert signal is followed by a wake signal composed of repeated IDLE characters encoded using the 64B/65B encoding technique. At the start of the wake signal all THP feedback delay lines are initialized with zeros.

55.4.2.4 PMA Receive function

Change the text in 55.4.2.4 as shown below

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, ~~and~~ estimation, and LPI functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

Insert the following text after existing text in 55.4.2.4:

PMA receive functions that support the optional LPI capability shall generate alert_detect when the alert signal is detected at the receiver. The alert signal is specified in 55.4.2.2. The criterion used to generate alert_detect is left to the implementor. The receive state diagram monitors rx_lpi_req to detect the link partner signaling sleep.

Insert the following text after existing text in 55.4.2.5.14

After reaching the PCS_Data state PHYs with the EEE capability can transition to the lower power receive mode under the control of the link partner. PHYs with the EEE capability shall implement the state diagram shown in Figure 55–24.

Insert the following figure within 55.4.6.4 as a new state diagram and renumber the figures appropriately.

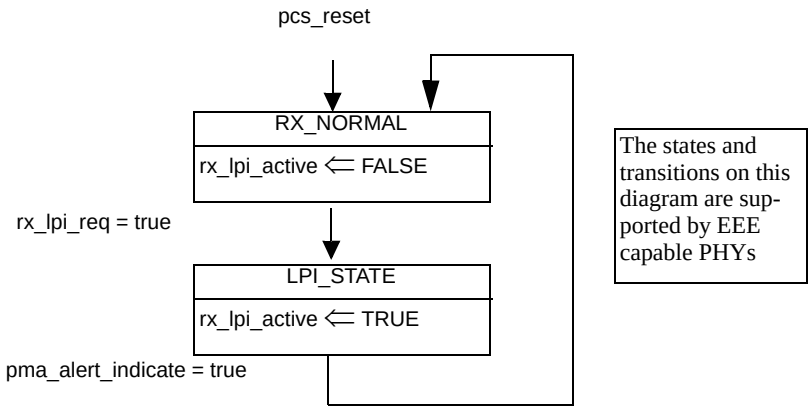


Figure 55–24—EEE receive state diagram

55.4.2.5.14 Startup sequence

Edit the text in 55.4.2.5.14 as shown below

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, each PHY announces a transition to the PCS_Test (trans_to_PCS_Test=1) and start the transition counter as described in 55.4.5.1. For PHYs with the EEE capability, further requirements for this transition are described in Clause 55.3.5.1.

55.4.5.1 State diagram variables

Edit the text in 55.4.5.1 as shown below

transition_count

This variable reports the value of the transition counter contained in the InfoField sent to the remote device. Transition_count must comply with the state diagram description given in 55.4.6.2. When the message field contains a flag for a state transition, the transition counter denotes the remaining number of InfoField until the next state transition. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a counter value of 2^9 (10 ms). The SLAVE responds prior to the counter reaching 2^6 (1 ms) with the same flag and a count value matching the MASTER. Then both PHY's transition to PMA_Coeff_Exch within one PMA frame. In non-EEE capable PHYs t~~T~~he same sequence is performed in the transition to PMA_Fine_Adjust state and PCS_Test state using the trans_to_Fine_Adjust=1 and trans_to_PCS_Test=1 flags respectively. In EEE capable PHYs the same sequence is performed in the transition to PMA_Fine_Adjust but the transition to PCS_Test is tightly controlled as described in Clause 55.3.5.1, so that both PHYs transition within an LDPC frame at the slave's MDI.

When the message field does not contain a flag for a state transition, the transition counter

is set to zero and ignored by the receiver.
Values: 0 to 2^9

55.5.3 Test modes.

Editor's Notes: *To be removed prior to publication.*

The following was proposed in taich_01_1108.pdf. The definition of further test modes may be required.

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, transmitted jitter, transmitter droop, ~~and~~ BER testing and EEE signaling.

For a PHY with an MDIO management interface, these modes shall be enabled by setting bits 1.132.15:13 and 1.132.9:8 (10GBASE-T Control Register) of the MDIO Management register set as shown in Table 55–8. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a MDIO shall provide a means to enable these modes for conformance testing.

Add two new columns and two new rows to Table 45-51 as shown below:

1.132.15	1.132.14	1.132.13	1.132.9	1.132.8	Mode
0	0	0	0	0	Normal operation.
0	0	1	0	0	Test mode 1—Setting of MASTER transmitter required by SLAVE for transmit jitter test in SLAVE mode.
0	1	0	0	0	Test mode 2—Transmit jitter test in MASTER mode.
0	1	1	0	0	Test mode 3—Transmit jitter test in SLAVE mode (if loop timing is supported).
1	0	0	0	0	Test mode 4—Transmit distortion test.
1	0	1	0	0	Test mode 5—Normal operation with no power backoff. This is for the PSD mask and power level test.
1	1	0	0	0	Test mode 6—Transmitter droop test mode.
1	1	1	0	0	Test mode 7—Pseudo random test mode for BER Monitor.
0	0	0	1	0	Test mode 8—EEE alert pattern test mode.
0	0	0	0	1	Test mode 9—Quiet/refresh signaling and frequency stability test mode

Insert the following text at the end of the existing text in 55.5.2

Test mode 8 is for testing the tranmission of the alert signal.When test mode 8 is enabled, the transmitter shall output a test pattern on transmitter A consisting of 128 zero symbols, followed by the Master alert signal, followed by 128 zero symbols, followed by the Slave alert signal. All other transmitters shall be silent.

Test mode 9 is for testing quiet/refresh signaling and frequency stability. When test mode 9 is enabled, the transmitter shall output full quiet-refresh cycles as described in Clause 55.3.5. During the refresh period the PHY shall transmit the test mode 2 pattern {two +16 symbols, followed by two -16 symbols continually} continually.

Editor's note: to be removed prior to publication.
This is a continuation of the previous editor's note.

55.5.3.1 Test fixtures

Insert the following figure after the existing text

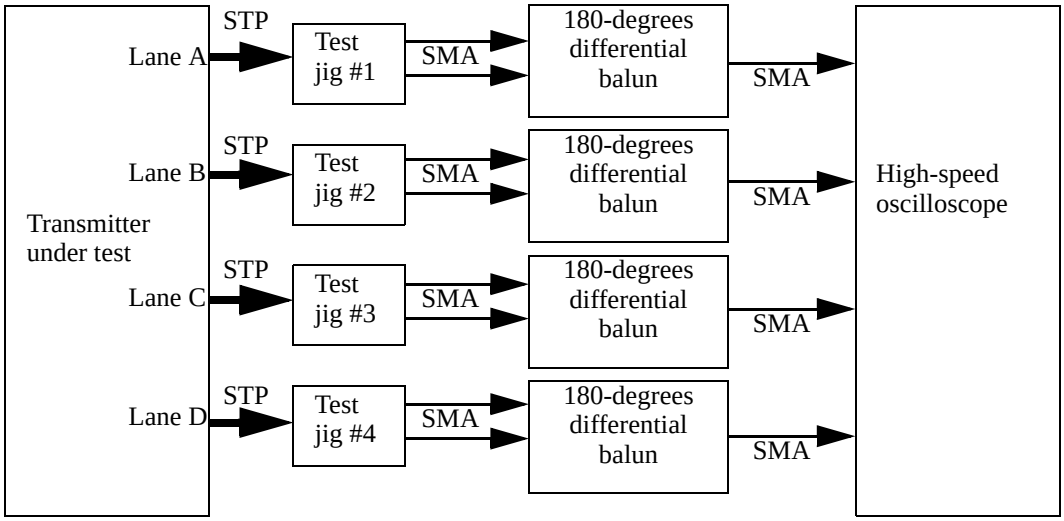


Figure 55-30—Transmitter test fixture 4 for test mode 9

55.5.3.5 Transmit clock frequency

Insert the following text after existing text in 55.5.3.5:

In the lower power mode the transmitter clock short term rate of frequency variation shall be less than 0.1 ppm/second.

55.6 Management interfaces

10GBASE-T makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

55.6.1 Support for Auto-Negotiation

Add item (d) and item (e) as new items in the list as shown below:

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.
c) To determine whether the local PHY performs PMA training pattern reset.

d) To determine whether the local PHY supports the EEE capability.

Add item e) to the existing list in clause 55.10 as shown below

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability and units thereof
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 10GBASE-T)
d) Any applicable safety warnings
e) EEE support

Editor's note: To be removed prior to publication.
This is the first draft of PICS for 802.3az Clause 55. The text should be reviewed carefully.

55.12 Protocol implementation conformance statement (PICS) proforma for Clause 55—Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
XGE	XGMII compatibility interface	46, 55.1.5	O	Yes [ ] No [ ]	Compatibility interface is supported
*LT	Support of loop timing		O	Yes [ ] No [ ]	
*EEE	Support of EEE capability		O	Yes [ ] No [ ]	

55.12.3 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	PCS Transmit function state diagram	55.3.2.2	M	Yes [ ]	See Figure 55–15
PCT1a	PCS Transmit function state diagram with EEE states	55.3.2.2	EEE:M	Yes [ ]	See Figure 55–15 and Figure 55–16
PCT2	PCS Transmit bit ordering	55.3.2.2.4	M	Yes [ ]	See Figure 55–6 and Figure 55–8
PCT3	Invalid control code handling	55.3.2.2.6	M	Yes [ ]	
PCT4	/I/ insertion and deletion	55.3.2.2.2	M	Yes [ ]	
PCT4a	/LI/ insertion and deletion	55.3.2.2.10	EEE:M	Yes [ ]	
PCT5	/O/ deletion	55.3.2.2.12	M	Yes [ ]	
PCT6	Scrambler as MASTER	55.3.2.2.15	M	Yes [ ]	
PCT7	Scrambler as SLAVE	55.3.2.2.15	M	Yes [ ]	
PCT8	CRC8	55.3.2.2.16	M	Yes [ ]	See Figure 55–11
PCT9	LDPC encoding	55.3.2.2.17	M	Yes [ ]	Generator matrix is described in Annex 55A
PCT10	DSQ128 mapping	55.3.2.2.18	M	Yes [ ]	
PCT10a	EEE Transmit function state diagram	55.3.2.2.21	EEE:M	Yes [ ]	See Figure 55–19
PCT10b	LP_IDLE input to scrambler during LPI mode	55.3.2.2.21	EEE:M	Yes [ ]	
PCT10c	lpi_tx_mode control	55.3.2.2.21	EEE:M	Yes [ ]	
PCT11	PCS test pattern mode	55.3.3	M	Yes [ ]	See Figure 55–6
PCT12	PMA training - MASTER scrambler	55.3.4	M	Yes [ ]	
PCT13	PMA training - SLAVE scrambler	55.3.4	M	Yes [ ]	
PCT14	PMA training scrambler reset	55.3.4	M	Yes [ ]	If requested by Link Partner during Auto Negotiation
PCT15	PMA training scrambler initial state	55.3.4	M	Yes [ ]	In no case shall the scrambler state be initialized to all zeros
PCT15a	Slave synchronization	55.3.5.1	EEE:M	Yes [ ]	
PCT15b	Quiet launch power	55.3.5.2	EEE:M	Yes [ ]	
PCT15c	LPI scrambler	55.3.5.3	EEE:M	Yes [ ]	The long training sequence described in 55.3.4 shall be used
PCT15d	Disable scrambler reinitialization	55.3.5.3	EEE:M	Yes [ ]	
PCT15d	Refresh using THP	55.3.5.3	EEE:M	Yes [ ]	

Item	Feature	Subclause	Status	Support	Value/Comment
PCT15e	Reset THP at the start of refresh	55.3.5.3	EEE:M	Yes [ ]	
PCT15f	Master alert on pair A, other pairs silent	55.3.5.3	EEE:M	Yes [ ]	
PCT15g	Slave alert on pair C, other pairs silent	55.3.5.3	EEE:M	Yes [ ]	
PCT15h	Inactive pairs transmit zeros	55.3.5.3	EEE:M	Yes [ ]	
PCT16	ENCODE function	55.3.5.2.4	M	Yes [ ]	Encode the block as specified in 55.3.2.2.2
PCT17	PCS loopback setup	55.3.6.3	M	Yes [ ]	

55.12.3.1 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function state diagram	55.3.2.3	M	Yes [ ]	See Figure 55–17 and state variables as specified in 55.3.5.2.
PCR2	PCS Receive bit ordering	55.3.2.3.1	M	Yes [ ]	See Figure 55–7
PCR3	Descrambling as MASTER	55.3.2.3.2	M	Yes [ ]	
PCR4	Descrambling as SLAVE	55.3.2.3.2	M	Yes [ ]	
PCR5	PMA training descrambler - MASTER	55.3.4.3	M	Yes [ ]	
PCR6	PMA training descrambler - SLAVE	55.3.4.3	M	Yes [ ]	
PCR7	DECODE operation	55.3.5.2.4	M	Yes [ ]	Decode the block as specified in 55.3.4
PCR7a					
PCR7b					
PCR8	LFER monitor	55.3.5.4	M	Yes [ ]	See state diagrams in Figure 55–14, Figure 55–15 and Figure 55–17.

55.12.3.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function	55.3.2.1	M	Yes [ ]	

55.12.4 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function	55.4.2.1	M	Yes [ ]	
PMF2	PMA transmission	55.4.2.2	M	Yes [ ]	
PMF3	Transmitter clocking	55.4.2.2	M	Yes [ ]	All driven by TX_TCLK
PMF4	PMA Transmit mapping	55.4.2.2	M	Yes [ ]	Per mathematical description given in 55.4.3.1
PMF5	PMA Transmit electrical compliance	55.4.2.2	M	Yes [ ]	See PMA electrical specifications given in 55.5
PMF6	Clocking as MASTER	55.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock
PMF7	Clocking as SLAVE in loop timed mode	55.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock
PMF8	Transmit fault mapping	55.4.2.2	O	Yes [ ]	Contribute to the transmit fault bit as specified in 45.2.1.7.4
PMF8a	Generates alert signal	55.4.2.2	EEE:M	Yes [ ]	Generates the alert signal defined in 55.4.2.2.1
PMF9	PMA Receive function performance	55.4.2.4	M	Yes [ ]	LDPC frame error rate of less than one frame in 3.2×10^9
PMF10	Receive fault mapping	55.4.2.4	O	Yes [ ]	Contribute to the receive fault bit as specified in 45.2.1.7.5
PMF10a	Implement alert_detect	55.4.2.4	EEE:M	Yes [ ]	Generates alert_detect when the alert signal is detected at the receiver
PMF11	PHY Control function	55.4.2.5	M	Yes [ ]	See state diagram in Figure 55–24 and state diagrams in Figure 55–25 and Figure 55–26
PMF12	InfoField	55.4.2.5	M	Yes [ ]	All subclauses from 55.4.2.5.1 to 55.4.2.5.13
PMF13	THP initialization	55.4.2.5.14	M	Yes [ ]	Last 16 symbols of PMA_Coeff_Exch
PMF14	PBO exchange	55.4.2.5.14	M	Yes [ ]	
PMF15	Slave PBO setting	55.4.2.5.14	M	Yes [ ]	Slave's PBO final setting should be within two levels (4dB) of the MASTER's PBO level
PMF16	THP coefficient exchange	55.4.2.5.14	M	Yes [ ]	
PMF16a	Recomended startup sequence timing	55.4.2.5.14	O	Yes [ ] No [ ]	See Table 55–6
PMF16b	Implements EEE Receive state diagram	55.4.2.5.14	EEE:M	Yes [ ]	
PMF17	Link Monitor	55.4.2.6	M	Yes [ ]	See state diagram in Figure 55–27

Item	Feature	Subclause	Status	Support	Value/Comment
PMF18	Clock Recovery function	55.4.2.7	M	Yes [ ]	
PMF19	Symbol response	55.4.3.1	M	Yes [ ]	Per electrical specifications given in 55.5
PMF20	THP filter coefficient setting	55.4.3.1	M	Yes [ ]	Fixed after startup
PMF21	PMA Transmit power backoff settings	55.4.3.1	M	Yes [ ]	
PMF22	Minimum power backoff requested	55.4.3.1	M	Yes [ ]	Per Table 55–7
PMF23	Automatic configuration	55.4.4	M	Yes [ ]	Comply with the specifications of 40.4.4.1 and 40.4.4.2
PMF24	Pair/Polarity swap detection and correction	55.4.4	M	Yes [ ]	
PMF25	PMA_CONFIG.indicate generation	55.4.5.1	M	Yes [ ]	
PMF26	Maxwait_timer expiration	55.4.5.2	M	Yes [ ]	
PMF27	Minwait_timer expiration	55.4.5.2	M	Yes [ ]	

55.12.5 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Support for Auto-Negotiation	55.6.1	M	Yes [ ]	See Clause 28
MF2	MASTER and SLAVE operation	55.6.1	M	Yes [ ]	Capable of operating either as MASTER or SLAVE
MF3	Extended next page support	55.6.1	M	Yes [ ]	
MF4	Optimized FLP timing	55.6.1	M	Yes [ ]	
MF5	Management registers	55.6.1.1	M	Yes [ ]	As defined in Table 55–10
MF6	10GBASE-T Extended Next Page bit assignments	55.6.1.2	M	Yes [ ]	As defined in Table 55–11
MF7	MASTER-SLAVE resolution with both or neither devices supporting loop timing	55.6.2	M	Yes [ ]	As defined in Table 55–12
MF8	MASTER-SLAVE resolution with one device supporting loop timing	55.6.2	M	Yes [ ]	Device supporting loop timing forced to SLAVE
MF9	Resolution completion	55.6.2	M	Yes [ ]	Successful completion of resolution treated as MASTER-SLAVE configuration resolution complete.
MF10	Seed counter	55.6.2	M	Yes [ ]	Counter provided to track number of seed attempts

Item	Feature	Subclause	Status	Support	Value/Comment
MF11	Counter set to zero at startup	55.6.2	M	Yes [ ]	
MF12	Counter increment	55.6.2	M	Yes [ ]	
MF13	Counter reset	55.6.2	M	Yes [ ]	After resolution is complete
MF14	Bit 7.33.15 set to zero after resolution is complete	55.6.2	M	Yes [ ]	After resolution is complete
MF15	Resolution fault declared	55.6.2	M	Yes [ ]	After generation of seven seeds
MF16	MASTER-SLAVE fault condition	55.6.2	M	Yes [ ]	Condition occurs when both devices manually select MASTER or SLAVE
MF17	MASTER-SLAVE fault condition bit	55.6.2	M	Yes [ ]	Set to one upon fault condition
MF18	MASTER-SLAVE fault resolution	55.6.2	M	Yes [ ]	Fault condition treated as MASTER-SLAVE resolution complete
MF19	MASTER-SLAVE fault condition indication	55.6.2	M	Yes [ ]	link_status_10GigT set to FAIL

55.12.6 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Electrical isolation	55.5.1	M	Yes [ ]	One of three electrical strength tests listed in 55.5.1
PME2	Insulation breakdown after test	55.5.1	M	Yes [ ]	>2 MΩ, measured at 500 V dc
PME3	Test modes supported	55.4.5.1	M	Yes [ ]	
PME4	Test mode enablement	55.4.5.1	M	Yes [ ]	Per management register settings shown in Table 55–8
PME5	The test modes only change the data symbols	55.4.5.1	M	Yes [ ]	
PME6	Alternate way to enable the test modes	55.4.5.1	O	Yes [ ]	Mandatory for PHYs without MDIO
PME7	Test mode 1 operation	55.4.5.1	M	Yes [ ]	
PME8	Test mode 2 operation	55.4.5.1	M	Yes [ ]	
PME9	Test mode 3 operation, pair D	55.4.5.1	LT:M	Yes [ ] N/A [ ]	Mandatory for PHY that supports loop timing
PME10	Test mode 3 operation, pairs A, B and C	55.4.5.1	M	Yes [ ]	Transmit silence
PME11	Test mode 4 waveform	55.4.5.1	M	Yes [ ]	Tones per Table 55–9
PME12	Test mode 4 levels	55.4.5.1	M	Yes [ ]	
PME13	Test mode 5 operation	55.4.5.1	M	Yes [ ]	
PME14	Test mode 6 operation	55.4.5.1	M	Yes [ ]	
PME15	Test mode 7 operation	55.4.5.1	M	Yes [ ]	
PME16	Text fixture 3 isolation	55.4.5.1	M	Yes [ ]	>30 dB between signals on any of {pairs A, B, C} and pair D
PME17	Transmitter nominal load	55.5.3	M	Yes [ ]	
PME18	AC coupling to the MDI	55.5.3	M	Yes [ ]	
PME19	Droop test	55.5.3.1	M	Yes [ ]	
PME20	SFDR of transmitter	55.5.3.2	M	Yes [ ]	
PME21	Transmitter jitter as MASTER	55.5.3.3	M	Yes [ ]	
PME22	Transmitter jitter as loop-timed SLAVE	55.5.3.3	LT: M	N/A [ ] Yes [ ]	Applicable only if loop timing is supported
PME23	Transmit power level	55.5.3.4	M	Yes [ ]	
PME24	Transmitter PSD	55.5.3.4	M	Yes [ ]	
PME25	MASTER symbol rate	55.5.3.5	M	Yes [ ]	
PME25a	Transmit clock frequency variation	55.5.3.5	EEE: M	Yes [ ]	
PME26	BER over a 55.7 compliant link	55.5.4.1	M	Yes [ ]	

Item	Feature	Subclause	Status	Support	Value/Comment
PME27	Receiver frequency tolerance	55.5.4.2	M	Yes [ ]	
PME28	Alien noise tolerance	55.5.4.4	M	Yes [ ]	

55.12.7 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	MDI compatibility	55.7	M	Yes [ ]	
LKS2	Insertion loss of each duplex channel	55.7.2.1	M	Yes [ ]	See Equation (55–11)
LKS3	Return loss	55.7.2.3	M	Yes [ ]	See (55–12)
LKS4	NEXT loss within pairs in a link segment	55.7.2.4.1	M	Yes [ ]	See (55–13)
LKS5	Power sum NEXT loss	55.7.2.4.2	M	Yes [ ]	See (55–14)
LKS6	Worst pair ELFEXT loss	55.7.2.4.4	M	Yes [ ]	See (55–18)
LKS7	Power sum ELFEXT loss	55.7.2.4.5	M	Yes [ ]	See (55–20)
LKS8	Propagation delay	55.7.2.5	M	Yes [ ]	
LKS9	Delay skew	55.7.2.6	M	Yes [ ]	
LKS10	Delay skew change	55.7.2.6	M	Yes [ ]	
LKS11	Power sum ANEXT loss	55.7.3.1.1	M	Yes [ ]	See (55–23)
LKS12	Average PS ANEXT loss	55.7.3.1.1	M	Yes [ ]	See (55–25)
LKS13	PSANEXT_constant	55.7.3.1.2	M	Yes [ ]	See (55–26)
LKS14	IL(250) used in PSANEXT_ constant equation	55.7.3.1.2	M	Yes [ ]	Actual measured insertion loss at 250 MHz
LKS15	PS AELFEXT loss	55.7.3.2.1	M	Yes [ ]	See (55–32)
LKS16	Average PS AELFEXT loss	55.7.3.2.1	M	Yes [ ]	See (55–34)
LKS17	PSAELFEXT_constant	55.7.3.2.2	M	Yes [ ]	See (55–35)
LKS18	IL(250) used in PSAELFEXT_ constant equation	55.7.3.2.2	M	Yes [ ]	Actual measured insertion loss at 250 MHz
LKS19	Alien crosstalk margin *YL*	55.7.3.3	M	Yes [ ]	Greater than zero

55.12.8 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	55.8.1	M	Yes [ ]	8-Way connector per IEC 60603-7:1996
MDI2	Cabling connector	55.8.1	M	Yes [ ]	Plug
MDI3	PHY connector	55.8.1	M	Yes [ ]	Jack (as opposed to plug)
MDI4	MDI connector jack plus plug performance	55.8.2	M	Yes [ ]	Per category 6 requirements specified in ANSI/TIA/EIA-568-B.2-1-2002 and ISO/IEC 11801:2002

Item	Feature	Subclause	Status	Support	Value/Comment
MDI5	Mated MDI connector FEXT loss	55.8.2	M	Yes [ ]	Per (55–53)
MDI6	MDI power down	55.8.2	M	Yes [ ]	
MDI7	MDI return loss	55.8.2.1	M	Yes [ ]	
MDI8	MDI impedance balance	55.8.2.2	M	Yes [ ]	
MDI9	MDI fault tolerance to short circuits	55.8.2.3	M	Yes [ ]	No damage with an indefinite short
MDI10	Recovery from short	55.8.2.3	M	Yes [ ]	
MDI11	Short circuit current	55.8.2.3	M	Yes [ ]	Less than 300 mA
MDI11a	Connection to PSE	55.8.2.3	M	Yes [ ]	No damage to PHY
MDI11b	Connection to PSE	55.8.2.3	M	Yes [ ]	No damage to PSE
MDI12	Common-mode impulse tolerance	55.8.2.3	M	Yes [ ]	1000 V common-mode impulse of either polarity

55.12.9 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	55.9.1	M	Yes [ ]	IEC 60950-1:2001
ENV2	Installation isolation integrity	55.9.3	INS:M	N/A [ ] Yes [ ]	No electrical contact with unintended conductors or ground
ENV3	Phone voltage immunity	55.9.4	M	Yes [ ]	
ENV4	Electromagnetic compatibility	55.9.5	INS:M	N/A [ ] Yes [ ]	With local and national codes

55.12.10 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TR1	Delay	55.11	M	Yes [ ]	

Revisions to IEEE Std 802.3-2008, Clause 69

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

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69. Introduction to Ethernet operation over electrical backplanes

Change the Scope in 69.1.1 to read as follows:

69.1.1 Scope

Ethernet operation over electrical backplanes, also referred to as "Backplane Ethernet", combines the IEEE 802.3 Media Access Control (MAC) and MAC Control sublayers with a family of Physical Layers defined to support operation over a modular chassis backplane.

Backplane Ethernet supports the IEEE 802.3 MAC operating at 1000 Mb/s or 10 Gb/s. For 1000 Mb/s operation, the family of 1000BASE-X Physical Layer signaling systems is extended to include 1000BASE-KX. For 10 Gb/s operation, two Physical Layer signaling systems are defined. For operation over four logical lanes, the 10GBASE-X family is extended to include 10GBASE-KX4. For serial operation, the 10GBASE-R family is extended to include 10GBASE-KR.

Backplane Ethernet also specifies an Auto-Negotiation function to enable two devices that share a backplane link segment to automatically select the best mode of operation common to both devices.

Backplane Ethernet optionally supports Energy Efficient Ethernet to reduce energy consumption. The Energy Efficient Ethernet capabilities are advertised during Auto-Negotiation.

Change the Scope in 69.1.2 to read as follows:

69.1.2 Objectives

The following are the objectives of Backplane Ethernet:

a) Support full-duplex operation only.
b) Provide for Auto-Negotiation among Backplane Ethernet Physical Layer signaling systems.
c) Not preclude compliance to CISPR/FCC Class A for RF emission and noise immunity.
d) Support operation of the following PHY over differential, controlled impedance traces on a printed circuit board with 2 connectors and total length up to at least 1 m consistent with the guidelines of Annex 69B.
    i) a 1 Gb/s PHY
    ii) a 4-lane 10 Gb/s PHY
    iii) single-lane 10 Gb/s PHY
e) Support a BER of 10^{-12} or better.
f) Optionally support Energy Efficient Ethernet.

69.2 Summary of Backplane Ethernet Sublayers

69.2.3 Physical Layer signaling systems

Change Table 69-1 to reference EEE Clause

Table 69–1—Nomenclature and clause correlation

Nomenclature	Clause									
	36	**48**	**49**	**51**	**70**	**71**	**72**	**73**	**74**	**78**
	1000BASE-X PCS/PMA	**10GBASE-X PCS/PMA**	**10GBASE-R PCS**	**Serial PMA**	**1000BASE-KX PMD**	**10GBASE-KX4 PMD**	**10GBASE-KR PMD**	**AUTO-NEGOTIATION**	**10GBASE-R FEC**	**Energy Efficient Ethernet**
1000BASE-KX	M[a]				M			M		O
10GBASE-KX4		M				M		M		O
10GBASE-KR			M	M			M	M	O	O

[a]O = Optional, M = Mandatory

Insert 69.2.6 as follows

69.2.6 Low-Power Idle

With the optional Energy Efficient Ethernet feature, described in Clause 78, the Backplane Ethernet PHYs can achieve lower power consumption during periods of low link utilization. The EEE capabilities are advertised during Auto-Negotiation for Backplane Ethernet. The Backplane Ethernet LPI allows each link direction to enter sleep, refresh or wake states asymmetric from the other direction.

Revisions to IEEE Std 802.3-2008, Clause 70

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Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

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70. Physical Medium Dependent Sublayer and Baseband Medium, Type 1000BASE-KX

70.1 Overview

Replace Table 70-1 with the following:

Table 70–1—PHY (Physical Layer) clauses associated with the 1000BASE-KX PMD

Associated clause	1000BASE-KX
35—GMII[a]	Optional
36—1000BASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
78-- Energy Efficient Ethernet	Optional

[a]The GMII is an optional interface. However, if the GMII is not implemented, a conforming implementation must behave functionally as though the RS and GMII were present.

Insert the following text at the end of section 70.1

A 1000BASE-KX PHY may optionally enter a low power state to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The assertion of low

power idle at the GMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as low power idle at the GMII. When low power idle is received, an Energy Efficient 1000BASE-KX PHY sends sleep symbols, then ceases transmission and deactivates transmit to conserve energy. When the receiver sees the sleep symbols, it transitions to a quiet state, The PHY periodically transmits during the quiet period to allow the remote PHY to refresh its receiver clocks (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the GMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power state.

Insert the following section after 70.3

70.3a PCS requirements for Low Power Idle

The KX PHY will use the 1000BASE-X PCS LPI modes described in 36.2.5.2.8.

70.3a PMA requirements for Low Power Idle

The KX PHY will use the 1000BASE-X PMA LPI modes described in 36.2.5.1.6. If Energy Efficient Ethernet is supported, the PMA associated with this PMD shall provide PMD_SIGNAL.indication(signal_detect) as described in 39.2.3.

70.5 PMD MDIO function mapping

Change Table 70-3 to include LPI control.

Table 70–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
LPI idle state indication	Status register 1	1.1.3	PMD_LPI_active
Transmit fault ability	1000BASE-KX status register	1.161.13	PMD_Transmit_fault_ability
Receive fault ability	1000BASE-KX status register	1.161.12	PMD_Receive_fault_ability
Transmit fault	1000BASE-KX status register	1.161.11	PMD_transmit_fault
Receive fault	1000BASE-KX status register	1.161.10	PMD_receive_fault
PMD transmit disable ability	1000BASE-KX status register	1.161.8	PMD_transmit_disable_ability
Signal detect from PMD	1000BASE-KX status register	1.161.0	PMD_signal_detect

70.6 PMD functional specifications

Change Table 70-3 to include LPI status

Change the text in 70.6.4 to read as follows:

70.6.4 PMD signal detect function during baseline operation

PMD signal detect is optional for 1000BASE-KX baseline operation but mandatory for support of Energy Efficient Ethernet. When Energy Efficient Ethernet is not implemented for 1000BASE-KX, PMD singal detect is optional and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

Insert the following section after 70.6.4

70.6.4a PMD signal detect for Energy Efficient Ethernet

If Energy Efficient Ethernet is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. The SIGNAL_DETECT parameter shall be set to OK within T_{SA} after a step increase in the differential peak-to-peak voltage exceeding the Signal_Detect assertion threshold of V_{SA} as specified in Table 70-6

The SIGNAL_DETECT parameter shall be set to FAIL within a maximum of T_{SD} after a step decrease in the differential peak-to-peak input voltage from a value greater than the Signal_Detect Assertion Threshold to a differential signal level less than the Signal_Detect Deassertion Threshold of V_{SD} as specified in Table 70-6

Change the 70.6.5 to read as follows:

70.6.5 PMD transmit disable function

The PMD_transmit_disable function is optional for normal operation, but mandatory for support of Energy Efficient Ethernet. When implemented, it allows the transmitter to be disabled with a single variable.

a) When the PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 70–4.
b) If a PMD_fault (70.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 70.6.6, shall not be affected by PMD_transmit_disable.
d) If Energy Efficient Ethernet is supported, the PMD transmit disable function shall turn off the transmitter such that the differential peak-to-peak output voltage is less than V_{TQ} within T_{TD} of tx_quiet being asserted as defined in Table 70-4. The PMD_transmit_disable function shall turn on the transmitter such that the differential peak-to-peak output voltage is greater than V_{TW} within T_{TA} of tx_quiet being deasserted as defined in Table 70-4.

Insert the following section after 70.6.9

70.6.10 PMD Low Power Idle function

The PMD Low Power Idle function controls the transitions between Active, Sleep, Quiet, Refresh, and Wake states. Implementation of the function is optional. Energy Efficient Ethernet capabilities and parameters are advertised during the Backplane Auto-negotiation as described in Clause 45. The transmitter on the local device informs the remote link partner's receiver when to sleep, refresh and wake. The local receiver's transitions are controlled by the remote link partner's transmitter and change independently from the local transmitter's states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards /I/ during the wake phase.

The following primatives are defined on the PMD Service Intereface when Energy Efficient Ethernet is supported:

PMD_RXQUIET.request
PMD_TXQUIET.request

70.6.10.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when Low Power Idle mode is implemented to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. See Clause 36.2.4.12a. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

70.6.10.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

70.6.10.1.2 When generated

The PCS generates this primitive to indicate the Quiet line state of Low Power Receive state.

70.6.10.1.3 Effect of receipt

This variable is from the Receive process of PCS to control the power saving function of local receiver.

70.6.10.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when Low Power Idle mode is implemented to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See Clause 70.6.5. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

70.6.10.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

70.6.10.2.2 When generated

The PCS generates this primitive to indicate the Quiet state of Low Power Transmit state.

70.6.10.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 70.6.5.

70.7 1000BASE-KX electrical characteristics

70.7.1 Transmitter characteristics

Change table 70-4 as indicated below.

Transmitter characteristics at TP1 are summarized in Table 70–4 and detailed in 70.7.1.1 through 70.7.1.9.

Table 70–4—Transmitter characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Signaling speed	70.7.1.3	1.25 ± 100 ppm	GBd
Differential peak-to-peak output voltage	70.7.1.5	800 to 1600	mV
Differential peak-to-peak output voltage (min.) with TX enabled (V_{TW})	70.6.5	Need Value	mV
Differential peak-to-peak output voltage (max.) with TX disabled (V_{TQ})	70.6.5	30	mV
Transmitter deactivation time from active (T_{TD}) for EEE	70.6.5	Need Value	μs
Transmitter activation time from EEE quiet mode (T_{TA})	70.6.5	Need Value	μs
DC common-mode voltage limits	70.7.1.5	–0.4 to 1.9	V
Differential output return loss (min.)	70.7.1.6	[See Equation (70–1) and Equation (70–2)]	dB
Transition time[a] (20%–80%)	70.7.1.7	60 to 320	ps
Output jitter (max. peak-to-peak) Deterministic jitter[b] Random jitter Total jitter[c]	70.7.1.8	 0.10 0.15 0.25	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]Deterministic jitter is already incorporated into the differential output template.
[c]At BER 10^{-12}.

70.7.2 Receiver characteristics

Change table 70-6 as indicated

Receiver characteristics at TP4 are summarized in Table 70–6 and detailed in 70.7.2.1 through 70.7.2.5.

Table 70–6—Receiver characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Bit error ratio	70.7.2.1	10^{-12}	
Signaling speed	70.7.2.2	1.25 ± 100 ppm	GBd
Receiver coupling	70.7.2.3	AC	
Differential input peak-to-peak amplitude (max.)	70.7.2.4	1600	mV
Differential input peak-to-peak amplitude (min.) to assert Signal Detect(V_{SA})	70.6.4a	Need Value	mV
Differential input peak-to-peak amplitude (max.) to deassert Signal Detect (V_{SD})	70.6.4a	Need Value	mV
Signal Detect deactivation time from active to quiet (T_{SD}) for EEE	70.6.4a	Need Value	µs
Signal Detect activation time from EEE quiet mode (T_{SA})	70.6.4a	Need Value	µs
Differential input return loss (min.)	70.7.2.5	[See Equation (70–1) and Equation (70–2)]	dB

70.10 Protocol implementation conformance statement (PICS) proforma for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX[1]

Replace Table in Section 70.10.3 with the following

70.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
GMII	GMII	70.1, 35	Interface is supported	O	Yes [ ] No [ ]
PCS	Support of 1000BASE-X PCS/ PMA	70.1, 36		M	Yes [ ] No [ ]
AN	Auto-Negotiation for Backplane Ethernet	70.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
FD	Full duplex operation	70.1	Clause 36 PCS/PMA when used with 1000GBASE-KX supports full-duplex operation only	M	Yes [ ]
DC	Delay Constraints	70.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO interface	70.5	Device implements MDIO	O	Yes [ ] No [ ]
*SD	Signal Detect Generation	70.6.4	Signal detect implemented	O	Yes [ ] No [ ]
*TD	PMD_transmit_disable	70.6.5		O	Yes [ ] No [ ]
LPI	Low Power Idle	70.6.10	Low Power Idle	O	Yes [ ] No [ ]

70.10.4 PICS proforma tables for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX.

Replace the table in section 70.10.4.1 with the following

70.10.4.1 PMD functional specifications

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	70.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	70.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS3	Receive function	70.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	70.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS5	PMD Signal Detect function	70.6.4	Continuously reported OK via PMD_SIGNAL.indication (SIGNAL_DETECT).	!SD:M	Yes [ ] No [ ]
FS6	PMD_fault	70.6.5	Transmit disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS7	PMD_transmit_disable	70.6.5	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS8	Loopback Function	70.6.6	Loopback function provided	M	Yes [ ]
FS9	Loopback affect on Transmitter	70.6.6	Loopback function does not disable transmitter	M	Yes [ ]
FS10	Low Power Idle function	70.6.10	Stops transmitting during LPI quiet state	O	Yes [ ] No [ ] N/A [ ]

Revisions to IEEE Std 802.3-2008, Clause 71

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71. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KX4

71.1 Overview

Insert the following text at the end of section 71.1

A 10GBASE-KX4 PHY may optionally enter a low power state to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The assertion of low power idle at the XGMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as low power idle at the XGMII. When low power idle is received, an Energy Efficient 10GBASE-KX4 PHY sends sleep symbols, then ceases transmission and deactivates transmit to conserve energy. When the receiver sees the sleep symbols it transitions to a quiet state. The PHY periodically transmits during the quiet period to allow the remote PHY to refresh its receiver clocks (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the XGMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power state.

Replace Table 71-1 with the following.

Table 71–1—PHY (Physical Layer) clauses associated with the 10GBASE-KX4 PMD

Associated clause	10GBASE-KX4
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
78--Energy Efficient Ethernet	Optional

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

71.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KX4 PMD utilizes the PMD service interface defined in 53.1.1.

71.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 48.2.7.)

71.5 PMD MDIO function mapping

Replace tables 72-3 with the following

.

71.6.4 Global PMD signal detect function during baseline operations

Global PMD signal detect is optional for 10GBASE-KX4 baseline operation but mandatory for Energy Efficient Ethernet. For baseline operation, its definition is beyond the scope of this standard. When Global PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

Insert the following section after 71.6.5

71.6.4a PMD signal detect for Energy Efficient Ethernet

If Energy Efficient Ethernet is supported, a local PMD signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously. The PMD SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. SIGNAL_DETECT shall be a global indicator of the presence of backplane sig-

Table 71–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
LP Idle state indication	Status register 1	1.1.3	PMD_LPI_active
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

nals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-KX4 signal is being received, however, the SIGNAL_DETECT shall be set to OK within T_{SA} after the absolute differential peak-to-peak input voltage on each of the four lanes at the MDI has exceeded V_{SA} for at least 1 UI (unit interval) as specified in Table 71-4. After any such assertion of SIGNAL_DETECT = OK, SIGNAL_DETECT = FAIL shall not be asserted for at least T_{SD}. The PMD shall assert SIGNAL_DETECT = FAIL within T_{SD} if the absolute differential peak-to-peak input voltage on any of the four lanes has dropped below V_{SD} and has remained below V_{SD} for longer than T_{SA}.

71.6.6 Global PMD transmit disable function

Change 71.6.6 to the following

The Global_PMD_transmit_disable function is optional for normal operation but mandatory for support of Energy Efficient Ethernet. When implemented for normal operation, it allows all of the transmitters to be disabled with a single variable.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by Global_PMD_transmit_disable.
d) If Energy Efficient Ethernet is supported, the PMD_transmit_disable function shall turn off all transmitter lanes such that the differential peak-to-peak output voltage is less than V_{TQ} within T_{TD} of tx_quiet being asserted as defined in Table 71-4. The PMD_transmit_disable function shall turn on all transmitter lanes such that the differential peak-to-peak output voltage is greater than V_{TW} within T_{TA} of tx_quiet being deasserted as defined in Table 71-4.

Insert the following section after 71.6.11

71.6.12 PMD Low Power Idle function

The PMD Low Power Idle function controls the transitions between Active, Sleep, Quiet, Refresh, and Wake states. Implementation of the function is optional. Energy Efficient Ethernet capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in Clause 45. The transmitter on the local device will inform the remote link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the remote link partners transmitter and can change independent of the local transmitter states and transitions.

The transmitter sends /LPI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards ||I|| during the wake phase.

The following primitives are defined on the PMD Service Interface when Energy Efficient Ethernet is supported:

PMD_RXQUIET.request
PMD_TXQUIET.request

71.6.12.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when Low Power Idle mode is implemented to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. See Clause 48.2.x. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

71.6.12.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

71.6.12.1.2 When generated

The PCS generates this primitive to indicate the Quiet line state of Low Power Receive state.

71.6.12.1.3 Effect of receipt

This variable is from the Receive process of PCS to control the power saving function of local receiver.

71.6.12.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when Low Power Idle mode is implemented to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See subclause 71.6.6. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

71.6.12.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

71.6.12.2.2 When generated

The PCS generates this primitive to indicate the Quiet state of Low Power Transmit state.

71.6.12.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 71.6.6.

71.7 Electrical characteristics for 10GBASE-KX4

71.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 71–4.

Table 71–4—Transmitter characteristics for 10GBASE-KX4

Parameter	Subclause reference	Value	Units
Signaling speed, per lane	71.7.1.3	3.125 ± 100 ppm	GBd
Differential peak-to-peak output voltage	71.7.1.4	800 to 1200	mV
Differential peak-to-peak output voltage (min.) with TX enabled (V_{TW})	71.6.6	Need Value	mV
Differential peak-to-peak output voltage (max.) with TX disabled (V_{TQ})	71.6.6, 71.6.7	30	mV
Transmitter deactivation time from active (T_{TD}) for EEE	71.6.6	Need Value	ns
Transmitter activation time from EEE quiet mode (T_{TA})	71.6.6	Need Value	ns
Common-mode voltage limits	71.7.1.4	–0.4 to 1.9	V
Differential output return loss (min.)	71.7.1.5	[See Equation (71–1) and Equation (71–2)]	dB
Differential output template	71.7.1.6	[See Figure 71–5 and Table 71–5]	V
Transition time[a] (20%-80%)	71.7.1.7	60 to 130	ps
Output jitter (max. peak-to-peak) Random jitter Deterministic jitter Total jitter[b]	71.7.1.8	 0.27 0.17 0.35	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]At BER 10^{-12}.

71.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 71–6 and detailed in 71.7.2.1 through 71.7.2.5.

Table 71–6—Receiver characteristics

Parameter	Subclause reference	Value	Units
Bit error ratio	71.7.2.1	10^{-12}	
Signaling speed, per lane	71.7.2.2	3.125 ± 100 ppm	GBd
Unit interval (UI) nominal	71.7.2.2	320	ps
Receiver coupling	71.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	71.7.2.4	1600	mV
Differential input peak-to-peak amplitude (min.) to assert Signal Detect(V_{SA})	71.6.4a	Need Value	mV
Differential input peak-to-peak amplitude (max.) to deassert Signal Detect (V_{SD})	71.6.4a	Need Value	mV
Signal Detect deactivation time from active to quiet (T_{SD}) for EEE	71.6.4a	Need Value	ns
Signal Detect activation time from EEE quiet mode (T_{SA})	71.6.4a	Need Value	ns
Differential input return loss[a] (minimum)	71.7.2.5	[See Equation (71–1) and Equation (71–2)]	dB

[a]Relative to 100 Ω differential.

71.10 Protocol implementation conformance statement (PICS) proforma for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4[1]

Replace the table in 71.10.3 with the following

71.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	71.1, 46	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	71.1, 47		O	Yes [ ] No [ ]
PCS	Support of 10GBASE-X PCS/ PMA	71.1, 48		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	71.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
DC	Delay Constraints	71.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO interface	71.5	Device implements MDIO	O	Yes [ ] No [ ]
*SD	Signal Detect Generation	71.6.4	Signal detect implemented	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	71.6.6		O	Yes [ ] No [ ]
LPI	Low Power Idle function	71.6.10	Low Power Idle supported	O	Yes [ ] No [ ]

71.10.4 PICS proforma tables for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4

Replace the table in section 71.10.4.2 with the following.

71.10.4.2 PMD functional specifications

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	71.6.2	Convert the 4 logical signals requested by PMD_UNITDATA.request (tx_bit<0:3>) to 4 electrical signals	M	Yes [ ]
FS2	Delivery to the MDI	71.6.2	Supplies 4 electrical signal streams for delivery to the MDI per 71.7.1	M	Yes [ ]
FS3	Transmitter signal	71.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS4	Transmit Signal order	71.6.2	PMD_UNITDATA.request(tx_bit<0:3>) = (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>)	M	Yes [ ]
FS5	Receive function	71.6.3	Convert the 4 electrical signals received from the MDI to 4 logical signals PMD_UNITDATA.indication (rx_bit<0:3>) per 71.7.2	M	Yes [ ]
FS6	Receiver signal	71.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS7	Receive Signal order	71.6.3	PMD_UNITDATA.request(rx_bit<0:3>) = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>)	M	Yes [ ]
FS8	Behavior when Global_PMD_signal_detect is not implemented	71.6.4	SIGNAL_DETECT = OK continuously	!SD:M	Yes [ ] N/A [ ]
FS9	Global_PMD_signal_detect function	71.6.4	Reported via PMD_SIGNAL.indication (SIGNAL_DETECT)	SD:M	Yes [ ] N/A [ ]
FS10	Global_PMD_transmit_disable function	71.6.6	Disables all transmitters by forcing a constant level.	TD:M	Yes [ ] N/A [ ]
FS11	PMD_fault global effect	71.6.6	All transmitters disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS12	Global_PMD_transmit_disable affect on loopback	71.6.6	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS13	PMD_transmit_disable_n function implemented	71.6.7		M	Yes [ ]
FS14	PMD_transmit_disable_n action when enabled	71.6.7	Disables transmitter by forcing a constant level	M	Yes [ ]
FS15	PMD_transmit_disable_n affect on loopback	71.6.7	Loopback function not affected	M	Yes [ ]
FS16	Loopback Function	71.6.8	Loopback function provided	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
FS17	Loopback affect on transmitters	71.6.8	Loopback function does not disable transmitters	M	Yes [ ]
FS18	Low Power Idle function	71.6.12	Stops transmitting during LPI quite state	O	Yes [ ] No [ ] N/A [ ]

Revisions to IEEE Std 802.3-2008, Clause 72

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of 802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions

Editors' Notes: To be removed prior to final publication.

References:
None.

Definitions:
None.

Abbreviations:
None.

Revision History:

Draft 0.9, August 2008	**Second draft for IEEE P802.3az Task Force review.**
Draft 1.0, October 2008	

72. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KR

72.1 Overview

Change table 72-1 to add Clause 78.

Table 72–1—PHY (Physical Layer) clauses associated with the 10GBASE-KR PMD

Associated clause	10GBASE-KR
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
49—10GBASE-R PCS	Required
51—10-Gigabit Serial PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
74—FEC	Optional
78—Energy Efficient Ethernet	Optional

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

Insert the following text at the end of section 72.1

A 10GBASE-KR PHY may optionally enter a low power state to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The assertion of low power idle at the XGMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as low power idle at the XGMII. When low power idle is received an Energy Efficient 10GBASE-KR PHY sends sleep symbols then ceases transmission and deactivates transmit to conserve energy. When the receiver sees the sleep symbols it transitions to a quiet state, The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver clocks (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the XGMII, the PHY re-activates transmit and receive functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power state.

Insert the following section after 70.3

72.3a PCS requirements for Low Power Idle

If Energy Efficient Ethernet is supported, the PCS transmit function tells this PMD's transmit function when to enter in low power mode by asserting the tx_quiet primitive via the PMD_RTXQUIET.request. The PCS tell the PMD to exit low power idle mode by deasserting tx_quiet. While tx_quiet is asserted the PCS, PMA and PMD should deactivate all or part of its functional blocks to conserver energy. The PCS receive function uses a quiet timer and rx_quiet primitive to tell this PMD's receive function when enter support Energy Efficient Ethernet, the PCS shall provide the following service interface signals:

PMD_RXQUIET.request(rx_quiet)

PMD_TXQUIET.request(tx_quiet)

PMD_RXALERT.indication(rx_alert)

These messages signals are described in 49.2.13.2.6.

72.3b PMA requirements for Low Power Idle

If Energy Efficient Ethernet is supported by this PMA, the PMA shall provide the following primitives as described in 51.2.3.

While rx_quiet = true, the PMA should disable receive channel data paths and control logic to save additional power. Similarly while tx_quiet = true, the PMA should disable transmit channel data paths and control logic also. However, the PMA's Transmit Clock Generation Unit and Receive Clock Recovery Unit must remain operational to maintain clock synchronization and the Signal Indication Logic, PMA_SIGNAL.indication and PMD_SIGNAL.indication signals must remain operational to wake and refresh the PHY.

To synchronize the start of FEC with the end of training, the assertion of signal_detect is coordinated to arrive at the PMA_SIGNAL.indicate interface coincident with the 1st received bit after the last wake training frame on PMA_UNITDATA.indication.

Change tables 72-3 as follows;.

Table 72–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
LP Idle state indication	Status register 1	1.1.3	PMD_LPI_active
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
Receiver status	10GBASE-KR PMD status register	1.151.0	rx_trained
Frame lock	10GBASE-KR PMD status register	1.151.1	frame_lock
Start-up protocol status	10GBASE-KR PMD status register	1.151.2	training
Training failure	10GBASE-KR PMD status register	1.151.3	training_failure

72.6 PMD functional specifications

Change the text in the 1st paragraph of section 72.6.4 to read a follows:

72.6.4 PMD signal detect function during baseline operation

Insert the following section after 72.6.4

72.6.4a PMD signal detect function during low power operation

A local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. The PMD_SIGNAL.indication is used by the Low Power Idle function to indicate successful return to Active state from a Low Power state. The SIGNAL_DETECT shall be set to FAIL upon entering the RX_DEACT state and set to OK upon entering the RX_LAST_WAKE state as defined in 72-7

72.6.4b PMD Sense Signal function for low power operation

If Energy Efficient Ethernet is supported, the PMD needs an alternative to Signal_Detect to indicate when the electrical signal level at the input of the receiver is within certain threshold voltages. The PMD shall provide a Sense Signal function which sets sense_signal to a value of TRUE within T_{SA} after a step increase in the differential peak-to-peak voltage exceeding the Sense Signal Assertion threshold of V_{SA} as specified in Table 72-6.

The sense_signal parameter shall be set to FAIL within a maximum of T_{SD} after a step decrease in the differential peak-to-peak input voltage from a value greater than the Sense Signal Assertion Threshold to a differential signal level less than the Sense Signal Deassertion Threshold of V_{SD} as specified in Table 72-9

Change the text in 72.6.5 as indicated

72.6.5 PMD transmit disable function

The Global_PMD_transmit_disable function is optional. When this function is supported, it shall meet the requirements of this subclause.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 72–6.
b) If a PMD_fault (72.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 72.6.6, shall not be affected by Global_PMD_transmit_disable.
d) If Energy Efficient Ethernet is supported, the PMD transmit disable function shall turn off the transmitter such that the differential peak-to-peak output voltage is less than V_{TQ} within T_{TD} of tx_disable being asserted as defined in Table 70-6. The PMD transmit disable function shall turn on the transmitter such that the differential peak-to-peak output voltage is greater than V_{TW} within T_{TA} of tx_disable being deasserted as defined in Table 70-6.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.5.

72.6.10 PMD control function

72.6.10.1 Overview

Change the text in 1st paragraph of 72.6.10.1 as follows:

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner. If the PHY supports Energy Efficient Ethernet option, it will also bring it in and out of Low Power Idle.

72.6.10.2 Training frame structure

72.6.10.2.3 Coefficient update field

72.6.10.2.3.3 Coefficient (*k*) update

Change the text in 72.6.10.2.3.3 as follow:

Each coefficient, *k*, is assigned a 2-bit field describing a requested update. Three request encodings are defined: increment, decrement, and hold. The default state for a given tap is hold, which corresponds to no change in the coefficient. The increment or decrement encodings are transmitted to request that the corresponding coefficient be increased or decreased. The amount of change implemented by the transmitter in response to the coefficient update request shall meet the requirements of Table 72–7 and 72.7.1.10. An increment or decrement request shall continue to be transmitted until the update status for that tap (as defined in 72.6.10.2.4.5) indicates updated, maximum, or minimum. At that point, the outgoing requests for that tap shall be set to hold. When tx_quiet has the value REFRESH or WAKE states the coefficient update fields shall be set to hold.

72.6.10.2.4 Status report field

Change the Status report field Table 72-5 as indicated below:

.

Table 72–5—Status report field

Cell(s)	Name	Description
15	Receiver ready	1 = The local receiver has determined that training is complete and is prepared to receive data. 0 = The local receiver is requesting that training continue.
14	Refresh	1 = This frame is an EEE Refresh Frame 0 = This frame is not an EEE Refresh Frame
13	Wake	1 = This frame is an EEE Wake Frame 0 = This frame is not an EEE Wake Frame
12	Last Training Frame	1 = This frame is the last training frame for either LPI refresh or wake. 0= This is not the last training frame for EEE refresh or wake states
11:6	Reserved	Transmitted as 0, ignored on reception.
5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated
3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated
1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated

72.6.10.2.4.4 Receiver ready

Insert the following sections after 72.6.10.2.4.4

72.6.10.2.4.4a Refresh

The Refresh bit is asserted by the transmitter to indicate that the current frame is an EEE Refresh Training frame. When the transmitter exits the Refresh State, it will de-assert this bit. The refresh frames are used by the receiver to re-synchronize its clocks to the transmitted signal as describe in Clause 78. The assertion of the Refresh and Wake bits shall be mutually exclusive of each other. The transmitter will either send a Refresh training frame or Wake training frame. The format of this bit shall be as show in Table 72–5.

72.6.10.2.4.4b Wake

The Wake bit is asserted by the transmitter to indicate that the current frame is an EEE Wake Training frame. When the transmitter exit the Wake State, it will de-assert this bit. The wake frames are used to wake up the receiver to an active state, and prepare it to reliably receiver data. The assertion of the Wake and Refresh bits shall be mutually exclusive of each other. The transmitter will either send Refresh training frames or Wake training frames. The format of this bit shall be as show in Table 72–5.

72.6.10.2.4.4c Last Training Frame

The Last Training Frame bit is asserted by the transmitter to indicate that this frame is the last frame in the Refresh or Wake sequence. The last Wake Frame indicates to the receiver that Wake state has ended and the receiver must return to the active state. The last Refresh Frame indicates to the receiver that the Refresh state has ended and the receiver must return to the Quiet state. The Last Training Frame bit only has meaning during a Refresh or Wake training frame and may be otherwise ignored. The format of this bit shall be as show in Table 72–5.

72.6.10.2.4.5 Coefficient (*k*) status

Change the 2nd paragraph in 72.6.10.2.4.5 to read as follows:

These status encodings indicate the corresponding state of the coefficient update state diagram for coefficient *k*. When tx_quiet has the values of REFRESH or WAKE states the coefficient status shall be not updated.

Insert the following section after 72.6.10

72.6.11 PMD Low Power Idle function

72.6.11.1 Overview

The PMD Low Power Idle function responds to PCS requests to transitions in and out of Quiet, Refresh and Wake states. Implementation of the function is optional. Energy Efficient Ethernet capabilities and parameters will be advertised during the Backplane Auto-negotiation as described in 45.2.7.13. The transmitter on the local device will inform the remote link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the remote link partners transmitter and can change independent of the local transmitter states and transitions.

The sleep state is indicated by /LPI/ ordered sets. The Refresh and Wake states use training frames.

72.6.11.2 LPI transmit operation

The PMD's LPI transmitter timing shall follow the parameters given in table 72-5a shall be within +/- 10%.

[Editors note: the values in the following table were not part of the adopted baseline and need careful scrutiny.

Table 72–5a —Local Transmitter Timing Parameters*.*

72.6.11.3 State Variables

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Parameter	Description	Min	Max	Units
T_{REF}	Number of training frames sent to refresh receiver		10	training frames
T_{WL}	Number of training frames sent to wake receiver		20	training frames

72.6.11.3.1 Variables

ref_fr

An integer variable representing Refresh time (T_{REF}) as measured in training frames.

wak_fr

An integer variable representing local Wake time (T_{WL}) as measure in training frames.

frame_lock

A boolean variable that is set to TRUE when the receiver acquires training frame delineation and is set to FALSE otherwise.

rx_coeff

A variable that contains the state of the receiver's current coefficient values. These values are used to quickly restore the receiver to it previous state prior to going quiet.

rx_quiet

A Boolean set by the PCS Receive process to indicate the quiet state of PCS receive function as communicated through PMD_RXQUIET.request primitive. Also used to control the power saving function of various receiver blocks (PCS, PMA, and PMD).

Values: TRUE; The local receiver is in quiet state
FALSE; The local receiver is not in quiet state

rx_saved

A variable that is gets the a copy of the rx_coeff information when in the RX_ACTIVE state and restores the data to rx_coeff when it enters the RX_TRAIN state.

sending_data

A boolean variable set to TRUE when the PMD's training state diagram is in the SEND_DATA state and is set to FALSE otherwise.

tx_coeff

A variable that contains the state of the transmitters current coefficient values. These values are used to quickly restore the transmitter to it previous state prior to disabling it transmitter and entering the TX_QUIET state.

tx_disable

A variable that controls the enabling and disabling of the transmitter's differential output as described in 72.6.5

tx_fec

[Editors note, (to replace with meaningful text before publication), need a way to synchronize the start of the FEC transmit function with the end of the last wake training frame.]

tx_quiet

tx_quiet

A Boolean set by the Transmit process to indicate the quiet state of the PCS transmit function as communicated through PMD_TXQUIET.request primitive. Also used to control the power saving function of various transmit blocks within the PCS and PMA.

Values: TRUE; The local transmitter is in quiet state
FALSE; The local transmitter is not in quiet state

tx_saved

A variable that is gets a copy of the tx_coeff information when in the TX_ACTIVE state and restores the data to tx_coeff when it enters the TX_PREP state.

72.6.11.3.2 Counters

tx_fr_cnt

This counter counts the number of training frames sent during the TX_WAKE and REFRESH states.

72.6.11.3.3 Functions

TF_STATUS_RX(frame)

This function return indicates the type of training frame received during a refresh or wake sequence by examining bits in the status field. The following enumerated types are returned after the PMD has received the last training pattern bit from the frame:

return type	when status field bits <14:12> equal
LAST_WAKE:	0 1 1
LAST_REF:	1 0 1
WAKE:	0 1 0
REFRESH:	1 0 0
NULL:	any other pattern

TF_STATUS_TX(p)

This function transmits an entire training frame with status field bits set based on the parameter (p) type. The function must complete the transmission of the entire frame before transition to the next state. The status field bits are set as follows based on the parameter type:

parameter (p) type	status field bits <14:12> set to
LAST_WAKE:	0 1 1
LAST_REF:	1 0 1
WAKE:	0 1 0
REFRESH:	1 0 0

72.6.11.4 State Diagrams

72.6.11.4.1 LPI Transmit

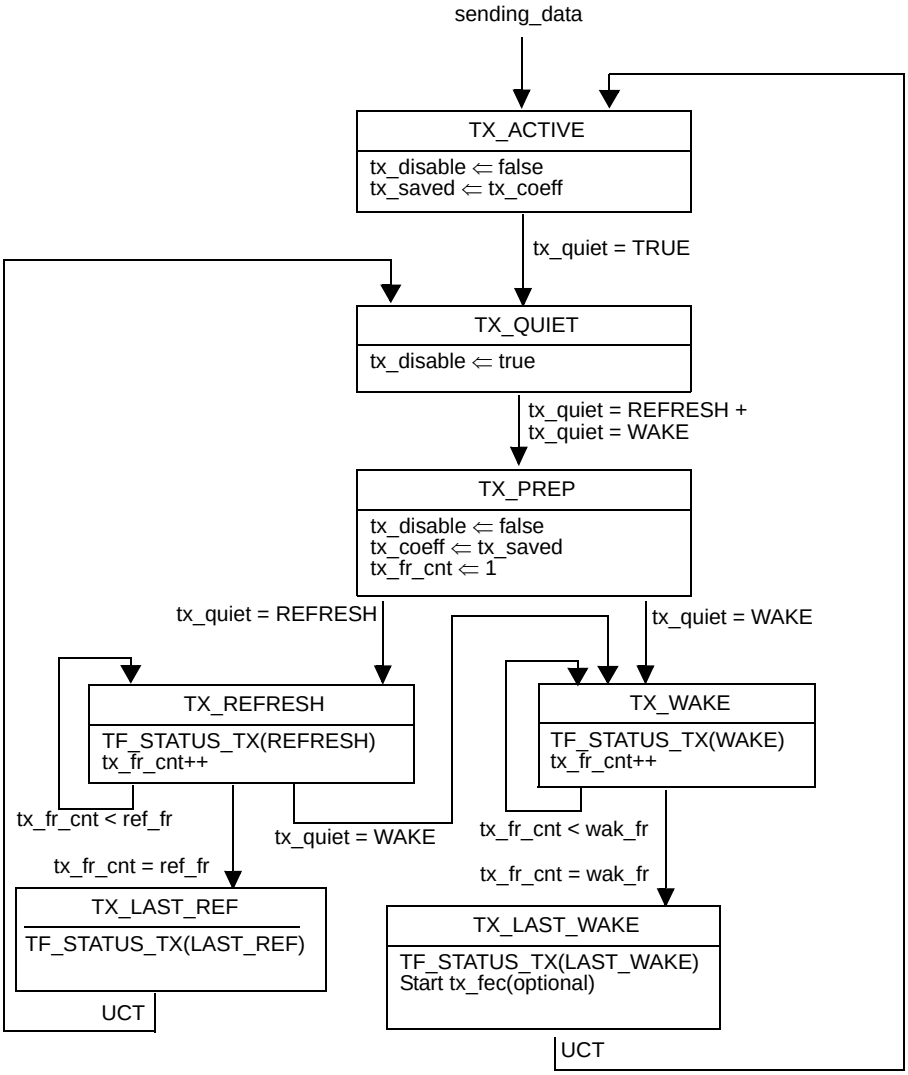

Figure 72–6—LPI Transmit state diagram

72.6.11.4.2 LPI Receive

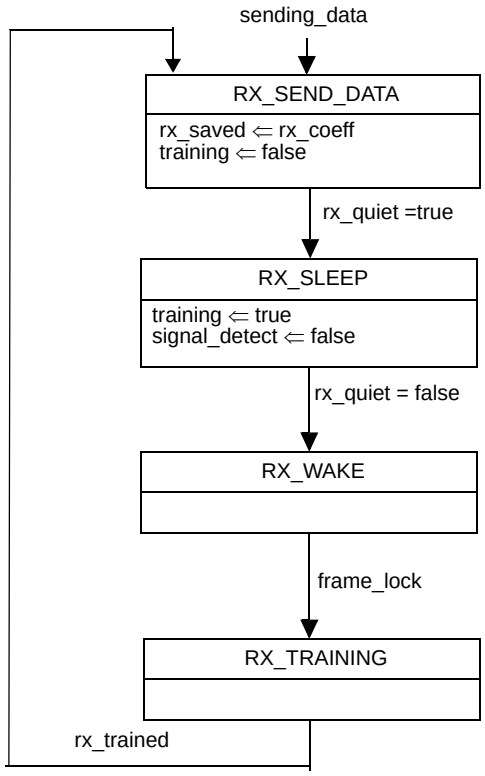

Figure 72–7—LPI Receive state diagram

72.7 10GBASE-KR electrical characteristics

72.7.1 Transmitter characteristics

Change Table 72-6 as indicated below:

Transmitter characteristics at TP1 are summarized in Table 72–6 and detailed in 72.7.1.1 through 72.7.1.11.

Table 72–6—Transmitter characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Signaling speed	72.7.1.3	10.3125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	72.7.1.4	1200	mV
Differential peak-to-peak output voltage (min.) with TX enabled (V_{TW})	70.6.5	Need Value	mV
Differential peak-to-peak output voltage (max.) with TX disabled (V_{TQ})	72.6.5	30	mV
Transmitter deactivation time from active (T_{TD}) for EEE	70.6.5	Need Value	ns
Transmitter activation time from EEE quiet mode (T_{TA})	70.6.5	Need Value	ns
Common-mode voltage limits	72.7.1.4	0–1.9	V
Differential output return loss (min.)	72.7.1.5	[See Equation (72–4) and Equation (72–5)]	dB
Common-mode output return loss (min.)	72.7.1.6	[See Equation (72–6) and Equation (72–7)]	dB
Transition time (20%–80%)	72.7.1.7	24–47	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	72.7.1.8	 0.15 0.15 0.035 0.28	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

72.7.2 Receiver characteristics

Change Table 72-9 as indicated below:

Receiver characteristics at TP4 are summarized in Table 72-9 and detailed in 72.7.2.1 through 72.7.2.5.

Table 72–9—Receiver characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Bit error ratio	72.7.2.1	10^{-12}	
Signaling speed	72.7.2.2	10.3125 ± 100 ppm	GBd
Receiver coupling	72.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	72.7.2.4	1200[a]	mV
Differential input peak-to-peak amplitude (min.) to assert Sense Signal(V_{SA})	70.6.4a	Need Value	mV
Differential input peak-to-peak amplitude (max.) to deassert Sense Signal (V_{SD})	70.6.4a	Need Value	mV
Signal Detect deactivation time from active to quiet (T_{SD}) for EEE	70.6.4a	Need Value	µs
Signal Detect activation time from EEE quiet mode (T_{SA})	70.6.4a	Need Value	µs
Differential input return loss (minimum)[b]	72.7.2.5	[See Equation (72–4) and Equation (72–5)]	dB

[a]The receiver shall tolerate amplitudes up to 1600 mV without permanent damage
[b]Relative to 100 Ω differential.

72.8 Protocol implementation conformance statement (PICS) proforma for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR[1]

Change the table in 72.7.3 as follows

72.8.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	72.1, 46	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	72.1, 47		O	Yes [ ] No [ ]
PCS	Support of 10GBASE-R PCS	72.1, 49		M	Yes [ ]
PMA	Support of 10 Gigabit serial PMA	72.1, 51		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	72.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
FEC	Forward Error Correction	72.1, 74	Device implements 10GBASE-R Forward Error Correction	O	Yes [ ]
DC	Delay Constraints	72.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO interface	72.5	Device implements MDIO	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	72.6.5		O	Yes [ ] No [ ]
LPI	Low Power Idle	72.6.11	Low Power Idle	O	Yes [ ] No [ ]

72.8.4 PICS proforma tables for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR.

Change the table in 72.7.4.2 as indicated

72.8.4.2 PMD functional specifications

Change the table in 72.7.4.4 by appending the following changes as indicated

72.8.4.4 PMD Control functions

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	72.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	72.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS3	Receive function	72.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	72.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS5	Signal detect	72.6.4	Report to PMD service interface	M	Yes [ ]
FS6	Global signal detect	72.6.4	Value described in 45.2.1.9.5	M	Yes [ ]
FS7	SIGNAL_DETECT value	72.6.4	Set to FAIL	M	Yes [ ]
FS8	SIGNAL_DETECT value	72.6.4	Set to OK when training is complete	M	Yes [ ]
FS9	SIGNAL_DETECT value	72.6.4	Set to OK when training disabled	M	Yes [ ]
FS10	Transmit disable requirements	72.6.5	Requirements of 72.6.5 and Table 72-6	TD:M	Yes [ ] N/A[ ]
FS11	Loopback support	72.6.6	Provided for 10GBASE-KR PMD by transmitter and receiver	M	Yes [ ]
FS12	Low Power Idle function	72.6.11	Enters LowPower_st when requested	LPI:M	Yes [ ] N/A

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Control Channel Encoding	72.6.10.2.2	Control channel transmitted using differential Manchester encoding (DME).	M	Yes [ ]
CF2	Differential Manchester Encoding rules	72.6.10.2.2	Transitions at cell boundary.	M	Yes [ ]
CF3	Differential Manchester Encoding rules	72.6.10.2.2	Presence of a mid-cell transition to signal logic 1	M	Yes [ ]
CF4	Differential Manchester Encoding rules	72.6.10.2.2	Absence of a mid-cell transition to signal logic 0	M	Yes [ ]
CF5	Coding violation	72.6.10.2.2	Ignore contents of control channel if coding violation found	M	Yes [ ]
CF6	Coefficient update field format	72.6.10.2.3	Format of the coefficient update field per Table 72–4	M	Yes [ ]
CF7	Cell 15 of the coefficient update field.	72.6.10.2.3	Transmitted first.		
CF8	Preset control	72.6.10.2.3.1	When received, pre-cursor and post-cursor coefficients set to zero	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CF9	Preset control	72.6.10.2.3.1	When received, main coefficient set to maximum value	M	Yes [ ]
CF10	Preset control initially sent	72.6.10.2.3.1	Only when all coefficient status fields indicate not_updated and continues until all coefficients indicate updated or maximum	M	Yes [ ]
CF11	Outgoing initialize control	72.6.10.2.3.1	Set to zero when all coefficients indicate updated or maximum following preset	M	Yes [ ]
CF12	Maximum status	72.6.10.2.3.1	Returned when the main coefficient is updated	M	Yes [ ]
CF13	Maximum status	72.6.10.2.3.1	Returned for pre-cursor and/or post-cursor coefficients when coefficient updated and zero is its maximum value	M	Yes [ ]
CF14	Updated status	72.6.10.2.3.1	Returned for pre-cursor and/or post-cursor coefficients when the coefficient is updated and it supports additional settings above the value zero	M	Yes [ ]
CF15	New Preset or Initialize requests	72.6.10.2.3.1	Not sent until the incoming status for all coefficients revert to not_updated	M	Yes [ ]
CF16	Preset	72.6.10.2.3.1	Not sent in combination with initialize or coefficient increment/decrement requests	M	Yes [ ]
CF17	Initalize control	72.6.10.2.3.2	When received, taps set to meet conditions of 72.6.10.4.2	M	Yes [ ]
CF18	Initalize control initially sent	72.6.10.2.3.2	Only when all coefficient status fields indicate not_updated and continues until all coefficients indicate updated	M	Yes [ ]
CF19	Updated status	72.6.10.2.3.2	Returned for each coefficient when the coefficient update is complete	M	Yes [ ]
CF20	Outgoing initalize field	72.6.10.2.3.2	Set to zero when all coefficients indicate update complete following initialize	M	Yes [ ]
CF21	New Preset or Initialize requests	72.6.10.2.3.2	Not sent until the incoming status for all coefficients revert to not_updated	M	Yes [ ]
CF22	Initialize	72.6.10.2.3.2	Not sent in combination with coefficient increment/decrement requests	M	Yes [ ]
CF23	Increment or decrement encodings transmitted	72.6.10.2.3.3	Transmitted until status indicates: updated, maximum, or minimum	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CF24	Outgoing requests	72.6.10.2.3.3	Set to hold once update status for tap indicates updated, maximum or minimum	M	Yes [ ]
CF25	Increment or decrement request	72.6.10.2.3.3	Not sent before status reverts to not_updated	M	Yes [ ]
CF26	Encoding of coefficient update	72.6.10.2.3.3	Per Table 72–4	M	Yes [ ]
CF27	Format of status report field	72.6.10.2.4	Per Table 72–5	M	
CF28	Cell 15 of the status report field	72.6.10.2.4	Transmitted first	M	
CF29	Receiver ready indication	72.6.10.2.4.4	Per Table 72–5	M	Yes [ ]
CF30	Coefficient status	72.6.10.2.4.5	Per Table 72–5	M	Yes [ ]
CF31	Training pattern length	72.6.10.2.6	512 octets	M	Yes [ ]
CF32	Training pattern generator	72.6.10.2.6	Per Figure 72–3	M	Yes [ ]
CF33	Training pattern seed	72.6.10.2.6	The pseudo-random generator shall have a random seed at the start of the training pattern.	M	Yes [ ]
CF34	Remote_rx_ready	72.6.10.3.1	TRUE after three or more consecutive training frames received with receiver ready indicated.	M	Yes [ ]
CF35	Wait Timer	72.6.10.3.2	100 to 300 training frames	M	Yes [ ]
CF36	Max Wait Timer	72.6.10.3.2	500 ms ± 1%	M	Yes [ ]
CF37	Slip function to find framesync	72.6.10.3.2	Evaluates all possible positions	M	Yes [ ]
CF38	Frame Lock state diagram	72.6.10.4.1	Meets requirements of Figure 72–4	M	Yes [ ]
CF39	Training state diagram	72.6.10.4.2	Meets requirements of Figure 72–5	M	Yes [ ]
CF40	Entry to INITIALIZE state	72.6.10.4.2	Transmitter equalizer configured per 72.6.10.4.2	M	Yes [ ]
CF41	Initial value of c(0) at the start of training	72.6.10.4.2	Meets the requirements of 72.6.10.4.2	M	Yes [ ]
CF42	Coefficient Update state diagram	72.6.10.4.3	Meets requirements of Figure 72–6	M	Yes [ ]
CF43	LPI Transmit state diagram	72.6.11.x	Meets requirement of Figure72-x	LPI:M	Yes [ ]
CF44	LPI Receive state diagram	72.6.11.x	Meets requirement of Figure 72-x	LPI:M	Yes [ ] N/A [ ]
CF45	Refresh	72.6.11.x		LPI:M	Yes [ ] N/A [ ]
CF46	Wake	72.6.11.x		LPI:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CF47	Last Training Frame	72.6.11.x		LPI:M	Yes [ ] N/A [ ]
CF48					

78. Energy Efficient Ethernet (EEE)

Editor's Notes: To be removed prior to publication: *Clause 78 is a new Clause*

78.1 Overview

78.1.1 Scope

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) Sublayer with a family of Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

EEE operational mode supports the IEEE 802.3 MAC operation at 100 Mb/s, 1000 Mb/s, and 10 Gb/s. For 100 Mb/s operation, 100BASE-TX Physical layer device is supported. For 1000 Mb/s, two Physical Layer signaling schemes are supported. For operation over twisted pair cabling, the 1000BASE-T is supported. For serial communication over electrical backplane, the 1000BASE-KX is supported. For 10 Gb/s, three Physical Layer signaling systems are supported. For operation over twisted pair cabling system 10GBASE-T signaling system is included. For operation over four logical lanes on electrical backplane, 10GBASE-KX4 signaling scheme is supported. For serial operation over electrical backplane, 10GBASE-KR signaling scheme is supported.

In addition to the above, EEE defines 10 Mb/s PHY (10BASE-Te) with reduced transmit amplitude requirements. The 10BASE-Te is fully interoperable with 10BASE-T PHYs over 100 m of class D (Category 5) or better cabling as specified in ISO/IEC 11801:1995. These requirements can also met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995. Definition of 10BASE-Te allows power consumption saving.

EEE also specifies means for the capabilities negotiation to enable link partners to determine whether EEE is supported and selection best set of parameters common to both devices.

78.1.2 Objectives

The following are the objectives of the Energy Efficient Ethernet:

a) Define a mechanism to reduce power consumption during periods of low link utilization for the following PHYs:
   1) 100BASE-TX (Full duplex)
   2) 1000BASE-T (Full duplex)
   3) 10GBASE-T
   4) 1000BASE-KX
   5) 10GBASE-KR
   6) 10GBASE-KX4
b) Define a protocol to coordinate transitions to or from a lower level of power consumption
c) The link status must not change as a result of the transition.
d) Frames must not be dropped or corrupted during the transition to and from the lower level of power consumption.
e) The transition time to and from the lower level of power consumption must be transparent to upper layer protocols and applications.
f) Define a 10 Mb/s PHY (10BASE-Te) with a reduced transmit amplitude requirement such that it is fully interoperable with 10BASE-T PHYs over 100 m of class D (Category 5) or better cabling to enable reduced power implementation.

g) Any twisted-pair and/or backplane PHY for EEE must support auto negotiation with non-EEE PHYs.

78.1.3 Conceptual description of the Low Power Idle mode

Low Power Idle mode is optional mode that allows power saving by switching off part of the communication device functionality when no data needs to be transmitted or/and received. The decision on whether system should enter Low Power Idle mode or exit Low Power Idle mode is done on the MAC level and communicated to PHY level in order to allow power saving. Figure 78–1 shows the decision flow and agents involved.

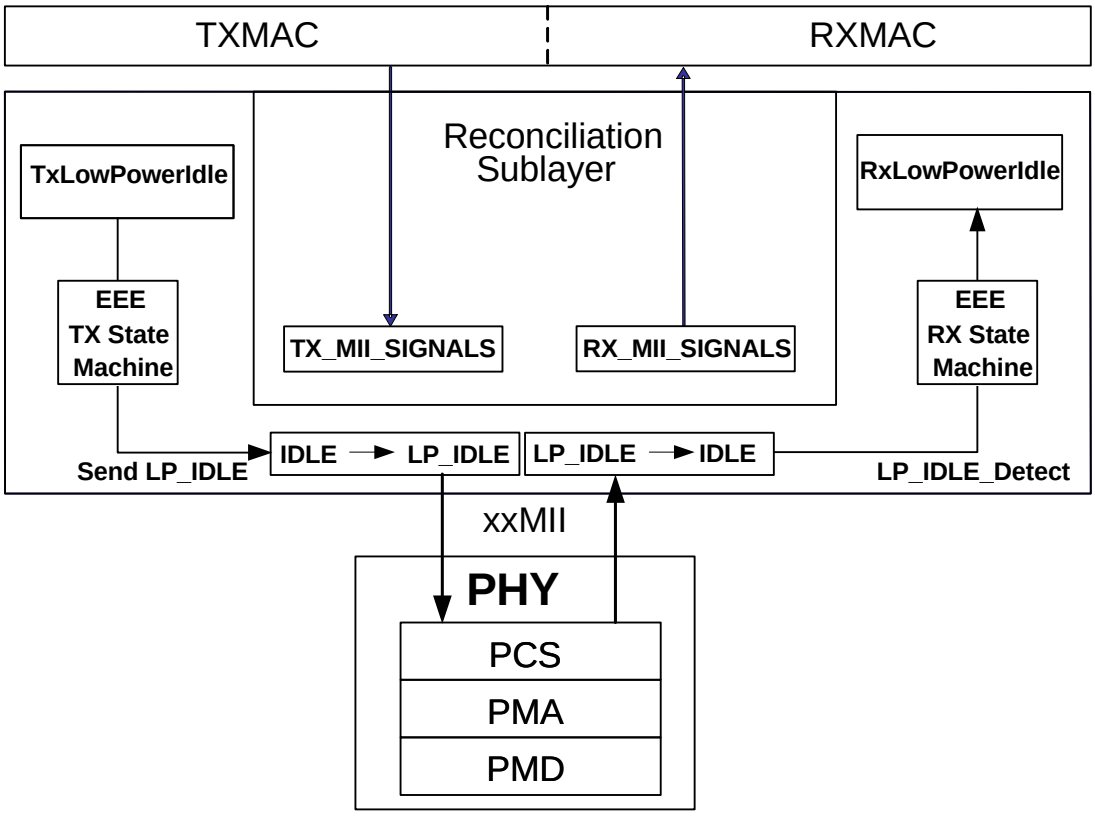

Figure 78–1—EEE Low Power Idle Generation and Detection Functionality

In the transmit direction entrance to Low Power Idle mode of operation is triggered by the reception of LP_IDLE codewords on the MAC interface. The specific interface depends on communication standard being used, therefore this interface is shown as xxMII in the diagram.

Following reception of LP_IDLE codeword, PHY transmits a special LP_Sleep signal to communicate to the link partner that the local system is entering Low Power Idle mode.

In 100BASE-T and 10GBASE-T EEE modes, the transmit function of the local PHY enters a quiet mode after the LP_Sleep signal transmission.

In 1000BASE-T Low Power Idle mode, the transmit function of the local PHY enters a quiet mode only after the local PHY transmits LP_Sleep and receives LP_Sleep from the remote PHY. If the remote PHY chooses not to signal Low Power Idle, then neither PHY can go quiet however Low Power Idle requests are passed from one end of the link to the other regardless and system energy savings can be achieved even if the PHY link does not go quiet.

The transmit function of the local PHY is enabled periodically to transmit LP_Refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity.

This quiet-refresh cycle continues until local MAC signals to the PHY that Low Power Idle mode should end by sending IDLE codewords. The transmit function in the PHY communicates this to the link partner by sending special LP_Wake signal for a pre-defined period of time. Then the PHY enters Active_st and resumes normal operation mode.

In the receive direction, entering Low Power Idle mode is triggered by the reception of LP_Sleep signal from the link partner. This signals that the link partner is about to enter Low Power Idle mode. After sending the LP_Sleep signal, the link partner ceases transmission and enters LP_Quiet_st state. While Link partner is in LP_Quiet_st state, the local receiver can disable some of the functionality to reduce power consumption.

The link partner periodically transmits LP_Refresh signals that are used by the local PHY to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner initiates transition back to normal mode by transmitting LP_Wake signal for a pre-determined period of time. This allows the local receiver to prepare for the full data-rate mode. After a a system specified recovery time the link supports nominal operational data rate.

Figure 78–2 illustrates general principles of the EEE-compliant transmitter operation.

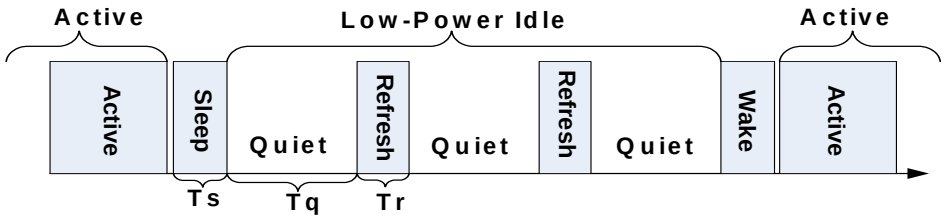

Figure 78–2—Active state - Low Power Idle mode - Active state cycle

No data frames are lost or corrupted during the transition to or from the Low Power Idle mode.

78.1.4 Relation of EEE to other standards

EEE defines Low Power Idle mode of operation for the following seven 802.3 PHYs. Table 78–1 lists the clauses associated with each PHY.

Table 78–1—Relation between EEE and IEEE protocols

Nomenclature	Clause
10BASE-Te	14
100BASE-TX	22
1000BASE-T	40
1000BASE-KX	70
10GBASE-T	55
10GBASE-KX4	71
10GBASE-KR	72

78.2 States and timing parameters

78.2.1 Low Power Idle mode states description:

Active_st: Normal operating state where data or idle transmitted

LowPower_st: Operating state used during period of no data transmission and reception, enabling system power reduction. Used by PHYs that support symmetric Low Power Idle mode

LowPowerTx_st: Operating state used during period no data transmission, enabling system power reduction. Used by PHYs that support asymmetric Low Power Idle mode

LowPowerRx_st: Operating state used during period of no data reception, enabling system power reduction. Used by PHYs that support asymmetric Low Power Idle mode

Following are Low Power Idle mode sub-states description:

LP_Sleep_st: During this state, Sleep signal is sent to communicate to the link partner that local system is about to enter LowPower_st

LP_Quiet_st: All local transmitters are off

LP_Refresh_st: During this state, Refresh signal is transmitted periodically to allow link partner to refresh timing and other essential parameters

LP_Wake_st: Signal that communicates to link partner that local system is about to return to Active state

78.2.2 Low Power Idle mode Signals description:

LP_IDLE: This codeword is used by MAC to force Transmit path of the local PHY to enter Low Power Mode

LP_Sleep: Signal transmitted to link partner to inform it that Transmit path of the local PHY is entering Low Power Idle mode

LP_Refresh: Signal transmitted to link partner to allow update of the timing and channel parameters

LP_Alert: Signal transmitted to link partner to inform that local PHY received IDLE signal on the XGMII interface and is about to exit LP_IDLE mode

LP_Wake: Signal transmitted to link partner to inform it that Transmit path of the local PHY is exiting Low Power Idle mode

78.2.3 Low Power Idle mode timing parameters description:

T_s: Duration of time PHY transmits Sleep signal before entering LP_Quiet_st

T_q: Duration PHY remains quiet before sending refresh signal

T_r: Duration of the refresh signal

T_{w_phy}: Period of time between reception IDLE signal appearing on the xxMII interface and when first codewords are permitted on the xxMII interface

T_{w_sys}: Period of time between transition from LP_IDLE to IDLE signaling on the xxMII interface and when the first data codewords are permitted on the xxMII interface. For proper system operation, following relationship must hold: $T_{w\_sys} > T_{w\_phy}$

78.3 Capabilities Negotiation

EEE support is advertised during Auto-Negotiation stage. Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed at power up, on command from management, upon detection of a PHY error, or due to user interaction.

For BASE-T type devices, Auto-Negotiation is performed using a pulse code sequence (FLP Bursts) that is compatible with the 10BASE-T link integrity test sequence - as described in clause 28.

For BASE-X type devices, the basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within /C/ ordered_sets as described in clause 37. /C/ ordered_sets are directly analogous to FLP Bursts.

For Backplane Ethernet PHYs (1000-KX, 10GBASE-KX4, and 10GBASE-KR devices), Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC balanced signal. DME does not add packet or upper layer overhead to the network devices. When the MDI supports multiple lanes (e.g., for operation of 10GBASE-KX4), then lane 0 of the MDI shall be used for Auto-Negotiation and for connection of any single-lane PHYs (e.g., 1000-KX or 10GBASE-KR). See Clause 73 for additional details on Auto-Negotiation for Backplane Ethernet.

During the link establishment process, both link partners indicate their EEE capabilities. If EEE is supported by both link partners for the negotiated PHY type then the EEE function may be used independently in either direction.

The Auto-Negotiation process uses next page messages or extended next page messages as defined in 28C.12, 28C.13 and 73A.4.

T_{w_sys} parameter can be adjusted based on systems needs and up-to-date traffic profile without breaking communication link using LLDP (Link Layer Data Protocol), see 78.4 for details.

78.4 Link Level Capabilities Discovery

In addition to the capabilities negotiation described in 78.3, capabilities and settings are also advertised using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Annex G of IEEE Std 802.1AB protocol (LLDP). The additional advertisement allows devices to choose and change system wake-up times and more or less aggressive energy saving modes.

Editor's Notes: To be removed prior to publication
This sub-clause will be changed based on L-2 ad-hoc committee report. This committee will use framework in diab_01_0109.pdf as adopted by the task force to come up with a way to exchange initial values for system wake time and to negotiate the system wake time T_w dynamically

78.4.1 LLDP and EEE TLV support

Implementations of Energy Efficient Ethernet may use LLDP. Implementation that use LLDP shall comply with all mandatory parts of IEEE Std 802.1AB and shall support the EEE Type, Length, Value (TLV) defined in 78.1.2. The default values for the parameters are given in the same section, operation with values other than the defaults is optional. The EEE TLV is sent periodically or following an update to the corresponding MIB objects defined in 78.4.2 (according to the rules defined in 802.1AB).

Editor's Notes: To be removed prior to publication
Cross reference to Clause 30 will be added when Clause 30 is completed.

78.4.2 EEE TLV

The EEE TLV is used to change the system wake-up and refresh mode. Figure 78–3 shows the format of this TLV.

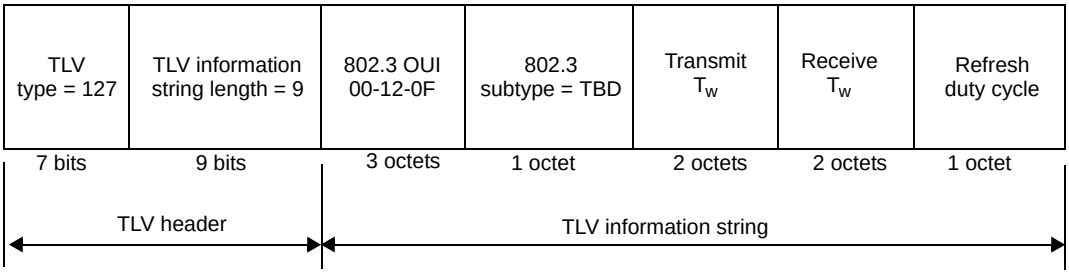

Figure 78–3—EEE TLV format

78.4.2.1 Transmit T_w definition

Transmit Tw_sys (2 octets wide) is the time (expressed in microseconds) that the system is capable of waiting before it starts transmitting data following the Low Power Idle. This limitation is a function of the transmit system design and may be limited, for example, by the transmit path buffering. The default value for Transmit T_{w_sys} is the T_{w_sys} defined for the PHY that is in use for the link.

78.4.2.2 Receive T_w definition

Receive Tw_sys (2 octets wide) is the time (expressed in microseconds) that the system is requesting the link partner to wait before it starts transmitting data following the Low Power Idle. This extra wait time is intended to allow a receive system to use power saving mechanisms that require longer wake-up time than the PHY-layer definitions. The default value for Receive T_{w_sys} is the T_{w_sys} defined for the PHY that is in use for the link.

78.4.2.3 T_w resolution and operation

In each direction, the Resolved Transmit T_{w_sys} is the lesser of the local Transmit T_{w_sys} and the received (from the link partner) Receive T_{w_sys}. The local device shall wait for the time indicated by the Resolved Transmit T_{w_sys} after de-asserting Low Power Idle (at the xxMII) before sending data frames. Similarly the local device can understand that the link partner will be bound by its Resolved Transmit T_{w_sys} and so the

78.4.2.4 Changes to EEE parameters

Local system shall send LLDP messages with updated parameters at least 4 times before relying on the link partner to have received and acted upon the change. LLDP frames that contain request for Low Power Idle parameters can only be send during *Active_st*. System shall not initiate transition into *LowPower_st* within 10 seconds period following sending or receiving LLDP frames that change any of *LowPower_st* parameters. In case systems receives request to transition into *LowPower_st* within period of less then 10 seconds after LLDP frames with modified Low Power Idle parameters being received, it should assume that old set of Low Power Idle parameters is valid.

78.5 Communication link access latency

In full duplex mode, predictable operation of the MAC ControlPAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

Editor's Notes: To be removed prior to publication
This sub-clause will be changed based on shinkage ad-hoc committee report. This committee will use framework in law_01_0109.pdf as adopted by the task force during January interim meeting. In this presentation David identified cases where there could be shrinkage in the system wake time. He introduced new variables, including one for a default system wake time as well as parameters to specify shrinkage

In addition, EEE operational mode adds latency to be considered by network designer. When at Low Power Idle mode, PHY device is not available immediately for data transmission request. System has to wake it up by sending normal idle code on the MAC interface. Following IDLE code reception on the MAC interface, PHY starts waking up process. The maximal PHY recovery time T_{w_phy} is defined for each PHY. Table 78–2 summarizes maximal T_{w_phy} for supported protocols along with three additional key parameters (T_s, T_q, and T_r). This should assist systems designer while considering Low Power Idle modes effect on the overall operation..

Editor's Notes: To be removed prior to publication
Values in Table 78-2 are based on the draft 1.1 and should be treated as temporary. Some of the parameters were taken from the presentation given by Task force members. Editor encourages detailed review and comments on this table values

Table 78–2—Summary of the key EEE parameters for supported PHYss

Protocol	T_{w_phy} μsec		T_s μsec		T_q μsec		T_r μsec	
	min	**max**	**min**	**max**	**min**	**max**	**min**	**max**
10GBASE-KR	11.0	16.9	4.5	5.5	1,530	1,870	15.2	18.5
10GBASE-KX4	8.0	18.0	18.0	22.0	2,250	2,750	18.0	22.0
1000BASE-KX	10.0	20.0	18.0	22.0	2,250	2,750	18.0	22.0
10GBASE-T	4.16	7.36	2.88	3.2	39.7	39.68	1.28	1.28
1000BASE-T	16.0	16.0	182.0	202.0	20,000	24,000	198.0	218.2
100BASE-TX	30.0	24,000	100	100	20,000	20,000	100	100

Annex 28C

(normative)

Next page Message Code field definitions

Editors' Notes: *To be removed prior to publication.*
Changes to autonegotiation for EEE operation.

Change Table 28C-1 for the new message code definition:

Table 28C–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability to follow.using unformatted next page
11	0	0	0	0	0	0	0	1	0	1	1	EEE Technology Message Code. EEE capability using extended next page
~~10~~12.....	0	0	0	0	0	0	0	1	0	~~0~~ 1	1	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

Insert 28C.12 & 28C.13 for message code definition:

28C.12 Message code 10—EEE technology message code

Multiple clauses use next page message code 10 to indicate that EEE technology messages will follow the transmission of this page [the initial, Message (formatted) next page] with at least two unformatted next pages that contain information defined in 45.2.7.13a.

28C.13 Message code 11—EEE technology message code (extended)

PHYs that negotiate extended next page support (reference) use next page message code 11 to indicate that this extended next page contains information defined in 45.2.7.13a. Multiple clauses use next page message code 11 to indicate that EEE technology message is contained in this unformatted extended next page.

Annex 73A

(normative)

Next page Message Code field definitions

Editors' Notes: *To be removed prior to publication.*
Changes to autonegotiation for EEE operation.

Change Table 73A-1 for the new message code definition:

Table 73A–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability to follow.using unformatted next page

Insert 73A.4 for message code definition:

73A.4 Message code 10—EEE technology message code

Multiple clauses use next page message code 10 to indicate that EEE technology messages will follow the transmission of this page [the initial, Message (formatted) next page] with at least two unformatted next pages that contain information defined in 45.2.7.13a.