MOS 6502 / MOS 6510

Deep Dive Instruction Set

LDA Load Accumulator with Memory

M -> A N Z C I D V

assembler	opc	bytes	cycls
LDA #oper LDA oper	A9 A5	2 2 2	2 3
LDA oper,X	B5	2	4
LDA oper	AD	3	4
LDA oper,X	BD	3	4*
LDA oper,Y	B9	3	4*
LDA (oper,X)	A1	2	6
LDA (oper),Y	В1	2	5*
	LDA #oper LDA oper,X LDA oper LDA oper,X LDA oper,X LDA oper,X LDA oper,X LDA (oper,X)	LDA #oper A9 LDA oper,X B5 LDA oper,X BD LDA oper,X BD LDA oper,X BD LDA oper,Y B9 LDA (oper,X) A1	LDA #oper A9 2 LDA oper, X B5 2 LDA oper, X B5 2 LDA oper, X BD 3 LDA oper, X BD 3 LDA oper, Y B9 3 LDA (oper, X) A1 2

- * add 1 to cycles if page boundary is crossed
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Legend to Flags: + modified - not modified

1 set

0 cleared

ADC Add Memory to Accumulator with Carry

$$A + M + C \rightarrow A$$
, C $N Z C I D V + + + - - +$

assembler	орс	bytes 	cycls
ADC #oper	69	2	2
ADC oper	65	2	3
ADC oper,X	75	2	4
ADC oper	6D	3	4
ADC oper,X	7D	3	4*
ADC oper,Y	79	3	4*
ADC (oper,X)	61	2	6
ADC (oper),Y	71	2	5*
	ADC #oper ADC oper,X ADC oper ADC oper,X ADC oper,X ADC oper,X ADC oper,X	ADC #oper 69 ADC oper,X 75 ADC oper,X 75 ADC oper,X 7D ADC oper,Y 79 ADC (oper,X) 61	ADC #oper 69 2 ADC oper 65 2 ADC oper,X 75 2 ADC oper 6D 3 ADC oper,X 7D 3 ADC oper,Y 79 3 ADC (oper,X) 61 2

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1 set

0 cleared

AND AND Memory with Accumulator

A AND $M \rightarrow A$

NZCIDV

addressing	assembler	opc	bytes	cycls
immediate	AND #oper	 29	 2	 2
zeropage	AND oper	25	2	3
zeropage,X	AND oper,X	35	2	4
absolute	AND oper	2D	3	4
absolute,X	AND oper,X	3D	3	4*
absolute,Y	AND oper,Y	39	3	4*
(indirect,X)	AND (oper,X)	21	2	6
(indirect),Y	AND (oper),Y	31	2	5*

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- not modified

1 set

0 cleared

M6 memory bit 6

$$A \cdot B = C$$
 $1 \cdot 1 = 1$
 $1 \cdot 0 = 0$
 $0 \cdot 1 = 0$
 $0 \cdot 0 = 0$

ASL Shift Left One Bit (Memory or Accumulator)

C <- ←76543210→ <- 0

NZCIDV

10010010

```
addressing
              assembler
                            opc bytes cycls
accumulator
              ASL A
                             0A
                             06 2
16 2
0E 3
              ASL oper
zeropage
              ASL oper,X
zeropage, X
                                          6
absolute
              ASL oper
                             1E
absolute,X
              ASL oper,X
```

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Legend to Flags: + modified

- not modified

1 set

0 cleared

BCC Branch on Carry Clear

branch on C = 0

4 Z C I D V

- - - - - -

addressing	assembler	opc	bytes	cycls
relative	BCC oper	90	2	2**

BCS Branch on Carry Set

branch on C = 1

NZCIDV

- - - - - -

addressing	assembler	opc	bytes	cycls
relative	BCS oper	 B0	 2	 2 * *

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Legend to Flags: + modified

- not modified

1 set

0 cleared

M6 memory bit 6

BEQ Branch on Result Zero

branch on Z = 1

NZCIDV

- - - - -

addressing	assembler	opc	bytes	cycls
relative	BEQ oper			244
reracive	pew ober	ГÜ	_	\Box \wedge \wedge

BMI Branch on Result Minus

branch on N = 1

N Z C I D V

- - - - - -

addressing	assembler	opc	bytes	cycls
relative	 BMI oper	 30		 2 * *

- * add 1 to cycles if page boundary is crossed
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Legend to Flags: + modified

- not modified

1 set

0 cleared

M6 memory bit 6

BIT Test Bits in Memory with Accumulator

bits 7 and 6 of operand are transferred to bit 7 and 6 of SR (N,V); the zeroflag is set to the result of operand AND accumulator.

A AND M, M7 \rightarrow N, M6 \rightarrow V N Z C I D V M7 + - - - M6

addressing	assembler	opc	bytes 	cycls
zeropage	BIT oper	24	2	3
absolute	BIT oper	2C	3	4

11010010

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Legend to Flags: + modified - not modified

1 set

0 cleared M6 memory bit 6

BNE Branch on Result not Zero

branch on
$$Z = 0$$

addressing	assembler	opc	bytes	cycls
relative	BNE oper	D0	2	2**

BPL Branch on Result Plus

branch on N = 0

NZCIDV

addressing		opc	_	_
relative	BPL oper	10	 2	

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Legend to Flags: + modified

- not modified

1 set

0 cleared

M6 memory bit 6

BVC Branch on Overflow Clear

branch on
$$V = 0$$

addressing	assembler	opc	bytes	cycls
relative	BVC oper	5 0	 2	2**

BVS Branch on Overflow Set

branch on V = 1

3		•	bytes	_
relative	BVS oper		 2	

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- not modified

1 set

0 cleared

M6 memory bit 6

BRK Force Break

addressing	assembler	opc	bytes	cycls
implied	BRK	 00	1	 7

CLC Clear Carry Flag

addressing	assembler	opc	bytes	cycls
implied	CLC	 18	1	2

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Legend to Flags: + modified

- not modified

1 set

0 cleared

M6 memory bit 6

CLD Clear Decimal Mode

addressing	assembler	opc	bytes	cycls
implied	CLD	D8	1	 2

CLI Clear Interrupt Disable Bit

$$0 \rightarrow I$$

addressing	assembler	opc	bytes	cycls
implied	CLI	 58	1	2

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Legend to Flags: + modified

- not modified

1 set

0 cleared

M6 memory bit 6

CLV Clear Overflow Flag

addressing	assembler	opc	bytes	cycls
implied	CLV	B8	1	2

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Legend to Flags: + modified - not modified

1 set

0 cleared