

VERA Registers

Vera Version 0.9 (Emulator R.37)

| Register | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|---------|--------------------|---|---------------|----------------|----------------|-------------------------------|----------------|-------------|----------------|
| 0 | \$9F20 | Address Lo | VRAM Memory address bits 0-7 | | | | | | | |
| 1 | \$9F21 | Address Mid | VRAM Memory address bits 8 - 15 | | | | | | | |
| 2 | \$9F22 | Address Hi | Address Increment | | | | Dec | - | | Bit 16 |
| 3 | \$9F23 | Data 0 | Data Register 0 | | | | | | | |
| 4 | \$9F24 | Data 1 | Data Register 1 | | | | | | | |
| 5 | \$9F25 | Control | Reset | - | | | | | DC | Address Select |
| 6 | \$9F26 | IEN | IRQ bit 8 | - | | | AFLOW | SPRCOL | LINE | VSYNC |
| 7 | \$9F27 | ISR | Sprite Collissions | | | | AFLOW | SPRCOL | LINE | VSYNC |
| 8 | \$9F28 | IRQ Line | IRQ bits 0-7 | | | | | | | |
| 9-0 | \$9F29 | Video | Current Field | Sprite Enable | Layer 1 Enable | Layer 0 Enable | - | Chroma Disable | Output Mode | |
| 10-0 | \$9F2A | Horizontal Scale | Active Display Horizontal Scale | | | | | | | |
| 11-0 | \$9F2B | Vertical Scale | Active Display Vertical Scale | | | | | | | |
| 12-0 | \$9F2C | Border Color | Border Color | | | | | | | |
| 9-1 | \$9F29 | Horizontal Start | Active Display Horizontal Start Bits 2 - 9 | | | | | | | |
| 10-1 | \$9F2A | Horizontal Stop | Active Display Horizontal Stop Bits 2 - 9 | | | | | | | |
| 11-1 | \$9F2B | Vertical Start | Active Display Vertical Start Bits 1 - 8 | | | | | | | |
| 12-1 | \$9F2C | vertical Stop | Active Display Vertical Stop Bits 1 - 8 | | | | | | | |
| 13 | \$9F2D | Layer 0 - Config | Map Height | | Map Width | | T256C | Bitmap Mode | Color Depth | |
| 14 | \$9F2E | Layer 0 - Mapbase | Map Base Address Bits 9 - 16 | | | | | | | |
| 15 | \$9F2F | Layer 0 - Tilebase | Tile Base Address Bits 11 - 16 | | | | | | Height | Width |
| 16 | \$9F30 | Layer 0 - H Scroll | Horizontal Scroll Bits 0 - 7 | | | | | | | |
| 17 | \$9F31 | Layer 0 H Scroll | - | | | | Horizontal Scroll Bits 8 - 11 | | | |
| 18 | \$9F32 | Layer 0 - V Scroll | Vertical Scroll Bits 0 - 7 | | | | | | | |
| 19 | \$9F33 | Layer 0 - V Scroll | - | | | | Vertical Scroll Bits 8 - 11 | | | |
| 20 | \$9F34 | Layer 1 - Config | Map Height | | Map Width | | T256C | Bitmap Mode | Color Depth | |
| 21 | \$9F35 | Layer 1 - Mapbase | Map Base Address Bits 9 - 16 | | | | | | | |
| 22 | \$9F36 | Layer 1 - Tilebase | Tile Base Address Bits 11 - 16 | | | | | | Height | Width |
| 23 | \$9F37 | Layer 1 - H Scroll | Horizontal Scroll Bits 0 - 7 | | | | | | | |
| 24 | \$9F38 | Layer 1 H Scroll | - | | | | Horizontal Scroll Bits 8 - 11 | | | |
| 25 | \$9F39 | Layer 1 - V Scroll | Vertical Scroll Bits 0 - 7 | | | | | | | |
| 26 | \$9F3A | Layer 1 - V Scroll | - | | | | Vertical Scroll Bits 8 - 11 | | | |
| 27 | \$9F3B | Audio Control | FIFO Full/Reset | - | 16 Bit | Stereo | PCM Volume | | | |
| 28 | \$9F3C | Audio Rate | PCM Sample Rate | | | | | | | |
| 29 | \$9F3D | Audio Data | Audio FIFO Write Only Data Register | | | | | | | |
| 30 | \$9F3E | SPI Data | SPI (Serial Peripheral Interface) Data Register | | | | | | | |
| 31 | \$9F3F | SPI Control | Busy | - | | | | | Slow Clock | Select |