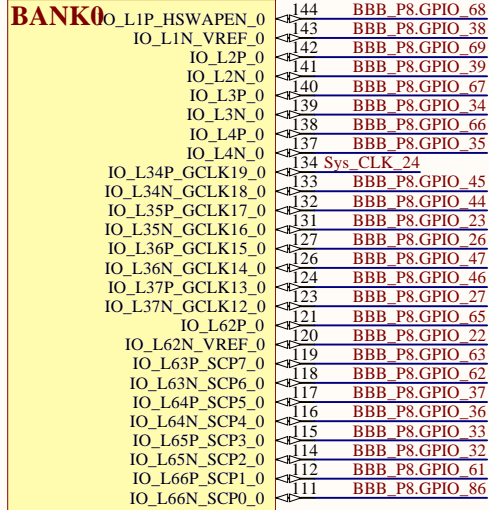


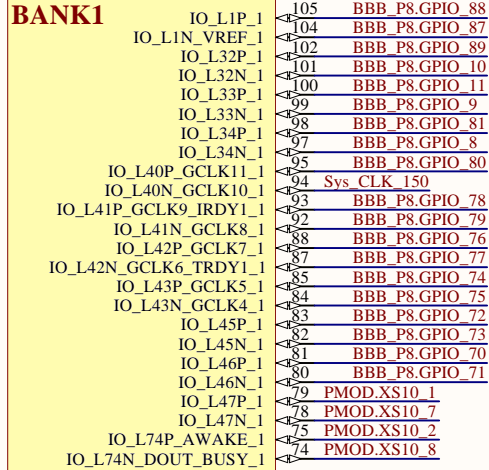
	1	2	3	4			
A	<div>FPGA [2]-FPGA.SchDoc</div> <div></div>	<div>CPLD [3]-CPLD.SchDoc</div> <div></div>	<div>USB [4]-USB.SchDoc</div> <div></div>	<div>BeagleBlack Connectors [5]-BeagleBlack Connectors.SchDoc</div> <div></div>	<div>PMOD Connectors [6]-PMOD Connectors.SchDoc</div> <div></div>	<div>FPGA-Power [7]-FPGA-Power.SchDoc</div> <div></div>	A
	<div>SPI_Memory [8]-SPI_Memory.SchDoc</div> <div></div>						
B	<div>[9]-Power Supply [9]-Power Supply.SchDoc</div> <div></div>						B
	<div>[10]-CPLD-Power [10]-CPLD-Power.SchDoc</div> <div></div>						
C							C
D						<div><div><div>Project: Beagle-DGX-XC6</div><div><div>Title: [1]-Beagle-DGX-XC6 Top.SchDoc</div><div>Variant: [No Variations]</div></div><div><div>Engineer: Sergej Bakhmach</div><div>Revision: 1</div></div><div><div>Size: A4</div><div>Sheet: 1 of 10</div></div><div>Company: Those Boards</div></div><div>tb</div></div> <td>D</td>	D
	1	2	3	4			

U7A



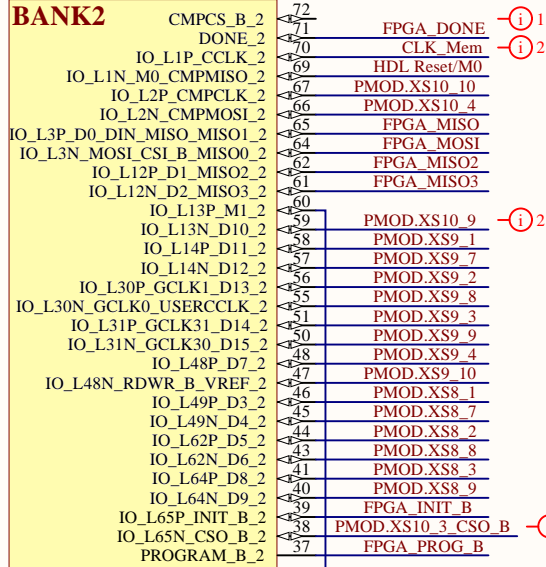
XC6SLX9-2TQG144C

U7B

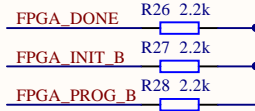
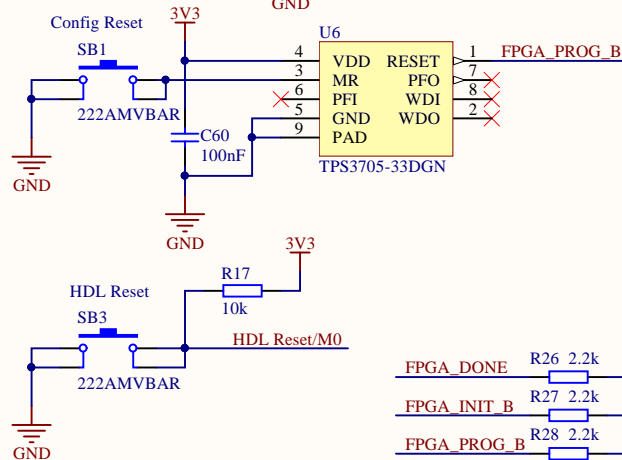


XC6SLX9-2TQG144C

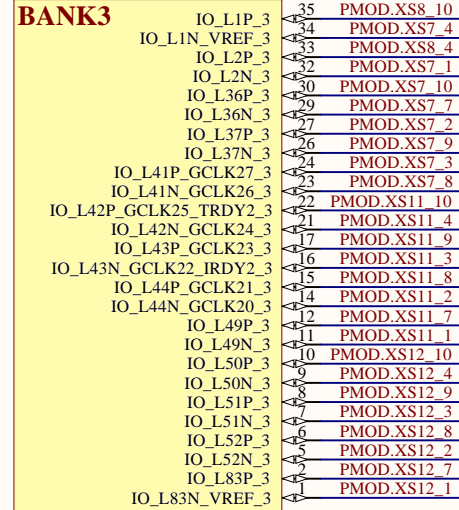
U7C



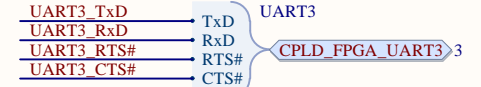
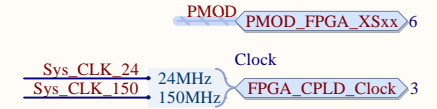
XC6SLX9-2TQG144C



U7D



XC6SLX9-2TQG144C



1 - Отпаять ножку 72 U7. Сигнал с разъема XS10 пин 3 (лист [6]-PMOD Connectors), завести на 38 ножку U7
2. - Поменять местами сигналы.

Project: **Beagle-DGX-XC6**Title: **[2]-FPGA.SchDoc**Variant:
[No Variations]Engineer: **Sergej Bakhmach**Revision: **1**Size: **A4**Sheet: **2 of 10**Company: **Those Boards**

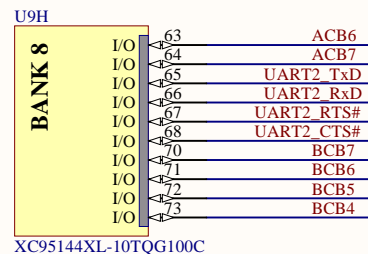
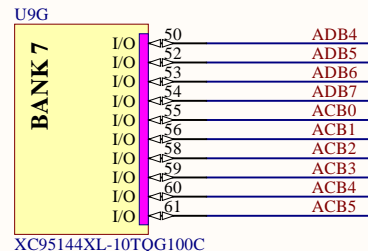
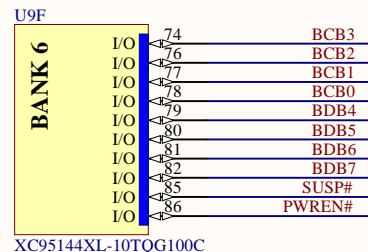
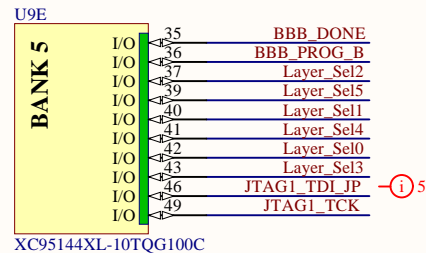
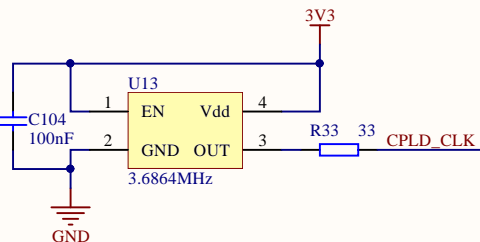
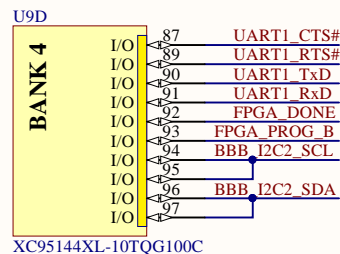
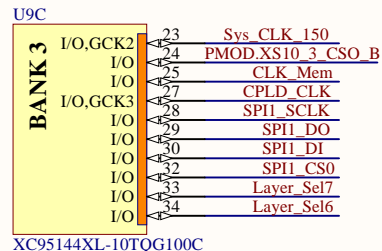
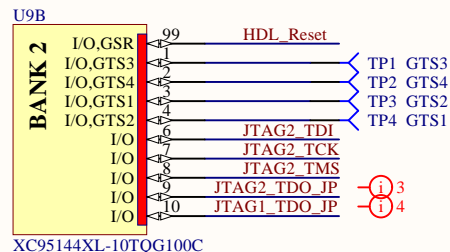
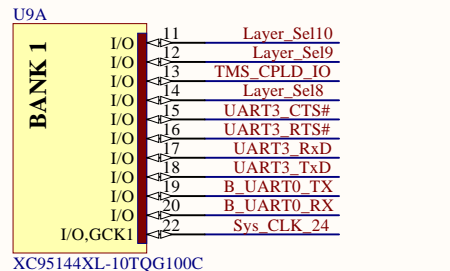
tb

A

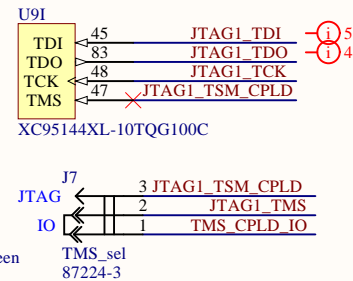
B

C

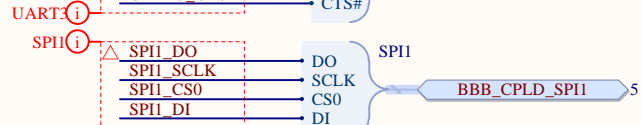
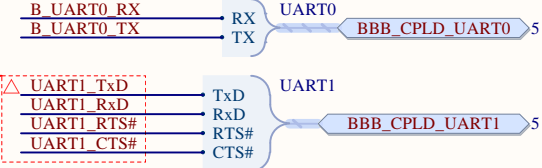
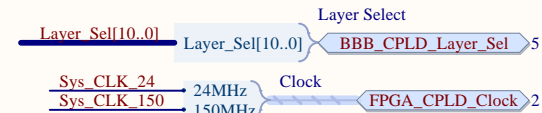
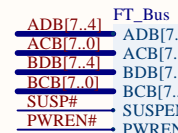
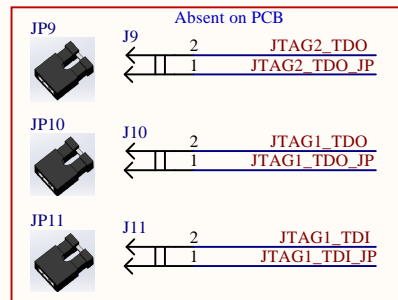
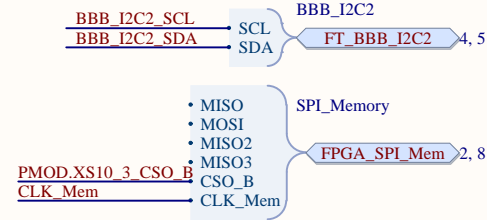
D



3 - Отпаять ножку 9 U9. Между ножкой 9 U9 и ножкой 106 U7 (лист [7]-FPGA-Power), поставить джампер.
4 - Отпаять ножку 10 U9. Между ножкой 10 U9 и ножкой 83 U9 поставить джампер.
5 - Отпаять ножку 46 U9. Между ножкой 46 U9 и ножкой 45 U9 поставить джампер.



Jumper Green



Project: **Beagle-DGX-XC6**

Title: **[3]-CPLD.SchDoc**

Variant:
[No Variations]

Engineer: **Sergej Bakhmach**

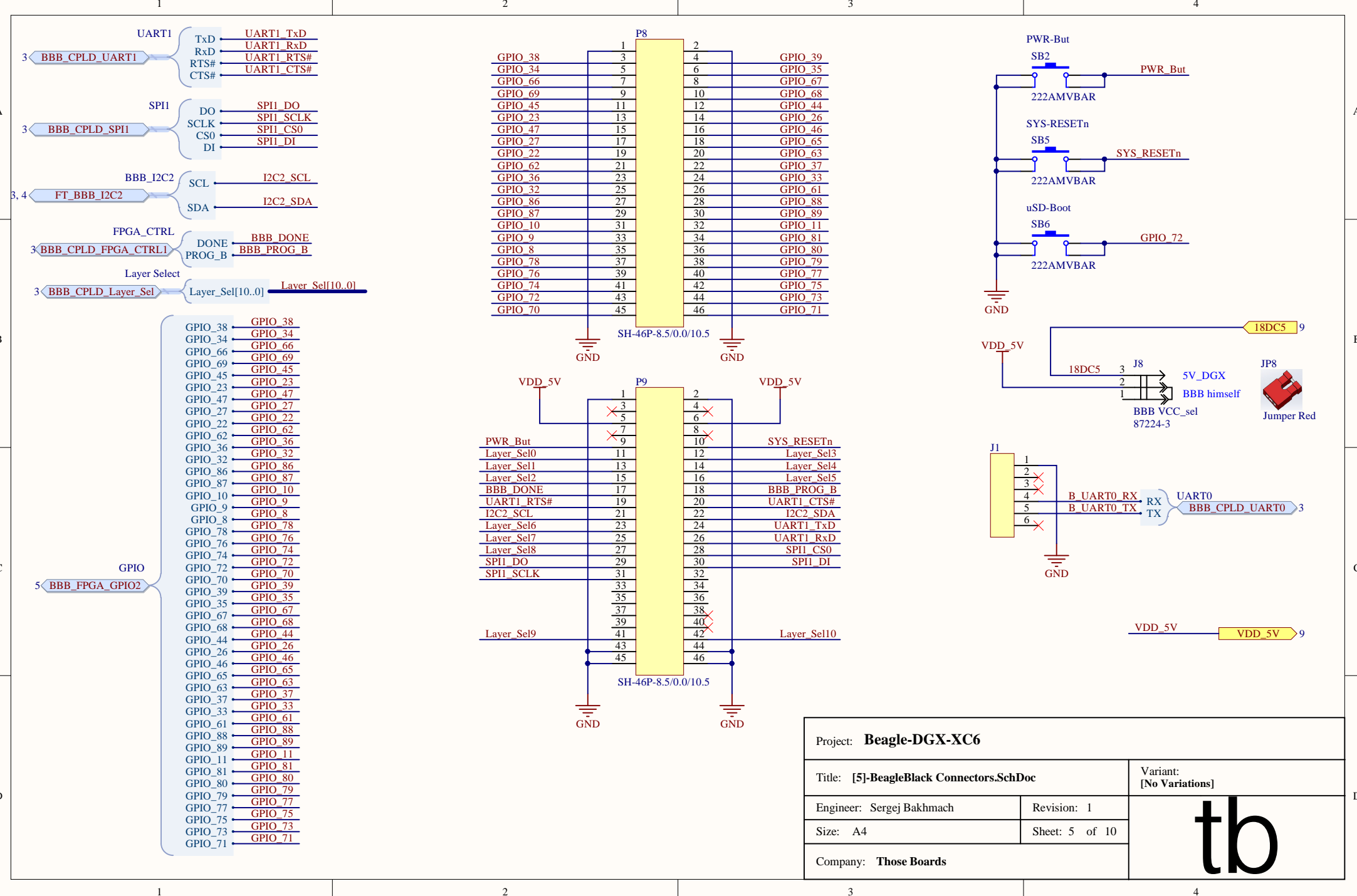
Revision: 1

Size: A4

Sheet: 3 of 10

Company: **Those Boards**

tb



A

B

C

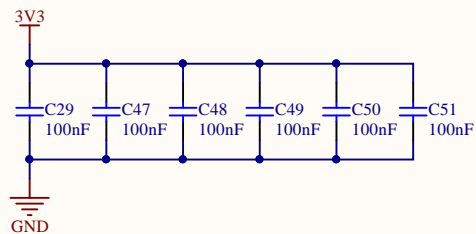
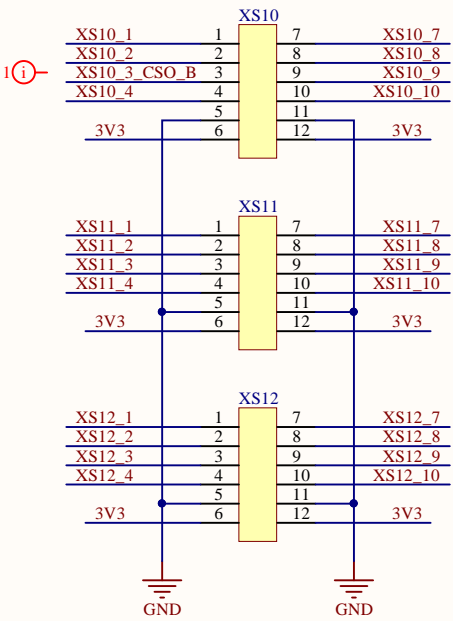
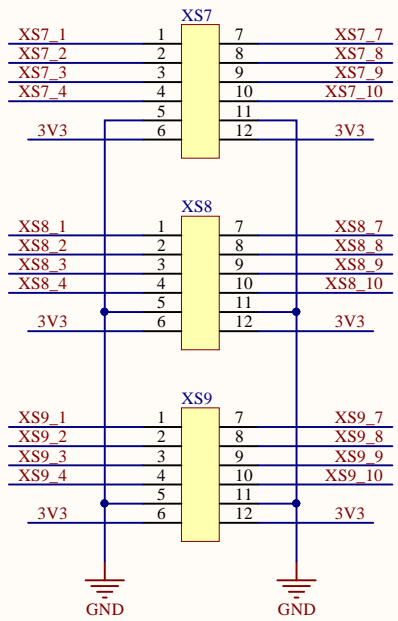
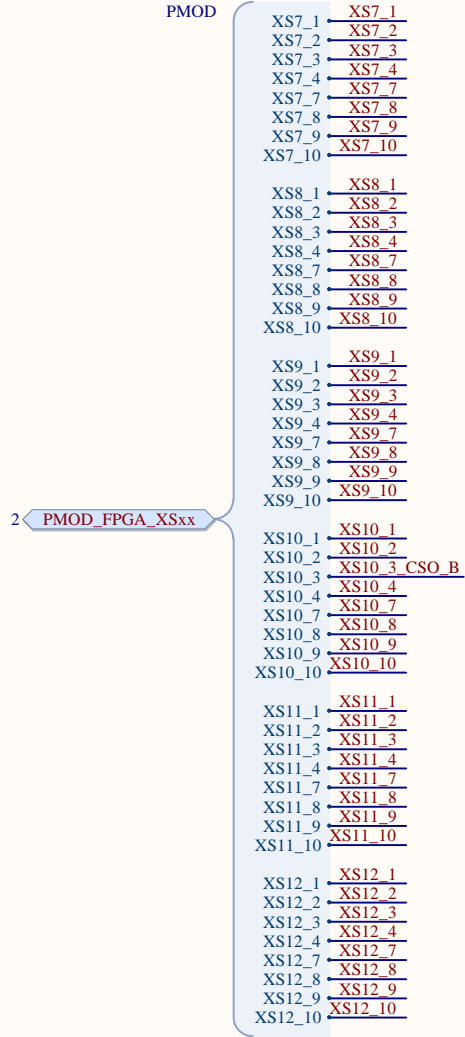
D

A


B

C

D



1 - Пояснения на листе [2]-FPGA

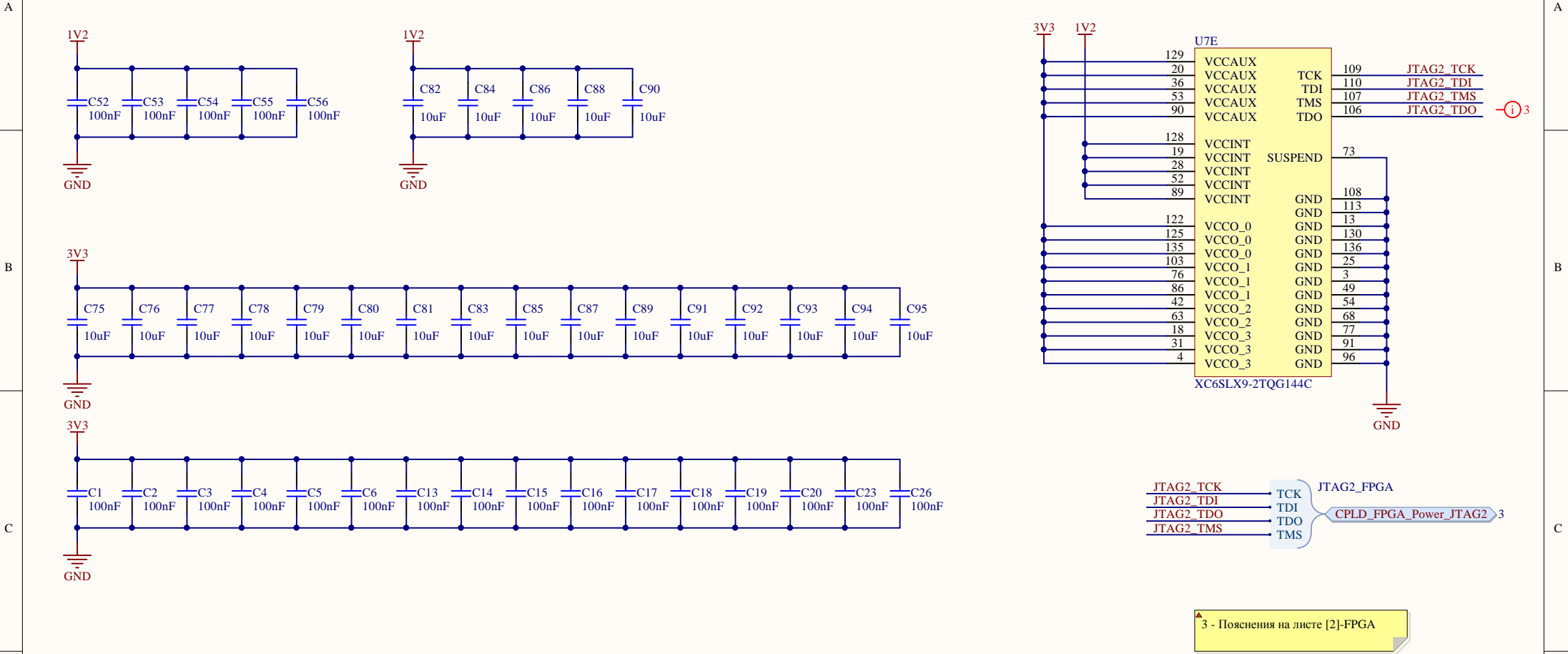
Project: Beagle-DGX-XC6		
Title: [6]-PMOD Connectors.SchDoc		Variant: [No Variations]
Engineer: Sergej Bakhmach	Revision: 1	
Size: A4	Sheet: 6 of 10	
Company: Those Boards		

A

B

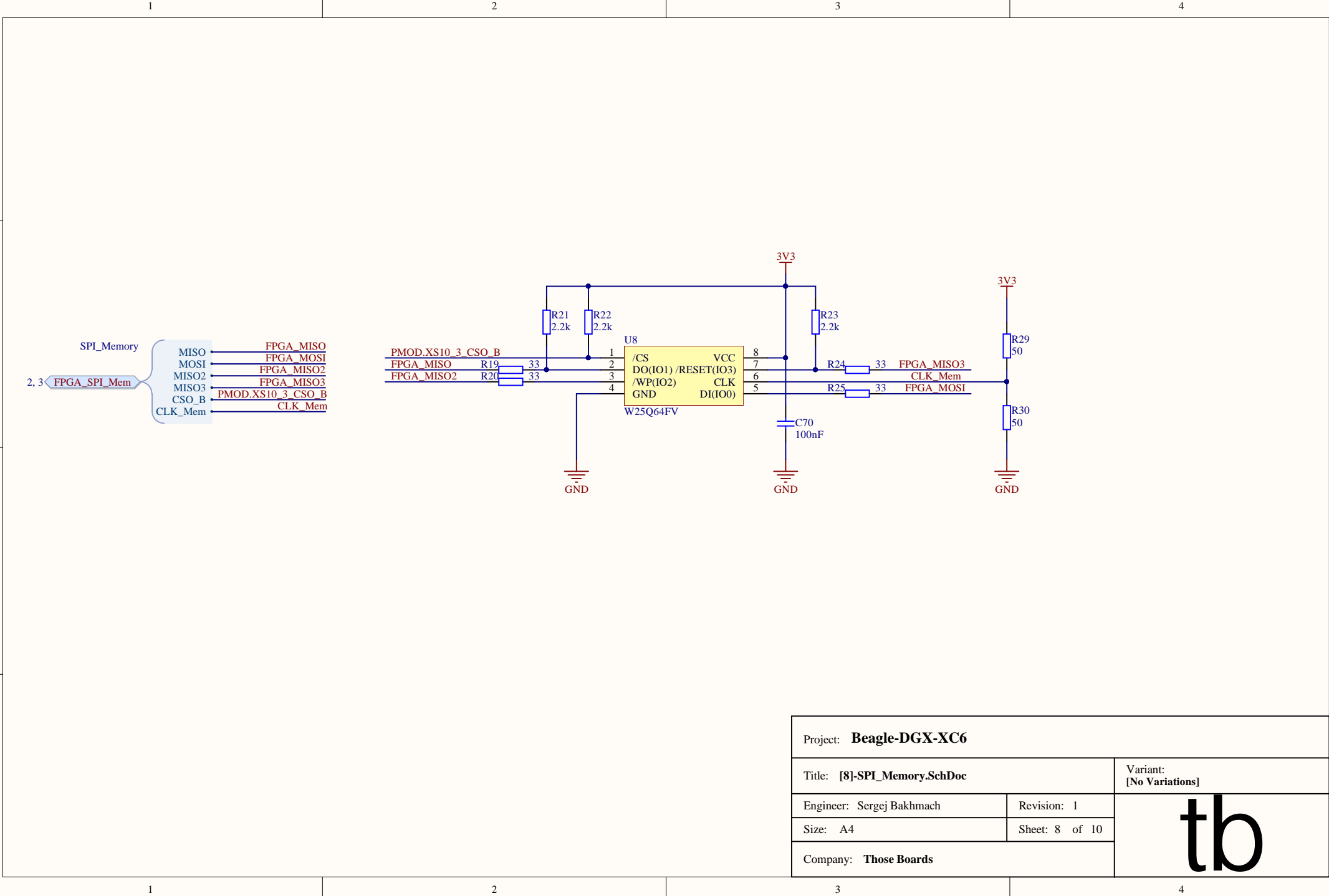
C

D

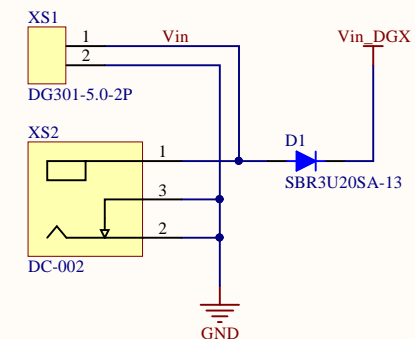


Project: Beagle-DGX-XC6		
Title: [7]-FPGA-Power.SchDoc		Variant: [No Variations]
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 7 of 10	
Company: Those Boards		

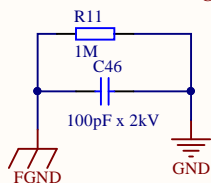
tb



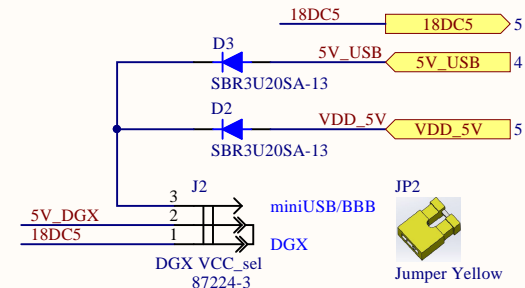
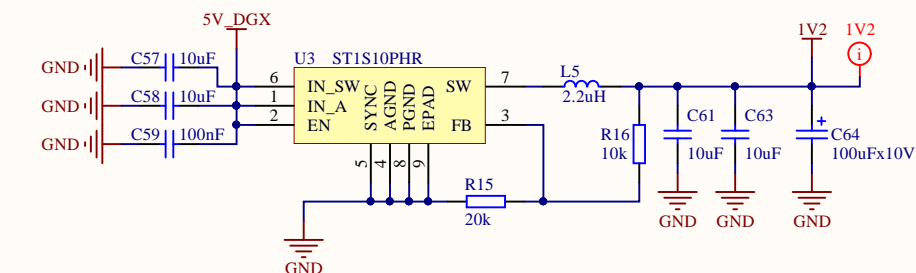
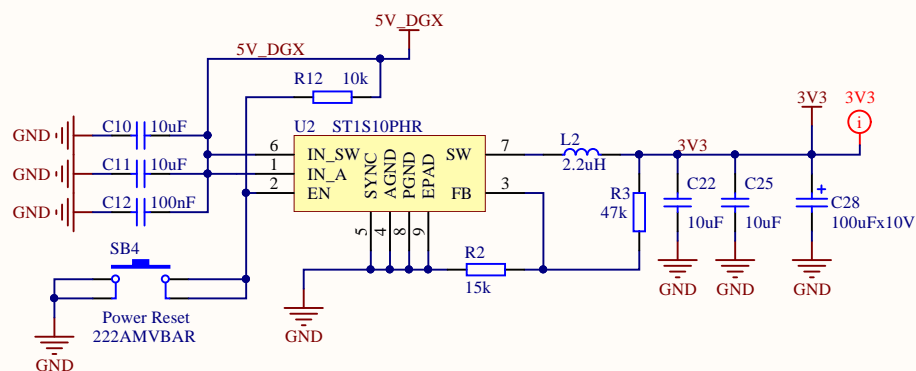
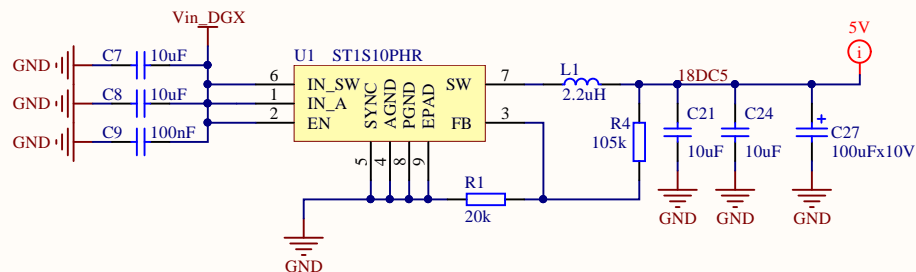
A



B



C



A

B

C

D

Project: **Beagle-DGX-XC6**Title: **[9]-Power Supply.SchDoc**Variant:
[No Variations]

Engineer: Sergej Bakhmach

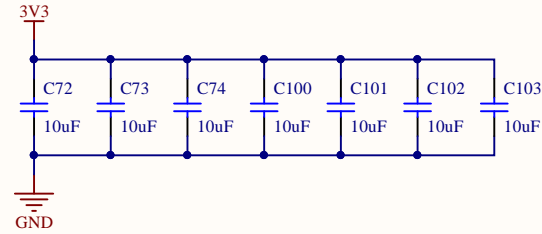
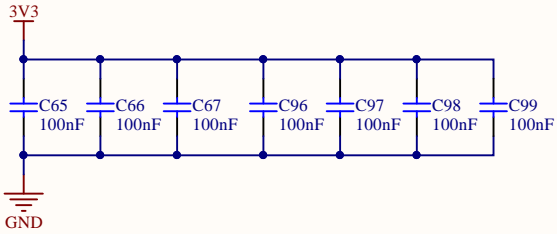
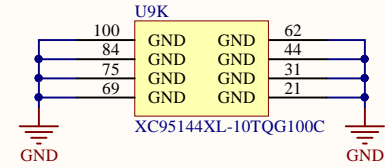
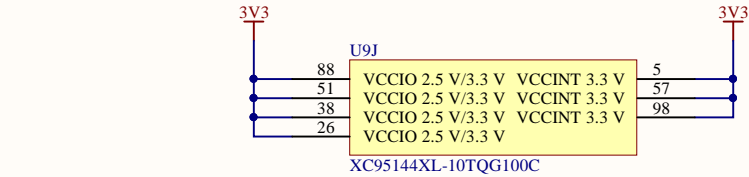
Revision: 1

Size: A4

Sheet: 9 of 10

Company: **Those Boards**

tb



Project: Beagle-DGX-XC6		
Title: [10]-CPLD-Power.SchDoc		Variant: [No Variations]
Engineer: Sergej Bakhmach	<div>tb</div>	
Revision: 1		
Size: A4		
Sheet: 10 of 10		
Company: Those Boards		