## 6502 INSTRUCTIONS

Modes  IP Implied Ac Accumulator LL Label IN Immediate Heliz Z Zero Page Siz
Thodes In Implied Accumulator Label In Immediate Holz In Impediate In Imp
REAL NUBDIZC IN IMMEDIZC
In Immediate
In Immediate
z Zero Page, \$12, \$12, \$12, \$12, \$12, \$12, \$12, \$12
Zy Zero Page, X siz. X zy Zero Page, Y siz. Y sh Absolute Sizo4, Y sh Ab
## NUBDIZC NUBDIZC ComPare X register Im2 23 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5+  ## Nubdizc Nubdizc Nubdizc ComPare X register Im2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5+  ## Nubdizc ComPare X register Im2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5+  ## Nubdizc ComPare X register Im2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5+  ## Nubdizc ComPare X register Im2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5+  ## Nubdizc ComPare X register Im2 Z3 Zx4 Ab4 Ax4+ Ax4+ Ay4+ Ix6 Iy5+  ## Nubdizc ComPare X register Im2 Z3 Zx4 Ab4 Ax4+ Ax4+ Ax4+ Ax4+ Ax4+ Ax4+ Ax4+ Ax4
Ax Absolute, X aligney, My Absolute, Y aligney, My Absolute, My Absolute
Aph shoulte, $V$ sized, $V$ in Indirect, $V$ (sized) in Indirect, $V$
In Indirect (\$12.4) Ix Indirect, (\$12.4) Ix Indirec
Is Indirect, X (\$12,X)
ADC NUBDIZC ComPare X register Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Im² Z³ Ab⁴ COMPare Y register Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay⁴+ Ix6 Iy5+ ComPare Y register Im² Z³ Zx⁴ Ab Ax⁴+ Ax⁴+ Ay²+ Ix6 Iy² Ip² Ix² NUBDIZC Ix² X NUBDIZC
ADD with Carry  Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴ Ix6 Iy5+  NUBDIZC Branch on PLus BPI NUBDIZC Branch on PLus Branch on MInus Im² Z³ Ab⁴  NUBDIZC Im² Z³ Ab⁴  NUBDIZC Im² Z³ Ab⁴  NUBDIZC Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Av Pegister Im² Z³ Zx⁴ Ab⁴ Ax⁴+ InlCrement Memory Z⁵ Zx6 Ab6 Ax²  Inl² Z³ Zx⁴ Ab⁴ Ax⁴+ Av Pegister Im² Z³ Zx⁴ Ab⁴ Ax⁴+ InlCrement Memory Z⁵ Zx6 Ab6 Ax²  Inl² Z³ Zx⁴ Ab⁴ Ax⁴+ InlCrement Memory Z⁵ Zx6 Ab6 Ax²  Inl² Z³ Zx⁴ Ab⁴ Ax⁴+ InlCrement Memory Z⁵ Zx6 Ab6 Ax²  Inl² Z³ Zx⁴ Ab⁴ Ax⁴+ InlCrement Memory Z⁵ Zx6 Ab6 Ax²  Inl² Z³ Zx⁴ Ab⁴ Ax⁴+ InlCrement Memory Z⁵ Zx6 Ab6 Ax²  Inl² NUBDIZC Inl² Nubbizc Inl² Nubbi
ADD with Carry  Im² 2³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴+ Ix⁶ Iy⁵+  AND NUBDIZC  Sitwise AND with accumulator  Im² 2³ Ab⁴ Ax⁴+ Ay⁴+ Ix⁶ Iy⁵+  AND NUBDIZC  Sitwise AND with accumulator  Im² 2³ Ab⁴  NUBDIZC  Im² 2³ Ab⁴  NUBDIZC  Arithmetic Shift Left A² Z⁵ Zx⁶ Ab⁶ Ax²  BIL NUBDIZC  Transfer A to Y  NUBDIZC  Arithmetic Shift Left A² Z⁵ Zx⁶ Ab⁶ Ax²  BIL NUBDIZC  Transfer Y to A  Ip²  NUBDIZC  Sitwise Exclusive OR Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴+ Ix⁶ Iy⁵+  NUBDIZC  Transfer Y to A  Ip²  NUBDIZC  Sitwise Exclusive OR Im² Z³ Zx⁴ Ab⁴ Ax⁴+ Ay⁴+ Ix⁶ Iy⁵+  NUBDIZC  Transfer A to X Ip²  NUBDIZC  Transfer Y to A  Ip²  NUBDIZC  Transfer A to X Ip²  NUBDIZC  Transfer A to X Ip²  NUBDIZC  Transfer Stack to X Ip²  NUBDIZC  Transfer X to A Ip²  NUBDIZC  Transfer Stack to X Ip²  NUBDIZC  Transfer Stack to X Ip²  NUBDIZC  Transfer X to A Ip²  NUBDIZC  DEX NUBDIZC  DEX NUBDIZC  DEX NUBDIZC  Push Accumulator
Size   Numbric   Size   Numbric   Size   Numbric   Size   Numbric   Size   Numbric   Size   Numbric   Size   Siz
AND NUBDIZC  Bitwise AND with accumulator  Im² Z³ Zx⁴ Ab⁴ Ax⁴ + Ay⁴ Ix⁶ Iy⁵ +  AY Z⁵ Zx⁶ Ab⁶ Ax 7  BI NUBDIZC Arithmetic Shift Left A² Z⁵ Zx⁶ Ab⁶ Ax 7  BI NUBDIZC Arithmetic Shift Left A² Z⁵ Zx⁶ Ab⁶ Ax 7  BI NUBDIZC ECC NUBDIZC Transfer Y to A  Ip² NUBDIZC Bitwise Exclusive OR Im² Z³ Zx⁴ Ab⁴ Ax⁴ + Ay⁴ Ix⁶ Iy⁵ +  Ay⁴ Ix⁶ Iy⁵ +  NUBDIZC Transfer Y to A  Ip² NUBDIZC Bitwise OR with Accumulator Im² Z³ Zx⁴ Ab⁴ Ax⁴ + Ay⁴ Ix⁶ Iy⁵ +  NUBDIZC Transfer A to X Ip²  BYL NUBDIZC Branch on PLus Lb² NUBDIZC Branch on MInus Ip²  NUBDIZC  SEC NUBDIZC Transfer A to X Ip²  INY NUBDIZC Transfer Stack to Y Ip²  InY NUBDIZC Transfer
AND NUBDIZC Ditwise AND with accumulator with accumulator Im² Z³ Zx⁴ Ab⁴ Ax⁴ Ay⁴ Ix⁶ Iy⁵⁴ DEC NUBDIZC Arithmetic Shift Left A² Z⁵ Zx⁶ Ab⁶ Ax² Im² Z³ Zx⁴ Ab⁴ Ax⁴ Ay⁴ Ix⁶ Iy⁵⁴ NUBDIZC Transfer Y to A Ip² Im² NUBDIZC Transfer A to Y Ip² Im² NUBDIZC Transfer Y to A Ip² Im² NUBDIZC Transfer A to X Ip² Im² NUBDIZC Transfer A to X Ip² Im² Im² Im² Im² Im² Im² Im² Im² Im² Im
bitwise AND with accumulator  Im <sup>2</sup> Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>4+</sup> Ay <sup>4+</sup> Ix <sup>6</sup> Iy <sup>5+</sup> ASL NUBDIZC Arithmetic Shift Left A <sup>2</sup> Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> BIT NUBDIZC test BITs Z <sup>3</sup> Ab <sup>4</sup> BPL NUBDIZC CLear Carry Ip <sup>2</sup> BPL NUBDIZC SET Carry  BPL NUBDIZC SET CARR
SITUSE HIND WITH accumulator  Im <sup>2</sup> Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>4+</sup> Ay <sup>4+</sup> Ix <sup>6</sup> Iy <sup>5+</sup> BIT NUBDIZC  Test BITs  Z <sup>3</sup> Ab <sup>4</sup> BPL NUBDIZC  Branch on PLus  Lb <sup>2+</sup> BVI NUBDIZC  Branch on MInus  NUBDIZC  Branch on MInus  NUBDIZC  Branch on MInus  NUBDIZC  Branch on MInus  NUBDIZC  Transfer A to X  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  Transfer Stack to X  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  Transfer Stack to X  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup> NUBDIZC  Transfer X to A  Ip <sup>2</sup> NUBDIZC  DECRMENT Y  Ip <sup>2</sup>
Im <sup>2</sup> Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>4+</sup> Ay <sup>4+</sup> Ix <sup>6</sup> Iy <sup>5+</sup> NUBDIZC Arithmetic Shift Left A <sup>2</sup> Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> BIT NUBDIZC test BITs Z <sup>3</sup> Ab <sup>4</sup> BPL NUBDIZC Branch on PLus Lb <sup>2+</sup> BYT NUBDIZC Branch on MInus Lc <sup>2+</sup> DECrement Memory Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> DECrement Memory Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> Ip <sup>2</sup> NUBDIZC DIA NUBDIZC DECREMENT Y to A DECREMENT Y
ASL NUBDIZC Arithmetic Shift Left A2 Z5 Zx6 Ab6 Ax7  BIT NUBDIZC test BITs Z3 Ab4  BPL NUBDIZC Branch on PLus Lb2+  BMI NUBDIZC Branch on MInus Lt2+  BOR NUBDIZC BOR NUBDIZC BOR NUBDIZC BOR NUBDIZC BOR NUBDIZC Bitwize OR with Accumulator  BMI NUBDIZC BOR NUBDIZC BITWI NUBDIZC BITWI NUBDIZC BOR NUBDIZC BITWI NUBDIZC BITWI NUBDIZC BOR NUBDIZC BITWI NUBDIZC BITWI NUBDIZC BITWI NUBDIZC BITWI NUBDIZC BITMI NUBDIZC BI
ASL NUBDIZC ASL NUBDIZC ASL NUBDIZC ASL NUBDIZC AST NU
Arithmetic Shift Left A2 Z5 Zx6 Ab6 Ax7  BIT NUBDIZC test BITs Z3 Ab4  BPL NUBDIZC Branch on PLus Lb2+  BMT NUBDIZC Branch on MInus Lt2+  BMT NUBDIZC Branch on MInus Lt2+  BNUBDIZC BRANCH OR ARACH ARACH BRACCUMUIATOR  BRCCUMUIATOR  BRCCUMUIA
Arithmetic Shift Left A2 Z5 Zx6 Ab6 Ax7  BIT NUBDIZC Test BITs Z3 Ab4 Ax4+ Ay4+ Ix6 Iy5+ Ay4+ Ix6 Iy
BIT NUBDIZC  test BITs  Z³Ab⁴  NUBDIZC  CLear Carry  Ip²  NUBDIZC  Transfer A to X  Ip²  INY NUBDIZC  INCREMENT Y  Ip²  INCREMENT Y  Ip²  IP²  INCREMENT Y  Ip²  IP²  INCREMENT Y  IP²  INCREMEN
TAX NUBDIZC  Test BITs  Z³Ab4  BPL NUBDIZC  Branch on PLus  Lb2+  BMI NUBDIZC  Branch on MInus  ELC NUBDIZC  Transfer A to X  Ip2  INV NUBDIZC  Transfer A to X  Ip2  IP2  IVA NUBDIZC  Transfer X to A  Ip2  IVA NUBDIZC  Transfer X to A  Ip2  IVA NUBDIZC  Transfer Stack to X  Ip2  BMI NUBDIZC  Branch on MInus  L2+  NUBDIZC  DEX NUBDIZC  Push Accumulator
Transfer A to X  Increment Y  Ip2  BP1 NVBDIZC Branch on PLus Lb2+  BVI NVBDIZC BVI NVBDIZ
Z³Ab4  CLear Carry Ip²  Ip²  Ip²  Ip²  Ip²  Ip²  Ip²  Ip²
BPL NUBDIZC Branch on PLus Lb2+  BMI NUBDIZC Branch on MInus Lb2+  NUBDIZC Branch on MInus Lb2+  NUBDIZC Branch on MInus Lb2+  NUBDIZC DECREMENT X  Ip2  NUBDIZC PHA NUBDIZC Push Accumulator
Branch on PLus Lb2+  SET Carry  BMI NUBDIZC Branch on MInus Lb2+  NUBDIZC  Branch on MInus Lb2+  NUBDIZC  DECREMENT X to A Lp2  NUBDIZC  DECREMENT X  NUBDIZC  Push Accumulator
Branch on PLus Lb2+  SET Carry  Ip2  BMI NVBDIZC Branch on MInus L 2+  NVBDIZC  NVBDIZC  NVBDIZC  DECRMENT X  NVBDIZC  Push Accumulator
BYI NVBDIZC Branch on MInus L2+  SEt Carry Ip2 Ip2 Ip2 IP2 PHA NVBDIZC DEcrement X
Branch on MInus  L.2+  NUBDIZC  DEX NUBDIZC  PHA NUBDIZC  Push Accumulator
Branch on MInus  NUBDIZC DEcrement X  Push Accumulator
DECREMENT X Push Accumulator
T-4
BUD NUBDIZO DI O NUBDIZO
Branch on overflow ST NVBDIZC INcrement X Pull Accumulator
Lb2+ SEt Interrupt Ip2 Ip4
ROS NOBDIZO PRIP NOBDIZO
Branch on overflow CLU NVBDIZC ROtate Left Push Processor Set 2 5 6 6 7
CLEAR OVERTION AZ 73 7x6 Ab 6x1
- Ing NVBDIZC
NUBDIZC NUBDIZC ROTATE Right PLP NUBDIZC
Branch on Carry Class Decives a2 75 7.6 o. 6 o. 7 Pull Processor
BCS NUBDIZC SED NUBDIZC ReTurn from STX NUBDIZC
Branch on Carry Set SEt Decimal STore X register
Lb2+ Ip <sup>2</sup> 73 7u <sup>4</sup> 8b <sup>4</sup>
ALS NABDISC
BNE NVBDIZC TYP NVBDIZC ReTurn from STY NVBDIZC
Branch on Not Equal Jump Subroutine STore Y register
Lb2+ Ab3 In5 Ip6 Z3 Zx4 Ab4