

65C02 INSTRUCTIONS

Modes		LSR		NUBDIZC		BEQ		NUBDIZC		Transfer	
Ip	Implied	Logical Shift Right		Branch on Equal		TAX		NUBDIZC		Transfer A to X	
Ac	Accumulator	Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		R ²		Transfer A to X		Ip ²			
Im	Immediate	ROL		NUBDIZC		BNE		NUBDIZC		TAY	
Z	ZeroPage	ROtate Left		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		Branch on Not Equal		R ²		Transfer A to Y	
Zx	ZeroPage,X	ROR		NUBDIZC		BCC		NUBDIZC		TXA	
Zy	ZeroPage,Y	ROtate Right		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		Branch on Carry Clear		R ²		Transfer X to A	
Ab	Absolute	AND		NUBDIZC		BCS		NUBDIZC		TYA	
Ax	Absolute,X	bitwise AND with accumulator		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Branch on Carry Set		R ²		Transfer Y to A	
Ay	Absolute,Y	Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		BUC		NUBDIZC			
R	Relative	ORA		NUBDIZC		Branch on oVerflow Clear		R ²		Calc	
Ix	Ind, zp X	bitwise OR with Accumulator		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		BUS		NUBDIZC		INA	
IaX	Ind, abs X	Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		Branch on oVerflow Set		R ²		INcrement Accumulator	
Iy	Ind, zp Y	EOR		NUBDIZC		BMI		NUBDIZC		INX	
Iz	Ind, zp	bitwise Exclusive OR		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Branch on MInus		R ²		INcrement X	
Ia	Ind, abs	Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		BPL		NUBDIZC		INY	
Load & Store		BIT		NUBDIZC		Branch on PLus		R ²		INcrement Y	
LDA	NUBDIZC	test BITs		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		BBR<0-7>		NUBDIZC		DEA	
Load Accumulator		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		Branch on Bit Reset		R ²		DEcrement Accumulator	
LDX	NUBDIZC	CMP		NUBDIZC		BBS<0-7>		NUBDIZC		DEX	
Load X register		CoMPare accumulator		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Branch on Bit Set		R ²		DEcrement X	
LDY	NUBDIZC	Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		Stack		PHA		DEY	
Load Y register		CPX		NUBDIZC		Push Accumulator		NUBDIZC		DEcrement Y	
Store Accumulator		CoMPare X register		Im ² Z ³ Ab ⁴		Ip ³		PHX		INC	
STX	NUBDIZC	Im ² Z ³ Ab ⁴		CPY		Push X register		NUBDIZC		INCrement memory	
Store X register		CoMPare Y register		Im ² Z ³ Ab ⁴		Ip ³		PHY		Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺	
STY	NUBDIZC	Im ² Z ³ Ab ⁴		TRB		NUBDIZC		Push Y register		Ip ³	
Store Y register		Test and Reset Bits		Z ⁵ Ab ⁶		PHP		NUBDIZC		DEC	
STZ	NUBDIZC	TSB		NUBDIZC		Push Processor status		NUBDIZC		DEcrement memory	
Store Zero		Test and Set Bits		Z ⁵ Ab ⁶		Ip ³		PLA		Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺	
Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺		RMB		NUBDIZC		PLX		NUBDIZC		SBC	
State		Reset Memory Bit		Z ⁵ Ab ⁶		Pull X register		NUBDIZC		SuBtract with Carry	
CLC	NUBDIZC	SMB		NUBDIZC		PLP		NUBDIZC		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺	
Clear Carry		Set Memory Bit		Z ⁵ Ab ⁶		Pull Processor status		NUBDIZC		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵	
Ip ²		Flow		JMP		NUBDIZC		PLX		NUBDIZC	
CLD	NUBDIZC	JUMP		Ab ³ Ia ⁵⁺ IaX ⁶⁺		NuMP		NUBDIZC		SuBtract with Carry	
Clear Decimal		JSR		NUBDIZC		Transfer X to Stack		NUBDIZC		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺	
Ip ²		Jump to SubRoutine		Ab ⁶		Ip ²		TXS		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵	
CLI	NUBDIZC	RTS		NUBDIZC		Transfer X to X		NUBDIZC		Misc	
Clear Interrupt		ReTurn from Subroutine		Ip ⁶		Ip ²		TXS		BRK	
Ip ²		RTI		NUBDIZC		Transfer Stack to X		NUBDIZC		BReaK	
CLU	NUBDIZC	ReTurn from Interrupt		Ip ⁶		Ip ²		TXS		Ip ⁷	
Clear oVerflow		BRA		NUBDIZC		Transfer Stack to X		NUBDIZC		NOP	
Ip ²		BRanch Always		R ³		Ip ²		TXS		No OPeration	
SEC	NUBDIZC	ASL		NUBDIZC		Ip ²		TXS		STP	
Set Carry		Arithmetic Shift Left		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		Ip ²		TXS		SToP	
Ip ²		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		R ³		Ip ²		TXS		Ip ³	
SED	NUBDIZC	R ³		R ³		Ip ²		TXS		Wait for Interrupt	
Set Decimal		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ²		R ³		R ³		Ip ²		TXS		Ip ³	
SEI	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Set Interrupt		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ²		R ³		R ³		Ip ²		TXS		Ip ³	
Bits		R ³		R ³		Ip ²		TXS		Ip ³	
ASL	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Arithmetic Shift Left		R ³		R ³		Ip ²		TXS		Ip ³	
Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		R ³		R ³		Ip ²		TXS		Ip ³	
Flow		R ³		R ³		Ip ²		TXS		Ip ³	
JMP	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
JuMP		R ³		R ³		Ip ²		TXS		Ip ³	
Ab ³ Ia ⁵⁺ IaX ⁶⁺		R ³		R ³		Ip ²		TXS		Ip ³	
JSR	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Jump to SubRoutine		R ³		R ³		Ip ²		TXS		Ip ³	
Ab ⁶		R ³		R ³		Ip ²		TXS		Ip ³	
RTS	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
ReTurn from Subroutine		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ⁶		R ³		R ³		Ip ²		TXS		Ip ³	
RTI	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
ReTurn from Interrupt		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ⁶		R ³		R ³		Ip ²		TXS		Ip ³	
BRA	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
BRanch Always		R ³		R ³		Ip ²		TXS		Ip ³	
R ³		R ³		R ³		Ip ²		TXS		Ip ³	
BEQ	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on Equal		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BNE	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on Not Equal		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BCC	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on Carry Clear		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BCS	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on Carry Set		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BUC	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on oVerflow Clear		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BUS	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on oVerflow Set		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BMI	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on MInus		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BPL	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on PLus		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BBR<0-7>	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on Bit Reset		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
BBS<0-7>	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Branch on Bit Set		R ³		R ³		Ip ²		TXS		Ip ³	
R ²		R ³		R ³		Ip ²		TXS		Ip ³	
Stack		R ³		R ³		Ip ²		TXS		Ip ³	
PHA	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Push Accumulator		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ³		R ³		R ³		Ip ²		TXS		Ip ³	
PHX	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Push X register		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ³		R ³		R ³		Ip ²		TXS		Ip ³	
PHY	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Push Y register		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ³		R ³		R ³		Ip ²		TXS		Ip ³	
PHP	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Push Processor status		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ³		R ³		R ³		Ip ²		TXS		Ip ³	
PLA	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Pull Accumulator		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ⁴		R ³		R ³		Ip ²		TXS		Ip ³	
PLP	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Pull Processor status		R ³		R ³		Ip ²		TXS		Ip ³	
Ip ⁴		R ³		R ³		Ip ²		TXS		Ip ³	
PLX	NUBDIZC	R ³		R ³		Ip ²		TXS		Ip ³	
Pull X register		R ³		R ³		Ip<					