65C02 INSTRUCTIONS

		TRUCTIONS	
Modes	LSR NVBDIZC	BEQ NVBDIZC	Transfer
	Logical Shift Right	Branch on EQual	
Ip Implied Ac Accumulator	Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺	R ²	
Im Immediate #\$12	ROL NVBDIZC	BNE NVBDIZC	Transfer A to X
Z ZeroPage \$12	ROtate Left	Branch on Not Equal	Ip ²
Zx ZeroPage,X \$12,X Zy ZeroPage,Y \$12,Y	Ac2 Z5 Zx6 Ab6 Ax7+	R2	TAY NUBDIZC
Ab Absolute \$1234			Thaneson A to V
Ax Absolute,X \$1234,X	ROR NVBDIZC	BCC NVBDIZC	Ip2
Ay Absolute,Y \$1234,Y	KUtate Kight	Branch on Carry Clear	
R Relative LABEL Ix Ind, zp X (\$12,X)	Ac2 Z5 Zx6 Ab6 Ax7+	R ²	TXA NVBDIZC
IAx Ind, abs X (\$1234,X)	AND NUBDIZC	BCS NVBDIZC	Transfer X to A
Iy Ind, zp Y (\$12),Y	bitwise AND with	Branch on Carry Set	I _P 2
Iz Ind, zp (\$12)	accumulator	_2	TVA NUBDIZC
Ia Ind, abs (\$1234)	Iм2 Z3 Zx4 Ab4 Ax4+		
Load & Store	Ay4+ Ix6 Iy5 Iz5	BUC NVBDIZC	- 2
	DRA NVBDIZC	Branch on oVerflow Clear	Ip ²
	bitwize OR with	Clear	Calc
LoaD Accumulator	Accumulator	R ²	
Iм ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴	TM2 73 7x4 Ab4 Ax4+	BUS NVBDIZC	INA NVBDIZC
Ay4+ Ix6 Iy5 Iz5	Au4+ Ix6 Iu5 Iz5	Branch on oVerflow Set	INcrement Accumulator
NVBDIZC	FOR NUBDIZC	R2	Ac ²
LoaD X register	2200		CTTT NUDDITE
IM2 Z3 Zy4 Ab4 Ay4+	bitwise Exclusive OR	BMI NVBDIZC	INX NVBDIZC
	IM2 Z3 Zx4 Ab4 Ax4+	Branch on MInus	INcrement X
CD I	119 1A 19 1E	R ²	Ip ²
LoaD Y register	BIT NVBDIZC	BPL NVBDIZC	NUBDIZC
Im2 Z3 Zy4 Ab4 Ay4+	test bils	Branch on PLus	INcrement Y
STA NVBDIZC	IM2 Z3 Zx4 Ab4 Ax4+	R ²	Ip ²
STore Accumulator	ESTER NUMBER C	K-	Th-
Z3 Zx4 Ab4 Ax5+ Ay5+	CoMPare accumulator	BBRC0-7> NVBDIZC	DEA NUBDIZC
Ix6 Iy6 Iz5	COLL OF ACCOMMENTATION	Pranck on Rit Paget	DEcrement Accumulator
COURT NUMBER TO CO	IM ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺ Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵	R ²	Ac ²
STX NVBD12C STore X register	Hy4. Ixo Iyo Izo	RRGZG=75 NURDIZC	DEX NUBDIZC
	CPX NVBDIZC	BBS(8-7) NVBDIZC Branch on Bit Set	DEX NVBDIZC
Z ³ Zy ⁴ Ab ⁴	ComPare X register		DECREMENT A
STY NVBDIZC	I _M 2 _Z 3 _{Ab} 4	R ²	Ip2
STore Y register	AM E NO		
	CPY NVBDIZC	Stack	
STore Y register Z ³ Zx ⁴ Ab ⁴	CPY NUBDIZC ComPare Y register	Stack PMA NVBDIZC	DEY NUBDIZC DEcrement Y
STore Y register Z ³ Z× ⁴ Ab ⁴ SIZ NUBDIZC STore Zero	ComPare Y register Im ² Z ³ Ab ⁴	Stack PIG NVBDIZC Push Accumulator	DECREMENT Y Ip2
STore Y register Z ³ Z× ⁴ Ab ⁴ SIZ NUBDIZC STore Zero	COMPare Y register Im ² Z ³ Ab ⁴ TRB NUBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3	DEY NUBDIZC DEcrement Y Ip ² ING NUBDIZC
STore Y register Z3 Zx4 Ab4 STZ NUBDIZC STore Zero Z3 Zx4 Ab4 Ax5+	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC	DEY NUBDIZC DEcrement Y Ip ² NUBDIZC INCrement memory
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRE NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶	Stack PHA NVBDIZC Push Accumulator Ip ³ PHX NVBDIZC Push X register	DEY NUBDIZC DEcrement Y Ip ² ING NUBDIZC
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State NUBDIZC	CPY NVBDIZC ComPare Y register Im² Z³ Ab⁴ TRE NVBDIZC Test and Reset Bits Z⁵ Ab⁶ TSE NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺ NUBDIZC
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State NUBDIZC CLear Carry	CPY NVBDIZC ComPare Y register Im² Z³ Ab⁴ TRE NVBDIZC Test and Reset Bits Z⁵ Ab⁶ TSE NVBDIZC Test and Set Bits	Stack PUB NVBDIZC PusH Accumulator Ip ³ PUX NVBDIZC PusH X register Ip ³	DEY NUBDIZC DEcrement Y Ip ² INC NUBDIZC INCrement memory Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺ DEC NUBDIZC
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State NUBDIZC	CPY NVBDIZC ComPare Y register Im² Z³ Ab⁴ TRE NVBDIZC Test and Reset Bits Z⁵ Ab⁶ TSE NVBDIZC	Stack PUB NVBDIZC PusH Accumulator Ip ³ PUX NVBDIZC PusH X register Ip ³	DEY NUBDIZC DEcrement Y Ip ² INC NUBDIZC INCrement memory Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺ DEC NUBDIZC
STore Y register Z ³ Zx ⁴ Ab ⁴ SIZ NUBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State State CLear Carry Ip ²	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶	Stack PUB NVBDIZC PusH Accumulator Ip ³ PUX NVBDIZC PusH X register Ip ³	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NVBDIZC STORE Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State State CLear Carry Ip ² NVBDIZC	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip ³ PHX NVBDIZC PusH X register Ip ³ PHY NVBDIZC PusH Y register Ip ³	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory Z5 Zx6 Ab6 Ax7+ DEC NUBDIZC DECrement memory Z5 Zx6 Ab6 Ax7+ ADC NUBDIZC
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NVBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺ State CLC CLear Carry Ip ² CLD NVBDIZC CLear Decimal	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRE NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSE NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RVB NVBDIZC Reset Memory Bit	Stack PHA NVBDIZC PusH Accumulator Ip ³ PHX NVBDIZC PusH X register Ip ³ PHY NVBDIZC PusH Y register Ip ³ PHY NVBDIZC PusH Y register	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement memory
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STORE Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State State FIG NUBDIZC CLear Carry Ip ² CLear Decimal Ip ²	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NUBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NUBDIZC Reset Memory Bit Z ⁵ Ab ⁶	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NVBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State CLEAR Carry Ip ² CLEAR Decimal Ip ² NVBDIZC	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NVBDIZC Reset Memory Bit Z ⁵ Ab ⁶ SMB NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3	DEY NUBDIZC DECREMENT Y Ip ² INC NUBDIZC INCrement memory Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷ + DEC NUBDIZC DECREMENT memory Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷ + ADC NUBDIZC ADD with Carry
STORE Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STORE Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺ State State CLEAR Carry Ip ² CLEAR Decimal Ip ² NUBDIZC CLEAR Decimal Ip ² NUBDIZC CLEAR Interrupt	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NVBDIZC Reset Memory Bit Z ⁵ Ab ⁶ SMB NVBDIZC Set Memory Bit	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement Memory
STore Y register Z ³ Zx ⁴ Ab ⁴ STZ NVBDIZC STore Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵ + State CLEAR Carry Ip ² CLEAR Decimal Ip ² NVBDIZC	CPY NVBDIZC ComPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NVBDIZC Reset Memory Bit Z ⁵ Ab ⁶ SMB NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC PusH Processor status Ip3 PLA NVBDIZC PusH Accumulator	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z ³ Zx ⁴ Ab ⁴ STZ NUBDIZC STORE Zero Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺ State State CLEAR Carry Ip ² CLEAR Decimal Ip ² NUBDIZC CLEAR Decimal Ip ² NUBDIZC CLEAR Interrupt	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSB NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory
STore Y register Z³ Zx⁴ Ab⁴ STZ NVBDIZC STore Zero Z³ Zx⁴ Ab⁴ Ax5+ State CIC NVBDIZC CLear Carry Ip² CLear Decimal Ip² NVBDIZC CLear Interrupt Ip²	CPY NVBDIZC ComPare Y register Im² Z³ Ab⁴ TRB NUBDIZC Test and Reset Bits Z⁵ Ab6 TSB NVBDIZC Test and Set Bits Z⁵ Ab6 RMB NUBDIZC Reset Memory Bit Z⁵ Ab6 SMB NVBDIZC Set Memory Bit Z⁵ Ab6 Flow	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State GIC NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR Interrupt Ip2 CLEAR OVERFIOW	CPY COMPare Y register IM2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSB NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow TSB NVBDIZC RMB NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory
STORE Y register Z3 Zx4 Ab4 SIZ NUBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State FIC NUBDIZC CLear Carry Ip2 CLear Decimal Ip2 CLear Interrupt Ip2 CLear overflow Ip2	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4 IRB NVBDIZC Test and Reset Bits Z5 Ab6 ISB NVBDIZC Test and Set Bits Z5 Ab6 RNB NVBDIZC Reset Memory Bit Z5 Ab6 SNB NVBDIZC Set Memory Bit Z5 Ab6 Flow JNP NVBDIZC Jump	Stack PHA NUBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NUBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NUBDIZC Pull Accumulator Ip4 PLA NVBDIZC Pull Processor status	DEY NUBDIZC DEcrement Y Ip2 INC NUBDIZC INCrement memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State FIC NVBDIZC CLear Carry Ip2 FID NVBDIZC CLear Decimal Ip2 CLear Interrupt Ip2 CLear overflow Ip2 SEC NVBDIZC	CPY COMPare Y register IM2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSB NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump Ab3 Ia5+ IAx6+	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4	DEY NUBDIZC DEcrement Y Ip2 INC NVBDIZC INCrement Memory Z5 Zx6 Ab6 Ax7+ DEC NVBDIZC DECrement Memory Z5 Zx6 Ab6 Ax7+ ADC NVBDIZC ADD with Carry IM2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5 Iz5 SEC NVBDIZC SuBtract with Carry IM2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5 Iz5 Misc
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State GIC NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR Interrupt Ip2 CLEAR OVERFLOW Ip2 SEC NVBDIZC SET Carry	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4 IRB NVBDIZC Test and Reset Bits Z5 Ab6 ISB NVBDIZC Test and Set Bits Z5 Ab6 RNB NVBDIZC Reset Memory Bit Z5 Ab6 SNB NVBDIZC Set Memory Bit Z5 Ab6 Flow JNP NVBDIZC Jump	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State FIC NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR Interrupt Ip2 CLEAR OVERFIOW Ip2 SEC NVBDIZC SET Carry Ip2	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4 IRE NVBDIZC Test and Reset Bits Z5 Ab6 ISE NVBDIZC Test and Set Bits Z5 Ab6 RMS NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump to SubRoutine	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLP NVBDIZC Pull Processor status Ip4 PLP NVBDIZC Pull Processor status Ip4 PLX NVBDIZC Pull X register	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State GIC NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR Interrupt Ip2 CLEAR OVERFLOW Ip2 SEC NVBDIZC SET Carry	CPY NVBDIZC ComPare Y register Im² Z³ Ab⁴ TRB NVBDIZC Test and Reset Bits Z⁵ Ab6 TSB NVBDIZC Test and Set Bits Z⁵ Ab6 RMB NVBDIZC Reset Memory Bit Z⁵ Ab6 SMB NVBDIZC Set Memory Bit Z⁵ Ab6 Flow JMP NVBDIZC Jump Ab³ Ia⁵+ IAx6+ USR NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State CIC NVBDIZC CLear Carry Ip2 CLear Decimal Ip2 CLear Interrupt Ip2 CLear oVerflow Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 SED NVBDIZC SET Decimal	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSB NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMB NVBDIZC Jump NVBDIZC Jump NVBDIZC Jump Ab3 Ia5+ IAx6+ JSR NVBDIZC Jump to SubRoutine Ab6	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLP NVBDIZC Pull Processor status Ip4 PLY NVBDIZC Pull Processor status Ip4 PLY NVBDIZC Pull Processor status Ip4	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State CIC NVBDIZC CLear Carry Ip2 CLear Decimal Ip2 CLear Interrupt Ip2 CLear oVerflow Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 SED NVBDIZC SET Decimal	CPY COMPare Y register IM2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSB NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump to SubRoutine Ab6 NVBDIZC Reset Memory Bit NVBDIZC	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLA NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4 PLA NVBDIZC Pull Processor status Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 STZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State STATE FIG. NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR NVBDIZC CLEAR OVERFLOW Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 NVBDIZC SET Decimal Ip2 NVBDIZC SET Decimal Ip2	CPY COMPare Y register IM2 Z3 Ab4 TRE NVBDIZC Test and Reset Bits Z5 Ab6 TSE NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump to SubRoutine Ab6 RMS NVBDIZC RETURN From Subroutine	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLY NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull X register	DEY NUBDIZC DECREMENT Y Ip2 INC NVBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State SIZ NVBDIZC CLear Carry Ip2 CLE NVBDIZC CLear Decimal Ip2 CLE NVBDIZC CLear Interrupt Ip2 CLU NVBDIZC CLear oVerflow Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 NVBDIZC SET Decimal Ip2 NVBDIZC SET Decimal Ip2 NVBDIZC	CPY COMPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NVBDIZC Reset Memory Bit Z ⁵ Ab ⁶ SMB NVBDIZC Set Memory Bit Z ⁵ Ab ⁶ Flow JMB NVBDIZC Set Memory Bit Z ⁵ Ab ⁶ Flow JMB NVBDIZC Set Memory Bit Ab ³ Ia ⁵⁺ IAx ⁶⁺ JSR NVBDIZC Jump to SubRoutine Ab ⁶ RTS NVBDIZC RETurn from Subroutine Ip ⁶	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLY NVBDIZC Pull Y register Ip4 PLX NVBDIZC Pull X register Ip4 PLY NVBDIZC Pull Y register Ip4	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 STZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State CLC CLear Carry Ip2 CLear Decimal Ip2 CLear Interrupt Ip2 CLear oVerflow Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Decimal Ip2 SED NVBDIZC SET Decimal Ip2 SET NVBDIZC SET Interrupt SED NVBDIZC SET Decimal Ip2 NVBDIZC SET Interrupt	CPY COMPare Y register IM2 Z3 Ab4 TRE NVBDIZC Test and Reset Bits Z5 Ab6 TSE NVBDIZC Test and Set Bits Z5 Ab6 RMB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump to SubRoutine Ab6 RMS NVBDIZC RETURN From Subroutine	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLY NVBDIZC Pull Y register Ip4 PLX NVBDIZC Pull X register Ip4 PLY NVBDIZC Pull Y register Ip4	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State SIZ NVBDIZC CLear Carry Ip2 CLE NVBDIZC CLear Decimal Ip2 CLE NVBDIZC CLear Interrupt Ip2 CLU NVBDIZC CLear oVerflow Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Carry Ip2 NVBDIZC SET Decimal Ip2 NVBDIZC SET Decimal Ip2 NVBDIZC	CPY COMPare Y register Im ² Z ³ Ab ⁴ TRB NVBDIZC Test and Reset Bits Z ⁵ Ab ⁶ TSB NVBDIZC Test and Set Bits Z ⁵ Ab ⁶ RMB NVBDIZC Reset Memory Bit Z ⁵ Ab ⁶ SMB NVBDIZC Set Memory Bit Z ⁵ Ab ⁶ Flow JMB NVBDIZC Set Memory Bit Z ⁵ Ab ⁶ Flow JMB NVBDIZC Set Memory Bit Ab ³ Ia ⁵⁺ IAx ⁶⁺ JSR NVBDIZC Jump to SubRoutine Ab ⁶ RTS NVBDIZC RETurn from Subroutine Ip ⁶	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLA NVBDIZC Pull Processor status Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull Y register Ip4	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 STZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State CLC CLear Carry Ip2 CLear Decimal Ip2 CLear Interrupt Ip2 CLear oVerflow Ip2 SEC NVBDIZC SET Carry Ip2 NVBDIZC SET Decimal Ip2 SED NVBDIZC SET Decimal Ip2 SET NVBDIZC SET Interrupt SED NVBDIZC SET Decimal Ip2 NVBDIZC SET Interrupt	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSE NVBDIZC Test and Set Bits Z5 Ab6 RNB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump NVBDIZC Jump NVBDIZC RESET NVBDIZC	Stack PHA NUBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NUBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NUBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLY NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull Y register Ip4 PLX NVBDIZC Pull Y register Ip4 PLX NVBDIZC Pull Y register Ip4 PLX NVBDIZC	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State FIC NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR NVBDIZC CLEAR OVERFLOW Ip2 SEC NVBDIZC CLEAR OVERFLOW Ip2 SEC NVBDIZC SET Carry Ip2 SET NVBDIZC SET Decimal Ip2 Bits	CPY COMPare Y register IM2 Z3 Ab4 IRB NVBDIZC Test and Reset Bits Z5 Ab6 ISB NVBDIZC Test and Set Bits Z5 Ab6 RNB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump NVBDIZC Jump NVBDIZC Jump NVBDIZC RETURN FROM Subroutine Ab6 RIS NVBDIZC RETURN FROM Subroutine Ip6 RII NVBDIZC RETURN FROM Interrupt Ip6	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC PuL1 Accumulator Ip4 PLP NVBDIZC PuL1 Processor status Ip4 PLY NVBDIZC PuL1 X register Ip4 PLY NVBDIZC PuL1 X register Ip4 PLY NVBDIZC PuL1 Y register Ip4 PLY NVBDIZC PuL1 Y register Ip4 IXS NVBDIZC Transfer X to Stack Ip2	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement memory
STORE Y register Z3 Zx4 Ab4 STZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State GLC NVBDIZC CLear Carry Ip2 CLD NVBDIZC CLear Decimal Ip2 NVBDIZC CLear Interrupt Ip2 SEC NVBDIZC CLear OVERFLOW Ip2 SEC NVBDIZC SET Carry Ip2 SET NVBDIZC SET Decimal Ip2 NVBDIZC SET Decimal Ip2 SET NVBDIZC SET NVBDIZC	CPY COMPare Y register IM2 Z3 Ab4 TRB NVBDIZC Test and Reset Bits Z5 Ab6 TSE NVBDIZC Test and Set Bits Z5 Ab6 RNB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC JUMP NVBDIZC JUMP NVBDIZC JUMP Ab3 Ia5+ IAx6+ JSR NVBDIZC JUMP Ab6 RTS NVBDIZC ReTurn from Subroutine Ip6 RTI NVBDIZC RETURN from Interrupt Ip6 RTI NVBDIZC	Stack PHA NUBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC Pull Accumulator Ip4 PLP NVBDIZC Pull Processor status Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull X register Ip4 PLX NVBDIZC Pull Y register Ip4 PLX NVBDIZC Pull Y register Ip4 PLX NVBDIZC Transfer X to Stack Ip2 ISX NVBDIZC	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory
STORE Y register Z3 Zx4 Ab4 SIZ NVBDIZC STORE Zero Z3 Zx4 Ab4 Ax5+ State GIC NVBDIZC CLear Carry Ip2 CLEAR Decimal Ip2 CLEAR Interrupt Ip2 CLEAR OVERFLOW Ip2 SEC NVBDIZC CLEAR OVERFLOW Ip2 SEC NVBDIZC SET Carry Ip2 SET NVBDIZC SET Decimal Ip2 SET NVBDIZC SET Decimal Ip2 SET NVBDIZC SET Interrupt Ip2 SET NVBDIZC SET Decimal Ip2 SET NVBDIZC SET Interrupt Ip2 Bits	CPY COMPare Y register IM2 Z3 Ab4 IRB NVBDIZC Test and Reset Bits Z5 Ab6 ISB NVBDIZC Test and Set Bits Z5 Ab6 RNB NVBDIZC Reset Memory Bit Z5 Ab6 SMB NVBDIZC Set Memory Bit Z5 Ab6 Flow JMP NVBDIZC Jump NVBDIZC Jump NVBDIZC Jump NVBDIZC Jump NVBDIZC RETURN FROM Subroutine Ab6 RIS NVBDIZC RETURN FROM Subroutine Ip6 RII NVBDIZC RETURN FROM Interrupt Ip6	Stack PHA NVBDIZC PusH Accumulator Ip3 PHX NVBDIZC PusH X register Ip3 PHY NVBDIZC PusH Y register Ip3 PHP NVBDIZC PusH Processor status Ip3 PLA NVBDIZC PuL1 Accumulator Ip4 PLP NVBDIZC PuL1 Processor status Ip4 PLY NVBDIZC PuL1 X register Ip4 PLY NVBDIZC PuL1 X register Ip4 PLY NVBDIZC PuL1 Y register Ip4 PLY NVBDIZC PuL1 Y register Ip4 IXS NVBDIZC Transfer X to Stack Ip2	DEY NUBDIZC DECREMENT Y Ip2 INC NUBDIZC INCrement Memory