

65C02 INSTRUCTIONS

Modes					
Ip	Implied				
Ac	Accumulator				
Im	Immediate	#s12			
Z	ZeroPage	\$12			
Zx	ZeroPage,X	\$12,X			
Zy	ZeroPage,Y	\$12,Y			
Ab	Absolute	\$1234			
Ax	Absolute,X	\$1234,X			
Ay	Absolute,Y	\$1234,Y			
R	Relative	LABEL			
Ix	Ind, zp X	(\$12,X)			
Iax	Ind, abs X	(\$1234,X)			
Iy	Ind, zp Y	(\$12,Y)			
Iz	Ind, zp	(\$12)			
Ia	Ind, abs	(\$1234)			
Load & Store					
LDA	NUBDIZC				
Load Accumulator					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
LDX	NUBDIZC				
Load X register					
		Im ² Z ³ Zy ⁴ Ab ⁴ Ay ⁴⁺			
LDY	NUBDIZC				
Load Y register					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ay ⁴⁺			
STA	NUBDIZC				
Store Accumulator					
		Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺ Ay ⁵⁺			
		Ix ⁶ Iy ⁶ Iz ⁵			
STX	NUBDIZC				
Store X register					
		Z ³ Zy ⁴ Ab ⁴			
STY	NUBDIZC				
Store Y register					
		Z ³ Zx ⁴ Ab ⁴			
STZ	NUBDIZC				
Store Zero					
		Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺			
State					
CLC	NUBDIZC				
Clear Carry					
		Ip ²			
CLD	NUBDIZC				
Clear Decimal					
		Ip ²			
CLI	NUBDIZC				
Clear Interrupt					
		Ip ²			
CLV	NUBDIZC				
Clear oVerflow					
		Ip ²			
SEC	NUBDIZC				
SEt Carry					
		Ip ²			
SED	NUBDIZC				
SEt Decimal					
		Ip ²			
SEI	NUBDIZC				
SEt Interrupt					
		Ip ²			
Bits					
ASL	NUBDIZC				
Arithmetic Shift Left					
		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺			
LSR	NUBDIZC				
Logical Shift Right					
		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺			
ROL	NUBDIZC				
ROtate Left					
		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺			
ROR	NUBDIZC				
ROtate Right					
		Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺			
AND	NUBDIZC				
bitwise AND with accumulator					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
ORA	NUBDIZC				
bitwise OR with Accumulator					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
EOR	NUBDIZC				
bitwise Exclusive OR					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
BIT	NUBDIZC				
test BITs					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
CMP	NUBDIZC				
CoMPare accumulator					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
CPX	NUBDIZC				
CoMPare X register					
		Im ² Z ³ Ab ⁴			
CPY	NUBDIZC				
CoMPare Y register					
		Im ² Z ³ Ab ⁴			
TRB	NUBDIZC				
Test and Reset Bits					
		Z ⁵ Ab ⁶			
TSB	NUBDIZC				
Test and Set Bits					
		Z ⁵ Ab ⁶			
RMB	NUBDIZC				
Reset Memory Bit					
		Z ⁵ Ab ⁶			
SMB	NUBDIZC				
Set Memory Bit					
		Z ⁵ Ab ⁶			
Flow					
JMP	NUBDIZC				
JuMP					
		Ab ³ Ia ⁵⁺ IAx ⁶⁺			
JSR	NUBDIZC				
Jump to SubRoutine					
		Ab ⁶			
RTS	NUBDIZC				
ReTurn from Subroutine					
		Ip ⁶			
RTI	NUBDIZC				
ReTurn from Interrupt					
		Ip ⁶			
BRA	NUBDIZC				
BRanch Always					
		R ³			
BEQ	NUBDIZC				
Branch on EQual					
		R ²			
BNE	NUBDIZC				
Branch on Not EQual					
		R ²			
BCC	NUBDIZC				
Branch on Carry Clear					
		R ²			
BCS	NUBDIZC				
Branch on Carry Set					
		R ²			
BUC	NUBDIZC				
Branch on oVerflow Clear					
		R ²			
BUS	NUBDIZC				
Branch on oVerflow Set					
		R ²			
BMI	NUBDIZC				
Branch on MInus					
		R ²			
BPL	NUBDIZC				
Branch on PLus					
		R ²			
BBR<0-7>	NUBDIZC				
Branch on Bit Reset					
		R ²			
BBS<0-7>	NUBDIZC				
Branch on Bit Set					
		R ²			
Stack					
PHA	NUBDIZC				
Push Accumulator					
		Ip ³			
PHX	NUBDIZC				
Push X register					
		Ip ³			
PHY	NUBDIZC				
Push Y register					
		Ip ³			
PHP	NUBDIZC				
Push Processor status					
		Ip ³			
PLA	NUBDIZC				
Pull Accumulator					
		Ip ⁴			
PLP	NUBDIZC				
Pull Processor status					
		Ip ⁴			
PLX	NUBDIZC				
Pull X register					
		Ip ⁴			
PLY	NUBDIZC				
Pull Y register					
		Ip ⁴			
TXS	NUBDIZC				
Transfer X to Stack					
		Ip ²			
TSX	NUBDIZC				
Transfer Stack to X					
		Ip ²			
Transfer					
TAX	NUBDIZC				
Transfer A to X					
		Ip ²			
TAY	NUBDIZC				
Transfer A to Y					
		Ip ²			
TXA	NUBDIZC				
Transfer X to A					
		Ip ²			
TYA	NUBDIZC				
Transfer Y to A					
		Ip ²			
Calc					
INA	NUBDIZC				
INcrement Accumulator					
		Ac ²			
INX	NUBDIZC				
INcrement X					
		Ip ²			
INY	NUBDIZC				
INcrement Y					
		Ip ²			
DEA	NUBDIZC				
DEcrement Accumulator					
		Ac ²			
DEX	NUBDIZC				
DEcrement X					
		Ip ²			
DEY	NUBDIZC				
DEcrement Y					
		Ip ²			
INC	NUBDIZC				
INCrement memory					
		Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺			
DEC	NUBDIZC				
DECrement memory					
		Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺			
ADC	NUBDIZC				
ADD with Carry					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
SBC	NUBDIZC				
SuBtract with Carry					
		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺			
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵			
Misc					
BRK	NUBDIZC				
BReak					
		Ip ⁷			
NOP	NUBDIZC				
No OPeration					
		Ip ²			
STP	NUBDIZC				
SToP					
		Ip ³			
WAI	NUBDIZC				
WAit for Interrupt					
		Ip ³			