## 65C02 INSTRUCTIONS

		TKUCTIUMO	
Modes	LSR NVBDIZC	REQ NVBDIZC	Transfer
	Logical Shift Right	Branch on EQual	
Ip Implied	Ac2 Z5 Zx6 Ab6 Ax7+	R <sup>2</sup>	TAX NVBDIZC
Ac Accumulator Im Immediate #\$12			Iransfer H to X
Z ZeroPage \$12		BNE NVBDIZC	Ip <sup>2</sup>
Zx ZeroPage,X \$12,X	ROtate Left	Branch on Not Equal	
Zy ZeroPage,Y \$12,Y	Ac2 Z5 Zx6 Ab6 Ax7+	R <sup>2</sup>	TAY NUBDIZC
Ab Absolute \$1234			Transfer A to Y
Ax Absolute,X \$1234,X	ROR NVBDIZC	BCC NVBDIZC	I <sub>P</sub> 2
Ay Absolute,Y \$1234,Y	ROtate Right	Branch on Carry Clear	
R Relative LABEL	<sub>Ac</sub> 2 <sub>Z</sub> 5 <sub>Zx</sub> 6 <sub>Ab</sub> 6 <sub>Ax</sub> 7+	R <sup>2</sup>	TXA NVBDIZC
Ix Ind, zp X (\$12,X) IAx Ind, abs X (\$1234,X)	AND NURDIZC	BCS NUBDIZC	Transfer X to A
	AND NOBDIZE		Ip2
Iy Ind, zp Y (\$12),Y Iz Ind, zp (\$12)	bitwise AND with accumulator	Branch on Carry Set	
To Total She (61224)		R <sup>2</sup>	TYA NVBDIZC
	1M- 24 2X 1HB 1HX 1	TOTAL NUMBER OF	Transfer Y to A
Load & Store	Im <sup>2</sup> Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>4+</sup> Ay <sup>4+</sup> Ix <sup>6</sup> Iy <sup>5</sup> Iz <sup>5</sup>	BOTH	Ip2
DA NVBDIZC	ORA NUBDIZC	Branch on oVerflow Clear	10
LoaD Accumulator	bitwize UK with		Calc
	Accumulator	R <sup>2</sup>	
Iм2 Z3 Zx4 дь4 дх4+	Tm2 73 7x4 Ab4 Ax4+	BUS NVBDIZC	INA NVBDIZC
Ay4+ Ix6 Iy5 Iz5	Au4+ 1v6 1u5 1z5	Branch on oVerflow Set	INcrement Accumulator
NVBDIZC	119 1A 19 12	R2	Ac <sup>2</sup>
LoaD X register	HOBDIZC	RE	
	bitwise Exclusive OR	BMI NUBDIZC	INX NVBDIZC
Im <sup>2</sup> Z <sup>3</sup> Zy <sup>4</sup> Ab <sup>4</sup> Ay <sup>4+</sup>	THE CALL OF THE	Branch on MInus	INcrement X
LDY NUBDIZC	Ay4+ Ix6 Iy5 Iz5	R <sup>2</sup>	Ip <sup>2</sup>
B III			
- 2 -3 - 4 - 4 - 4+	BIT	RPL NVBDIZC	INV NVBDIZC
Im <sup>2</sup> Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ay <sup>4+</sup>	test BITs	Branch on PLus	INcrement Y
STA NVBDIZC	IM2 Z3 Zx4 Ab4 Ax4+	<sub>2</sub> 2	Ip <sup>2</sup>
<del></del>			19
Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5+</sup> Ay <sup>5+</sup>	HOBDIZC	BBRC0-7> NVBDIZC	DEA NVBDIZC
Ix6 Iy6 Iz5		Branch on Bit Reset	DEcrement Accumulator
1x- 19- 12-	Im2 73 7x4 Ab4 Ax4+	<sub>R</sub> 2	Ac <sup>2</sup>
STX NVBDIZC			HC-
STore X register	rang MURDITAC	BBSC0=7> NVBDIZC	DEX NUBDIZC
Z <sup>3</sup> Zy <sup>4</sup> Ab <sup>4</sup>		Branch on Bit Set	DEcrement X
		R <sup>2</sup>	Ip <sup>2</sup>
STY NVBDIZC	I <sub>M</sub> 2 <sub>Z</sub> 3 <sub>Ab</sub> 4	N.	Ib-
		Stack	
		Stack	DEV NUBDIZC
STore Y register Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup>	CPY NVBDIZC ComPare Y register	Stack PHA NVBDIZC	DEY NUBDIZC DEcrement Y
STore Y register Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ NVBDIZC	CPY NVBDIZC ComPare Y register	Stack PHA NVBDIZC Push Accumulator	DET NUBDIZC DEcrement Y Ip <sup>2</sup>
STore Y register Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ NVBDIZC	COMPare Y register  Im <sup>2</sup> Z <sup>3</sup> Ab <sup>4</sup>	Stack PHA NVBDIZC Push Accumulator	DET NUBDIZC DEcrement Y Ip <sup>2</sup>
STore Y register Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ NVBDIZC	COMPare Y register  Im <sup>2</sup> Z <sup>3</sup> Ab <sup>4</sup>	Stack PHA NVBDIZC Push Accumulator	DET NUBDIZC DEcrement Y Ip2
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ NVBDIZC  STore Zero  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +	COMPare Y register Im <sup>2</sup> Z <sup>3</sup> Ab <sup>4</sup> TRE NVBDIZC Test and Reset Bits	Stack PHA NVBDIZC Push Accumulator Ip3 PHX NVBDIZC	DEY NUBDIZC DEcrement Y  Ip <sup>2</sup> INC NUBDIZC INCrement memory
STore Y register Z3 Zx4 Ab4 STZ NUBDIZC STore Zero Z3 Zx4 Ab4 Ax5+ State	CPY NVBDIZC ComPare Y register Im2 Z <sup>3</sup> Ab <sup>4</sup> TRB NVBDIZC Test and Reset Bits Z <sup>5</sup> Ab <sup>6</sup>	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register	DET NUBDIZC DEcrement Y Ip2
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ NVBDIZC  STore Zero  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +	CPY NVBDIZC ComPare Y register Im2 Z <sup>3</sup> Ab <sup>4</sup> TRB NVBDIZC Test and Reset Bits Z <sup>5</sup> Ab <sup>6</sup>	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup>	DEY NUBDIZC DEcrement Y  Ip <sup>2</sup> INC NUBDIZC INCrement memory Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> + NUBDIZC
STore Y register Z3 Zx4 Ab4 STZ NUBDIZC STore Zero Z3 Zx4 Ab4 Ax5+ State	CPY NVBDIZC ComPare Y register Im2 Z <sup>3</sup> Ab <sup>4</sup> TRB NVBDIZC Test and Reset Bits Z <sup>5</sup> Ab <sup>6</sup>	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup>	DEY NUBDIZC DEcrement Y  Ip <sup>2</sup> INC NUBDIZC INCrement memory Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> + NUBDIZC
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ  NUBDIZC  STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC  NUBDIZC  CLear Carry	CPY NUBDIZC ComPare Y register Im <sup>2</sup> Z <sup>3</sup> Ab <sup>4</sup> TRB NVBDIZC Test and Reset Bits Z <sup>5</sup> Ab <sup>6</sup> TSB NVBDIZC Test and Set Bits	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup> PHY NVBDIZC	DEY NUBDIZC DEcrement Y  Ip2  INC NUBDIZC INCrement memory  Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> +  DEC NUBDIZC DECrement memory
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC NUBDIZC  CLear Carry	CPY NUBDIZC ComPare Y register Im2 z3 Ab4 TRB NUBDIZC Test and Reset Bits z5 Ab6 TSB NUBDIZC Test and Set Bits Z5 Ab6	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup> PHY NVBDIZC  Push Y register	DEY NUBDIZC DEcrement Y  Ip <sup>2</sup> INC NUBDIZC INCrement memory Z <sup>5</sup> Zx <sup>6</sup> Ab <sup>6</sup> Ax <sup>7</sup> + NUBDIZC
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> SIZ NVBDIZC  STore Zero  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  GIC NVBDIZC  CLear Carry  Ip <sup>2</sup> GLD NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup> PHY NVBDIZC  Push Y register  Ip <sup>3</sup>	DEY NUBDIZC DEcrement Y  Ip2  INC NUBDIZC INCrement memory
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ  NVBDIZC  STore Zero  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC  CLear Carry  Ip <sup>2</sup> CLD  NVBDIZC  CLear Decimal	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RVB NVBDIZC Reset Memory Bit	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup> PHY NVBDIZC  Push Y register	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement memory
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ  NVBDIZC  STore Zero  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC  CLear Carry  Ip <sup>2</sup> CLD  NVBDIZC  CLear Decimal	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC	Stack  PHA NVBDIZC  Push Accumulator  Ip <sup>3</sup> PHX NVBDIZC  Push X register  Ip <sup>3</sup> PHY NVBDIZC  Push Y register  Ip <sup>3</sup>	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement memory
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> SIZ NVBDIZC  STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  GIC NVBDIZC  CLear Carry  Ip <sup>2</sup> CLD NVBDIZC  CLear Decimal	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6	Stack  PHA NVBDIZC  PusH Accumulator  Ip3  PHX NVBDIZC  PusH X register  Ip3  PHY NVBDIZC  PusH Y register  Ip3  PHP NVBDIZC  PusH Processor status	DEY NUBDIZC DEcrement Y  Ip2  INC NUBDIZC INCrement memory
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> SIZ NVBDIZC  STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC NVBDIZC  CLear Carry  Ip <sup>2</sup> CLD NVBDIZC  CLear Decimal  Ip <sup>2</sup> NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRB NUBDIZC Test and Reset Bits Z5 Ab6  TSB NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC	Stack  PHA NVBDIZC  Push Accumulator  Ip3  PHX NVBDIZC  Push X register  Ip3  PHY NVBDIZC  Push Y register  Ip3  PHP NVBDIZC  Push Processor status Ip3	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  GIC NVBDIZC  CLear Carry  Ip2  CLD CLear Decimal  Ip2  CLI NVBDIZC  CLear Interrupt	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NVBDIZC Test and Reset Bits Z5 Ab6  TSE NVBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NVBDIZC Reset Memory Bit SMB NVBDIZC Set Memory Bit	Stack  PHA NVBDIZC  Push Accumulator  Ip3  PHX NVBDIZC  Push X register  Ip3  PHY NVBDIZC  Push Y register  Ip3  PHP NVBDIZC  Push Processor status  Ip3  PLA NVBDIZC	DEY NUBDIZC DEcrement Y  Ip2  INC NVBDIZC INCrement memory
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> SIZ NVBDIZC  STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC NVBDIZC  CLear Carry  Ip <sup>2</sup> CLD NVBDIZC  CLear Decimal  Ip <sup>2</sup> NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRB NUBDIZC Test and Reset Bits Z5 Ab6  TSB NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC	Stack  PHA NVBDIZC  Push Accumulator  Ip3  PHX NVBDIZC  Push X register  Ip3  PHY NVBDIZC  Push Y register  Ip3  PHP NVBDIZC  Push Processor status  Ip3  PLA NVBDIZC  Pull Accumulator	DEY NUBDIZC DEcrement Y  Ip2  INC NVBDIZC INCrement memory
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ  NVBDIZC  STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC  CLear Carry  Ip <sup>2</sup> CLear Decimal  Ip <sup>2</sup> CLear Interrupt  Ip <sup>2</sup>	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RMB NVBDIZC Reset Memory Bit z5 Ab6  SMB NVBDIZC Set Memory Bit z5 Ab6	Stack  PHA NVBDIZC  Push Accumulator  Ip3  PHX NVBDIZC  Push X register  Ip3  PHY NVBDIZC  Push Y register  Ip3  PHP NVBDIZC  Push Processor status  Ip3  PLA NVBDIZC  Pull Accumulator	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement memory
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> SIZ NVBDIZC  STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> +  State  CLC NVBDIZC  CLear Carry  Ip <sup>2</sup> CLD NVBDIZC  CLear Decimal  Ip <sup>2</sup> CLI NVBDIZC  CLear Interrupt  Ip <sup>2</sup> CLU NVBDIZC	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RNB NVBDIZC Reset Memory Bit z5 Ab6  SNB NUBDIZC Set Memory Bit z5 Ab6  Flow	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Accumulator Ip4	NUBDIZC DECREMENT Y  Ip <sup>2</sup> INC NUBDIZC INCrement memory
STORE Y register  Z3 Zx4 Ab4  SIZ  NVBDIZC  STORE Zero  Z3 Zx4 Ab4 Ax5+  State  GIC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLI NVBDIZC  CLear Interrupt  Ip2  CLU NVBDIZC  CLear OVERF10W	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RMB NVBDIZC Reset Memory Bit z5 Ab6  SMB NVBDIZC Set Memory Bit z5 Ab6	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Accumulator Ip4  PLP NVBDIZC	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC  CLear Carry  Ip2  CLD  NVBDIZC  CLear Decimal  Ip2  CLI  NVBDIZC  CLear Interrupt  Ip2  CLU  CLear OVERFIOW  Ip2	CPV NVBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NVBDIZC Test and Set Bits z5 Ab6  RMB NVBDIZC Reset Memory Bit z5 Ab6  SMB NVBDIZC Set Memory Bit z5 Ab6  Flow  JMP NVBDIZC  JMP	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLP NVBDIZC Pull Processor status	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STore Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STZ  NUBDIZC  STore Zero  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5+</sup> State  CLC CLear Carry  Ip <sup>2</sup> CLD NUBDIZC CLear Decimal Ip <sup>2</sup> CLear Interrupt Ip <sup>2</sup> CLU CLear oVerflow Ip <sup>2</sup>	CPV NVBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NVBDIZC Test and Set Bits z5 Ab6  RMB NVBDIZC Reset Memory Bit z5 Ab6  SMB NVBDIZC Set Memory Bit z5 Ab6  Flow  JMP NVBDIZC  JMP	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLP NVBDIZC Pull Processor status	NUBDIZC DECREMENT Y  Ip <sup>2</sup> INC NUBDIZC INCrement memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE Zero  Z3 Zx4 Ab4 Ax5+  State  CLC CLear Carry  Ip2  CLD NVBDIZC CLear Decimal Ip2  CLEAR Interrupt  Ip2  CLU CLear oVerflow Ip2  SIC  NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Jump Ab3 Ia5+ IAx6+	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator Ip4  PLP NVBDIZC Pull Processor status Ip4	NUBDIZC DECREMENT Y  Ip2  INC NVBDIZC INCrement Memory Z5 Zx6 Ab6 Ax7+  DEC NUBDIZC DECREMENT MEMORY Z5 Zx6 Ab6 Ax7+  ADC ADD with Carry IM2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5 Iz5  SBC NUBDIZC SuBtract with Carry IM2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5 Iz5  MISC  MISC
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLU NVBDIZC  CLear Interrupt  Ip2  CLU NVBDIZC  CLear OVERFIOW  Ip2  SEC NVBDIZC  SEt Carry	CPV NUBDIZC ComPare Y register Im2 z3 Ab4  TRE NUBDIZC Test and Reset Bits z5 Ab6  TSE NUBDIZC Test and Set Bits z5 Ab6  RNE NUBDIZC Reset Memory Bit z5 Ab6  SNE NUBDIZC Set Memory Bit z5 Ab6  Flow JNP NUBDIZC Jump Ab3 Ia5+ IAx6+  USR NUBDIZC	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator Ip4  PLP NVBDIZC Pull Processor status Ip4  PLA NVBDIZC Pull Processor status Ip4  PLA NVBDIZC Pull Processor status Ip4  PLA NVBDIZC	NUBDIZC DECREMENT Y  Ip2  INC NVBDIZC INCrement Memory Z5 Zx6 Ab6 Ax7+  DEC NUBDIZC DECREMENT MEMORY Z5 Zx6 Ab6 Ax7+  ADC ADD with Carry IM2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5 Iz5  SBC NUBDIZC SuBtract with Carry IM2 Z3 Zx4 Ab4 Ax4+ Ay4+ Ix6 Iy5 Iz5  MISC  MISC
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> State  CIC NUBDIZC  CLear Carry  Ip <sup>2</sup> CLD NVBDIZC  CLear Decimal  Ip <sup>2</sup> CLear Interrupt  Ip <sup>2</sup> CLear oVerflow  Ip <sup>2</sup> SEC NVBDIZC  SET Carry  Ip <sup>2</sup>	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RVB NVBDIZC Reset Memory Bit z5 Ab6  SMB NVBDIZC Set Memory Bit z5 Ab6  Flow  JMP NVBDIZC Jump NVBDIZC Jump to SubRoutine	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Accumulator Ip4  PLP NVBDIZC Puli Processor status Ip4  PLA NVBDIZC Puli Processor status Ip4  PLA NVBDIZC Puli Processor status Ip4  PLA NVBDIZC Puli Processor status Ip4  PLX NVBDIZC Puli X register	DET NUBDIZC DECREMENT Y  Ip2  INC NVBDIZC INCrement memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLU NVBDIZC  CLear Interrupt  Ip2  CLU NVBDIZC  CLear OVERFIOW  Ip2  SEC NVBDIZC  SEt Carry	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NVBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RVB NVBDIZC Reset Memory Bit z5 Ab6  SMB NVBDIZC Set Memory Bit z5 Ab6  Flow  JMP NVBDIZC Jump NVBDIZC Jump to SubRoutine	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator Ip4  PLP NVBDIZC Pull Processor status Ip4  PLA NVBDIZC Pull Processor status Ip4  PLA NVBDIZC Pull Processor status Ip4  PLA NVBDIZC	DEY NUBDIZC DECREMENT Y  Ip2  INC NVBDIZC INCrement memory
STORE Y register  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> STORE ZERO  Z <sup>3</sup> Zx <sup>4</sup> Ab <sup>4</sup> Ax <sup>5</sup> State  CIC NUBDIZC  CLear Carry  Ip <sup>2</sup> CLD NVBDIZC  CLear Decimal  Ip <sup>2</sup> CLear Interrupt  Ip <sup>2</sup> CLear oVerflow  Ip <sup>2</sup> SEC NVBDIZC  SET Carry  Ip <sup>2</sup>	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SME NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump to SubRoutine Ab6	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLP NVBDIZC Pull Processor status Ip4  PLX NVBDIZC Pull Processor status Ip4  PLX NVBDIZC Pull X register  Ip4	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC CLear Carry  Ip2  CLD NVBDIZC CLear Decimal  Ip2  CLU CLear Interrupt  Ip2  CLU CLear oVerflow  Ip2  SEC SET Carry  NVBDIZC  SET Decimal	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NUBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RNB NUBDIZC Reset Memory Bit z5 Ab6  SNB NUBDIZC Set Memory Bit z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump to SubRoutine Ab6  RNB NUBDIZC Reset Memory Bit RNB NUBDIZC Reset Memory Bit RNB NUBDIZC Reset Memory Bit RNB NUBDIZC	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Processor status Ip4  PLY NVBDIZC Puli Processor status Ip4  PLY NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  SIZ  NVBDIZC  STORE Zero  Z3 Zx4 Ab4 Ax5+  State  GIC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLE NVBDIZC  CLear OVERFLOW  Ip2  SET Carry  Ip2  NVBDIZC  SET Carry  Ip2  NVBDIZC  SET Carry  Ip2  NVBDIZC  SET Decimal  Ip2	CPY NVBDIZC ComPare Y register Im2 Z3 Ab4  TRE NVBDIZC Test and Reset Bits Z5 Ab6  TSE NVBDIZC Test and Set Bits Z5 Ab6  RNE NVBDIZC Reset Memory Bit Z5 Ab6  SNE NVBDIZC Set Memory Bit Z5 Ab6  Flow  JNP NVBDIZC Jump Ab3 Ia5+ IAx6+  USR NVBDIZC Jump to SubRoutine Ab6  RIS NVBDIZC RETurn from Subroutine	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator Ip4  PLY NVBDIZC Pull Processor status Ip4  PLY NVBDIZC Pull Processor status Ip4  PLY NVBDIZC Pull Y register  Ip4  PLY NVBDIZC Pull Y register	DEY NUBDIZC DECREMENT Y  Ip2  INC NVBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC CLear Carry  Ip2  CLD NVBDIZC CLear Decimal  Ip2  CLU CLear Interrupt  Ip2  CLU CLear oVerflow  Ip2  SEC SET Carry  NVBDIZC  SET Decimal	CPY NUBDIZC ComPare Y register Im2 z3 Ab4  TRB NUBDIZC Test and Reset Bits z5 Ab6  TSB NUBDIZC Test and Set Bits z5 Ab6  RNB NUBDIZC Reset Memory Bit z5 Ab6  SNB NUBDIZC Set Memory Bit z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump to SubRoutine Ab6  RNB NUBDIZC Reset Memory Bit RNB NUBDIZC Reset Memory Bit RNB NUBDIZC Reset Memory Bit RNB NUBDIZC	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Processor status Ip4  PLY NVBDIZC Puli Processor status Ip4  PLY NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC  CLear Carry  Ip2  CLD  NVBDIZC  CLear Decimal  Ip2  CLU  CLear Interrupt  Ip2  CLU  CLear oVerflow  Ip2  SEC  SET Carry  Ip2  SED  NVBDIZC  SET Decimal  Ip2  SET  NVBDIZC  SET Decimal  Ip2  SET  NVBDIZC  SET  SET  NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RNE NUBDIZC Reset Memory Bit Z5 Ab6  SNE NUBDIZC Set Memory Bit Z5 Ab6  Flow  JNP NUBDIZC JUMP Ab3 Ia5+ IAx6+  JSR NUBDIZC Jump to SubRoutine Ab6  RIS NUBDIZC RETURN from Subroutine Ip6	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLA NVBDIZC Pull Processor status Ip4  PLY NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull X register  Ip4  PLY NVBDIZC Pull Y register  Ip4	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC  CLear Carry  Ip2  CLD  NVBDIZC  CLear Decimal  Ip2  CLU  CLear Interrupt  Ip2  CLU  CLear oVerflow  Ip2  SEC  SET Carry  Ip2  SED  NVBDIZC  SET Decimal  Ip2  SET  NVBDIZC  SET Decimal  Ip2  SET  NVBDIZC  SET  SET  NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump NUBDIZC Jump NUBDIZC RETURN FROM Subroutine Ab6  RTS NUBDIZC RETURN FROM Subroutine Ip6  RTI NUBDIZC	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Accumulator Ip4  PLP NVBDIZC Puli Processor status Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli Y register  Ip4  PLY NVBDIZC Puli Y register  Ip4  PLY NVBDIZC	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLU NVBDIZC  CLear Interrupt  Ip2  CLU NVBDIZC  CLear OVERFIOW  Ip2  SEC NVBDIZC  SET Carry  Ip2  SET NVBDIZC  SET Decimal  Ip2  NVBDIZC  SET Decimal  Ip2  NVBDIZC  SET NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RNE NUBDIZC Reset Memory Bit Z5 Ab6  SNE NUBDIZC Set Memory Bit Z5 Ab6  Flow  JNP NUBDIZC Set Memory Bit Z5 Ab6  Flow  JNP NUBDIZC JUMP Ab3 Ia5+ IAx6+  JSR NUBDIZC Jump to SubRoutine Ab6  RIS NUBDIZC ReTurn from Subroutine Ip6  RIS NUBDIZC ReTurn from Interrupt	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLY NVBDIZC Pull Processor status Ip4  PLY NVBDIZC Pull X register  Ip4  PLY NVBDIZC Pull X register  Ip4  PLY NVBDIZC Pull X register  Ip4  PLY NVBDIZC Pull Y register  Ip4	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  STZ  NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC  CLear Carry  Ip2  CLD  NVBDIZC  CLear Decimal  Ip2  CLU  CLear Interrupt  Ip2  CLU  CLear oVerflow  Ip2  SEC  SET Carry  Ip2  SED  NVBDIZC  SET Decimal  Ip2  SET  NVBDIZC  SET Decimal  Ip2  SET  NVBDIZC  SET  SET  NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump NUBDIZC Jump NUBDIZC RETURN FROM Subroutine Ab6  RTS NUBDIZC RETURN FROM Subroutine Ip6  RTI NUBDIZC	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Accumulator Ip4  PLP NVBDIZC Puli Processor status Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli Y register  Ip4  PLY NVBDIZC Puli Y register  Ip4  PLY NVBDIZC	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  GLC NVBDIZC  CLear Carry  Ip2  GLD NVBDIZC  CLear Decimal  Ip2  GLU NVBDIZC  CLear OVERFLOW  Ip2  SEC NVBDIZC  SET Carry  Ip2  SET NVBDIZC  SET Decimal  Ip2  NVBDIZC  SET Decimal  Ip2  NVBDIZC  SET Decimal  Ip2  SET NVBDIZC  SET Decimal  Ip2  SET NVBDIZC  SET Interrupt  Ip2  SET NVBDIZC  SET Decimal  Ip2  SET NVBDIZC  SET Interrupt  Ip2  SET NVBDIZC  SET Interrupt  Ip2	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Set Memory Bit Z5 Ab6  Flow  Flow  MUBDIZC JUMP Ab3 Ia5+ IAx6+  JSR NUBDIZC JUMP Ab6  RTS NUBDIZC RETURN from Subroutine Ip6  RTI NUBDIZC RETURN from Interrupt Ip6	Stack  PHA NVBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Puli Accumulator Ip4  PLP NVBDIZC Puli Processor status Ip4  PLX NVBDIZC Puli X register  Ip4  PLX NVBDIZC Puli Y register  Ip4  TXS NVBDIZC Transfer X to Stack Ip2	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLU NVBDIZC  CLear OVERFIOW  Ip2  SEC NVBDIZC  SET Carry  Ip2  SET NVBDIZC  SET Decimal  Ip2  NVBDIZC  SET Decimal  Ip2  NVBDIZC  SET NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump NUBDIZC Jump NUBDIZC Jump NUBDIZC Refurn from Subroutine Ab6  RTS NUBDIZC Refurn from Interrupt Ip6  RTI NUBDIZC Refurn from Interrupt Ip6  RTI NUBDIZC	Stack  PHA NUBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NUBDIZC Push Processor status  Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLP NVBDIZC Pull Processor status  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Transfer X to Stack  Ip2	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  GLC NVBDIZC  CLear Carry  Ip2  GLD NVBDIZC  CLear Decimal  Ip2  GLU NVBDIZC  CLear OVERFLOW  Ip2  SEC NVBDIZC  SET Carry  Ip2  SET NVBDIZC  SET Decimal  Ip2  SET NVBDIZC  SET NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SME NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC JUMP NUBDIZC JUMP NUBDIZC JUMP NUBDIZC JUMP NUBDIZC RETURN from Subroutine Ip6  RTI NUBDIZC RETURN from Interrupt Ip6	Stack  PHA NUBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NVBDIZC Push Processor status Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLP NVBDIZC Pull Processor status Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Pull Y register  Ip4  IXS NVBDIZC Transfer X to Stack Ip2  ISX NVBDIZC Transfer Stack to X	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory
STORE Y register  Z3 Zx4 Ab4  SIZ NVBDIZC  STORE ZERO  Z3 Zx4 Ab4 Ax5+  State  CLC NVBDIZC  CLear Carry  Ip2  CLD NVBDIZC  CLear Decimal  Ip2  CLU NVBDIZC  CLear OVERFLOW  Ip2  SEC NVBDIZC  SET Carry  Ip2  SET NVBDIZC  SET Decimal  Ip2  SET NVBDIZC  SET Decimal  Ip2  SET NVBDIZC  SET NVBDIZC  SET Decimal  Ip2  SET NVBDIZC	CPY NUBDIZC ComPare Y register Im2 Z3 Ab4  TRE NUBDIZC Test and Reset Bits Z5 Ab6  TSE NUBDIZC Test and Set Bits Z5 Ab6  RMB NUBDIZC Reset Memory Bit Z5 Ab6  SMB NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Set Memory Bit Z5 Ab6  Flow  JMP NUBDIZC Jump NUBDIZC Jump NUBDIZC Jump NUBDIZC Jump NUBDIZC Refurn from Subroutine Ab6  RTS NUBDIZC Refurn from Interrupt Ip6  RTI NUBDIZC Refurn from Interrupt Ip6  RTI NUBDIZC	Stack  PHA NUBDIZC Push Accumulator  Ip3  PHX NVBDIZC Push X register  Ip3  PHY NVBDIZC Push Y register  Ip3  PHP NUBDIZC Push Processor status  Ip3  PLA NVBDIZC Pull Accumulator  Ip4  PLP NVBDIZC Pull Processor status  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull X register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Pull Y register  Ip4  PLX NVBDIZC Transfer X to Stack  Ip2	DEY NUBDIZC DECREMENT Y  Ip2  INC NUBDIZC INCrement Memory

Flags (Right Upper corner): N=Negative, V=Overflow, B=Break, D=Decimal, I=Interrupt Disable, Z=Zero, C=Carry. Green flags are affected by the instruction.

Timing: The green number next to each mode is the number of CPU cycles for that addressing mode. A "+" means an extra cycle may be used (e.g. on page crossing).