

65C02 INSTRUCTIONS

Modes		LSR		NUBDIZC		Transfer	
Ip	Implied	Logical Shift Right		Branch on Equal		TAX	
Ac	Accumulator	Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		R ²		Transfer A to X	
Im	Immediate	ROL		NUBDIZC		Ip ²	
Z	ZeroPage	ROtate Left		BNE		TAY	
Zx	ZeroPage,X	Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		Branch on Not Equal		Transfer A to Y	
Zy	ZeroPage,Y	ROR		R ²		Ip ²	
Ab	Absolute	ROtate Right		BCC		TXA	
Ax	Absolute,X	Ac ² Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺		Branch on Carry Clear		Transfer X to A	
Ay	Absolute,Y	AND		R ²		Ip ²	
R	Relative	bitwise AND with accumulator		BCS		TYA	
Ix	Ind, zp X	Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Branch on Carry Set		Transfer Y to A	
IAx	Ind, abs X	Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		R ²		Ip ²	
Iy	Ind, zp Y	ORA		BUC		Calc	
Iz	Ind, zp	bitwise OR with Accumulator		Branch on oVerflow Clear		INA	
Ia	Ind, abs	Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		R ²		INcrement Accumulator	
		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		BUS		Ac ²	
Load & Store		EOR		Branch on oVerflow Set		INX	
LDA	NUBDIZC	bitwise Exclusive OR		R ²		INcrement X	
Load Accumulator		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		BMT		Ip ²	
Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		Branch on MInus		INY	
Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		BIT		R ²		INcrement Y	
LDX	NUBDIZC	test BITs		BPL		Ip ²	
Load X register		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Branch on PLus		DEA	
Im ² Z ³ Zy ⁴ Ab ⁴ Ay ⁴⁺		CMP		R ²		DEcrement Accumulator	
LDY	NUBDIZC	CoMPare accumulator		BBR<0-7>		Ac ²	
Load Y register		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺		Branch on Bit Reset		DEX	
Im ² Z ³ Zx ⁴ Ab ⁴ Ay ⁴⁺		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵		R ²		DEcrement X	
STA	NUBDIZC	CPX		BBs<0-7>		Ip ²	
Store Accumulator		CoMPare X register		R ²		DEV	
Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺ Ay ⁵⁺		Im ² Z ³ Ab ⁴		Stack		DEcrement Y	
Ix ⁶ Iy ⁶ Iz ⁵		CPY		PHA		Ip ²	
STX	NUBDIZC	CoMPare Y register		Push Accumulator		INC	
Store X register		Im ² Z ³ Ab ⁴		Ip ³		INCrement memory	
Z ³ Zy ⁴ Ab ⁴		TRB		PHX		Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺	
STY	NUBDIZC	Test and Reset Bits		Push X register		DEC	
Store Y register		Z ⁵ Ab ⁶		Ip ³		DEcrement memory	
Z ³ Zx ⁴ Ab ⁴		TSB		PHY		Z ⁵ Zx ⁶ Ab ⁶ Ax ⁷⁺	
STZ	NUBDIZC	Test and Set Bits		Push Y register		ADC	
Store Zero		Z ⁵ Ab ⁶		Ip ³		ADD with Carry	
Z ³ Zx ⁴ Ab ⁴ Ax ⁵⁺		RMB		PHP		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺	
		Reset Memory Bit		Push Processor status		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵	
		Z ⁵ Ab ⁶		Ip ³		SBC	
		SMB		PLA		SuBtract with Carry	
		Set Memory Bit		Pull Accumulator		Im ² Z ³ Zx ⁴ Ab ⁴ Ax ⁴⁺	
		Z ⁵ Ab ⁶		Ip ⁴		Ay ⁴⁺ Ix ⁶ Iy ⁵ Iz ⁵	
		Flow		PLP		Misc	
		JMP		Pull Processor status		BRK	
		JuMP		Ip ⁴		BReaK	
		Ab ³ Ia ⁵⁺ IAx ⁶⁺		PLX		Ip ⁷	
		JSR		Pull X register		NOP	
		Jump to SubRoutine		Ip ⁴		No OPeration	
		Ab ⁶		PLY		Ip ²	
		RTS		Pull Y register		STP	
		ReTurn from Subroutine		Ip ⁴		SToP	
		Ip ⁶		TXS		Ip ³	
		RTI		Transfer X to Stack			
		ReTurn from Interrupt		Ip ²			
		Ip ⁶		TSX			
		BRA		Transfer Stack to X			
		BRanch Always		Ip ²			
		R ³					
		BEQ					
		Branch on Equal					
		R ²					
		BNE					
		Branch on Not Equal					
		R ²					
		BCC					
		Branch on Carry Clear					
		R ²					
		BCS					
		Branch on Carry Set					
		R ²					
		BUC					
		Branch on oVerflow Clear					
		R ²					
		BUS					
		Branch on oVerflow Set					
		R ²					
		BMT					
		Branch on MInus					
		R ²					
		BPL					
		Branch on PLus					
		R ²					
		BBR<0-7>					
		Branch on Bit Reset					
		R ²					
		BBs<0-7>					
		Branch on Bit Set					
		R ²					
		Stack					
		PHA					
		Push Accumulator					
		Ip ³					
		PHX					
		Push X register					
		Ip ³					
		PHY					
		Push Y register					
		Ip ³					
		PHP					
		Push Processor status					
		Ip ³					
		PLA					
		Pull Accumulator					
		Ip ⁴					
		PLP					
		Pull Processor status					
		Ip ⁴					
		PLX					
		Pull X register					
		Ip ⁴					
		PLY					
		Pull Y register					
		Ip ⁴					
		TXS					
		Transfer X to Stack					
		Ip ²					
		TSX					
		Transfer Stack to X					
		Ip ²					
		Wait					
		Wait for Interrupt					
		Ip ³					