Laboratory Exercise #3

Structural Modeling of Combinational Circuits

Name: _____ **Group:** _____

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Intended Learning Outcomes:

- Create design entry of a combinational circuit using structural modeling in Verilog HDL code
- Synthesize the Verilog HDL design entry
- Simulate the designed circuit using a testbench file

Supplement:

This exercise requires a basic understanding of the Intel Quartus Prime design flow with ModelSim functional verification, as detailed in Units 1-2 and Laboratory Exercises #1-2. It is also expected that Laboratory Exercise #2 has already been completed before performing this exercise.

Instructions:

Perform this hands-on laboratory exercise after attending/watching the onsite/online lecture for Unit 3. This activity is intended to be done individually.

Exercise 3A: 2x4 Decoder

Under a new project, create a Verilog HDL description of a ***2-to-line decoder with active-high enable (E) signal*** using **gate primitives** and **structural modeling**. Use the entity diagram and truth table below for reference. For structural modeling, derive the Boolean functions and draw the logic diagram of the circuit. Synthesize the design. *(In the laboratory report, don't forget to include the solutions in obtaining the Boolean functions/logic diagram.)*

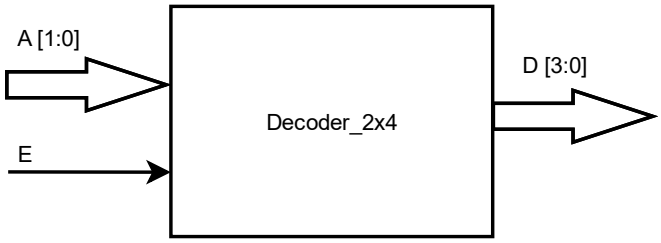

Figure 1.Entity Diagram of 2x4 Decoder

Truth Table:

Inputs		Output
E	**A**	**D**
0	xx	0000
1	00	0001
1	01	0010
1	10	0100
1	11	1000

After the design synthesis, create a simulation (testbench) file to the project. Simulate and verify the results. Show both a simulation log (standard output) and simulation waveform (timing diagram) in the laboratory report.

Test Cases for Simulation: Include ALL possible input combinations for **A** and vary the **E** values.

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	

Exercise 3B: 4-Bit Adder

Using the **full adder** design in Exercise 2B (from Lab Exercise #2), create a **structural description** of a ***4-bit adder***. Use the entity and structural diagrams below for reference. Synthesize the design.

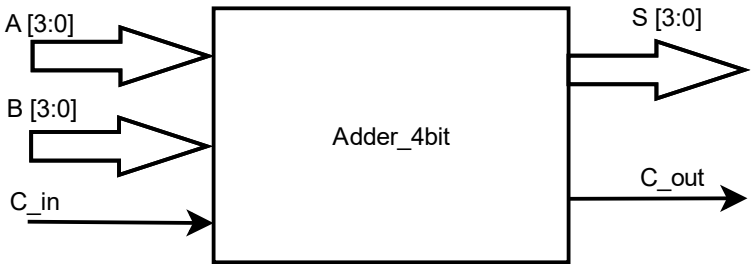

Figure 2. Entity Diagram of a 4-Bit Adder

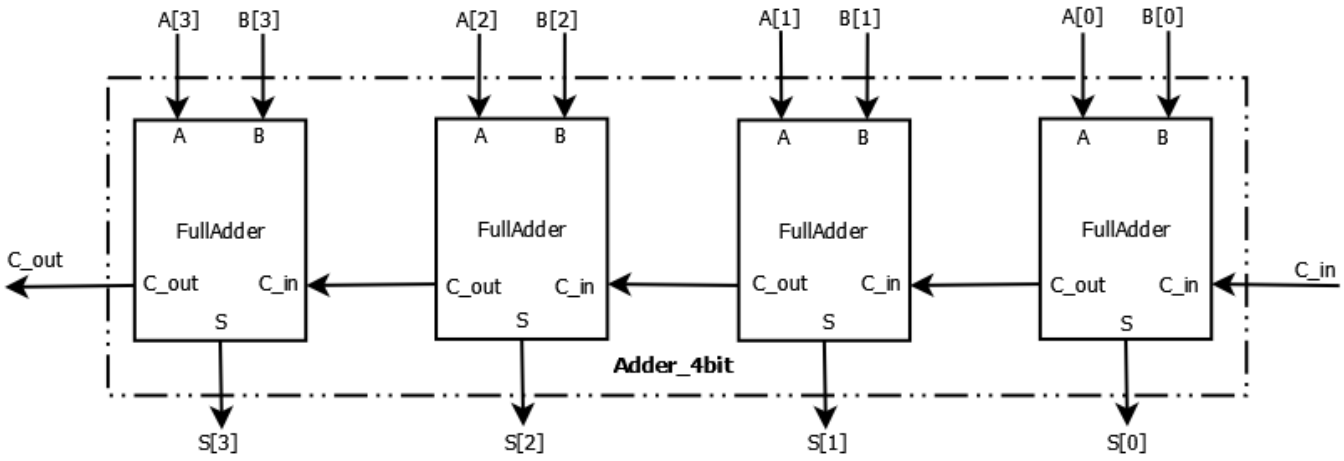

Figure 3. Structural Diagram of a 4-Bit Adder

After the design synthesis, create a simulation (testbench) file to the project. Simulate and verify the results. Show both a simulation log (standard output) and simulation waveform (timing diagram) in the laboratory report.

For easier verification of the results, change the radix of all the signals to **Unsigned**.

Test Cases for Simulation: Include AT LEAST 8 possible input combinations for **A** and **B**, and vary **C_in** values.

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	

CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	

For the laboratory report (LR #3), include the following items:

- **Exercise 3A: 2x4 Decoder**
  - Boolean function, logic diagram, and the respective solutions
  - Label the logic diagram that corresponds to its Verilog design entry *(names of I/O ports, internal signals, etc.)*
  - Proof of successful design synthesis *(screenshot showing 0 errors)*
  - Schematic diagram of synthesized circuit using RTL Viewer
  - Proof of successful simulation results *(screenshots of simulation results with annotations or discussion of results)*
- **Exercise 3B: 4-bit Adder**
  - Internal block diagram with appropriate labels that corresponds to its Verilog design entry *(names of I/O ports, internal signals, etc.)*
  - Proof of successful design synthesis *(screenshot showing 0 errors)*
  - Schematic diagram of synthesized circuit using RTL Viewer
  - Proof of successful simulation results *(screenshots of simulation results with annotations or discussion of results)*
- All Verilog files (.v) must be submitted along with LR #3