荧光显示屏产品规格书
SPECIFICATION OF VACUUM FLUORESCENT DISPLAY

	Date	Description
1	2014.03.20	ORIGINAL

Customer's Approval

Designed by	Checked and Approved by
余春桥 14.3.20	陶光彦 14.3.20

control No.	QG/ZBOE-VFD 030.07.3-05
Spec. No.	SPC14.03.01-01
MODEL	

用途 Application	机顶盒 STB
显示颜色 Color Of Illumination	绿色 Green X=0.24 Y=0.41

概要 Features
12Grid X 37Anode 1 Colors Cadmium Free Phosphor Lead Free solder

外形尺寸 Outer Dimensions	长 Panel Length	95.0 $^{+0.8}_{-0.5}$	mm
	宽 Panel Height	20.5 $^{+0.7}_{-0.5}$	mm
	厚 Panel Thickness	6.1±0.5	mm
引出端子 Lead	端子间距 Lead Pitch	2.0	mm
	端子引出形式 Lead Out	单列折弯	

极限工作条件 Absolute Maximum Condition

项目 Item	符号Symbol	引出端子符号Terminals	变动范围 Ratings	单位Unit
灯丝电压 Filament Voltage	Ef	F+,F−	3.1~4.7	Vdc
逻辑供给电压 Logic Supply Voltage	V_{DD}	V_{DD}	−0.3~+6.0	Vdc
驱动供给电压 Driver Supply Voltage	V_{DISP}	V_{DISP}	−0.3~40	Vdc
逻辑输入电压 Logic Input Voltage	V_{IN}	CS,CP,DA,RESET	−0.3~V_{DD}+0.3	Vdc
使用温度 Operating Temperature	Top	————	−20 ~ +70	℃
储存温度 Storage Temperature	Tstg	————	−55 ~ +80	℃

推荐工作条件 Recommended Operating Condition

项目 Item	符号 Symbol	条件 Condition	最小值 Min	推荐值 TYP.	最大值 Max	单位 Unit
灯丝电压 Filament Voltage	Ef	————	3.51	3.9	4.29	Vdc
截止电压 Cut−off Voltage	Ek	————	2.0	——	3.0	Vdc
逻辑供给电压 Logic Supply Voltage	V_{DD}	————	4.5	5.0	5.5	Vdc
驱动供给电压 Driver Supply Voltage	V_{DISP}	————	30.0	33.0	36.0	Vdc
逻辑高电平输入 Hi−level Logic Input	V_{IH}	CS,CP,DA,RESET	V_{DD}×0.8	——	——	Vdc
逻辑低电平输入 Lo−level Logic Input	V_{IL}	CS,CP,DA,RESET	——	——	V_{DD}×0.2	Vdc
时钟频率 CP Frequency	fc	————	——	——	0.5	MHz
振荡器频率 Oscillation Frequency	fosc	V_{DD}=5.0V R = 33 kΩ	——	1.1	——	MHz
扫描频率 Frame Frequency	f_{FR}		——	269	——	Hz
交流特性 AC Characteristics		见时序图 See Timing Chart				

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电气特性 Electrical Chardcteristics

项 目 Item	符 号 Symbol	测试条件 Test Condition	最小值 Min	典型值 Typical	最大值 Max	单位 Unit
灯丝电流 Filament Current	If	Ef=3.9 Vdc	99	110	121	mAdc
逻辑供给电流 Logic Supply Current	I_{DD}	V_{DD} No Load V_{DD}=5.0V, fosc=1.1MHZ	—	—	5	mA
驱动供给电流(1) Driver Supply Current(1)	$I_{DISP1(AVG)}$	V_{DISP} No Load fosc= 1.1 MHz; All output lights ON Typ:Tj=25℃ Max:Tj=85℃	—	10.0	20.0	mA
	$I_{DISP1(PEAK)}$		—	12.0	24.0	mA
	I_{DISP2}	All output lights OFF Typ:Tj=25℃ Max:Tj=85℃	—	1.0	15.0	μA
驱动供给电流(2) Driver Supply Current(2)	I_{DD}	V_{DD} No Load Stand-by mode Typ:Tj=25℃ Max:Tj=85℃	—	1.0	1.0	μA
	I_{DISP}	V_{DISP}	—	1.0	1.0	μA
高电平输入电流 Hi-level Input Current	I_{IH}	$V_{IN}=V_{DD}$ CS,CP,DA RESET	-1.0	—	1.0	μA
低电平输入电流 Lo-level Input Current	I_{IL}	V_{IN}=0 V CS,CP,DA RESET	-1.0	—	1.0	μA
亮度 Luminance	L(G)	Ef=3.9 Vdc V_{DISP}=33.0 Vdc Ek=2.0Vdc Dimming=240/255 (Duty=1/14.9)	500 (146)	1000 (292)	—	cd/m² (fl)
	L(R)		—	—	—	cd/m² (fl)
	—		—	—	—	cd/m² (fl)
位间亮度比 Luminance Ratio	Lmin/Lmax	Filament Level Ef V_H Ek	50	—	—	%

功能表 Function Table

功 能 Function	符 号 Symbol	输入/输出 Input/Output	描 述 Description
移位寄存器时钟信号 Shift clock input	CP	Input	Serial data is shifted on the rising edge of CP
串行数据输入 Serial Data Input	DA	Input	Serial data input (positive logic).Input from LSB
片选信号 Chip select input	CS	Input	Serial data transfer is disabled when CS pin is "H" level
复位输入 Reset Input	RESET	Input	"Low" initializes all the functions
驱动供给电源 Power Supply To VFD	V_{DISP}	—	Power Supply Pin for Drive Circuit
逻辑供给电源 Power Supply To Logic	V_{DD}	—	Power Supply Pin for Logic Circuit
电源地 Ground	LGND,PGND	—	Ground of Circuit
振荡器输入端 oscillator input	OSC	I/O	Pin for self-oscillation
测试端 Test mode control pin	TSA	—	Factory test pin, leave it open
测试端 Test mode control pin	TSB	—	Connect it with L-GND

注：驱动方式 动态
Drive mode:Dynamic state

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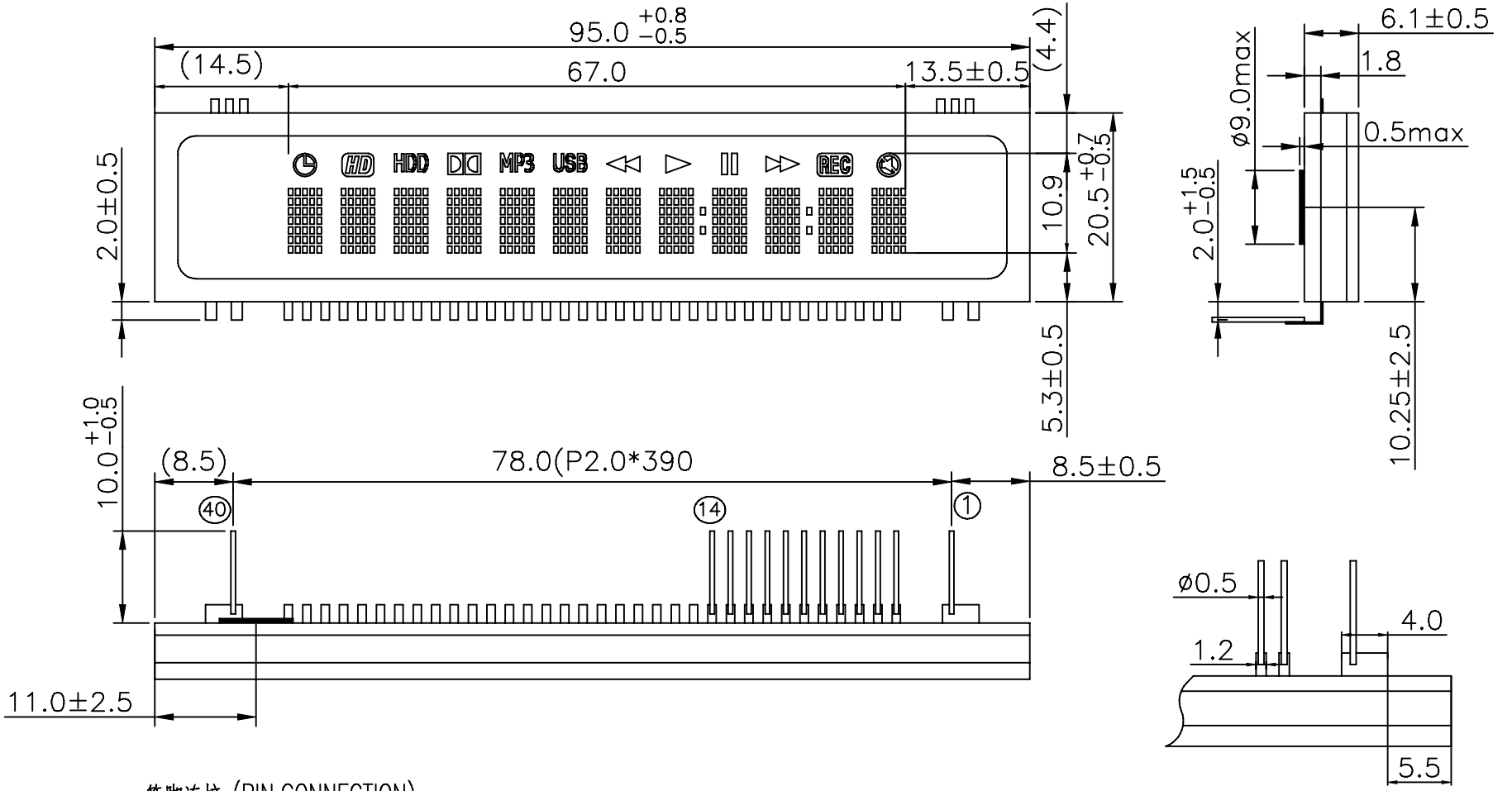
附图1：外形图 Outline Drawing(Unit:mm)



管脚连接 (PIN CONNECTION)

端子序号 (PIN NO.)	40	39	38	37～15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
连接 (CONNECTION)	F+	NP	NP	NC	TSB	TSA	DA	CP	CS	RESET	OSC	VDD	VDISP	PGND	LGND	NP	NP	F−

注 Note：F: 灯丝 (Filament) NP: 无引出脚 (No pin) NC: 无连接 (No Connection)

LEAD FREE SOLDER

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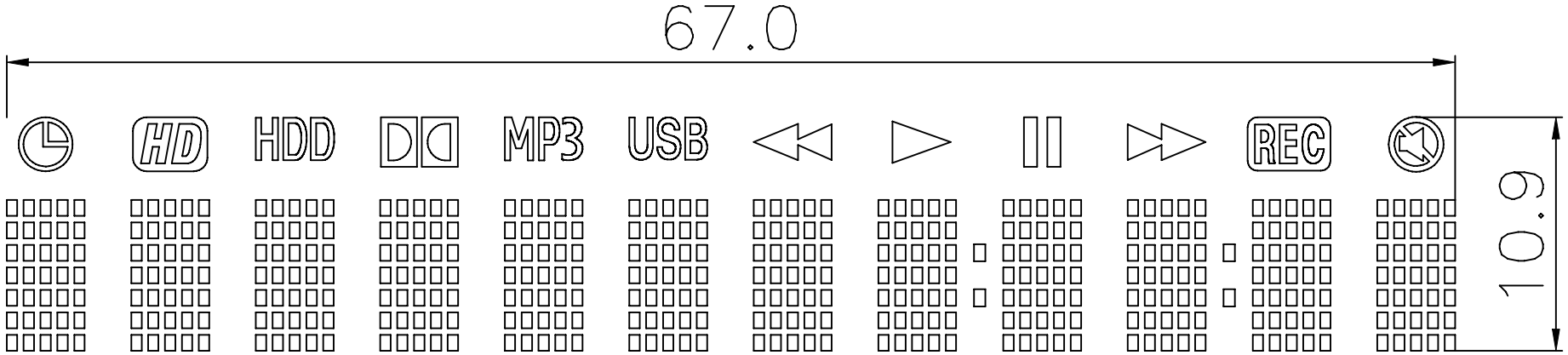
附图2：显示内容 Display Pattern (Unit:mm)



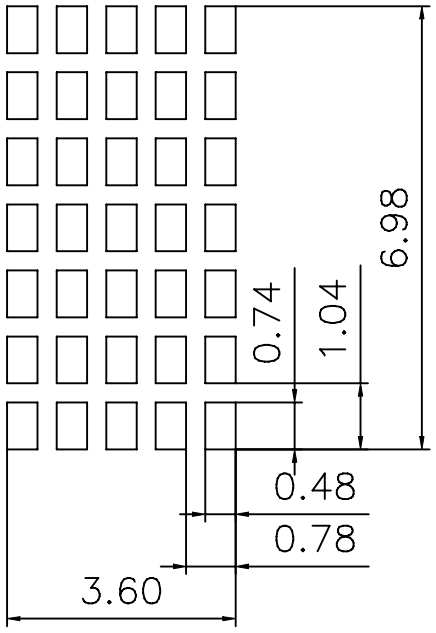
显示颜色 Color of Illumination:

绿色 Green (X=0.24, Y=0.41): 全部 All

Cadmium Free Phosphor used

阴体字 Negative pattern

HD REC



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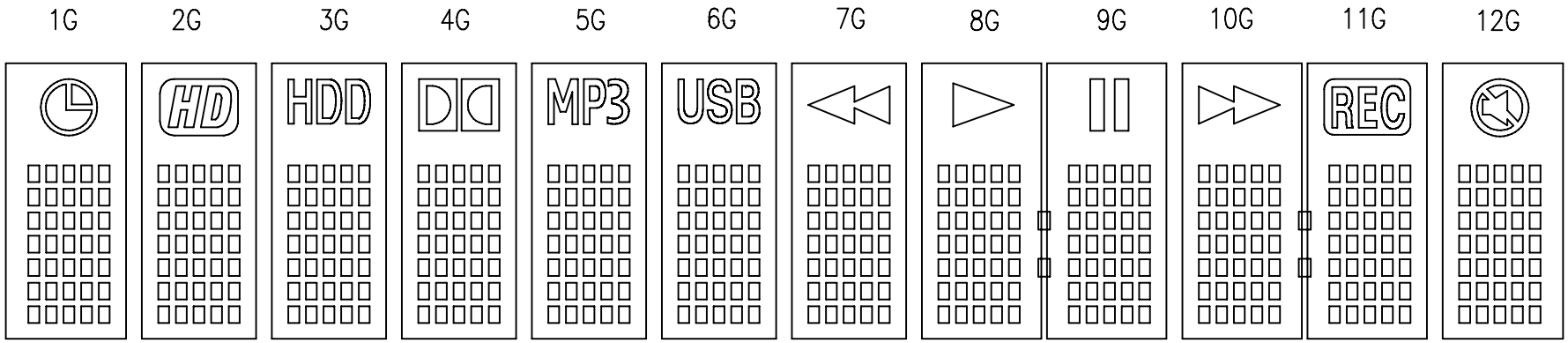
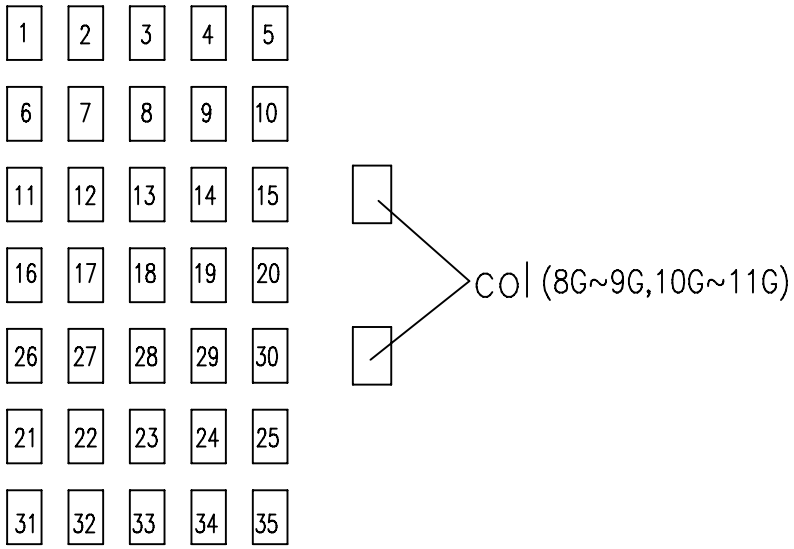
附图3: 栅网分割 Grid Assignment





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附图4－1：IC引脚连接Connection of IC pin

	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G
SEGA1	1	1	1	1	1	1	1	1	1	1	1	1
SEGA2	2	2	2	2	2	2	2	2	2	2	2	2
SEGA3	3	3	3	3	3	3	3	3	3	3	3	3
SEGA4	4	4	4	4	4	4	4	4	4	4	4	4
SEGA5	5	5	5	5	5	5	5	5	5	5	5	5
SEGA6	6	6	6	6	6	6	6	6	6	6	6	6
SEGA7	7	7	7	7	7	7	7	7	7	7	7	7
SEGA8	8	8	8	8	8	8	8	8	8	8	8	8
SEGA9	9	9	9	9	9	9	9	9	9	9	9	9
SEGA10	10	10	10	10	10	10	10	10	10	10	10	10
SEGA11	11	11	11	11	11	11	11	11	11	11	11	11
SEGA12	12	12	12	12	12	12	12	12	12	12	12	12
SEGA13	13	13	13	13	13	13	13	13	13	13	13	13
SEGA14	14	14	14	14	14	14	14	14	14	14	14	14
SEGA15	15	15	15	15	15	15	15	15	15	15	15	15
SEGA16	16	16	16	16	16	16	16	16	16	16	16	16
SEGA17	17	17	17	17	17	17	17	17	17	17	17	17
SEGA18	18	18	18	18	18	18	18	18	18	18	18	18
SEGA19	19	19	19	19	19	19	19	19	19	19	19	19
SEGA20	20	20	20	20	20	20	20	20	20	20	20	20
SEGA21	21	21	21	21	21	21	21	21	21	21	21	21
SEGA22	22	22	22	22	22	22	22	22	22	22	22	22
SEGA23	23	23	23	23	23	23	23	23	23	23	23	23
SEGA24	24	24	24	24	24	24	24	24	24	24	24	24
SEGA25	25	25	25	25	25	25	25	25	25	25	25	25
SEGA26	26	26	26	26	26	26	26	26	26	26	26	26
SEGA27	27	27	27	27	27	27	27	27	27	27	27	27
SEGA28	28	28	28	28	28	28	28	28	28	28	28	28
SEGA29	29	29	29	29	29	29	29	29	29	29	29	29
SEGA30	30	30	30	30	30	30	30	30	30	30	30	30
SEGA31	31	31	31	31	31	31	31	31	31	31	31	31
SEGA32	32	32	32	32	32	32	32	32	32	32	32	32
SEGA33	33	33	33	33	33	33	33	33	33	33	33	33
SEGA34	34	34	34	34	34	34	34	34	34	34	34	34
SEGA35	35	35	35	35	35	35	35	35	35	35	35	35
AD1								col		col		
AD2		HD	HDD	DIC	MP3	USB					REC	

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附图 4-2：时序图Timing Chart

	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G
SEGA1	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA2	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA3	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA4	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA5	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA6	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA7	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA8	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA9	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA10	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA11	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA12	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA13	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA14	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA15	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA16	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA17	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA18	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA19	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA20	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA21	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA22	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA23	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA24	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA25	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA26	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA27	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA28	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA29	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA30	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA31	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA32	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA33	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA34	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
SEGA35	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
AD1								T17		T18		
AD2	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12

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附图 4-3：时序图Timing Chart

Grid Scan Timing	DCRAM/ADRAM/ GSRAM address	ON/OFF timing of Grid												Codes selection	
		1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G	DCRAM	ADRAM
T1	00H	H	L	L	L	L	L	L	L	L	L	L	L	NOTE1	NOTE2
T2	01H	L	H	L	L	L	L	L	L	L	L	L	L	NOTE1	NOTE2
T3	02H	L	L	H	L	L	L	L	L	L	L	L	L	NOTE1	NOTE2
T4	03H	L	L	L	H	L	L	L	L	L	L	L	L	NOTE1	NOTE2
T5	04H	L	L	L	L	H	L	L	L	L	L	L	L	NOTE1	NOTE2
T6	05H	L	L	L	L	L	H	L	L	L	L	L	L	NOTE1	NOTE2
T7	06H	L	L	L	L	L	L	H	L	L	L	L	L	NOTE1	NOTE2
T8	07H	L	L	L	L	L	L	L	H	L	L	L	L	NOTE1	NOTE2
T9	08H	L	L	L	L	L	L	L	L	H	L	L	L	NOTE1	NOTE2
T10	09H	L	L	L	L	L	L	L	L	L	H	L	L	NOTE1	NOTE2
T11	0AH	L	L	L	L	L	L	L	L	L	L	H	L	NOTE1	NOTE2
T12	0BH	L	L	L	L	L	L	L	L	L	L	L	H	NOTE1	NOTE2
T13	0CH	Don't use it on this type												*	*
T14	0DH													*	*
T15	0EH													*	*
T16	0FH													*	*
T17	10H	L	L	L	L	L	L	L	H	H	L	L	L	20H	NOTE2
T18	11H	L	L	L	L	L	L	L	L	L	H	H	L	20H	NOTE2
T19	12H	Don't use it on this type												*	*
T20	13H													*	*
T21	14H													*	*
T22	15H													*	*
T23	16H													*	*
T24	17H													*	*

NOTE1: Set random code by CGROM codes

NOTE2: Set the standard pattern by P6-1

*: Don't Care

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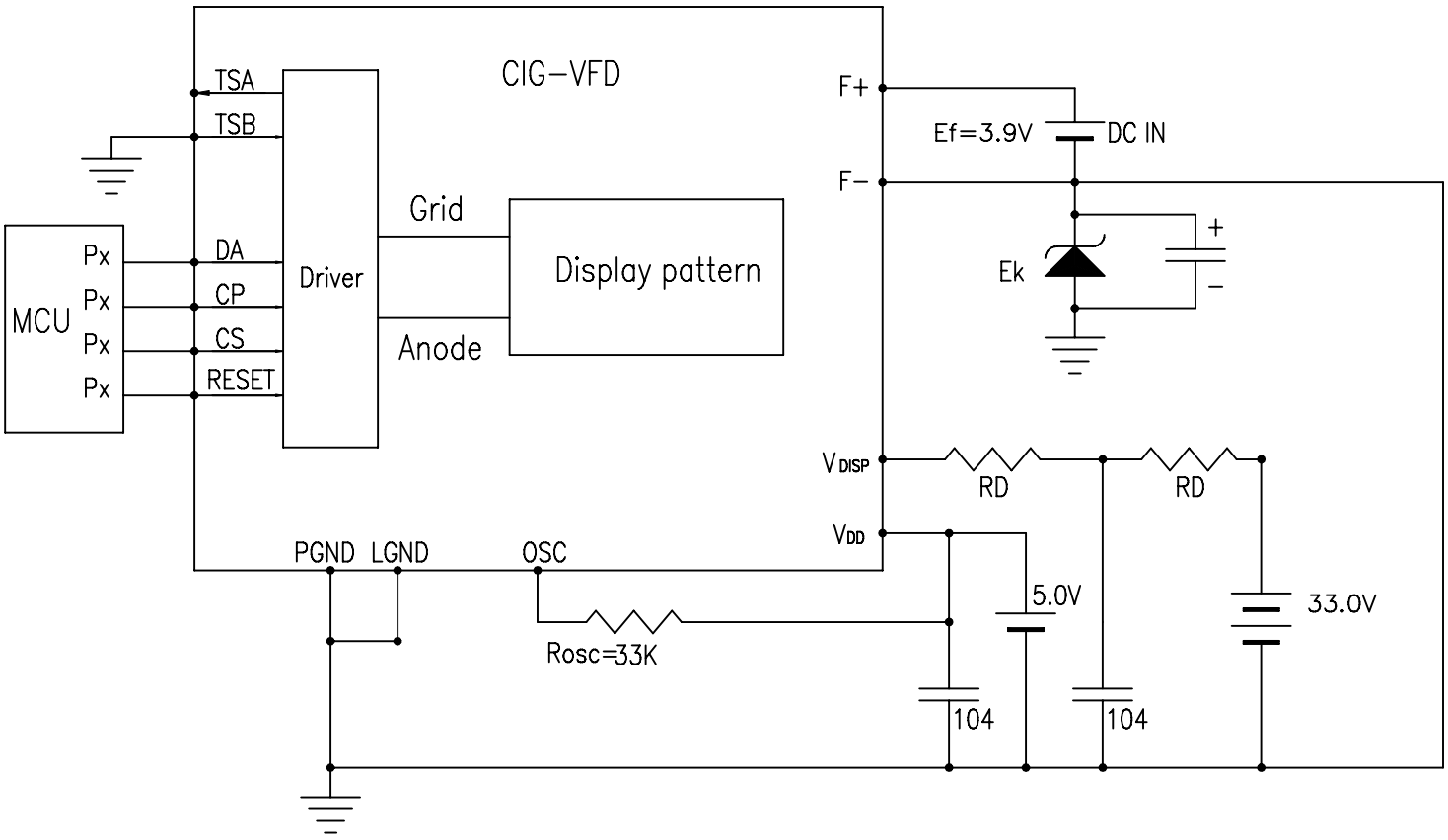
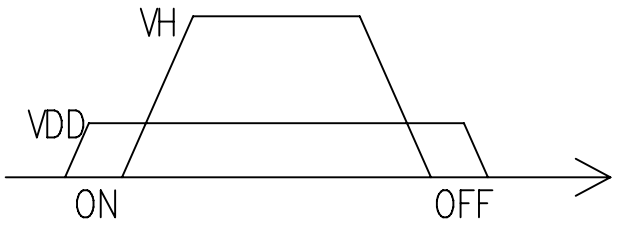
Block Diagram and Drive Circuit



注1)： RD=10Ω为限流电路,104 电容为电源VDD和VDISP的退耦电容。

Note 1) :The series resister RD =22Ω is resister for limitation of over current.
The capacitors for noise filter to the VH and VDD.

Power supply sequence



VDD should be applied and higher than 5.0V when applying VDISP.
VDD and VH should be on at the same time, or VDISP should be on after VDD is on.
VDD and VH should be off at the same time, or VDD should be off after VDISP is off.

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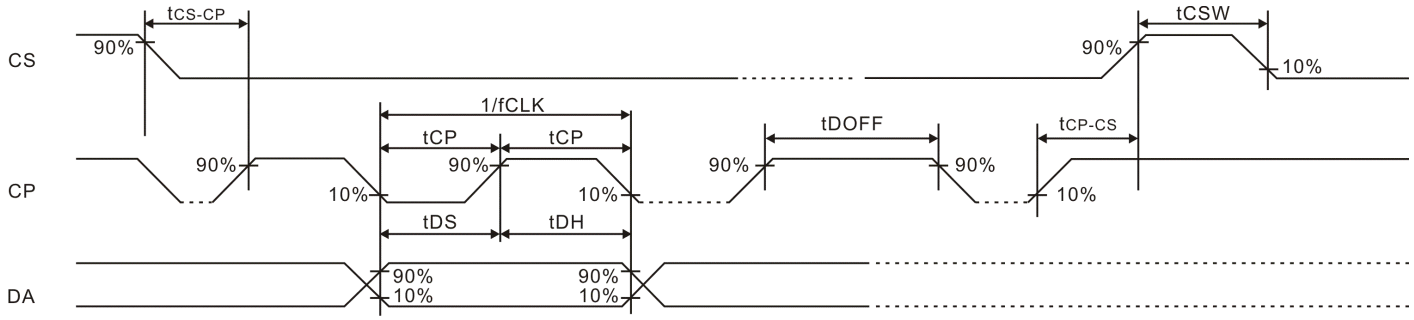
1. TIMING CHARACTERISTICS

(Unless otherwise specified, Tj=-20℃~+85℃, VDISP=50V, LGND=PGND=0V)

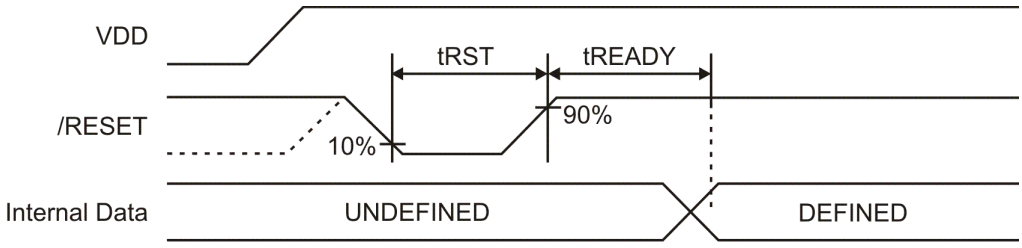
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CP Frequency	fCLK	–	-	-	0.5	MHz
CP Pulse Width	tcpw	–	700	-	-	ns
Time needed between CS and CP	tcs-cp	–	1000	-	-	ns
Data Setup Time	tDS	–	300	-	-	ns
Data Hold Time	tDH	–	300	-	-	ns
Time to Process Data	tDOFF	oscillating	2	-	-	μs
Time need between CP and CS	tcp-cs	–	1000	-	-	ns
Time to wait CS	tcsw	oscillating	1000	-	-	ns
Output Data Delay Time	tODD	–	80	-	-	ns
Reset Pulse Width	tRST	–	15	-	-	μs
After Reset Ready Time	tREADY	–	2	-	-	ms

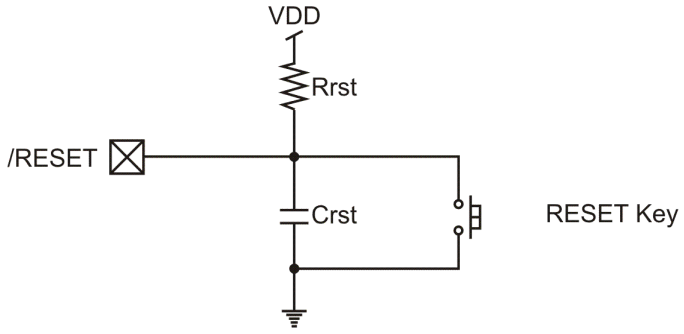
1.1 WAVEFORMS

WRITING WAVEFORM



RESTE(/RESET) CONTROL WAVEFORM





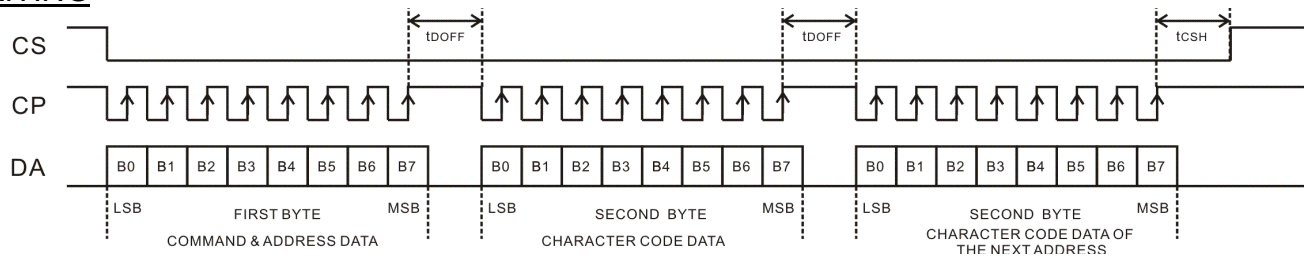
Power-On Reset Circuit

2. FUNCTION DESCRIPTION

2.1 DATA TRANSFER

The Display Control Command and the data are written by an 8-bit serial data transfer. Please refer to the diagram below.

WRITING



Note: When data is written into the RAM (DCRAM, ADRAM, CGRAM, URAM) in a continuous manner, the address are automatically incremented. Therefore it is not necessary to specify the first byte of the 2nd and later bytes when writing the RAM data.

When the CS pin is set to "LOW" Level, data transfer operation is enabled. 8-bit of data are sequentially inputted into the DA Pin (LSB first). The shift register reads the data at the rising edge of the shift clock. The data is then inputted into the CP Pin. The internal load signals are automatically generated and the data is written to each register and RAM. Thus, it is not necessary to input load signals externally.

When the CS Pin is set to "HIGH" Level, the data transfer operation is disabled. The data input when the CS Pin changes from "HIGH" to "LOW" be recognized in 8-bit units.

2.2 INSTRUCTIONS TABLE

The following are the list of commands issued by IC. When data is written into the RAM in a continuous manner, the addresses are automatically incremented internally. It is therefore not necessary to specify the first byte.

Instruction	MSB			First Byte				LSB	MSB			Second Byte				LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
DCRAM Data Write	0	0	1	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
CGRAM Data Write	0	1	0	*	*	Y2	Y1	Y0	*	D30	D25	D20	D15	D10	D5	D0	2nd Byte
									*	D31	D26	D21	D16	D11	D6	D1	3rd Byte
									*	D32	D27	D22	D17	D12	D7	D2	4th Byte
									*	D33	D28	D23	D18	D13	D8	D3	5th Byte
									*	D34	D29	D24	D19	D14	D9	D4	6th Byte
ADRAM Control Set	0	1	1	X4	X3	X2	X1	X0	*	*	*	*	E3	E2	E1	E0	
URAM Control Set	1	0	0	*	*	U2	U1	U0	G8	G7	G6	G5	G4	G3	G2	1G	
									G16	G15	G14	G13	G12	G11	G10	G9	
Number of Digit Set	1	1	1	0	0	0	*	*	UV	F6	F5	F4	F3	F2	F1	F0	
Dimming Set	1	1	1	0	0	1	*	*	H7	H6	H5	H4	H3	H2	H1	H0	
Display Light On/Off	1	1	1	0	1	0	LS	HS	*	*	*	*	*	*	*	*	
Standby Mode	1	1	1	0	1	1	*	ST	*	*	*	*	*	*	*	*	
Test Mode	1	1	1	1	1	1	*	*	L7	L6	L5	L4	L3	L2	L1	L0	

Notes:

1. *=Not Relevant.
2. Xn=Duty Timing (Digit) Address Set, n=0 to 4.
3. Cn=CGRAM/CGROM Character Code Bit, n=0 to 7.
4. Yn=CGRAM Address Bit, n=0 to 2.
5. Dn=CGRAM Character Code Setting, n=0 to 34.
6. En=Segment Pin Setting, n=0 to 3.
7. Un=URAM Address Set, n=0 to 2.
8. Gn=Grid ON/OFF Setting, n=1 to 16.
9. Fn=Number of Digits Set, n=0 to 6.
10. UV="1": Universal Function Enable.
    UV="0": Universal Function Disable.
11. Hn=Dimming Quantity Setting, n=0 to 7.
12. HS="1": All Output (Anode, Segment) Data="H".
13. HS="0": Normal Mode.
14. LS="1": All Output (Anode, Segment) Data="L".
    LS="0": Normal Mode.
15. ST="1": Stand-by Mode.
    ST="0": Normal Mode.
16. Ln=Test Mode Command Setting, n=0 to 7.

2.3 DATA CONTROL RAM (DCRAM) DATA WRITE COMMAND

The DCRAM Data Write Command is used to specify the address of the DCRAM and writes the character code of the CGROM and CGRAM (C0 to C7 bits). The DCRAM consists of 5 address bits which are used to store the CGRAM & CGROM character codes. The character codes specified by the DCRAM are converted to a 5 x 7 dot matrix character pattern via the CGROM and CGRAM. The DCRAM can each store up to 24 characters. The DCRAM Data Write Command Format is shown below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	DCRAM Data Write Mode is selected and the DCRAM Address is specified. (i.e. DCRAM Address=0H)
	0	0	1	X4	X3	X2	X1	X0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	CGROM & CGRAM Character Codes are specified. (They are written into the DCRAM Address 0H)
	C7	C6	C5	C4	C3	C2	C1	C0	

During a continuous data write operation from one DCRAM Address to the next, it is not necessary to specify the DCRAM address since they are automatically incremented; however, the character code must be specified. Please refer to the information below.

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 1H.
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 2H.
	C7	C6	C5	C4	C3	C2	C1	C0	

:
:

	MSB							LSB	
2nd Byte (25th)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 17H.
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
2nd Byte (26th)	B7	B6	B5	B4	B3	B2	B1	B0	Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 0H.
	C7	C6	C5	C4	C3	C2	C1	C0	

where:
1. X4 (MSB) to X0 (LSB): DCRAM Address Bits (24 Characters).
2. C7 (MSB) to C0 (LSB): CGROM & CGRAM Character Code Bits (256 Characters).

Please refer to the table below for the Duty Timing position and DCRAM Address setting relationship.

X4	X3	X2	X1	X0	Duty Timing Position
0	0	0	0	0	T1 (1G is used)
0	0	0	0	1	T2 (2G is used)
0	0	0	1	0	T3 (3G is used)
0	0	0	1	1	T4 (4G is used)
0	0	1	0	0	T5 (5G is used)
0	0	1	0	1	T6 (6G is used)
0	0	1	1	0	T7 (7G is used)
0	0	1	1	1	T8 (8G is used)
0	1	0	0	0	T9 (9G is used)
0	1	0	0	1	T10 (10G is used)
0	1	0	1	0	T11 (11G is used)
0	1	0	1	1	T12 (12G is used)
0	1	1	0	0	T13 (13G is used)
0	1	1	0	1	T14 (14G is used)
0	1	1	1	0	T15 (15G is used)
0	1	1	1	1	T16 (16G is used)
1	0	0	0	0	T17 (Only Universal is used)
1	0	0	0	1	T18 (Only Universal is used)
1	0	0	1	0	T19 (Only Universal is used)
1	0	0	1	1	T20 (Only Universal is used)
1	0	1	0	0	T21 (Only Universal is used)
1	0	1	0	1	T22 (Only Universal is used)
1	0	1	1	0	T23 (Only Universal is used)
1	0	1	1	1	T24 (Only Universal is used)

2.4 CGRAM DATA WRITE COMMAND

The Character Generator RAM (CGRAM) Data Write Command is used to specify the CGRAM address (00H to 07H) and write the character pattern data. It consists of 3 address bits which is used to store the 5 x 7 dot matrix character patterns. The CGRAM can store up to 8 types of character patterns which may be displayed by specifying the Character Code (DCRAM Address). The CGRAM Data Write Command Format is given below.

1st Byte (1st)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	*	*	Y2	Y1	Y0

CGRAM Data Write Mode is selected and the CGRAM Address is specified (i.e. CGRAM Address=00H).

2nd Byte (2nd)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D30	D25	D20	D15	D10	D5	D0

1st Column Data is specified and rewritten into the CGRAM Address 00H.

2nd Byte (3rd)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D31	D26	D21	D16	D11	D6	D1

2nd Column Data is specified and rewritten into the CGRAM Address 00H.

2nd Byte (4th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D32	D27	D22	D17	D12	D7	D2

3rd Column Data is specified and rewritten into the CGRAM Address 00H.

2nd Byte (5th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D33	D28	D23	D18	D13	D8	D3

4th Column Data is specified and rewritten into the CGRAM Address 00H.

2nd Byte (6th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D34	D29	D24	D19	D14	D9	D4

5th Column Data is specified and rewritten into the CGRAM Address 00H.

During a continuous data write operation from one CGRAM Address to the next, it is not necessary to specify the CGRAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 6th character pattern data byte are considered as one data item, **therefore 2µs is sufficient value for parameter tDOFF between bytes**. Please refer to the information below.

2nd Byte (7th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D30	D25	D20	D15	D10	D5	D0

1st Column Data is specified and rewritten into the CGRAM Address 01H.

⋮

2nd Byte (11th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	D34	D29	D24	D19	D14	D9	D4

5th Column Data is specified and rewritten into the CGRAM Address 01H.

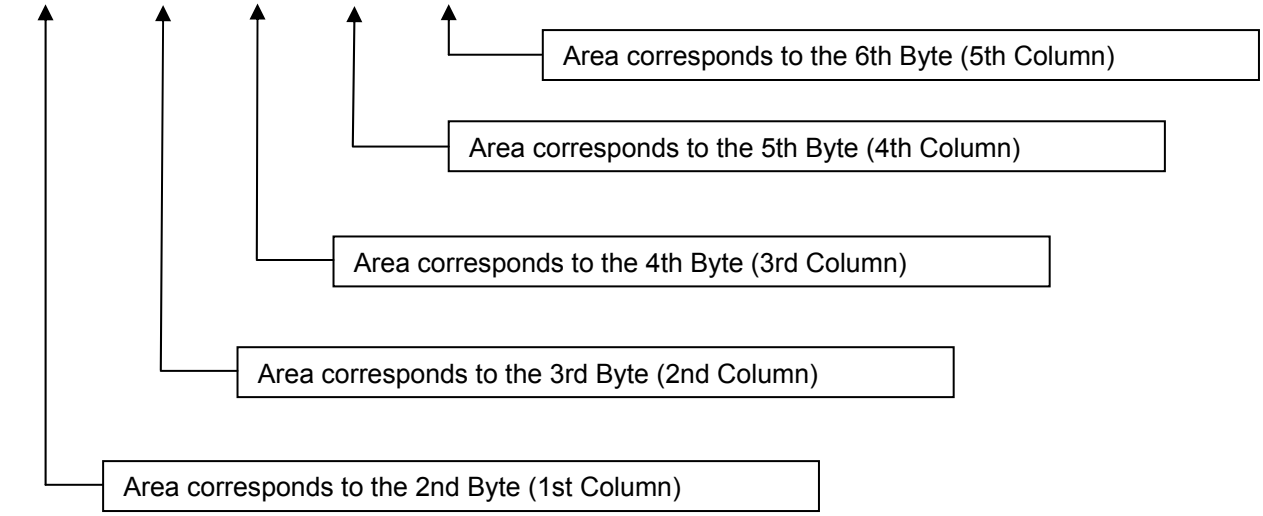
where:
1. Y2 (MSB) to Y0 (LSB): CGRAM Address Bits (8 characters).
2. D34 (MSB) to D0 (LSB): Character Pattern Data Bits (35 outputs).

Please refer below for the CGROM Address and CGRAM Address Setting relationship.

Y2	Y1	Y0	CGROM Address	HEX
0	0	0	RAM00 (00000000B)	0
0	0	1	RAM01 (00000001B)	1
0	1	0	RAM02 (00000010B)	2
0	1	1	RAM03 (00000011B)	3
1	0	0	RAM04 (00000100B)	4
1	0	1	RAM05 (00000101B)	5
1	1	0	RAM06 (00000110B)	6
1	1	1	RAM07 (00000111B)	7

The CGROM and CGRAM output area placement is given in the table below.

D0	D1	D2	D3	D4
D5	D6	D7	D8	D9
D10	D11	D12	D13	D14
D15	D16	D17	D18	D19
D20	D21	D22	D23	D24
D25	D26	D27	D28	D29
D30	D31	D32	D33	D34



The Character Generator ROM (CGROM) consists of 8 CGROM Address bits generating 5 x 7 dot matrix character patterns. It can store up to a maximum of 248 types of character patterns.

2.5 ADRAM CONTROL SET COMMAND

The Additional Data RAM (ADRAM) consists of 5 address bits used to store the symbol data. It can store up to 4 types of symbol patterns per timing. The symbol data specified by the ADRAM is directly outputted. The terminals to which the ADRAM data are outputted may be used as a cursor. The ADRAM command format is given below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	ADRAM Data Write Mode is selected and the ADRAM address is specified. (i.e. ADRAM Address = 0H)
	0	1	1	X4	X3	X2	X1	X0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 0H.
	*	*	*	*	E3	E2	E1	E0	

During a continuous data write operation from one ADRAM Address to the next, it is not necessary to specify the ADRAM address since they are automatically incremented; however, the symbol data must be specified. Please refer to the information below.

	MSB							LSB	
2nd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 1H.
	*	*	*	*	E3	E2	E1	E0	

	MSB							LSB	
2nd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 2H.
	*	*	*	*	E3	E2	E1	E0	

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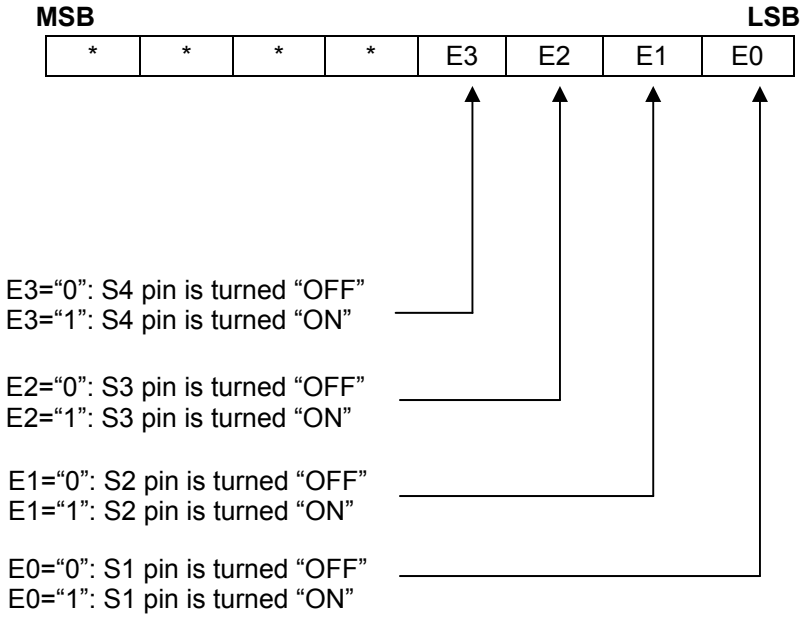
	MSB							LSB	
2nd Byte (25th)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and written into the ADRAM Address 17H.
	*	*	*	*	E3	E2	E1	E0	

	MSB							LSB	
2nd Byte (26th)	B7	B6	B5	B4	B3	B2	B1	B0	Symbol Data is specified and rewritten into the ADRAM Address 0H.
	*	*	*	*	E3	E2	E1	E0	

where:

1. X4 (MSB) to X0 (LSB): ADRAM Address Bits (24 Characters).
2. E5 (MSB) to E0 (LSB): Symbol Data Bits (Symbol Data per timing).

Please refer to below for the segment position setting relationship.



Please refer to the table below for segment (E0~E3) position and ADRAM (X0~X4) Duty Timing (Digit) Address setting relationship.

Duty Timing (Digit) Address	S4 (E3)	S3 (E2)	S2 (E1)	S1 (E0)
T1 (01100000B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T2 (01100001B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T3 (01100010B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T4 (01100011B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T5 (01100100B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T6 (01100101B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T7 (01100110B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T8 (01100111B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T9 (01101000B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T10 (01101001B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T11 (01101010B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T12 (01101011B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T13 (01101100B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T14 (01101101B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T15 (01101110B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T16 (01101111B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T17 (01110000B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T18 (01110001B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T19 (01110010B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T20 (01110011B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T21 (01110100B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T22 (01110101B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T23 (01110110B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF
T24 (01110111B)	ON/OFF	ON/OFF	ON/OFF	ON/OFF

2.6 URAM CONTROL SET COMMAND

The Universal RAM (URAM) consists of 3 address bits used to store the symbol data. It can store up to 16 types of symbol patterns per timing (T17~T24). The symbol data specified by the URAM is directly outputted. The URAM command format is given below.

1st Byte (1st)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	*	*	U2	U1	U0

Universal Control Set Mode is selected and the URAM address is specified. (i.e. URAM Address=00H)

2nd Byte (2nd)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
8G	7G	6G	5G	4G	3G	2G	1G

1st Data is specified and rewritten into the URAM Address 00H.

2nd Byte (3rd)

MSB							LSB
B7	B6	B2	B5	B4	B3	B1	B0
16G	15G	14G	13G	12G	11G	10G	9G

2nd Data is specified and rewritten into the URAM Address 00H.

During a continuous data write operation from one URAM Address to the next, it is not necessary to specify the URAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 3th character pattern data byte are considered as one data item, **therefore 2μs is sufficient value for parameter tDOFF between bytes**. Please refer to the information below.

2nd Byte (4th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
8G	7G	6G	5G	4G	3G	2G	1G

1st Column Data is specified and rewritten into the URAM Address 01H.

2nd Byte (5th)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
16G	15G	14G	13G	12G	11G	10G	9G

2nd Column Data is specified and rewritten into the URAM Address 01H.

where:
1. U2 (MSB) to U0 (LSB): URAM Address Bits.
2. 16G (MSB) to 1G (LSB): Grid Pin Setting.

Please refer to the table below for the Grid (1G ~16G) position and URAM (U0~U2) Duty Timing Address setting relationship.

Duty Timing (Digit) Address				1G	2G	……	15G	16G
Universal Name	U2	U1	U0					
T17	0	0	0	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T18	0	0	1	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T19	0	1	0	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T20	0	1	1	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T21	1	0	0	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T22	1	0	1	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T23	1	1	0	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF
T24	1	1	1	ON/OFF	ON/OFF	……	ON/OFF	ON/OFF

Notes:
1. 1G ~16G =“0”: Grid is turned “OFF”.
2. 1G ~16G =“1”: Grid is turned “ON”.

2.7 NUMBER OF DIGITS SET COMMAND

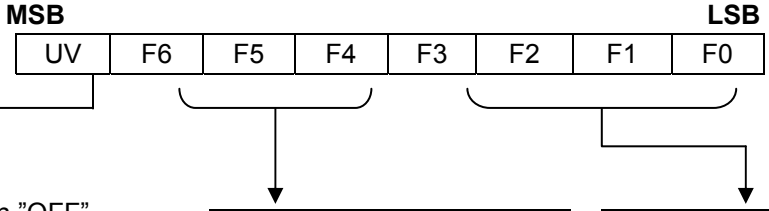
The Number of Digits Set Command is used to write the number of display digits into the display digit register. Using a 7-bit data, the Number of Digits Set Command can display 16 to 24 digits. When the power is turned ON or when the /RESET signal is inputted, the value of B7 to B4 is set to "0" and the value of B3 to B0 is set to “1”. It is advisable to always execute this command before the turning on the display. The command format is given below.

	MSB							LSB
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0
	UV	F6	F5	F4	F3	F2	F1	F0

The Number of Digits Set Mode is selected and the number of digit value is specified, Universal Function set to ON/OFF.

where:
1. F6 (MSB) to F0 (LSB): Display Duty Data Bits (24 stages).
2. UV (MSB): Universal Function Set.

The table below shows the relationship between the Setup Data and the Controlled Duty Timing (Digit).



UV=”0”: Universal Function ”OFF”.
Digits can set up to 16,
and disable F4~F6.
UV=”1”: Universal Function ”ON”.
Digits can set up to 24,
and enable F4~F6.

F6	F5	F4	Digits
0	0	0	T17
0	0	1	T17~T18
0	1	0	T17~T19
0	1	1	T17~T20
1	0	0	T17~T21
1	0	1	T17~T22
1	1	0	T17~T23
1	1	1	T17~T24

F3	F2	F1	F0	Digits
0	0	0	0	T1 (1G)
0	0	0	1	T1 (1G)~T2 (2G)
0	0	1	0	T1 (1G)~T3 (3G)
0	0	1	1	T1 (1G)~T4 (4G)
0	1	0	0	T1 (1G)~T5 (5G)
0	1	0	1	T1 (1G)~T6 (6G)
0	1	1	0	T1 (1G)~T7 (7G)
0	1	1	1	T1 (1G)~T8 (8G)
1	0	0	0	T1 (1G)~T9 (9G)
1	0	0	1	T1 (1G)~T10 (10G)
1	0	1	0	T1 (1G)~T11 (11G)
1	0	1	1	T1 (1G)~T12 (12G)
1	1	0	0	T1 (1G)~T13 (13G)
1	1	0	1	T1 (1G)~T14 (14G)
1	1	1	0	T1 (1G)~T15 (15G)
1	1	1	1	T1 (1G)~T16 (16G)

Output port ON/OFF setting

	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G	13G	14G	15G	16G	S1	S2	S3	S4
T1	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L				
T2	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L				
T3	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L				
T4	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L				
T5	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L				
T6	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L				
T7	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L				
T8	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L				
T9	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L				
T10	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L		**On/Off Setting by ADRAM**		
T11	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L				
T12	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L				
T13	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L				
T14	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L				
T15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L				
T16	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H				
T17	**On/Off Setting by URAM**																			
T18																				
T19																				
T20																				
T21																				
T22																				
T23																				
T24																				

Notes:
1. When not using URAM: Grid scan from T1 to T16
2. When using URAM: T17 to T24 can be set by universal command

FRAME FREQUENCY

Frame Frequency=f_{OSC} x $\frac{1}{256} \times \frac{1}{(X-Y)}$, X=1~16, Y=1~8

Where X means the digits of T1 to T16 and
Where Y means the digits of T17 to T24

2.8 DIMMING SET COMMAND (GRID, ANODE AND SEGMENT)

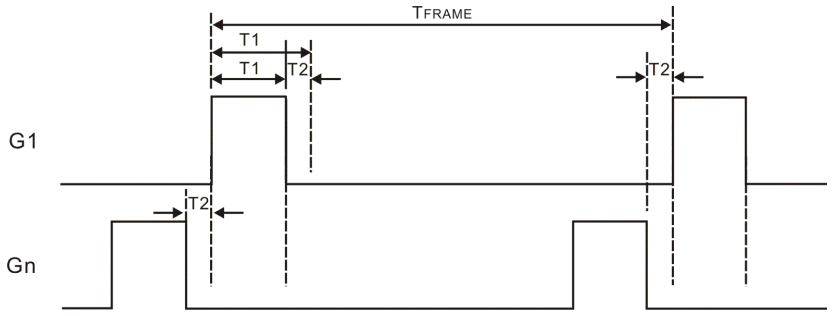
The Dimming Set Command is used to write the display duty value to the duty cycle register. Using a 8-bit data, the display duty adjusts the contrast in 240 stages. When the power is turned ON or when the /RESET signal is inputted, the duty cycle register value is set to “0”. It’s advisable to always execute this command before turning on the display, after which the desired duty value may be set. The command format is given below.

	MSB							LSB	
1st Byte	B7	B6	B5	B4	B3	B2	B1	B0	To select the dimming data set
	1	1	1	0	0	1	*	*	

	MSB							LSB	
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0	Display Duty Set Mode is selected and the duty value is specified.
	H7	H6	H5	H4	H3	H2	H1	H0	

The relationship between the Setup Data, Controlled Output Duty and the Synchronous Signal Quantity are given in the table below.

H7	H6	H5	H4	H3	H2	H1	H0	Dimming Quantity	Synchronous Signal Quantity (SYNC pin)
0	0	0	0	0	0	0	0	0/255 x T	0/255 x T
0	0	0	0	0	0	0	1	1/255 x T	1/255 x T
0	0	0	0	0	0	1	0	2/255 x T	2/255 x T
0	0	0	0	0	0	1	1	3/255 x T	3/255 x T
0	0	0	0	0	1	0	0	4/255 x T	4/255 x T
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	1	239/255 x T	239/255 x T
1	1	1	1	0	0	0	0	240/255 x T	240/255 x T
1	1	1	1	0	0	0	1	240/255 x T	240/255 x T
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	240/255 x T	240/255 x T
1	1	1	1	1	1	1	1	240/255 x T	240/255 x T



where:
1. n=number of Grid.
2. T=T1 + T2
   T1=Brightness pulse width
   T2=Blank pulse `width

2.9 DISPLAY LIGHT SET COMMAND

The Display Light Set Command is used to turn all display lights ON or OFF. All Display Lights On Mode is primarily used for testing the display. The All Display Light OFF Mode is used for the blinking display and to prevent any malfunction when the power is turned on. The command format is given below.

	MSB							LSB
	B7	B6	B5	B4	B3	B2	B1	B0
1st Byte	1	1	1	0	1	0	LS	HS

where:
1. HS: All Display Lights are turned ON.
2. LS: All Display Lights are turned OFF.

The table below shows Segment and Anode Display Status in relation to the Display Light Set Command data.

Bit Name	Segment and Anode Display Status
HS	"0": Normal Display Mode "1": All outputs (Anode, Segment)="High" The duty of Outputs will follow Dimming Setting.
LS	"0": Normal Display Mode "1": All outputs (Anode, Segment)="Low" and the "HS" bit become don't-care. The duty of Outputs will follow Dimming Setting

2.10 STAND-BY MODE COMMAND

The Stand-by Mode Command is stopped the IC's OSC Frequency and entered into the Test Mode Function. However, in the meantime, the Anode, Segment and Grid will be Low Level Output when ST set to "1" of the Stand-by Mode Command. Otherwise, it is a Normal Mode (OSC Frequency Activize) when ST set to "0".

	MSB							LSB
	B7	B6	B5	B4	B3	B2	B1	B0
1st Byte	1	1	1	0	1	1	*	ST

where:
1. ST="0": Normal Mode.
   ST="1": Stand-by Mode.
2. *=Reserved.

2.11 RESET FUNCTION

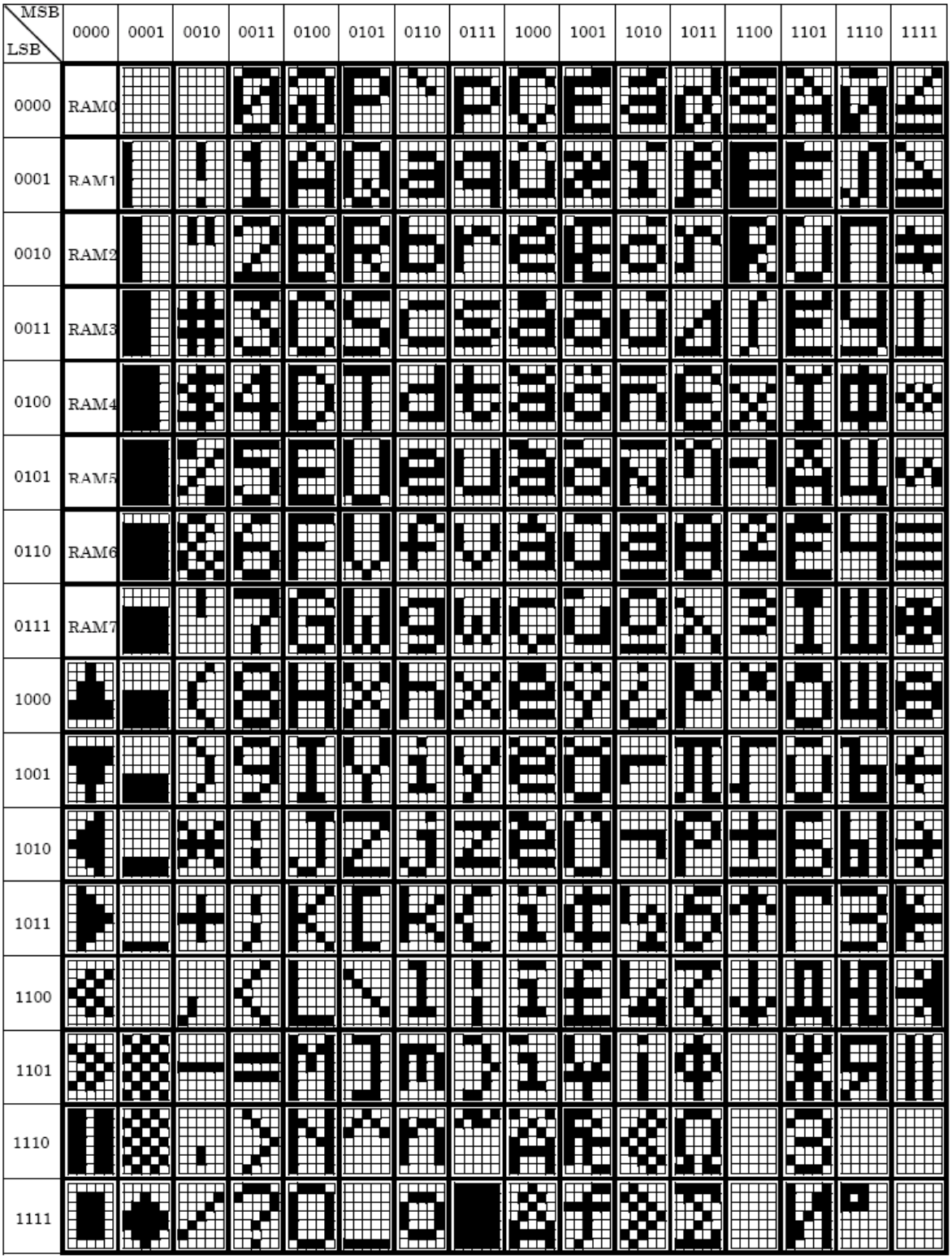
When IC is initialized, the internal status after power supply has been reset as follows.

Instruction	At Reset Condition
DCRAM	DCRAM Address=00H All DCRAM Data=20H
CGRAM	CGRAM Address=00H All CGRAM Data=00H
ADRAM	ADRAM Address=00H All ADRAM Data=00H Segment OFF(S1~S4 off)
URAM	URAM Disable URAM Address=00H All URAM Data=00H Grid OFF(1G~16G off)
Number of Digit Set	F0~F3=“1111”, F4~F6=“000” Universal Function Disable (UV=“0”)
Dimming Set	Dimming Quantity=0/255 (H0~H7=“0”)
Display Light Set	HS=“0” LS=“1” Normal Mode(Display all off)
Stand-by Mode	ST=”0” (Normal Mode)

3. FONT TABLE

CGROM, which is ROM for generating character patterns of 5 x 7 dots from 8-bit character codes, generates 248 types of character patterns. The character codes 00H to 07H are allocated to the CGRAM.

Code No. : 001



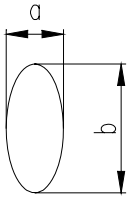
Vacuum Fluorescent Display Quality Inspection Standard

真空荧光显示屏质量检验标准

General 一般

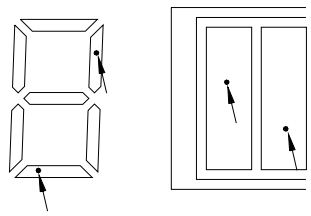
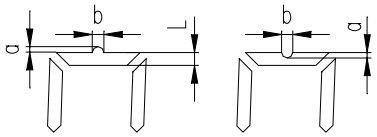
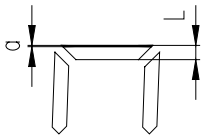
This standard should be adapted to the VFD quality inspection.
本规格书只适用于真空荧光显示屏的质量检验

Inspection Condition 检验条件

Item 项目	Condition 条件
①VFD Operating Condition VFD 驱动条件	Typ. Recommended Condition 推荐的驱动条件
②Inspection Aide 检验附带条件	The inspection is to be performed with ZBOE standard filter or a applicable customer's filter and unaided eyes from 300mm distance under brightness of 90～110 Lx. 用 ZBOE 标准的滤色板或顾客指定的滤色板检验，在观察距离约为 300mm、周围照度约为 90～110Lx 的环境状态下，用目测判定。
③Defect Point Definition 不良点的测定方法	 $\phi S=\frac{a+b}{2}$

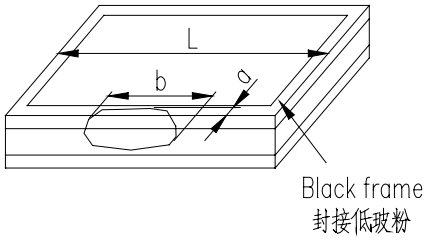
Limit sample should be provided upon mutual agreement by both parties when necessary.
必要时可以通过双方相互协商下保存限度样品。

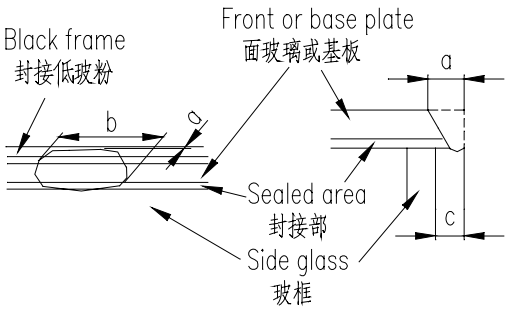
Individual Quality Standard 个别质量检验标准

Item 项目	Phenomena 现象	Criterion 判定标准
① Foreign Particles Black Spot Printing Error 管内异物 黑点 印刷不良	Spots（Black spot）on the lighted segment due to dirt or dust. 笔段中不发光的斑点（黑点）。 	1.A black spot of over ø 0.3mm is counted as defected point. 不允许有超过 S=ø 0.3mm 的黑点。 2.In case of spot size is over ø 0.2mm，less than ø 0.3mm，one spot on the same segment，or maximum 3 spots in a digit is to be allowed. ø 0.2mm～ ø 0.3mm 之间的黑点，同一笔段内允许 1 个，同一产品内允许 3 个。 3.A spot of less than ø 0.2mm should not be counted as defect point. ø 0.2mm 以下的黑点允许存在。
② Irregularity of segment shape by printing error. 印刷不良引起的笔段不规则形状。	Partial irregularity on a segment. 部分笔段不规则的形状。 	1.Acceptable size of irregularities with respect to the segment width（L）. 允许范围内的不规则笔段形状（笔段宽度为 L） a=0.3mm max，b=0.3mm max； a=0.3mm 以下，b=0.3mm ； 2.In case of the （L）below 0.5mm wide，the acceptable irregularities is a=1/2max of the segment width（L）. 笔段宽度在 0.5mm 以下，笔段不规则形状不得超过笔段的 1/2。
③ Uneven Luminance 亮度不匀	Partial dark area on the lighted segment. 发光笔段有亮度差异。	No significant irregularity of luminance is acceptable. 不允许存在明显的亮度不匀。
④ Shaded Segment 笔段阴影	Shaded area appeared on the edge of segment. 笔段边缘的阴影。 	1.Shaded Segments up to 1/3 of the segment width are accepted.. 不允许有超过笔段宽度 1/3 的阴影。 2.In case of a segment below 0.5mm wide，the acceptable shaded segment should be up to 1/2 of the segment wide. 笔段宽度在 0.5mm 以下，不允许有超过笔段宽度 1/2 的阴影。
⑤ Extra lighting 多余亮点	Undesirable lighting area or points, a star dust or a bright spot due like to extra phosphor particle. 多余的星屑状、亮点状发光体。	Extra lighting which can be clearly observed through the specified filter should be judged as a defect. 通过指定的滤色板，若能清楚地观察到额外的亮点就判定为不合格品。
⑥ Scratch/Stain on/in glass 玻璃的污迹和划伤	A scratch， dent， or foreign particles such as stain，attached on the surface or the inside of the front glass. 表玻璃内外面上的划伤、凹痕、异物附着。	1.Scratch which can be clearly observed through the specified filter should be judged as defect. 通过指定的滤色板，若能清楚地观察到划伤就判定为不合格品 2.The criterion for the dent and foreign particle are the same as the specified in ①. 凹痕、污迹的判定标准同①。
⑦ Chip on the front glass and base plate 面玻璃和基板缺口	For chip on the front glass and base plate，refer to the next page. 面玻璃和基板缺口见下一页。	Refer to the next page. 见下一页。

Criterion for the glass chip on the front glass or the base plate
面玻璃和基板缺口的检验标准

Definition 定义	Judgment Criterion 判定标准





a: depth of chipping
缺口深度
b: length of chipping
缺口长度
c: chipping size in relation to thickness of the side glass
缺口尺寸与玻框的关系
L: package width (length wide)
玻盖宽度（长度方向）

1.Chipping size Spec. 缺口尺寸规定

	a (VFD)	a (FLVFD)	b	c
L≤100	within the black frame 封接低玻粉内	3.0max	10max	1/3max
L>100	within the black frame 封接低玻粉内	3.5max	15max	1/3max

VFD: Vacuum Fluorescent Display
荧光显示屏
FLVFD: Front Luminous Vacuum Fluorescent Display
前面发光型荧光显示屏

2.A chip with "a" less than 1mm should not be counted as defect point.
a 尺寸小于 1mm 的缺口不作为不合格品。

3.A chip area covered with sealing cement should not be counted as defect point.
封接前的缺口在封接时封着了低玻粉为合格品。

4.Upto 3 chip within this specification in a same display to be allowed.
同一产品最多允许有 3 处缺口。