74HC299; 74HCT299

8-bit universal shift register; 3-state
Rev. 03 — 28 July 2008

Product data sheet

1. **General description**

The 74HC299; 74HCT299 are high-speed Si-gate CMOS devices which are pin-compatible with Low-power Schottky TTL (LSTTL) devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC299; 74HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. An operation is determined by the mode select inputs S0 and S1, as shown in Table 3.

Pins I/O0 to I/O7 are flip-flop 3-state buffer outputs which allow them to operate as data inputs in parallel load mode. The serial outputs Q0 and Q7 are used for expansion in serial shifting of longer words.

A LOW signal on the asynchronous master reset input $\overline{\text{MR}}$ overrides the Sn and clock CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is in either state, provided that the recommended set-up and hold times are observed.

A HIGH signal on the 3-state output enable inputs $\overline{OE}1$ or $\overline{OE}2$ disables the 3-state buffers and the I/On outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations still occur when preparing for a parallel load operation. The 3-state buffers are also disabled by HIGH signals on both S0 and S1.

2. **Features**

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
 - Shift left
 - Shift right
 - Hold (store)
 - Load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Cascadable for n-bit word lengths
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

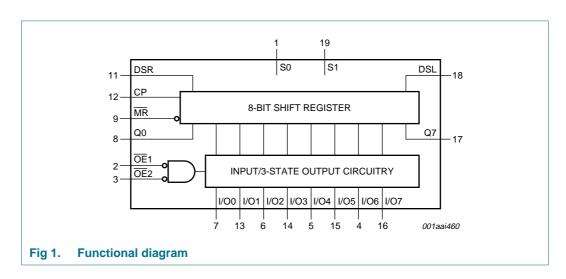


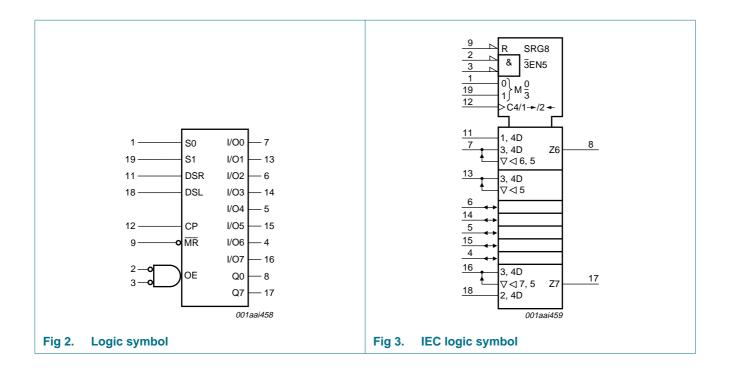
3. Ordering information

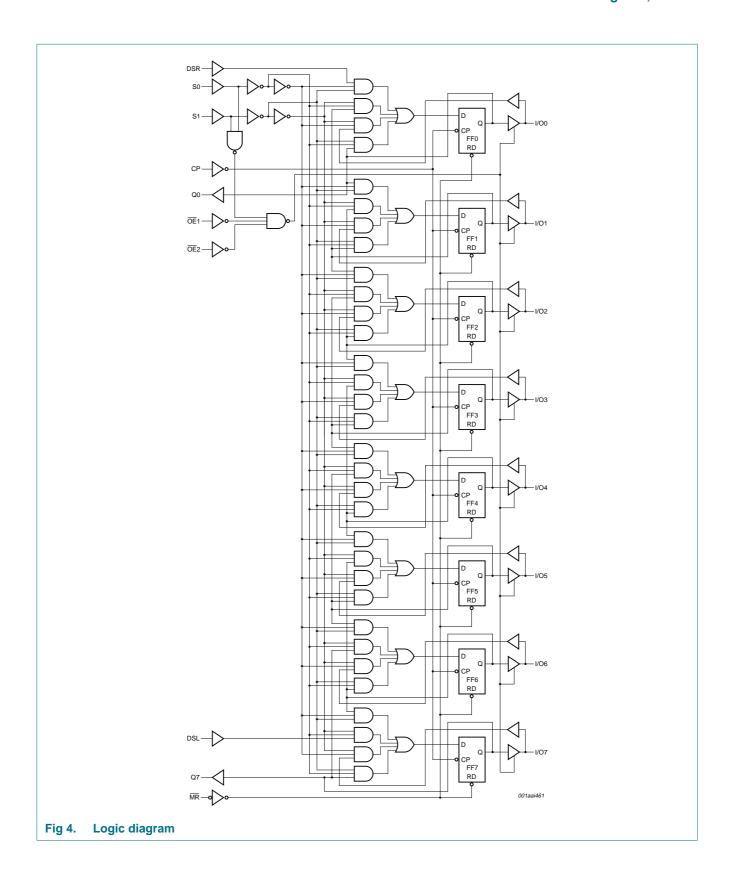
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC299				
74HC299D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC299DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC299N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC299PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT299				
74HCT299D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT299DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT299N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT299PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

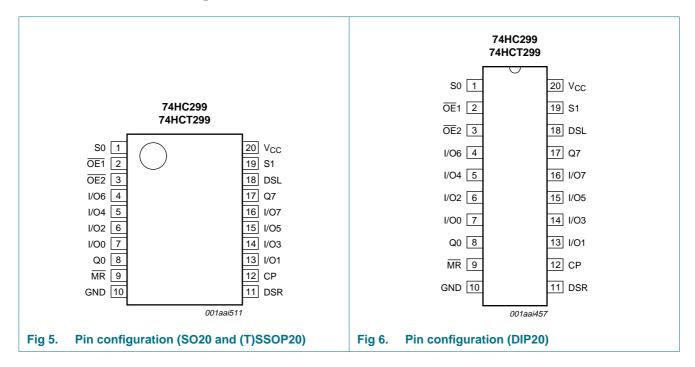






5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

<u> </u>		
Symbol	Pin	Description
S0	1	mode select input
ŌE1	2	3-state output enable input (active LOW)
OE2	3	3-state output enable input (active LOW)
1/06	4	parallel data input or 3-state parallel output (bus driver)
1/O4	5	parallel data input or 3-state parallel output (bus driver)
I/O2	6	parallel data input or 3-state parallel output (bus driver)
1/00	7	parallel data input or 3-state parallel output (bus driver)
Q0	8	serial output (standard output)
MR	9	asynchronous master reset input (active LOW)
GND	10	ground (0 V)
DSR	11	serial data shift-right input
CP	12	clock input (LOW to HIGH, edge-triggered)
1/01	13	parallel data input or 3-state parallel output (bus driver)
I/O3	14	parallel data input or 3-state parallel output (bus driver)
I/O5	15	parallel data input or 3-state parallel output (bus driver)
1/07	16	parallel data input or 3-state parallel output (bus driver)
Q7	17	serial output (standard output)

 Table 2.
 Pin description ...continued

Symbol	Pin	Description
DSL	18	serial data shift-left input
S1	19	mode select input
V _{CC}	20	positive supply voltage

6. Functional description

Table 3. Function table[1]

Input				Response
MR	S1	S0	СР	
L	X	X	X	asynchronous reset; Q0 to Q7 = LOW
Н	Н	Н	↑	parallel load; I/On → Qn
Н	L	Н	↑	shift right; DSR \rightarrow Q0, Q0 \rightarrow Q1, etc.
Н	Н	L	↑	shift left; DSL \rightarrow Q7, Q7 \rightarrow Q6, etc.
Н	L	L	Χ	hold

^[1] H = HIGH voltage level;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$			
	standard outputs		-	±25	mA
	bus driver outputs		-	±35	mA
I _{CC}	supply current				
	standard outputs		-	50	mA
	bus driver outputs		-	70	mA
I_{GND}	ground current				
	standard outputs		-50	-	mA
	bus driver outputs		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$			
		DIP20 package	[2] _	750	mW
		SO20 package	[3] _	500	mW
		(T)SSOP20 package	<u>[4]</u> -	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

L = LOW voltage level;

 $[\]uparrow$ = LOW to HIGH CP transition;

X = don't care.

- [2] Ptot derates linearly at 12 mW/K above 70 °C.
- [3] P_{tot} derates linearly at 8 mW/K above 70 °C.
- [4] P_{tot} derates linearly at 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol Parameter Co		Conditions	74HC	299		74HC	Unit		
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_{I}	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
Vo	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate								
		$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	1.39	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	–40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC299		'	·	'						
V_{IH}	HIGH-level	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level	$V_{CC} = 2.0 \text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Table 6. Static characteristics ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Uni
			Min	Тур	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}	'						•	
	output voltage	all outputs								
		$I_O = -20 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A$; $V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		standard outputs								
		$I_O = -4.0 \text{ mA};$ $V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2 \text{ mA};$ $V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
		bus driver outputs								
		$I_O = -6.0 \text{ mA};$ $V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -7.8 \text{ mA};$ $V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	all outputs								
		$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μ A; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	V
		standard outputs								
		I_{O} = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
		bus driver outputs								
		$I_O = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.5	-	±5.0	-	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
C _{I/O}	input/output capacitance		-	10	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per package	[1] -	120	-	-	-	-	-	pF
74HCT29	9									
V _{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	all outputs								
		$I_O = -20 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		standard outputs								
		$I_O = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
	oL LOW-level output voltage	bus driver outputs								
		$I_O = -6.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}		$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	all outputs								
		$I_O = 20 \mu A$	-	0	0.1	-	0.1	-	0.1	V
		standard outputs								
		$I_0 = 4.0 \text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V
		bus driver outputs								
		$I_0 = 6.0 \text{ mA}$	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	±0.5	-	±5.0	-	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
Δl _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V								
		I/On, DSR, DSL, $\overline{\text{MR}}$ and S1	-	25	90	-	112.5	-	122.5	μΑ
		CP, S0	-	60	216	-	270	-	294	μΑ
		ŌĒn	-	30	108	-	135	-	147	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
C _{I/O}	input/output capacitance		-	10	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per package	<u>1]</u> -	125	-	-	-	-	-	pF

^[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum (C_L \times V_{CC}{}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

 $V_I = GND$ to V_{CC} for 74HC299;

 $V_I = GND$ to $(V_{CC} - 1.5 \text{ V})$ for 74HCT299.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions			25 °C			°C to 5 °C		°C to 5 °C	Unit
	propagation delay			Min	Тур	Max	Min	Max	Min	Max	
74HC299											
t_{pd}		CP to Q0, Q7; see Figure 7	<u>[1]</u>								
	delay	$V_{CC} = 2.0 \text{ V}$		-	66	200	-	250	-	300	ns
		$V_{CC} = 4.5 \text{ V}$		-	24	40	-	50	-	60	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V		-	19	34	-	43	-	51	ns
		CP to I/On; see Figure 7									
		V _{CC} = 2.0 V		-	66	200	-	250	-	300	ns
		V _{CC} = 4.5 V		-	24	40	-	50	-	60	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V		-	19	34	-	43	-	51	ns
		MR to Q0, Q7 or I/On; see Figure 8	[2]								
		V _{CC} = 2.0 V		-	66	200	-	250	-	300	ns
		V _{CC} = 4.5 V		-	24	40	-	50	-	60	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V		-	19	34	-	43	-	51	ns
t _t	transition time	bus driver (I/On); see Figure 7	[3]								
		V _{CC} = 2.0 V		-	14	60	-	75	-	90	ns
		V _{CC} = 4.5 V		-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0 \text{ V}$		-	4	10	-	13	-	15	ns
		standard (Q0, Q7); see Figure 7									
		$V_{CC} = 2.0 \text{ V}$		-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V		-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$		-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics ...continued GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions			25 °C			°C to 5 °C	–40 °C to +125 °C		Unit
			ı	Vin	Тур	Max	Min	Max	Min	Max	
t_W	pulse width	CP HIGH or LOW; see Figure 7									
		$V_{CC} = 2.0 \text{ V}$		80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$		16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$		14	5	-	17	-	20	-	ns
		MR LOW; see Figure 8									
		$V_{CC} = 2.0 \text{ V}$		80	19	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$		16	7	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$		14	6	-	17	-	20	-	ns
t _{PZH}	OFF-state to	OEn to I/On; see Figure 10	<u>[4]</u>								
	HIGH	$V_{CC} = 2.0 \text{ V}$		-	50	155	-	195	-	235	ns
	propagation delay	$V_{CC} = 4.5 \text{ V}$		-	18	31	-	39	-	47	ns
	-	$V_{CC} = 6.0 \text{ V}$		-	14	26	-	33	-	40	ns
t_{PZL}	OFF-state to LOW propagation delay	OEn to I/On; see Figure 10									
		$V_{CC} = 2.0 \text{ V}$		-	41	130	-	165	-	195	ns
		$V_{CC} = 4.5 \text{ V}$		-	15	26	-	33	-	39	ns
	j	$V_{CC} = 6.0 \text{ V}$		-	12	22	-	28	-	33	ns
t _{PHZ}	HIGH to	OEn to I/On; see Figure 10	<u>[5]</u>								
	OFF-state propagation	$V_{CC} = 2.0 \text{ V}$		-	66	185	-	230	-	280	ns
	delay	$V_{CC} = 4.5 \text{ V}$		-	24	37	-	46	-	56	ns
	•	$V_{CC} = 6.0 \text{ V}$		-	19	31	-	39	-	48	ns
t_{PLZ}	LOW to	OEn to I/On; see Figure 10									
	OFF-state	$V_{CC} = 2.0 \text{ V}$		-	55	155	-	195	-	235	ns
	propagation delay	$V_{CC} = 4.5 \text{ V}$		-	20	31	-	39	-	47	ns
	·	$V_{CC} = 6.0 \text{ V}$		-	16	26	-	33	-	40	ns
t _{rec}	recovery time	MR to CP; see Figure 8									
		$V_{CC} = 2.0 \text{ V}$		5	-14	-	5	-	5	-	ns
		V _{CC} = 4.5 V		5	- 5	-	5	-	5	-	ns
		V _{CC} = 6.0 V		5	-4	-	5	-	5	-	ns

Table 7. Dynamic characteristics ...continued GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	1	°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
t _{su}	set-up time	DSR, DSL to CP; see Figure 7								
		$V_{CC} = 2.0 \text{ V}$	100	33	-	125	-	150	-	ns
		$V_{CC} = 4.5 \text{ V}$	20	12	-	25	-	30	-	ns
		$V_{CC} = 6.0 \text{ V}$	17	10	-	21	-	26	-	ns
		S0, S1 to CP; see Figure 9								
		$V_{CC} = 2.0 \text{ V}$	100	33	-	125	-	150	-	ns
		$V_{CC} = 4.5 \text{ V}$	20	12	-	25	-	30	-	ns
		$V_{CC} = 6.0 \text{ V}$	17	10	-	21	-	26	-	ns
		I/On to CP; see Figure 7								
		$V_{CC} = 2.0 \text{ V}$	125	39	-	155	-	190	-	ns
		$V_{CC} = 4.5 \text{ V}$	25	14	-	31	-	38	-	ns
		$V_{CC} = 6.0 \text{ V}$	21	11	-	26	-	32	-	ns
t _h	hold time	I/On, DSR, DSL to CP; see Figure 7								
		$V_{CC} = 2.0 \text{ V}$	0	-14	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	-5	-	0	-	0	-	ns
	$V_{CC} = 6.0 \text{ V}$	0	-4	-	0	-	0	-	ns	
		S0, S1 to CP; see Figure 9								
		$V_{CC} = 2.0 \text{ V}$	0	-28	-	0	-	0	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-10	-	0	-	0	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-8	-	0	-	0	-	ns
f _{max}	maximum	CP input; see Figure 7								
	frequency	V _{CC} = 2.0 V	5.0	15	-	4.0	-	3.4	-	МН
		V _{CC} = 4.5 V	25	45	-	20	-	17	-	МН
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	50	-	-	-	-	-	МН
		V _{CC} = 6.0 V	29	54	-	24	-	20	-	MH
74HCT29	9									
t _{pd}	propagation	CP to Q0, Q7; see Figure 7	<u>[1]</u>							
	delay	V _{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
		CP to I/On; see Figure 7								
		V _{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
		MR to Q0, Q7 or I/On; see Figure 8	[2]							
		V _{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	23	-	-	-	-	-	ns

Table 7. Dynamic characteristics ...continued GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions			25 °C			°C to 5 °C		°C to 5 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	1
t _t	transition time	bus driver (I/On); see Figure 7	[3]								
		V _{CC} = 4.5 V		-	5	12	-	15	-	18	ns
		standard (Q0, Q7); see Figure 7									
		V _{CC} = 4.5 V		-	7	15	-	19	-	22	ns
t _W	pulse width	clock HIGH or LOW; see Figure 7									
		V _{CC} = 4.5 V		20	10	-	25	-	30	-	ns
		master reset LOW; see Figure 8									
		V _{CC} = 4.5 V		20	11	-	25	-	30	-	ns
t _{en}	enable time	OEn to I/On; see Figure 10	<u>[4]</u>								
		V _{CC} = 4.5 V		-	19	30	-	38	-	45	ns
t _{PHZ}	HIGH to	OEn to I/On; see Figure 10	<u>[5]</u>								
	OFF-state propagation delay	V _{CC} = 4.5 V		-	24	37	-	46	-	56	ns
t _{PLZ}	LOW to	OEn to I/On; see Figure 10									
	OFF-state propagation delay	V _{CC} = 4.5 V		-	20	32	-	40	-	48	ns
t _{rec}	recovery time	MR to CP; see Figure 8									
		V _{CC} = 4.5 V		10	2	-	9	-	11	-	ns
t _{su}	set-up time	I/On, DSR, DSL to CP; see Figure 7									
		V _{CC} = 4.5 V		25	14	-	31	-	38	-	ns
		S0, S1 to CP; see Figure 9									
		V _{CC} = 4.5 V		32	18	-	40	-	48	-	ns
t _h	hold time	I/On, DSR, DSL to CP; see Figure 7									
		$V_{CC} = 4.5 V$		0	-11	-	0	-	0	-	ns
		S0, S1 to CP; see Figure 9									
		V _{CC} = 4.5 V		0	-17	-	0	-	0	-	ns
f _{max}	maximum	CP input; see Figure 7									
	frequency	V _{CC} = 4.5 V		25	42	-	20	-	17	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	46	-	-	-	-	-	MHz

^[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

^[2] t_{pd} is the same as t_{PHL} .

^[3] $\ t_t$ is the same as t_{THL} and $t_{TLH}.$

^[4] t_{en} is the same as t_{PZH} and t_{PZL} .

^[5] t_{dis} is the same as t_{PHZ} and t_{PLZ} .

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

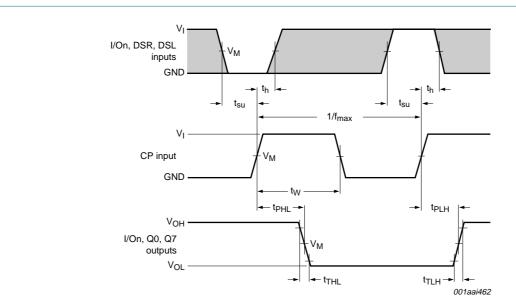
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching.

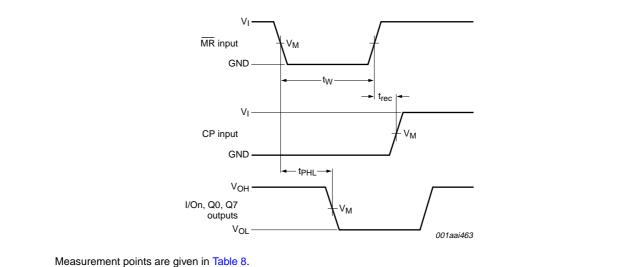
11. Waveforms



The shaded areas indicate when the input is permitted to change for predictable output performance. Measurement points are given in Table 8.

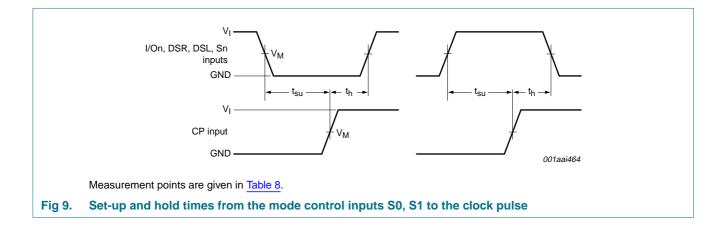
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

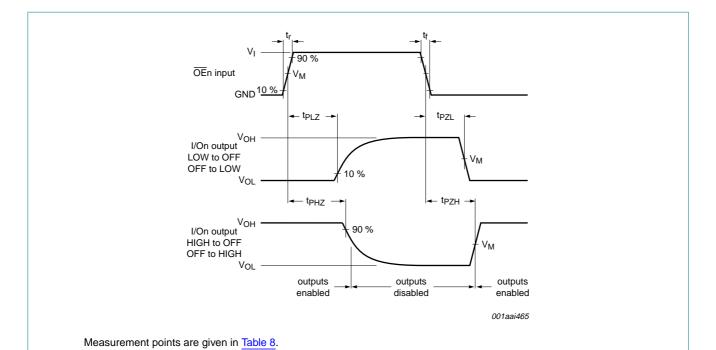
Fig 7. Clock pulse to outputs I/On, Q0, Q7 propagation delays, the clock pulse width, the I/On, DSR and DSL to clock pulse set-up and hold times, the output transition times and the maximum clock frequency



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. The master reset pulse width (LOW), the master reset to outputs I/On, Q0, Q7 propagation delays and the master reset to clock pulse removal time



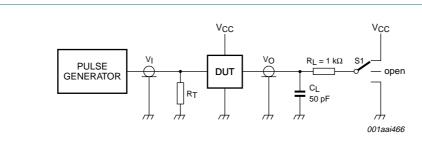


Measurement points

Table 8.

Fig 10. 3-state enable and disable times for $\overline{\text{OE}}$ n inputs

Туре	Input		Output
	V _I	V _M	V _M
74HC299	V_{CC}	0.5V _{CC}	0.5V _{CC}
74HCT299	3 V	1.3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

DUT = Device Under Test.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

C_L = Load capacitance including jig and probe capacitance.

 R_L = Load resistance.

S1 = Test selection switch

Fig 11. Test circuit for measuring switching times

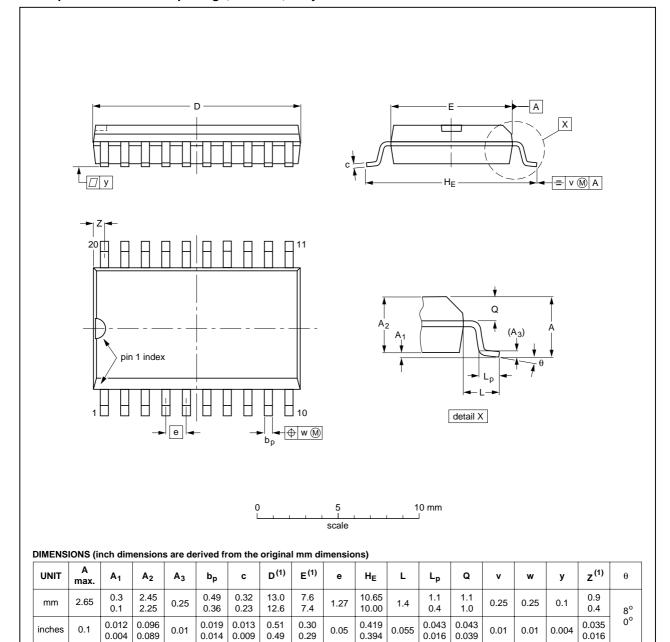
Table 9. Test data

Туре	Input		Load	S1 position	
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}
74HC299	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT299	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014

0.009

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013				99-12-27 03-02-19

0.394

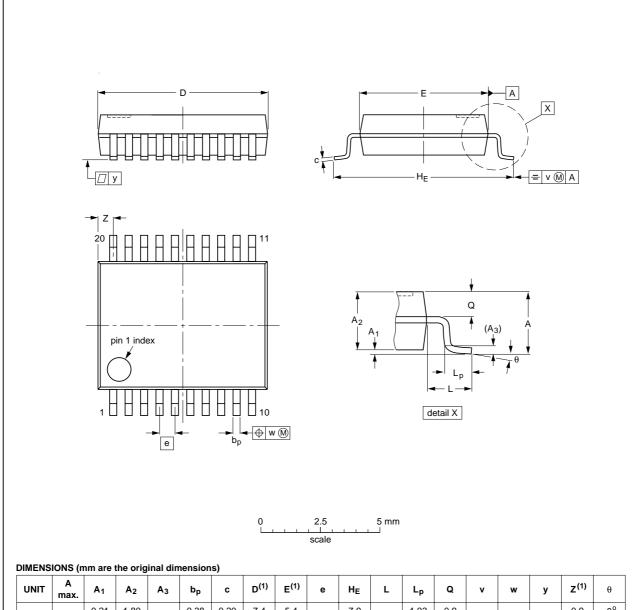
Fig 12. Package outline SOT163-1 (SO20)

0.004

0.089

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

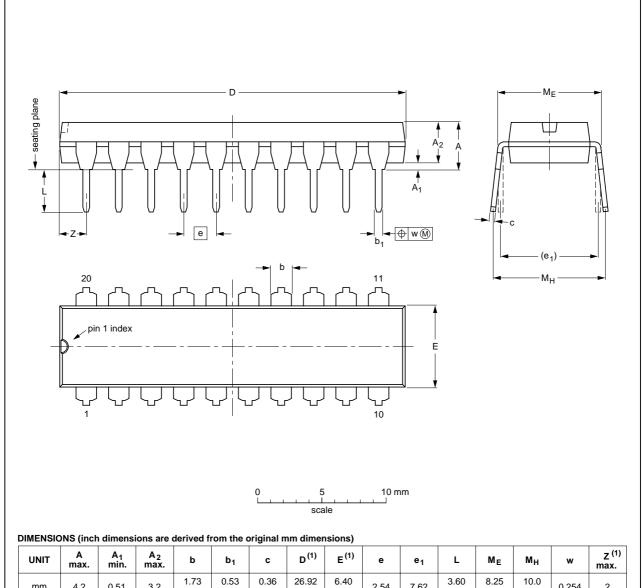
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

PROJECTION ISSUE DATE	
99-12-27- 03-02-19	
	99-12-27

Fig 13. Package outline SOT339-1 (SSOP20)

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ΜE	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

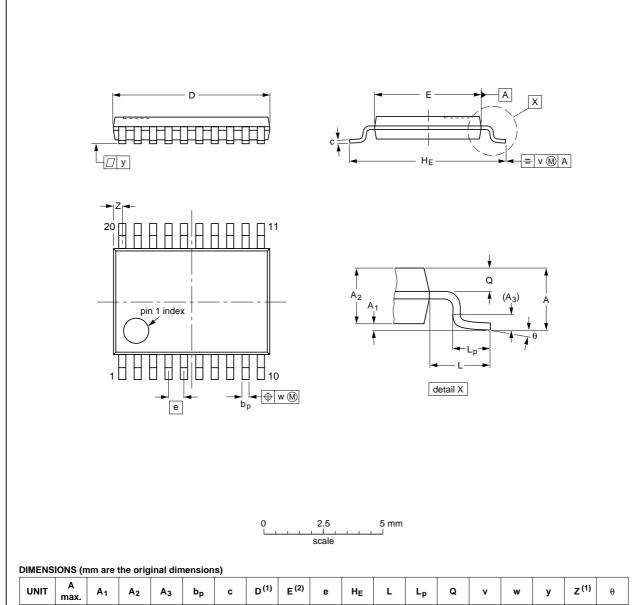
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT146-1		MS-001	SC-603			99-12-27 03-02-13	

Fig 14. Package outline SOT146-1 (DIP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



=							-,												
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT360-1		MO-153			99-12-27 03-02-19

Fig 15. Package outline SOT360-1 (TSSOP20)

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes					
74HC_HCT299_3	20080728	Product data sheet	-	74HC_HCT299_CNV_2					
Modifications:		 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 							
	 Legal texts I 	 Legal texts have been adapted to the new company name where appropriate. 							
	 Section 3: C 	Ordering information added							
	• <u>Section 12</u> :	Package outline drawings a	dded						
	Section 9 "Static characteristics": Family data added								
	 Section 11 "Waveforms": Test circuit added 								
74HC_HCT299_CNV_2	19970828	Product specification	-	-					

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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