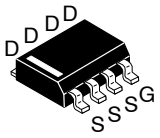
SyncFET™ – N-Channel, POWERTRENCH®

30 V

FDS6676AS, FDS6676AS-G

V_{DSS} MAX	$R_{DS(on)}$ MAX	I_D MAX
30 V	6.0 mΩ @ 10 V	14.5 A
	7.25 mΩ @ 4.5 V	



SOIC8
(SO−8)
CASE 751EB

General Description

The FDS6676AS is designed to replace a single SO−8 MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30 V MOSFET is designed to maximize power conversion efficiency, providing a low $R_{DS(ON)}$ and low gate charge. The FDS6676AS includes an integrated Schottky diode using **onsemi**'s monolithic SyncFET technology.

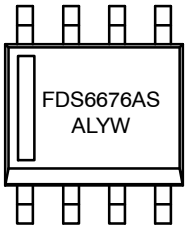
Features

- 14.5 A, 30 V
  - $R_{DS(ON)}$ Max = 6.0 mΩ at V_{GS} = 10 V
  - $R_{DS(ON)}$ Max = 7.25 mΩ at V_{GS} = 4.5 V
- Includes SyncFET Schottky Body Diode
- Low Gate Charge (45 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$ and Fast Switching
- High Power and Current Handling Capability
- These Devices are Pb−Free and are RoHS Compliant

Applications

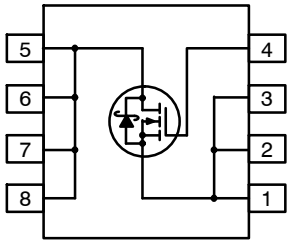
- DC/DC Converter
- Low Side Notebook

MARKING DIAGRAM



FDS6676AS	= Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

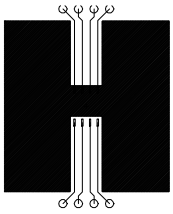
Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain−Source Voltage		30	V
V_{GSS}	Gate−Source Voltage		±20	V
I_D	Drain Current	Continuous (Note 1a)	14.5	A
		Pulsed	50	A
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

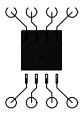
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	25	°C/W

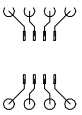
1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 105°C/W when mounted on a .04 in^2 pad of 2 oz copper.



c.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	20	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	500	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	−4	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 14.5 A	–	4.5	6.0	mΩ
		V_{GS} = 4.5 V, I_D = 13.2 A	–	5.9	7.25	
		V_{GS} = 10 V, I_D = 14.5 A, T_J = 125°C	–	6.7	8.5	
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	50	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 14.5 A	–	66	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	–	2510	–	pF
C_{oss}	Output Capacitance		–	710	–	pF
C_{rss}	Reverse Transfer Capacitance		–	270	–	pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	–	1.6	2.8	Ω
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 1 A V_{GS} = 10 V, R_{GEN} = 6 Ω	–	10	20	ns
t_r	Turn−On Rise Time		–	12	22	ns
$t_{d(off)}$	Turn−Off Delay Time		–	43	69	ns
t_f	Turn−Off Fall Time		–	29	46	ns
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 1 A V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	17	31	ns
t_r	Turn−On Rise Time		–	22	35	ns
$t_{d(off)}$	Turn−Off Delay Time		–	34	54	ns
t_f	Turn−Off Fall Time		–	29	46	ns
$Q_{g(TOT)}$	Total Gate Charge at Vgs = 10 V	V_{DD} = 15 V, I_D = 14.5 A	–	45	63	nC
Q_g	Total Gate Charge at Vgs = 5 V		–	25	35	nC
Q_{gs}	Gate−Source Charge		–	7	–	nC
Q_{gd}	Gate−Drain Charge		–	8	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.5 A (Note 2)	–	0.4	0.7	V
		V_{GS} = 0 V, I_S = 7 A (Note 2)	–	0.5	–	V
t_{rr}	Diode Reverse Recovery Time	I_F = 14.5 A, d_{iF}/d_t = 300 A/μs (Note 3)	–	27	–	ns
I_{RM}	Diode Reverse Recovery Current		–	1.9	–	A
Q_{rr}	Diode Reverse Recovery Charge		–	26	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. See "SyncFET Schottky Body Diode Characteristics" below.

TYPICAL CHARACTERISTICS

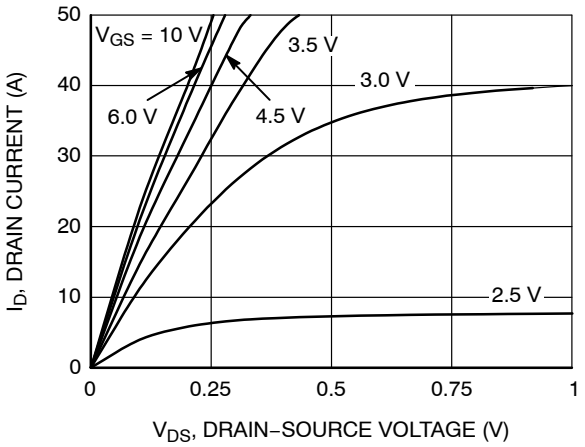


Figure 1. On−Region Characteristics

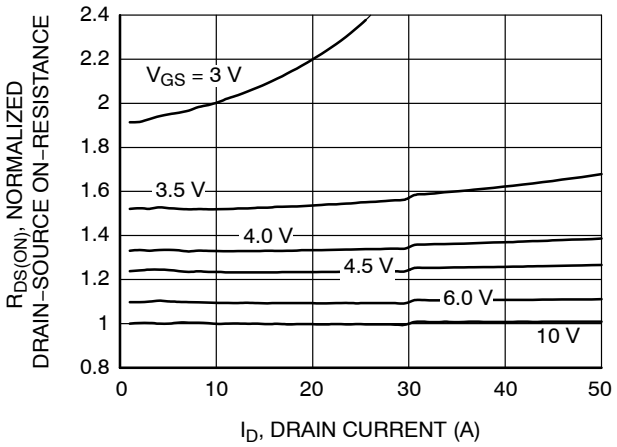


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

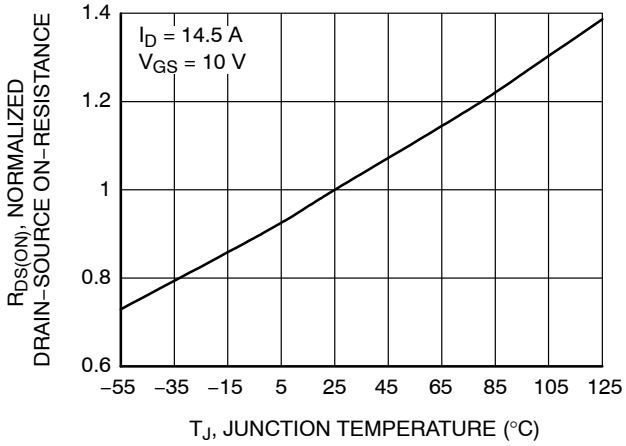


Figure 3. On−Resistance Variation with Junction Temperature

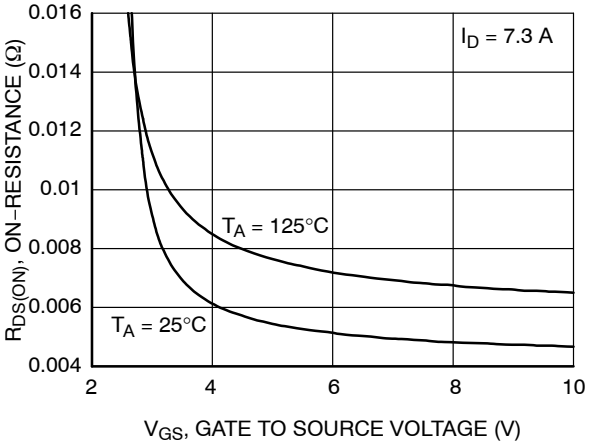


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

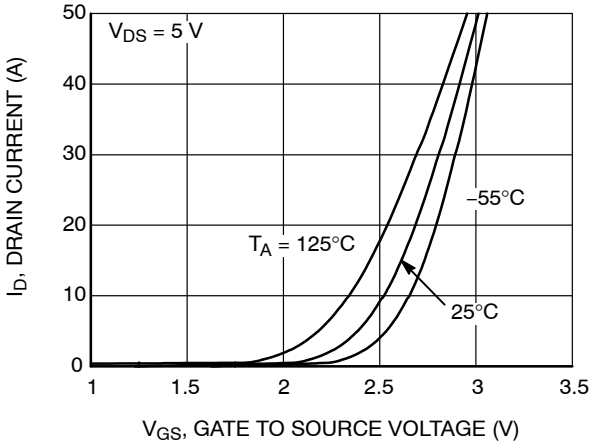


Figure 5. Transfer Characteristics

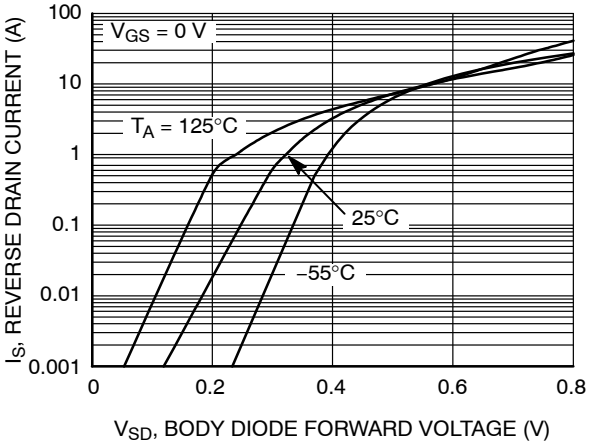


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

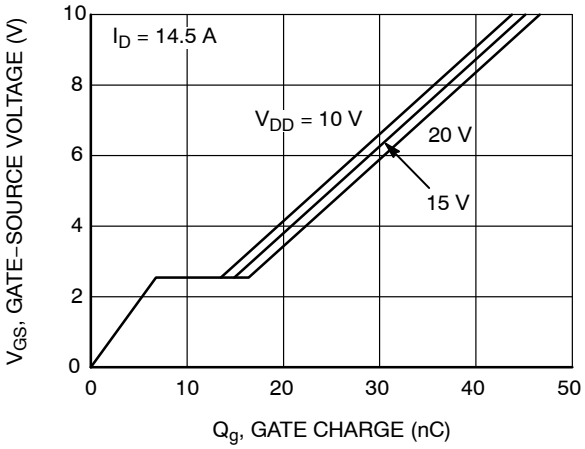


Figure 7. Gate Charge Characteristics

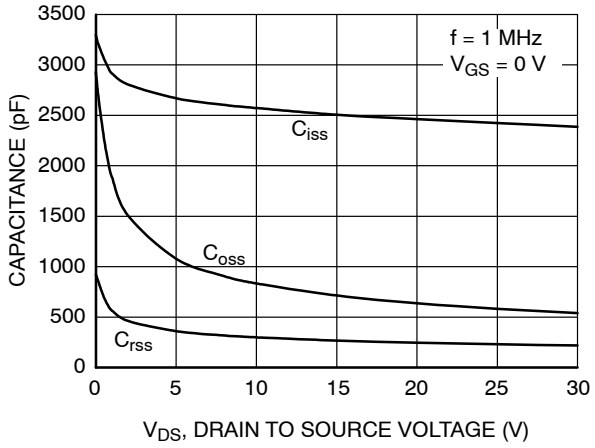


Figure 8. Capacitance Characteristics

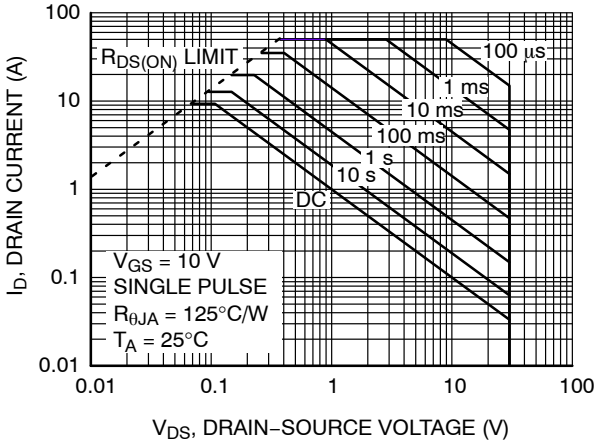


Figure 9. Maximum Safe Operating Area

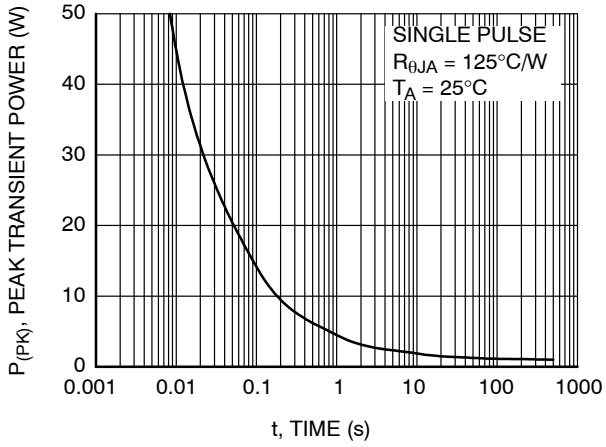


Figure 10. Single Pulse Maximum Power Dissipation

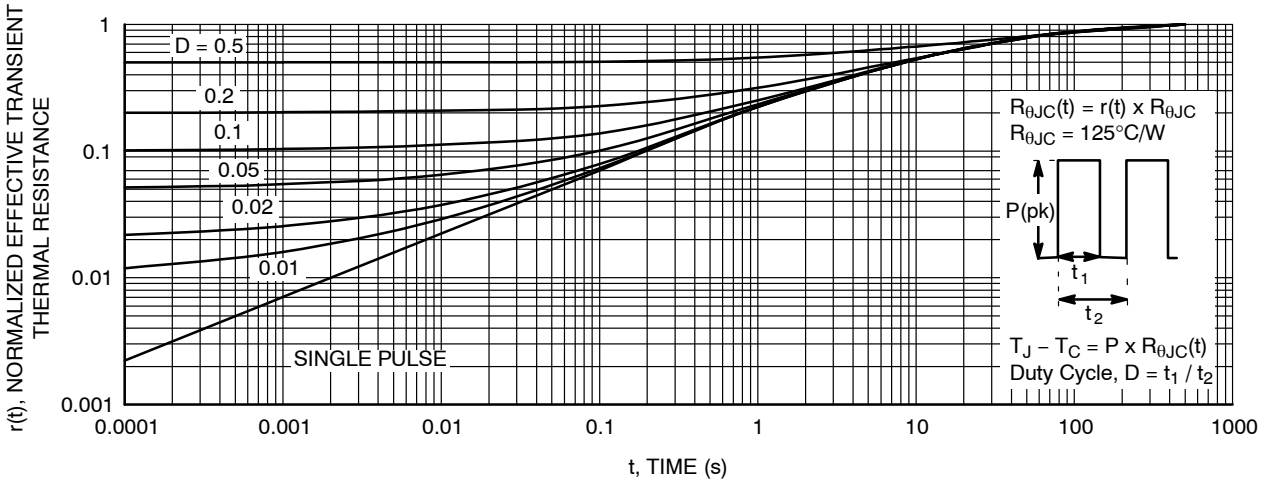


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDS6676AS.

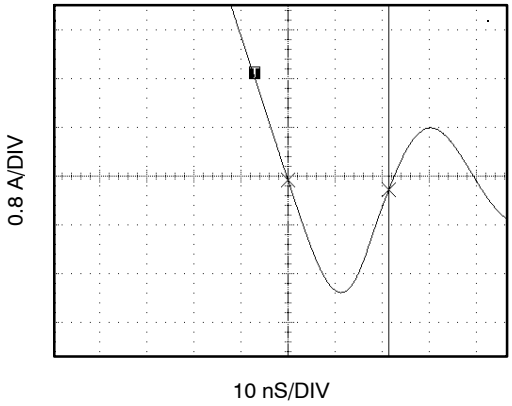


Figure 12. FDS6676AS SyncFET Body Diode Reverse Recovery Characteristics

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6676).

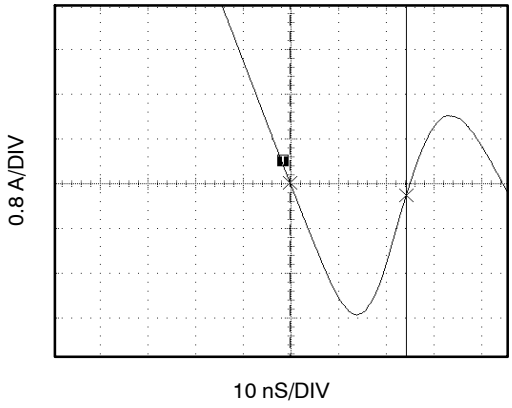


Figure 13. Non−SyncFET (FDS6676) Body Diode Reverse Recovery Characteristics

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

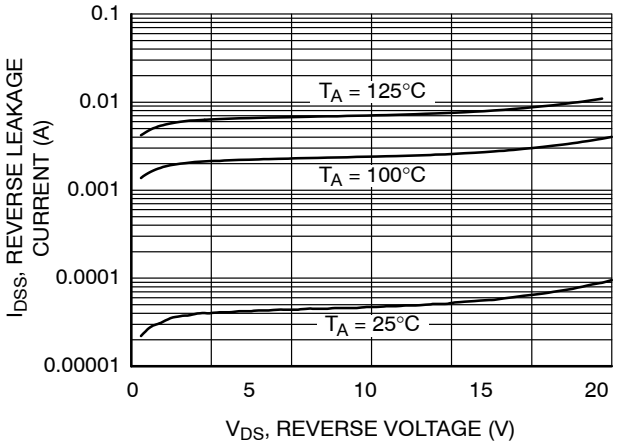


Figure 14. SyncFET Body Diode Reverse Leakage vs. Drain−Source Voltage and Temperature

TYPICAL CHARACTERISTICS (continued)

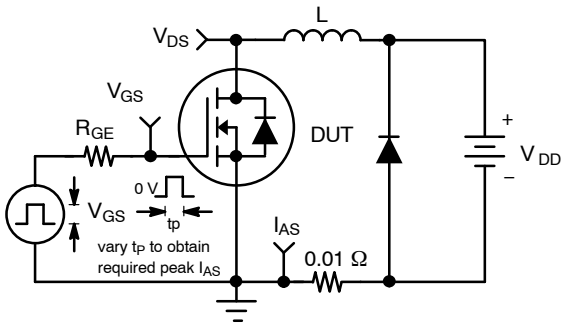


Figure 15. Unclamped Inductive Load Test Circuit

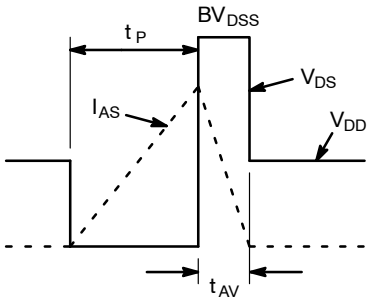


Figure 16. Unclamped Inductive Waveforms

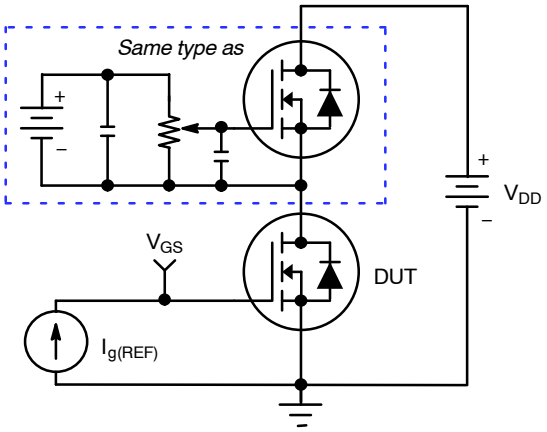


Figure 17. Gate Charge Test Circuit

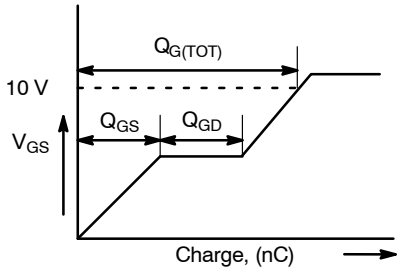


Figure 18. Gate Charge Waveforms

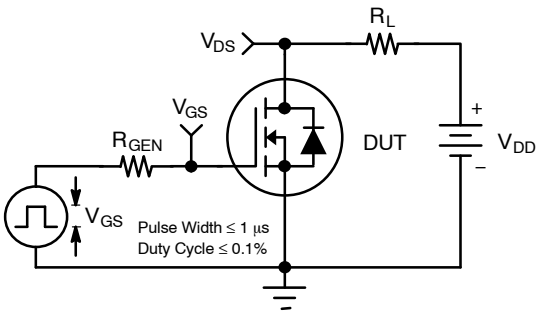


Figure 19. Switching Time Test Circuit

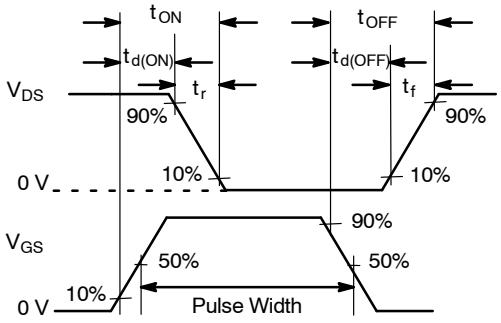


Figure 20. Switching Time Waveforms

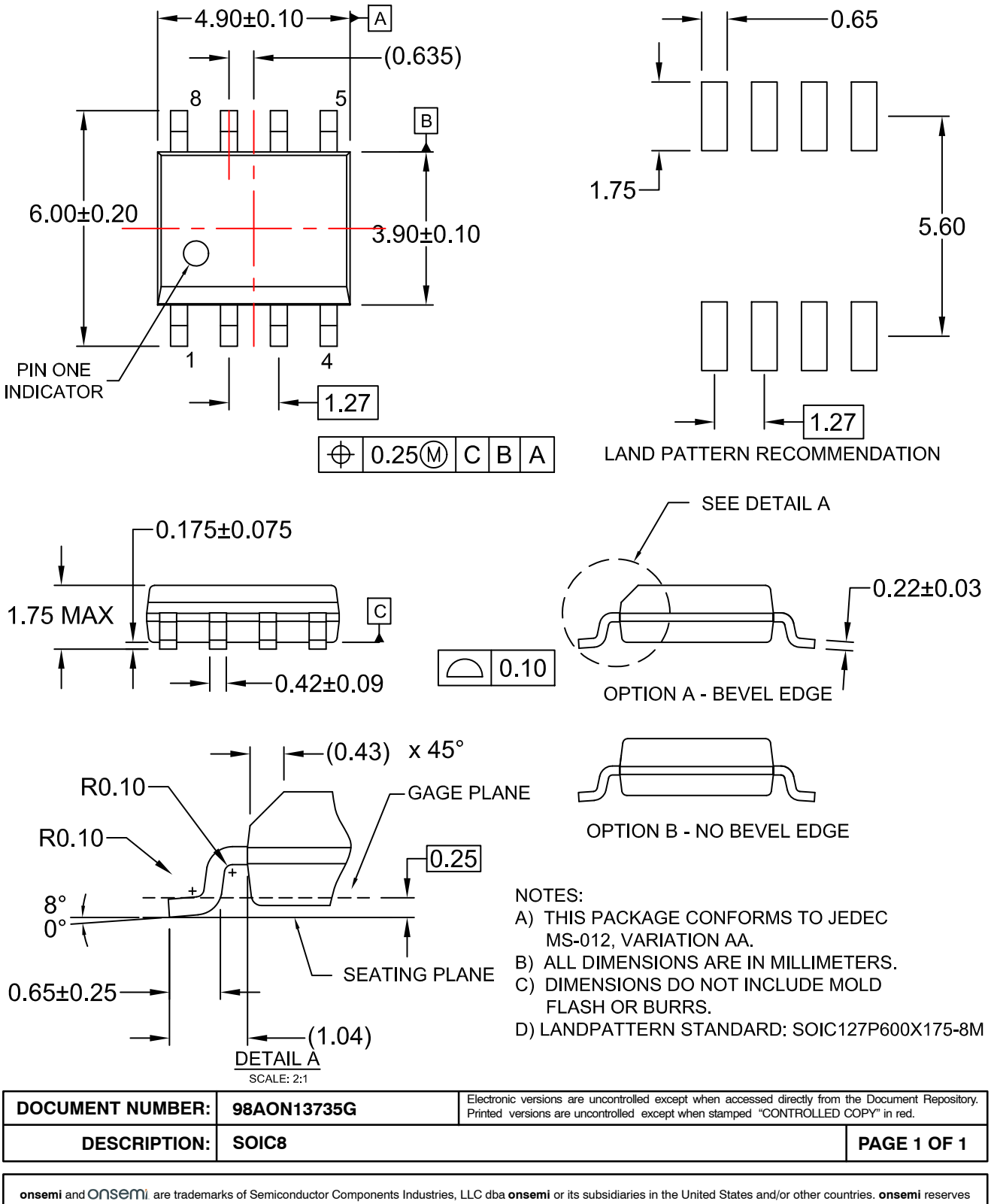
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDS6676AS	FDS6676AS	SOIC8 (SO−8) (Pb−Free)	13”	12 mm	2500 / Tape & Reel
FDS6676AS−G	FDS6676AS	SOIC8 (SO−8) (Pb−Free)	13”	12 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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DESCRIPTION:	**SOIC8**	**PAGE 1 OF 1**

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