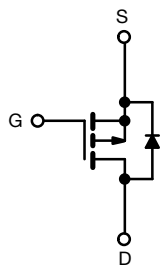


Power MOSFET

TO-220AB


P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	3.0
Q_g max. (nC)	11	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	4.0	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9610PbF
Lead (Pb)-free and halogen-free	IRF9610PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	-200	V
Gate-source voltage			V _{GS}	± 20	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	I _D	-1.8	A
		T _C = 100 °C		-1.0	
Pulsed drain current ^a			I _{DM}	-7.0	
Linear derating factor				0.16	W/°C
Single pulse avalanche energy ^b			P _D	20	W
Repetitive avalanche current ^a			I _{LM}	-7.0	A
Repetitive avalanche energy ^a			dV/dt	-5.0	V/ns
Maximum power dissipation	T _C = 25 °C		T _J , T _{stg}	-55 to +150	°C
Peak diode recovery dV/dt ^c				300	
Operating junction and storage temperature range				10	lbf · in
Soldering recommendations (peak temperature) ^d		For 10 s		1.1	N · m

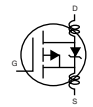
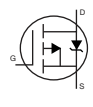
Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
- Not applicable
- $I_{SD} \leq -1.8$ A, $dI/dt \leq 70$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

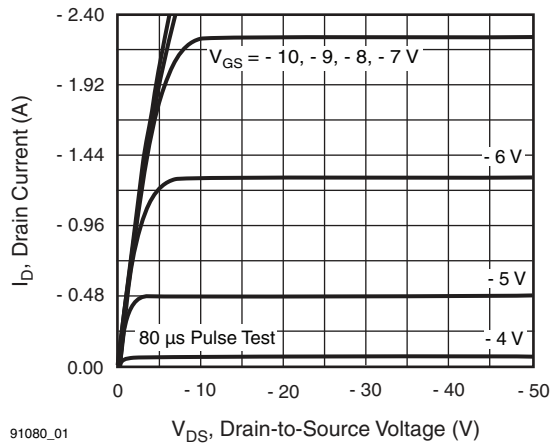
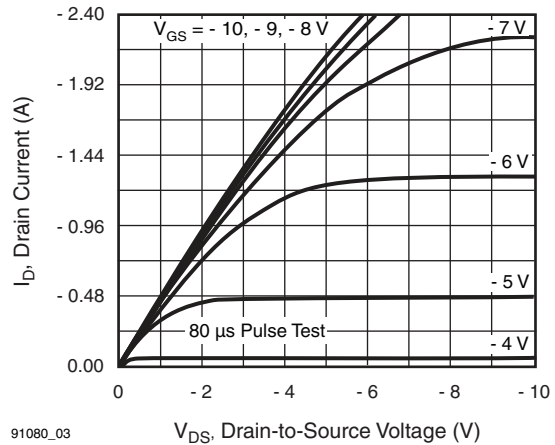
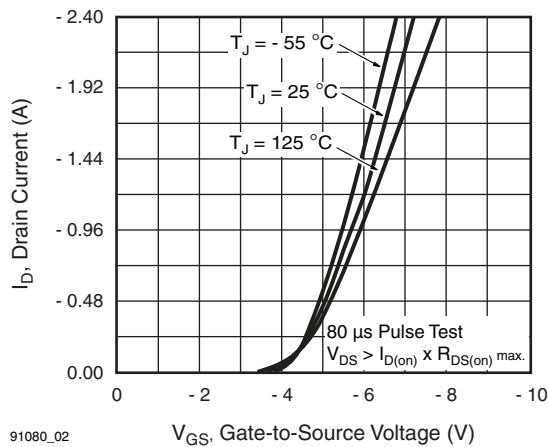
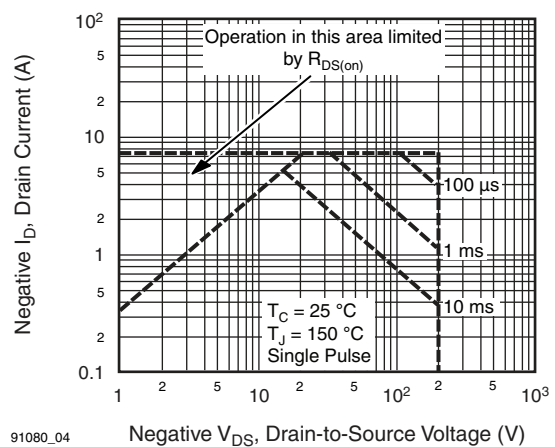
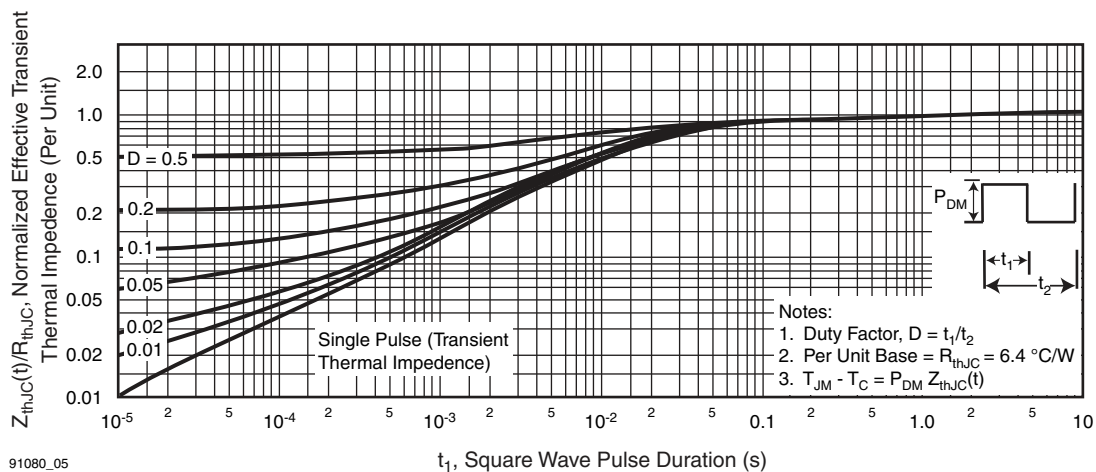
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	6.4	

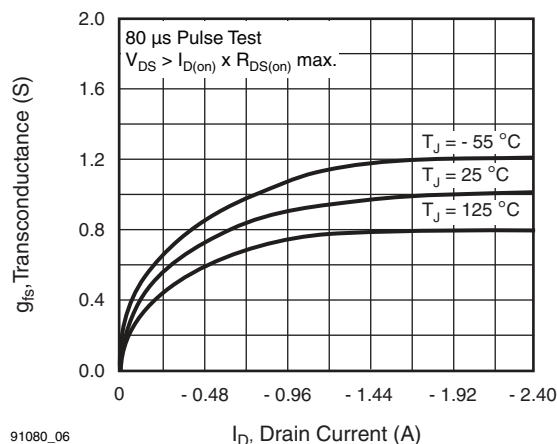
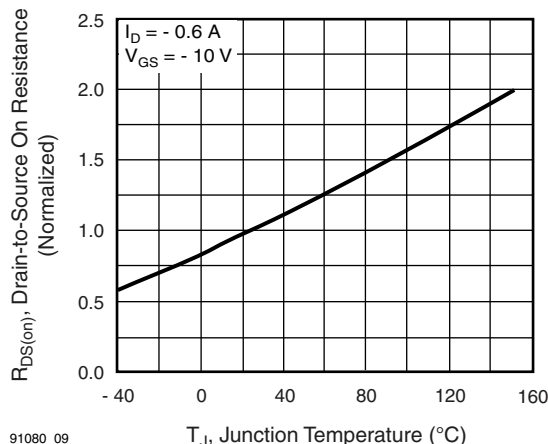
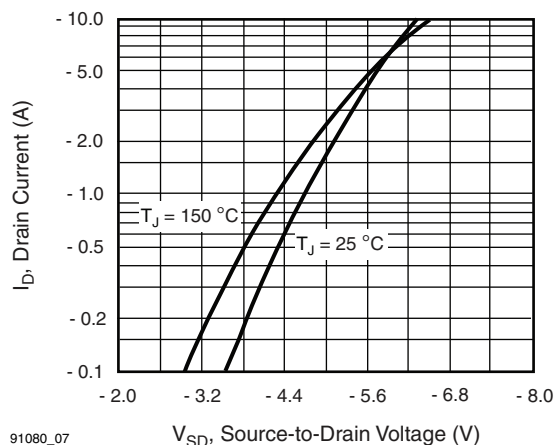
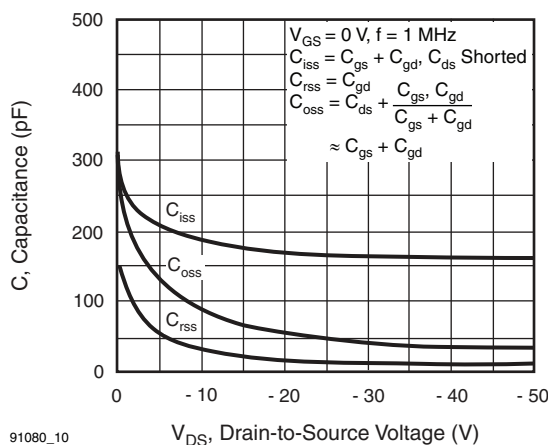
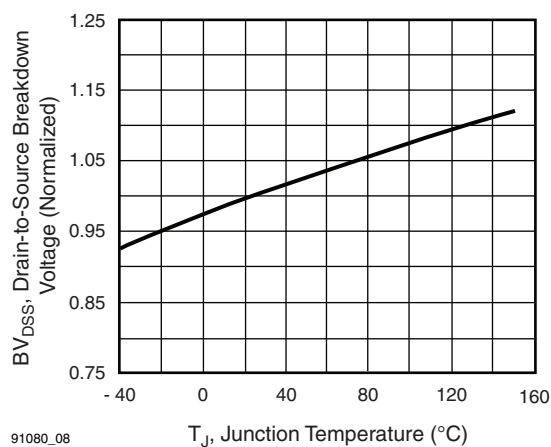
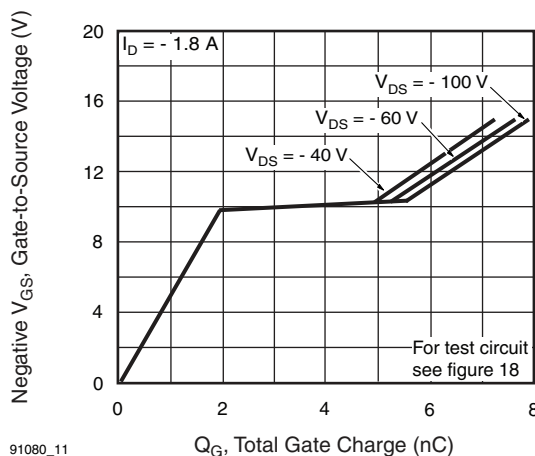
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

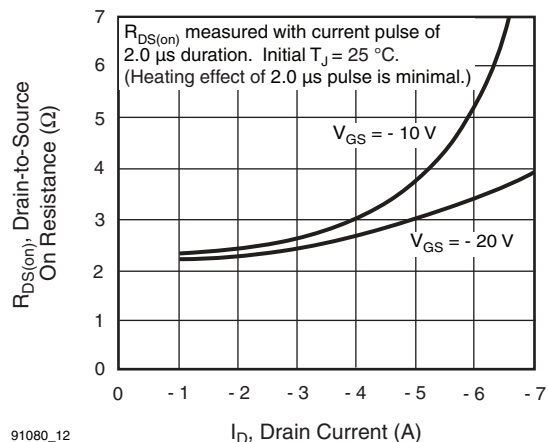
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA		-200	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA		-	-0.23	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -200 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	-500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -0.90 A ^b	-	-	3.0	Ω
Forward transconductance	g _{fs}	V _{DS} = -50 V, I _D = -0.90 A ^b		0.90	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 10		-	170	-	pF
Output capacitance	C _{oss}			-	50	-	
Reverse transfer capacitance	C _{rss}			-	15	-	
Total gate charge	Q _g	V _{GS} = -10 V	I _D = -3.5 A, V _{DS} = -160 V, see fig. 11 and 18 ^b	-	-	11	nC
Gate-source charge	Q _{gs}			-	-	7.0	
Gate-drain charge	Q _{gd}			-	-	4.0	
Turn-on delay time	t _{d(on)}	V _{DD} = -100 V, I _D = -0.90 A, R _g = 50 Ω, R _D = 110 Ω, see fig. 17 ^b		-	8.0	-	ns
Rise time	t _r			-	15	-	
Turn-off delay time	t _{d(off)}			-	10	-	
Fall time	t _f			-	8.0	-	
Gate input resistance	R _g	f = 1 MHz, open drain		2.5	-	14.3	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-1.8	A
Pulsed diode forward current ^a	I _{SM}			-	-	-7.0	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = -1.8 A, V _{GS} = 0 V ^b		-	-	-5.8	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = -1.8 A, dI/dt = 100 A/μs ^b		-	240	360	ns
Body diode reverse recovery charge	Q _{rr}			-	1.7	2.6	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

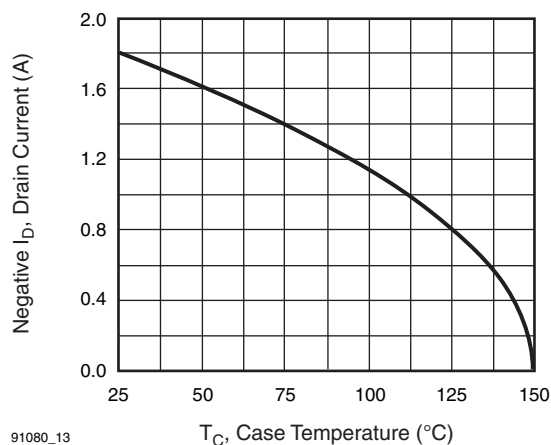
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Saturation Characteristics

Fig. 2 - Typical Transfer Characteristics

Fig. 4 - Maximum Safe Operating Area

Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

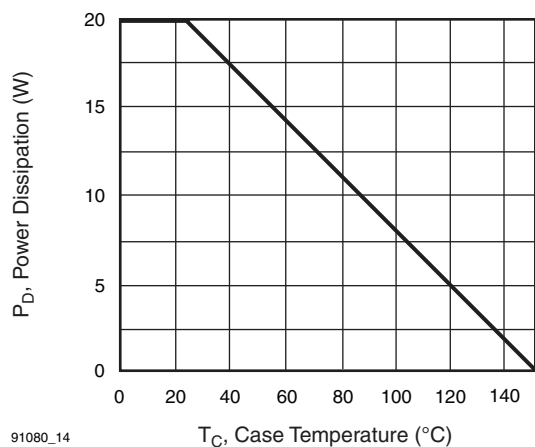

Fig. 6 - Typical Transconductance vs. Drain Current

Fig. 9 - Normalized On-Resistance vs. Temperature

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 8 - Breakdown Voltage vs. Temperature

Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage



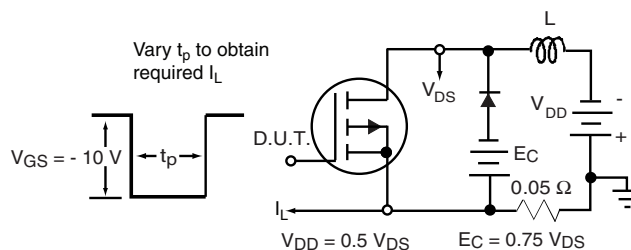
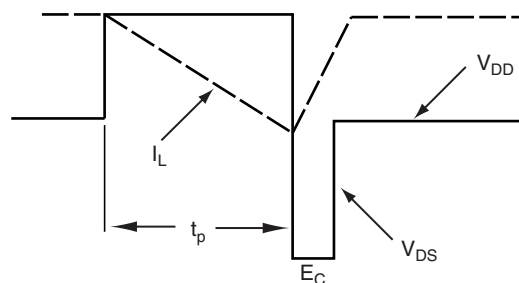
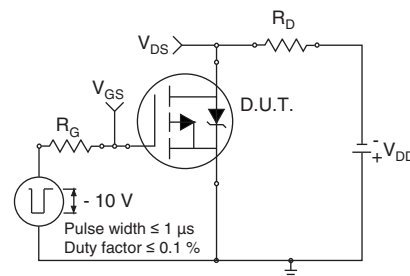
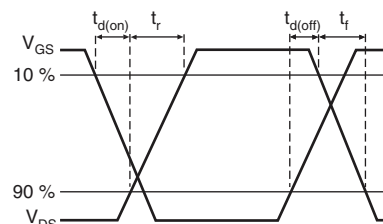
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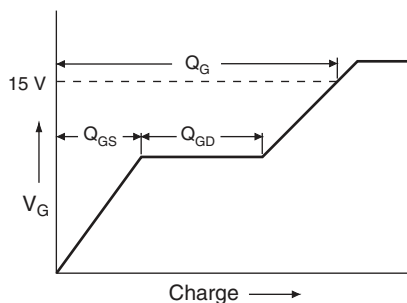
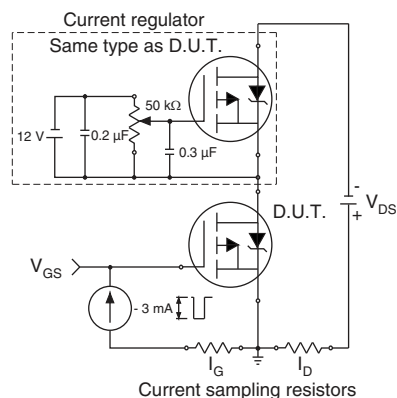
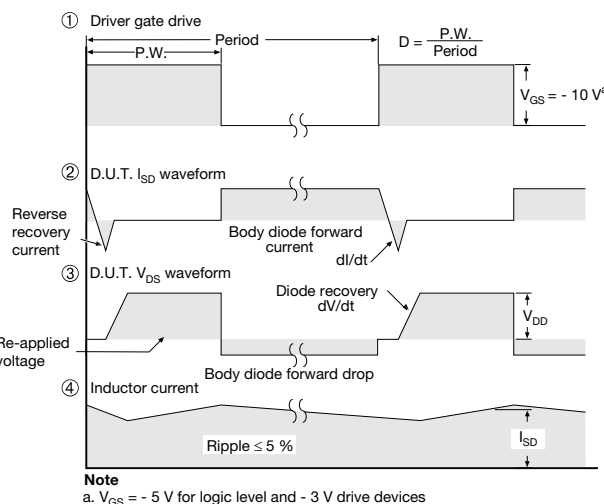
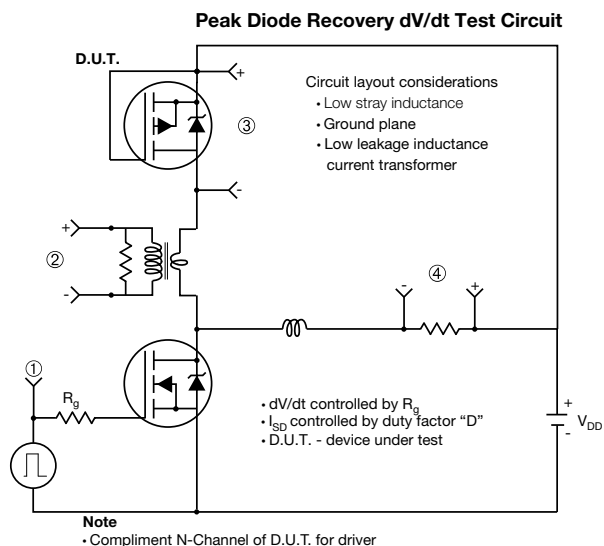
Fig. 12 - Typical On-Resistance vs. Drain Current


91080_13

Fig. 13 - Maximum Drain Current vs. Case Temperature


91080_14

Fig. 14 - Power vs. Temperature Derating Curve

Fig. 15 - Clamped Inductive Test Circuit

Fig. 16 - Clamped Inductive Waveforms

Fig. 17a - Switching Time Test Circuit

Fig. 17b - Switching Time Waveforms


Fig. 18a - Basic Gate Charge Waveform

Fig. 18b - Gate Charge Test Circuit

Fig. 19 - For P-Channel

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