
STM32
CubeMX

1. Description

1.1. Project

Project Name	ProgramWithBSP
Board Name	STM32L476G-DISCO
Generated with:	STM32CubeMX 6.5.0
Date	06/12/2022

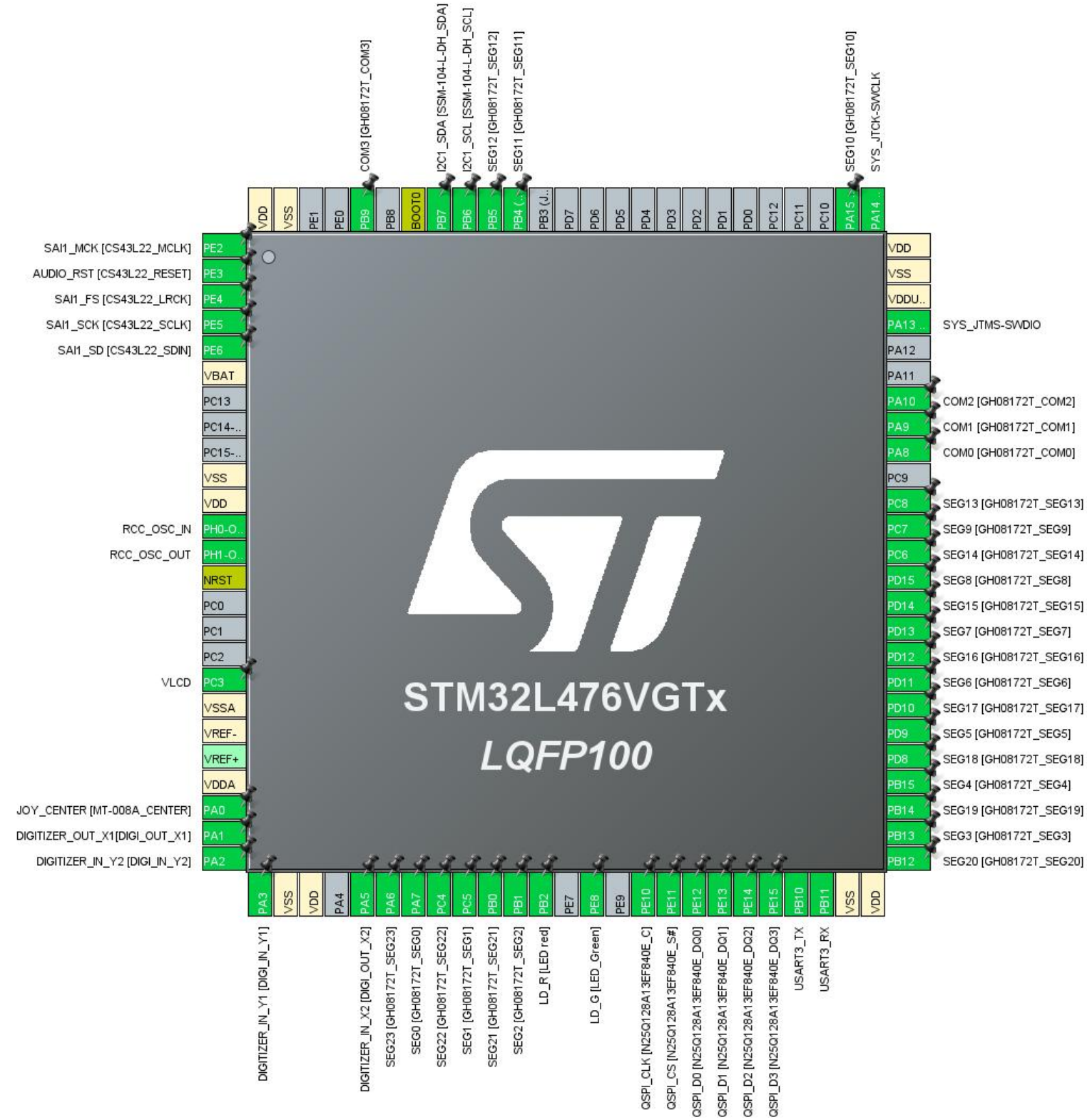
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

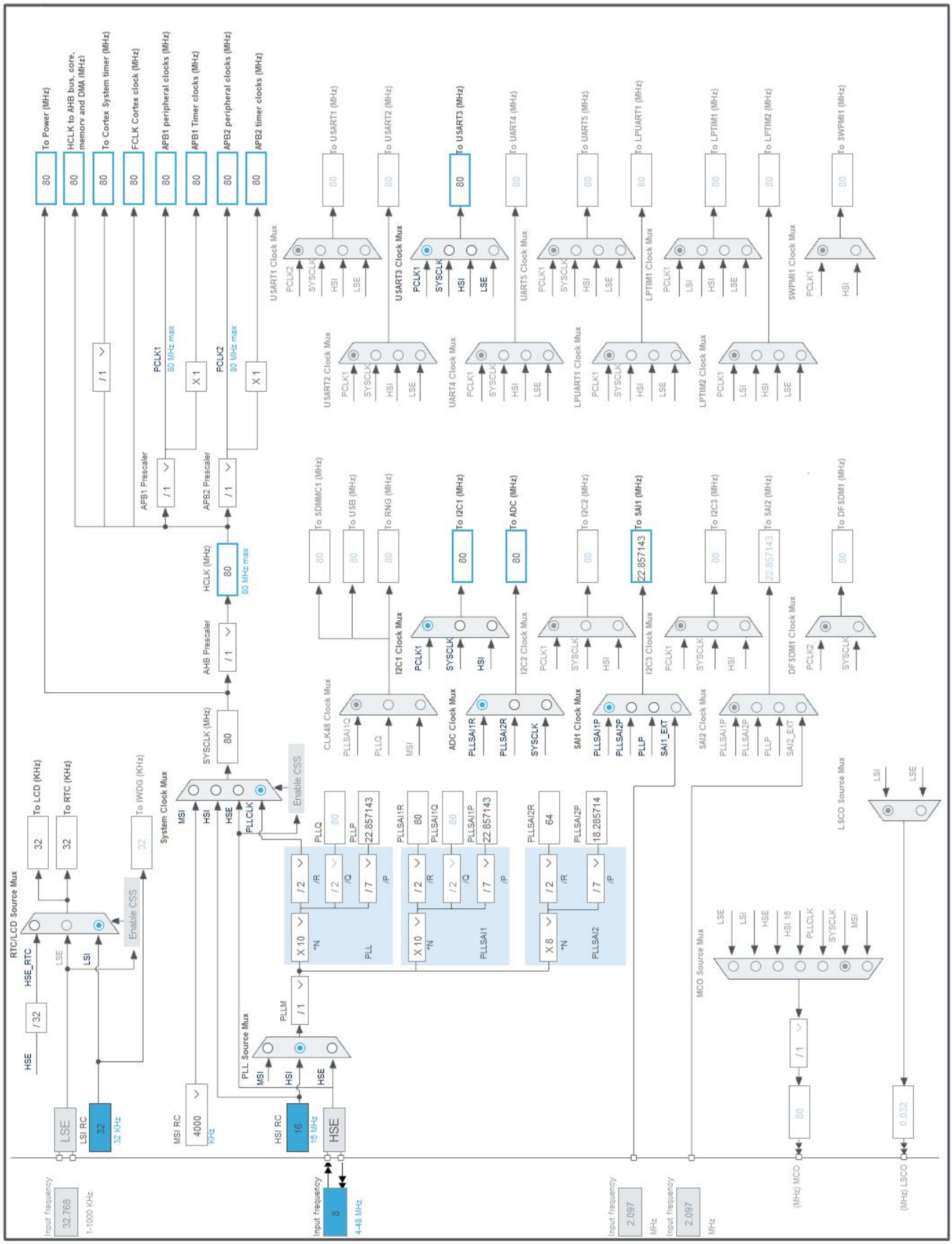
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SAI1_MCLK_A	SAI1_MCK [CS43L22_MCLK]
2	PE3 *	I/O	GPIO_Output	AUDIO_RST [CS43L22_RESET]
3	PE4	I/O	SAI1_FS_A	SAI1_FS [CS43L22_LRCK]
4	PE5	I/O	SAI1_SCK_A	SAI1_SCK [CS43L22_SCLK]
5	PE6	I/O	SAI1_SD_A	SAI1_SD [CS43L22_SDIN]
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
18	PC3	I/O	LCD_VLCD	VLCD
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0 *	I/O	GPIO_Input	JOY_CENTER [MT-008A_CENTER]
24	PA1 *	I/O	GPIO_Output	DIGITIZER_OUT_X1[DIGI_OUT_X1]
25	PA2 *	I/O	GPIO_Input	DIGITIZER_IN_Y2 [DIGI_IN_Y2]
26	PA3	I/O	ADC1_IN8	DIGITIZER_IN_Y1 [DIGI_IN_Y1]
27	VSS	Power		
28	VDD	Power		
30	PA5 *	I/O	GPIO_Output	DIGITIZER_IN_X2 [DIGI_OUT_X2]
31	PA6	I/O	LCD_SEG3	SEG23 [GH08172T_SEG23]
32	PA7	I/O	LCD_SEG4	SEG0 [GH08172T_SEG0]
33	PC4	I/O	LCD_SEG22	SEG22 [GH08172T_SEG22]
34	PC5	I/O	LCD_SEG23	SEG1 [GH08172T_SEG1]
35	PB0	I/O	LCD_SEG5	SEG21 [GH08172T_SEG21]
36	PB1	I/O	LCD_SEG6	SEG2 [GH08172T_SEG2]
37	PB2 *	I/O	GPIO_Output	LD_R [LED red]

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PE8 *	I/O	GPIO_Output	LD_G [LED_Green]
41	PE10	I/O	QUADSPI_CLK	QSPI_CLK [N25Q128A13EF840E_C]
42	PE11	I/O	QUADSPI_NCS	QSPI_CS [N25Q128A13EF840E_S#]
43	PE12	I/O	QUADSPI_BK1_IO0	QSPI_D0 [N25Q128A13EF840E_DQ0]
44	PE13	I/O	QUADSPI_BK1_IO1	QSPI_D1 [N25Q128A13EF840E_DQ1]
45	PE14	I/O	QUADSPI_BK1_IO2	QSPI_D2 [N25Q128A13EF840E_DQ2]
46	PE15	I/O	QUADSPI_BK1_IO3	QSPI_D3 [N25Q128A13EF840E_DQ3]
47	PB10	I/O	USART3_TX	
48	PB11	I/O	USART3_RX	
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	LCD_SEG12	SEG20 [GH08172T_SEG20]
52	PB13	I/O	LCD_SEG13	SEG3 [GH08172T_SEG3]
53	PB14	I/O	LCD_SEG14	SEG19 [GH08172T_SEG19]
54	PB15	I/O	LCD_SEG15	SEG4 [GH08172T_SEG4]
55	PD8	I/O	LCD_SEG28	SEG18 [GH08172T_SEG18]
56	PD9	I/O	LCD_SEG29	SEG5 [GH08172T_SEG5]
57	PD10	I/O	LCD_SEG30	SEG17 [GH08172T_SEG17]
58	PD11	I/O	LCD_SEG31	SEG6 [GH08172T_SEG6]
59	PD12	I/O	LCD_SEG32	SEG16 [GH08172T_SEG16]
60	PD13	I/O	LCD_SEG33	SEG7 [GH08172T_SEG7]
61	PD14	I/O	LCD_SEG34	SEG15 [GH08172T_SEG15]
62	PD15	I/O	LCD_SEG35	SEG8 [GH08172T_SEG8]
63	PC6	I/O	LCD_SEG24	SEG14 [GH08172T_SEG14]
64	PC7	I/O	LCD_SEG25	SEG9 [GH08172T_SEG9]
65	PC8	I/O	LCD_SEG26	SEG13 [GH08172T_SEG13]
67	PA8	I/O	LCD_COM0	COM0 [GH08172T_COM0]
68	PA9	I/O	LCD_COM1	COM1 [GH08172T_COM1]
69	PA10	I/O	LCD_COM2	COM2 [GH08172T_COM2]
72	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
73	VDDUSB	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	LCD_SEG17	SEG10 [GH08172T_SEG10]
90	PB4 (NJTRST)	I/O	LCD_SEG8	SEG11 [GH08172T_SEG11]
91	PB5	I/O	LCD_SEG9	SEG12 [GH08172T_SEG12]
92	PB6	I/O	I2C1_SCL	I2C1_SCL [SSM-104-L-DH_SCL]
93	PB7	I/O	I2C1_SDA	I2C1_SDA [SSM-104-L-DH_SDA]
94	BOOT0	Boot		
96	PB9	I/O	LCD_COM3	COM3 [GH08172T_COM3]
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	ProgramWithBSP
Project Folder	C:\Users\admin\Desktop\Uczelnia\semestr_6\SR\PalPer-main\ProgramWithBSP
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LCD_Init	LCD
4	MX_QUADSPI_Init	QUADSPI
5	MX_RTC_Init	RTC
6	MX_I2C1_Init	I2C1
7	MX_DMA_Init	DMA
8	MX_USART3_UART_Init	USART3
9	MX_SAI1_Init	SAI1
10	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476VGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

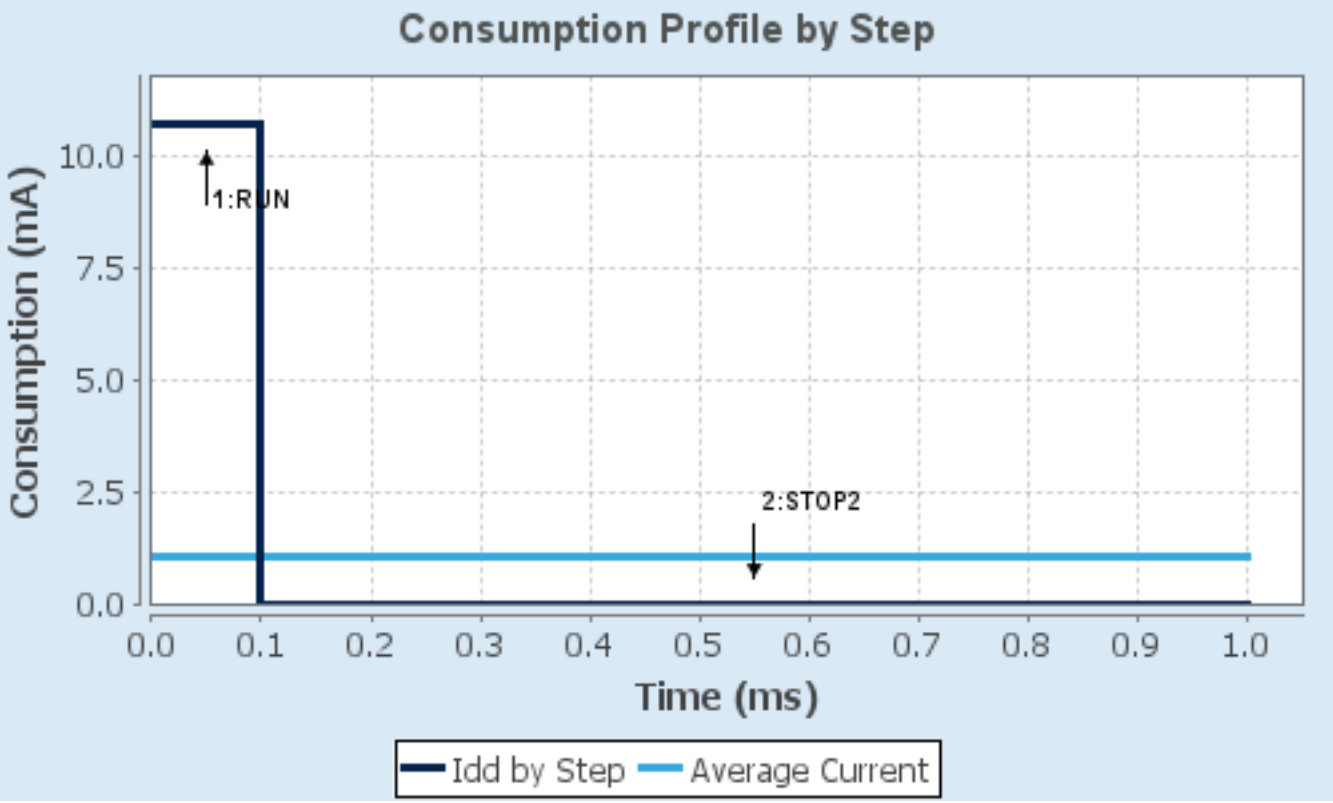
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.65	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN8: IN8 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 8-bit resolution ***
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 8
Sampling Time	**92.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10909CEC ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. LCD

Mode: 1/4 Duty Cycle

mode: SEG3

mode: SEG4

mode: SEG5

mode: SEG6

mode: SEG8

mode: SEG9

mode: SEG12

mode: SEG13

mode: SEG14

mode: SEG15

mode: SEG17

mode: SEG22

mode: SEG23

mode: SEG24

mode: SEG25
mode: SEG26
mode: SEG28
mode: SEG29
mode: SEG30
mode: SEG31
mode: SEG32
mode: SEG33
mode: SEG34
mode: SEG35

7.3.1. Parameter Settings:

Clock Parameters:

Clock Prescaler	1
Clock Divider	**31 ***

Basic Parameters:

Duty Selection	1/4
Bias Selector	**1/3 ***
Multiplex mode	Disable

Advanced Parameters:

Voltage Source Selection	Internal
Contrast Control	**2.86V ***
Dead Time Duration	No dead Time
High Drive	Disable
Pulse ON Duration	**4/CK_PS ***
Blink Mode	Disabled
Blink Frequency	**fLCD/32 ***

7.4. QUADSPI

Single Bank: Quad SPI Line

7.4.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	**4 ***
Sample Shifting	**Sample Shifting Half Cycle ***

Flash Size	**24 ***
Chip Select High Time	1 Cycle
Clock Mode	Low

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.6. RTC

mode: Activate Clock Source

7.6.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.7. SAI1

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

7.7.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Basic Parameters	
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	**44.1 KHz ***
Real Audio Frequency	**44.642 KHz ***
Error between Selected	**1.45 % ***
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

7.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.9. USART3

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN8	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	DIGITIZER_IN_Y1 [DIGI_IN_Y1]
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C1_SCL [SSM-104-L-DH_SCL]
	PB7	I2C1_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C1_SDA [SSM-104-L-DH_SDA]
LCD	PC3	LCD_VLCD	Alternate Function Push Pull	No pull-up and no pull-down	Low	VLCD
	PA6	LCD_SEG3	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG23 [GH08172T_SEG23]
	PA7	LCD_SEG4	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG0 [GH08172T_SEG0]
	PC4	LCD_SEG22	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG22 [GH08172T_SEG22]
	PC5	LCD_SEG23	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG1 [GH08172T_SEG1]
	PB0	LCD_SEG5	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG21 [GH08172T_SEG21]
	PB1	LCD_SEG6	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG2 [GH08172T_SEG2]
	PB12	LCD_SEG12	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG20 [GH08172T_SEG20]
	PB13	LCD_SEG13	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG3 [GH08172T_SEG3]
	PB14	LCD_SEG14	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG19 [GH08172T_SEG19]
	PB15	LCD_SEG15	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG4 [GH08172T_SEG4]
	PD8	LCD_SEG28	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG18 [GH08172T_SEG18]
	PD9	LCD_SEG29	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG5 [GH08172T_SEG5]
	PD10	LCD_SEG30	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG17 [GH08172T_SEG17]
	PD11	LCD_SEG31	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG6 [GH08172T_SEG6]
	PD12	LCD_SEG32	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG16 [GH08172T_SEG16]
	PD13	LCD_SEG33	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG7 [GH08172T_SEG7]
	PD14	LCD_SEG34	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG15 [GH08172T_SEG15]
	PD15	LCD_SEG35	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG8 [GH08172T_SEG8]
	PC6	LCD_SEG24	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG14 [GH08172T_SEG14]
	PC7	LCD_SEG25	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG9 [GH08172T_SEG9]
	PC8	LCD_SEG26	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG13

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						[GH08172T_SEG13]
	PA8	LCD_COM0	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM0 [GH08172T_COM0]
	PA9	LCD_COM1	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM1 [GH08172T_COM1]
	PA10	LCD_COM2	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM2 [GH08172T_COM2]
	PA15 (JTDI)	LCD_SEG17	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG10 [GH08172T_SEG10]
	PB4 (NJTRST)	LCD_SEG8	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG11 [GH08172T_SEG11]
	PB5	LCD_SEG9	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG12 [GH08172T_SEG12]
	PB9	LCD_COM3	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM3 [GH08172T_COM3]
QUADSPI	PE10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_CLK [N25Q128A13EF840E_C]
	PE11	QUADSPI_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_CS [N25Q128A13EF840E_S#]
	PE12	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D0 [N25Q128A13EF840E_DQ0]
	PE13	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D1 [N25Q128A13EF840E_DQ1]
	PE14	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D2 [N25Q128A13EF840E_DQ2]
	PE15	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D3 [N25Q128A13EF840E_DQ3]
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SAI1	PE2	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_MCK [CS43L22_MCLK]
	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_FS [CS43L22_LRCK]
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_SCK [CS43L22_SCLK]
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SAI1_SD [CS43L22_SDIN]
SYS	PA13	SYS_JTMS-	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	(JTMS-SWDIO)	SWDIO				
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	AUDIO_RST [CS43L22_RESET]
	PA0	GPIO_Input	Input mode	**Pull-down ***	**n/a**	JOY_CENTER [MT-008A_CENTER]
	PA1	GPIO_Output	Output Push Pull	**Pull-up ***	Low	DIGITIZER_OUT_X1[DIGI_OUT_X1]
	PA2	GPIO_Input	Input mode	**Pull-down ***	n/a	DIGITIZER_IN_Y2 [DIGI_IN_Y2]
	PA5	GPIO_Output	Output Push Pull	**Pull-down ***	Low	DIGITIZER_IN_X2 [DIGI_OUT_X2]
	PB2	GPIO_Output	Output Push Pull	**Pull-up ***	**Very High ***	LD_R [LED red]
	PE8	GPIO_Output	Output Push Pull	**Pull-up ***	**Very High ***	LD_G [LED_Green]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SAI1_A	DMA2_Channel1	Memory To Peripheral	Low

SAI1_A: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
ADC1 and ADC2 interrupts	true	0	0
USART3 global interrupt	true	0	0
DMA2 channel1 global interrupt	true	0	0
SAI1 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
QUADSPI global interrupt	unused		
LCD global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
ADC1 and ADC2 interrupts	false	true	true
USART3 global interrupt	false	true	true

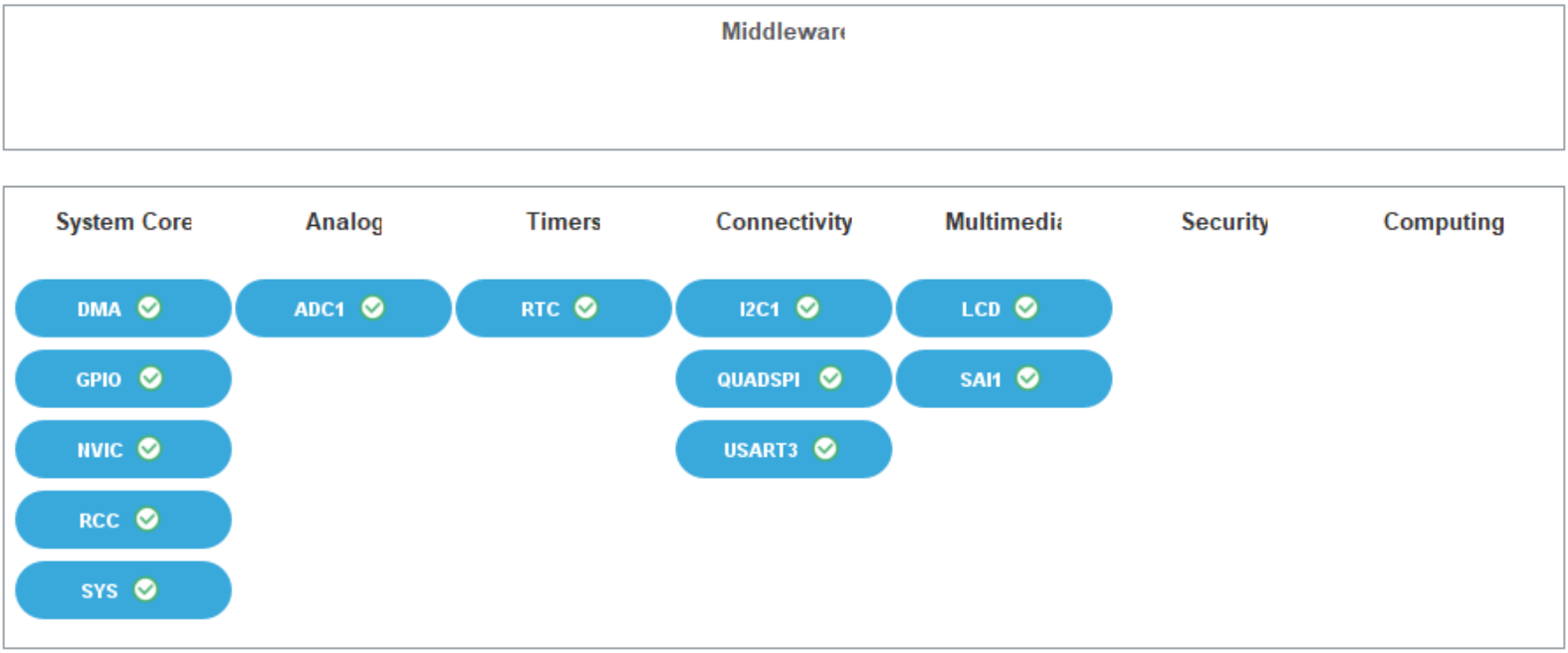
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA2 channel1 global interrupt	false	true	true
SAI1 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link