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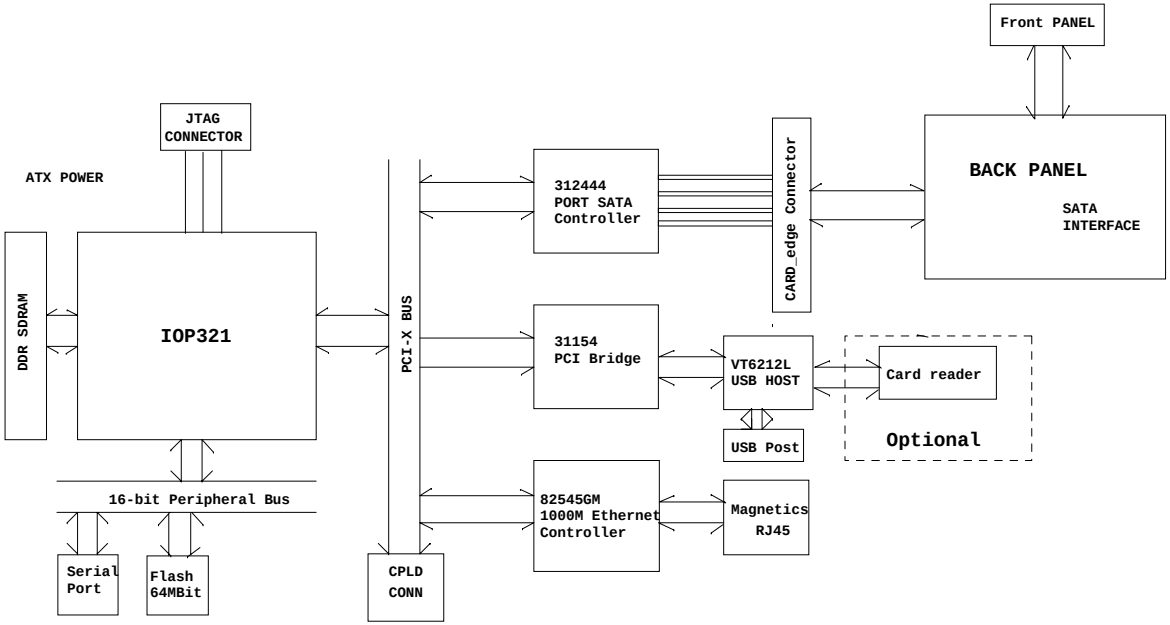

Title: Title page		
Size: C	Document Number: USI DHNSIN01 CONFIDENTIAL	Rev: 2.1
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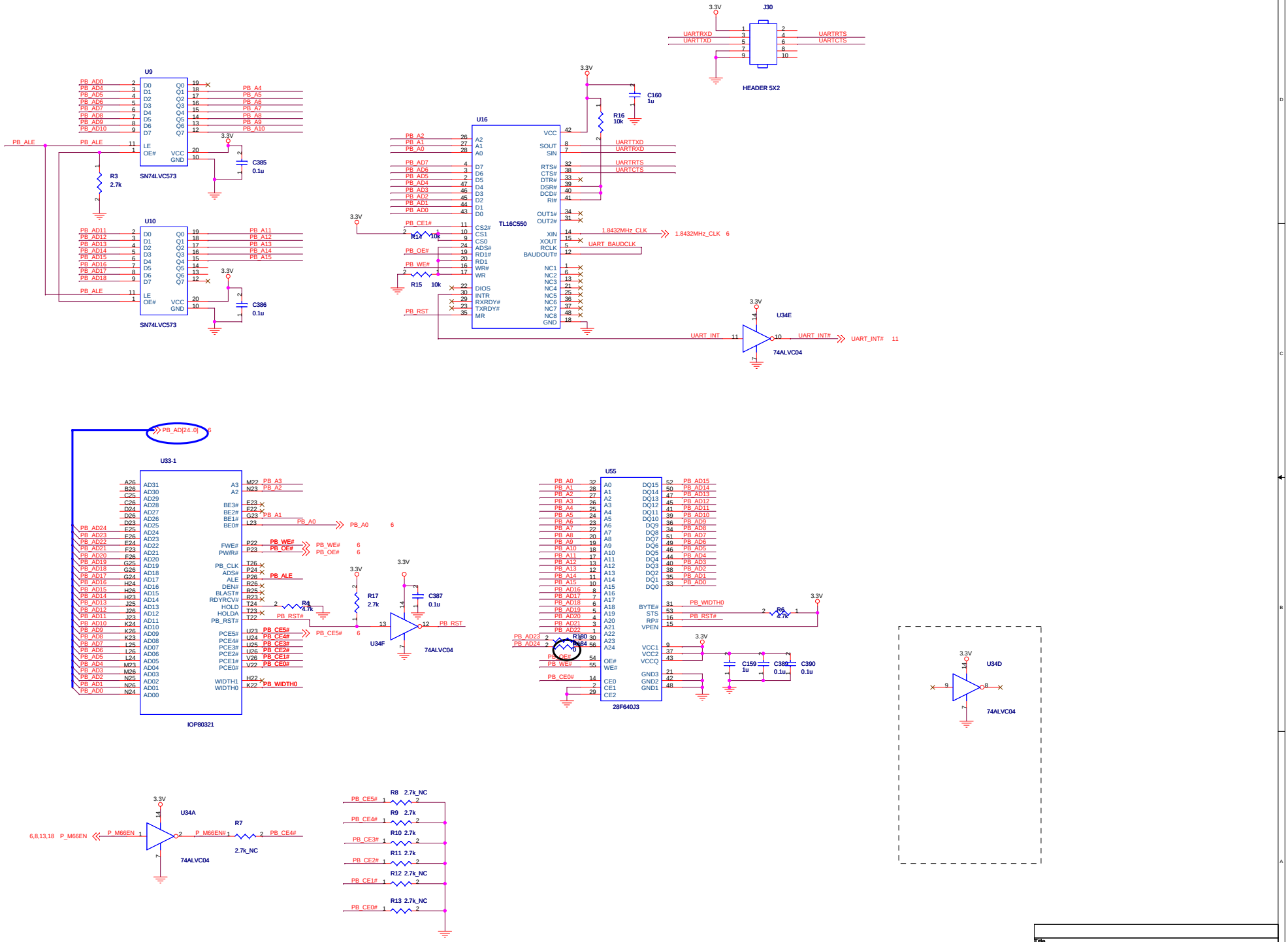

Title	80321_PDI & COM & Flash	
Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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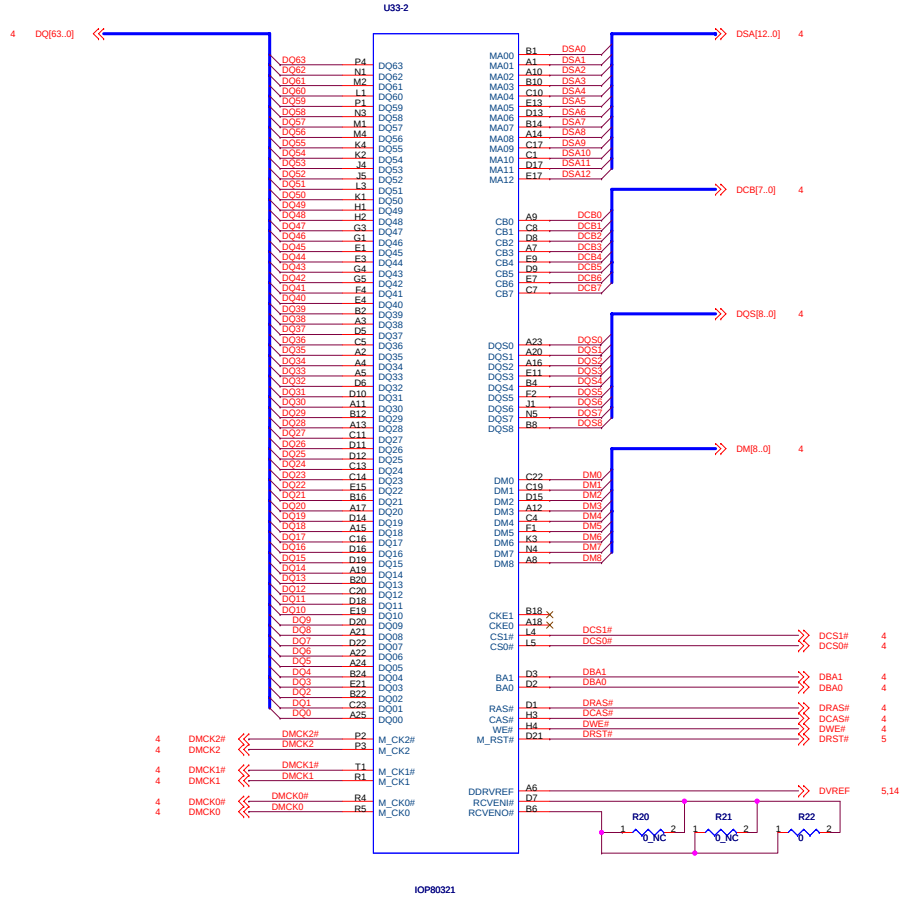

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Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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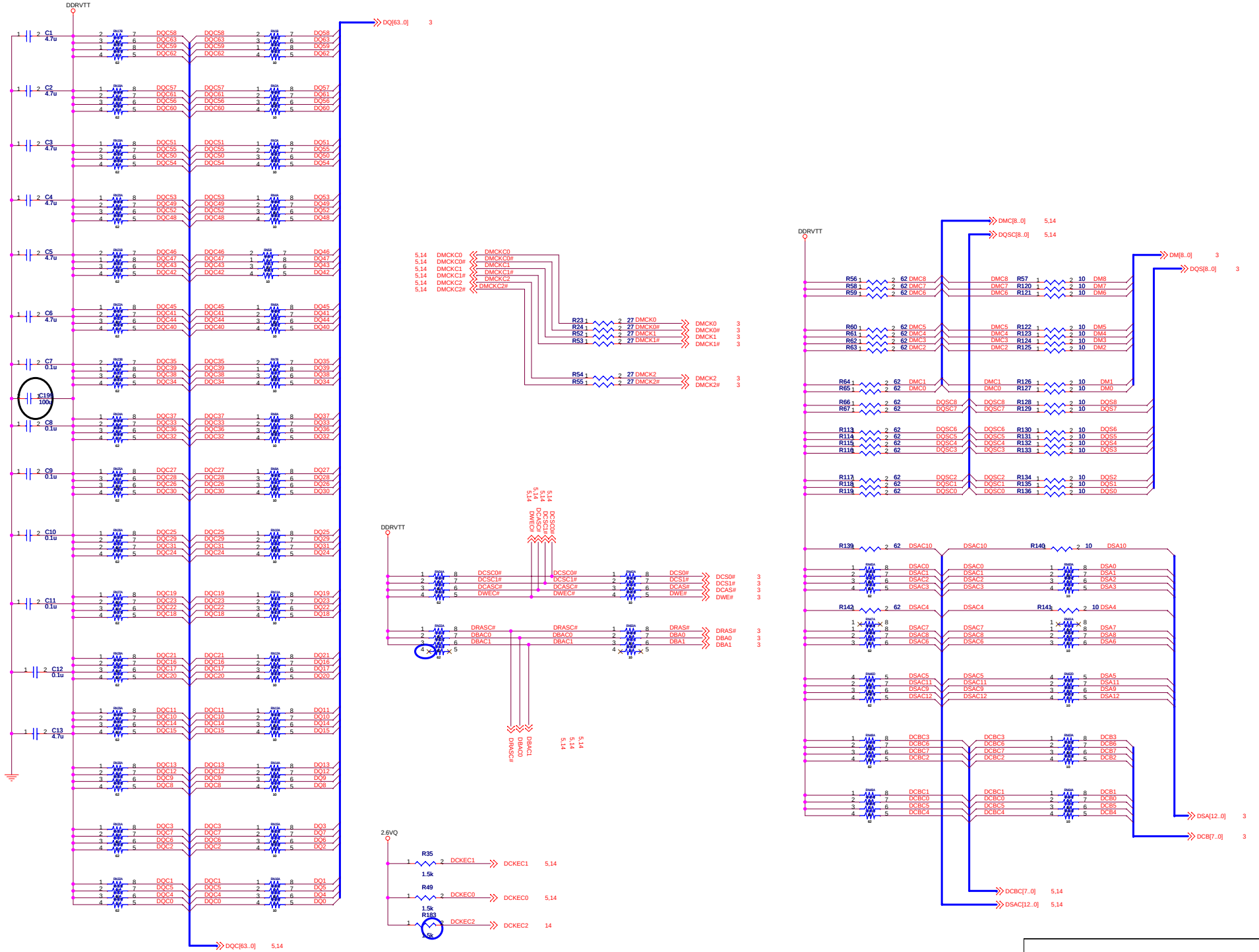

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Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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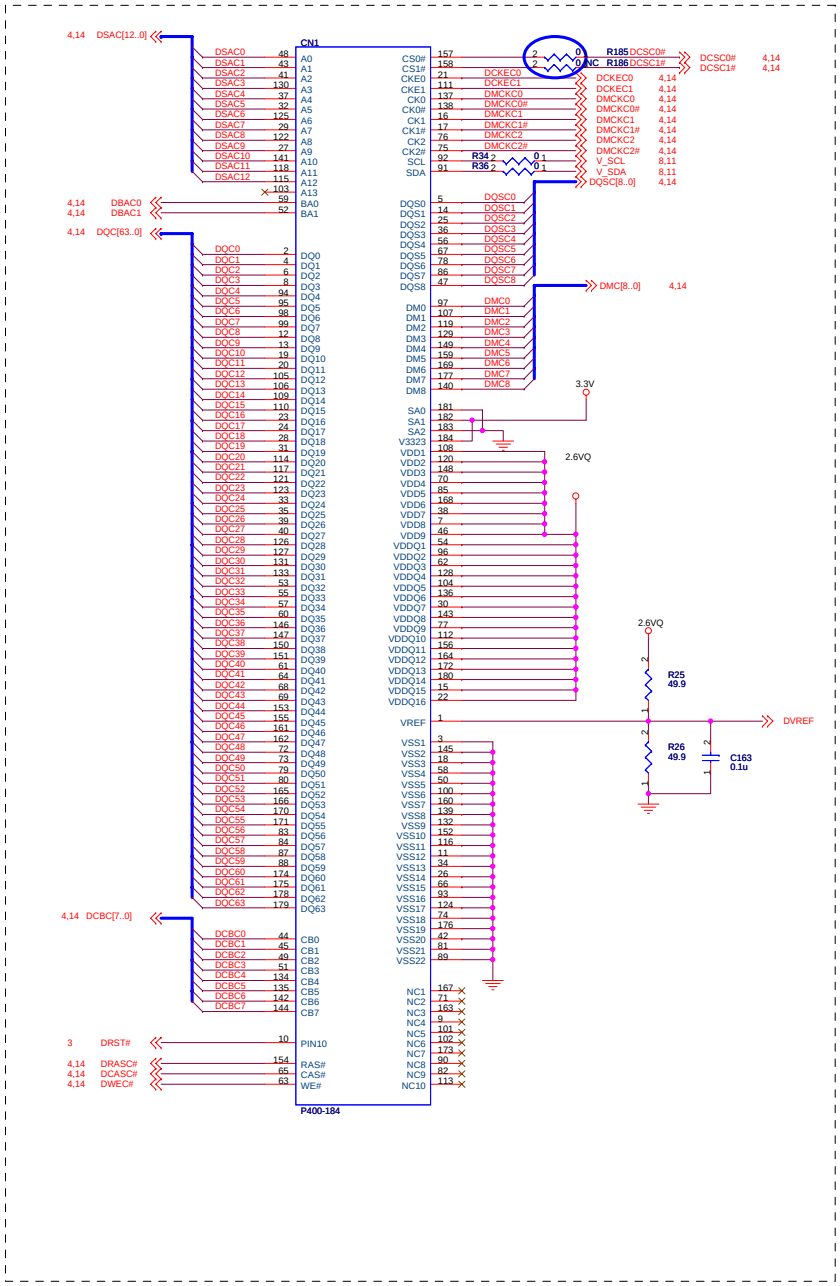

Title	DIMM connector	
Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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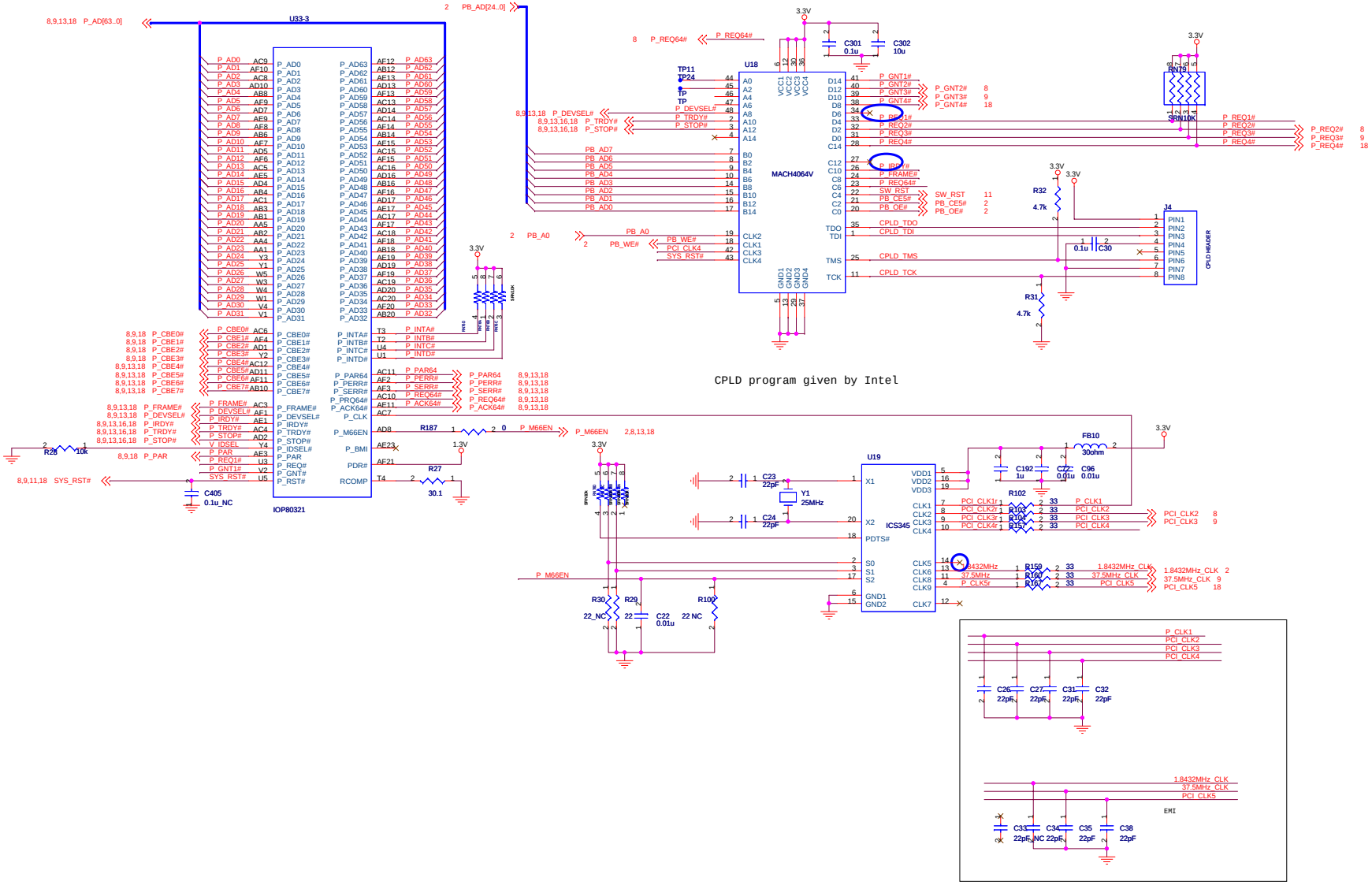

Title	80321_PCI&CLK GEN		
Size C	Document Number USI DHNSIN01 CONFIDENTIAL		Rev 2.1
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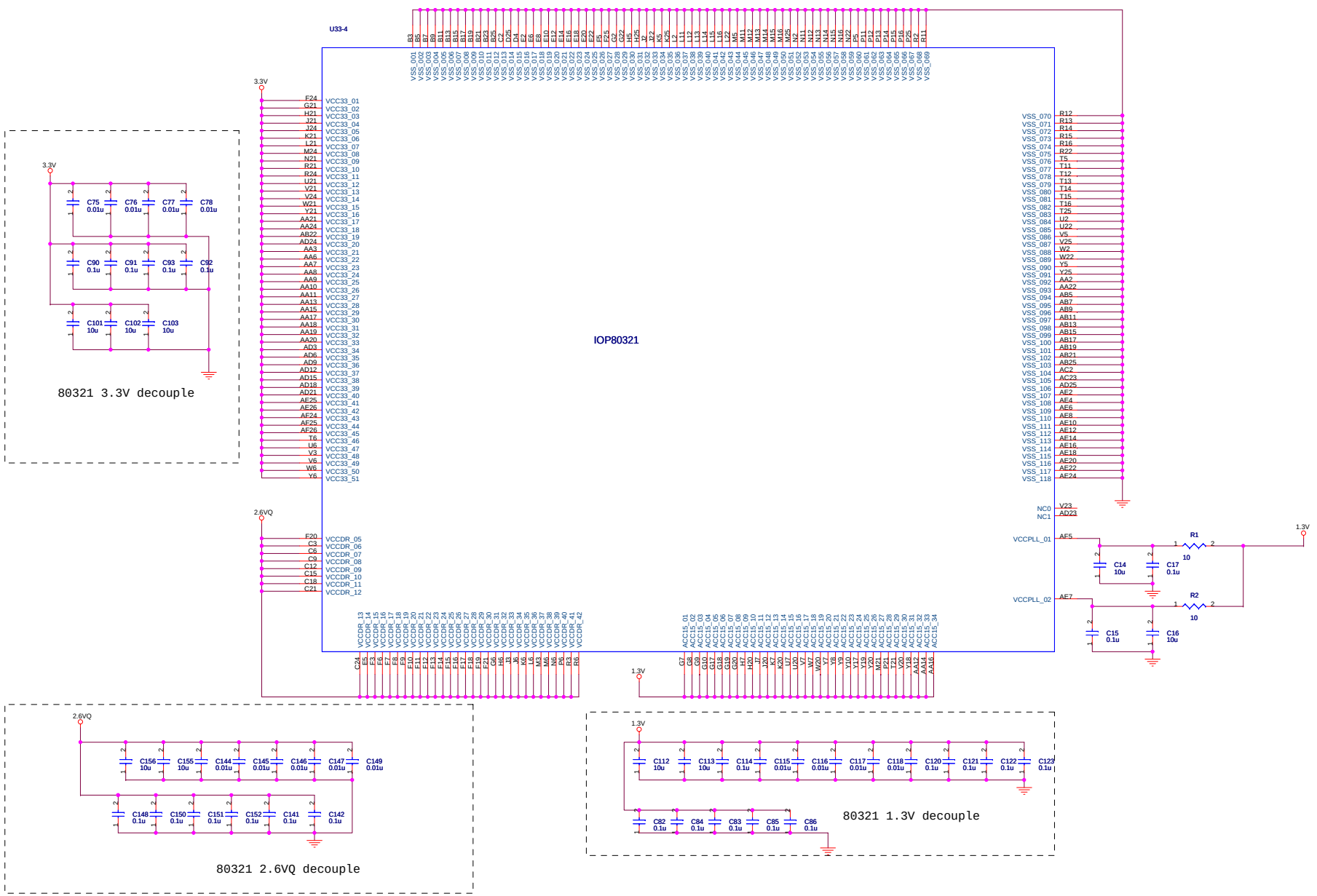

Title	80321_PWR&GND	
Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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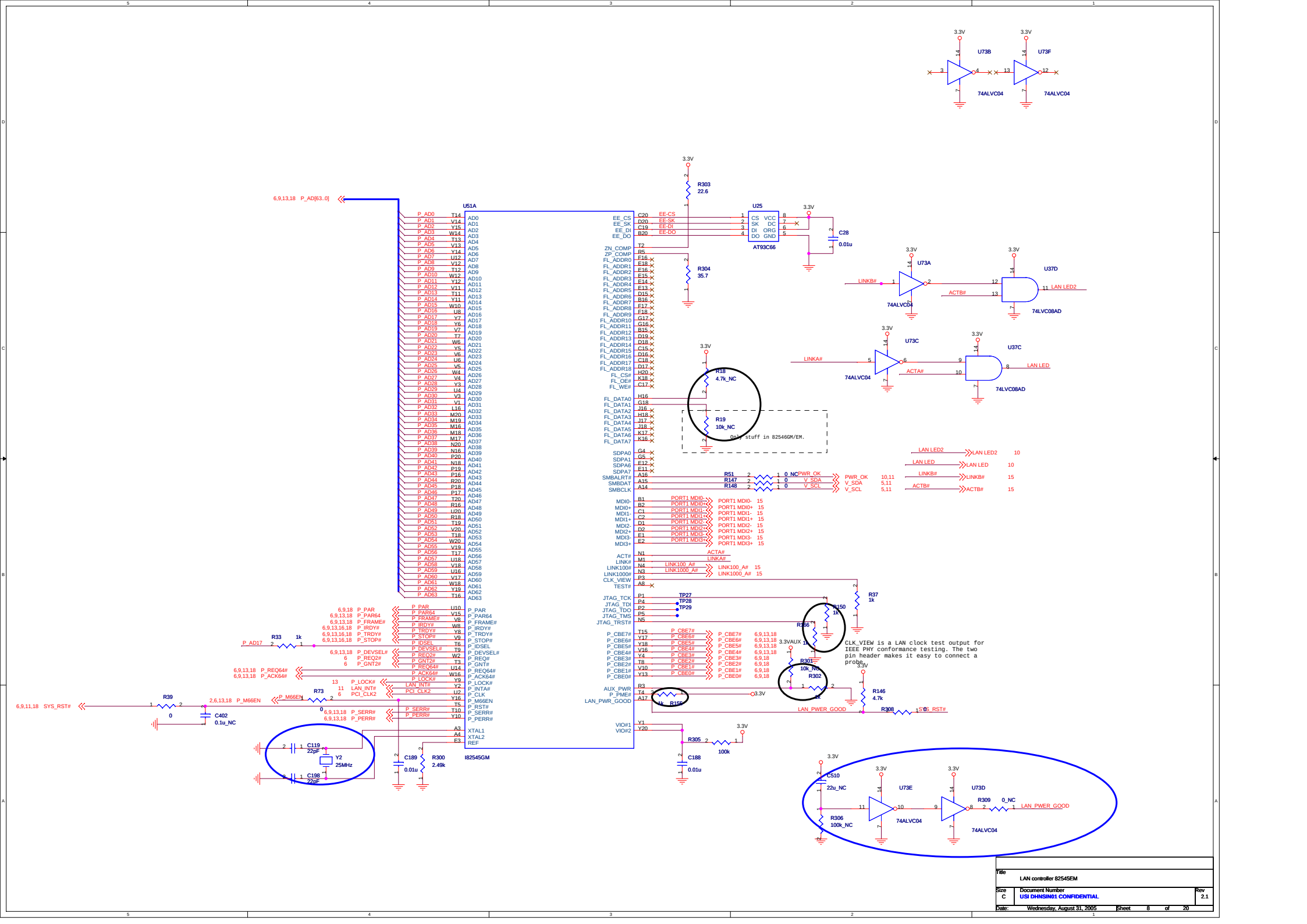
U51A
I82545GM
U25
AT93C66
U73A
U73B
U73C
U73D
U73E
U73F
74ALVC04
74LVC08AD
R303 22.6
R304 35.7
R18 4.7k_NC
R19 10k_NC
Only stuff in 82546GM/EM.
R33 1k
R39 0
R73 0
C402 0.1u_NC
C119 22pF
C198 22pF
Y2 25MHz
C189 0.01u
R300 2.49k
C188 0.01u
R305 100k
C28 0.01u
R37 1k
R150 1k
R301 10k_NC
R302 43
R155 1k
R146 4.7k
R308 0
C510 22u_NC
R306 100k_NC
R309 0_NC
CLK_VIEW is a LAN clock test output for IEEE PHY conformance testing. The two pin header makes it easy to connect a probe.
Title
LAN controller 82545EM
Size C
Document Number
USI DHNSIN01 CONFIDENTIAL
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Date: Wednesday, August 31, 2005
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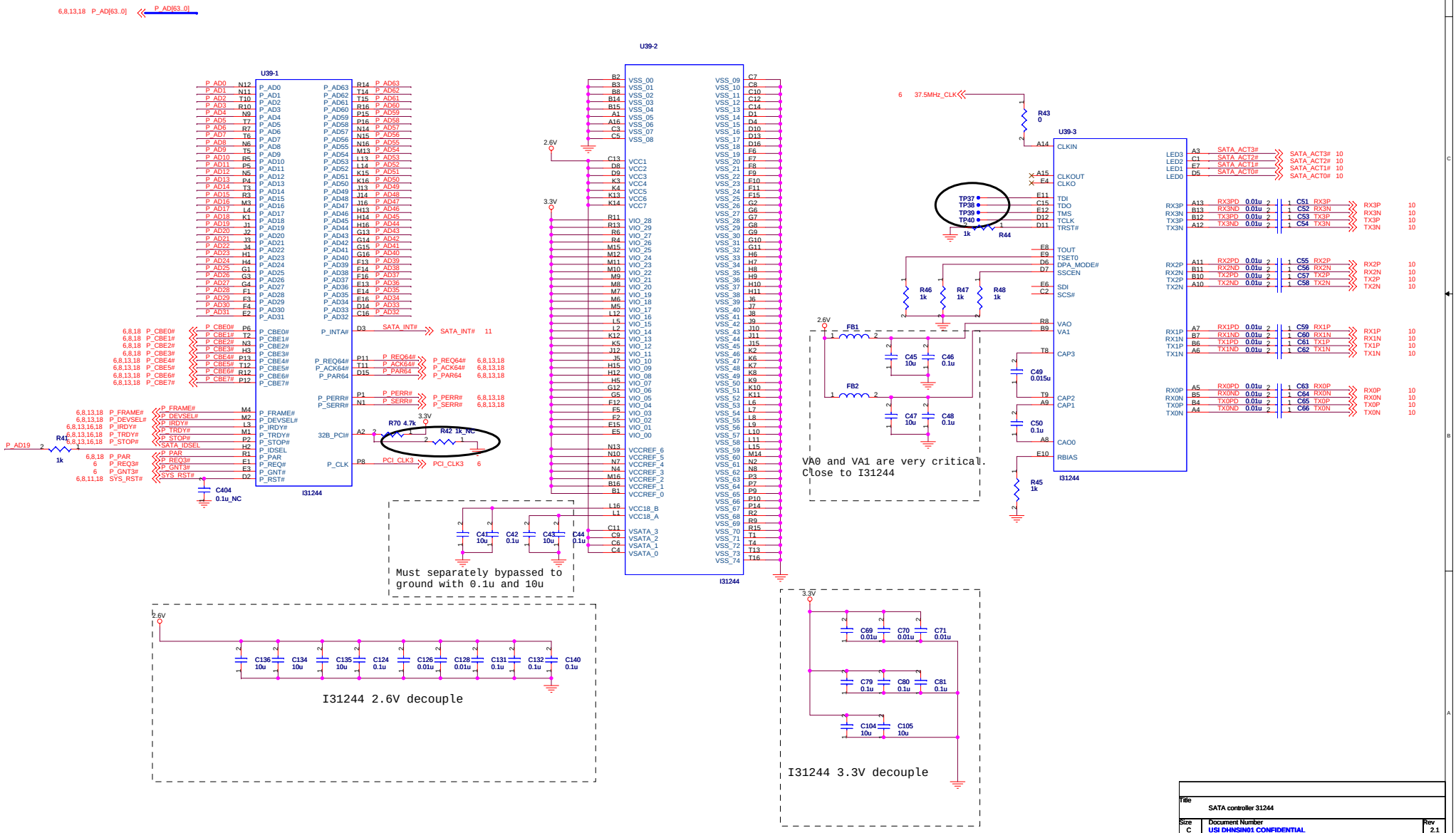
6,8,13,18 P_AD[63..0]
P_AD[63..0]
U39-1
U39-2
U39-3
I31244
P_AD0 N12
P_AD1 N11
P_AD2 T10
P_AD3 R10
P_AD4 N9
P_AD5 T7
P_AD6 R7
P_AD7 T6
P_AD8 N6
P_AD9 T5
P_AD10 R5
P_AD11 P5
P_AD12 N5
P_AD13 P4
P_AD14 T3
P_AD15 R3
P_AD16 M3
P_AD17 L4
P_AD18 K1
P_AD19 J1
P_AD20 J2
P_AD21 J3
P_AD22 J4
P_AD23 H1
P_AD24 H4
P_AD25 G1
P_AD26 G3
P_AD27 G4
P_AD28 F1
P_AD29 F3
P_AD30 F4
P_AD31 E2
P_AD63 R14
P_AD62 T14
P_AD61 T15
P_AD60 R16
P_AD59 P15
P_AD58 P16
P_AD57 N14
P_AD56 N15
P_AD55 N16
P_AD54 M13
P_AD53 L13
P_AD52 L14
P_AD51 K15
P_AD50 K16
P_AD49 J13
P_AD48 J14
P_AD47 J16
P_AD46 H13
P_AD45 H14
P_AD44 H16
P_AD43 G13
P_AD42 G14
P_AD41 G15
P_AD40 G16
P_AD39 F13
P_AD38 F14
P_AD37 F16
P_AD36 E13
P_AD35 E14
P_AD34 E16
P_AD33 D14
P_AD32 C16
6,8,18 P_CBE0# P6
6,8,18 P_CBE1# T2
6,8,18 P_CBE2# N3
6,8,18 P_CBE3# H3
6,8,13,18 P_CBE4# P13
6,8,13,18 P_CBE5# T12
6,8,13,18 P_CBE6# R12
6,8,13,18 P_CBE7# P12
P_CBE0#
P_CBE1#
P_CBE2#
P_CBE3#
P_CBE4#
P_CBE5#
P_CBE6#
P_CBE7#
P_INTA# D3
SATA_INT# SATA_INT# 11
P_REQ64# P11
P_ACK64# T11
P_PAR64 D15
P_REQ64# 6,8,13,18
P_ACK64# 6,8,13,18
P_PAR64 6,8,13,18
P_PERR# P1
P_SERR# N1
P_PERR# 6,8,13,18
P_SERR# 6,8,13,18
32B_PCI# A2
P_CLK P8
PCI_CLK3 PCI_CLK3 6
6,8,13,18 P_FRAME# M4
6,8,13,18 P_DEVSEL# M2
6,8,13,16,18 P_IRDY# L3
6,8,13,16,18 P_TRDY# M1
6,8,13,16,18 P_STOP# P2
SATA_IDSEL H2
6,8,18 P_PAR R1
6 P_REQ3# E1
6 P_GNT3# E3
6,8,11,18 SYS_RST# D2
P_FRAME#
P_DEVSEL#
P_IRDY#
P_TRDY#
P_STOP#
P_IDSEL
P_PAR
P_REQ#
P_GNT#
P_RST#
P_AD19
R41 1k
C404 0.1u_NC
R70 4.7k
R42 1k_NC
3.3V
2.6V
VSS_00 B2
VSS_01 B3
VSS_02 B8
VSS_03 B14
VSS_04 B15
VSS_05 A1
VSS_06 A16
VSS_07 C3
VSS_08 C5
VCC1 C13
VCC2 D8
VCC3 D9
VCC4 K3
VCC5 K4
VCC6 K13
VCC7 K14
VIO_28 R11
VIO_29 R13
VIO_27 R6
VIO_26 R4
VIO_25 M15
VIO_24 M12
VIO_23 M11
VIO_22 M10
VIO_21 M9
VIO_20 M8
VIO_19 M7
VIO_18 M6
VIO_17 M5
VIO_16 L12
VIO_15 L5
VIO_14 L2
VIO_13 K12
VIO_12 K5
VIO_11 J12
VIO_10 J5
VIO_09 H15
VIO_08 H12
VIO_07 H5
VIO_06 G12
VIO_05 G5
VIO_04 F12
VIO_03 F5
VIO_02 F2
VIO_01 E15
VIO_00 E5
VCCREF_6 N13
VCCREF_5 N10
VCCREF_4 N7
VCCREF_3 N4
VCCREF_2 M16
VCCREF_1 B16
VCCREF_0 B1
VCC18_B L16
VCC18_A L1
VSATA_3 C11
VSATA_2 C9
VSATA_1 C6
VSATA_0 C4
VSS_09 C7
VSS_10 C8
VSS_11 C10
VSS_12 C12
VSS_13 C14
VSS_14 D1
VSS_15 D4
VSS_16 D10
VSS_17 D13
VSS_18 D16
VSS_19 F6
VSS_20 F7
VSS_21 F8
VSS_22 F9
VSS_23 F10
VSS_24 F11
VSS_25 F15
VSS_26 G2
VSS_27 G6
VSS_28 G7
VSS_29 G8
VSS_30 G9
VSS_31 G10
VSS_32 G11
VSS_33 H6
VSS_34 H7
VSS_35 H8
VSS_36 H9
VSS_37 H10
VSS_38 H11
VSS_39 J6
VSS_40 J7
VSS_41 J8
VSS_42 J9
VSS_43 J10
VSS_44 J11
VSS_45 J15
VSS_46 K2
VSS_47 K6
VSS_48 K7
VSS_49 K8
VSS_50 K9
VSS_51 K10
VSS_52 K11
VSS_53 L6
VSS_54 L7
VSS_55 L8
VSS_56 L9
VSS_57 L10
VSS_58 L11
VSS_59 L15
VSS_60 M14
VSS_61 N2
VSS_62 N8
VSS_63 P3
VSS_64 P7
VSS_65 P9
VSS_66 P10
VSS_67 P14
VSS_68 R2
VSS_69 R9
VSS_70 R15
VSS_71 T1
VSS_72 T4
VSS_73 T13
VSS_74 T16
C41 10u
C42 0.1u
C43 10u
C44 0.1u
Must separately bypassed to ground with 0.1u and 10u
2.6V
C136 10u
C134 10u
C135 10u
C124 0.1u
C126 0.01u
C128 0.01u
C131 0.1u
C132 0.1u
C140 0.1u
I31244 2.6V decouple
6 37.5MHz_CLK
R43 0
A14 CLKIN
A15 CLKOUT
E4 CLKO
TP37
TP38
TP39
TP40
R44 1k
E11 TDI
C15 TDO
E12 TMS
D12 TCLK
D11 TRST#
E8 TOUT
E9 TSET0
D6 DPA_MODE#
D7 SSCEN
E6 SDI
C2 SCS#
R46 1k
R47 1k
R48 1k
R9 VAO
B9 VA1
T8 CAP3
T9 CAP2
A9 CAP1
A8 CAO0
E10 RBIAS
R45 1k
FB1
FB2
C45 10u
C46 0.1u
C47 10u
C48 0.1u
C49 0.015u
C50 0.1u
VA0 and VA1 are very critical. Close to I31244
LED3 A3 SATA_ACT3#
LED2 C1 SATA_ACT2#
LED1 E7 SATA_ACT1#
LED0 D5 SATA_ACT0#
SATA_ACT3# 10
SATA_ACT2# 10
SATA_ACT1# 10
SATA_ACT0# 10
RX3P A13 RX3PD 0.01u
RX3N B13 RX3ND 0.01u
TX3P B12 TX3PD 0.01u
TX3N A12 TX3ND 0.01u
C51 RX3P
C52 RX3N
C53 TX3P
C54 TX3N
RX2P A11 RX2PD 0.01u
RX2N B11 RX2ND 0.01u
TX2P B10 TX2PD 0.01u
TX2N A10 TX2ND 0.01u
C55 RX2P
C56 RX2N
C57 TX2P
C58 TX2N
RX1P A7 RX1PD 0.01u
RX1N B7 RX1ND 0.01u
TX1P B6 TX1PD 0.01u
TX1N A6 TX1ND 0.01u
C59 RX1P
C60 RX1N
C61 TX1P
C62 TX1N
RX0P A5 RX0PD 0.01u
RX0N B5 RX0ND 0.01u
TX0P B4 TX0PD 0.01u
TX0N A4 TX0ND 0.01u
C63 RX0P
C64 RX0N
C65 TX0P
C66 TX0N
RX3P 10
RX3N 10
TX3P 10
TX3N 10
RX2P 10
RX2N 10
TX2P 10
TX2N 10
RX1P 10
RX1N 10
TX1P 10
TX1N 10
RX0P 10
RX0N 10
TX0P 10
TX0N 10
C69 0.01u
C70 0.01u
C71 0.01u
C79 0.1u
C80 0.1u
C81 0.1u
C104 10u
C105 10u
I31244 3.3V decouple
Title
SATA controller 31244
Size C
Document Number
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Date: Wednesday, August 31, 2005
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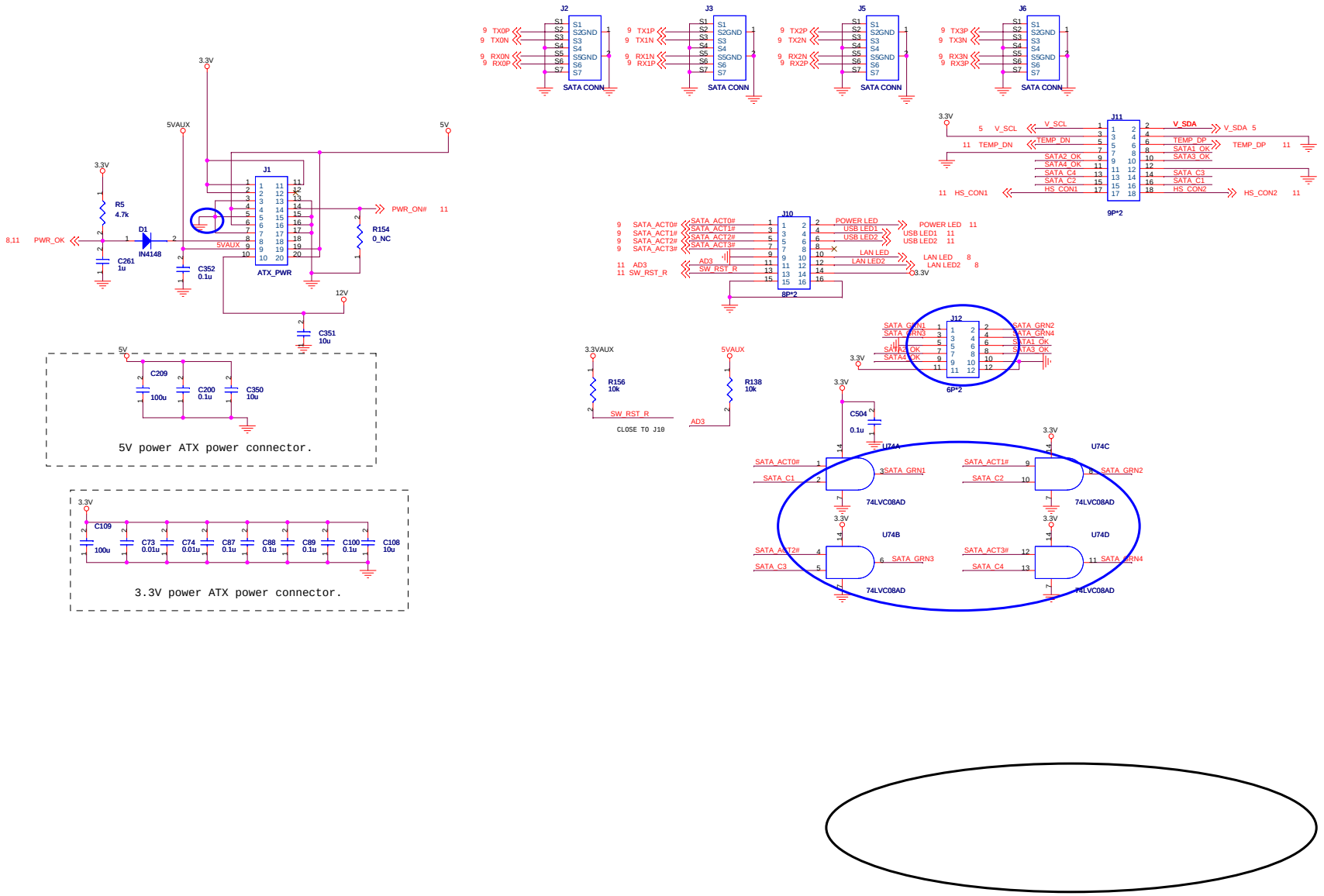

Title	Card-edge connector	
Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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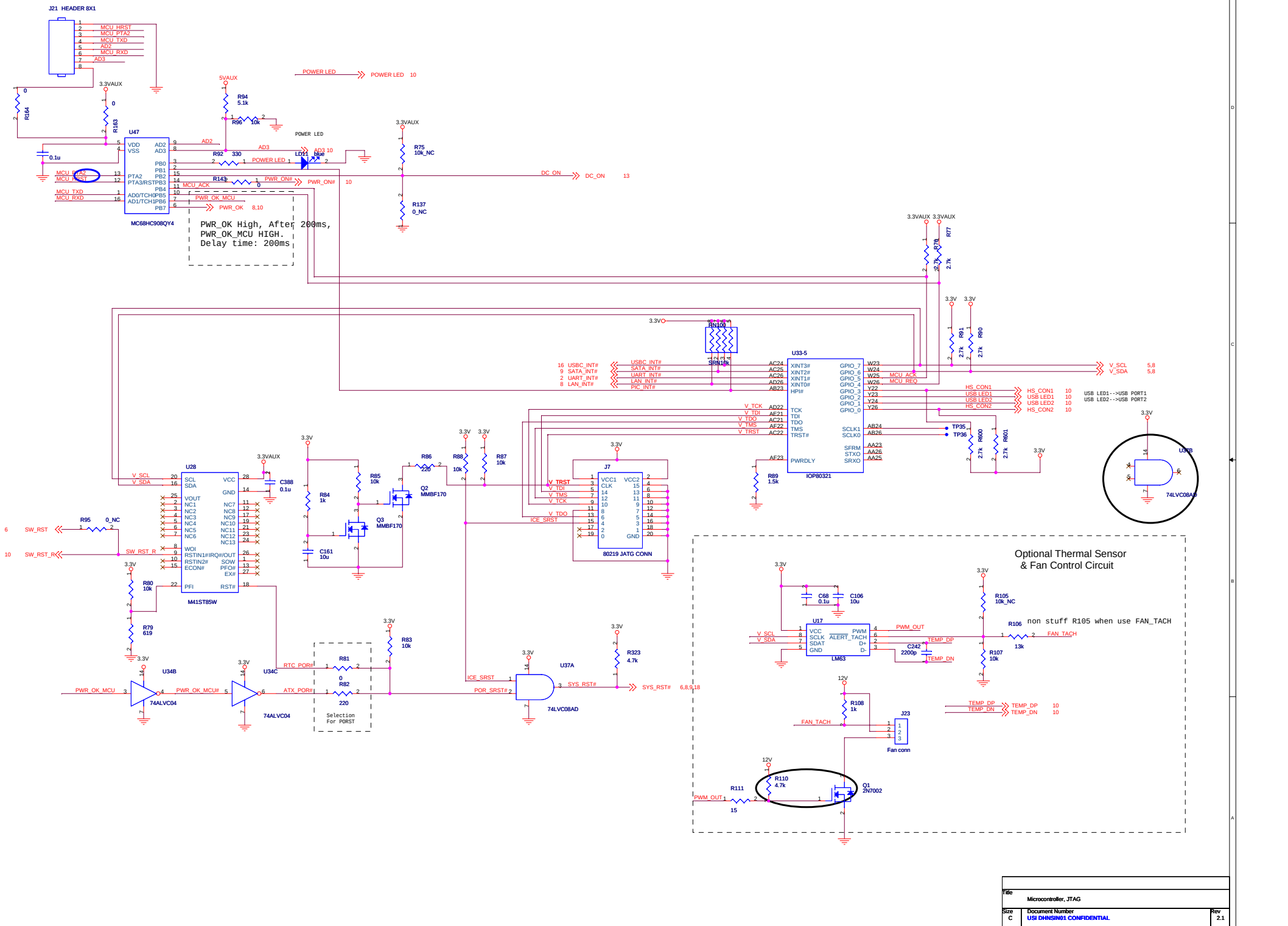
J21 HEADER 8X1
MCU_HRST
MCU_PTA2
MCU_TXD
AD2
MCU_RXD
AD3
3.3VAUX
5VAUX
POWER LED
POWER LED 10
R94 5.1k
R96 10k
R92 330
LD11 blue
R164
R163
U47
MC68HC908QY4
R143 0
PWR_ON#
PWR_ON# 10
PWR_OK_MCU
PWR_OK 8,10
MCU_ACK
PWR_OK High, After 200ms,
PWR_OK_MCU HIGH.
Delay time: 200ms
R75 10k_NC
R137 0_NC
DC_ON
DC_ON 13
U33-5
IOP80321
RN100 SRN10k
USBC_INT#
SATA_INT#
UART_INT#
LAN_INT#
PIC_INT#
V_SCL 5,8
V_SDA 5,8
MCU_REQ
HS_CON1
USB LED1
USB LED2
HS_CON2
USB LED1-->USB PORT1
USB LED2-->USB PORT2
V_TCK
V_TDI
V_TDO
V_TMS
V_TRST
TP35
TP36
R89 1.5k
R77 2.7k
R78 2.7k
R91 2.7k
R90 2.7k
R600 2.7k
R601 2.7k
U38B
74LVC08AD
U28
M41ST85W
C388 0.1u
R95 0_NC
SW_RST
SW_RST_R
R80 10k
R79 619
R84 1k
R85 10k
R86 220
Q2 MMBF170
Q3 MMBF170
C161 10u
R88 10k
R87 10k
J7
80219 JATG CONN
ICE_SRST
U34B
U34C
74ALVC04
PWR_OK_MCU#
RTC_PORR#
ATX_PORR#
R81 0
R82 220
Selection For PORST
R83 10k
U37A
74LVC08AD
POR_SRST#
SYS_RST#
R323 4.7k
SYS_RST# 6,8,9,18
Optional Thermal Sensor
& Fan Control Circuit
U17
LM63
C68 0.1u
C106 10u
C242 2200p
PWM_OUT
TEMP_DP
TEMP_DN
R105 10k_NC
R106 13k
R107 10k
non stuff R105 when use FAN_TACH
FAN_TACH
TEMP_DP 10
TEMP_DN 10
R108 1k
J23
Fan conn
R110 4.7k
R111 15
Q1 2N7002
Title
Microcontroller, JTAG
Size C
Document Number
USI DHNSIN01 CONFIDENTIAL
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Date: Thursday, September 01, 2005
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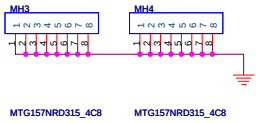

MH1 Connects with COMMON_GDN on page17

MH2 Connects with GND_EARTH on page15

Title: Mechanical hole		
Size: C	Document Number: USI DHNSIN01 CONFIDENTIAL	Rev: 2.1
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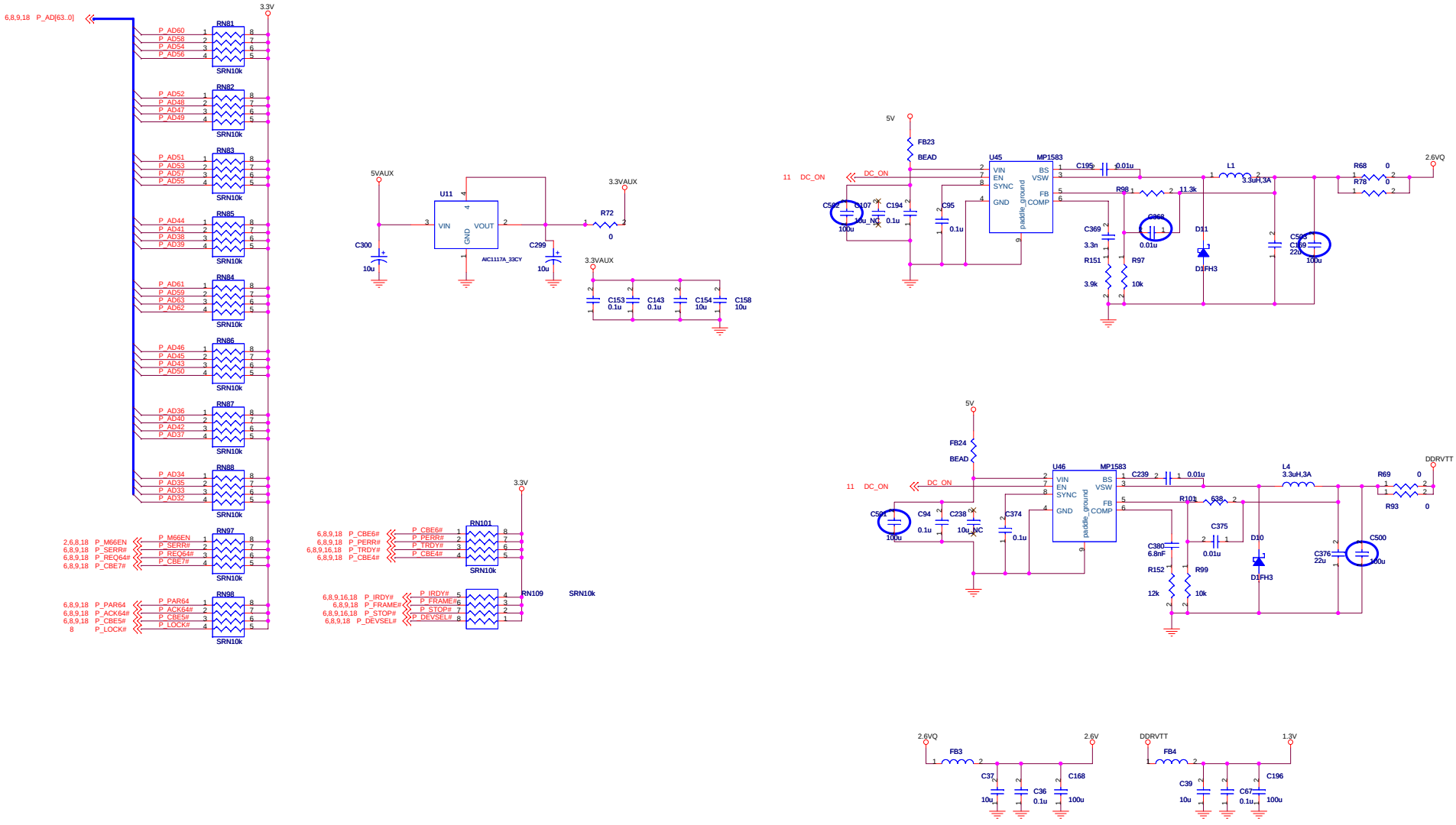

Title	PCI Termi & DDR PWR	
Size C	Document Number USI DHNSIN01 CONFIDENTIAL	Rev 2.1
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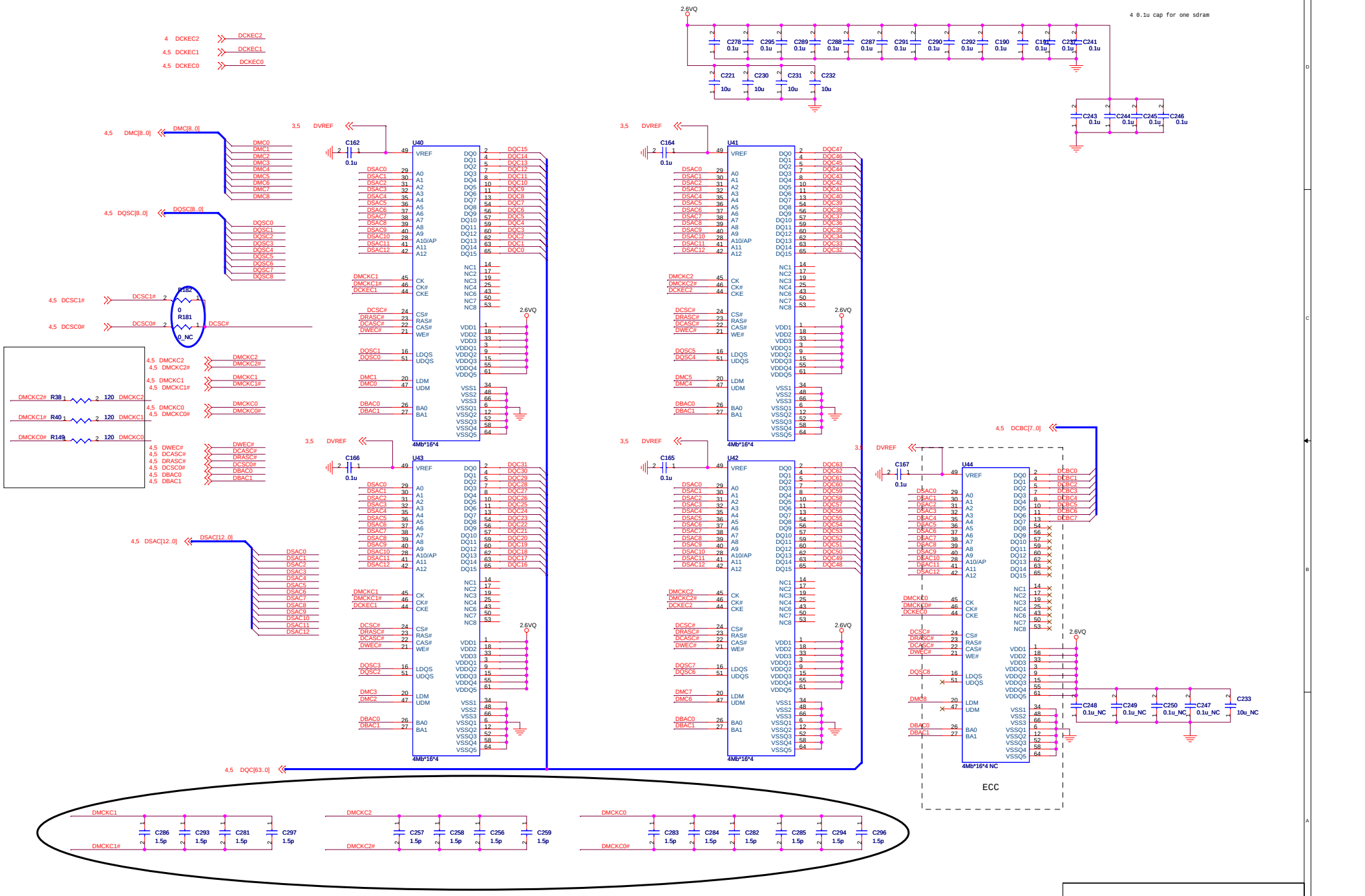
4 DCKEC2
4,5 DCKEC1
4,5 DCKEC0
DCKEC2
DCKEC1
DCKEC0
2.6VQ
4 0.1u cap for one sdram
C278 0.1u
C295 0.1u
C289 0.1u
C288 0.1u
C287 0.1u
C291 0.1u
C290 0.1u
C292 0.1u
C190 0.1u
C191 0.1u
C237 0.1u
C241 0.1u
C221 10u
C230 10u
C231 10u
C232 10u
C243 0.1u
C244 0.1u
C245 0.1u
C246 0.1u
4,5 DMC[8..0]
DMC[8..0]
DMC0
DMC1
DMC2
DMC3
DMC4
DMC5
DMC6
DMC7
DMC8
4,5 DQSC[8..0]
DQSC[8..0]
DQSC0
DQSC1
DQSC2
DQSC3
DQSC4
DQSC5
DQSC6
DQSC7
DQSC8
4,5 DSAC[12..0]
DSAC[12..0]
DSAC0
DSAC1
DSAC2
DSAC3
DSAC4
DSAC5
DSAC6
DSAC7
DSAC8
DSAC9
DSAC10
DSAC11
DSAC12
4,5 DQC[63..0]
3,5 DVREF
C162 0.1u
C164 0.1u
C166 0.1u
C165 0.1u
C167 0.1u
U40
U41
U43
U42
U44
4Mb*16*4
4Mb*16*4 NC
R182 0
R181 0_NC
4,5 DCSC1#
4,5 DCSC0#
DCSC1#
DCSC0#
DCSC#
4,5 DMCKC2
4,5 DMCKC2#
4,5 DMCKC1
4,5 DMCKC1#
4,5 DMCKC0
4,5 DMCKC0#
DMCKC2#
DMCKC1#
DMCKC0#
R38 120 DMCKC2
R40 120 DMCKC1
R149 120 DMCKC0
DMCKC2
DMCKC2#
DMCKC1
DMCKC1#
DMCKC0
DMCKC0#
4,5 DWEC#
4,5 DCASC#
4,5 DRASC#
4,5 DCSC0#
4,5 DBAC0
4,5 DBAC1
DWEC#
DCASC#
DRASC#
DCSC0#
DBAC0
DBAC1
4,5 DCBC[7..0]
DCBC0
DCBC1
DCBC2
DCBC3
DCBC4
DCBC5
DCBC6
DCBC7
2.6VQ
C248 0.1u_NC
C249 0.1u_NC
C250 0.1u_NC
C247 0.1u_NC
C233 10u_NC
ECC
DMCKC1
DMCKC1#
C286 1.5p
C293 1.5p
C281 1.5p
C297 1.5p
DMCKC2
DMCKC2#
C257 1.5p
C258 1.5p
C256 1.5p
C259 1.5p
DMCKC0
DMCKC0#
C283 1.5p
C284 1.5p
C282 1.5p
C285 1.5p
C294 1.5p
C296 1.5p
Title
On board memory
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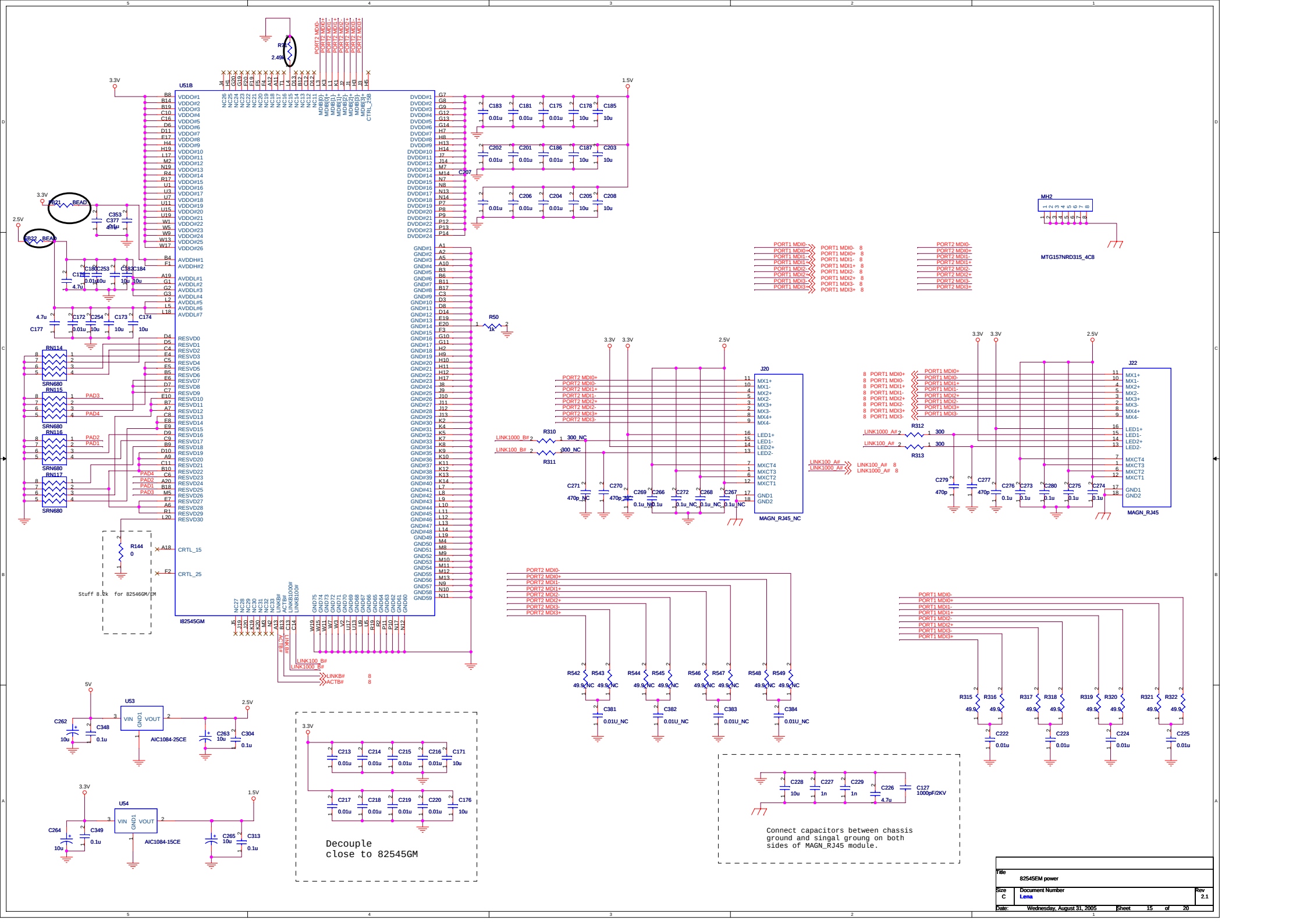
U51B
I82545GM
R144
0
Stuff 8.2k for 82546GM/EM
U53
AIC1084-25CE
U54
AIC1084-15CE
Decouple
close to 82545GM
Connect capacitors between chassis
ground and singal groung on both
sides of MAGN_RJ45 module.
J20
J22
MAGN_RJ45_NC
MAGN_RJ45
MTG157NRD315_4C8
Title
82545EM power
Size
C
Document Number
Lena
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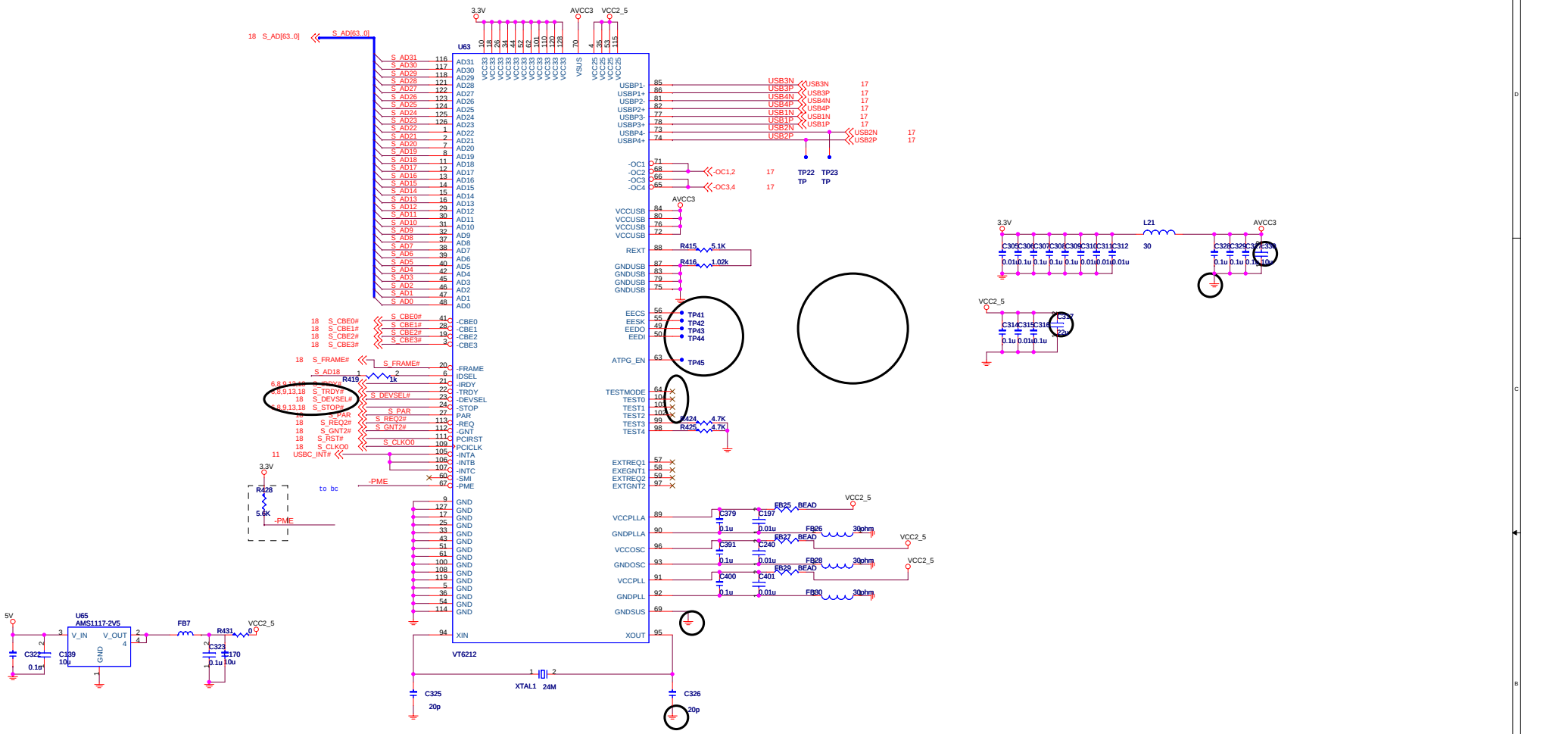

Title	USB Controller	
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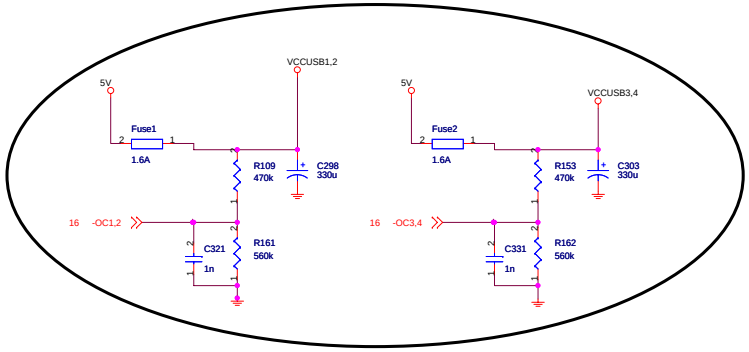

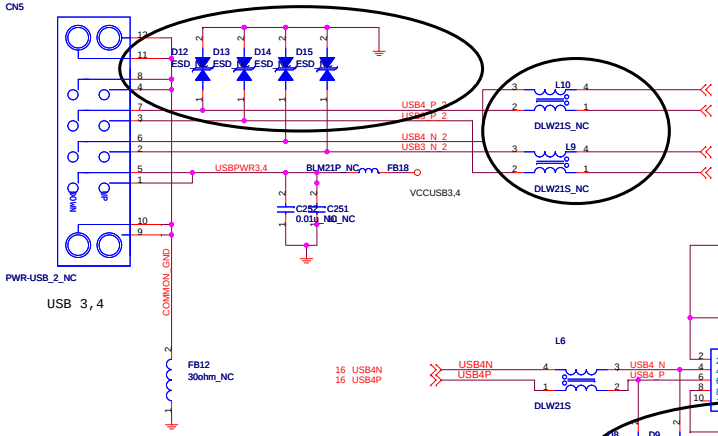

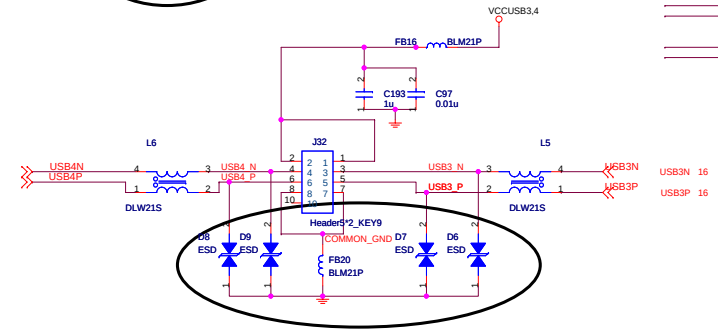

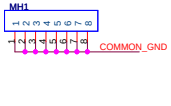

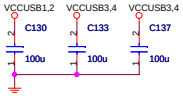

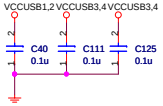

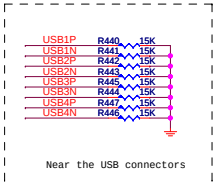

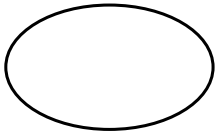

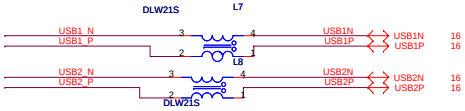

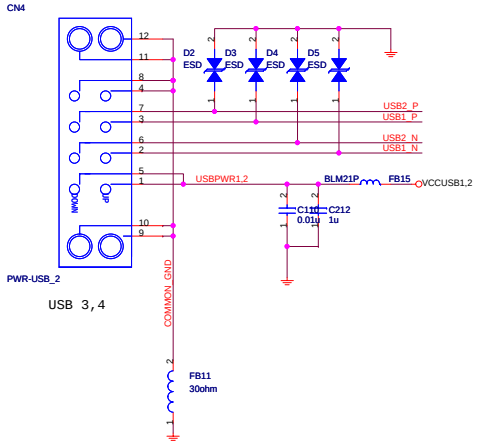

Title: USB CONN		
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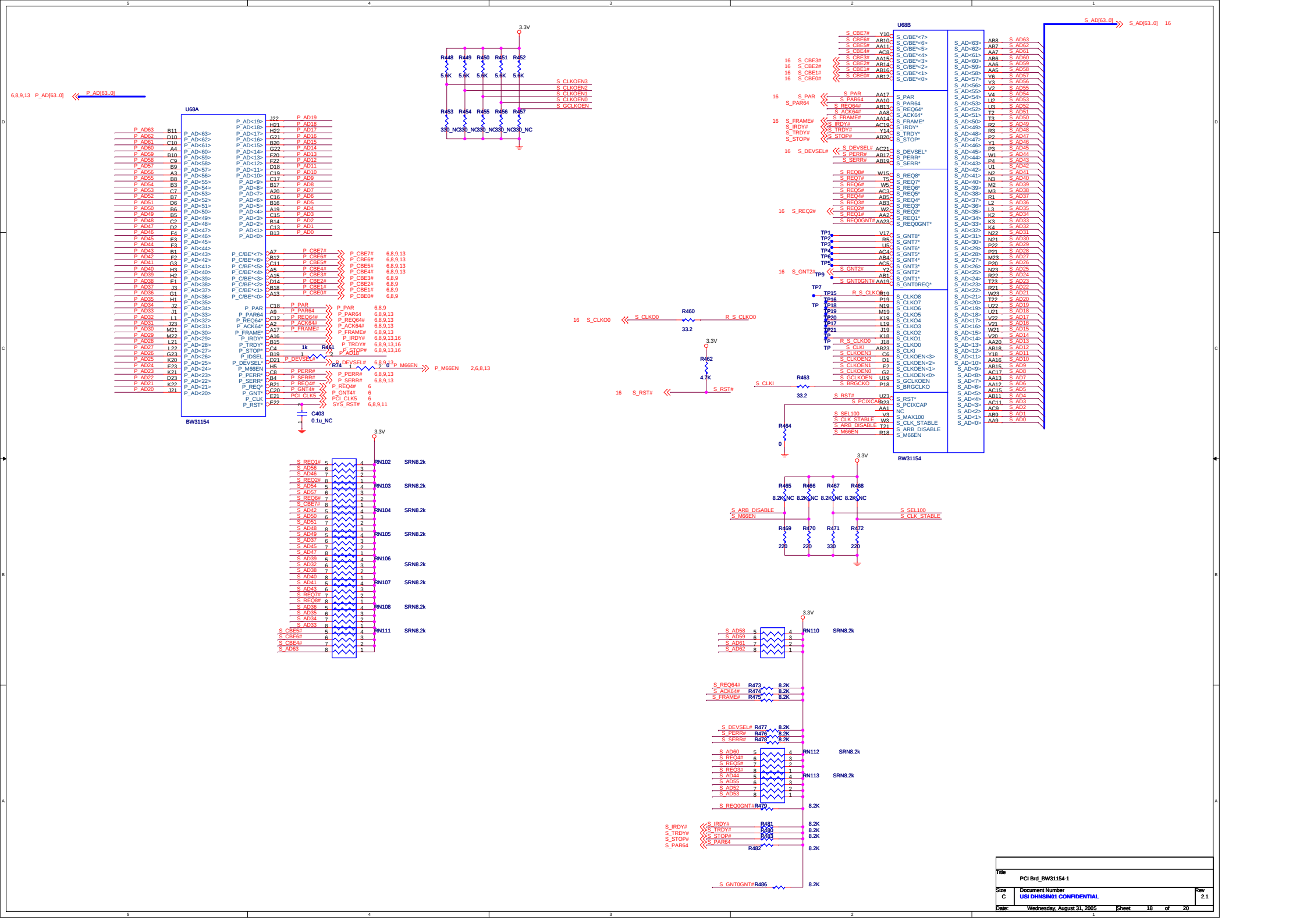
U68A
BW31154
U68B
BW31154
3.3V
R448 R449 R450 R451 R452
5.6K 5.6K 5.6K 5.6K 5.6K
R453 R454 R455 R456 R457
330_NC 330_NC 330_NC 330_NC 330_NC
S_CLKOEN3
S_CLKOEN2
S_CLKOEN1
S_CLKOEN0
S_GCLKOEN
6,8,9,13 P_AD[63..0]
P_AD[63..0]
S_AD[63..0]
S_AD[63..0] 16
16 S_CLKO0
S_CLKO0
R460
33.2
R_S_CLKO0
R462
4.7K
16 S_RST#
S_RST#
S_CLKI
R463
33.2
R464
0
R465 R466 R467 R468
8.2K_NC 8.2K_NC 8.2K_NC 8.2K_NC
S_ARB_DISABLE
S_M66EN
S_SEL100
S_CLK_STABLE
R469 R470 R471 R472
220 220 330 220
RN102 SRN8.2k
RN103 SRN8.2k
RN104 SRN8.2k
RN105 SRN8.2k
RN106 SRN8.2k
RN107 SRN8.2k
RN108 SRN8.2k
RN111 SRN8.2k
RN110 SRN8.2k
RN112 SRN8.2k
RN113 SRN8.2k
R473 8.2K
R474 8.2K
R475 8.2K
R477 8.2K
R476 8.2K
R478 8.2K
R479 8.2K
R481 8.2K
R480 8.2K
R483 8.2K
R482 8.2K
R486 8.2K
S_IRDY#
S_TRDY#
S_STOP#
S_PAR64
S_GNT0GNT#
R461 1k
R74 1
P_M66EN 2,6,8,13
C403
0.1u_NC
Title
PCI Brd_BW31154-1
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C
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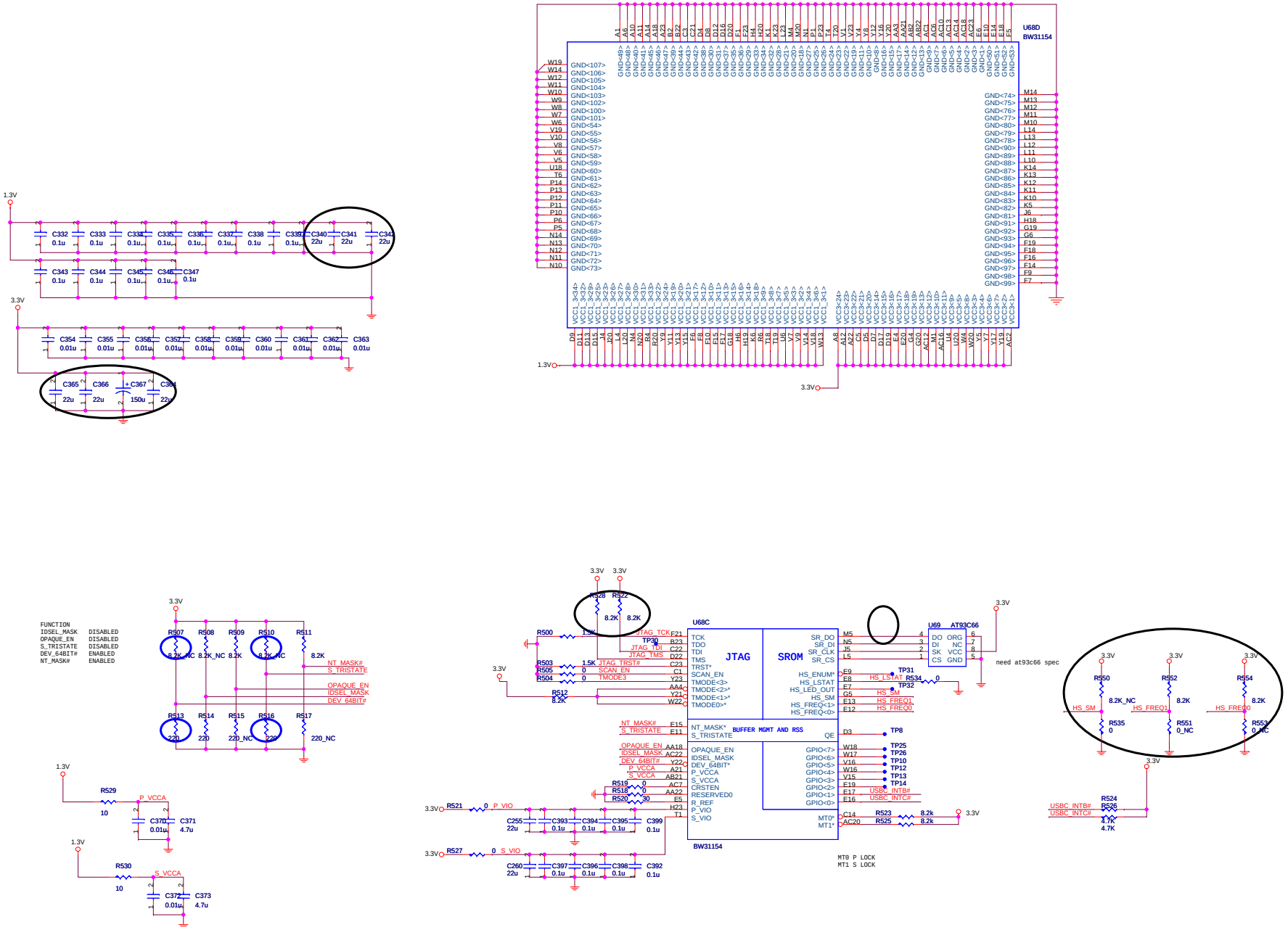

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Ver1.0--> Ver1.1
1: Change R35,R49,R50 pull up the voltage:VTT -> 3.3V (Page 4)
2: Delete U9 pin19 net(Page 2)
3: Add 4.7k pull up resistor in U55 pin53(Page 2)
4: Delete 4.7k pull up resistor in U55 pin15(Page 2)
5: Modify netP_AD19 to connect R41
6: Delete CRTL_15 and CRTL_25 circuit
7: Add AIC1117_18 voltage LDO

Ver1.1--> Lena MB V0.1
1: Add USB Host Controller
2: Change EMI and ESD component on page17
3: Delete Power MCU fuction on page11
4: Add Mount hole
5: Add U62(IDTQ3126) on page 11
6: Add power test resistor
7: Change Ethernet Controller from 82545 to 82546
8: Add PCI Bridge BW311544
9: Change USB controller from ISP1760 to VT6212
10: Change U63 footprint(PQFP->LQFP)
11: Change DDR CKE pull-up voltage value(3.3v->2.6VQ)

Leba MB V0.1--> Lena MB V0.2
1: Change R460,R463 value(33ohm-->33.2ohm)
2: Remove R459,R522,R528
3: Add C255,C256,C292,C293,C294,C295,C296,C297,C298,C299,c391
4: Change 2.6VQ and VTTDDR power module
5: Chagne 2.5V and 1.5V power module
6: Change J21 connector model

Leba MB V0.2--> Lena MB V2.1
1: Stuff R183,R308,R516,C375,C368
2: Delete R158,R145,R423,R510,C107,C238,C33
3: Add C500,C501,C502,C503,C504,U74,R600,R601
4: Change R152 value: 1.96K--> 12K

Title: History		
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