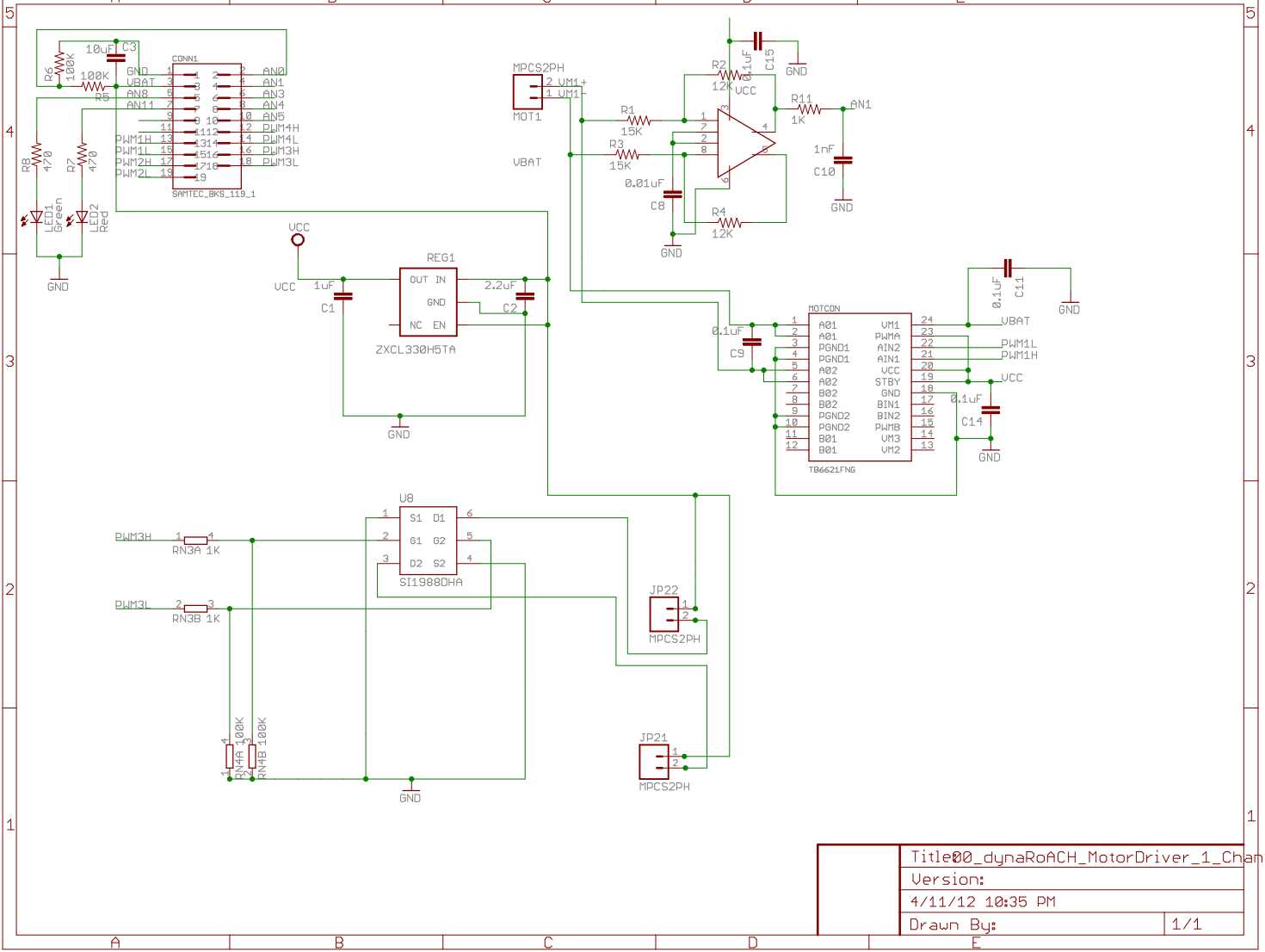
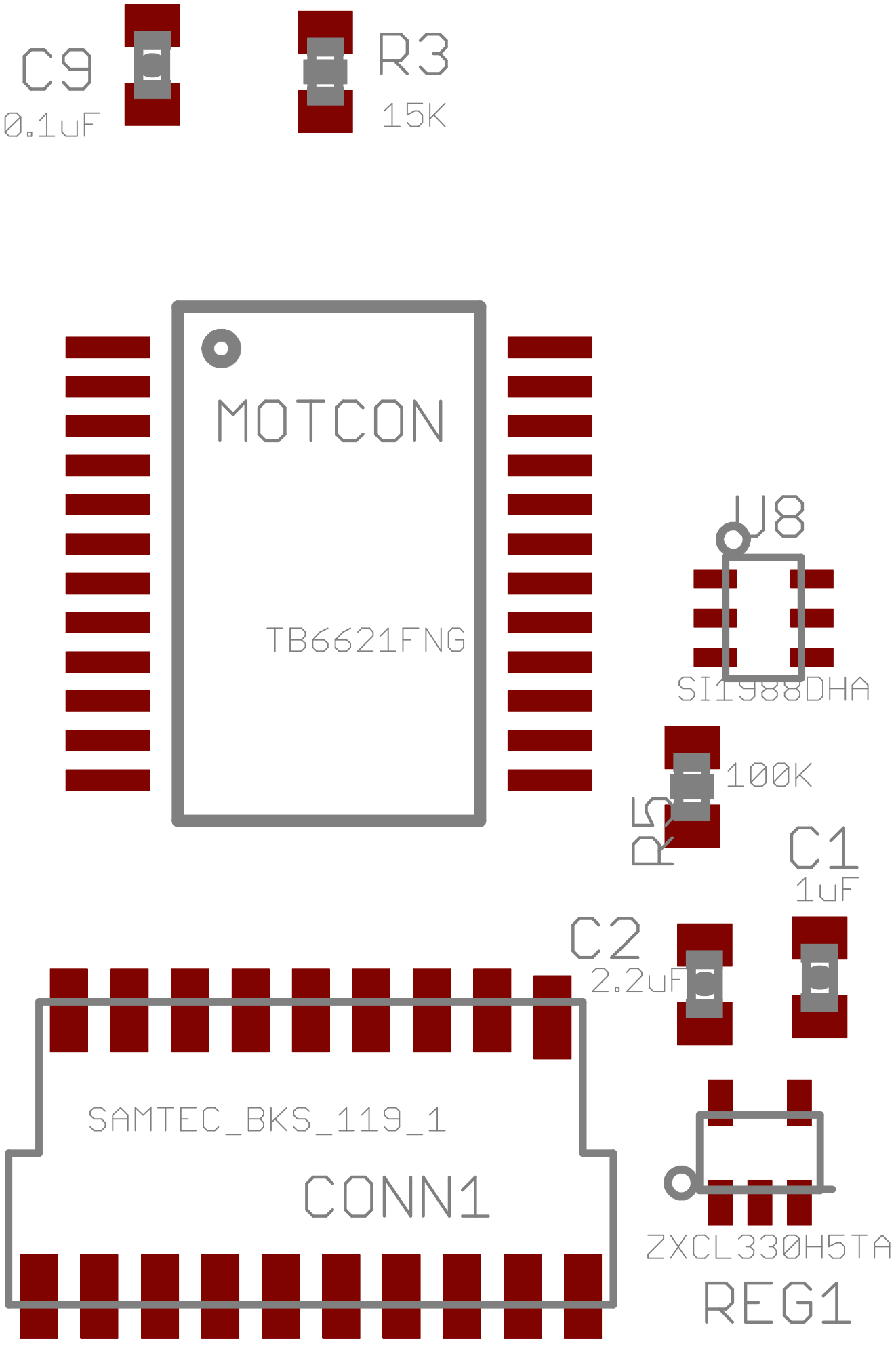
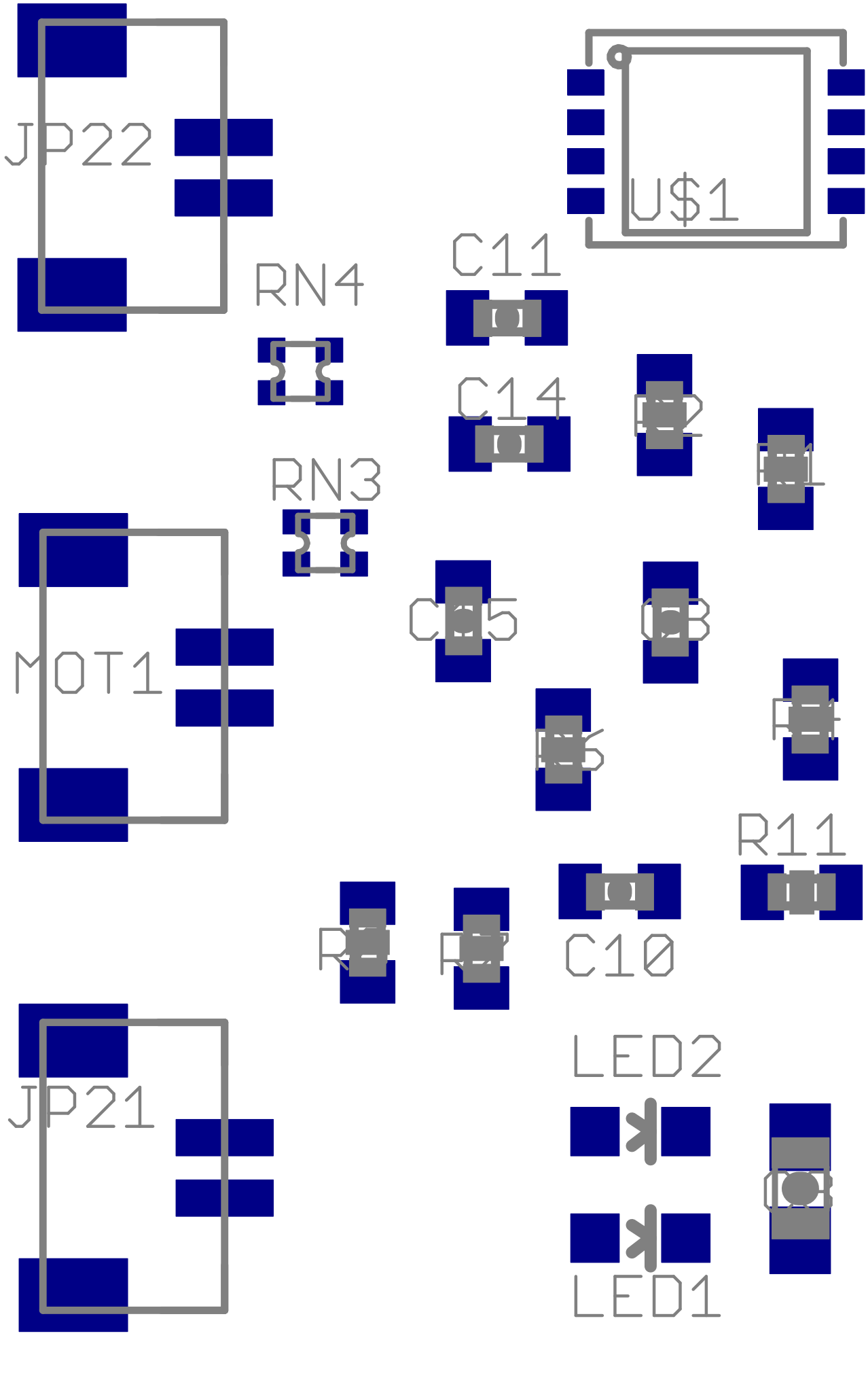



| | |
|---|---|
| Title | 00_dynaRoACH_MotorDriver_1_Cham |
| Version: | |
| 4/11/12 10:35 PM | |
| Drawn By: | 1/1 |


C9
0.1uF
R3
15K
MOTCON
TB6621FNG
U8
SI1988DHA
100K
R5
C1
1uF
C2
2.2uF
SAMTEC_BKS_119_1
CONN1
ZXCL330H5TA
REG1

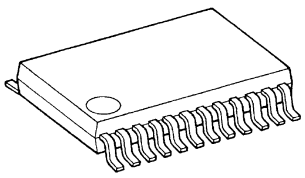

JP22
U$1
C11
RN4
C14
RN3
MOT1
C5
C8
R1
C6
R4
R11
C10
JP21
LED2
LED1

Toshiba Bi-CD Integrated Circuit Silicon Monolithic

# TB6612FNG

Driver IC for Dual DC motor

TB6612FNG is a driver IC for DC motor with output transistor in LD MOS structure with low ON-resistor. Two input signals, IN1 and IN2, can choose one of four modes such as CW, CCW, short brake, and stop mode.



SSOP24-P-300-0.65A

質量: 0.14 g (標準)

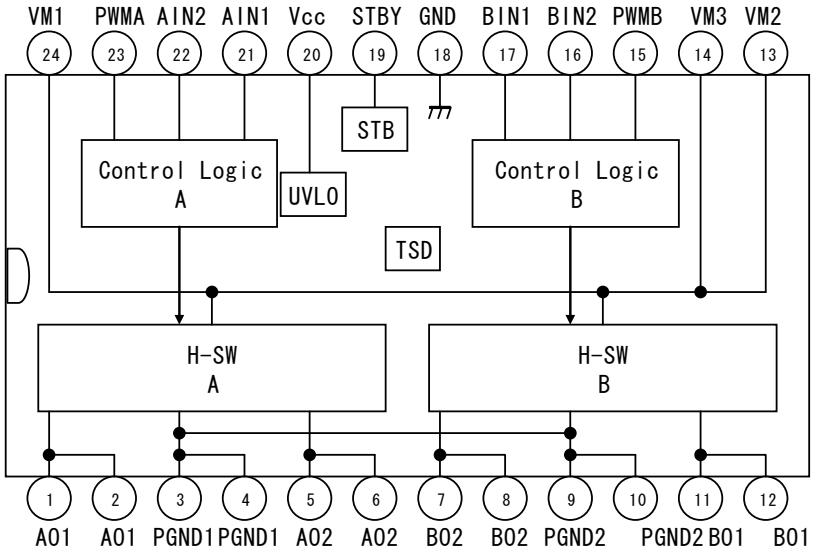
## Features

- Power supply voltage; $V_M$ = 15 V(Max)
- Output current; $I_{OUT}$=1.2 A(ave) / 3.2 A (peak)
- Output low ON resistor; 0.5Ω (upper+lower Typ. @$V_M \geq 5$ V)
- Standby (Power save) system
- CW / CCW / short brake / stop function modes
- Built-in thermal shutdown circuit and low voltage detecting circuit
- Small faced package(SSOP24: 0.65 mm Lead pitch)
- Response to Pb free packaging

* This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

The TB6612FNG is a Pb-free product.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds

## Block Diagram




## Pin Functions

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | AO1 | O | ch A output1 |
| 2 | AO1 | | |
| 3 | PGND1 | — | Power GND 1 |
| 4 | PGND1 | | |
| 5 | AO2 | O | ch A output2 |
| 6 | AO2 | | |
| 7 | BO2 | O | ch B output2 |
| 8 | BO2 | | |
| 9 | PGND2 | — | Power GND 2 |
| 10 | PGND2 | | |
| 11 | BO1 | O | ch B output1 |
| 12 | BO1 | | |
| 13 | VM2 | — | Motor supply (2.5 V to 13.5 V) |
| 14 | VM3 | | |
| 15 | PWMB | I | ch B PWM input / 200 kΩ pull-down at internal |
| 16 | BIN2 | I | ch B input 2 / 200 kΩ pull-down at internal |
| 17 | BIN1 | I | ch B input 1 / 200 kΩ pull-down at internal |
| 18 | GND | — | Small signal GND |
| 19 | STBY | I | “L”=standby / 200 kΩ pull-down at internal |
| 20 | Vcc | — | Small signal supply |
| 21 | AIN1 | I | ch A input 1 / 200 kΩ pull-down at internal |
| 22 | AIN2 | I | ch A input 2 / 200 kΩ pull-down at internal |
| 23 | PWMA | I | ch A PWM input / 200 kΩ pull-down at internal |
| 24 | VM1 | — | Motor supply (2.5 V~13.5 V) |

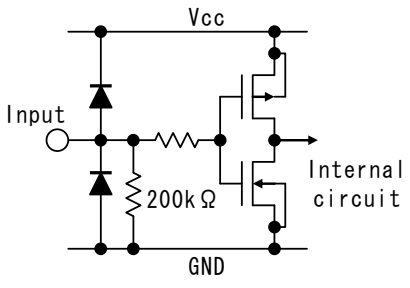
## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit | Remarks |
|---|---|---|---|---|
| Supply voltage | $V_M$ | 15 | V | |
| | $V_{CC}$ | 6 | | |
| Input voltage | $V_{IN}$ | -0.2 to 6 | V | IN1,IN2,STBY,PWM pins |
| Output voltage | $V_{OUT}$ | 15 | V | O1,O2 pins |
| Output current | $I_{OUT}$ | 1.2 | A | Per 1 ch |
| | $I_{OUT}$ (peak) | 2 | | tw = 20 ms Continuous pulse, Duty ≤ 20% |
| | | 3.2 | | tw = 10 ms Single pulse |
| Power dissipation | $P_D$ | 0.78 | W | IC only |
| | | 0.89 | | 50 mm × 50 mm t=1.6 mm Cu ≥ 40% in PCB mounting |
| | | 1.36 | | 76.2 mm × 114.3 mm t=1.6 mm Cu ≥ 30% in PCB monting |
| Operating temperature | $T_{opr}$ | -20 to 85 | ℃ | |
| Storage temperature | $T_{stg}$ | -55 to 150 | ℃ | |

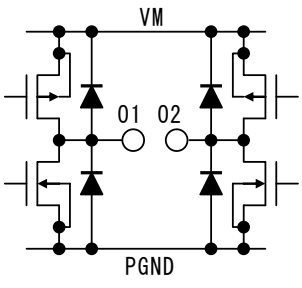
## Operating Range (Ta=-20～85℃)

| Characteristics | Symbol | Min | Typ. | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.7 | 3 | 5.5 | V | |
| | $V_M$ | 2.5 | 5 | 13.5 | V | |
| Output current (H-SW) | $I_{OUT}$ | — | — | 1.0 | A | $V_M \geq 4.5$ V |
| | | — | — | 0.4 | | 4.5 V > $V_M \geq$ 2.5 V<br>Without PWM Operation |
| Switching frequency | $f_{PWM}$ | — | — | 100 | kHz | |

**Input pin;** IN1, IN2, PWM, STBY




**Output pin;** O1, O2

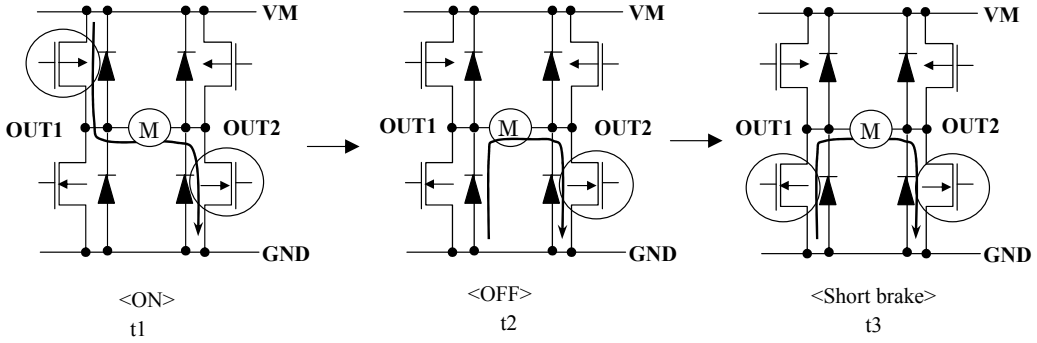


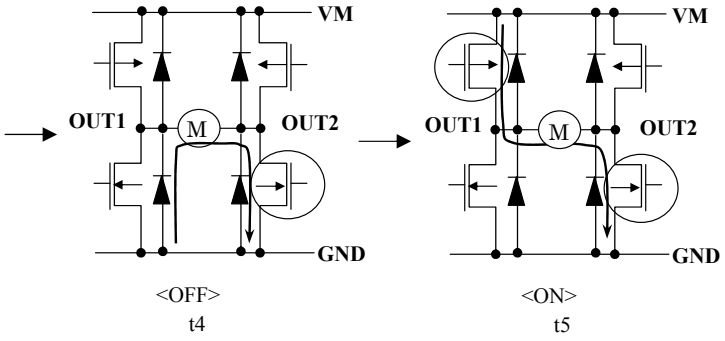
## H-SW Control Function

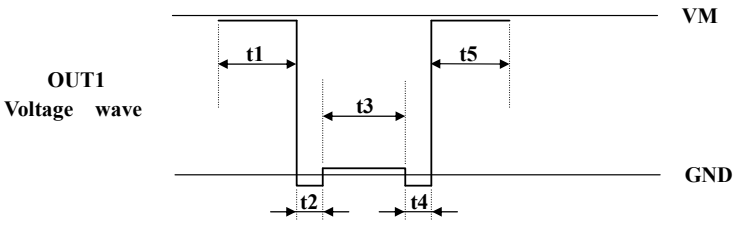
| Input | | | | Output | | |
|---|---|---|---|---|---|---|
| IN1 | IN2 | PWM | STBY | OUT1 | OUT2 | Mode |
| H | H | H/L | H | L | L | Short brake |
| L | H | H | H | L | H | CCW |
| | | L | H | L | L | Short brake |
| H | L | H | H | H | L | CW |
| | | L | H | L | L | Short brake |
| L | L | H | H | OFF (High impedance) | | Stop |
| H/L | H/L | H/L | L | OFF (High impedance) | | Standby |

## H-SW Operating Description

・To prevent penetrating current, dead time t2 and t4 is provided in switching to each mode in the IC.



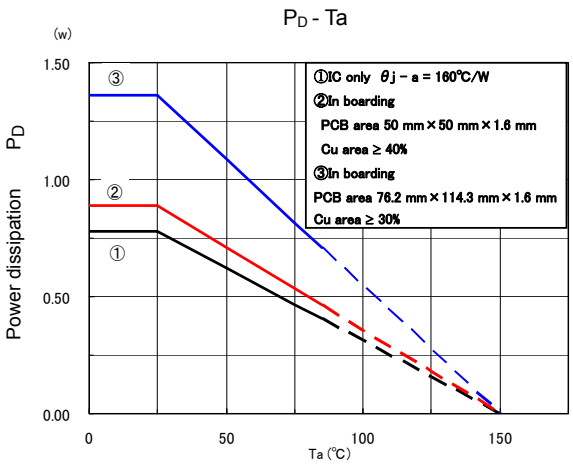



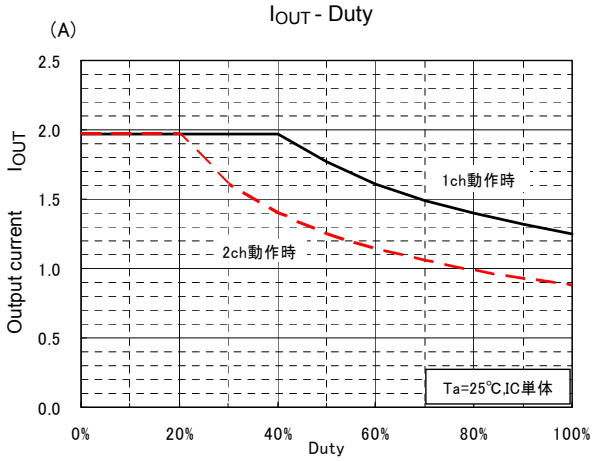



**Electrical Characteristics (unless otherwise specified, Ta = 25°C, $V_{CC}$ = 3 V, $V_M$ = 5 V)**

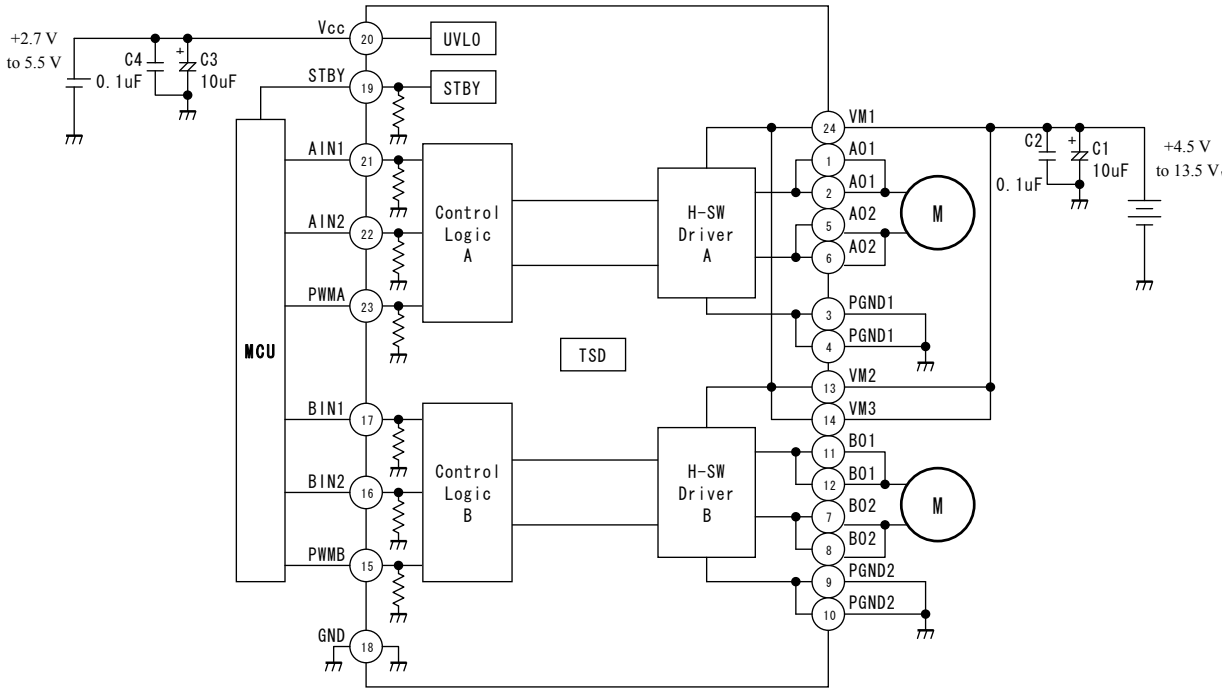
| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$(3V) | STBY = $V_{CC}$ = 3 V, $V_M$ = 5 V | — | 1.1 | 1.8 | mA |
| | $I_{CC}$(5.5V) | STBY = $V_{CC}$ = 5.5 V, $V_M$ = 5 V | — | 1.5 | 2.2 | |
| | $I_{CC(STB)}$ | STBY = 0 V | — | — | 1 | µA |
| | $I_{M(STB)}$ | | — | — | 1 | |
| Control input voltage | $V_{IH}$ | | $V_{CC}$×0.7 | — | $V_{CC}$+0.2 | V |
| | $V_{IL}$ | | -0.2 | — | $V_{CC}$×0.3 | |
| Control input current | $I_{IH}$ | $V_{IN}$ = 3 V | 5 | 15 | 25 | µA |
| | $I_{IL}$ | $V_{IN}$ = 0 V | — | — | 1 | |
| Standby input voltage | $V_{IH(STB)}$ | | $V_{CC}$×0.7 | — | $V_{CC}$+0.2 | V |
| | $V_{IL(STB)}$ | | -0.2 | — | $V_{CC}$×0.3 | |
| Standby input current | $I_{IH(STB)}$ | $V_{IN}$ = 3 V | 5 | 15 | 25 | µA |
| | $I_{IL(STB)}$ | $V_{IN}$ = 0 V | — | — | 1 | |
| Output saturating voltage | $V_{sat(U+L)1}$ | $I_O$ = 1 A, $V_{CC}$ = $V_M$ = 5 V | — | 0.5 | 0.7 | V |
| | $V_{sat(U+L)2}$ | $I_O$ = 0.3 A, $V_{CC}$ = $V_M$ = 5 V | | 0.15 | 0.21 | |
| Output leakage current | $I_{L(U)}$ | $V_M$ = $V_{OUT}$ = 15 V | — | — | 1 | µA |
| | $I_{L(L)}$ | $V_M$ = 15 V, $V_{OUT}$ = 0 V | -1 | — | — | |
| Regenerative diode VF | $V_{F(U)}$ | $I_F$ = 1A | — | 1 | 1.1 | V |
| | $V_{F(L)}$ | | — | 1 | 1.1 | |
| Low voltage detecting voltage | UVLD | (Designed value) | — | 1.9 | — | V |
| Recovering voltage | UVLC | | — | 2.2 | — | |
| Response speed | $t_r$ | (Designed value) | — | 24 | — | ns |
| | $t_f$ | | — | 41 | — | |
| | Dead time H to L | Penetration protect time | — | 50 | — | |
| | Dead time L to H | (Designed value) | — | 230 | — | |
| Thermal shutdown circuit operating temperature | TSD | (Designed value) | — | 175 | — | °C |
| Thermal shutdown hysteresis | △TSD | | — | 20 | — | |

## Target characteristics



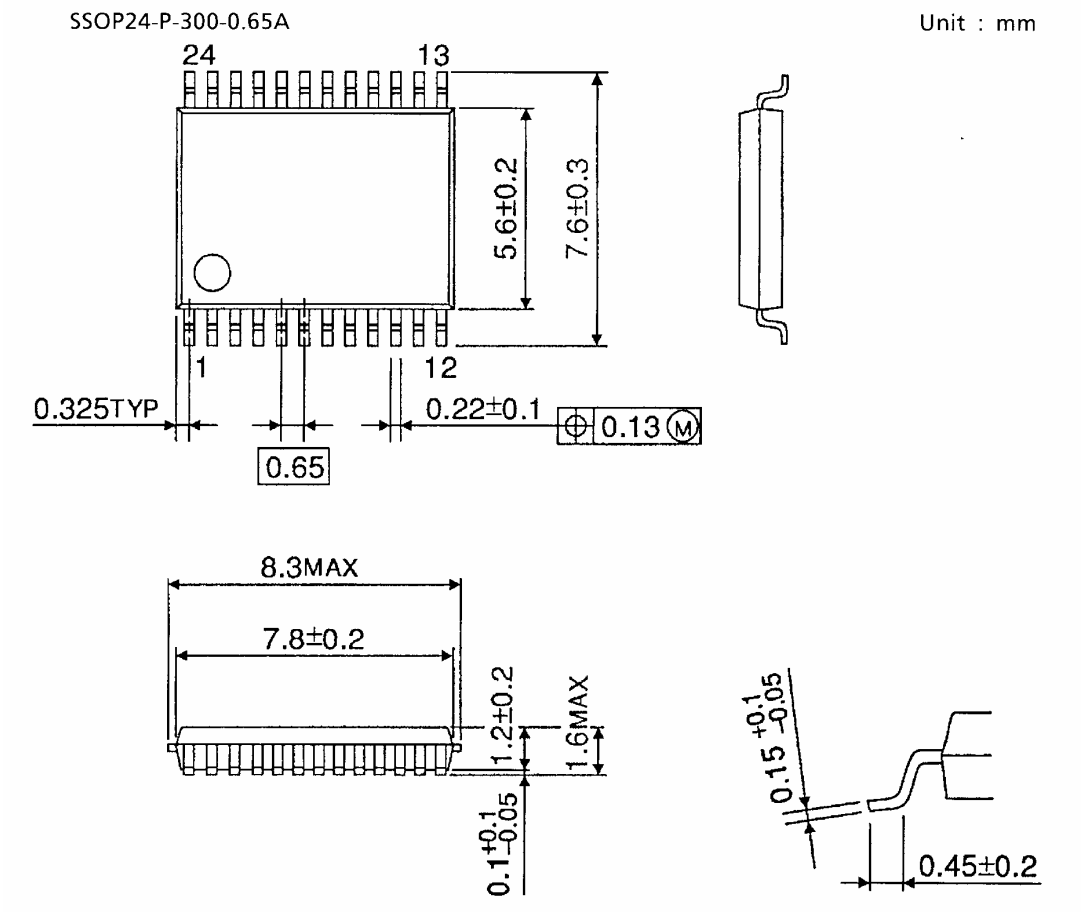



## Typical Application Diagram




Note: Condensers for noise absorption (C1, C2, C3, and C4) should be connected as close as possible to the IC.

**Package Dimennsions**




Weght: 0.14 g (typ)

## Notes on Contents

### 1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

### 2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### 3. Timing Charts
Timing charts may be simplified for explanatory purposes.

### 4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

### 5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

## IC Usage Considerations
### Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

**Points to remember on handling of ICs**

(1) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ($T_J$) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

## RESTRICTIONS ON PRODUCT USE

070122EBA_R6

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# Low Power, Fully Differential Input/Output Amplifier/Driver Family

## FEATURES

- **Adjustable Gain and Fixed Gain Blocks of 1, 2, 5 and 10**
- **±0.3% (Max) Gain Error from –40°C to 85°C**
- **3.5ppm/°C Gain Temperature Coefficient**
- **5ppm Gain Long Term Stability**
- **Fully Differential Input and Output**
- **$C_{LOAD}$ Stable up to 10,000pF**
- **Adjustable Output Common Mode Voltage**
- Rail-to-Rail Output Swing
- Low Supply Current: 1mA (Max)
- High Output Current: 10mA (Min)
- Specified on a Single 2.7V to ±5V Supply
- DC Offset Voltage <2.5mV (Max)
- Available in 8-Lead MSOP Package

## APPLICATIONS

- Differential Driver/Receiver
- Differential Amplification
- Single-Ended to Differential Conversion
- Level Shifting
- Trimmed Phase Response for Multichannel Systems

## DESCRIPTION

The LTC®1992 product family consists of five fully differential, low power amplifiers. The LTC1992 is an unconstrained fully differential amplifier. The LTC1992-1, LTC1992-2, LTC1992-5 and LTC1992-10 are fixed gain blocks (with gains of 1, 2, 5 and 10 respectively) featuring precision on-chip resistors for accurate and ultrastable gain. All of the LTC1992 parts have a separate internal common mode feedback path for outstanding output phase balancing and reduced second order harmonics. The $V_{OCM}$ pin sets the output common mode level independent of the input common mode level. This feature makes level shifting of signals easy.

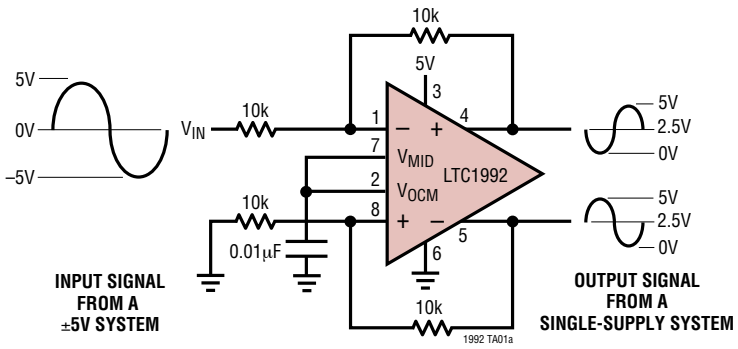
The amplifiers' differential inputs operate with signals ranging from rail-to-rail with a common mode level from the negative supply up to 1.3V from the positive supply. The differential input DC offset is typically 250µV. The rail-to-rail outputs sink and source 10mA. The LTC1992 is stable for all capacitive loads up to 10,000pF.

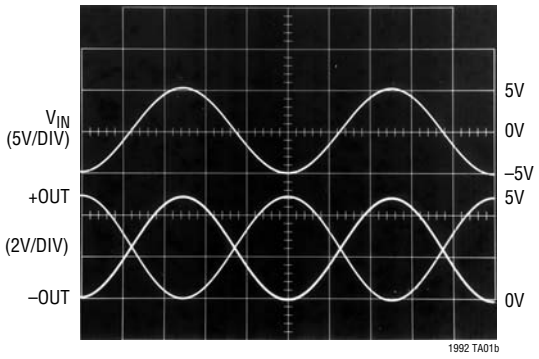
The LTC1992 can be used in single supply applications with supply voltages as low as 2.7V. It can also be used with dual supplies up to ±5V. The LTC1992 is available in an 8-pin MSOP package.



## TYPICAL APPLICATION

**Single-Supply, Single-Ended to Differential Conversion**



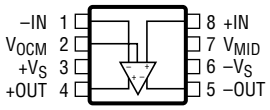



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($+V_S$ to $-V_S$) ..... 12V
Maximum Voltage
on any Pin ..... $(-V_S - 0.3V) \leq V_{PIN} \leq (+V_S + 0.3V)$
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 5)
LTC1992CMS8/LTC1992-XCMS8/
LTC1992IMS8/LTC1992-XIMS8 .....–40°C to 85°C
LTC1992HMS8/LTC1992-XHMS8 .....–40°C to 125°C
Specified Temperature Range (Note 6)
LTC1992CMS8/LTC1992-XCMS8/
LTC1992IMS8/LTC1992-XIMS8 .....–40°C to 85°C
LTC1992HMS8/LTC1992-XHMS8 .....–40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION

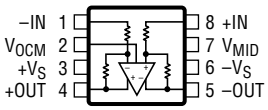
TOP VIEW




MS8 PACKAGE
8-LEAD PLASTIC MSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 250°C/W

TOP VIEW




MS8 PACKAGE
8-LEAD PLASTIC MSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 250°C/W

| ORDER PART NUMBER | MS8 PART MARKING |
|---|---|
| LTC1992CMS8 | LTYU |
| LTC1992IMS8 | LTZC |
| LTC1992HMS8 | LTAGR |

| ORDER PART NUMBER | MS8 PART MARKING |
|---|---|
| LTC1992-1CMS8 | LTACJ |
| LTC1992-1IMS8 | LTACM |
| LTC1992-1HMS8 | LTAFZ |
| LTC1992-2CMS8 | LTYV |
| LTC1992-2IMS8 | LTZD |
| LTC1992-2HMS8 | LTAGA |
| LTC1992-5CMS8 | LTACK |
| LTC1992-5IMS8 | LTACN |
| LTC1992-5HMS8 | LTAJH |
| LTC1992-10CMS8 | LTACL |
| LTC1992-10IMS8 | LTACP |
| LTC1992-10HMS8 | LTAJJ |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Specifications applicable to all parts in the LTC1992 family.**

| SYMBOL | PARAMETER | CONDITIONS | | ALL C AND I GRADE MIN | ALL C AND I GRADE TYP | ALL C AND I GRADE MAX | ALL H GRADE MIN | ALL H GRADE TYP | ALL H GRADE MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_S$ | Supply Voltage Range | | ● | 2.7 | | 11 | 2.7 | | 11 | V |
| $I_S$ | Supply Current | $V_S$ = 2.7V to 5V | | | 0.65 | 1.0 | | 0.65 | 1.0 | mA |
| | | | ● | | 0.75 | 1.2 | | 0.8 | 1.5 | mA |
| | | $V_S$ = ±5V | | | 0.7 | 1.2 | | 0.7 | 1.2 | mA |
| | | | ● | | 0.8 | 1.5 | | 0.9 | 1.8 | mA |
| $V_{OSDIFF}$ | Differential Offset Voltage (Input Referred) (Note 7) | $V_S$ = 2.7V | ● | | ±0.25 | ±2.5 | | ±0.25 | ±4 | mV |
| | | $V_S$ = 5V | ● | | ±0.25 | ±2.5 | | ±0.25 | ±4 | mV |
| | | $V_S$ = ±5V | ● | | ±0.25 | ±2.5 | | ±0.25 | ±4 | mV |
| $\Delta V_{OSDIFF}/\Delta T$ | Differential Offset Voltage Drift (Input Referred) (Note 7) | $V_S$ = 2.7V | ● | | 10 | | | 10 | | µV/°C |
| | | $V_S$ = 5V | ● | | 10 | | | 10 | | µV/°C |
| | | $V_S$ = ±5V | ● | | 10 | | | 10 | | µV/°C |
| PSRR | Power Supply Rejection Ratio (Input Referred) (Note 7) | $V_S$ = 2.7V to ±5V | ● | 75 | 80 | | 72 | 80 | | dB |
| $G_{CM}$ | Common Mode Gain($V_{OUTCM}/V_{OCM}$) | | ● | | 1 | | | 1 | | |
| | Common Mode Gain Error | | ● | | ±0.1 | ±0.3 | | ±0.1 | ±0.35 | % |
| | Output Balance ($\Delta V_{OUTCM}/(\Delta V_{OUTDIFF}$) | $V_{OUTDIFF}$ = –2V to +2V | ● | | –85 | –60 | | –85 | –60 | dB |
| $V_{OSCM}$ | Common Mode Offset Voltage ($V_{OUTCM} - V_{OCM}$) | $V_S$ = 2.7V | ● | | ±0.5 | ±12 | | ±0.5 | ±15 | mV |
| | | $V_S$ = 5V | ● | | ±1 | ±15 | | ±1 | ±17 | mV |
| | | $V_S$ = ±5V | ● | | ±2 | ±18 | | ±2 | ±20 | mV |
| $\Delta V_{OSCM}/\Delta T$ | Common Mode Offset Voltage Drift | $V_S$ = 2.7V | ● | | 10 | | | 10 | | µV/°C |
| | | $V_S$ = 5V | ● | | 10 | | | 10 | | µV/°C |
| | | $V_S$ = ±5V | ● | | 10 | | | 10 | | µV/°C |
| $V_{OUTCMR}$ | Output Signal Common Mode Range (Voltage Range for the $V_{OCM}$ Pin) | | ● | $(-V_S)$+0.5V | | $(+V_S)$–1.3V | $(-V_S)$+0.5V | | $(+V_S)$–1.3V | V |
| $R_{INVOCM}$ | Input Resistance, $V_{OCM}$ Pin | | ● | | 500 | | | 500 | | MΩ |
| $I_{BVOCM}$ | Input Bias Current, $V_{OCM}$ Pin | $V_S$ = 2.7V to ±5V | ● | | ±2 | | | ±2 | | pA |
| $V_{MID}$ | Voltage at the $V_{MID}$ Pin | | ● | 2.44 | 2.50 | 2.56 | 2.43 | 2.50 | 2.57 | V |
| $V_{OUT}$ | Output Voltage, High (Note 2) | $V_S$ = 2.7V, Load = 10k | ● | 2.60 | 2.69 | | 2.60 | 2.69 | | V |
| | | $V_S$ = 2.7V, Load = 5mA | ● | 2.50 | 2.61 | | 2.50 | 2.61 | | V |
| | | $V_S$ = 2.7V,Load = 10mA | ● | 2.29 | 2.52 | | 2.29 | 2.52 | | V |
| | Output Voltage, Low (Note 2) | $V_S$ = 2.7V, Load = 10k | ● | | 0.02 | 0.10 | | 0.02 | 0.10 | V |
| | | $V_S$ = 2.7V, Load = 5mA | ● | | 0.10 | 0.25 | | 0.10 | 0.25 | V |
| | | $V_S$ = 2.7V, Load = 10mA | ● | | 0.20 | 0.35 | | 0.20 | 0.41 | V |
| | Output Voltage, High (Note 2) | $V_S$ = 5V, Load = 10k | ● | 4.90 | 4.99 | | 4.90 | 4.99 | | V |
| | | $V_S$ = 5V, Load = 5mA | ● | 4.85 | 4.90 | | 4.80 | 4.90 | | V |
| | | $V_S$ = 5V, Load = 10mA | ● | 4.75 | 4.81 | | 4.70 | 4.81 | | V |
| | Output Voltage, Low (Note 2) | $V_S$ = 5V, Load = 10k | ● | | 0.02 | 0.10 | | 0.02 | 0.10 | V |
| | | $V_S$ = 5V, Load = 5mA | ● | | 0.10 | 0.25 | | 0.10 | 0.30 | V |
| | | $V_S$ = 5V, Load = 10mA | ● | | 0.20 | 0.35 | | 0.20 | 0.42 | V |
| | Output Voltage, High (Note 2) | $V_S$ = ±5V, Load = 10k | ● | 4.90 | 4.99 | | 4.85 | 4.99 | | V |
| | | $V_S$ = ±5V, Load = 5mA | ● | 4.85 | 4.89 | | 4.80 | 4.89 | | V |
| | | $V_S$ = ±5V, Load = 10mA | ● | 4.65 | 4.80 | | 4.60 | 4.80 | | V |
| | Output Voltage, Low (Note 2) | $V_S$ = ±5V, Load = 10k | ● | | –4.99 | –4.90 | | –4.98 | –4.85 | V |
| | | $V_S$ = ±5V, Load = 5mA | ● | | –4.90 | –4.75 | | –4.90 | –4.75 | V |
| | | $V_S$ = ±5V, Load = 10mA | ● | | –4.80 | –4.65 | | –4.80 | –4.55 | V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Specifications applicable to all parts in the LTC1992 family.**

| SYMBOL | PARAMETER | CONDITIONS | | ALL C AND I GRADE MIN | ALL C AND I GRADE TYP | ALL C AND I GRADE MAX | ALL H GRADE MIN | ALL H GRADE TYP | ALL H GRADE MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{SC}$ | Output Short-Circuit Current Sourcing (Notes 2,3) | $V_S$ = 2.7V, $V_{OUT}$ = 1.35V | ● | 20 | 30 | | 20 | 30 | | mA |
| | | $V_S$ = 5V, $V_{OUT}$ = 2.5V | ● | 20 | 30 | | 20 | 30 | | mA |
| | | $V_S$ = ±5V, $V_{OUT}$ = 0V | ● | 20 | 30 | | 20 | 30 | | mA |
| | Output Short-Circuit Current Sinking (Notes 2,3) | $V_S$ = 2.7V, $V_{OUT}$ =1.35V | ● | 13 | 30 | | 13 | 30 | | mA |
| | | $V_S$ = 5V, $V_{OUT}$ = 2.5V | ● | 13 | 30 | | 13 | 30 | | mA |
| | | $V_S$ = ±5V, $V_{OUT}$ = 0V | ● | 13 | 30 | | 13 | 30 | | mA |
| $A_{VOL}$ | Large-Signal Voltage Gain | | ● | | 80 | | | 80 | | dB |

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Specifications applicable to the LTC1992 only.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1992CMS8 LTC1992ISM8 MIN | LTC1992CMS8 LTC1992ISM8 TYP | LTC1992CMS8 LTC1992ISM8 MAX | LTC1992HMS8 MIN | LTC1992HMS8 TYP | LTC1992HMS8 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_B$ | Input Bias Current | $V_S$ = 2.7V to ±5V | ● | | 2 | 250 | | 2 | 400 | pA |
| $I_{OS}$ | Input Offset Current | $V_S$ = 2.7V to ±5V | ● | | 0.1 | 100 | | 0.1 | 150 | pA |
| $R_{IN}$ | Input Resistance | | ● | | 500 | | | 500 | | MΩ |
| $C_{IN}$ | Input Capacitance | | ● | | 3 | | | 3 | | pF |
| $e_n$ | Input Referred Noise Voltage Density | f = 1kHz | | | 35 | | | 35 | | nV/√Hz |
| $i_n$ | Input Noise Current Density | f = 1kHz | | | 1 | | | 1 | | fA/√Hz |
| $V_{INCMR}$ | Input Signal Common Mode Range | | ● | $(-V_S)-0.1V$ | | $(+V_S)-1.3V$ | $(-V_S)-0.1V$ | | $(+V_S)-1.3V$ | V |
| CMRR | Common Mode Rejection Ratio (Input Referred) | $V_{INCM}$ = −0.1V to 3.7V | ● | 69 | 90 | | 69 | 90 | | dB |
| SR | Slew Rate (Note 4) | | ● | 0.5 | 1.5 | | 0.5 | 1.5 | | V/µs |
| GBW | Gain-Bandwidth Product ($f_{TEST}$ = 100kHz) | $T_A$ = 25°C | | 3.0 | 3.2 | 3.5 | 3.0 | 3.2 | 3.5 | MHz |
| | | LTC1992CMS8 | ● | 2.5 | 3.0 | 4.0 | | | | MHz |
| | | LTC1992IMS8/ LTC1992HMS8 | ● | 1.9 | | 4.0 | 1.9 | | 4.0 | MHz |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Typical values are at $T_A$ = 25°C. Specifications apply to the LTC1992-1 only.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1992-1CMS8 LTC1992-1IMS8 MIN | TYP | MAX | LTC1992-1HMS8 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $G_{DIFF}$ | Differential Gain | | | | 1 | | | 1 | | V/V |
| | Differential Gain Error | | ● | | ±0.1 | ±0.3 | | ±0.1 | ±0.35 | % |
| | Differential Gain Nonlinearity | | | | 50 | | | 50 | | ppm |
| | Differential Gain Temperature Coefficient | | ● | | 3.5 | | | 3.5 | | ppm/°C |
| $e_n$ | Input Referred Noise Voltage Density (Note 7) | f = 1kHz | | | 45 | | | 45 | | nV/√Hz |
| $R_{IN}$ | Input Resistance, Single-Ended +IN, –IN Pins | | ● | 22.5 | 30 | 37.5 | 22 | 30 | 38 | kΩ |
| $V_{INCMR}$ | Input Signal Common Mode Range | $V_S$ = 5V | | | –0.1V to 4.9V | | | –0.1V to 4.9V | | V |
| CMRR | Common Mode Rejection Ratio (Amplifier Input Referred) (Note 7) | $V_{INCM}$ = –0.1V to 3.7V | ● | 55 | 60 | | 55 | 60 | | dB |
| SR | Slew Rate (Note 4) | | ● | 0.5 | 1.5 | | 0.5 | 1.5 | | V/µs |
| GBW | Gain-Bandwidth Product | $f_{TEST}$ = 180kHz | | | 3 | | | 3 | | MHz |

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Typical values are at $T_A$ = 25°C. Specifications apply to the LTC1992-2 only.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1992-2CMS8 LTC1992-2IMS8 MIN | TYP | MAX | LTC1992-2HMS8 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $G_{DIFF}$ | Differential Gain | | | | 2 | | | 2 | | V/V |
| | Differential Gain Error | | ● | | ±0.1 | ±0.3 | | ±0.1 | ±0.35 | % |
| | Differential Gain Nonlinearity | | | | 50 | | | 50 | | ppm |
| | Differential Gain Temperature Coefficient | | ● | | 3.5 | | | 3.5 | | ppm/°C |
| $e_n$ | Input Referred Noise Voltage Density (Note 7) | f = 1kHz | | | 45 | | | 45 | | nV/√Hz |
| $R_{IN}$ | Input Resistance, Single-Ended +IN, –IN Pins | | ● | 22.5 | 30 | 37.5 | 22 | 30 | 38 | kΩ |
| $V_{INCMR}$ | Input Signal Common Mode Range | $V_S$ = 5V | | | –0.1V to 4.9V | | | –0.1V to 4.9V | | V |
| CMRR | Common Mode Rejection Ratio (Amplifier Input Referred) (Note 7) | $V_{INCM}$ = –0.1V to 3.7V | ● | 55 | 60 | | 55 | 60 | | dB |
| SR | Slew Rate (Note 4) | | ● | 0.7 | 2 | | 0.7 | 2 | | V/µs |
| GBW | Gain-Bandwidth Product | $f_{TEST}$ = 180kHz | | | 4 | | | 4 | | MHz |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Typical values are at $T_A$ = 25°C. Specifications apply to the LTC1992-5 only.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1992-5CMS8 LTC1992-5IMS8 MIN | TYP | MAX | LTC1992-5HMS8 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $G_{DIFF}$ | Differential Gain | | | | 5 | | | 5 | | V/V |
| | Differential Gain Error | | ● | | ±0.1 | ±0.3 | | ±0.1 | ±0.35 | % |
| | Differential Gain Nonlinearity | | | | 50 | | | 50 | | ppm |
| | Differential Gain Temperature Coefficient | | ● | | 3.5 | | | 3.5 | | ppm/°C |
| $e_n$ | Input Referred Noise Voltage Density (Note 7) | f = 1kHz | | | 45 | | | 45 | | nV/√Hz |
| $R_{IN}$ | Input Resistance, Single-Ended +IN, –IN Pins | | ● | 22.5 | 30 | 37.5 | 22 | 30 | 38 | kΩ |
| $V_{INCMR}$ | Input Signal Common Mode Range | $V_S$ = 5V | | | –0.1V to 3.9V | | | –0.1V to 3.9V | | V |
| CMRR | Common Mode Rejection Ratio (Amplifier Input Referred) (Note 7) | $V_{INCM}$ = –0.1V to 3.7V | ● | 55 | 60 | | 55 | 60 | | dB |
| SR | Slew Rate (Note 4) | | ● | 0.7 | 2 | | 0.7 | 2 | | V/µs |
| GBW | Gain-Bandwidth Product | $f_{TEST}$ = 180kHz | | | 4 | | | 4 | | MHz |

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $+V_S$ = 5V, $-V_S$ = 0V, $V_{INCM}$ = $V_{OUTCM}$ = $V_{OCM}$ = 2.5V, unless otherwise noted. $V_{OCM}$ is the voltage on the $V_{OCM}$ pin. $V_{OUTCM}$ is defined as $(+V_{OUT} + -V_{OUT})/2$. $V_{INCM}$ is defined as $(+V_{IN} + -V_{IN})/2$. $V_{INDIFF}$ is defined as $(+V_{IN} - -V_{IN})$. $V_{OUTDIFF}$ is defined as $(+V_{OUT} - -V_{OUT})$. Typical values are at $T_A$ = 25°C. Specifications apply to the LTC1992-10 only.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1992-10CMS8 LTC1992-10IMS8 MIN | TYP | MAX | LTC1992-10HMS8 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $G_{DIFF}$ | Differential Gain | | | | 10 | | | 10 | | V/V |
| | Differential Gain Error | | ● | | ±0.1 | ±0.3 | | ±0.1 | ±0.35 | % |
| | Differential Gain Nonlinearity | | | | 50 | | | 50 | | ppm |
| | Differential Gain Temperature Coefficient | | ● | | 3.5 | | | 3.5 | | ppm/°C |
| $e_n$ | Input Referred Noise Voltage Density (Note 7) | f = 1kHz | | | 45 | | | 45 | | nV/√Hz |
| $R_{IN}$ | Input Resistance, Single-Ended +IN, –IN Pins | | ● | 11.3 | 15 | 18.8 | 11 | 15 | 19 | kΩ |
| $V_{INCMR}$ | Input Signal Common Mode Range | $V_S$ = 5V | | | –0.1V to 3.8V | | | –0.1V to 3.8V | | V |
| CMRR | Common Mode Rejection Ratio (Amplifier Input Referred) (Note 7) | $V_{INCM}$ = –0.1V to 3.7V | ● | 55 | 60 | | 55 | 60 | | dB |
| SR | Slew Rate (Note 4) | | ● | 0.7 | 2 | | 0.7 | 2 | | V/µs |
| GBW | Gain-Bandwidth Product | $f_{TEST}$ = 180kHz | | | 4 | | | 4 | | MHz |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Output load is connected to the midpoint of the $+V_S$ and $-V_S$ potentials. Measurement is taken single-ended, one output loaded at a time.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum when the output is shorted indefinitely.

**Note 4:** Differential output slew rate. Slew rate is measured single ended and doubled to get the listed numbers.

**Note 5:** The LTC1992C/LTC1992-XC/LTC1992I/LTC1992-XI are guaranteed functional over an operating temperature of –40°C to 85°C. The LTC1992H/LTC1992-XH are guaranteed functional over the extended operating temperature of –40°C to 125°C.

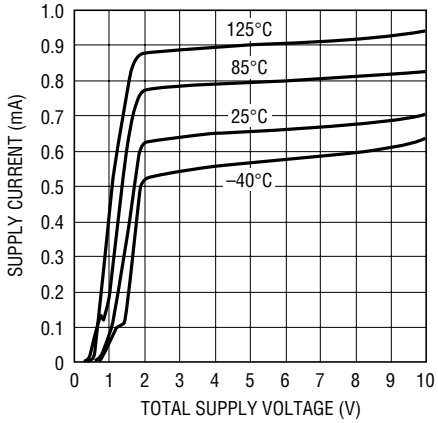
**Note 6:** The LTC1992C/LTC1992-XC are guaranteed to meet the specified performance limits over the 0°C to 70°C temperature range and are designed, characterized and expected to meet the specified performance limits over the –40°C to 85°C temperature range but are not tested or QA sampled at these temperatures. The LTC1992I/LTC1992-XI are guaranteed to meet the specified performance limits over the –40°C to 85°C temperature range. The LTC1992H/LTC1992-XH are guaranteed to meet the specified performance limits over the –40°C to 125°C temperature range.

**Note 7:** Differential offset voltage, differential offset voltage drift, CMRR, noise voltage density and PSRR are referred to the internal amplifier's input to allow for direct comparison of gain blocks with discrete amplifiers.

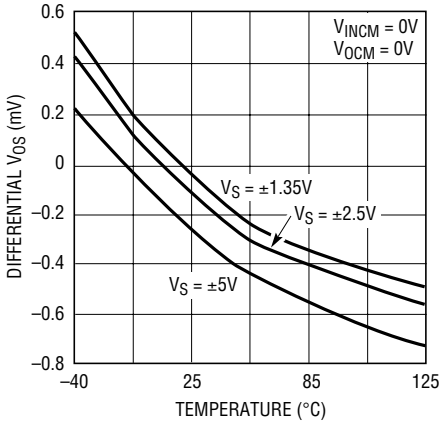
## TYPICAL PERFORMANCE CHARACTERISTICS

**Applicable to all parts in the LTC1992 family.**

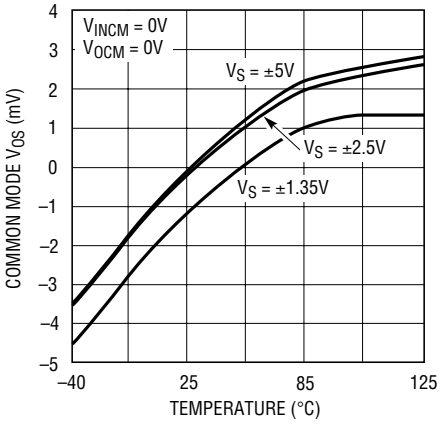
### Supply Current vs Supply Voltage



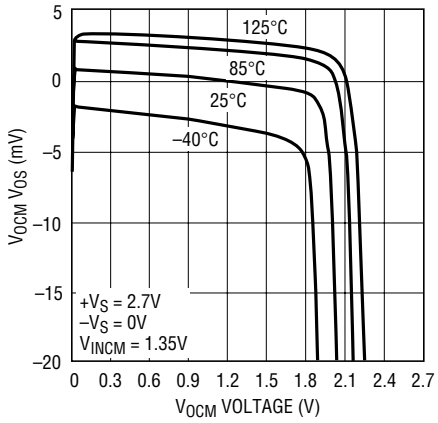

### Differential Input Offset Voltage vs Temperature (Note 7)



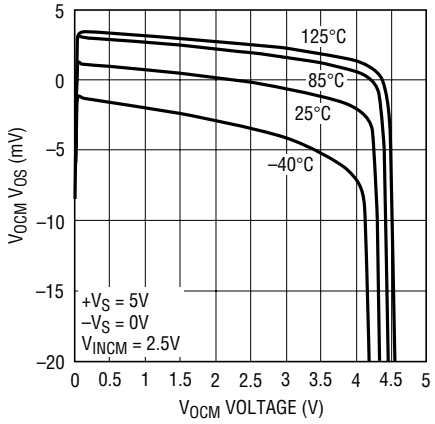

### Common Mode Offset Voltage vs Temperature



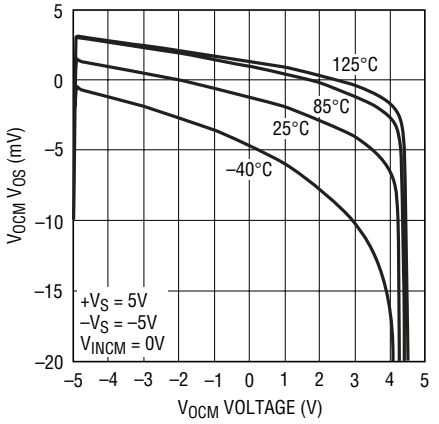

### Common Mode Offset Voltage vs $V_{OCM}$ Voltage



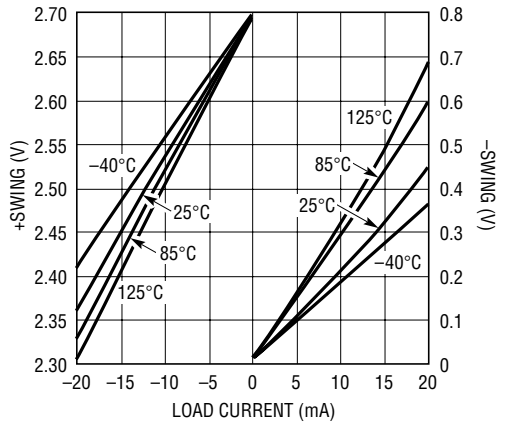

### Common Mode Offset Voltage vs $V_{OCM}$ Voltage



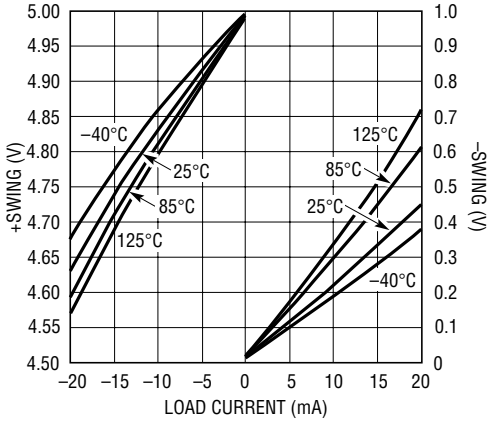

### Common Mode Offset Voltage vs $V_{OCM}$ Voltage




### Output Voltage Swing vs Output Load, $V_S$ = 2.7V



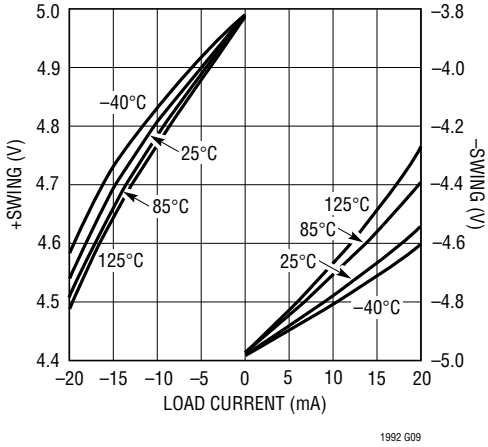

### Output Voltage Swing vs Output Load, $V_S$ = 5V



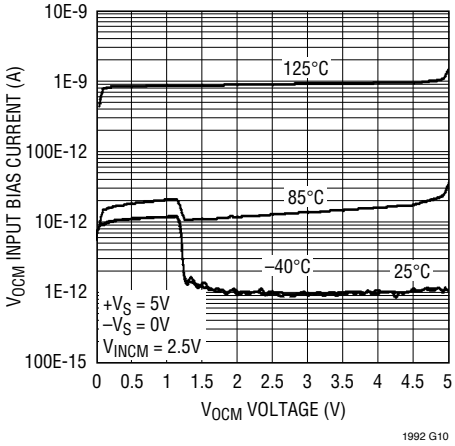
## TYPICAL PERFORMANCE CHARACTERISTICS

**Applicable to all parts in the LTC1992 family.**

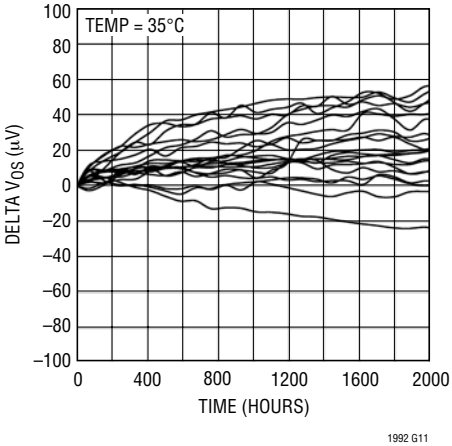
### Output Voltage Swing vs Output Load, $V_S$ = ±5V



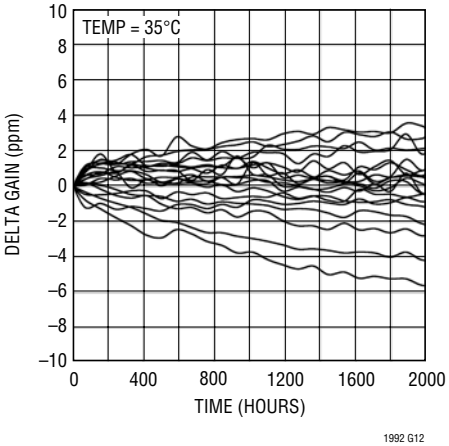

### $V_{OCM}$ Input Bias Current vs $V_{OCM}$ Voltage



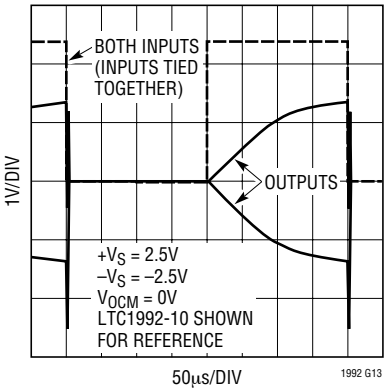

### Differential Input Offset Voltage vs Time (Normalized to t = 0)



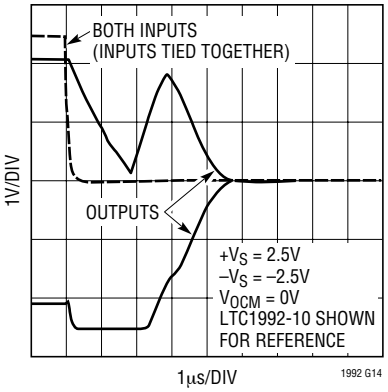

### Differential Gain vs Time (Normalized to t = 0)



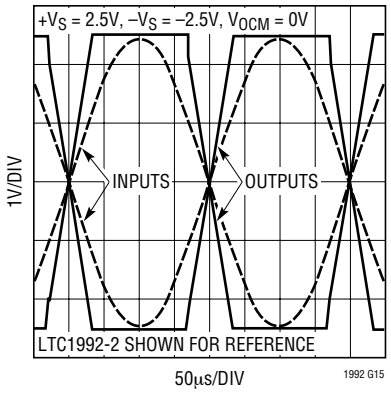

### Input Common Mode Overdrive Recovery (Expanded View)



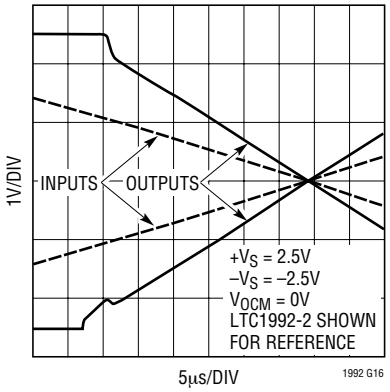

### Input Common Mode Overdrive Recovery (Detailed View)




### Output Overdrive Recovery (Expanded View)

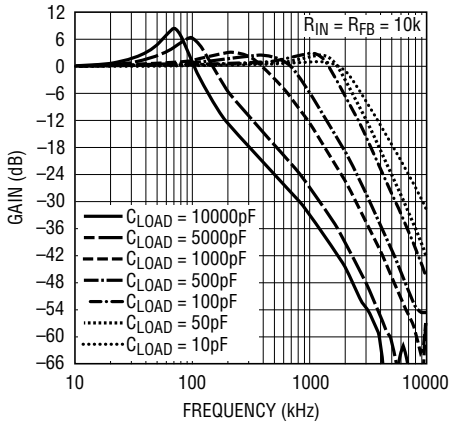



### Output Overdrive Recovery (Detailed View)

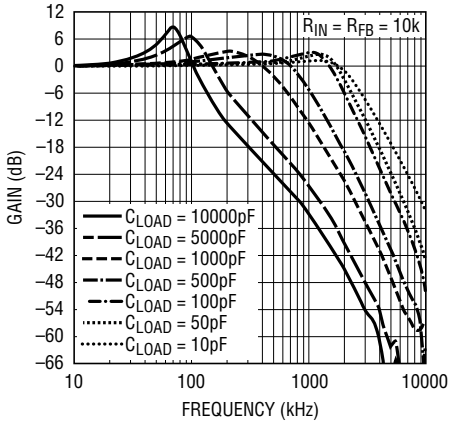


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992 only.

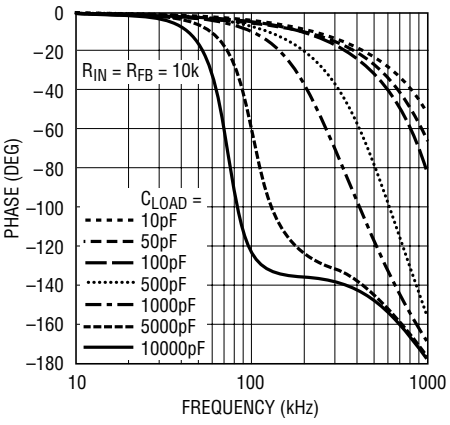
### Differential Input Differential Gain vs Frequency, $V_S$ = ±2.5V



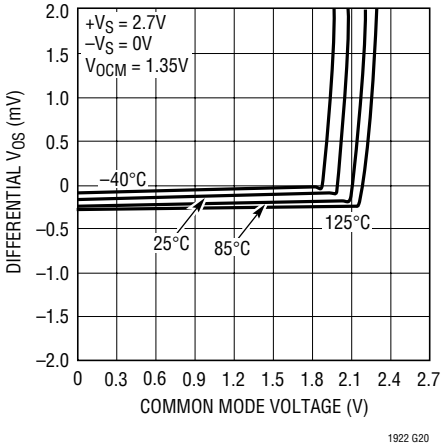

### Single-Ended Input Differential Gain vs Frequency, $V_S$ = ±2.5V



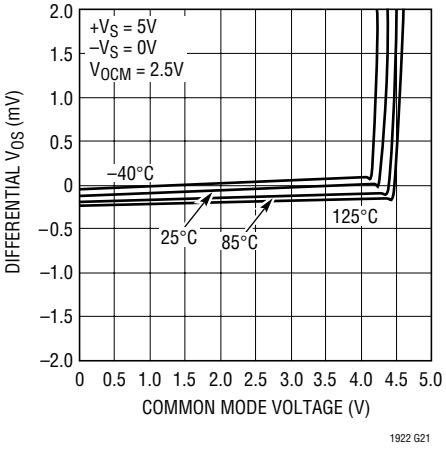

### Differential Phase Response vs Frequency



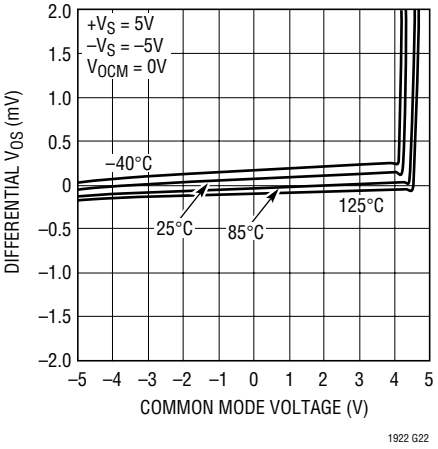

### Differential Input Offset Voltage vs Input Common Mode Voltage



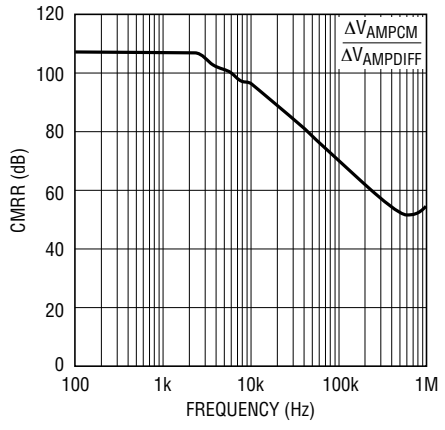

### Differential Input Offset Voltage vs Input Common Mode Voltage



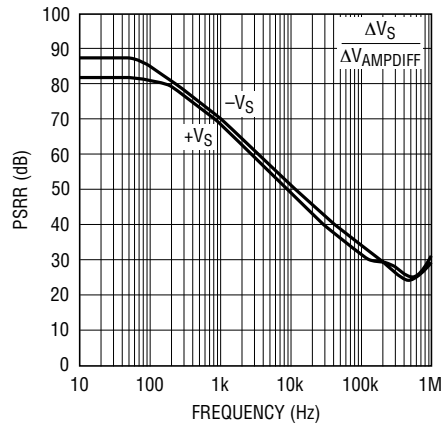

### Differential Input Offset Voltage vs Input Common Mode Voltage



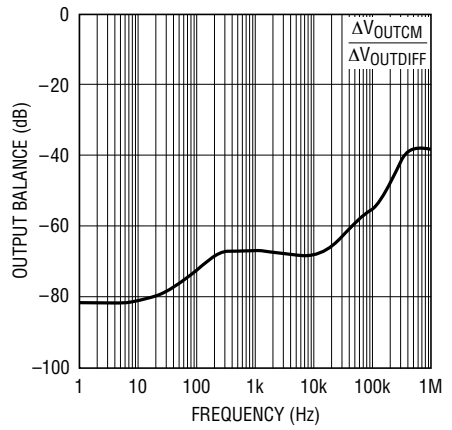

### Common Mode Rejection Ratio vs Frequency (Note 7)




### Power Supply Rejection Ratio vs Frequency (Note 7)

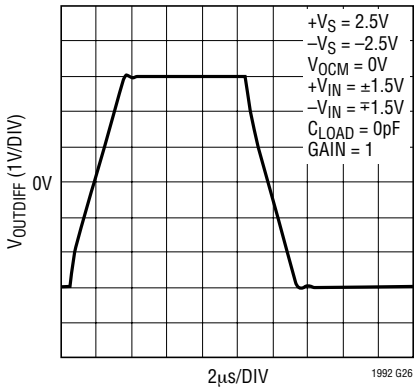



### Output Balance vs Frequency

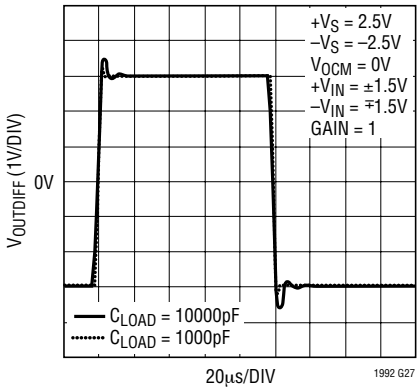


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992 only.

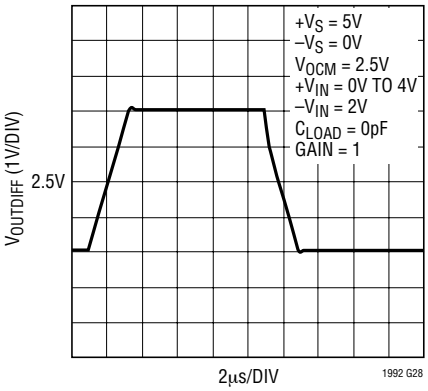
### Differential Input Large-Signal Step Response



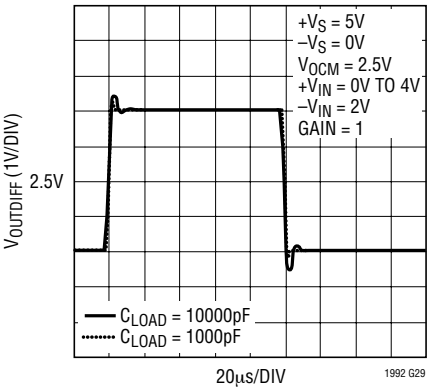

### Differential Input Large-Signal Step Response



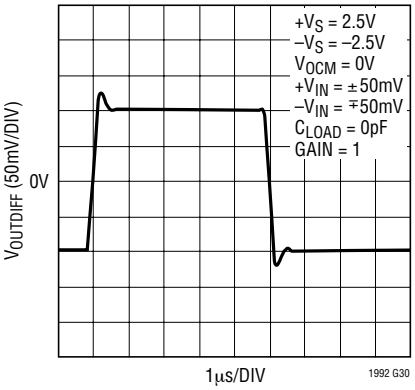

### Single-Ended Input Large-Signal Step Response



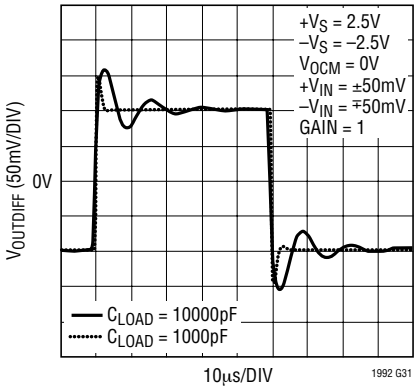

### Single-Ended Input Large-Signal Step Response




### Differential Input Small-Signal Step Response

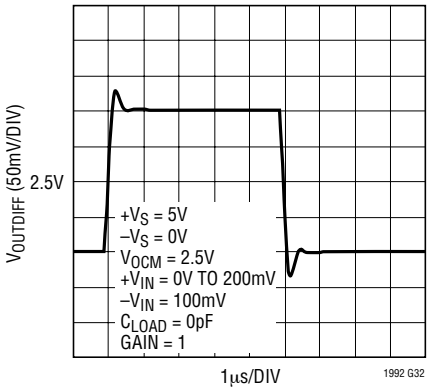



### Differential Input Small-Signal Step Response

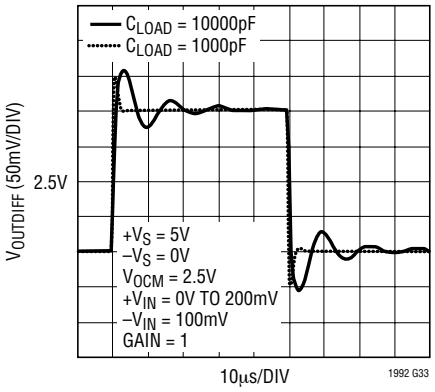


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992 only.

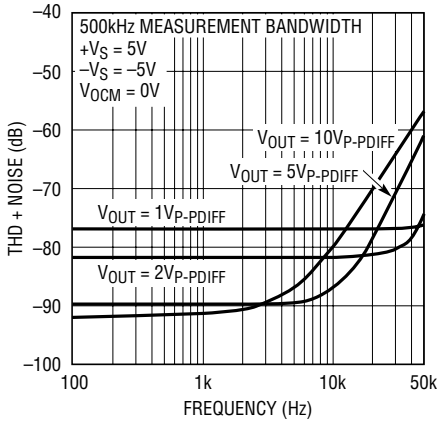
### Single-Ended Input Small-Signal Step Response



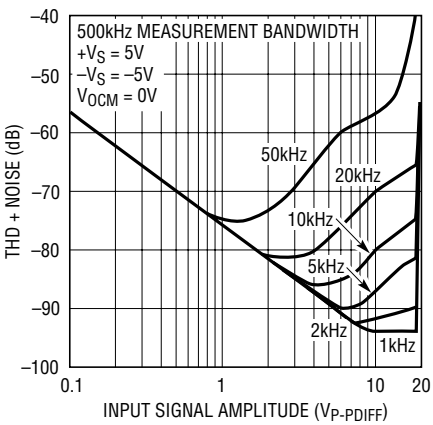

### Single-Ended Input Small-Signal Step Response



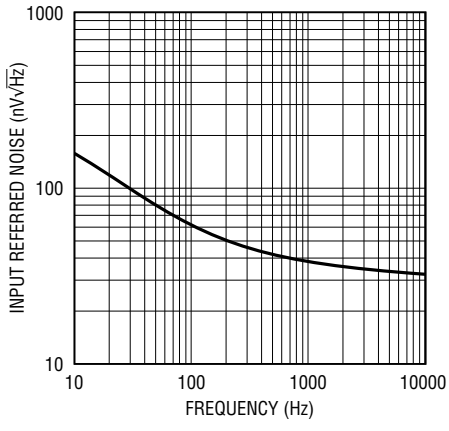

### THD + Noise vs Frequency



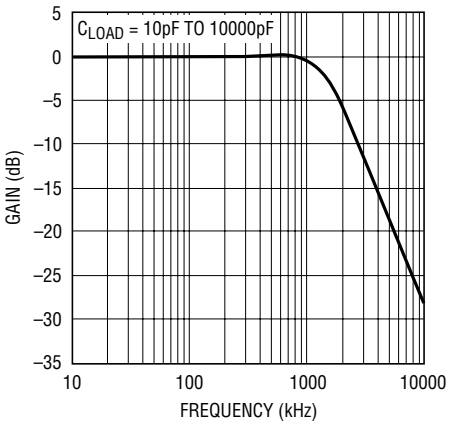

### THD + Noise vs Amplitude




### Differential Noise Voltage Density vs Frequency

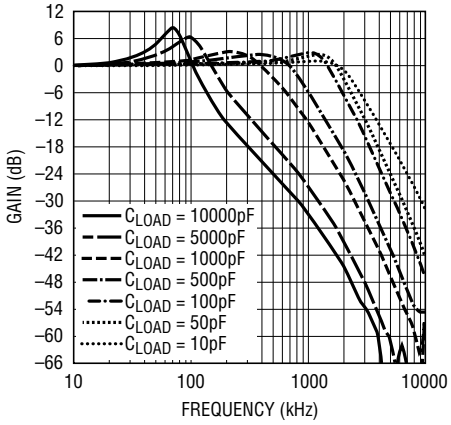



### $V_{OCM}$ Gain vs Frequency, $V_S = \pm 2.5V$

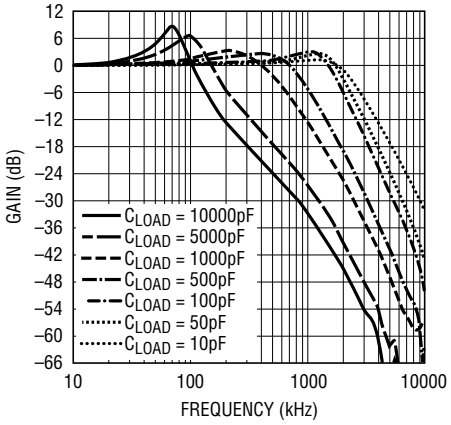


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-1 only.

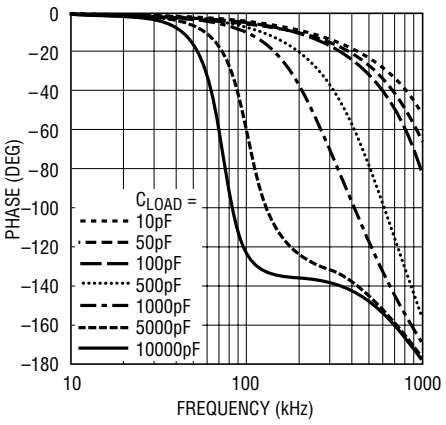
### Differential Input Differential Gain vs Frequency, $V_S$ = ±2.5V



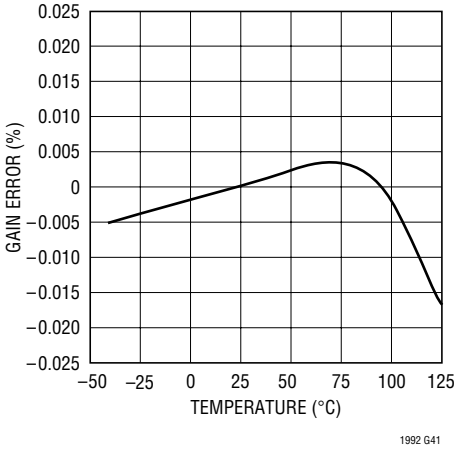

### Single-Ended Input Differential Gain vs Frequency, $V_S$ = ±2.5V



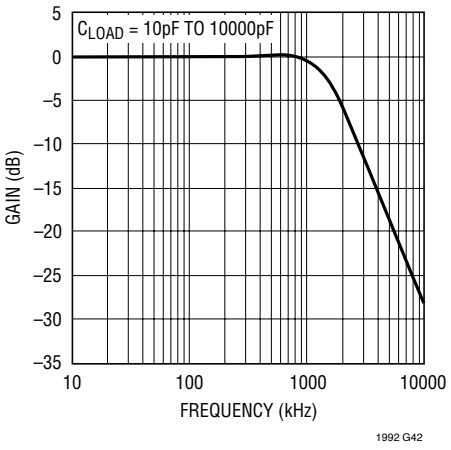

### Differential Phase Response vs Frequency



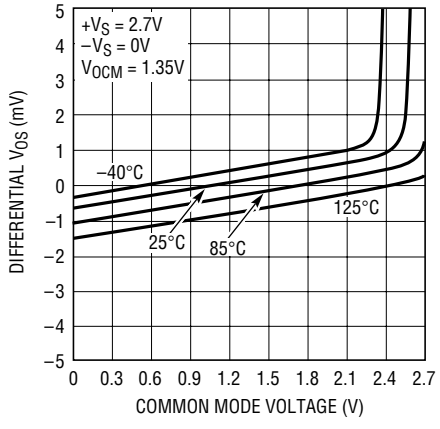

### Differential Gain Error vs Temperature



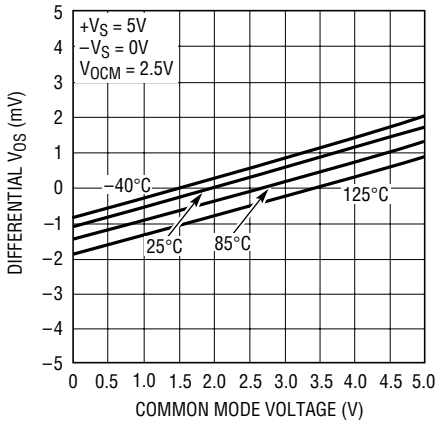

### $V_{OCM}$ Gain vs Frequency



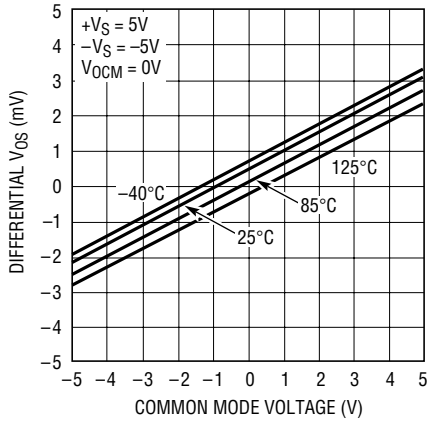

### Differential Input Offset Voltage vs Input Common Mode Voltage




### Differential Input Offset Voltage vs Input Common Mode Voltage

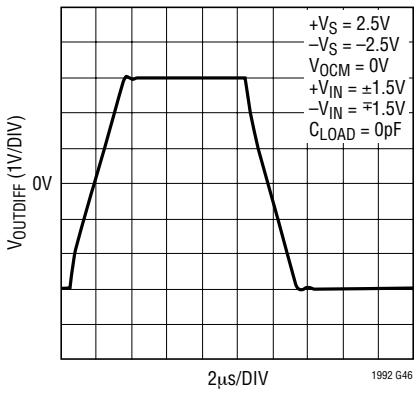



### Differential Input Offset Voltage vs Input Common Mode Voltage

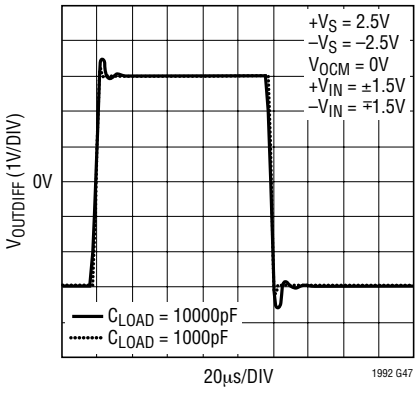


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-1 only.

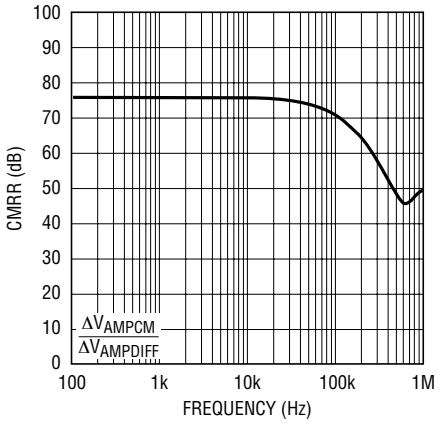
### Differential Input Large-Signal Step Response



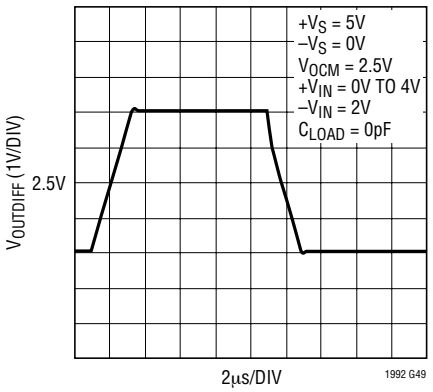

### Differential Input Large-Signal Step Response



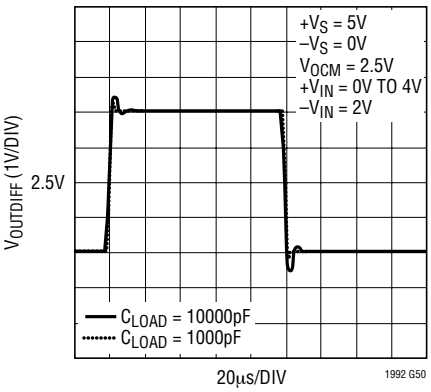

### Common Mode Rejection Ratio vs Frequency



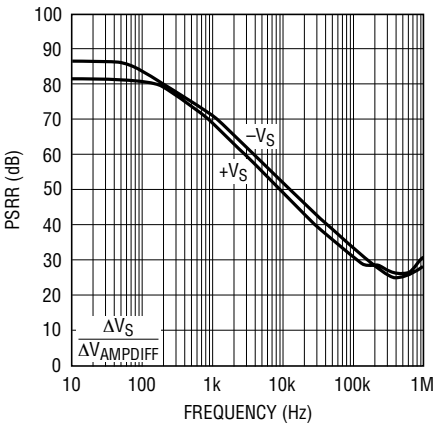

### Single-Ended Input Large-Signal Step Response



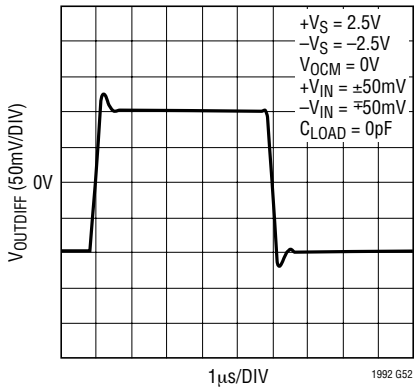

### Single-Ended Input Large-Signal Step Response



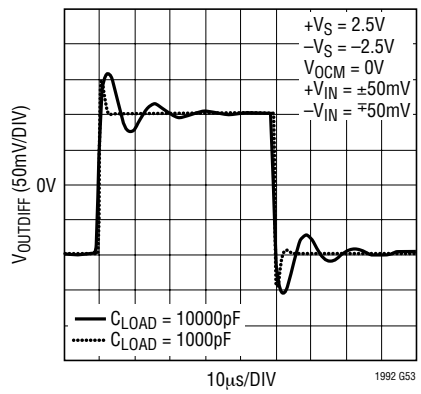

### Power Supply Rejection Ratio vs Frequency



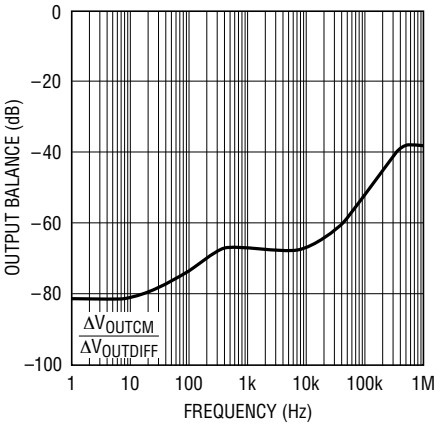

### Differential Input Small-Signal Step Response




### Differential Input Small-Signal Step Response

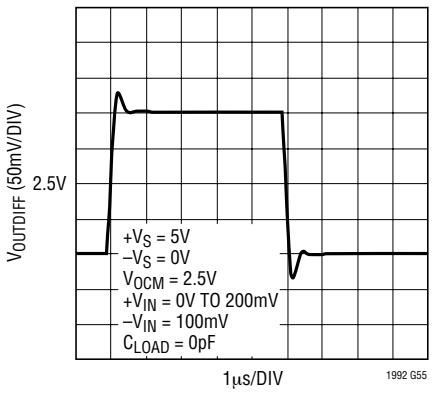



### Output Balance vs Frequency

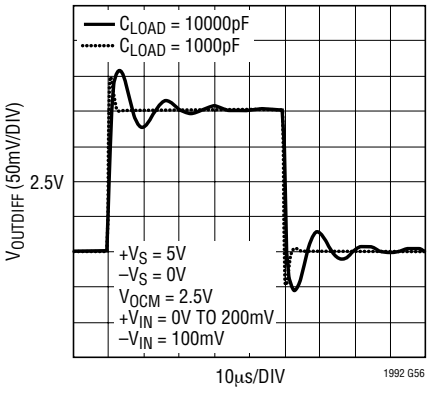


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-1 only.

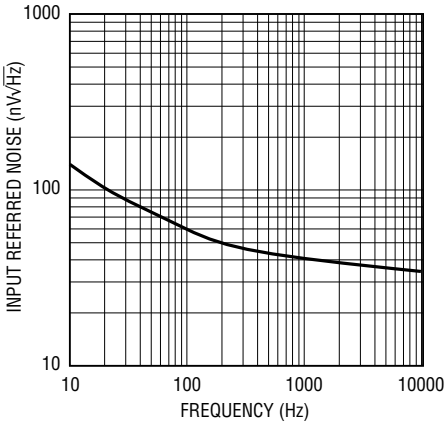
### Single-Ended Input Small-Signal Step Response



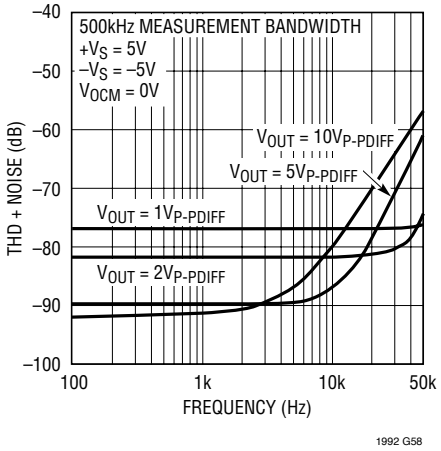

### Single-Ended Input Small-Signal Step Response



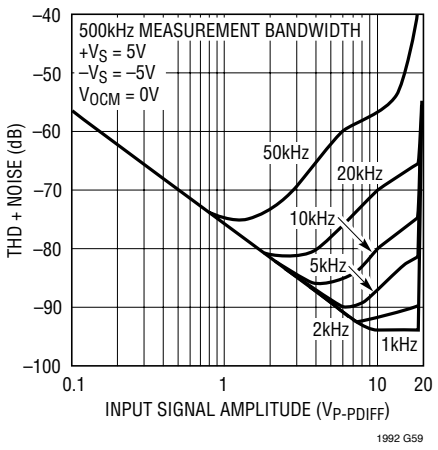

### Differential Noise Voltage Density vs Frequency




### THD + Noise vs Frequency

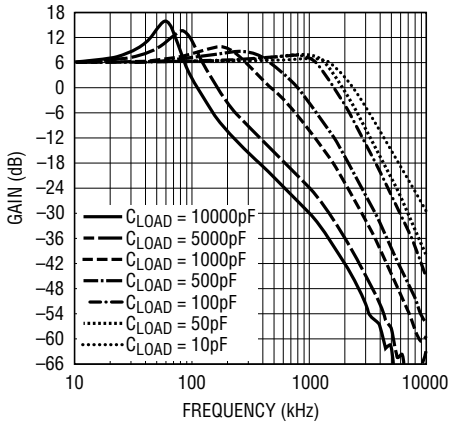



### THD + Noise vs Amplitude

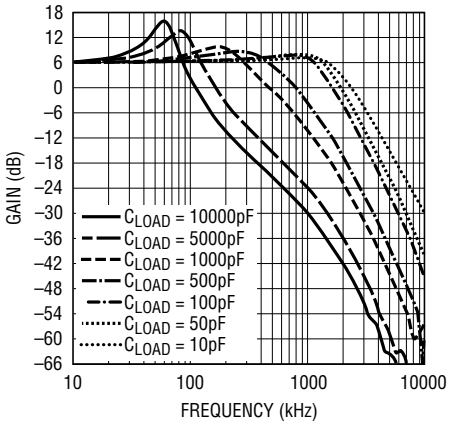


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-2 only.

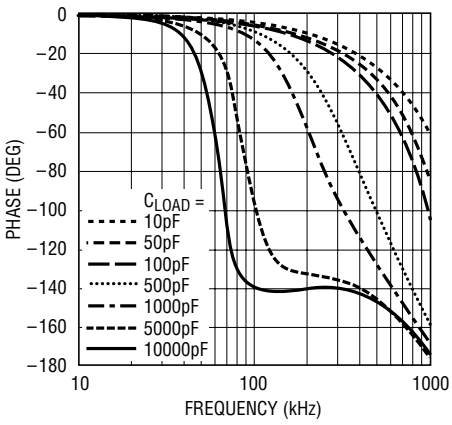
### Differential Input Differential Gain vs Frequency, $V_S$ = ±2.5V



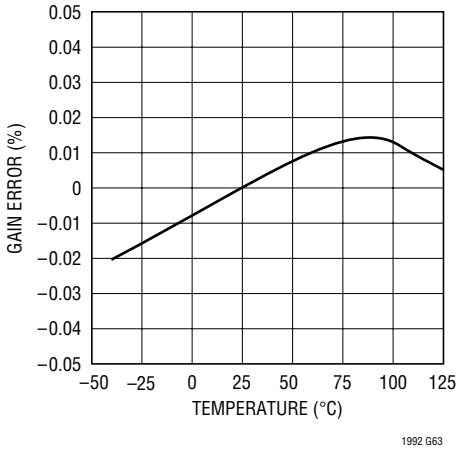

### Single-Ended Input Differential Gain vs Frequency, $V_S$ = ±2.5V



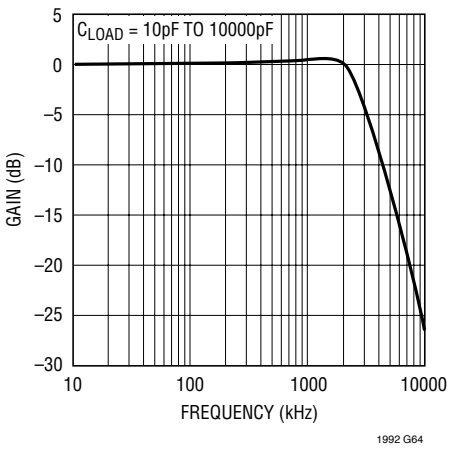

### Differential Phase Response vs Frequency



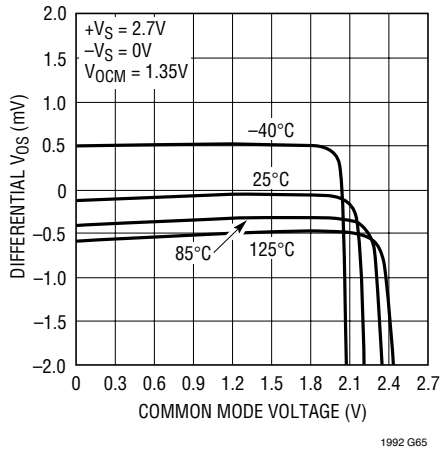

### Differential Gain Error vs Temperature



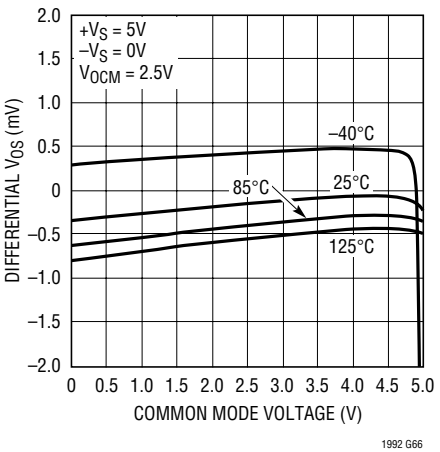

### $V_{OCM}$ Gain vs Frequency, $V_S$ = ±2.5V



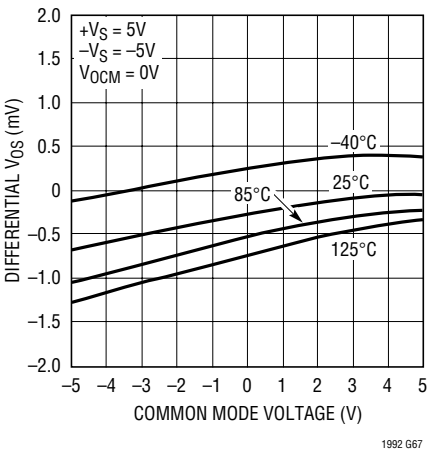

### Differential Input Offset Voltage vs Input Common Mode Voltage (Note 7)




### Differential Input Offset Voltage vs Input Common Mode Voltage (Note 7)

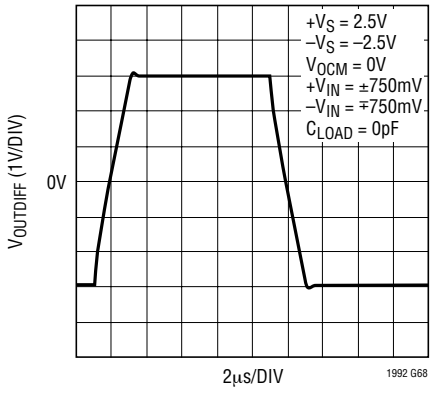



### Differential Input Offset Voltage vs Input Common Mode Voltage (Note 7)

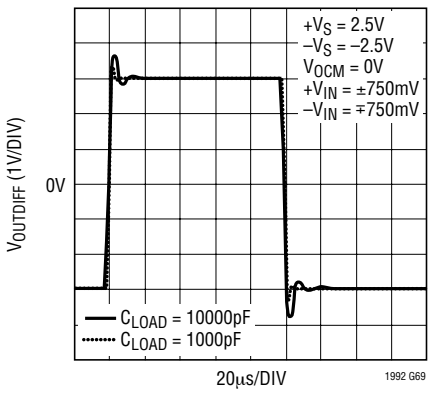


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-2 only.

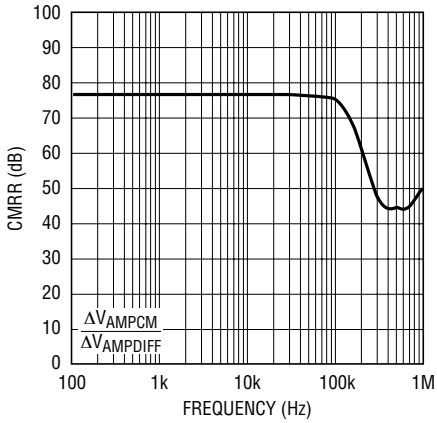
### Differential Input Large-Signal Step Response



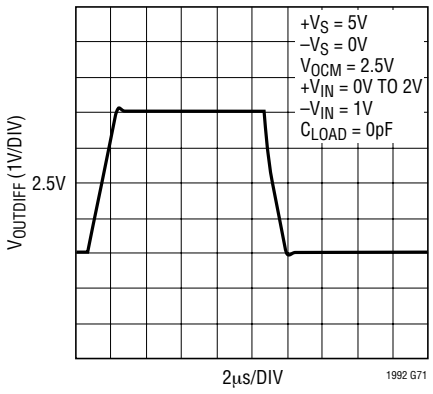

### Differential Input Large-Signal Step Response



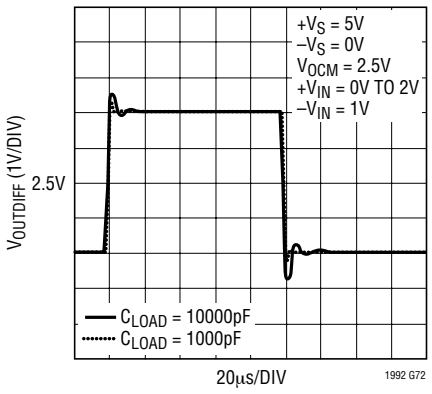

### Common Mode Rejection Ratio vs Frequency (Note 7)



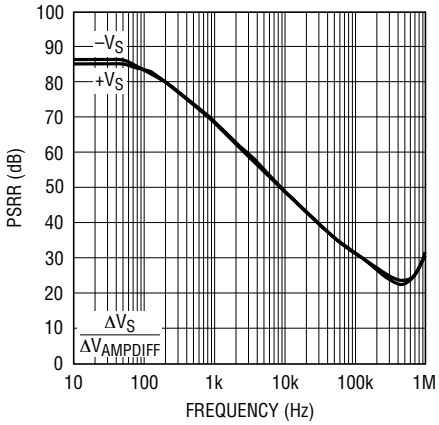

### Single-Ended Input Large-Signal Step Response



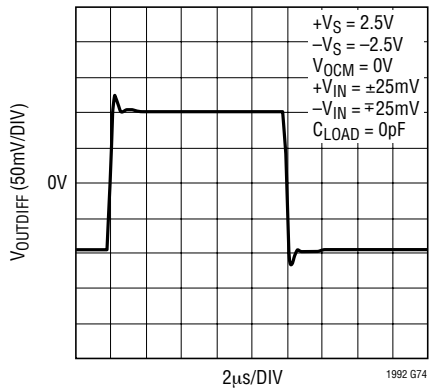

### Single-Ended Input Large-Signal Step Response



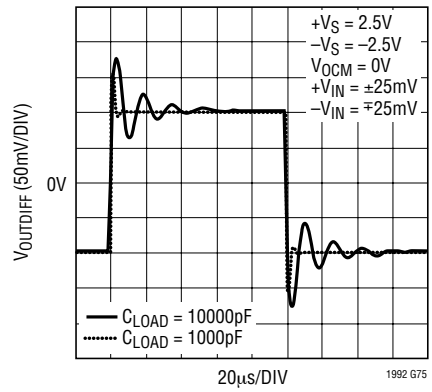

### Power Supply Rejection Ratio vs Frequency (Note 7)



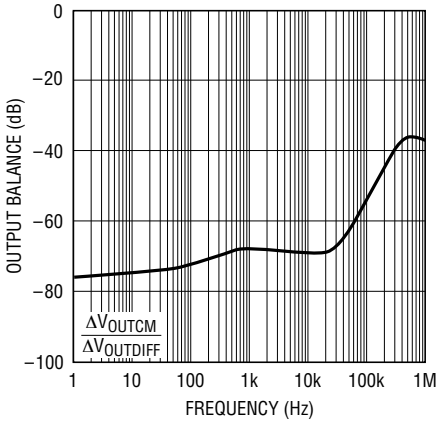

### Differential Input Small-Signal Step Response




### Differential Input Small-Signal Step Response

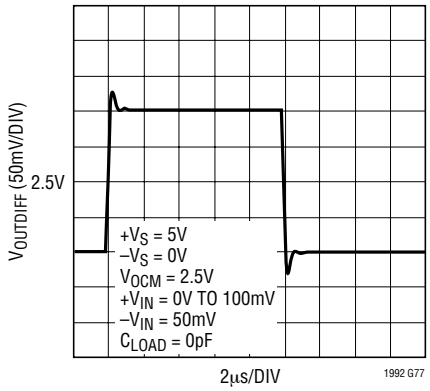



### Output Balance vs Frequency

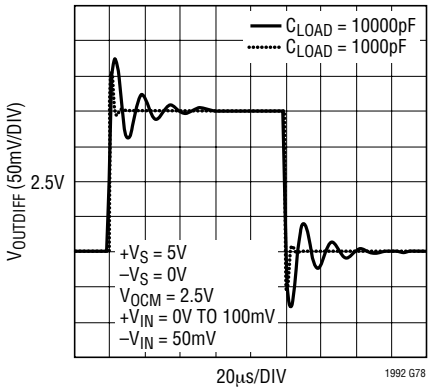


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-2 only.

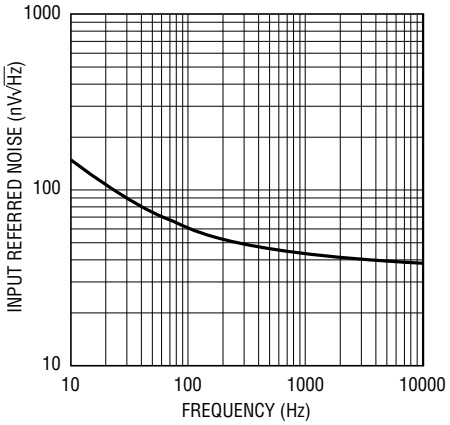
### Single-Ended Input Small-Signal Step Response



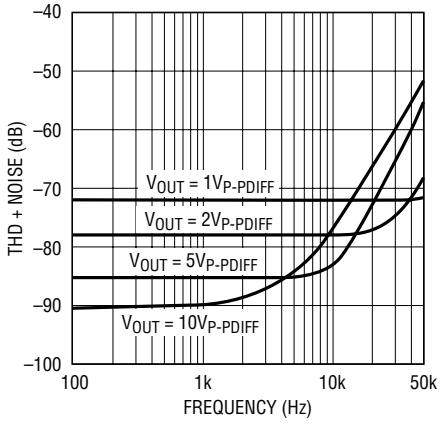

### Single-Ended Input Small-Signal Step Response



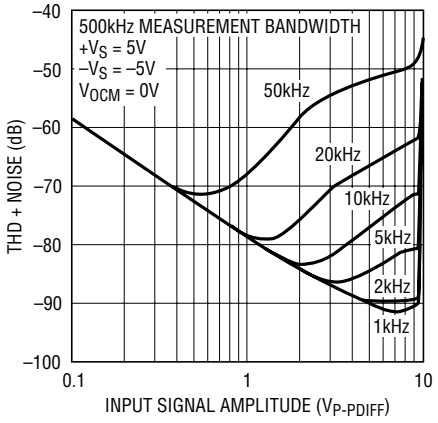

### Differential Noise Voltage Density vs Frequency




### THD + Noise vs Frequency

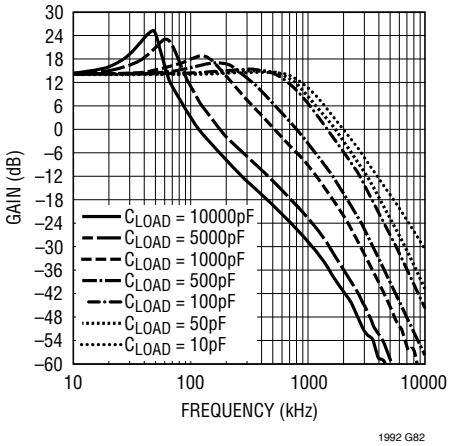



### THD + Noise vs Amplitude

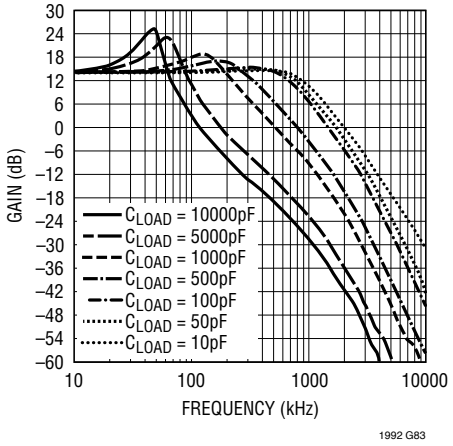


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-5 only.

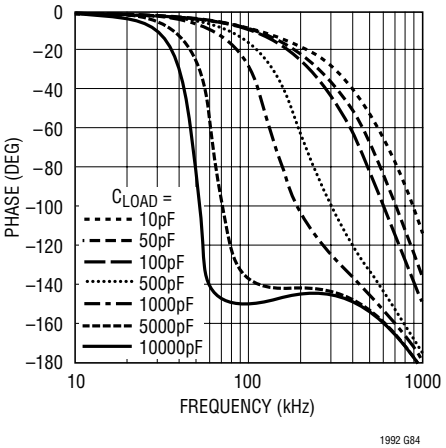
### Differential Input Differential Gain vs Frequency, $V_S$ = ±2.5V



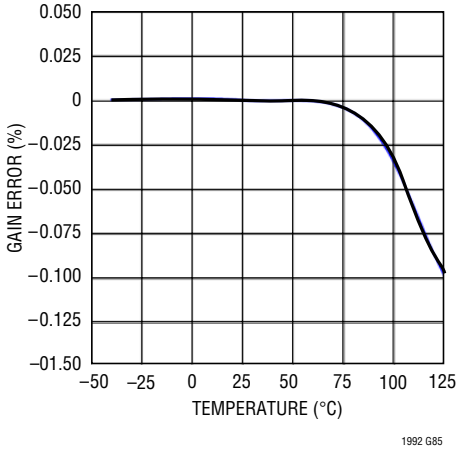

### Single-Ended Input Differential Gain vs Frequency, $V_S$ = ±2.5V



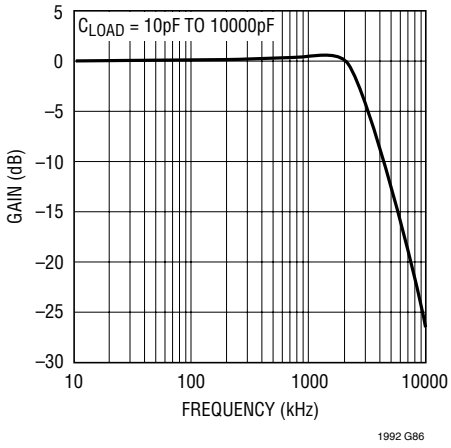

### Differential Phase Response vs Frequency



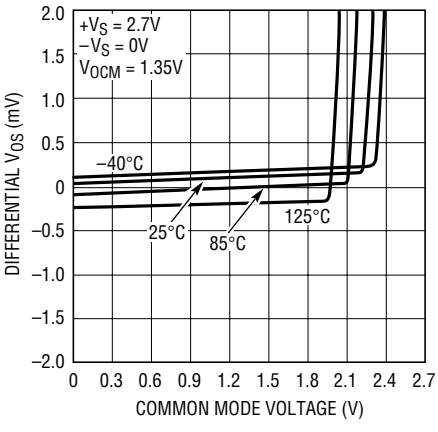

### Differential Gain Error vs Temperature



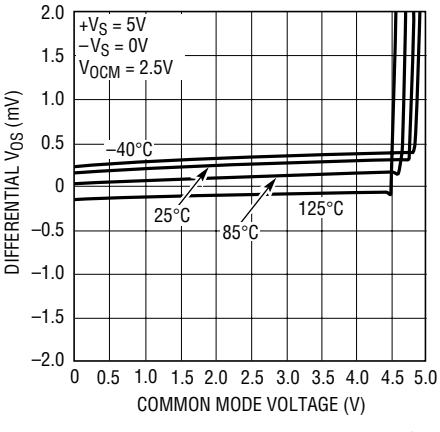

### $V_{OCM}$ Gain vs Frequency



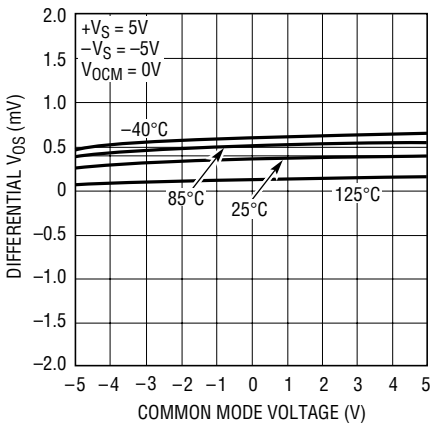

### Differential Input Offset Voltage vs Input Common Mode Voltage




### Differential Input Offset Voltage vs Input Common Mode Voltage

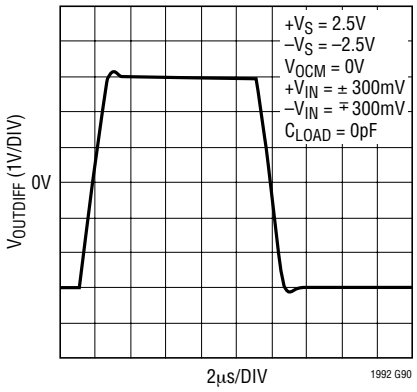



### Differential Input Offset Voltage vs Input Common Mode Voltage

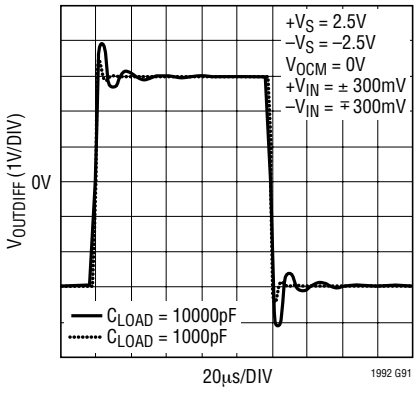


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-5 only.

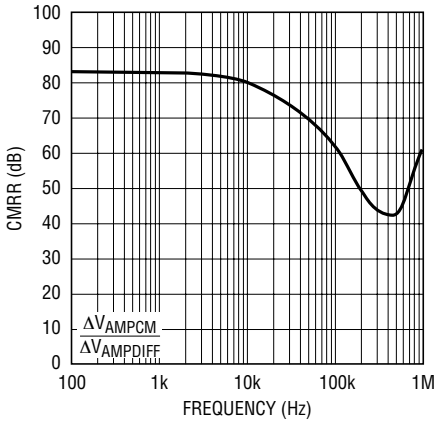
### Differential Input Large-Signal Step Response



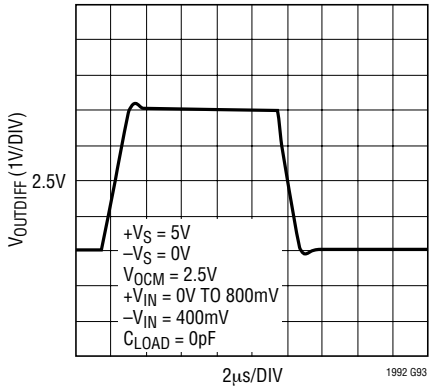

### Differential Input Large-Signal Step Response



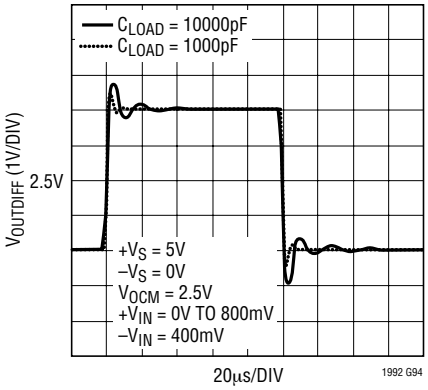

### Common Mode Rejection Ratio vs Frequency (Note 7)



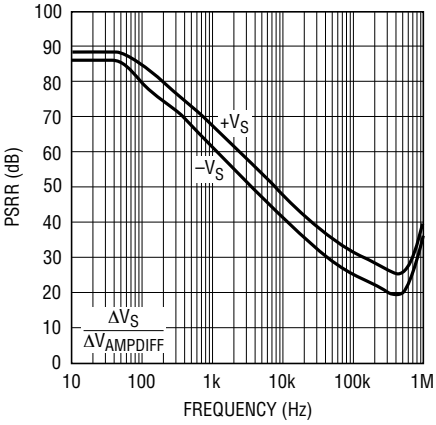

### Single-Ended Input Large-Signal Step Response



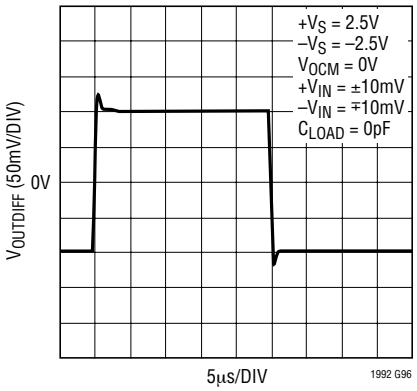

### Single-Ended Input Large-Signal Step Response



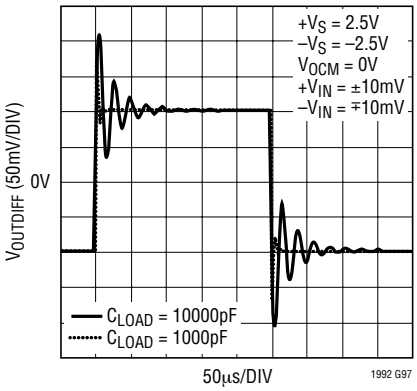

### Power Supply Rejection Ratio vs Frequency (Note 7)



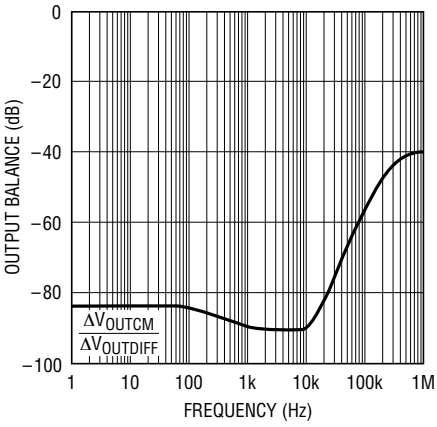

### Differential Input Small-Signal Step Response




### Differential Input Small-Signal Step Response

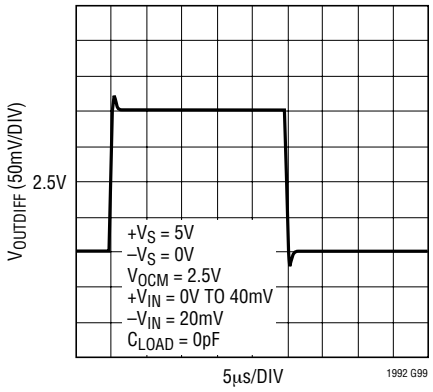



### Output Balance vs Frequency

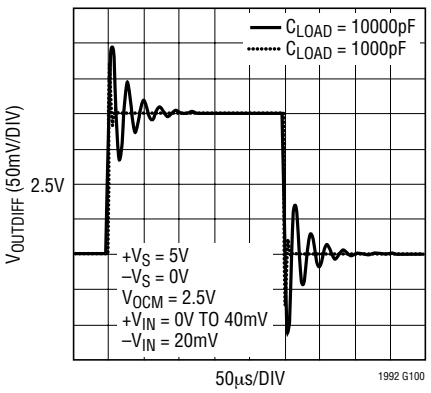


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-5 only.

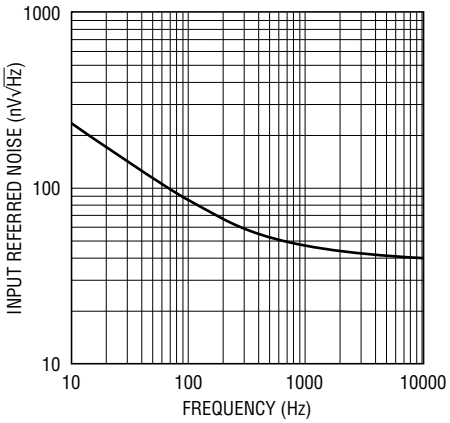
### Single-Ended Input Small-Signal Step Response



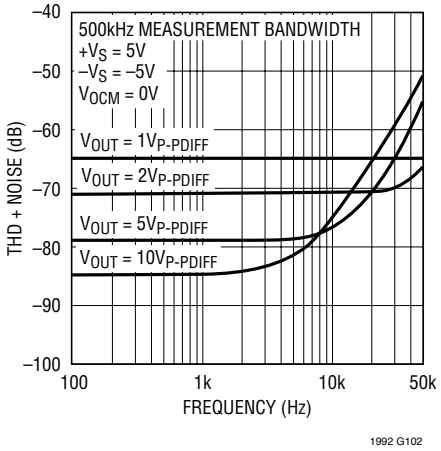

### Single-Ended Input Small-Signal Step Response



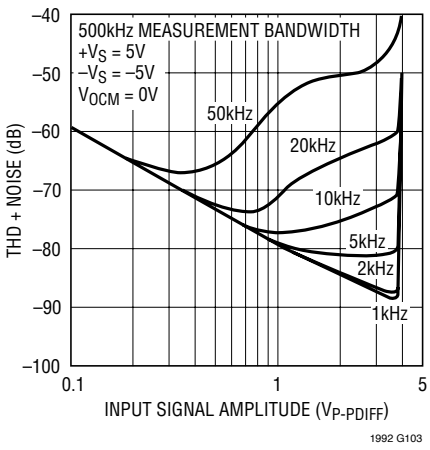

### Differential Noise Voltage Density vs Frequency




### THD + Noise vs Frequency

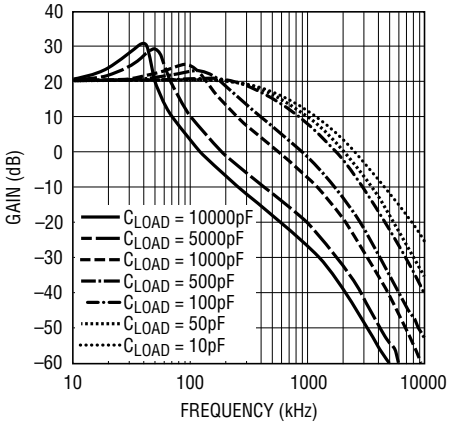



### THD + Noise vs Amplitude

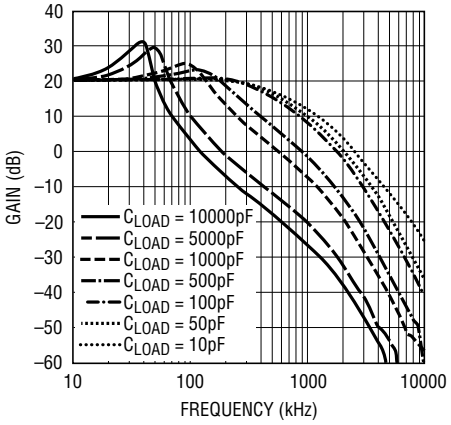


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-10 only.

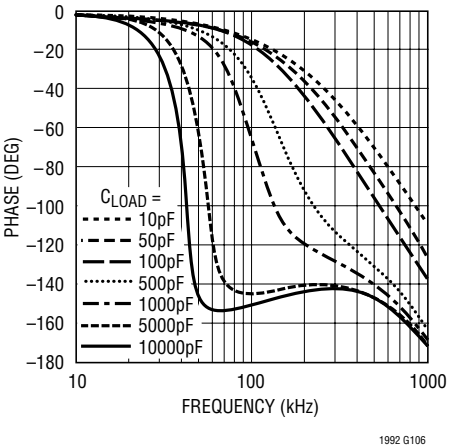
### Differential Input Differential Gain vs Frequency, $V_S$ = ±2.5V



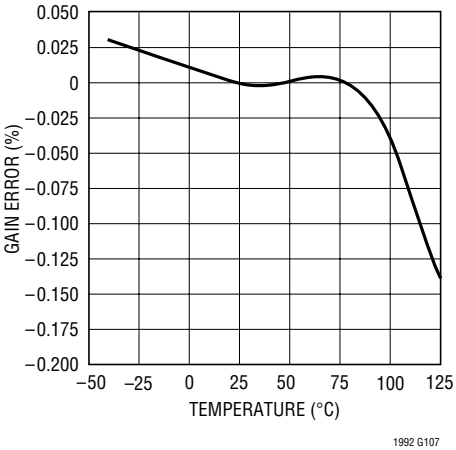

### Single-Ended Input Differential Gain vs Frequency, $V_S$ = ±2.5V



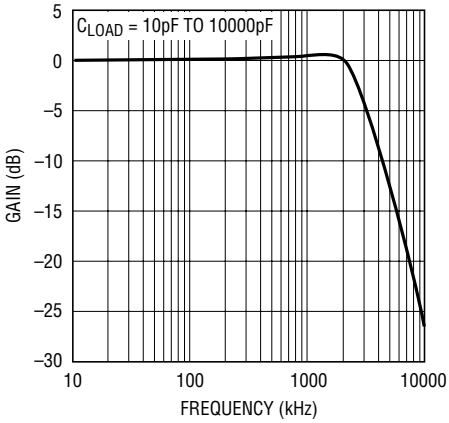

### Differential Phase Response vs Frequency



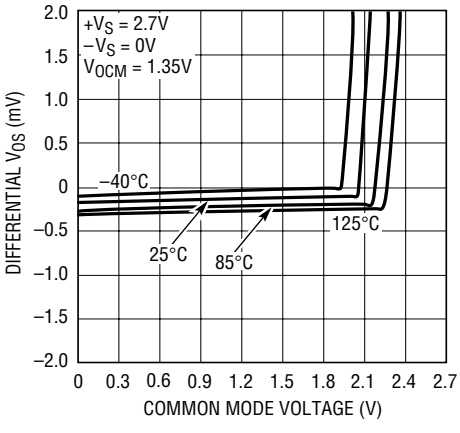

### Differential Gain Error vs Temperature



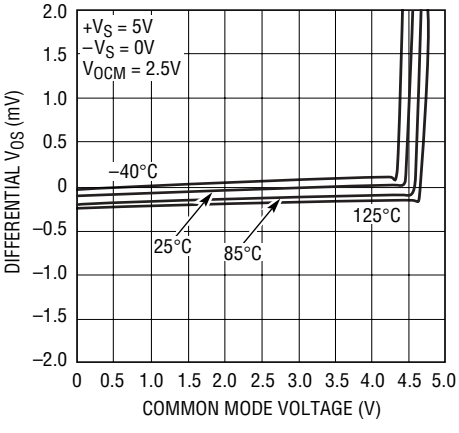

### $V_{OCM}$ Gain vs Frequency



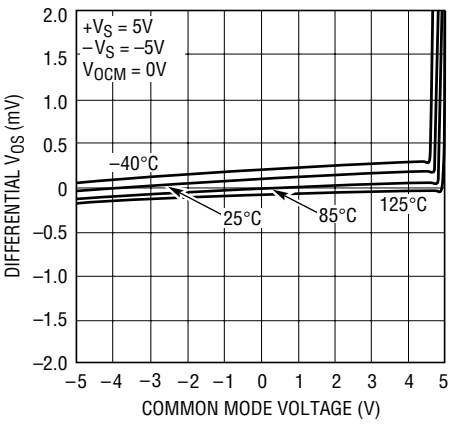

### Differential Input Offset Voltage vs Input Common Mode Voltage




### Differential Input Offset Voltage vs Input Common Mode Voltage

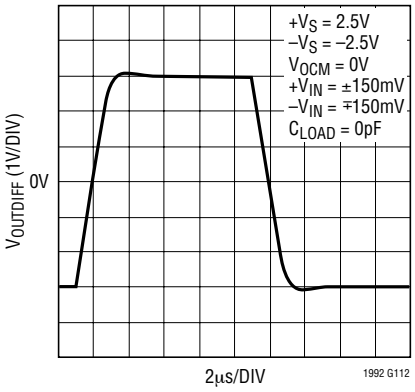



### Differential Input Offset Voltage vs Input Common Mode Voltage

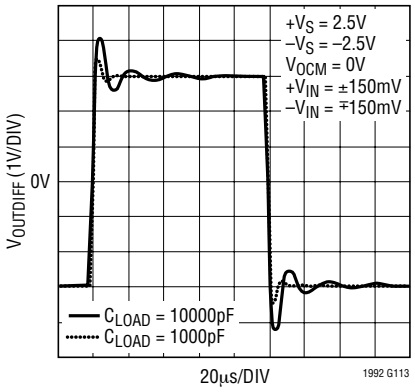


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-10 only.

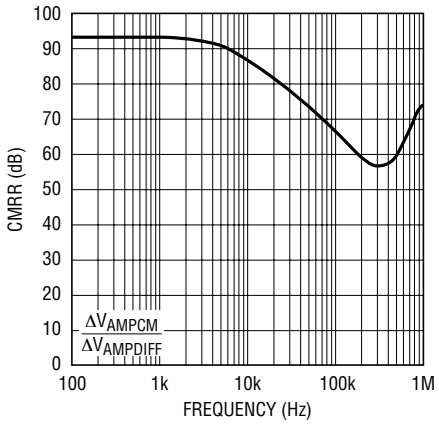
### Differential Input Large-Signal Step Response



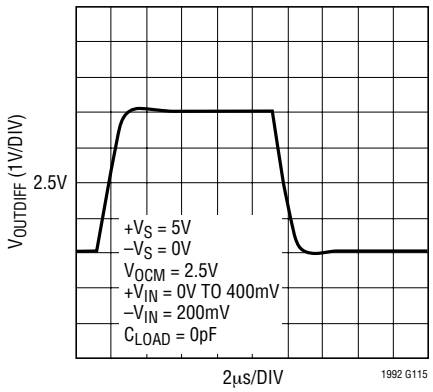

### Differential Input Large-Signal Step Response



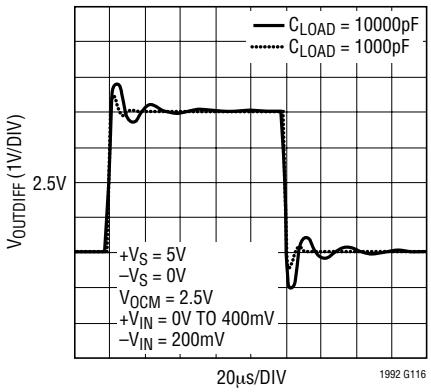

### Common Mode Rejection Ratio vs Frequency (Note 7)



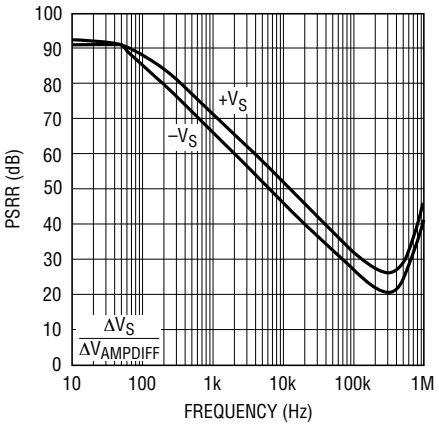

### Single-Ended Input Large-Signal Step Response



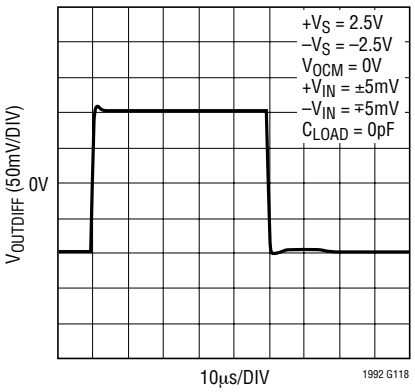

### Single-Ended Input Large-Signal Step Response



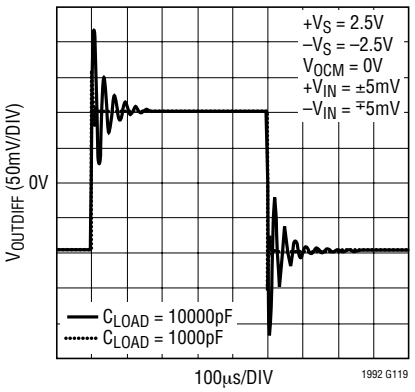

### Power Supply Rejection Ratio vs Frequency (Note 7)



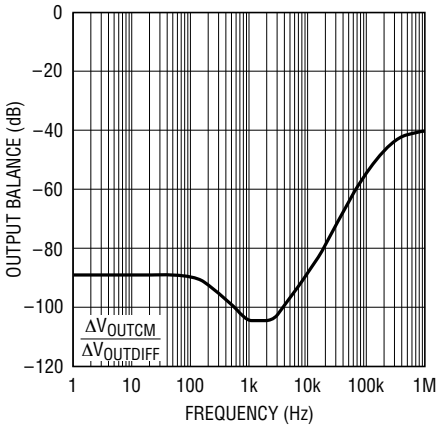

### Differential Input Small-Signal Step Response




### Differential Input Small-Signal Step Response

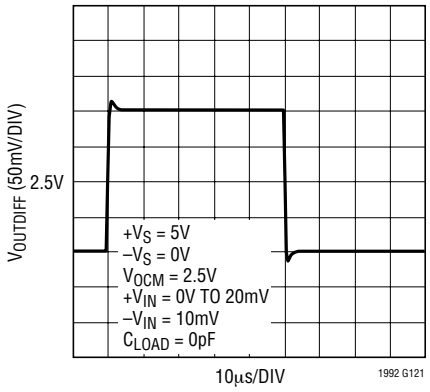



### Output Balance vs Frequency

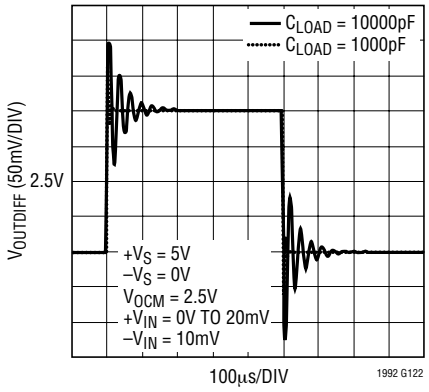


## TYPICAL PERFORMANCE CHARACTERISTICS Applicable to the LTC1992-10 only.

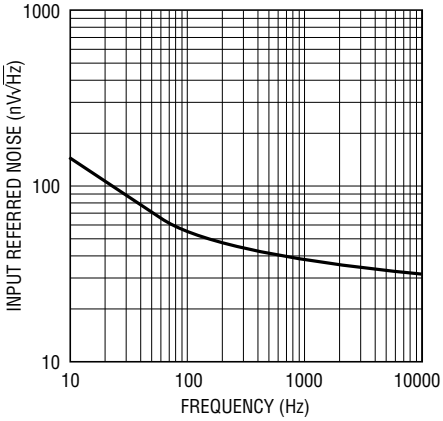
### Single-Ended Input Small-Signal Step Response



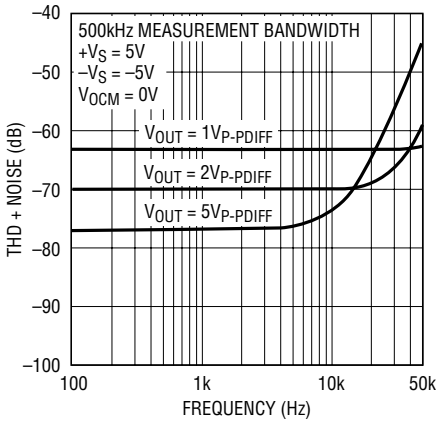

### Single-Ended Input Small-Signal Step Response



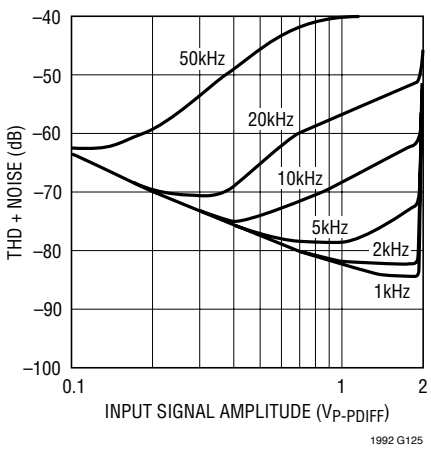

### Differential Noise Voltage Density vs Frequency




### THD + Noise vs Frequency




### THD + Noise vs Amplitude



## PIN FUNCTIONS

**–IN, +IN (Pins 1, 8):** Inverting and Noninverting Inputs of the Amplifier. For the LTC1992 part, these pins are connected directly to the amplifier's P-channel MOSFET input devices. The fixed gain LTC1992-X parts have precision, on-chip gain setting resistors. The input resistors are nominally 30k for the LTC1992-1, LTC1992-2 and LTC1992-5 parts. The input resistors are nominally 15k for the LTC1992-10 part.

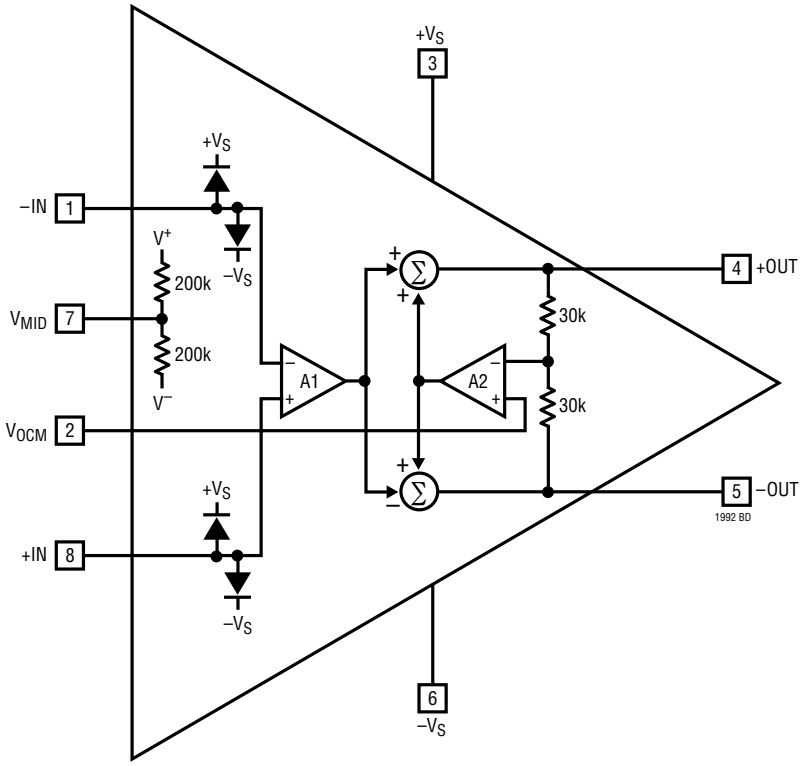
**$V_{OCM}$ (Pin 2):** Output Common Mode Voltage Set Pin. The voltage on this pin sets the output signal's common mode voltage level. The output common mode level is set independent of the input common mode level. This is a high impedance input and must be connected to a known and controlled voltage. It must never be left floating.

**$+V_S$, $-V_S$ (Pins 3, 6):** The $+V_S$ and $-V_S$ power supply pins should be bypassed with 0.1μF capacitors to an adequate analog ground or ground plane. The bypass capacitors should be located as closely as possible to the supply pins.

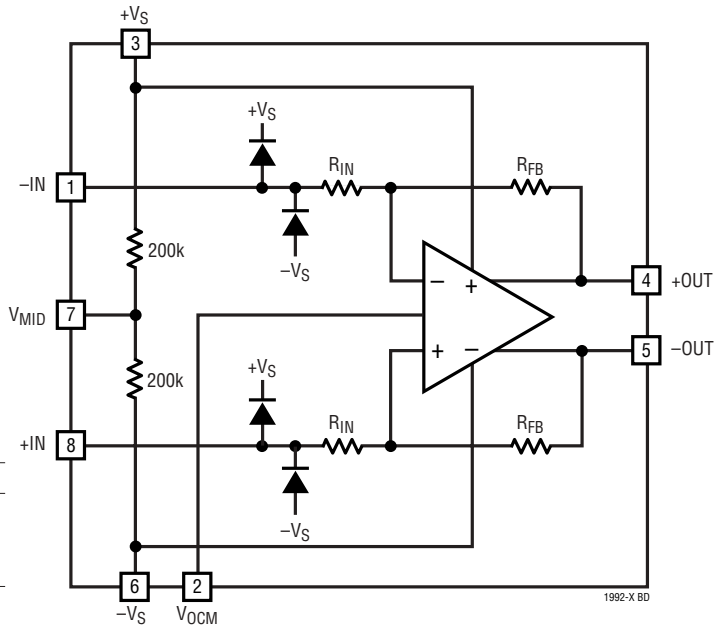
**+OUT, –OUT (Pins 4, 5):** The Positive and Negative Outputs of the Amplifier. These rail-to-rail outputs are designed to drive capacitive loads as high as 10,000pF.

**$V_{MID}$ (Pin 7):** Mid-Supply Reference. This pin is connected to an on-chip resistive voltage divider to provide a mid-supply reference. This provides a convenient way to set the output common mode level at half-supply. If used for this purpose, Pin 2 will be shorted to Pin 7, Pin 7 should be bypassed with a 0.1μF capacitor to ground. If this reference voltage is not used, leave the pin floating.

## BLOCK DIAGRAMS (1992)



## BLOCK DIAGRAMS (1992-X)




| PART | $R_{IN}$ | $R_{FB}$ |
|---|---|---|
| LTC1992-1 | 30k | 30k |
| LTC1992-2 | 30k | 60k |
| LTC1992-5 | 30k | 150k |
| LTC1992-10 | 15k | 150k |

## APPLICATIONS INFORMATION

### Theory of Operation

The LTC1992 family consists of five fully differential, low power amplifiers. The LTC1992 is an unconstrained fully differential amplifier. The LTC1992-1, LTC1992-2, LTC1992-5 and LTC1992-10 are fixed gain blocks (with gains of 1, 2, 5 and 10 respectively) featuring precision on-chip resistors for accurate and ultra stable gain.

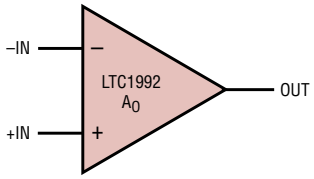
In many ways, a fully differential amplifier functions much like the familiar, ubiquitous op amp. However, there are several key areas where the two differ. Referring to Figure 1, an op amp has a differential input, a high open-loop gain and utilizes negative feedback (through resistors) to set the closed-loop gain and thus control the amplifier's gain with great precision. A fully differential amplifier has all of these features plus an additional input and a complementary output. The complementary output reacts to the input signal in the same manner as the other output, but in the opposite direction. Two outputs changing in an equal but opposite manner require a common reference point (i.e., opposite relative to what?). The additional input, the $V_{OCM}$ pin, sets this reference point. The voltage on the $V_{OCM}$ input directly sets the output signal's common mode voltage and allows the output signal's common mode voltage to be set completely independent of the input signal's common mode voltage. **Uncoupling the input and output common mode voltages makes signal level shifting easy.**

For a better understanding of the operation of a fully differential amplifier, refer to Figure 2. Here, the LTC1992 functional block diagram adds external resistors to realize a basic gain block. Note that the LTC1992 functional block diagram is not an *exact* replica of the LTC1992 circuitry. However, the Block Diagram is correct and is a very good tool for understanding the operation of fully differential amplifier circuits. Basic op amp fundamentals together with this block diagram provide all of the tools needed for understanding fully differential amplifier circuit applications.

The LTC1992 Block Diagram has two op amps, two summing blocks (pay close attention the **signs**) and four resistors. Two resistors, $R_{MID1}$ and $R_{MID2}$, connect directly to the $V_{MID}$ pin and simply provide a convenient midsupply reference. Its use is optional and it is not involved in the operation of the LTC1992's amplifier. The LTC1992 functions through the use of two servo networks

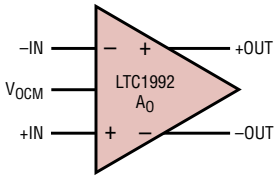
## APPLICATIONS INFORMATION

**Op Amp**



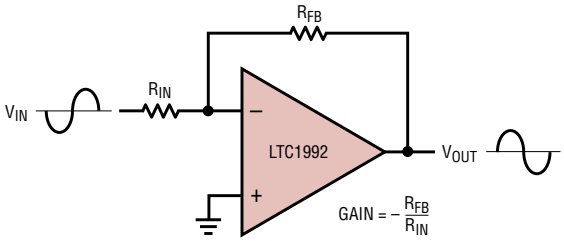

- DIFFERENTIAL INPUT
- HIGH OPEN-LOOP GAIN
- SINGLE-ENDED OUTPUT

**Fully Differential Amplifier**




- DIFFERENTIAL INPUT
- HIGH OPEN-LOOP GAIN
- DIFFERENTIAL OUTPUT
- $V_{OCM}$ INPUT SETS OUTPUT COMMON MODE LEVEL

**Op Amp with Negative Feedback**




**Fully Differential Amplifier with Negative Feedback**

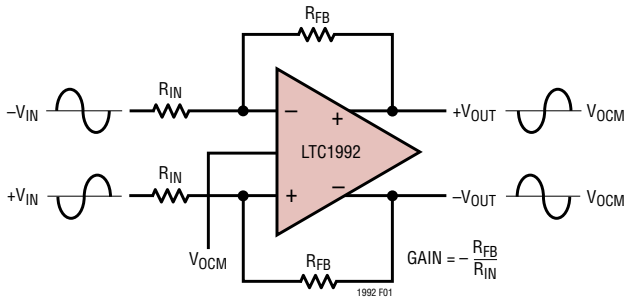



**Figure 1. Comparison of an Op Amp and a Fully Differential Amplifier**

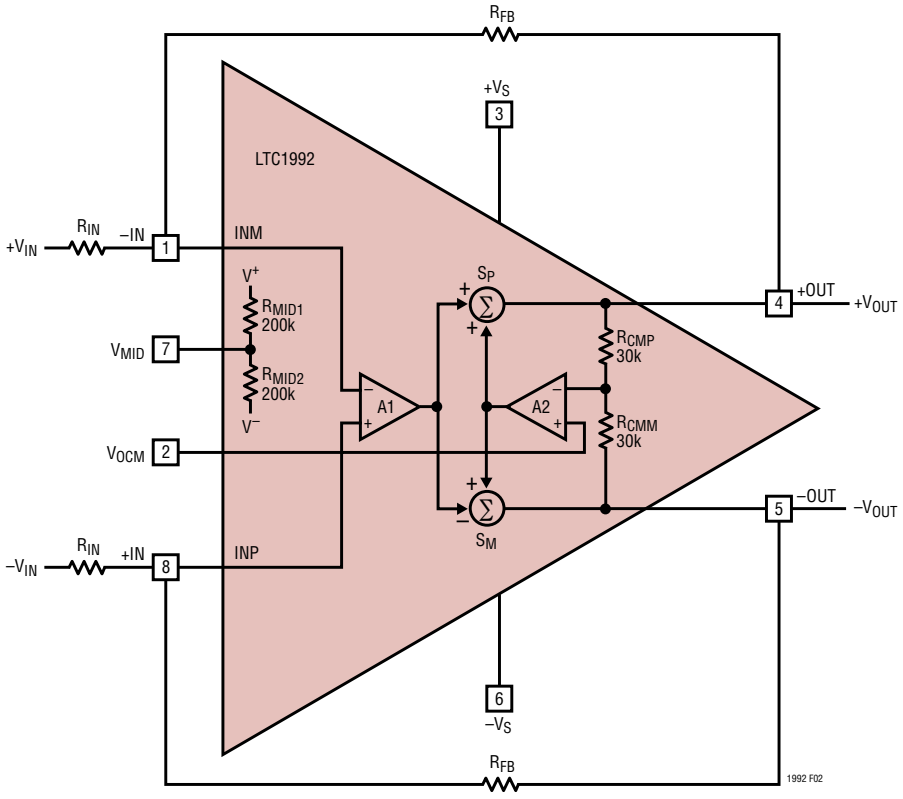



**Figure 2. LTC1992 Functional Block Diagram with External Gain Setting Resistors**

## APPLICATIONS INFORMATION

each employing negative feedback and using an op amp's differential input to create the servo's summing junction.

One servo controls the signal gain path. The differential input of op amp A1 creates the summing junction of this servo. Any voltage present at the input of A1 is amplified (by the op amp's large open-loop gain), sent to the summing blocks and then onto the outputs. Taking note of the signs on the summing blocks, op amp A1's output moves +OUT and –OUT in **opposite** directions. Applying a voltage step at the INM node increases the +OUT voltage while the –OUT voltage decreases. The $R_{FB}$ resistors connect the outputs to the appropriate inputs establishing negative feedback and closing the servo's loop. Any servo loop always attempts to drive its error voltage to zero. In this servo, the error voltage is the voltage between the INM and INP nodes, thus A1 will force the voltages on the INP and INM nodes to be equal (within the part's DC offset, open loop gain and bandwidth limits). The "virtual short" between the two inputs is conceptually the same as that for op amps and is critical to understanding fully differential amplifier applications.

The other servo controls the output common mode level. The differential input of op amp A2 creates the summing junction of this servo. Similar to the signal gain servo above, any voltage present at the input of A2 is amplified, sent to the summing blocks and then onto the outputs. However, in this case, both outputs move in the **same** direction. The resistors $R_{CMP}$ and $R_{CMM}$ connect the +OUT and –OUT outputs to A2's inverting input establishing negative feedback and closing the servo's loop. The midpoint of resistors $R_{CMP}$ and $R_{CMM}$ derives the output's common mode level (i.e., its average). This measure of the output's common mode level connects to A2's inverting input while A2's noninverting input connects directly to the $V_{OCM}$ pin. A2 forces the voltages on its inverting and noninverting inputs to be equal. In other words, it forces the output common mode voltage to be equal to the voltage on the $V_{OCM}$ input pin.

For any fully differential amplifier application to function properly both the signal gain servo and the common mode level servo must be satisfied. When analyzing an applications circuit, the INP node voltage must equal the INM node voltage **and** the output common mode voltage must equal the $V_{OCM}$ voltage. If either of these servos is taken out of the specified areas of operation (e.g., inputs taken beyond the common mode range specifications, outputs hitting the supply rails or input signals varying faster than the part can track), the circuit will not function properly.

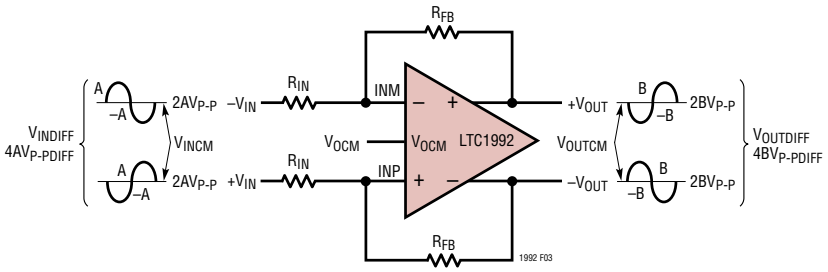
### Fully Differential Amplifier Signal Conventions

Fully differential amplifiers have a multitude of signals and signal ranges to consider. To maintain proper operation with conventional op amps, the op amp's inputs and its output must not hit the supply rails and the input signal's common mode level must also be within the part's specified limits. These considerations also apply to fully differential amplifiers, but here there is an additional output to consider and common mode level shifting complicates matters. Figure 3 provides a list of the many signals and specifications as well as the naming convention. The phrase "common mode" appears in many places and often leads to confusion. The fully differential amplifier's ability to uncouple input and output common mode levels yields great design flexibility, but also complicates matters some. For simplicity, the equations in Figure 3 also assume an ideal amplifier and perfect resistor matching. For a detailed analysis, consult the fully differential amplifier applications circuit analysis section..

### Basic Applications Circuits

Most fully differential amplifier applications circuits employ symmetrical feedback networks and are familiar territory for op amp users. Symmetrical feedback networks require that the $–V_{IN}/+V_{OUT}$ network is a mirror image duplicate of the $+V_{IN}/–V_{OUT}$ network. Each of these half circuits is basically just a standard inverting gain op amp circuit. Figure 4 shows three basic inverting gain op amp circuits and their corresponding fully differential amplifier cousins. The vast majority of fully differential amplifier circuits derive from old tried and true inverting op amp circuits. To create a fully differential amplifier circuit from an inverting op amp circuit, first simply transfer the op amp's $V_{IN}/V_{OUT}$ network to the fully differential amplifier's $–V_{IN}/+V_{OUT}$ nodes. Then, take a mirror image duplicate of the network and apply it to the fully differential amplifier's $+V_{IN}/–V_{OUT}$ nodes. Op amp users can comfortably transfer any inverting op amp circuit to a fully differential amplifier in this manner.

## APPLICATIONS INFORMATION




DIFFERENTIAL INPUT VOLTAGE $= V_{INDIFF} = +V_{IN} - -V_{IN}$

DIFFERENTIAL OUTPUT VOLTAGE $= V_{OUTDIFF} = +V_{OUT} - -V_{OUT}$

INPUT COMMON MODE VOLTAGE $= V_{INCM} = \frac{+V_{IN} + -V_{IN}}{2}$

OUTPUT COMMON MODE VOLTAGE $= V_{OUTCM} = \frac{+V_{OUT} + -V_{OUT}}{2}$

$$+V_{OUT} = \left(+V_{IN} - -V_{IN}\right) \bullet \frac{1}{2} \bullet \frac{R_{FB}}{R_{IN}} + V_{OCM} \quad ; V_{OSCM} = 0V$$

$$-V_{OUT} = \left(-V_{IN} - +V_{IN}\right) \bullet \frac{1}{2} \bullet \frac{R_{FB}}{R_{IN}} + V_{OCM} \quad ; V_{OSCM} = 0V$$

$$V_{OUTDIFF} = V_{INDIFF} \bullet \frac{R_{FB}}{R_{IN}}$$

$$V_{AMPDIFF} = V_{INP} - V_{INM}$$

$$V_{AMPCM} = \frac{V_{INP} + V_{INM}}{2}$$

$$V_{OUTCM} = V_{OCM}$$

$$CMRR = \frac{\Delta V_{AMPCM}}{\Delta V_{AMPDIFF}} ; +V_{IN} = -V_{IN}$$

$$\text{OUTPUT BALANCE} = \frac{\Delta V_{OUTCM}}{\Delta V_{OUTDIFF}}$$

$$e_{NOUT} = \left(\frac{R_{FB}}{R_{IN}} + 1\right) \bullet \sqrt{e_{NIN}^2 + r_N^2}$$

WHERE: $e_{NOUT}$ = OUTPUT REFERRED NOISE VOLTAGE DENSITY

$e_{NIN}$ = INPUT REFERRED NOISE VOLTAGE DENSITY

$$r_N \approx (0.13nV/\sqrt{Hz})\left(\frac{R_{IN} \bullet R_{FB}}{R_{IN} + R_{FB}}\right)$$

(RESISTIVE NOISE IS ALREADY INCLUDED IN THE SPECIFICATIONS FOR THE FIXED GAIN LTC1992-X PARTS)

$$V_{OSDIFFOUT} = V_{OSDIFFIN} \bullet \left(\frac{R_{FB}}{R_{IN}} + 1\right)$$

$$V_{OSCM} = V_{OUTCM} - V_{OCM}$$

**Figure 3. Fully Differential Amplifier Signal Conventions (Ideal Amplifier and Perfect Resistor Matching is Assumed)**

### Single-Ended to Differential Conversion

One of the most important applications of fully differential amplifiers is single-ended signaling to differential signaling conversion. Many systems have a single-ended signal that must connect to an ADC with a differential input. The ADC could be run in a single-ended manner, but performance usually degrades. Fortunately, all of basic applications circuits shown in Figure 4, as well as all of the fixed gain LTC1992-X parts, are equally suitable for both differential and single-ended input signals. For single-ended input signals, connect one of the inputs to a reference voltage (e.g., ground or midsupply) and connect the other to the signal path. There are no tradeoffs here as the part's performance is the same with single-ended or differential input signals. Which input is used for the signal path only affects the polarity of the differential output signal.

### Signal Level Shifting

Another important application of fully differential amplifier is signal level shifting. Single-ended to differential conversion accompanied by a signal level shift is very commonplace when driving ADCs. As noted in the theory of operation section, fully differential amplifiers have a common mode level servo that determines the output common mode level independent of the input common mode level. To set the output common mode level, simply apply the desired voltage to the $V_{OCM}$ input pin. The voltage range on the $V_{OCM}$ pin is from $(-V_S + 0.5V)$ to $(+V_S - 1.3V)$.

## APPLICATIONS INFORMATION

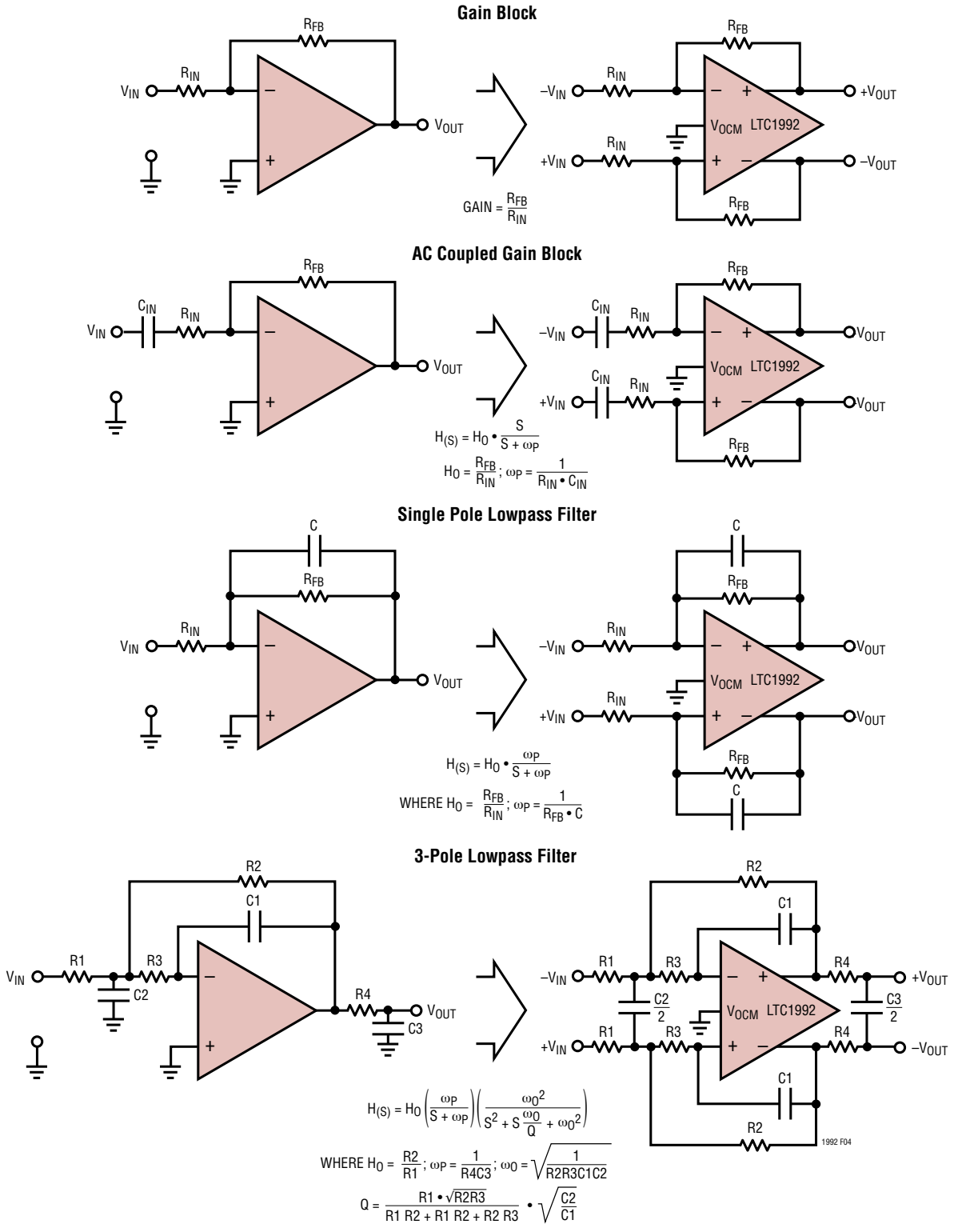



**Figure 4. Basic Fully Differential Amplifier Application Circuits (Note: Single-Ended to Differential Conversion is Easily Accomplished by Connecting One of the Input Nodes, $+V_{IN}$ or $-V_{IN}$, to a DC Reference Level (e.g., Ground))**

## APPLICATIONS INFORMATION

The $V_{OCM}$ input pin has a very high input impedance and is easily driven by even the weakest of sources. Many ADCs provide a voltage reference output that defines either its common mode level or its full-scale level. Apply the ADC's reference potential either directly to the $V_{OCM}$ pin or through a resistive voltage divider depending on the reference voltage's definition. When controlling the $V_{OCM}$ pin by a high impedance source, connect a bypass capacitor (1000pF to 0.1µF) from the $V_{OCM}$ pin to ground to lower the high frequency impedance and limit external noise coupling. Other applications will want the output biased at a midpoint of the power supplies for maximum output voltage swing. For these applications, the LTC1992 provides a midsupply potential at the $V_{MID}$ pin. The $V_{MID}$ pin connects to a simple resistive voltage divider with two 200k resistors connected between the supply pins. To use this feature, connect the $V_{MID}$ pin to the $V_{OCM}$ pin and bypass this node with a capacitor.

One undesired effect of utilizing the level shifting function is an increase in the differential output offset voltage due to gain setting resistor mismatch. The offset is approximately the amount of level shift ($V_{OUTCM} – V_{INCM}$) multiplied by the amount of resistor mismatch. For example, a 2V level shift with 0.1% resistors will give around 2mV of output offset (2 • 0.1% = 2mV). The exact amount of offset is dependent on the application's gain and the resistor mismatch. For a detail description, consult the Fully Differential Amplifier Applications Circuit Analysis section.

### CMRR and Output Balance

One common misconception of fully differential amplifiers is that the common mode level servo guarantees an infinite common mode rejection ratio (CMRR). This is not true. The common mode level servo does, however, force the two outputs to be truly complementary (i.e., exactly opposite or 180 degrees out of phase). Output balance is a measure of how complementary the two outputs are.

At low frequencies, CMRR is primarily determined by the matching of the gain setting resistors. Like any op amp, the LTC1992 does not have infinite CMRR, however resistor mismatching of only 0.018%, halves the circuit's CMRR. Standard 1% tolerance resistors yield a CMRR of about 40dB. For most applications, resistor matching dominates low frequency CMRR performance. The specifications for the fixed gain LTC1992-X parts include the on-chip resistor matching effects. Also, note that an *input common mode* signal appears as a *differential output* signal reduced by the CMRR. As with op amps, at higher frequencies the CMRR degrades. Refer to the Typical Performance plots for the details of the CMRR performance over frequency.

At low frequencies, the output balance specification is determined by the matching of the on-chip $R_{CMM}$ and $R_{CMP}$ resistors. At higher frequencies, the output balance degrades. Refer to the typical performance plots for the details of the output balance performance over frequency.

### Input Impedance

The input impedance for a fully differential amplifier application circuit is similar to that of a standard op amp inverting amplifier. One major difference is that the input impedance is different for differential input signals and single-ended signals. Referring to Figure 3, for differential input signals the input impedance is expressed by the following expression:

$$R_{INDIFF} = 2 \bullet R_{IN}$$

For single-ended signals, the input impedance is expressed by the following expression:

$$R_{INS-E} = \frac{R_{IN}}{1 - \frac{R_{FB}}{2 \bullet (R_{IN} + R_{FB})}}$$

The input impedance for single-ended signals is slightly higher than the $R_{IN}$ value since some of the input signal is fed back and appears as the amplifier's input common mode level. This small amount of positive feedback increases the input impedance.

### Driving Capacitive Loads

The LTC1992 family of parts is stable for all capacitive loads up to at least 10,000pF. While stability is guaranteed, the part's performance is not unaffected by capacitive loading. Large capacitive loads increase output step response ringing and settling time, decrease the bandwidth

## APPLICATIONS INFORMATION

and increase the frequency response peaking. Refer to the Typical Performance plots for small-signal step response, large-signal step response and gain over frequency to appraise the effects of capacitive loading. While the consequences are minor in most instances, consider these effects when designing application circuits with large capacitive loads.

### Input Signal Amplitude Considerations

For application circuits to operate correctly, the amplifier must be in its linear operating range. To be in the linear operating range, the input signal's common mode voltage must be within the part's specified limits and the rail-to-rail outputs must stay within the supply voltage rails. Additionally, the fixed gain LTC1992-X parts have input protection diodes that limit the input signal to be within the supply voltage rails. The unconstrained LTC1992 uses external resistors allowing the source signals to go beyond the supply voltage rails.

When taken outside of the linear operating range, the circuit does not perform as expected, however nothing extreme occurs. Outputs driven into the supply voltage rails are simply clipped. There is no phase reversal or oscillation. Once the outputs return to the linear operating range, there is a small recovery time, then normal operation proceeds. When the input common mode voltage is below the specified lower limit, on-chip protection diodes conduct and clamp the signal. Once the signal returns to the specified operating range, normal operation proceeds. If the input common mode voltage goes slightly above the specified upper limit (by no more than about 500mV), the amplifier's open-loop gain reduces and DC offset and closed-loop gain errors increase. Return the input back to the specified range and normal performance commences. If taken well above the upper limit, the amplifier's input stage is cut off. The gain servo is now open loop; however, the common mode servo is still functional. Output balance is maintained and the outputs go to opposite supply rails. However, which output goes to which supply rail is random. Once the input returns to the specified input common mode range, there is a small recovery time then normal operation proceeds.

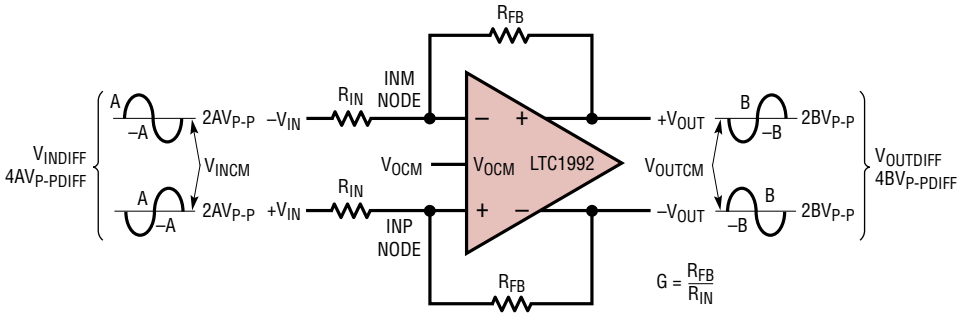
The LTC1992's input signal common mode range ($V_{INCMR}$) is from ($-V_S$ – 0.1V) to ($+V_S$ – 1.3V). This specification applies to the voltage at the **amplifier's** input, the INP and INM nodes of Figure 2. The specifications for the fixed gain LTC1992-X parts reflect a higher maximum limit as this specification is for the entire gain block and references the signal at the input resistors. Differential input signals and single-ended signals require a slightly different set of formulae. Differential signals separate very nicely into common mode and differential components while single ended signals do not. Refer to Figure 5 for the formulae for calculating the available signal range. Additionally, Table 1 lists some common configurations and their appropriate signal levels.

The LTC1992's outputs allow rail-to-rail signal swings. The output voltage on either output is a function of the input signal's amplitude, the gain configured and the output signal's common mode level set by the $V_{OCM}$ pin. For maximum signal swing, the $V_{OCM}$ pin is set at the midpoint of the supply voltages. For other applications, such as an ADC driver, the required level must fall within the $V_{OCM}$ range of ($-V_S$ + 0.5V) to ($+V_S$ – 1.3V). For single-ended input signals, it is not always obvious which output will clip first thus both outputs are calculated and the minimum value determines the signal limit. Refer to Figure 5 for the formulae and Table 1 for examples.

To ensure proper linear operation both the input common mode level and the output signal level must be within the specified limits. These same criteria are also present with standard op amps. However, with a fully differential amplifier, it is a bit more complex and old familiar op amp intuition often leads to the wrong result. This is especially true for single-ended to differential conversion with level shifting. The required calculations are a bit tedious, but are necessary to guarantee proper linear operation.

## APPLICATIONS INFORMATION

### Differential Input Signals




**INPUT COMMON MODE LIMITS**

A. CALCULATE $V_{INCM}$ MINIMUM AND MAXIMUM GIVEN $R_{IN}$, $R_{FB}$ AND $V_{OCM}$

$$V_{INCM(MAX)} = (+V_S - 1.3V) + \frac{1}{G}(+V_S - 1.3V - V_{OCM})$$

$$V_{INCM(MIN)} = (-V_S - 0.1V) + \frac{1}{G}(-V_S - 0.1V - V_{OCM})$$

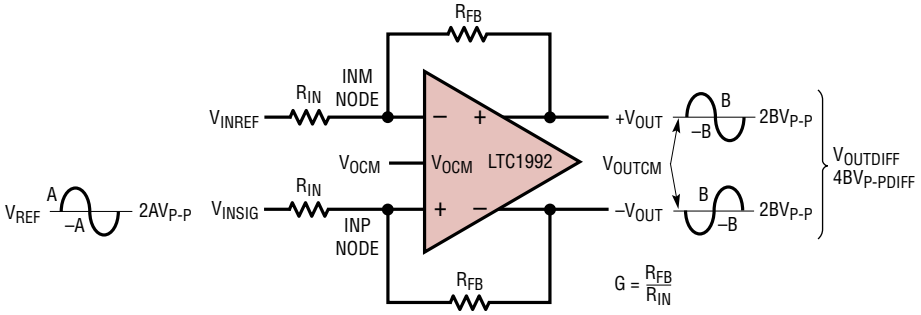
**OR** B. WITH A KNOWN $V_{INCM}$, $R_{IN}$, $R_{FB}$ AND $V_{OCM}$, CALCULATE COMMON MODE VOLTAGE AT INP AND INM NODES ($V_{INCM(AMP)}$) AND CHECK THAT IT IS WITHIN THE SPECIFIED LIMITS.

$$V_{INCM(AMP)} = \frac{V_{INP} + V_{INM}}{2} = \frac{G}{G+1}V_{INCM} + \frac{1}{G+1}V_{OCM}$$

**OUTPUT SIGNAL CLIPPING LIMIT**

$V_{INDIFF(MAX)}(V_{P-PDIFF})$ = THE LESSER VALUE OF $\frac{4}{G}(+V_S - V_{OCM})$ OR $\frac{4}{G}(V_{OCM} - -V_S)$

### Single End Input Signals




**INPUT COMMON MODE LIMITS** (NOTE: FOR THE FIXED GAIN LTC1992-X PARTS, $V_{INREF}$ AND $V_{INSIG}$ CANNOT EXCEED THE SUPPLIES)

$$V_{INSIG(MAX)} = 2\left[\left(+V_S - 1.3V - \frac{V_{INREF}}{2}\right) + \frac{1}{G}\left(+V_S - 1.3V - V_{OCM}\right)\right]$$

$$V_{INSIG(MIN)} = 2\left[\left(-V_S - 0.1V - \frac{V_{INREF}}{2}\right) + \frac{1}{G}\left(-V_S - 0.1V - V_{OCM}\right)\right]$$

**OR**

$$V_{INSIGP-P} = 2\left[\left((+V_S - -V_S) - 1.2V\right) + \frac{1}{G}\left((+V_S - -V_S) - 1.2V\right)\right]$$

**OUTPUT SIGNAL CLIPPING LIMIT**

$V_{INSIG(MAX)}$ = THE LESSER VALUE OF $V_{INREF} + \frac{2}{G}(+V_S - V_{OCM})$ OR $V_{INREF} + \frac{2}{G}(V_{OCM} - -V_S)$

$V_{INSIG(MIN)}$ = THE GREATER VALUE OF $V_{INREF} + \frac{2}{G}(-V_S - V_{OCM})$ OR $V_{INREF} + \frac{2}{G}(V_{OCM} - +V_S)$ 1992 F05

**Figure 5. Input Signal Limitations**

# APPLICATIONS INFORMATION

**Table 1. Input Signal Limitations for Some Common Applications**

**Differential Input Signal, $V_{OCM}$ at Midsupply**. ($V_{INCM}$ must be within the Min and Max table values and $V_{INDIFF}$ must be less than the table value)

| $+V_S$ (V) | $-V_S$ (V) | GAIN (V/V) | $V_{OCM}$ (V) | $V_{INCM(MAX)}$ (V) | $V_{INCM(MIN)}$ (V) | $V_{INDIFF(MAX)}$ ($V_{P-PDIFF}$) | $V_{OUTDIFF(MAX)}$ ($V_{P-PDIFF}$) |
|---|---|---|---|---|---|---|---|
| 2.7 | 0 | 1 | 1.35 | 1.450 | –1.550 | 5.40 | 5.40 |
| 2.7 | 0 | 2 | 1.35 | 1.425 | –0.825 | 2.70 | 5.40 |
| 2.7 | 0 | 5 | 1.35 | 1.410 | –0.390 | 1.08 | 5.40 |
| 2.7 | 0 | 10 | 1.35 | 1.405 | –0.245 | 0.54 | 5.40 |
| 5 | 0 | 1 | 2.5 | 4.900 | –2.700 | 10.00 | 10.00 |
| 5 | 0 | 2 | 2.5 | 4.300 | –1.400 | 5.00 | 10.00 |
| 5 | 0 | 5 | 2.5 | 3.940 | –0.620 | 2.00 | 10.00 |
| 5 | 0 | 10 | 2.5 | 3.820 | –0.360 | 1.00 | 10.00 |
| 5 | –5 | 1 | 0 | 7.400 | –10.200 | 20.00 | 20.00 |
| 5 | –5 | 2 | 0 | 5.550 | –7.650 | 10.00 | 20.00 |
| 5 | –5 | 5 | 0 | 4.440 | –6.120 | 4.00 | 20.00 |
| 5 | –5 | 10 | 0 | 4.070 | –5.610 | 2.00 | 20.00 |

**Differential Input Signal, $V_{OCM}$ at Typical ADC Levels**. ($V_{INCM}$ must be within the Min and Max table values and $V_{INDIFF}$ must be less than the table value)

| $+V_S$ (V) | $-V_S$ (V) | GAIN (V/V) | $V_{OCM}$ (V) | $V_{INCM(MAX)}$ (V) | $V_{INCM(MIN)}$ (V) | $V_{INDIFF(MAX)}$ ($V_{P-PDIFF}$) | $V_{OUTDIFF(MAX)}$ ($V_{P-PDIFF}$) |
|---|---|---|---|---|---|---|---|
| 2.7 | 0 | 1 | 1 | 1.800 | –1.200 | 4.00 | 4.00 |
| 2.7 | 0 | 2 | 1 | 1.600 | –0.650 | 2.00 | 4.00 |
| 2.7 | 0 | 5 | 1 | 1.480 | –0.320 | 0.80 | 4.00 |
| 2.7 | 0 | 10 | 1 | 1.440 | –0.210 | 0.40 | 4.00 |
| 5 | 0 | 1 | 2 | 5.400 | –2.200 | 8.00 | 8.00 |
| 5 | 0 | 2 | 2 | 4.550 | –1.150 | 4.00 | 8.00 |
| 5 | 0 | 5 | 2 | 4.040 | –0.520 | 1.60 | 8.00 |
| 5 | 0 | 10 | 2 | 3.870 | –0.310 | 0.80 | 8.00 |
| 5 | –5 | 1 | 2 | 5.400 | –12.200 | 12.00 | 12.00 |
| 5 | –5 | 2 | 2 | 4.550 | –8.650 | 6.00 | 12.00 |
| 5 | –5 | 5 | 2 | 4.040 | –6.520 | 2.40 | 12.00 |
| 5 | –5 | 10 | 2 | 3.870 | –5.810 | 1.20 | 12.00 |

## APPLICATIONS INFORMATION

**Table 1. Input Signal Limitations for Some Common Applications**

**Midsupply Referenced Single-Ended Input Signal, $V_{OCM}$ at Midsupply**. (The $V_{INSIG}$ Min and Max values listed account for both the input common mode limits and the output clipping)

| $+V_S$ (V) | $-V_S$ (V) | GAIN (V/V) | $V_{OCM}$ (V) | $V_{INREF}$ (V) | $V_{INSIG(MAX)}$ (V) | $V_{INSIG(MIN)}$ (V) | $V_{INSIGP-P(MAX)}$ ($V_{P-P}$ AROUND $V_{INREF}$) | $V_{OUTDIFF(MAX)}$ ($V_{P-PDIFF}$) |
|---|---|---|---|---|---|---|---|---|
| 2.7 | 0 | 1 | 1.35 | 1.35 | 1.550 | –1.350 | 0.40 | 0.40 |
| 2.7 | 0 | 2 | 1.35 | 1.35 | 1.500 | 0.000 | 0.30 | 0.60 |
| 2.7 | 0 | 5 | 1.35 | 1.35 | 1.470 | 0.810 | 0.24 | 1.20 |
| 2.7 | 0 | 10 | 1.35 | 1.35 | 1.460 | 1.080 | 0.22 | 2.20 |
| 5 | 0 | 1 | 2.5 | 2.5 | 7.300 | –2.500 | 9.60 | 9.60 |
| 5 | 0 | 2 | 2.5 | 2.5 | 5.000 | 0.000 | 5.00 | 10.00 |
| 5 | 0 | 5 | 2.5 | 2.5 | 3.500 | 1.500 | 2.00 | 10.00 |
| 5 | 0 | 10 | 2.5 | 2.5 | 3.000 | 2.000 | 1.00 | 10.00 |
| 5 | –5 | 1 | 0 | 0 | 10.000 | –10.000 | 20.00 | 20.00 |
| 5 | –5 | 2 | 0 | 0 | 5.000 | –5.000 | 10.00 | 20.00 |
| 5 | –5 | 5 | 0 | 0 | 2.000 | –2.000 | 4.00 | 20.00 |
| 5 | –5 | 10 | 0 | 0 | 1.000 | –1.000 | 2.00 | 20.00 |

**Midsupply Referenced Single-Ended Input Signal, $V_{OCM}$ at Typical ADC Levels**. (The $V_{INSIG}$ Min and Max values listed account for both the input common mode limits and the output clipping)

| $+V_S$ (V) | $-V_S$ (V) | GAIN (V/V) | $V_{OCM}$ (V) | $V_{INREF}$ (V) | $V_{INSIG(MAX)}$ (V) | $V_{INSIG(MIN)}$ (V) | $V_{INSIGP-P(MAX)}$ ($V_{P-P}$ AROUND $V_{INREF}$) | $V_{OUTDIFF(MAX)}$ ($V_{P-PDIFF}$) |
|---|---|---|---|---|---|---|---|---|
| 2.7 | 0 | 1 | 1 | 1.35 | 2.250 | –0.650 | 1.80 | 1.80 |
| 2.7 | 0 | 2 | 1 | 1.35 | 1.850 | 0.350 | 1.00 | 2.00 |
| 2.7 | 0 | 5 | 1 | 1.35 | 1.610 | 0.950 | 0.52 | 2.60 |
| 2.7 | 0 | 10 | 1 | 1.35 | 1.530 | 1.150 | 0.36 | 3.60 |
| 5 | 0 | 1 | 2 | 2.5 | 6.500 | –1.500 | 8.00 | 8.00 |
| 5 | 0 | 2 | 2 | 2.5 | 4.500 | 0.500 | 4.00 | 8.00 |
| 5 | 0 | 5 | 2 | 2.5 | 3.300 | 1.700 | 1.60 | 8.00 |
| 5 | 0 | 10 | 2 | 2.5 | 2.900 | 2.100 | 0.80 | 8.00 |
| 5 | –5 | 1 | 2 | 0 | 6.000 | –6.000 | 12.00 | 12.00 |
| 5 | –5 | 2 | 2 | 0 | 3.000 | –3.000 | 6.00 | 12.00 |
| 5 | –5 | 5 | 2 | 0 | 1.200 | –1.200 | 2.40 | 12.00 |
| 5 | –5 | 10 | 2 | 0 | 0.600 | –0.600 | 1.20 | 12.00 |

## APPLICATIONS INFORMATION

**Table 1. Input Signal Limitations for Some Common Applications**

**Single Supply Ground Referenced Single-Ended Input Signal, $V_{OCM}$ at Midsupply**. (The $V_{INSIG}$ Min and Max values listed account for both the input common mode limits and the output clipping)

| $+V_S$ (V) | $-V_S$ (V) | GAIN (V/V) | $V_{OCM}$ (V) | $V_{INREF}$ (V) | $V_{INSIG(MAX)}$ (V) | $V_{INSIG(MIN)}$ (V) | $V_{INSIGP-P(MAX)}$ ($V_{P-P}$ AROUND $V_{INREF}$) | $V_{OUTDIFF(MAX)}$ ($V_{P-PDIFF}$) |
|---|---|---|---|---|---|---|---|---|
| 2.7 | 0 | 1 | 1.35 | 0 | 2.700 | –2.700 | 5.40 | 5.40 |
| 2.7 | 0 | 2 | 1.35 | 0 | 1.350 | –1.350 | 2.70 | 5.40 |
| 2.7 | 0 | 5 | 1.35 | 0 | 0.540 | –0.540 | 1.08 | 5.40 |
| 2.7 | 0 | 10 | 1.35 | 0 | 0.270 | –0.270 | 0.54 | 5.40 |
| 5 | 0 | 1 | 2.5 | 0 | 5.000 | –5.000 | 10.00 | 10.00 |
| 5 | 0 | 2 | 2.5 | 0 | 2.500 | –2.500 | 5.00 | 10.00 |
| 5 | 0 | 5 | 2.5 | 0 | 1.000 | –1.000 | 2.00 | 10.00 |
| 5 | 0 | 10 | 2.5 | 0 | 0.500 | –0.500 | 1.00 | 10.00 |

**Single Supply Ground Referenced Single-Ended Input Signal, $V_{OCM}$ at Typical ADC Reference Levels**. (The $V_{INSIG}$ Min and Max values listed account for both the input common mode limits and the output clipping)

| $+V_S$ (V) | $-V_S$ (V) | GAIN (V/V) | $V_{OCM}$ (V) | $V_{INREF}$ (V) | $V_{INSIG(MAX)}$ (V) | $V_{INSIG(MIN)}$ (V) | $V_{INSIGP-P(MAX)}$ ($V_{P-P}$ AROUND $V_{INREF}$) | $V_{OUTDIFF(MAX)}$ ($V_{P-PDIFF}$) |
|---|---|---|---|---|---|---|---|---|
| 2.7 | 0 | 1 | 1 | 0 | 2.000 | –2.000 | 4.00 | 4.00 |
| 2.7 | 0 | 2 | 1 | 0 | 1.000 | –1.000 | 2.00 | 4.00 |
| 2.7 | 0 | 5 | 1 | 0 | 0.400 | –0.400 | 0.80 | 4.00 |
| 2.7 | 0 | 10 | 1 | 0 | 0.200 | –0.200 | 0.40 | 4.00 |
| 5 | 0 | 1 | 2 | 0 | 4.000 | –4.000 | 8.00 | 8.00 |
| 5 | 0 | 2 | 2 | 0 | 2.000 | –2.000 | 4.00 | 8.00 |
| 5 | 0 | 5 | 2 | 0 | 0.800 | –0.800 | 1.60 | 8.00 |
| 5 | 0 | 10 | 2 | 0 | 0.400 | –0.400 | 0.80 | 8.00 |

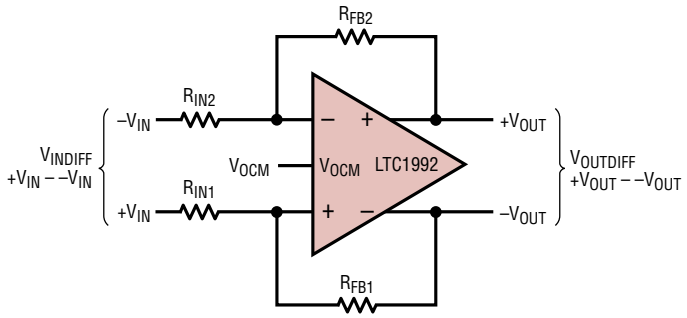
### Fully Differential Amplifier Applications Circuit Analysis

All of the previous applications circuit discussions have assumed perfectly matched symmetrical feedback networks. To consider the effects of mismatched or asymmetrical feedback networks, the equations get a bit messier.

Figure 6 lists the basic gain equation for the differential output voltage in terms of $+V_{IN}$, $-V_{IN}$, $V_{OSDIFF}$, $V_{OUTCM}$ and the feedback factors $\beta1$ and $\beta2$. The feedback factors are simply the portion of the output that is fed back to the input summing junction by the $R_{FB}$-$R_{IN}$ resistive voltage divider. $\beta1$ and $\beta2$ have the range of zero to one. The $V_{OUTCM}$ term also includes its offset voltage, $V_{OSCM}$, and its gain mismatch term, $K_{CM}$. The $K_{CM}$ term is determined by the matching of the on-chip $R_{CMP}$ and $R_{CMM}$ resistors in the common mode level servo (see Figure 2).

While mathematically correct, the basic signal equation does not immediately yield any intuitive feel for fully differential amplifier application operation. However, by nulling out specific terms, some basic observations and sensitivities come forth. Setting $\beta1$ equal to $\beta2$, $V_{OSDIFF}$ to zero and $V_{OUTCM}$ to $V_{OCM}$ gives the old gain equation from Figure 3. The ground referenced, single-ended input signal equation yields the interesting result that the driven side feedback factor ($\beta1$) has a very different sensitivity than the grounded side ($\beta2$). The CMRR is twice the feedback factor difference divided by the feedback factor sum. The differential output offset voltage has two terms. The first term is determined by the input offset term, $V_{OSDIFF}$, and the application's gain. Note that this term equates to the formula in Figure 3 when $\beta1$ equals $\beta2$. The amount of signal level shifting and the feedback factor mismatch determines the second term. This term

## APPLICATIONS INFORMATION




$$V_{OUTDIFF} = \frac{2[+V_{IN} \bullet (1-\beta1) - (-V_{IN}) \bullet (1-\beta2)] + 2V_{OSDIFF} + 2V_{OUTCM}(\beta1-\beta2)}{\beta1+\beta2}$$

WHERE:

$$\beta1 = \frac{R_{IN1}}{R_{IN1}+R_{FB1}};\ \beta2 = \frac{R_{IN2}}{R_{IN2}+R_{FB2}}$$

; $V_{OSDIFF}$ = AMPLIFIER INPUT REFERRED OFFSET VOLTAGE

$V_{OUTCM} = K_{CM} \bullet V_{OCM} + V_{OSCM}$

$0.999 < K_{CM} < 1.001$

• FOR GROUND REFERENCED, SINGLE-ENDED INPUT SIGNAL, LET $+V_{IN} = V_{INSIG}$ AND $-V_{IN} = 0V$

$$V_{OUTDIFF} = \frac{2 \bullet V_{INSIG} \bullet (1-\beta1) + 2V_{OSDIFF} + 2V_{OUTCM}(\beta1-\beta2)}{\beta1+\beta2}$$

• COMMON MODE REJECTION: SET $+V_{IN} = -V_{IN} = V_{INCM}$, $V_{OSDIFF} = 0V$, $V_{OUTCM} = 0V$

$$CMRR = \frac{\Delta V_{INCM}}{\Delta V_{OUTDIFF}} = 2\frac{\beta1+\beta2}{\beta2-\beta1};\ \text{OUTPUT REFERRED}$$

• OUTPUT DC OFFSET VOLTAGE: SET $+V_{IN} = -V_{IN} = V_{INCM}$

$$V_{OSDIFFOUT} = V_{OSDIFF}\frac{2}{\beta1+\beta2} + (V_{OUTCM} - V_{INCM})\,2\frac{\beta2-\beta1}{\beta1+\beta2}$$

**Figure 6. Basic Equations for Mismatched or Asymmetrical Feedback Applications Circuits**

quantifies the undesired effect of signal level shifting discussed earlier in the Signal Level Shifting section.

### Asymmetrical Feedback Application Circuits

The basic signal equation in Figure 6 also gives insight to another piece of intuition. The feedback factors may be deliberately set to different values. One interesting class of these application circuits sets one or both of the feedback factors to the extreme values of either zero or one. Figure 7 shows three such circuits.

At first these application circuits may look to be unstable or open loop. It is the common mode feedback loop that enables these circuits to function. While they are useful circuits, they have some shortcomings that must be considered. First, do to the severe feedback factor asymmetry, the $V_{OCM}$ level influences the **differential** output voltage with about the same strength as the input signal. With this much gain in the $V_{OCM}$ path, differential output offset and noise increase. The large $V_{OCM}$ to $V_{OUTDIFF}$ gain also necessitates that these circuits are largely limited to dual, split supply voltage applications with a ground referenced input signal and a grounded $V_{OCM}$ pin.

The top application circuit in Figure 7 yields a high input impedance, precision gain of 2 block without any external resistors. The on-chip common mode feedback servo resistors determine the gain precision (better than 0.1 percent). By using the $-V_{OUT}$ output alone, this circuit is also useful to get a precision, single-ended output, high input impedance inverter. To intuitively understand this circuit, consider it as a standard op amp voltage follower (delivered through the signal gain servo) with a complementary output (delivered through the common mode level servo). As usual, the amplifier's input common mode range must not be exceeded. As with a standard op amp voltage follower, the common mode signal seen at the amplifier's input is the input signal itself. This condition limits the input signal swing, as well as the output signal swing, to be the input signal common mode range specification.

The middle circuit is largely the same as the first except that the noninverting amplifier path has gain. Note that

## APPLICATIONS INFORMATION

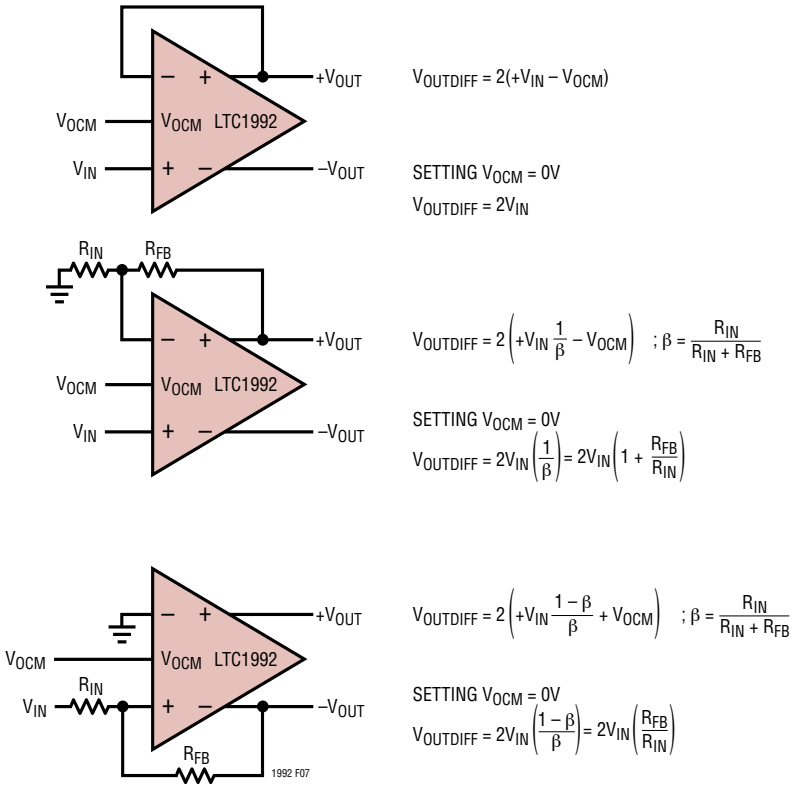


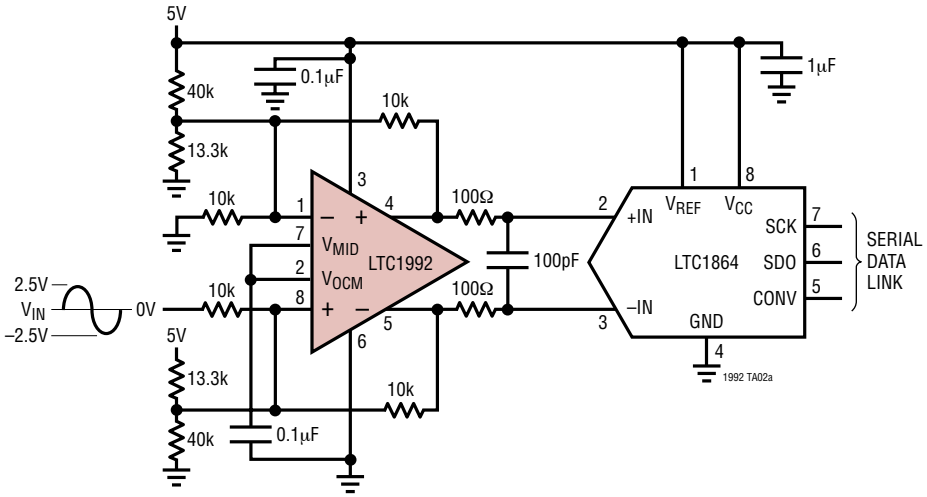

**Figure 7. Asymmetrical Feedback Application Circuits (Most Suitable in Applications with Dual, Split Supplies (e.g., ±5V), Ground Referenced Single-Ended Input Signals and $V_{OCM}$ Connected to Ground)**

once the $V_{OCM}$ voltage is set to zero, the gain formula is the same as a standard noninverting op amp circuit multiplied by two to account for the complementary output. Taking $R_{FB}$ to zero (i.e., taking β to one) gives the same formula as the top circuit. As in the top circuit, this circuit is also useful as a single-ended output, high input impedance inverting gain block (this time with gain). The input common mode considerations are similar to the top circuit's, but are not nearly as constrained since there is now gain in the noninverting amplifier path. This circuit, with $V_{OCM}$ at ground, also permits a rail-to-rail output swing in most applications.

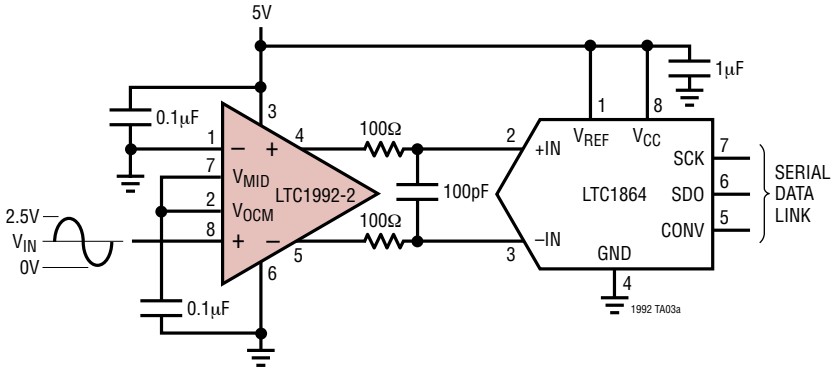
The bottom circuit is another circuit that utilizes a standard op amp configuration with a complementary output. In this case, the standard op amp circuit has an inverting configuration. With $V_{OCM}$ at zero volts, the gain formula is the same as a standard inverting op amp circuit multiplied by two to account for the complementary output. This circuit does not have any common mode level constraints as the inverting input voltage sets the input common mode level. This circuit also delivers rail-to-rail output voltage swing without any concerns.

## TYPICAL APPLICATIONS

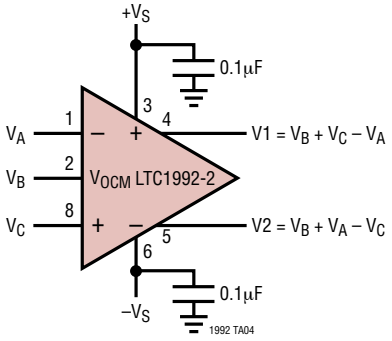
**Interfacing a Bipolar, Ground Referenced, Single-Ended Signal to a Unipolar Single Supply, Differential Input ADC ($V_{IN}$ = 0V Gives a Digital Mid-Scale Code)**




**Compact, Unipolar Serial Data Conversion**

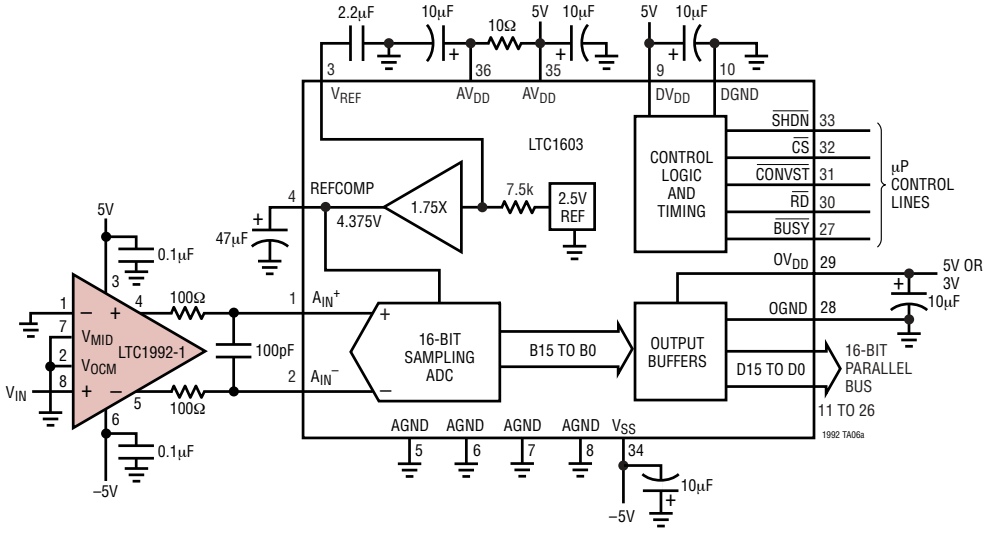



**Zero Components, Single-Ended Adder/Subtracter**

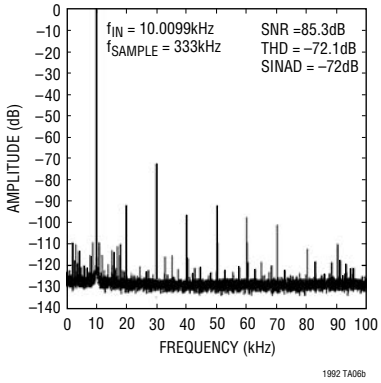


# TYPICAL APPLICATIONS

### Single-Ended to Differential Conversion Driving an ADC

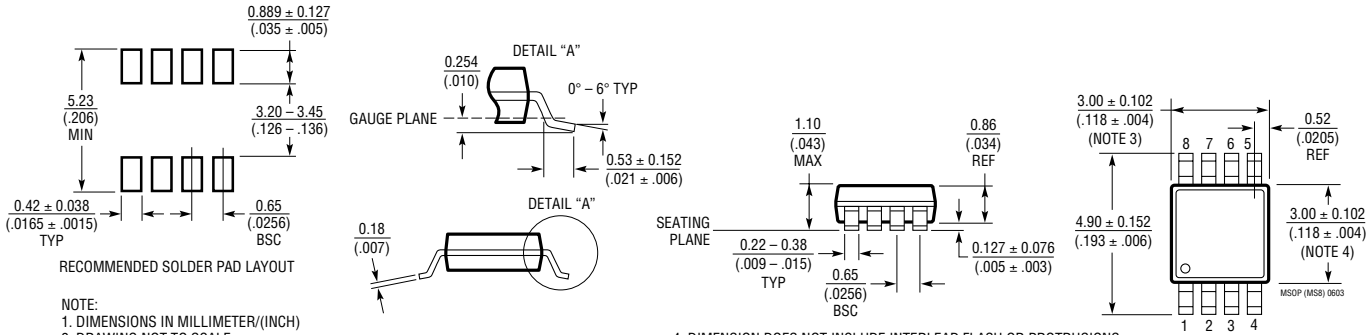



### FFT of the Output Data




# PACKAGE DESCRIPTION

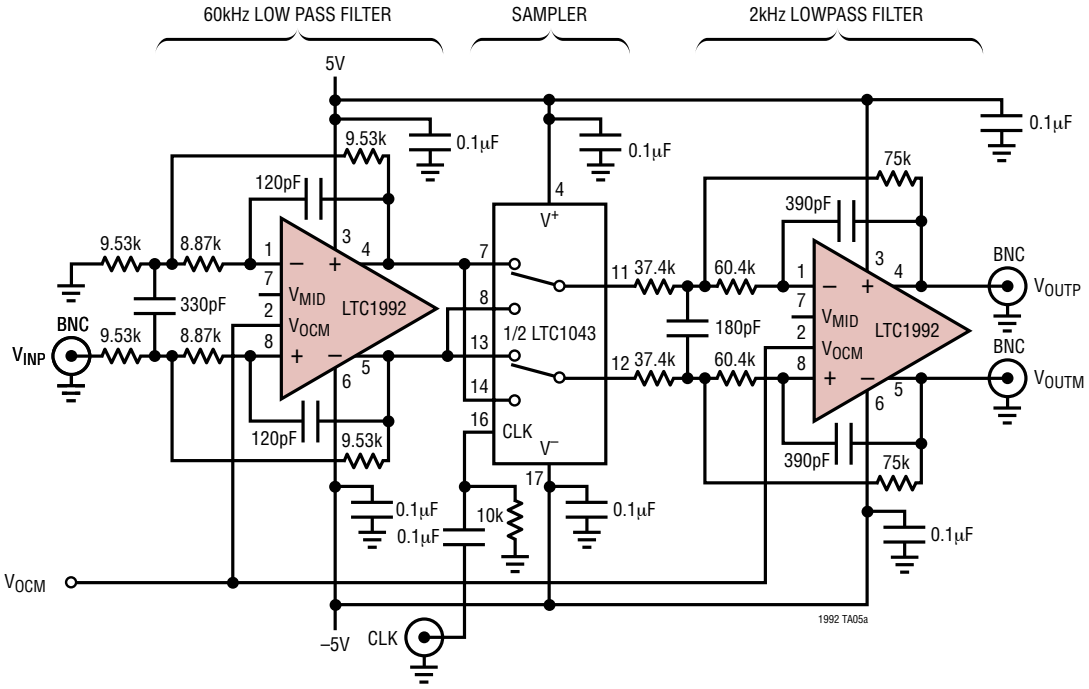
**MS8 Package**
**8-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1660)

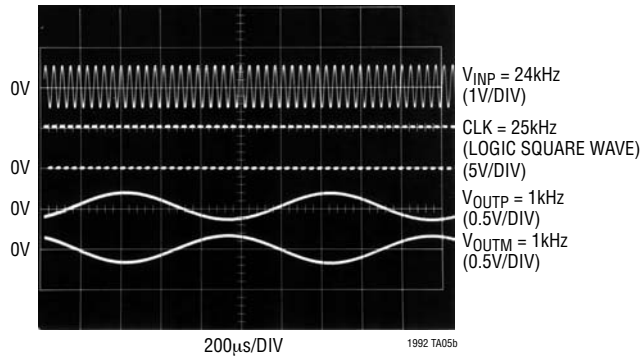



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## TYPICAL APPLICATION

**Balanced Frequency Converter (Suitable for Frequencies up to 50kHz)**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT1167 | Precision Instrumentation Amplifier | Single Resistor Sets the Gain |
| LT1990 | High Voltage, Gain Selectable Difference Amplifier | ±250V Common Mode, Micropower, Selectable Gain = 1, 10 |
| LT1991 | Precision Gain Selectable Difference Amplifier | Micropower, Pin Selectable Gain = –13 to 14 |
| LT1995 | High Speed Gain Selectable Difference Amplifier | 30MHz, 1000V/µs, Pin Selectable Gain = –7 to 8 |
| LT6600-X | Differential In/Out Amplifier Lowpass Filter | Very Low Noise, Standard Differential Amplifier Pinout |

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LT/TP 0105 1K • PRINTED IN USA

# Dual N-Channel 20 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A)[a] | $Q_g$ (Typ.) |
| 20 | 0.168 at $V_{GS}$ = 4.5 V | 1.3[a] | 1.6 nC |
| | 0.200 at $V_{GS}$ = 2.5 V | 1.3[a] | |
| | 0.250 at $V_{GS}$ = 1.8 V | 1.3[a] | |

## FEATURES

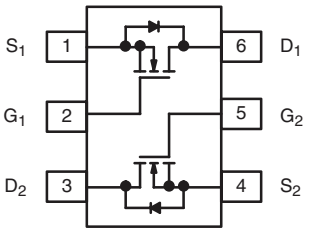
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

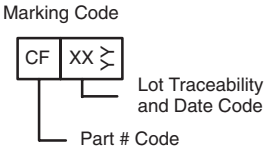
## APPLICATIONS

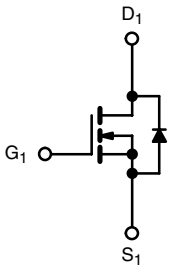
- Load Switch for Portable Applications

**SOT-363**
SC-70 (6-LEADS)

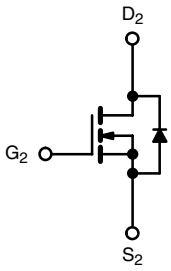



Top View




N-Channel MOSFET




N-Channel MOSFET

**Ordering Information:** Si1988DH-T1-E3 (Lead (Pb)-free)
Si1988DH-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 8 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 1.3[a] | A |
| | $T_C$ = 70 °C | | 1.3[a] | |
| | $T_A$ = 25 °C | | 1.3[a, b, c] | |
| | $T_A$ = 70 °C | | 1.3[a, b, c] | |
| Pulsed Drain Current | | $I_{DM}$ | 4 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | 1.0 | |
| | $T_A$ = 25 °C | | 0.61[b, c] | |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 1.25 | W |
| | $T_C$ = 70 °C | | 0.8 | |
| | $T_A$ = 25 °C | | 0.74[b, c] | |
| | $T_A$ = 70 °C | | 0.47[b, c] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | °C |
| Soldering Recommendations (Peak Temperature)[d, e] | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typical** | **Maximum** | **Unit** |
| Maximum Junction-to-Ambient[b, f] | t ≤ 5 s | $R_{thJA}$ | 130 | 170 | °C/W |
| Maximum Junction-to-Foot (Drain) | Steady State | $R_{thJF}$ | 80 | 100 | |

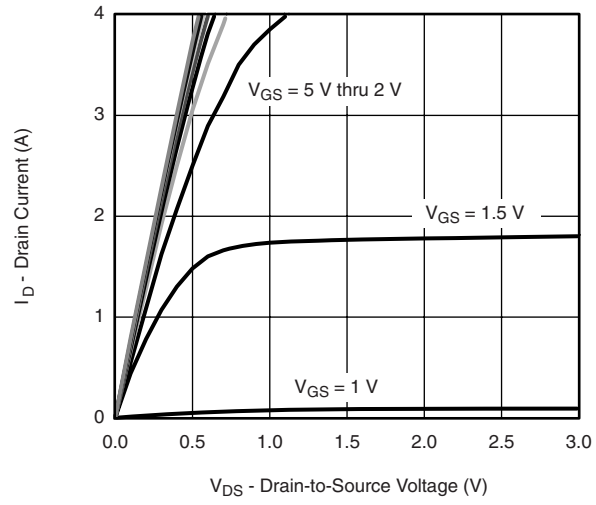
Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. Maximum under steady state conditions is 220 °C/W.

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 20 | | | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 µA | | 19.7 | | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | - 2.4 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 0.4 | | 1 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 8 V | | | ± 100 | ns |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | | | 10 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS} \leq$ 5 V, $V_{GS}$ = 4.5 V | 4 | | | A |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 1.4 A | | 0.139 | 0.168 | Ω |
| | | $V_{GS}$ = 2.5 V, $I_D$ = 1.3 A | | 0.165 | 0.200 | |
| | | $V_{GS}$ = 1.8 V, $I_D$ = 0.4 A | | 0.205 | 0.250 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 4 V, $I_D$ = 1.4 A | | 4 | | S |
| **Dynamic[b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | | 110 | | pF |
| Output Capacitance | $C_{oss}$ | | | 25 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 11 | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 8 V, $I_D$ = 1.6 A | | 2.7 | 4.1 | nC |
| | | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 1.6 A | | 1.6 | 2.4 | |
| Gate-Source Charge | $Q_{gs}$ | | | 0.3 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 0.25 | | |
| Gate Resistance | $R_g$ | f = 1 MHz | | 4 | | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 7.7 Ω<br>$I_D \cong$ 1.3 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | | 8 | 12 | ns |
| Rise Time | $t_r$ | | | 20 | 30 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 15 | 25 | |
| Fall Time | $t_f$ | | | 10 | 15 | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 7.7 Ω<br>$I_D \cong$ 1.3 A, $V_{GEN}$ = 8 V, $R_g$ = 1 Ω | | 5 | 10 | |
| Rise Time | tr | | | 11 | 20 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 10 | 15 | |
| Fall Time | tr | | | 6 | 10 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | | | 1 | A |
| Pulse Diode Forward Current | $I_{SM}$ | | | | 4 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 1.3 A, $V_{GS}$ = 0 V | | 0.8 | 1.2 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 1.3 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | | 20 | 40 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | 20 | 40 | nC |
| Reverse Recovery Fall Time | $t_a$ | | | 16 | | ns |
| Reverse Recovery Rise Time | $t_b$ | | | 4 | | |

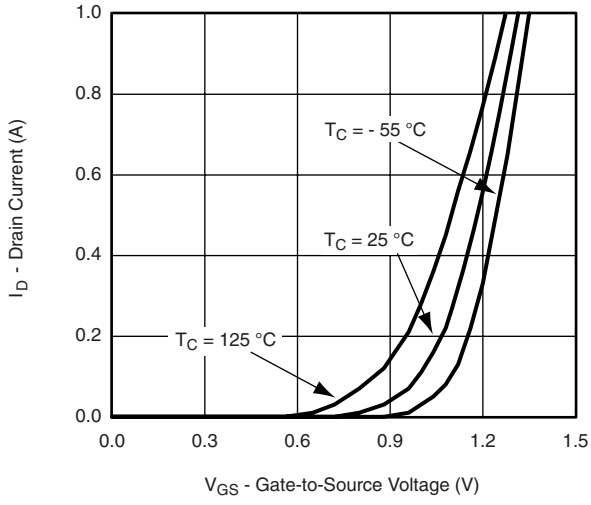
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

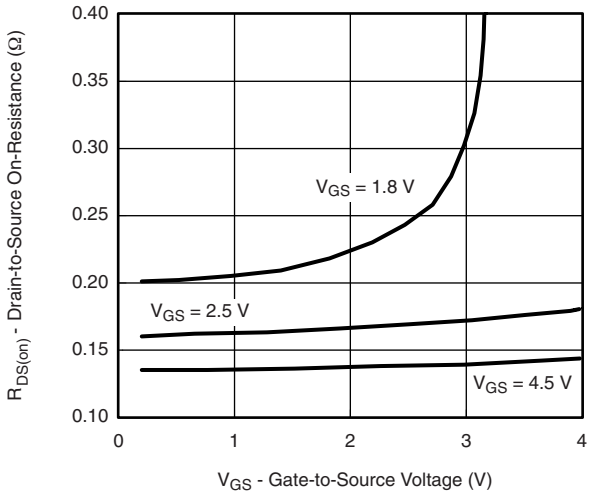
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



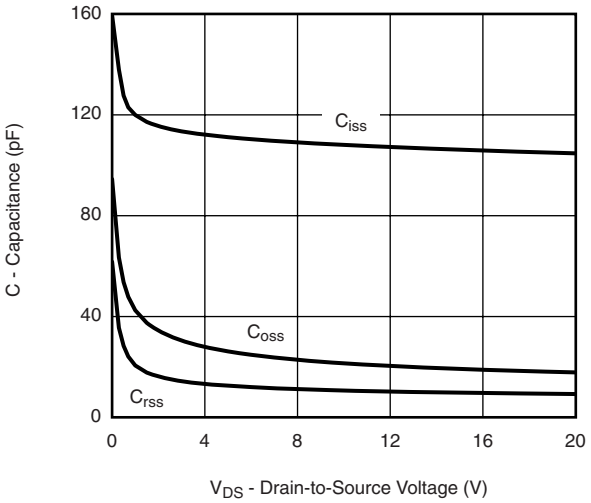

**Output Characteristics**



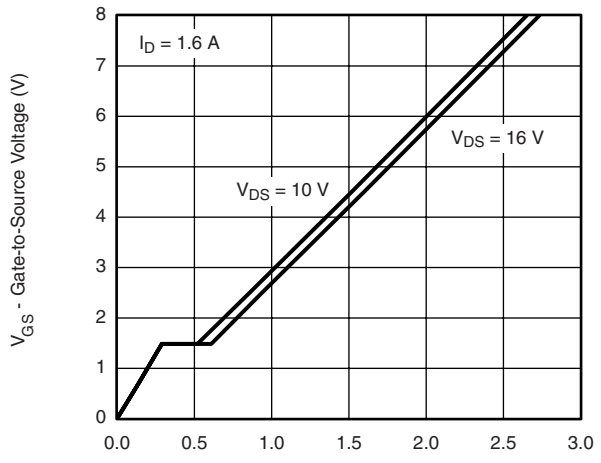

**Transfer Characteristics**



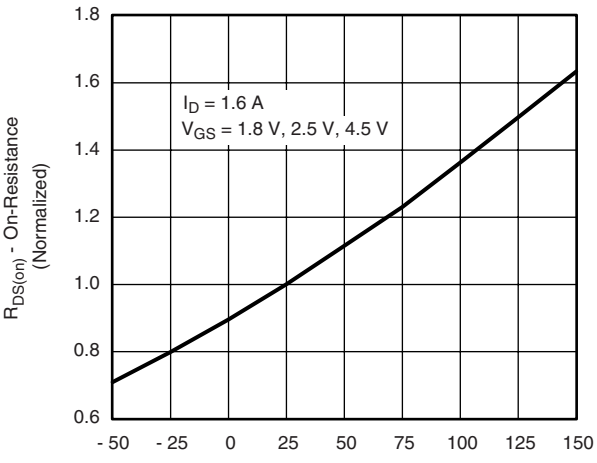

**On-Resistance vs. Drain Current**




**Capacitance**

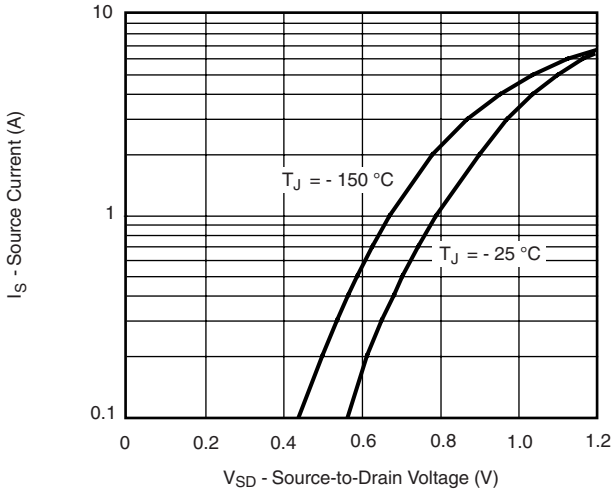



**Gate Charge**

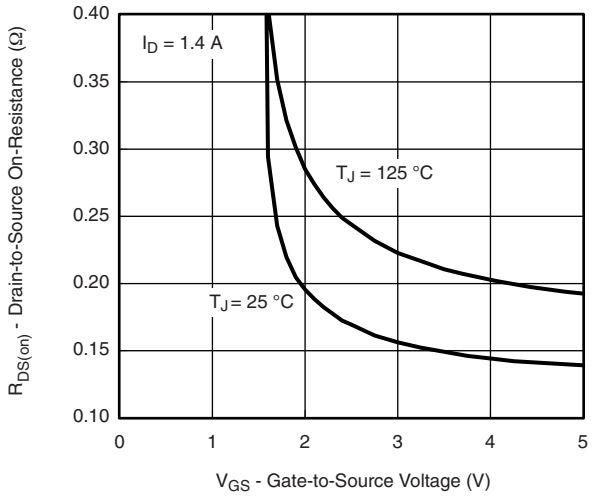



**On-Resistance vs. Junction Temperature**

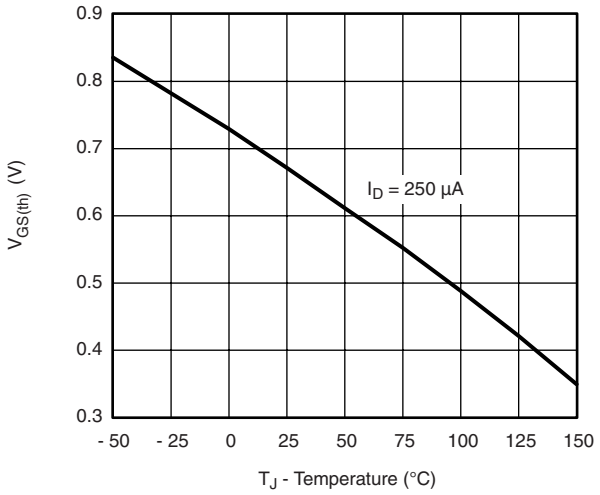
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



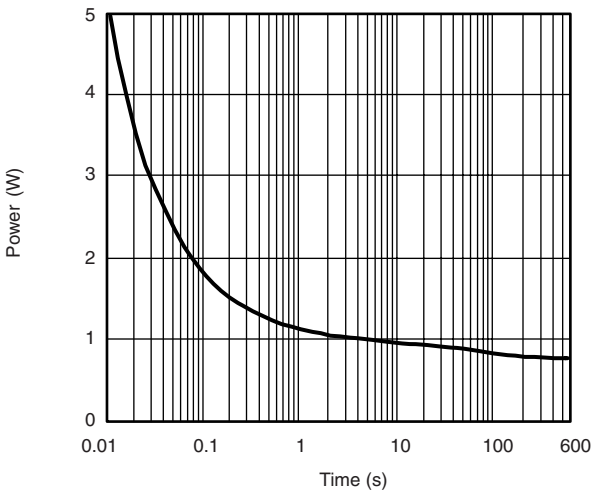

**Forward Diode Voltage**



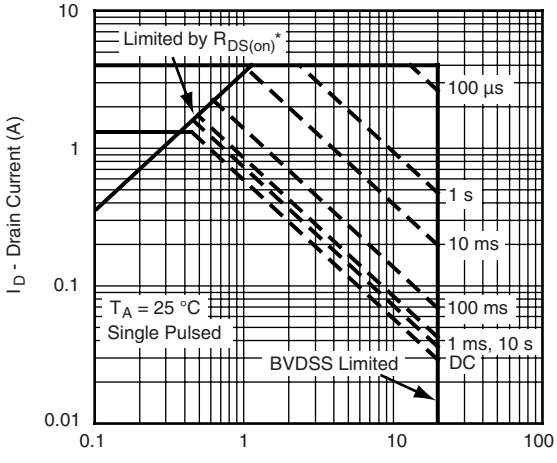

**On-Resistance vs. Gate-Source Voltage**




**Threshold Voltage**



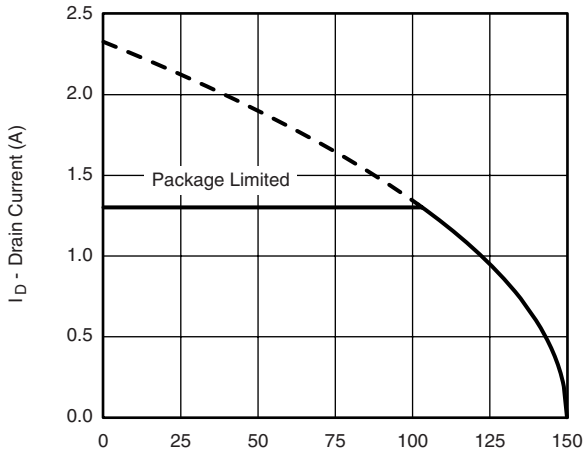

**Single Pulse Power**



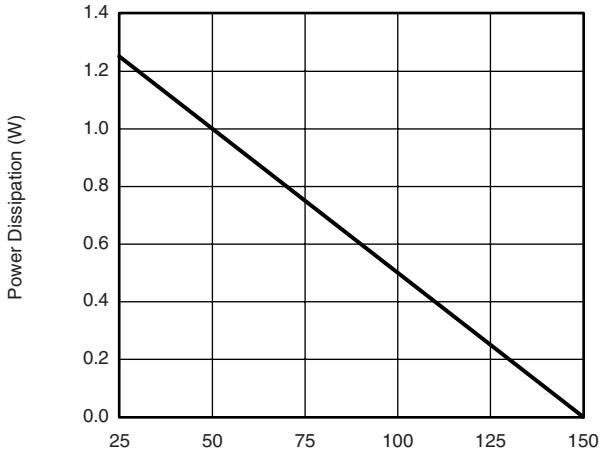

* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area, Junction-to-Case**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



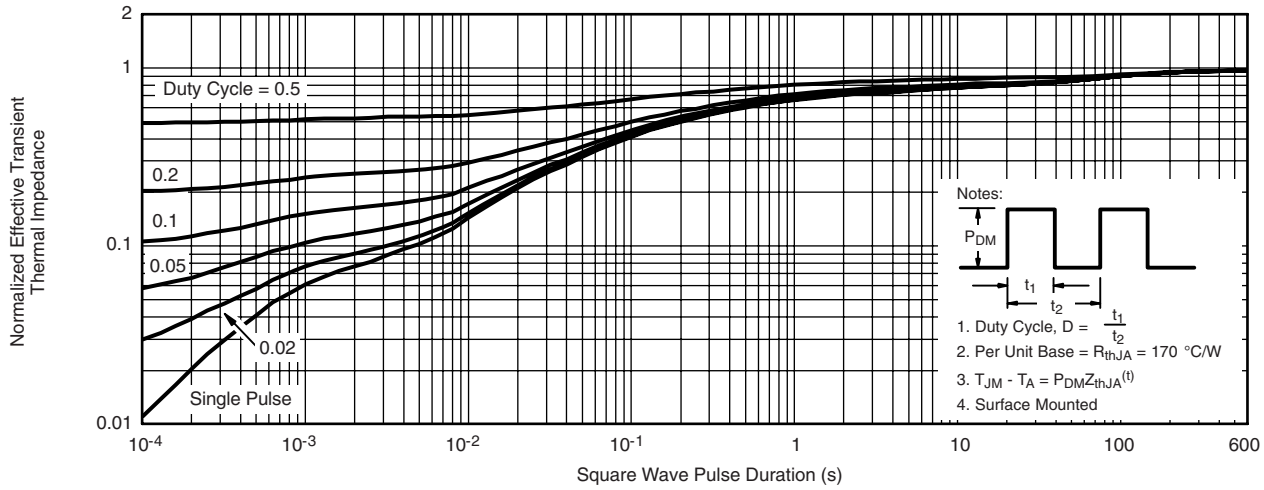

**Current Derating***



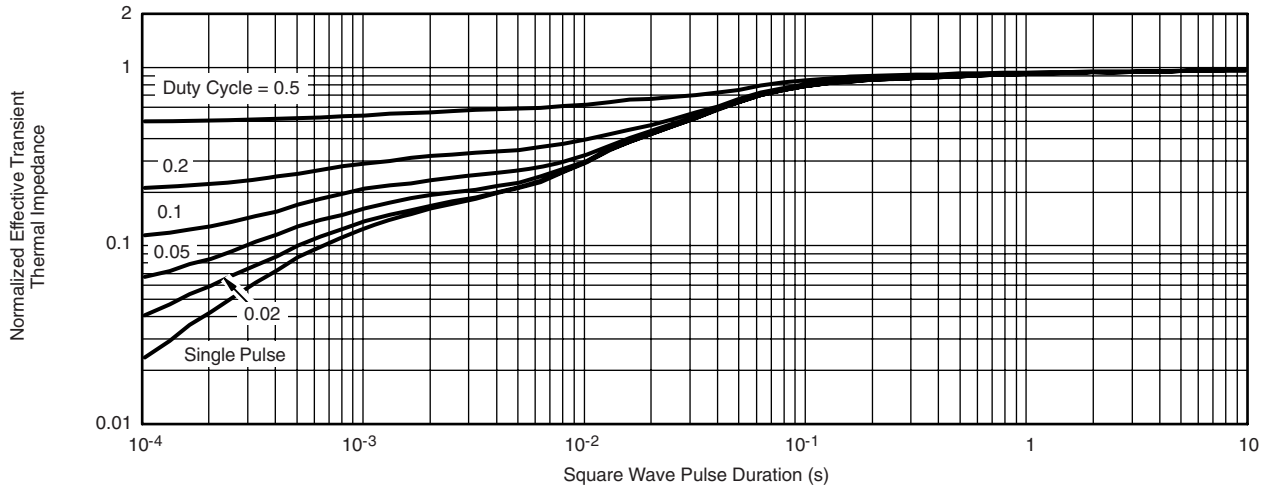

**Power Derating**

* The power dissipation $P_D$ is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted




**Normalized Thermal Transient Impedance, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Foot**

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