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# Basys3 Pin Assignments
# pour Disp1Digit.vhd
# version du 24/11/2016
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# On-board Slide Switches #
# Connection: V(3) de Disp1Digit sur SW3 => W17
set_property PACKAGE_PIN W17 [get_ports {V[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {V[3]}]
# Connection: V(2) de Disp1Digit sur SW2 => W16
set_property PACKAGE_PIN W16 [get_ports {V[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {V[2]}]
# Connection: V(1) de Disp1Digit sur SW1 => V16
set_property PACKAGE_PIN V16 [get_ports {V[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {V[1]}]
# Connection: V(0) de Disp1Digit sur SW0 => V17
set_property PACKAGE_PIN V17 [get_ports {V[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {V[0]}]
#maintenant Nous de complter un peu plus!
#n'oubliez pas de dfcommenter les lignes Complter
# Connection: N(1) de Disp1Digit sur SW15 => __vous
#set_property PACKAGE_PIN _vous [get_ports {N[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {N[1]}]
# Connection: N(0) de Disp1Digit sur SW14 => \widehat{\text{L}}vous
#set_property PACKAGE_PIN _vous [get_ports {N[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {N[0]}]
# On-board 7-segment Display #
# SEGMENTS
# Connection: S(6) de Disp1Digit sur vous => vous
#set_property PACKAGE_PIN _vous [get_ports {S[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[6]}]
# Connection: S(5) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {S[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[5]}]
# Connection: S(4) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {S[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[4]}]
# Connection: S(3) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {S[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[3]}]
# Connection: S(2) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {S[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[2]}]
# Connection: S(1) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {S[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[1]}]
# Connection: S(0) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {S[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {S[0]}]
# Connection: ENAN(3) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {ENAN[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ENAN[3]}]
# Connection: ENAN(2) de Disp1Digit sur vous => vous
#set_property PACKAGE_PIN _vous [get_ports {ENAN[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ENAN[2]}]
# Connection: ENAN(1) de Disp1Digit sur _vous ⇒ vous
#set_property PACKAGE_PIN _vous [get_ports {ENAN[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ENAN[1]}]
# Connection: ENAN(0) de Disp1Digit sur _vous => _vous
#set_property PACKAGE_PIN _vous [get_ports {ENAN[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {ENAN[0]}]
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