# Lab 3 Task 1

Name	Value	400 ns  500 ns  600 ns  700 ns  800 ns  900 ns  1,000 ns	1
Inputs			
¼ clk	0		
¼ rst	0		
> 🥞 A[15:0]	62385	U 0 X 67 X 53264 X 149 X 21 X	0
> 🥞 B[15:0]	49	U 0 151 32 19 49 6	52819
> 🥞 C[15:0]	61680	U	0
> 🥞 D[15:0]	35	U 1 (65535 X 10 X 65332 X	38
Output			
> <b>¾</b> O[31:0]	13	X 0 X 5 X 814 X 12 X 179736	χ 6
Internal Signals			
> 🤏 INTA[15:0]	63945	U 0 X 67 X 53264 X 149 X 21	X
> 🥞 INTB[15:0]	308	U 0 \( \) 181 \( \) 32 \( \) 19 \( \) 49	χ 6:
> 🥞 INTC[15:0]	61961	U 0 X 5 X 61961 X 61680	<del>-</del>
> 🥞 INTD[15:0]	10	U 1 (65535 X 10 (65332	5/5
> 🥞 INT1[17:0]	191835	X 0 X 201 X 159792 X 447 X 63	<del>-</del>
> 🥞 INT2[31:0]	19083988	X 0 X 604 X 160 X 1177259 X 3022320	<del>-</del> X
> 🥞 INT3[31:0]	19275823	X 0 X 805 X 159952 X 1177706 X 3022383	=
> 🥞 INT4[31:0]	1927582	X 0 X 805 X 2 X 117770 X 46	<del>-</del> X
> 🥞 INT5[31:0]	1989543	X 0 X 809 X 7 X 179731 X 61726	=
> <b>₹</b> INTO[31:0]	1989548	X 5 X 814 X 12 X 179736 X 61731	<del>-</del>

Name	Value	1,100 ns	1,200	ns  1,	300 ns	1,400 ns	1,500 ns	1,600	ns  1,700
Inputs									
ଧ⊌ clk	0								
₩ rst	0								
> 🤏 A[15:0]	65349	X O X	37 8	18 X 6	59 X 64!	06 X 64586	5 X 63:	945 623	885 (63919
> 🥞 B[15:0]	61664	62819 61	664 65	432 65	004	9	Х 31	08 4	9 (64474
> N C[15:0]	135	X o X	36 63	113 / 64	565	5	X 61:	961 616	580 X 0
> N D[15:0]	64255	38 / 62	309 8	4 (65	350	X 6184	5 \( \)	.0 3	5 18
Output									
→ N O[31:0]	153384	179736 (61731	X 5	176	76537378	128793	193573	(13	1989548
Internal Signals									
> <b>3 INTA[15:0]</b>	63919	21 0	37	88	69	64506 X	64586	63945	62385
> <b>考</b> INTB[15:0]	64474	49 (62819	61664	65432	65004	9		308	49
> 🐴 INTC[15:0]	0	61680 0	86	63113	64565	5		61961	61680
→ NTD[15:0]	18	65332 38	62309	54	65350	1	61845	10	35
→ 🥞 INT1[17:0]	191757	63 0	111	264	207	193518	193758	191835	187155
> 🔧 INT2[31:0]	0	30220 0	5303104	4129609816	X4196983260	45		19083988	3022320
→ NT3[31:0]	191757	30220 0	5303215	4129610080	4196983467	193563	193803	19275823	3209475
> <b>考</b> INT4[31:0]	10653	46 0	85	76474260	64223	193563	3	1927582	91699
→ NT5[31:0]	10653	61726 0	171	76537373	128788	193568	8	1989543	153379
> <b>3</b> INTO[31:0]	10658	61731 V 5	X 176	X 76537378	128793	193573 X	13	X 1989548	153384 X

Inputs   Uk clk	0 ns
13 rst     0       > % A[15:0]     65535     630	
> ¾ A[15.0]       65535       630	
> % B[15:0]       65535       308       49       64474       € 61664       X 63714       € 6535         > % C[15:0]       65535       610       € 61680       0       1 135       X 63924       € 6535         > % D[15:0]       65535       10       35       18       X 64255       X 244       X 65335         Output       35       18       X 64255       X 244       X 65335         internal Signals       13       X 1989548       X 153384       X 10658       X 272       X 16786744	
> % C[15:0]     65535     610	
> % D[15:0] 65535 10 \ 35 \ 18 \ \ 64255 \ \ 244 \ \ 65535 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
Output         3         O[31:0]         4         13         1989548         X         153384         10658         X         272         X         16786748           Internal Signals         10658 </td <td></td>	
> % O[31:0] 4 13 X 1989548 X 153384 X 10658 X 272 X 16756748 Internal Signals	
Internal Signals	
	X 4
> % INTA[15:0] 65535 63945 X 62385 X 63919 X 65349 X 64467 X	
	65535
> % INTB[15:0] 65535 308 X 49 X 64474 61664 X 63714 X	65535
> % INTC[15:0] 65535 61961 X 61680 X 0 135 X 63924 X	65535
> % INTD[15:0] 65535 10 X 35 X 18 64255 X 244 X	65535
> \$\inv11[17:0]   \q	.96605
> \$\ \mathre{\pi}	4836225
> %INT3[31:0] 65534 19275823 X 3209475 X 191757 X 6520687 X 4073047137 X	65534
> \$\ \text{INT4[31:0]} \ 0 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0
> % INT5[15:0] 4 61966 1927582 61685 X 5 140 X 63929 X	4
> % INTO[31:0] 4 1989548 X 153384 X 10658 X 272 X 16756745 X	4

```
Error:
test vectors {f value} 0
for inputs
A: 67
B: 151
C: 4
D: 1
for outputs
Actual value
0: 814
Predicted value
0: 814
Time: 880 ns Iteration: O Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 1
for inputs
A: 53264
B: 32
C: 5
D: 65535
for outputs
Actual value
0: 12
Predicted value
0: 12
Time: 960 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
INFO: [USF-XSim-96] XSim completed. Design snapshot
'Algorithm Lab 2A tb behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:04; elapsed = 00:00:05.
Memory (MB): peak = 826.105; gain = 4.074
run 5 us
Error:
test vectors value 2
for inputs
A: 149
B: 19
C: 61961
D: 10
for outputs
Actual value
0: 179736
Predicted value
O: 179736
```

```
Time: 1040 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 3
for inputs
A: 21
B: 49
C: 61680
D: 65332
for outputs
Actual value
0: 61731
Predicted value
O: 61731
Time: 1120 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 4
for inputs
A: 0
B: 62819
C: 0
D: 38
for outputs
Actual value
0: 5
Predicted value
Time: 1200 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 5
for inputs
A: 37
B: 61664
C: 86
D: 62309
for outputs
Actual value
O: 176
Predicted value
0: 176
Time: 1280 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 6
for inputs
A: 88
B: 65432
C: 63113
D: 54
for outputs
Actual value
O: 76537378
Predicted value
o: 76537378
```

```
Time: 1360 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 7
for inputs
A: 69
B: 65004
C: 64565
D: 65350
for outputs
Actual value
0: 128793
Predicted value
0: 128793
Time: 1440 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 8
for inputs
A: 64506
B: 9
C: 5
D: 1
for outputs
Actual value
O: 193573
Predicted value
0: 193573
Time: 1520 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 9
for inputs
A: 64586
B: 9
C: 5
D: 61845
for outputs
Actual value
0: 13
Predicted value
Time: 1600 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 10
for inputs
A: 63945
B: 308
C: 61961
D: 10
for outputs
Actual value
O: 1989548
Predicted value
0: 1989548
```

```
Time: 1680 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 11
for inputs
A: 62385
B: 49
C: 61680
D: 35
for outputs
Actual value
O: 153384
Predicted value
0: 153384
Time: 1760 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 12
for inputs
A: 63919
B: 64474
C: 0
D: 18
for outputs
Actual value
O: 10658
Predicted value
O: 10658
Time: 1840 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 13
for inputs
A: 65349
B: 61664
C: 135
D: 64255
for outputs
Actual value
O: 272
Predicted value
0: 272
Time: 1920 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 14
for inputs
A: 64467
B: 63714
C: 63924
D: 244
for outputs
Actual value
O: 16756745
Predicted value
0: 16756745
```

```
Time: 2 us Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4
Time: 2080 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

create\_clock -period 106.000 -name clk -waveform {0.000 53.000} [get\_ports clk]

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
√ impl_1	constrs_1	route_design Complete!	0.318	0.000	0.476	0.000	0.000	0.109	0	887	96	0.00	0	0

Name	Value	500 ns	600 ns	700 ns	800 ns		900 ns	1,000 ns	1,100 ns	1,200	.ns  1 <sub>2</sub>
Inputs											
¼ clk	0										
V₀ rst	0										
> 🤏 A[15:0]	65535	ū	0	X 67	532	64	149 2	1 X	o X :	17 (8	8 X 6
> = B[15:0]	65535	U (	0	151	У 3:	<u> </u>	19 4	9 \ 62	2819 61	664 65	432 65
> N C[15:0]	65535	U	0	X 4	X 5		51961 X 61	680 X	0 (	63	113 64
> 🥞 D[15:0]	65535	ū	1		655	35	10 \ 65	332 X	38 62	309 \ 5	4 65
Output											
> <b>3</b> O[31:0]	65540	×	0	$\square$ X	5		814	12	X 179736	61731	5
Internal Signals											
> 🥞 INTA[15:0]	65535	U	0	X	67	53264	149	21	χ ο	37	( 88
> 🥞 INTB[15:0]	65535	U	0		151	32	19	49	62819	61664	65432
> NTC[15:0]	65535	U	0		4	5	61961	61680	χ ο	86	63113
> 😽 INTD[15:0]	65535	U	X	1		65535	10	65332	Х 38	62309	54
> 🥞 INT1[17:0]	196605	×	0		201	159792	447	63	χ ο	111	264
> 🥞 INT2[31:0]	4294836225	х	0		604	160	1177259	3022320	χ •	5303104	4129609816
> 😽 INT3[31:0]	65534	Х	0	$\square$ X	805	159952	1177706	3022383	χο	5303215	4129610080
> 🥞 INT4[31:0]	0	х	X	0		805	) 2	117770	X 46	X •	85
> 🥞 INT5[31:0]	65540	Х	5		9	10	61966	61685	X 5	91	63118
> 🖥 INTO[31:0]	65540	х	0 X	5		814	12	179736	61731	X 5	176
Internal Pipeline 1 Signals											
> = INT3_pipeline_1[31:0]	65534	Х	X	0		805	159952	1177706	3022383	$\overline{}$	5303215
> 3 INT5_pipeline_1[31:0]	65540	×	× · ×	5		9	10	61966	61685	<u> </u>	91
> = INTD_pipeline_1[15:0]	65535	U	X	1			65535	10	65332	38	62309

Name	Value	1,200 ns
Inputs		
¹⊌ clk	0	
¹⊌ rst	0	
> 🍑 A[15:0]	65535	37 X 88 X 69 X 64506 X 64586 X 63945 X 62385 X 63919 X 65349 X 6446
> 🥞 B[15:0]	65535	6D 65432 65004 9 308 49 64474 61664 6371
> N C[15:0]	65535	86 (63113 (64565 ) 5 (61961 (61680 ) 0 (135 (6392
> 📲 D[15:0]	65535	60 54 65350 1 61845 10 35 18 64255 244
Output		
> NG O[31:0]	65540	61731 \ 5 \ 176 \ 76537378 \ 128793 \ 193573 \ 13 \ 1989548 \ 153384 \
Internal Signals		
> 🥞 INTA[15:0]	65535	37 X 88 X 69 X 64506 X 64586 X 63945 X 62385 X 63919 X 65349 X
> 🥞 INTB[15:0]	65535	61564
> 3 INTC[15:0]	65535	86
> 💐 INTD[15:0]	65535	62309 X 54 X 65350 X 1 X 61845 X 1D X 35 X 18 X 64255 X
> 🥞 INT1[17:0]	196605	111
> 🖥 INT2[31:0]	429483622	5303104 \( \) 41296090 \( \) 41969830 \( \) 45 \( \) \( \) 19083988 \( \) 3022320 \( \) 0 \( \) 8324640 \( \)
> 📲 INT3[31:0]	65534	5303215 (41296100 (41969830 ) 193563 (193803 (19275823 (3209475 ) 191757 (8520687 )
> 喝 INT4[31:0]	0	0 X 85 X 76474260 X 64223 X 193563 X 3 X 1927582 X 91699 X 10653 X
> 🥞 INT5[31:0]	65540	91
> 🔏 INTO[31:0]	65540	5 \ 176 \ \ 76537378 \ \ 128793 \ \ 193573 \ \ 13 \ \ 1989548 \ \ 153384 \ \ 10658 \
Internal Pipeline 1 Signals		
> 🥞 INT3_pipeline_1[31:0]	65534	0
> 🥞 INT5_pipeline_1[31:0]	65540	5
> 3 INTD_pipeline_1[15:0]	65535	38

Name	Value	1,800 ns  2,000 ns
Inputs		
¹ <mark>₀ c</mark> lk	0	
₩ rst	0	
> 🤏 A[15:0]	65535	62385 X 63919 X 65349 X 64467 X 65535
> 🥞 B[15:0]	65535	49 X 64474 X 61664 X 63714 X 65535
> NGC[15:0]	65535	61680 X 0 X 135 X 63924 X 65535
> 🥞 D[15:0]	65535	35 X 18 X 64255 X 244 X 65535
Output		
> NG O[31:0]	4	□ X 13 X 1989548 X 153384 X 10658 X 272 X 16756745 X 4
Internal Signals		
> 🖥 INTA[15:0]	65535	□ X 62385 X 63919 X 65349 X 64467 X 65535
> 喝 INTB[15:0]	65535	□ X 49 X 64474 X 61664 X 63714 X 65535
> = INTC[15:0]	65535	□ X 61680 X 0 X 135 X 63924 X 65535
> 🔻 INTD[15:0]	65535	10 35 18 64255 244 65535
> 🥞 INT1[17:0]	196605	□ X 187155 X 191757 X 196047 X 193401 X 196605
> 🖥 INT2[31:0]	429483622	□ 🗎 3022320 🚶 0 📉 8324640 📈 4072853□ 📈 4294836225
> 🖥 INT3[31:0]	65534	□ X 3209475 X 191757 X 8520687 X 4073047□ X 65534
> 🖥 INT4[31:0]	0	3 \ 1927582 \ \ 91699 \ \ 10653 \ \ 132 \ \ 16692816 \ \ 0
> 🔏 INT5[15:0]	4	□ X 61685 X 5 X 140 X 63929 X 4
> <b>¾</b> INTO[31:0]	4	13 1989548 153384 10658 272 16756745 4
Internal Pipeline 1 Signals		
> 3 INT3_pipeline_1[31:0]	65534	□ X 19275823 X 3209475 X 191757 X 8520687 X 4073047□ X 65534
> 🥞 INT5_pipeline_1[15:0]	4	10 61966 61685 5 140 63929 4
> 3 INTD_pipeline_1[15:0]	65535	□ \ 10 \ 35 \ 18 \ 64255 \ 244 \ 65535

```
Error:
test vectors {f value} 0
for inputs
A: 67
B: 151
C: 4
D: 1
for outputs
Actual value
0: 814
Predicted value
0: 814
Time: 960 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 1
for inputs
A: 53264
B: 32
C: 5
D: 65535
for outputs
Actual value
0: 12
Predicted value
0: 12
Time: 1040 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 2
for inputs
A: 149
B: 19
C: 61961
D: 10
for outputs
Actual value
0: 179736
Predicted value
O: 179736
Time: 1120 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 3
for inputs
A: 21
B: 49
C: 61680
D: 65332
for outputs
Actual value
0: 61731
Predicted value
O: 61731
```

```
Time: 1200 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 4
for inputs
A: 0
B: 62819
C: 0
D: 38
for outputs
Actual value
0: 5
Predicted value
0: 5
Time: 1280 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 5
for inputs
A: 37
B: 61664
C: 86
D: 62309
for outputs
Actual value
0: 176
Predicted value
0: 176
Time: 1360 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 6
for inputs
A: 88
B: 65432
C: 63113
D: 54
for outputs
Actual value
O: 76537378
Predicted value
O: 76537378
Time: 1440 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 7
for inputs
A: 69
B: 65004
C: 64565
D: 65350
for outputs
Actual value
0: 128793
Predicted value
O: 128793
```

```
Time: 1520 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 8
for inputs
A: 64506
B: 9
C: 5
D: 1
for outputs
Actual value
O: 193573
Predicted value
0: 193573
Time: 1600 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 9
for inputs
A: 64586
B: 9
C: 5
D: 61845
for outputs
Actual value
0: 13
Predicted value
0: 13
Time: 1680 ns Iteration: O Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 10
for inputs
A: 63945
B: 308
C: 61961
D: 10
for outputs
Actual value
O: 1989548
Predicted value
O: 1989548
Time: 1760 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 11
for inputs
A: 62385
B: 49
C: 61680
D: 35
```

```
for outputs
Actual value
0: 153384
Predicted value
O: 153384
Time: 1840 ns Iteration: O Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 12
for inputs
A: 63919
B: 64474
C: 0
D: 18
for outputs
Actual value
O: 10658
Predicted value
O: 10658
Time: 1920 ns Iteration: O Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 13
for inputs
A: 65349
B: 61664
C: 135
D: 64255
for outputs
Actual value
O: 272
Predicted value
0: 272
Time: 2 us Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 14
for inputs
A: 64467
B: 63714
C: 63924
D: 244
for outputs
Actual value
O: 16756745
Predicted value
O: 16756745
Time: 2080 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 15
```

create\_clock -period 98.000 -name clk -waveform {0.000 49.000} [get\_ports clk]

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
✓ ✓ synth_1	constrs_1	synth_design Complete!								897	161	0.00	0	0
✓ impl_1	constrs_1	route_design Complete!	0.634	0.000	0.166	0.000	0.000	0.109	0	887	161	0.00	0	0

The circuit is expected to reduce the critical paths length and in turn reduce total transition time for all of the combinational logic. The addition of pipeline 1 allows the multiplication's and the division sections of the equation to take place in two separate clock cycles. The multiplication and division are the most time-consuming sections of the combinational logic, the separation of these allows the clock period to be reduced thus increasing the maximum frequency. This happens because the time taken for the multiplication can happen in one clock cycle pre-pipeline 1 and then the division can happen in the next clock cycle separating the total time for each rather than it being a total of both which is what would happens pre including pipeline 1. The practice does match the theory that decreasing the length of the critical path increases the maximum frequency of the circuit.

Name	Value	500 ns		600 ns	1	700 ns		800	ns		900 ns		1.	,000 ns
Inputs														
¼ clk	1													
₩ rst	1													
> 🥞 A[15:0]	0	U	X	0		$=\chi$	67		53264	X	149	X	21	$=$ $\chi$
> 🥞 B[15:0]	0	U	X	0			151	<u> </u>	32	$=_{\chi}=$	19	$\overline{}$	49	$=$ $\chi$
> 🥞 C[15:0]	0	U	X	0		$\equiv_{\chi}$	4		5	$\overline{}$	6196.	ı X	6168	- X
> 💐 D[15:0]	1	U	X		1				65535	<u> </u>	10	<u> </u>	6533	2 X
Output														
> <b>%</b> O[31:0]	0	X		X		0			Х		5		X	814
Original Internal Signals														
> 🥞 INTA[15:0]	0	Ū		X	0		Χ	67	χ	53264	X	149	X	21
> 💐 INTB[15:0]	0	U		X	0		$=$ $\chi$	151	$\equiv_{\chi}$	32	$\equiv$ X	19		49
> 🥞 INTC[15:0]	0	U			0		X	4		5	$\Box$ X	61961		6168
> 💐 INTD[15:0]	1	υ				1			$\equiv$ X $\equiv$	65535	$\Box$ X	10		6533
> 💐 INT1[17:0]	0	×		X	0		$\equiv$ X $\equiv$	201		159792	$\Box$ X	447		63
> 💐 INT2[31:0]	0	×		X	0		$\equiv$ X $\equiv$	604	$\equiv \chi$	160	$\square X$	1177259	=X	30223
> 🥞 INT3[31:0]	0	X		X	0		X	805		159952	$\Box$ X	1177706		30223
> 🥞 INT4[31:0]	0	X		XX		0			=	805	$\square X$	2	$=$ $\times$	1177
> 喝 INT5[31:0]	5	×		X	5		$\equiv$ X $\equiv$	9	$\equiv$ X $\equiv$	10	$\square X$	61966		6168
> 🥞 INTO[31:0]	0	X		X	0		$-\chi$		5		$\square X$	814	$=$ $\times$	12
Internal Pipeline 1 Signals														
> 3 INT3_pipeline_1[31:0]	0	×		X		0			X	805	$\square X$	159952	$=$ $\times$	11777
> 🥞 INT5_pipeline_1[31:0]	0	X		0	=		5		=X $=$	9	$\perp x$	10	=X	6196
> 🥞 INTD_pipeline_1[15:0]	1	υ					1				$\perp x$	65535	=X	10
Internal Pipeline 2 Signals														
> 3 INT4_pipeline_2[31:0]	0	×		X			0				$\square X$	805	$=$ $\times$	2
> % INT5_pipeline_2[31:0]	0	X		<u> </u>	0		X_		5		$-\chi$	9	\	10

Name	Value		1,000 ns		1,100 ns	s .	1,20	0 ns	1	1,300	ns	[3	L,400 ns		1,500 ns
Inputs															
¹₀ clk	1														
¹₀ rst	1														
> N A[15:0]	0	149 2	1	0	$\Box$ X	37	$=$ $\times$	88	3 X	69	Х	645	06	64586	
> 🥞 B[15:0]	0	19 4	9	62819		6166	1 X	654	32	6500	4 X		9		
> N C[15:0]	0	610 616	80	0	$\Box$ X	86	$=$ $\times$	631.	13	6456	5		5		
> 🔏 D[15:0]	1	10 653	32	38	$\Box \chi \Box$	62309	<del>,</del>	54	ι χ	6535	o X		$\overline{}$	61845	$\perp \times$
Output															
> N O[31:0]	0	5	814	X	12	X	179736	X	61731	$\Box \chi$	5	X	176	$-\chi$	7653737
Original Internal Signals															
> NTA[15:0]	0	149	21	X	0	X	37	X	88	$\Box \chi$	69	$=$ $^{\!$	64506	$-\chi$	64586
> 🥞 INTB[15:0]	0	19	49		62819	$\overline{x}$	61664		65432		65004			9	
> = INTC[15:0]	0	61961	61680	$\neg x$	0	$\overline{}$	86	$\equiv$ X	63113	$\Box$ X	64565	$=$ $\times$		5	
> 🖥 INTD[15:0]	1	10	65332	$\supset \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	38	X	62309	=	54	$\square$ X	65350	$=$ $\times$	1	$ = \chi $	61845
> 🥞 INT1[17:0]	0	447	63		0	$\equiv$ X	111	$\equiv$ X	264	$\square$ X	207	=X	193518		193758
> 🥞 INT2[31:0]	0	1177259	3022320		0	$\overline{x}$	5303104		412960981	5 X	41969832	60 X		45	
> 🥞 INT3[31:0]	0	1177706	3022383		0	$\equiv$ X	5303215	$\equiv$ X	412961008	<u>-</u> Σχ	41969834	67 X	193563	$\equiv$ X $\equiv$	193803
> NT4[31:0]	0	2	117770	$\supset \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	46	X	0	=	85	$\square$ X	7647426	• X	64223	$ = \chi $	193563
> 🥞 INT5[31:0]	5	61966	61685		5	$\equiv$ X	91	$\equiv$ X	63118	$\square$ X	64570	=X		10	
> 🥞 INTO[31:0]	0	814	12		179736	X	61731	=X	5	$\square$ X	176	$=$ $\times$	76537378	$\perp X$	128793
Internal Pipeline 1 Signals															
> 3 INT3_pipeline_1[31:0]	0	159952	1177706	$\square$ X $\square$	3022383	X	0	X	5303215	X	41296100	80 X	4196983467	7_X	193563
> = INT5_pipeline_1[31:0]	0	10	61966	$\supset \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	61685	=X	5	$\equiv$ X	91	$\square$ X	63118	=X	64570	$\equiv \chi$	
> 3 INTD_pipeline_1[15:0]	1	65535	10		65332	$\equiv$ X $$	38	$=$ $\hat{X}$	62309	$\square$ X	54		65350		1
Internal Pipeline 2 Signals															
> 3 INT4_pipeline_2[31:0]	0	805	2		117770	$\equiv \chi$	46	X	0	$\square$ X	85	X	76474260	$\square$ X	64223
> NT5_pipeline_2[31:0]	0	9	10	$-\chi$	61966	$\overline{\chi}$	61685	$\overline{\chi}$	5	$-\chi$	91	X	63118	$\neg \chi \overline{}$	64570

Name	Value	]	1,500 ns	1,600 n	s	1,700 n	·	1,800 ns	
Inputs									
ી∳ clk	1								
¼ rst	1								
> N A[15:0]	0	64506 64586	63	945 6	2385	63919	65:	349	64467
> 📲 B[15:0]	0	9	Х 3	08	49	64474	61	64	63714
> = C[15:0]	0	5	61	961 6:	1680	0	1:	35	63924
> 🖥 D[15:0]	1	1 61845	X :	10	35	18	64:	55	244
Output									
> <b>3</b> O[31:0]	0	176	76537378	128793	193573	$\perp$ X $\equiv$	13	1989548	
Original Internal Signals									
> 考 INTA[15:0]	0	64506	64586	63945	62385	$ \subset X \subset$	63919	65349	
> 考 INTB[15:0]	0	9		308	X 49	$\equiv$ X $\equiv$	64474	61664	
> = INTC[15:0]	0	5		61961	X 61680	=X $=$	0	135	
> 🔏 INTD[15:0]	1	1	61845	10	35	$\square$ X $\square$	18	64255	$\equiv$ X $\equiv$
> 🔧 INT1[17:0]	0	193518	193758	191835	187155	$\square$ X $\square$	191757	196047	$\equiv$ X $\equiv$
> 🔧 INT2[31:0]	0	45		19083988	3022320	$\square$ X $\square$	0	8324640	$\square$ X $\square$
> 🔧 INT3[31:0]	0	193563	193803	19275823	3209475	$\square$ X $\square$	191757	8520687	$\perp \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$
> 🔧 INT4[31:0]	0	64223	193563	X 3	1927582	$\square$ X $\square$	91699	10653	$\perp X$
> 🐴 INT5[31:0]	5	10		61966	61685	=	5	140	=X $=$
> 🔏 INTO[31:0]	0	76537378	128793	193573	13	X	1989548	153384	=X $=$
Internal Pipeline 1 Signals									
> 🐴 INT3_pipeline_1[31:0]	0	4196983467	193563	193803	19275823	$\equiv$ X $\equiv$	3209475	191757	$\equiv$ X $\equiv$
> 考 INT5_pipeline_1[31:0]	0	64570		10	61966	=	61685	5	=X $=$
> 🔏 INTD_pipeline_1[15:0]	1	65350	1	61845	10		35	18	=
Internal Pipeline 2 Signals									
> 🔏 INT4_pipeline_2[31:0]	0	76474260	64223	193563	Х	$\square$ X $\square$	1927582	91699	
> 🔏 INT5_pipeline_2[31:0]	0	63118	64570	X	10	$\equiv \chi$	61966	61685	=X $=$

Name	Value		1,800 ns		1,900 ns		2,000	ns	2,	100 ns		2,200 :	ns
Inputs													
¼ clk	1										1		
¹७ rst	U												
> 🥞 A[15:0]	U	65	349 X 64	467	Χ				55	535			
> 🖥 B[15:0]	U	61	664 X 63	714	E <sub>X</sub>				55	535			
> N C[15:0]	U		35 <b>X</b> 63	924	X				55	535			
> 🥞 D[15:0]	U	64	255 / 2	44					55	535			
Output													
> N O[31:0]	Х	13	1989548	χ_	153384	10	658	χ 2'	2	X 167	56745	<u> </u>	4
Original Internal Signals													
> 🖥 INTA[15:0]	U	60 )	65349	X_	64467					65535			
> 💐 INTB[15:0]	U	60	61664	χ	63714	=				65535			
> 3 INTC[15:0]	U	=	135	χ	63924	=				65535			
> 🖥 INTD[15:0]	U	18	64255	χ	244	$\equiv$				65535			
> 🥞 INT1[17:0]	X	=	196047	χ	193401	$\overline{}$				196605			
> 🥞 INT2[31:0]	X	=	8324640	X 40	72853736	$\equiv$			42	2948362	25		
> 🥞 INT3[31:0]	X	$\equiv$	8520687	X 40	73047137	$\overline{}$				65534			
> 🥞 INT4[31:0]	X	90	10653	χ	132	1669	2816	χ			0		
> 🥞 INT5[15:0]	X	5	140	χĦ	63929	$\overline{}$				4			
> 😽 INTO[31:0]	X	=	153384	χĦ	10658		72	X 1675	6745	χ		4	
Internal Pipeline 1 Signals	6												
> 3 INT3_pipeline_1[31:0]	Х	30	191757	χ	8520687	40730	47137	χ			65534		

```
Error:
test vectors value 0
for inputs
A: 67
B: 151
C: 4
D: 1
for outputs
Actual value
0: 814
Predicted value
0: 814
Time: 1040 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 1
for inputs
A: 53264
B: 32
C: 5
D: 65535
for outputs
Actual value
0: 12
Predicted value
0: 12
Time: 1120 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 2
for inputs
A: 149
B: 19
C: 61961
D: 10
for outputs
Actual value
O: 179736
Predicted value
O: 179736
Time: 1200 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 3
for inputs
A: 21
B: 49
C: 61680
D: 65332
```

```
for outputs
Actual value
O: 61731
Predicted value
0: 61731
Time: 1280 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 4
for inputs
A: 0
B: 62819
C: 0
D: 38
for outputs
Actual value
0: 5
Predicted value
0: 5
Time: 1360 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 5
for inputs
A: 37
B: 61664
C: 86
D: 62309
for outputs
Actual value
0: 176
Predicted value
0: 176
Time: 1440 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 6
for inputs
A: 88
B: 65432
C: 63113
D: 54
for outputs
Actual value
O: 76537378
Predicted value
O: 76537378
Time: 1520 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 7
for inputs
A: 69
B: 65004
C: 64565
D: 65350
```

```
for outputs
Actual value
0: 128793
Predicted value
O: 128793
Time: 1600 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 8
for inputs
A: 64506
B: 9
C: 5
D: 1
for outputs
Actual value
O: 193573
Predicted value
0: 193573
Time: 1680 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 9
for inputs
A: 64586
B: 9
C: 5
D: 61845
for outputs
Actual value
0: 13
Predicted value
0: 13
Time: 1760 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 10
for inputs
A: 63945
B: 308
C: 61961
D: 10
for outputs
Actual value
O: 1989548
Predicted value
O: 1989548
Time: 1840 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 11
for inputs
A: 62385
B: 49
C: 61680
D: 35
```

```
for outputs
Actual value
0: 153384
Predicted value
0: 153384
Time: 1920 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 12
for inputs
A: 63919
B: 64474
C: 0
D: 18
for outputs
Actual value
O: 10658
Predicted value
O: 10658
Time: 2 us Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test_vectors value 13
for inputs
A: 65349
B: 61664
C: 135
D: 64255
for outputs
Actual value
0: 272
Predicted value
O: 272
Time: 2080 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 14
for inputs
A: 64467
B: 63714
C: 63924
D: 244
for outputs
Actual value
O: 16756745
Predicted value
O: 16756745
```

```
Time: 2160 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT

Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4
Time: 2240 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

# 2.1.6 create\_clock -period 93.000 -name clk -waveform {0.000 46.500} [get\_ports clk]

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	210	0.00	0	0
√ impl_1	constrs_1	route_design Complete!	0.802	0.000	0.122	0.000	0.000	0.110	0	887	210	0.00	0	0

The expectation of the maximum frequency after the inclusion of pipeline 2 is an increase due to the isolation of the division between the pipelines 1 & 2. Previously the time taken to process the division and the addition was the critical path, the isolation of the combinational logic of the divider between the pipelines means that the critical path is once more reduced. This reduction of the critical path also reduces the time for the combinational logic as it is only the time for the divider to process and not the result of the divider and addition to process. This means the critical paths time is reduced and increasing the frequency of the circuit over all. Without the pipeline 2 the maximum frequency would be lower as the time taken to process the divider and addition is higher than the time to process just the divider.

Name	Value	300 ns	400 ns	500 ns	600 ns	700 2	15	800 ns	s  99	00 ns	1,000 ns	1,100 ns	1,200	ns
Inputs														
¹% clk	0													
₽ rst	U													
> = A[15:0]	U		U	X	0		67	532	64 1	149 \ 2	1 X	0 X 3	37 (	88 X
> = B[15:0]	U		U		0		151	Х 3	2 X	19 / 4	9 ( 62	819 (61	664 65	432
> N C[15:0]	U		U		0		4	X 5	(61	1961 \ 61	680 X	0 X 8	63	113
> N D[15:0]	U		U	X		1		655	35	10 \ 65:	332 X 3	38 (62	309	54
Output														
> NGO[31:0]	X		х		X		0			χ	s	814	12	17973
Original Internal Signals														
> = INTA[15:0]	U		U		χ	0	$\square$ X	67	53264	X 149	21	X 0 .	37	X 88
> = INTB[15:0]	U		U		χ	0	X:	151	32	X 19	49	62819	61664	6543
> = INTC[15:0]	U		U		Χ	0	=	4	5	61961	61680	X 0	X 86	6311:
> = INTD[15:0]	U		U		X	1			65535	X 10	65332	Х 38	62309	54
> = INT1[17:0]	X		х		X	0	_X :	201	159792	447	63	X 0	111	264
> = INT2[31:0]	X		х		Χ	0	_X_,	504	160	1177259	3022320	X 0	5303104	X4129609
> = INT3[31:0]	X		х		X	0			805	159952	1177706	3022383	X	53032.
> = INT4[31:0]	X		х		Χ		0			X 805	2	117770	46	χ ο
> 🔧 INT5[31:0]	Х		х		Χ	5	=	9	10	61966	61685	5	91	6311:
> = INTO[31:0]	Х		х		X	0				5	814	12	179736	6173.
Internal Pipeline 1 Signals														
> = INT3_pipeline_1[31:0]	Х		х		X		0			X 805	159952	1177706	3022383	χ •
> = INT5_pipeline_1[31:0]	X		х		χ	0	=			X 9	10	61966	61685	5
> NTD_pipeline_1[15:0]	U		U		Χ			1			65535	10	65332	Х 38
Internal Pipeline 2 Signals														
> 3 INT4_pipeline_2[31:0]	X		х		X			0			805	2	117770	46
> 3 INT5_pipeline_2[31:0]	Х		х		Χ	0				5	9	10	61966	6168
Internal Pipeline 3 Signals														
> = INT1_pipeline_3[17:0]	X		х		X	0			201	159792	447	63	X	X 111
> 🔏 INT2_pipeline_3[31:0]	Х		х		X	0		$\Box$	604	160	1177259	3022320	X	53031
> 🔻 INTD_pipeline_3[15:0]	U		U		X		1			65535	10	65332	Х 38	6230:
> 3 INT5_pipeline_3[31:0]	Х		х		X 0	$\subset$	5		9	X 10	61966	61685	X 5	91

Name	Value	
Inputs		
ଧ₀ clk	0	
¹७ rst	U	
> 🔏 A[15:0]	U	0
> 🤏 B[15:0]	U	62819 (61664 ) 65432 (65004 ) 9 (308 ) 49
> 🥞 C[15:0]	U	0
> 🥞 D[15:0]	U	38
Output		
> <b>™</b> O[31:0]	X	5 814 12 179736 61731 5 176 76537378 128793
Original Internal Signals		
> 🥞 INTA[15:0]	U	21 0 37 88 69 64506 64586 63945 62385
> 🥞 INTB[15:0]	U	49 62819 61664 65432 65004 9 308 49
> 3 INTC[15:0]	U	D 0 86 63113 64565 5 61961 61680
> 😽 INTD[15:0]	U	□ \ 38 \ 62309 \ 54 \ 65350 \ 1 \ 61845 \ 10 \ 35
> 🥞 INT1[17:0]	X	63 0 111 264 207 193518 193758 191835 187158
> 🥞 INT2[31:0]	X	0 \ 5303104 \\\ 4129609816 \\\ 4196983260 \\\ 45 \\\ \\ 19083988 \\\ 302232
> 🥞 INT3[31:0]	X	□ X 3022383 X 0 X 5303215 X4129610080 X4196983467 X 193563 X 193803 X 1927582
> 🥞 INT4[31:0]	X	2 117770 46 0 85 76474260 64223 193563 3
> 🥞 INT5[31:0]	X	D 5 91 63118 64570 10 61966 61685
> 🥞 INTO[31:0]	X	12     179736     61731     5     176     75537378     128793     193573
Internal Pipeline 1 Signals		
> 3 INT3_pipeline_1[31:0]	X	□ \ 1177706 \ 3022383 \ 0 \ \ 5303215 \ \ \ 4129610080 \ \ 41 \ 96983467 \ \ 193563 \ \ 193803
> 🥞 INT5_pipeline_1[31:0]	X	10 61966 61685 5 91 63118 64570 10
> 3 INTD_pipeline_1[15:0]	U	D 10 65332 38 62309 54 65350 1 61845
Internal Pipeline 2 Signals		
> 🐝 INT4_pipeline_2[31:0]	X	0     2     117770     46     0     85     75474260     64223     193563
> 3 INT5_pipeline_2[31:0]	X	9 10 61966 61685 5 91 63118 64570
Internal Pipeline 3 Signals		
> 😽 INT1_pipeline_3[17:0]	Χ	□ X 63 X 0 X 111 X 264 X 207 X 193518 X 193758 X 191838
> 🥞 INT2_pipeline_3[31:0]	X	□ X 3022320 X 0 X 5303104 X4129609816 X4196983260 X 45 X 1908396
>  INTD_pipeline_3[15:0]	U	10 65332 38 62309 54 65350 1 61845 10
> 🐝 INT5_pipeline_3[31:0]	Х	□ X 61685 X 5 X 91 X 63118 X 64570 X 10 X 61966

Name	Value	
Inputs		
⅓ clk	0	
¼ rst	U	
> 🥞 A[15:0]	U	63945
> 🥞 B[15:0]	U	308 49 64474 61664 63714 65535
> NG C[15:0]	U	61961
> N D[15:0]	U	10 35 18 64255 244 65535
Output		
> NG O[31:0]	X	□ \( \frac{7653}{378} \) \( \frac{128793}{128793} \) \( \frac{193573}{13} \) \( \frac{1989548}{1989548} \) \( \frac{153384}{10658} \) \( \frac{272}{16756745} \) \( 4 \)
Original Internal Signals		
> 🥞 INTA[15:0]	U	□ X 63945 X 62385 X 63919 X 65349 X 64467 X 65535
> 😽 INTB[15:0]	U	9 308 49 64474 61664 63714 65535
> NTC[15:0]	U	5 (61961 (61680 ) 0 135 (63924 ) 65535
> 😽 INTD[15:0]	U	□ \ 1D \ 35 \ 18 \ 64255 \ 244 \ 65535
> 😽 INT1[17:0]	X	□ \ 191335 \ 187155 \ 191757 \ 196047 \ 193401 \ \ 196605
> 😽 INT2[31:0]	X	45 (19083988 X 3022320 X 0 X 8324640 X 40728530 X 4294836225
> 🖥 INT3[31:0]	X	□ X 193303 X 19275823 X 3209475 X 191757 X 8520687 X 4073047□ X 65\$34
> 🖥 INT4[31:0]	X	□ X 193563 X 3 X 1927582 X 91699 X 10653 X 132 X 16692816 X 0
> 🔏 INT5[15:0]	X	10 61966 61685 5 140 63929 4
> = INTO[31:0]	X	□ X 128793 X 193573 X 13 X 1989548 X 153384 X 10658 X 272 X 16756745 X 4
Internal Pipeline 1 Signals		
> 🖥 INT3_pipeline_1[31:0]	X	□ X 193563 X 193803 X19275823 X 3209475 X 191757 X 8520687 X4073047□ X 65534
> 考 INT5_pipeline_1[15:0]	X	□ \ 10 \ \ 61966 \ 61685 \ 5 \ \ 140 \ \ 63929 \ 4
> NTD_pipeline_1[15:0]	U	□ \ 1 \ \ 61845 \ \ 10 \ \ 35 \ \ 18 \ \ 64255 \ \ 244 \ \ 65535
Internal Pipeline 2 Signals		
> = INT4_pipeline_2[31:0]	X	□ X 64223 X 193563 X 3 X 1927582 X 91699 X 10653 X 132 X 16692816 X 0
> 3 INT5_pipeline_2[15:0]	Х	□ X 64\$70 X 10 X 61966 X 61685 X 5 X 140 X 63929 X 4
Internal Pipeline 3 Signals		
> 考 INT1_pipeline_3[17:0]	X	□ X 193758 X 191835 X 187155 X 191757 X 196047 X 193401 X 196605
> 💐 INT2_pipeline_3[31:0]	X	45 X19083988 X 3022320 X 0 X 8324640 X 4072853D X 4294836225
> NTD_pipeline_3[15:0]	U	1 61845 10 35 18 64255 244 65535

```
run 5 us
Error:
test vectors value 0
for inputs
A: 67
B: 151
C: 4
D: 1
for outputs
Actual value
0: 814
Predicted value
0: 814
Time: 1120 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 1
for inputs
A: 53264
B: 32
C: 5
D: 65535
for outputs
Actual value
0: 12
Predicted value
Time: 1200 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 2
for inputs
A: 149
B: 19
C: 61961
D: 10
for outputs
Actual value
O: 179736
Predicted value
0: 179736
Time: 1280 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 3
for inputs
A: 21
B: 49
C: 61680
D: 65332
for outputs
Actual value
0: 61731
Predicted value
O: 61731
```

```
Time: 1360 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 4
for inputs
A: 0
B: 62819
C: 0
D: 38
for outputs
Actual value
0: 5
Predicted value
0: 5
Time: 1440 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 5
for inputs
A: 37
B: 61664
C: 86
D: 62309
for outputs
Actual value
O: 176
Predicted value
0: 176
Time: 1520 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 6
for inputs
A: 88
B: 65432
C: 63113
D: 54
for outputs
Actual value
O: 76537378
Predicted value
O: 76537378
Time: 1600 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 7
for inputs
A: 69
B: 65004
C: 64565
D: 65350
for outputs
Actual value
0: 128793
Predicted value
O: 128793
```

```
Time: 1680 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 8
for inputs
A: 64506
B: 9
C: 5
D: 1
for outputs
Actual value
O: 193573
Predicted value
0: 193573
Time: 1760 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 9
for inputs
A: 64586
B: 9
C: 5
D: 61845
for outputs
Actual value
0: 13
Predicted value
Time: 1840 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 10
for inputs
A: 63945
B: 308
C: 61961
D: 10
for outputs
Actual value
O: 1989548
Predicted value
O: 1989548
Time: 1920 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 11
for inputs
A: 62385
B: 49
C: 61680
D: 35
for outputs
Actual value
0: 153384
Predicted value
0: 153384
```

```
Time: 2 us Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 12
for inputs
A: 63919
B: 64474
C: 0
D: 18
for outputs
Actual value
O: 10658
Predicted value
O: 10658
Time: 2080 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 13
for inputs
A: 65349
B: 61664
C: 135
D: 64255
for outputs
Actual value
0: 272
Predicted value
O: 272
Time: 2160 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 14
for inputs
A: 64467
B: 63714
C: 63924
D: 244
for outputs
Actual value
O: 16756745
Predicted value
0: 16756745
Time: 2240 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 15
for inputs
A: 65535
B: 65535
C: 65535
D: 65535
for outputs
Actual value
Predicted value
0:4
Time: 2320 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
```

2.1.8

create\_clock -period 92.000 -name clk -waveform {0.000 46.000} [get\_ports clk]

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	293	0.00	0	0
√ impl_1	constrs_1	route_design Complete!	0.737	0.000	0.095	0.000	0.000	0.110	0	887	293	0.00	0	0

The addition of pipeline 3 is not expected to increase the maximum frequency but it does as it separates the multiplications and the preceding addition. The increase in the frequency was not expected as the multiplications are separated from the extra addition but the critical path is still located in the divider so the small increase in the maximum frequency is a surprise as it does match the theory that pipelining increases the maximum frequency but does not match the theory in that the critical path was not affected this time and still the maximum frequency increased.

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
use work.DigEng.all;
-- Algorithm entity
-- Synchronous calculator of the equation
-- O <= (A*3 + B*C)/D + C +5
-- 6 inputs, including standard clk and reset
-- Inputs A, B, C, D 16 bit std logic vector inputs of values
-- to computate.
-- output O is result of the equation.
-- 5 registered pipelined sections including input and outputs
-- Computation of equation takes 5 clk clyes from input to output
-- 1st Input Register input registers to store inputs
-- 2nd "pipeline 3" results of (3*A), (B*C), D, (5+C) each stored in
registers
-- 3rd "pipeline 1" results of (3*A)+(B*C), D, (5+C) each stored in
registers
-- Note* divider has 34 internal pipelined sections requiring a
-- Pipelined array of (5+C) made up of 34 registers using the FIFO
-- 4th "pipeline 2" results of (3*A) + (B*C) / D, (5+C) each stored in
registers
-- 5th output registers results of ((3*A)+(B*C)/D)+(5+C) stored in
register
entity algorithm is
    generic (data size : integer := 16);
    Port ( A : in STD LOGIC VECTOR (data size-1 downto 0);
           B : in STD LOGIC VECTOR (data_size-1 downto 0);
           C : in STD LOGIC VECTOR (data_size-1 downto 0);
           D : in STD LOGIC VECTOR (data size-1 downto 0);
           O : out STD LOGIC VECTOR (data size*2-1 downto 0);
           clk: in STD LOGIC;
           rst : in STD LOGIC);
end algorithm;
architecture Behavioral of algorithm is
-- internal input signals
signal INTA, INTB, INTC, INTD : UNSIGNED (data size-1 downto 0);
-- internal signals connecting signals to modify via math functions
signal INT1 : UNSIGNED (data_size+1 downto 0);
signal INT2 : UNSIGNED (data_size*2-1 downto 0);
signal INT3 : UNSIGNED (data_size*2-1 downto 0);
signal INT4 : UNSIGNED (data_size*2-1 downto 0);
signal INT5 : UNSIGNED (data_size-1 downto 0);
signal INTO : UNSIGNED (data size*2-1 downto 0);
-- signals added for pipeline 1
signal INT3 pipeline 1 : UNSIGNED (data size*2-1 downto 0);
signal INT5_pipeline_1 : UNSIGNED (data_size-1 downto 0);
signal INTD pipeline 1 : UNSIGNED (data size-1 downto 0);
```

```
-- signals added for pipeline 2
signal INT4 pipeline 2 : UNSIGNED (data size*2-1 downto 0);
signal INT5 pipeline 2 : UNSIGNED (data size-1 downto 0);
-- signals added for pipeline 3
signal INT1 pipeline 3 : UNSIGNED (data size+1 downto 0);
signal INT2_pipeline_3 : UNSIGNED (data size*2-1 downto 0);
signal INTD pipeline 3 : UNSIGNED (data size-1 downto 0);
signal INT5 pipeline 3 : UNSIGNED (data size-1 downto 0);
begin
-- setup for individual input registers for inputs A,B, C & D
-- All Synchronous with reset to zero when reset signal active,
-- NO enable signals required.
input regs: process (clk) is
begin
  if rising edge(clk) then
  -- resets internal signals below to zero
    if rst = '1' then
      INTA <= (others => '0');
      INTB <= (others => '0');
      INTC <= (others => '0');
      INTD \langle = (0 \Rightarrow '1', others \Rightarrow '0'); -- aggregate notation
      INTD <= to unsigned(1,INTD'length); -- type conversion notation</pre>
    else
     -- connects inputs to internal signal values
      INTA <= unsigned(A);</pre>
      INTB <= unsigned(B);</pre>
      INTC <= unsigned(C);</pre>
      INTD <= unsigned(D);</pre>
    end if;
  end if;
end process input_regs;
-- equation maths defined per internal signals
-- INT1 result of INTA multiplied by 3
INT1 <= INTA * to unsigned(3, 2);</pre>
INT2 <= INTB * INTC;</pre>
INT5 <= INTC + to_unsigned(5, INT5'length);</pre>
--in between pipline 3 and pipline 1
INT3 <= INT1 pipeline 3 + INT2 pipeline 3;</pre>
--in between pipline 1 and pipline 2
INT4 <= INT3 pipeline 1 / INTD pipeline 1;</pre>
--in between pipline 2 and pipline output registers
INTO <= INT5 pipeline 2 + INT4 pipeline 2;</pre>
-- output register.
-- synchronous.
-- NO enable
-- output = 0 at rising clk edge
-- when input reset is active.
-- output = INTO at rising clk edge.
output regs: process (clk) is
begin
```

```
if rising_edge(clk) then
    if rst = '1' then
      0 <= (others => '0');
    else
      0 <= std logic vector(INTO);</pre>
    end if;
  end if;
end process output regs;
-- pipline 1 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline 1: process (clk) is
begin
 if rising_edge(clk) then
   if rst = '1' then
    INT3 pipeline 1 <= (others => '0');
    INT5 pipeline 1 <= (others => '0');
    INTD pipeline 1 <= to unsigned(1,INTD'length); -- type conversion</pre>
notation
    else
    INT3 pipeline 1 <= INT3;</pre>
    INT5 pipeline 1 <= INT5 pipeline 3;</pre>
    INTD pipeline 1 <= INTD pipeline 3;</pre>
    end if:
  end if;
end process pipeline 1;
-- pipeline 2
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline 2: process (clk) is
begin
  if rising edge(clk) then
    if rst = '1' then
    INT4 pipeline 2 <= (others => '0');
    INT5 pipeline 2 <= (others => '0');
    else
    INT4 pipeline 2 <= INT4;</pre>
    INT5 pipeline 2 <= INT5 pipeline 1;</pre>
    end if;
  end if;
end process pipeline_2;
-- pipeline 3
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
```

```
pipeline 3: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT1_pipeline_3 <= (others => '0');
    INT2_pipeline_3 <= (others => '0');
    INT5_pipeline_3 <= (others => '0');
INTD_pipeline_3 <= to_unsigned(1,INTD'length); -- type conversion</pre>
notation
    else
    INT1 pipeline 3 <= INT1;</pre>
    INT2_pipeline_3 <= INT2;</pre>
    INT5_pipeline_3 <= INT5;</pre>
    INTD_pipeline_3 <= INTD;</pre>
    end if;
  end if;
end process pipeline 3;
end Behavioral;
```

# Lab 3 Task 2

### 2.2.1

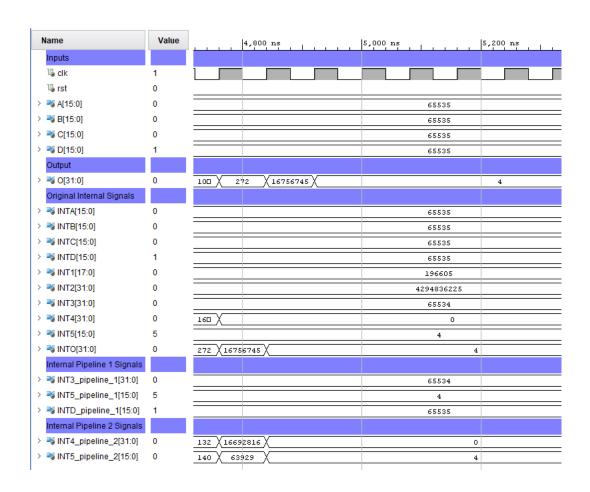
Name	Value	0 ns	100 ns	200 ns	300 ns	400 ns	500 ns	600 ns	700 ns	800 ns    900
Inputs										
ଧ୍ଜ clk	0									
₩ rst	0									
> 🔏 A[15:0]	88			U			X	0	67	53264 / 1
> 🥞 B[15:0]	65432			U			X	0	151	32 / 1
> 🥞 C[15:0]	63113			U			X	0	X 4	5 (61
> 🥞 D[15:0]	54			U			X	1		65535
Output										
> <b>%</b> O[31:0]	0	υX			х			<u> </u>		0
Original Internal Signals										
> NTA[15:0]	37			τ	,			0	χ	57 🗶 53264
> 🔧 INTB[15:0]	61664			τ	,			0	) 1	51 X 32
> NTC[15:0]	86			τ	,			0		4 / 5
> 🔏 INTD[15:0]	62309			τ	r			( <del></del>	1	65535
> 🥞 INT1[17:0]	111			>				0	X 2	01   159792
> 考 INT2[31:0]	5303104			)				0	χ 6	04 / 160
> 🔧 INT3[31:0]	5303215	$\overline{}$		>				0	X 8	05   159952
> 🔧 INT4[31:0]	0						0			
> 🔧 INT5[15:0]	91	$\overline{}$		>				5	Х	9 / 10
> NTO[31:0]	0			>						0
Internal Pipeline 1 Signals										
> NT3_pipeline_1[31:0]	0	U			х			<u> </u>	0	805
> 考 INT5_pipeline_1[15:0]	5	U X			х			· X	5	Д 9
> 3 INTD_pipeline_1[15:0]	38			τ					1	
Internal Pipeline 2 Signals										
> 3 INT4_pipeline_2[31:0]	0	U (						0		
> 3 INT5_pipeline_2[15:0]	0			τ	,					0

Name	Value	
Inputs		
ଧି₀ dk	1	
V₀ rst	0	
> 🥞 A[15:0]	0	67 53264 149 21 0 37 88 69 64506 64586
> 🔧 B[15:0]	0	151 32 19 49 62819 61664 65432 65004 9
> N C[15:0]	0	4
> 🥞 D[15:0]	1	1 65535 10 65332 38 62309 54 65350 1 61845
Output		
> <b>3</b> O[31:0]	0	0
Original Internal Signals		
> 🥞 INTA[15:0]	0	67 \ 53264 \ 149 \ 21 \ \ 0 \ \ 37 \ 88 \ \ 69 \ \ 64506 \ \ 64
> 喝 INTB[15:0]	0	151
> = INTC[15:0]	0	4
> 喝 INTD[15:0]	1	1 (65535 ) 10 (65332 ) 38 (62309 ) 54 (65350 ) 1 (61
> 🥞 INT1[17:0]	0	201
> 喝 INT2[31:0]	0	604
> 喝 INT3[31:0]	0	805
> 🖥 INT4[31:0]	0	0
> 🔧 INT5[15:0]	5	9
> 🥞 INTO[31:0]	0	0
Internal Pipeline 1 Signals		
> <b>3</b> INT3_pipeline_1[31:0]	0	0
> 🥞 INT5_pipeline_1[15:0]	5	5
> 3 INTD_pipeline_1[15:0]	1	1
Internal Pipeline 2 Signals		
> <b>%</b> INT4_pipeline_2[31:0]	0	0
> 3 INT5_pipeline_2[15:0]	0	

Name	Value	
Inputs		
<b>¼</b> clk	1	
¼ rst	0	
> 🔧 A[15:0]	0	6D X 64586 X 63945 X 62385 X 63919 X 65349 X 64467 X 65535
> 🥞 B[15:0]	0	9
> N C[15:0]	0	5
> N D[15:0]	1	1 (61845 ) 10 (35 ) 18 (64255 ) 244 ( 65535
Output		
> <b>3</b> O[31:0]	0	0
Original Internal Signals		
> 🔧 INTA[15:0]	0	64506 X 64586 X 63945 X 62385 X 63919 X 65349 X 64467 X 65535
> 考 INTB[15:0]	0	9 X 308 X 49 X 64474 X 61664 X 63714 X 65535
> = INTC[15:0]	0	5
> 🖥 INTD[15:0]	1	1
> 🥞 INT1[17:0]	0	193518 X 193758 X 191835 X 187155 X 191757 X 196047 X 193401 X 196605
> 🔧 INT2[31:0]	0	45 X 19083988 X 3022320 X 0 X 8324640 X 4072853736 X 4294836225
> 🔧 INT3[31:0]	0	193563 X 193803 X 19275823 X 3209475 X 191757 X 8520687 X4073047137 X 65534
> 🥞 INT4[31:0]	0	0
> 🔧 INT5[15:0]	5	10
> <b>¾</b> INTO[31:0]	0	0
Internal Pipeline 1 Signals		
> 3 INT3_pipeline_1[31:0]	0	41969830 X 193563 X 193803 X 19275823 X 3209475 X 191757 X 6520687 X4073047137  65534
> <b>%</b> INT5_pipeline_1[15:0]	5	64570 \ 10 \ \ 61966 \ \ 61685 \ 5 \ \ 140 \ \ 63929 \ 4
> 3 INTD_pipeline_1[15:0]	1	65350 X 1 X 61845 X 10 X 35 X 18 X 64255 X 244 X 65535
Internal Pipeline 2 Signals		
> 3 INT4_pipeline_2[31:0]	0	0
> 🥞 INT5_pipeline_2[15:0]	0	0

Name	Value	Ι.		3,400	ns		3,50	0 ns	ı	3,600 1	is	3,7	00 ns	[3,	800 ns		3,900	ns	4,	000 ns		4,100
Inputs												Т										
ଧ₀ clk	1		1		1					Г												
¹ೌ rst	0																					
> N A[15:0]	0											63	5535									
> 🥞 B[15:0]	0											63	5535									
> 🥞 C[15:0]	0											63	5535									
> 🖥 D[15:0]	1											63	5535									
Output																						
> <b>™</b> O[31:0]	0			0	)			Х		5		$\top X$	814	X	12	$\overline{\chi}$	179736	: X	61731	$\overline{}$	5	χ_
Original Internal Signals																						
> 🐴 INTA[15:0]	0											63	5535									
> 💐 INTB[15:0]	0											63	5535									
> 3 INTC[15:0]	0											63	5535									
> 🐴 INTD[15:0]	1											63	5535									
> 🔏 INT1[17:0]	0											19	6605									
> 🥞 INT2[31:0]	0											4294	836225									
> 🥞 INT3[31:0]	0											63	5534									
> 🥞 INT4[31:0]	0			0	)			=X	80	5 X	2	$\equiv X$	117770	=X $=$	46	=X	0	$\supset X$	85	7	647426	• X 🗖
> 🔏 INT5[15:0]	5												4									
> 🔏 INTO[31:0]	0			0		$X\Box$		5		=X	814		12	=X $=$	179736	•X	61731	$\supset X$	5	=X $=$	176	
Internal Pipeline 1 Signals																						
> 🔏 INT3_pipeline_1[31:0]	0											63	5534									
> 🔏 INT5_pipeline_1[15:0]	5												4									
> <b>3</b> INTD_pipeline_1[15:0]	1											63	5535									
Internal Pipeline 2 Signals																						
> 3 INT4_pipeline_2[31:0]	0					0				X	805	$\Box$ X	2		117770	-X	46		0	X	85	Χo
> 3 INT5_pipeline_2[15:0]	0			0		$X_{\square}$		5		X	9	$\Rightarrow$ X	10	=	61966	=X	61685		5	X	91	×ο

Name	Value		4,100 n	s	4,200 n	s	4,300	ns	4,400	ns	4,50	ns.	4,6	00 ns		4,700	ns .	4,80	00 ns
Inputs																			
¹⊌ clk	1																		
₩ rst	0																		
> 🥞 A[15:0]	0									65535									
> 🥞 B[15:0]	0									65535									
> NG C[15:0]	0									65535									
> 🤏 D[15:0]	1									65535									
Output																			
> N O[31:0]	0	5	X	L76	765373	378 X	128793	19	3573	13	$\Box$ X	1989548	\1	.53384	X	10658	$\supset$	272	X 10
Original Internal Signals																			
> 🖥 INTA[15:0]	0									65535									
> 🥞 INTB[15:0]	0									65535									
> 3 INTC[15:0]	0									65535									
> 🥞 INTD[15:0]	1									65535									
> 🥞 INT1[17:0]	0									196605									
> 🥞 INT2[31:0]	0									12948362	25								
> 🥞 INT3[31:0]	0									65534									
> 🥞 INT4[31:0]	0	764740	J 64	1223	19356	33 X	3	192	7582	91699		10653	$\mathbb{X}$	132	X 1	569281	5 X	0	
> 😽 INT5[15:0]	5									4									
> 🥞 INTO[31:0]	0	176	765	37378	12879	3 X	193573		13	198954	18 X	153384	$\mathbb{X}$	10658	$\supset \subset$	272	16	756745	$\propto$
Internal Pipeline 1 Signals																			
> 🥞 INT3_pipeline_1[31:0]	0									65534									
> 考 INT5_pipeline_1[15:0]	5									4									
> NTD_pipeline_1[15:0]	1									65535									
Internal Pipeline 2 Signals																			
> 3 INT4_pipeline_2[31:0]	0	85	764	74260	6422	з Х	193563	X	3	192758	32 X	91699	$\mathbb{X}^{-}$	10653	$\supset \subset$	132	16	592816	X
> 🥞 INT5_pipeline_2[15:0]	0	91	X 63	3118	6457	•X		10		61966	$\Box$ X	61685	$\mathbb{X}$	5	X	140	X 6	3929	$\mathcal{X}$

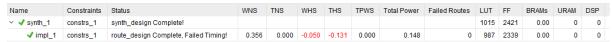


```
run 5 us
Error:
test_vectors value 0
for inputs
A: 67
B: 151
C: 4
D: 1
for outputs
Actual value
0: 814
Predicted value
0: 814
Time: 3760 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 1
for inputs
A: 53264
B: 32
C: 5
D: 65535
for outputs
Actual value
0: 12
Predicted value
0: 12
Time: 3840 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 2
for inputs
A: 149
B: 19
C: 61961
D: 10
for outputs
Actual value
O: 179736
Predicted value
0: 179736
Time: 3920 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3
for inputs
A: 21
B: 49
C: 61680
D: 65332
for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 4 us Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 4
for inputs
A: 0
B: 62819
C: 0
D: 38
for outputs
Actual value
0: 5
Predicted value
0: 5
Time: 4080 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 5
for inputs
A: 37
B: 61664
C: 86
D: 62309
for outputs
Actual value
O: 176
Predicted value
0: 176
Time: 4160 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 6
for inputs
A: 88
B: 65432
C: 63113
D: 54
for outputs
Actual value
O: 76537378
Predicted value
O: 76537378
Time: 4240 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 7
for inputs
A: 69
B: 65004
C: 64565
D: 65350
for outputs
Actual value
0: 128793
Predicted value
0: 128793
```

```
Time: 4320 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 8
for inputs
A: 64506
B: 9
C: 5
D: 1
for outputs
Actual value
0: 193573
Predicted value
0: 193573
Time: 4400 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 9
for inputs
A: 64586
B: 9
C: 5
D: 61845
for outputs
Actual value
0: 13
Predicted value
Time: 4480 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 10
for inputs
A: 63945
B: 308
C: 61961
D: 10
for outputs
Actual value
O: 1989548
Predicted value
O: 1989548
Time: 4560 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 11
for inputs
A: 62385
B: 49
C: 61680
D: 35
for outputs
Actual value
0: 153384
Predicted value
0: 153384
```

```
Time: 4640 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 12
for inputs
A: 63919
B: 64474
C: 0
D: 18
for outputs
Actual value
O: 10658
Predicted value
O: 10658
Time: 4720 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 13
for inputs
A: 65349
B: 61664
C: 135
D: 64255
for outputs
Actual value
0: 272
Predicted value
O: 272
Time: 4800 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 14
for inputs
A: 64467
B: 63714
C: 63924
D: 244
for outputs
Actual value
O: 16756745
Predicted value
0: 16756745
Time: 4880 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 15
for inputs
A: 65535
B: 65535
C: 65535
D: 65535
for outputs
Actual value
O: 4
Predicted value
O: 4
Time: 4960 ns
```



create\_clock -period 15.000 -name clk -waveform {0.000 7.5000} [get\_ports clk]

### 2.2.3

A setup violation occurs when the circuit cannot meet the setup criteria specified by the designer, in this case the setup violations that occurred from testing were the clock period being defined as above. When the circuit could not meet the specified clock period a violation occurs.

No.   No.	Name	Value	0 ns	200 ns		400 ns	600	ns .	800 ns	1,000
15 ct   15 c	Inputs			1 1 1 1 1 1		111111111111111111111111111111111111111		<del></del>	1 1 1 1 1	
94 MINGS    0555    0   0   0   0   0   0   0		0								
9 49 (150   650   650   7										
9   9   9   9   9   9   9   9   9   9	> ■ A[15:0]	65535			U			• X	67 \$ 53264 \$	149 ( 21 )
9 4 (1916)   9000   9   1   1   1   1   1   1   1   1   1		65535								
2 - 00 0010	> ■ C[15:0]	65535						=====		
Second columns of co	> 🥞 D[15:0]	65535	U		U			1	65535	10 ( 65332 )
December   Property   Company   Co	Output									
WATTISTON   COUNTY   COUNTY	> <b>™</b> O[31:0]	4	U /		х		X		0	
94 HTT[166]	Original Internal Signals									
WATTICTION   CONTINUE   CONTINU	> 3 INTA[15:0]	65535			υ		X	0	X 67 X 5326	149 21
WHITE  SS    SS	> 🥞 INTB[15:0]	65535			υ			0	X 151 X 32	19 49
West	> 3 INTC[15:0]	65535			υ			0	X 4 X 5	61961 (610
West   March   Water   Water	> 🥞 INTD[15:0]	65535			U			1	6553	10 650
3	> 🥞 INT1[17:0]	196605			X			0	201   15979	2 447 63
West   Composition	> 🥞 INT2[31:0]	42948362			х			0	X 604 X 160	1177259 300
2	> 🥞 INT3[31:0]	65534			х			0	805	159952 110
West   Washed   Was	> 3 INT4[31:0]	0					0			
Western   Properties   Chipseles   Chips	> 🥞 INT5[15:0]	4			X			5	9 10	61966 610
West		4			Х		X		0	
West										
Wastern   Depote   1500   15			U		Х		X_		0	
							X_	0	X 5	
2		65535			U		X		1	X 650
Warring perime, 215-01   A										
	> 3 INT4_pipeline_2[31:0]		n X				0			
2		4			υ		X		0	
2										
Name			===						X 201	===
Name			U X				<u> </u>	0	X 604	===
Name							——⊱			
Injus   Inju	> - IN15_pipeline_3[15:0]	4	U X		Х			<u>•X</u>	5 X 9	X 10 ( e10
Injus   Inju										
1	Name	Value	1,000 n	s  1,100 n	s 1,200 r	ıs  1,300 ns	1,400 ns	1,500 ns	1,600 ns	1,700 ns 1
14										
3										
> \$ B[15:0]	¼ rst	0								
3	> N A[15:0]	149	DX 21 X	• X	37 88	X 69 X	64506 X 6	4586 (639	62385	63919 6534
Section   Sect	> ■ B[15:0]	19	□X 49 X	62819 (6	1664 6543	65004	9	Х 30	)8 X 49 X	64474 X 6166
Output	> N C[15:0]	61961	□X 61680 X	• X	86 6311	.3 (64565	5	X 619	61680 X	0 135
3   0    0   0   0   0   0   0   0   0	> ■ D[15:0]	10	□X 65332 X	38 X 6	2309 🗶 54	65350	1 X e	1845 1	0 35 X	18 6425
Diginal Internal Signals   Diginal Internal Signals	Output									
3   NTA 150    53264   149   21   0   37   88   69   64506   64586   63945   62385   63919	> N O[31:0]	0								
1	Original Internal Signals								0	
> \$\ \text{intT(15:0]} \ 5 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	NINTAGE € 01								0	
NITD_15:0	[U:crjAtvii 🗗 🗎	53264	149 21	X 0	X 37 X	88 X 69	64506	X 64586		15 X 63919 X
159792   447   63   0   111   264   207   193518   193758   191835   187155   191757				===				$\sim$	63945 X 6231	
Note	> <b>考</b> INTB[15:0]	32	19 49	62819	X 61664 X	65432 6500	04	9	63945 X 6231	64474
Sintal   S	> <b>¾</b> INTB[15:0] > <b>¾</b> INTC[15:0]	32 5	19 49 61961 61680	X 62819	X 61664 X 86	65432 X 6500 63113 X 6456	65	9 5	63945	X 64474 X
NT4[31:0]   0   0   0   0   0   0   0   0   0	> ■ INTB[15:0] > ■ INTC[15:0] > ■ INTC[15:0]	32 5 65535	19 49 61961 61680 10 65332	0 0 0 2 38	X 61664 X X 86 X X 62309 X	65432 X 6500 63113 X 6456 54 X 6533	04 65 50 1	9 5 X 61845	63945	X 64474 30 X 0 X 18
NT4[31:0]   0   0   0   0   0   0   0   0   0	> ■ INTB[15:0] > ■ INTC[15:0] > ■ INTC[15:0] > ■ INTD[15:0] > ■ INT1[17:0]	32 5 65535 159792	19 49 61961 61680 10 65332 447 63	X 62819 0 X 0 2 X 38 X 0	X 61664 X X 86 X X 62309 X X 111 X	65432 X 6500 63113 X 6450 54 X 6533 264 X 20	04 65 50 1 7 193518	9 5 X 61845 X 193758	63945	X 64474 X 0 X 18 X 191757 X
Signature   Signate   Si	> № INTB[15:0] > № INTC[15:0] > № INTC[15:0] > № INTD[15:0] > № INT1[17:0] > № INT2[31:0]	32 5 65535 159792 160	19 49 61961 61680 10 65333 447 63 11770 302233	X 62819 0 X 0 2 X 38 X 0 20 X 0	86 X 62309 X 111 X 5303104 X	65432 \ 6500 63113 \ 6450 54 \ 6531 264 \ 20' 4129609816 \ 419698	04 65 50 1 7 193518	9 5 X 61845 X 193758 45	63945	64474 00 0 0 18 0 55 191757 020 0
NTO[31:0]   0   0   0   0   0   0   0   0   0	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INT1[17:0] > % INT2[31:0] > % INT3[31:0]	32 5 65535 159792 160 805	19 49 61961 61680 10 65333 447 63 11770 302233	X 62819 0 X 0 2 X 38 X 0 20 X 0	86 X 62309 X 111 X 5303104 X	65432 \ 6500 63113 \ 6450 54 \ 6531 264 \ 20' 4129609816 \ 419698	04 65 50 1 7 193518	9 5 X 61845 X 193758 45	63945	64474 00 0 0 18 0 55 191757 020 0
Internal Pipeline 1 Signals	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INT1[17:0] > % INT2[31:0] > % INT3[31:0] > % INT4[31:0]	32 5 65535 159792 160 805 0	19 49 61961 61680 10 65333 447 63 11770 302233 159952 117770	X 62819 0	61664 86 62309 111 5303104 0	65432 \ 6500 63113 \ 6450 54 \ 6531 264 \ 20' 4129609816 \ 419698 5303215 \ \ 412961	04	9 5	63945	64474 00 0 18 55 191757 020 0 823 3209475
> ★ INT3_pipeline_1[31:0]       0       805	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INT1[17:0] > % INT2[31:0] > % INT3[31:0] > % INT4[31:0] > % INT4[31:0] > % INT5[15:0]	32 5 65535 159792 160 805 0	19 49 61961 61680 10 65333 447 63 11770 302233 159952 117770	X 62819 0	61664 86 62309 111 5303104 0	65432 \ 6500 63113 \ 6450 54 \ 6531 264 \ 20' 4129609816 \ 419698 5303215 \ \ 412961	04	9 5	63945	64474 00 0 18 55 191757 020 0 823 3209475
> ★ INT5_pipeline_1[15:0]       5       9       10       61966       61685       5       91       63118       64570       10       61966         > ★ INTD_pipeline_1[15:0]       1       65535       10       65332       38       62309       54       65350       1       61845       10         Internal Pipeline 2 Signals       INT4_pipeline_2[31:0]       0       0       0       0       0       0       0       Internal Pipeline 3 Signals       INT1_pipeline_3[17:0]       201       159792       447       63       0       111       264       207       193518       193758       191835       187155 </td <td>&gt; % INTE(15:0) &gt; % INTC(15:0) &gt; % INTC(15:0) &gt; % INT1(17:0) &gt; % INT2(31:0) &gt; % INT3(31:0) &gt; % INT4(31:0) &gt; % INT5(15:0) &gt; % INT5(15:0) &gt; % INT0(31:0)</td> <td>32 5 65535 159792 160 805 0 10</td> <td>19 49 61961 61680 10 65333 447 63 11770 302233 159952 117770</td> <td>X 62819 0</td> <td>61664 86 62309 111 5303104 0</td> <td>65432 \ 6500 63113 \ 6450 54 \ 6531 264 \ 20' 4129609816 \ 419698 5303215 \ \ 412961</td> <td>04</td> <td>9 5</td> <td>63945</td> <td>64474 00 0 18 55 191757 020 0 823 3209475</td>	> % INTE(15:0) > % INTC(15:0) > % INTC(15:0) > % INT1(17:0) > % INT2(31:0) > % INT3(31:0) > % INT4(31:0) > % INT5(15:0) > % INT5(15:0) > % INT0(31:0)	32 5 65535 159792 160 805 0 10	19 49 61961 61680 10 65333 447 63 11770 302233 159952 117770	X 62819 0	61664 86 62309 111 5303104 0	65432 \ 6500 63113 \ 6450 54 \ 6531 264 \ 20' 4129609816 \ 419698 5303215 \ \ 412961	04	9 5	63945	64474 00 0 18 55 191757 020 0 823 3209475
> % INTD_pipeline_1[15:0] 1 1 65535 10 65332 38 62309 54 65350 1 61845 10     Internal Pipeline_2 Signals	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INT1[17:0] > % INT2[31:0] > % INT3[31:0] > % INT4[31:0] > % INT5[15:0] > % INT5[15:0]   mintal Pipeline 1 Signals	32 5 65535 159792 160 805 0 10 0	19 49 61961 61680 10 65332 447 63 11770 302232 159982 117770 61966 61680	\( \begin{array}{c} 62819 \\ 0 \\ 0 \\ 2 \\ 38 \\ \ 0 \\ 20 \\ \ 0 \\ \ \ \ \ \ \ \ \	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \)	65432	04	9	63945	X 64474 X 100 X 0 X 18 X 191757 X 120 X 0 X 1823 X 3209475 X 15 X 5
Internal Pipeline 2 Signals	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT2[31:0] > % INT3[31:0] > % INT4[31:0] > % INT5[15:0] > % INT0[31:0] internal Pipeline 1 Signals > % INT3_pipeline_1[31:0]	32 5 65535 159792 160 805 0 10 0	19 49 61961 61680 10 65932 447 63 11770 302232 159952 117770 61966 61680	62819 0	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \) 3022383 \( \)	65432	04	9	63945	X 64474 X 100 X 0 X 18 X 191757 X 120 X 0 X 1823 X 3209475 X 19275823 X 19275
> % INT4_pipeline_2[31:0] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	> ≈ INTB[15:0] > ≈ INTC[15:0] > ≈ INTC[15:0] > ≈ INT[17:0] > ≈ INT[17:0] > ≈ INT[231:0] > ≈ INT[231:0] > ≈ INT[31:0]	32 5 65535 159792 160 805 0 10 0	19 49 61961 61680 10 6593; 447 63 11770 30223; 159952 117770 61966 61680	62819 0	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \) 91 \( \) 3022383 \( \) 61685 \( \)	65432	004	9	63945	X 64474 X 190 X 0 X 18 X 191757 X 120 X 0 X 19275823 X 19275823 X 61966 X 19266 X 19266 X 19266 X 19266 X 19266 X 19266 X 1926823 X 1926
> \$\ \text{INT5_pipeline_2[15:0]} \ 0 \ 0 \ 0 \ 0 \ \ \text{Internal Pipeline_3 Signals} \ \text{> \$\ \text{INT1_pipeline_3[17:0]}} \ 201 \ \ \text{159792} \ \ \ 447 \ \ 63 \ \ 0 \ \ \ \ 111 \ \ 264 \ \ 207 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INT[17:0] > % INT2[31:0] > % INT3[31:0] > % INT5[31:0] > % INT5[31:0] > % INT5[31:0]	32 5 65535 159792 160 805 0 10 0 5	19 49 61961 61680 10 6593; 447 63 11770 30223; 159952 117770 61966 61680	62819 0	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \) 91 \( \) 3022383 \( \) 61685 \( \)	65432	004	9	63945	X 64474 X 190 X 0 X 18 X 191757 X 120 X 0 X 19275823 X 19275823 X 61966 X 19266 X 19266 X 19266 X 19266 X 19266 X 19266 X 1926823 X 1926
Internal Pipeline 3 Signals	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT2[31:0] > % INT3[31:0] > % INT4[31:0] > % INT5[51:0] > % INT5[31:0]   mitmal Pipeline 1 Signals > % INT3_pipeline_1[31:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_1[15:0]   mitmal Pipeline 2 Signals	32 5 65535 159792 160 805 0 10 0 5 1	19 49 61961 61680 10 6593; 447 63 11770 30223; 159952 117770 61966 61680	62819 0	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \) 91 \( \) 3022383 \( \) 61685 \( \)	65432	004	9	63945	X 64474 X 190 X 0 X 18 X 191757 X 120 X 0 X 19275823 X 19275823 X 61966 X 19266 X 19266 X 19266 X 19266 X 19266 X 19266 X 1926823 X 1926
> % INT1_pipeline_3[17:0]       201       159792       447       63       0       111       264       207       193518       193758       191835       187155         > % INT2_pipeline_3[31:0]       604       160       1177259       3022320       0       5303104       4129609816       4196983260       45       19083988       3022320       0         > % INTD_pipeline_3[15:0]       1       65535       10       65532       38       62309       54       65350       1       61845       10       35	> % INTB[15:0] > % INTD[15:0] > % INTC[15:0] > % INTD[15:0] > % INT1[17:0] > % INT3[31:0] > % INT3[31:0] > % INT5[15:0] > % INT5[15:0] > % INT5[15:0] > % INTD[31:0] Internal Pipeline 1 Signals > % INT5_pipeline_1[31:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_2[31:0]  Internal Pipeline 2 Signals > % INT4_pipeline_2[31:0]	32 5 65535 159792 160 805 0 10 0 5 1	19 49 61961 61680 10 6593; 447 63 11770 30223; 159952 117770 61966 61680	62819 0	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \) 91 \( \) 3022383 \( \) 61685 \( \)	65432	004	9	63345	X 64474 X 190 X 0 X 18 X 191757 X 120 X 0 X 19275823 X 19275823 X 61966 X 19266 X 19266 X 19266 X 19266 X 19266 X 19266 X 1926823 X 1926
> % INT2_pipeline_3[31:0] 604 160 1177259 X 5022320 X 0 X 5303104 X4129609816 X4196983260 X 45 X 19083988 X 3022320 X	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT1[17:0] > % INT2[31:0] > % INT3[31:0] > % INT5[15:0] > % INT5[15:0] > % INT5[15:0] > % INT5_pipeline_1[31:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_1[15:0] > % INT5_pipeline_2[31:0]	32 5 65535 159792 160 805 0 0 5 1 1 0 5	19 49 61961 61680 10 6593; 447 63 11770 30223; 159952 117770 61966 61680	62819 0	\( \) 61664 \( \) 86 \( \) 86 \( \) 62309 \( \) 1111 \( \) 5303104 \( \) 0 \( \) 91 \( \) 91 \( \) 3022383 \( \) 61685 \( \)	65432	004	9	63345	X 64474 X 190 X 0 X 18 X 191757 X 120 X 0 X 19275823 X 19275823 X 61966 X 19266 X 19266 X 19266 X 19266 X 19266 X 19266 X 1926823 X 1926
> % INTD_pipeline_3[15:0] 1 65535 10 (65332 ) 38 (62309 ) 54 (65350 ) 1 (61645 ) 10 (35 )	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT1[17:0] > % INT3[31:0] > % INT5[31:0] > % INT5[15:0] > % INT5[31:0] > % INT5[31:0] > % INT5[31:0]  internal Pipeline 1 Signals > % INT5_pipeline_1[15:0] > % INT5_pipeline_1[15:0]  internal Pipeline 2 Signals > % INT5_pipeline_2[31:0] > % INT5_pipeline_2[31:0] > % INT5_pipeline_2[31:0] > % INT5_pipeline_3[15:0] internal Pipeline 3 Signals	32 5 65535 159792 160 805 0 10 0 5 1 1	19 49 61961 61686 10 6533; 447 63 11770 30223; 159952 117770 61966 6168; 805 15995 9 10 1 6553;	\$\begin{array}{c} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	\$\begin{align*} 61664 \\ 86	65432	04	9	63345	\( \begin{array}{c} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT1[17:0] > % INT3[31:0] > % INT4[31:0] > % INT5[15:0]   internal Pipeline 1 Signals > % INT5_pipeline_1[31:0] > % INT5_pipeline_1[45:0]   internal Pipeline 2 Signals > % INT5_pipeline_2[31:0]   internal Pipeline 2 Signals > % INT5_pipeline_2[31:0]   internal Pipeline 3 Signals > % INT5_pipeline_3[7:0]   internal Pipeline 3 Signals > % INT1_pipeline_3[7:0]	32 5 65535 159792 160 805 0 10 0 5 1 1 0 0 5 1	19 49 61961 61680 10 6533; 447 63 11770 30223; 159952 117770 61966 61680 805 15995 9 10 1 6553;	\$\begin{array}{c} 62819 &  0 &  0 &  0 &  2 &  38 &  0 &  20 &  0 &  0 &  222383 &  5 &  5 &  5 &  5 &  61966 &  5 &  10 &    63 &     63 &   \tex	\$\begin{align*} \left\{ 61664 \\ \\ 86 \\ \\ 62309 \\ \\ 111 \\ \\ 5303104 \\ \\ \\ 91 \\ \\ 3022383 \\ \\ 61685 \\ \\ 65332 \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	65432	04	9	63345	\( \begin{array}{c} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
7 % INID_DIDENINE_S[75:U] 9 10 X 61966 X 61685 X \$ X 91 X 63118 X 64570 X 10 X 61966 X 61685 X	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT1[17:0] > % INT3[31:0] > % INT4[31:0] > % INT5[15:0]  internal Pipeline 1 Signals > % INT5_pipeline_1[31:0] > % INT5_pipeline_1[15:0]  internal Pipeline 2 Signals > % INT5_pipeline_2[31:0]  internal Pipeline 3 Signals > % INT5_pipeline_2[15:0]  internal Pipeline 3 Signals > % INT1_pipeline_3[31:0] > % INT1_pipeline_3[31:0] > % INT2_pipeline_3[31:0]	32 5 65535 159792 160 805 0 10 0 5 1 0 5 1	19 49 61961 61680 10 6533; 447 63 11770 30223; 159982 117770 61966 6168; 808 15998 9 10 1 6583; 159792 447 160 11772;	\$\begin{array}{c} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	\( \begin{align*}     ali	65432	04	9	63945	X 64474 X 100 X 0 0 X 18
	> % INTB[15:0] > % INTC[15:0] > % INTC[15:0] > % INTD[15:0] > % INT1[17:0] > % INT3[31:0] > % INT5[15:0] > % INT5[15:0]	32 5 65535 159792 160 805 0 10 0 5 1 0 0 5 1 1 0 0 201 604 1	19 49 61961 61690 10 6533; 447 63 11770 30223; 159952 117770 61966 6168;  805 15995 9 10 1 65531 159792 447 160 11772 65535 10	\$\begin{array}{c} 62819 \\ 0 & 0 & 0 \\ 2 & 38 & \\ 0 & 0 & 0 \\ 20 & 0 & 0 \\ 06 & \$3022383 \\ 5 & \$107706 \\ 5 & \$10 \\ \end{array}\$\$\$ \$\$ 63 \\ 59 & \$3022320 \\ 65332 \\ 65332	\( \begin{align*}     ali	65432	04	9	63945	X 64474 X 100 X 0 0 X 18

lame	Value										ns	2,100					444	ns	تالبيب	400
Inputs																				
¼ clk	0				-													_	_	
l₀ rst	0																			
₹ A[15:0]	149	□X	63919	_X_	65349	_X_,	54467	_X					655	35						
<b>■</b> B[15:0]	19	□X	64474	_X_	61664	X(	53714	_X					655	35						
<b>™</b> C[15:0]	61961		0	$\perp$ X $\perp$	135	_X_,	53924	_X_					655	35						
<b>™</b> D[15:0]	10		18	$\supset \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$	64255	X	244	$\square X$					655	35						
Output																				
₹ O[31:0]	0										0									
Original Internal Signals																				
■ INTA[15:0]	53264	6238	5 X	63919	X	65349	$\supset$	64467	χ					65535	5					
₹ INTB[15:0]	32	49	$\exists x \equiv$	64474	$=$ $\!$	61664	$\overline{\chi}$	63714	X					65535	5					
■ INTC[15:0]	5	6168	ōχ	0	_X_	135	$\neg \chi^-$	63924	$\chi$					65535	5					
₹ INTD[15:0]	65535	35	$\Box$ X $\Box$	18		64255	=	244	X					65535	5					
<b>™</b> INT1[17:0]	159792	18715	55 X	191757	=	196047	= =	193401	X ==					19660	5					
■ INT2[31:0]	160	30223	20 X	0	=/=	324640	X40	7285373	εX				42:	4836	225					
■ INT3[31:0]	805	19275	==	20947	=	191757	=	520687	X40730	47137	x				65534					
■ INT4[31:0]	0				=															
■ INT5[15:0]	10	6168	5 Y	5	$\neg$	140	$\overline{}$	63929	<u>ү</u>					4						
■ INTO[31:0]	0	2200			$\dashv$		_^_				0	+		É		_			-	
Internal Pipeline 1 Signals																				
™ INT3_pipeline_1[31:0]	0	1000	. V -	00000	. V .	2200455	~	191757	X 8520	607	Vannosis	125V				6555	4			
	5	19380	=	927582	ٿا	209475	⇌	191757	==	=	X4073047	==				6553	4			
■ INT5_pipeline_1[15:0]		10	=	61966	=(}=	61685	={}=	5	X 14	=	X 63925	<u>'</u>				4				
NTD_pipeline_1[15:0]	1	6184	5_X	10	_ř_	35	_X_	18	X 642	55	X 244	X_				6553	5			
Internal Pipeline 2 Signals																				
¾ INT4_pipeline_2[31:0]	0										0									
NT5_pipeline_2[15:0]	0										0									
Internal Pipeline 3 Signals																				
NT1_pipeline_3[17:0]	201	19183	35 X	187155		191757	$\supset \subset$	196047	193	401	X				196608	5				
INT2_pipeline_3[31:0]	604	19083	30 X 3	022320	- X	0	-V :	324640	V40720	53736	X			4:	2948362	225				
						_	_/_	324640	V40.50											
NTD_pipeline_3[15:0]	1	10		35		18	=	64255	X 24	=	$\equiv$				65535					
INT5_pipeline_3[15:0]	1 9 Value	10 6196	6 X	35 61685	500 ns	18	=	64255 140	₹=	29	3,80	) ns	3,900	ns	4	,000	ns	4	,100 n	ıs
int5_pipeline_3[15:0]	9 Value		6 X	35 61685		18		64255 140	X 24	29	3,800	) ns	3,900	ns	4		ns	4	,100 n	15
INT5_pipeline_3[15:0]  Name  Inputs  Li clk	Value		5 X	35 61685		18		64255 140	X 24	29	3,80	ns	3,900	ns	4		ns	4	,100 n	is .
INT5_pipeline_3[15:0]  Name Inputs  G clk  F rst	Value 0 0		6 X	35 61685		18		64255 140	X 24	29		) ns	3,900	ns	4		ns	4	,100 n	15
NNT5_pipeline_3[15:0]  Name  Inputs  1è clk  1è rst	9 <b>Value</b> 0 0 149		ξ 6 X	35 61685		18		64255 140	X 24	29	65535	) ns	3,900	ns	4		ns	4	,100 n	15
NT5_pipeline_3[15:0]  Name  Inputs  1a clk  1a rst  34 [15:0]  36 B[15:0]	9 <b>Value</b> 0 0 149 19		6 X	35 61685		18		64255 140	X 24	29	65535 65535	) ns	3,900	ns	4		ns	4	,100 n	ıs I
Name Inputs  lip clk  lip rst  4 [15:0]  5 [15:0]  6 [15:0]	9 <b>Value</b> 0 0 149 19 61961		6 X	35 61685		18		64255 140	X 24	29	6\$535 6\$535	) ns	3,900	ns	4		ns	4	,100 n	ns I
INT5_pipeline_3[15:0]   Iame	9 <b>Value</b> 0 0 149 19		ξ 6 X	35 61685		18		64255 140	X 24	29	65535 65535	) ns	3,900	ns	4		ns	4	,100 n	ns I
INT5_pipeline_3[15:0]   Name	9 <b>Value</b> 0 0 149 19 61961 10		ξ X	35 61685		18		64255 140	X 24	29	6\$535 6\$535	) ns	3,900	ns	4		ns	4	,100 n	ns
INT5_pipeline_3[15:0]	9 <b>Value</b> 0 0 149 19 61961		6 X	35 61685		18		64255 140	X 24	29	65535 65535 65535	) ns	3,900	ns	4	,000		1731	,100 n	5
INT5_pipeline_3[15:0]     Iame	9 Value 0 0 149 19 61961 10		ξ 6 X	35 61685		18		64255 140	X 24	29	65535 65535 65535			ns	4	,000			,100 n	5
INT5_pipeline_3[15:0]     Iame	9 <b>Value</b> 0 0 149 19 61961 10		6 X	35 61685		18		64255 140	X 24	29	65535 65535 65535			ns	4	,000			,100 n	as 5
INT5_pipeline_3[15:0]     Iame	9 Value 0 0 149 19 61961 10		66 X	35 61685		18		64255 140	X 24	29	65535 65535 65535 65535			ns X	4	,000			,100 n	5
INT5_pipeline_3[15:0]     Iame	9 Value 0 0 149 19 61961 10 0 53264			35 61685		18		64255 140	X 24	29	6\$535 6\$535 6\$535 6\$535			, ns	4	,000			, 100 n	5
INT5_pipeline_3[15:0]	9 Value 0 0 149 19 61961 10 0 53264 32		X	35 61685		18		64255 140	X 24	29	65535 65535 65535 65535 65535 65535			ns	4	,000			, 100 n	5
INT5_pipeline_3[15:0]     Iame	9 Value 0 0 149 19 61961 10 0 53264 32 5		X	35 61685		18		64255 140	X 24	29	65535 65535 65535 65535 65535 65535			ns X	4	,000			,100 n	5
INT5_pipeline_3[15:0]	9 Value 0 0 149 19 61961 10 0 53264 32 5 65535		X	35 61685		18		64255 140	X 24	14 1/29 ns	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535	314		ns X	4	,000			,100 n	5
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792		66 X	35 61685		18		64255 140	X 24	14 1/29 ns	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535	314		ns X	4	,000			,100 n	5
INT5_pipeline_3[15:0]     Imme	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160		66 X	35 61685	)	18		64255 140	X 24 X 639 3,700	14 129 ns	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534	314	12	ns.	4	,000	61	1731	X	5
INT5_pipeline_3[15:0]     Iame     Inputs     Ib clk     Ib rst     A[15:0]     E[15:0]     O[15:0]     O[15:0]     Original Internal Signals     INTA[15:0]     INTB[15:0]     INTD[15:0]     INTD[15:0]     INT1[17:0]     INT2[31:0]     INT3[31:0]     INT4[31:0]     INT4[31:0]     INT4[31:0]     INT4[31:0]     INT4[31:0]     INT4[31:0]     INT4[31:0]     INT4[31:0]     INTA[31:0]     INTA[31:	9  Value  0  149  19  61961  10  0  53264  32  5  65535  159792  160  805		66 X	35 61685	)	18		64255 140	X 24 X 639 3,700	14 1/29 ns	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534	314		ns.	17977	,000	61		X	5
INT5_pipeline_3[15:0]     Imme	9  Value  0  149  19  61961  10  0  53264  32  5  65535  159792  160  805  0  10			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	ns ns 4	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534	2:5	12	X	17973	,000 y	61	85	X 76·	5
INT5_pipeline_3[15:0]     Imme	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10		66 X	35 61685	)	18		64255 140	X 24 X 639 3,700	14 129 ns	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534	314	12	X	17977	,000 y	61	1731	X 76·	5
INT5_pipeline_3[15:0]     Imme	9  Value  0  149  19  61961  10  0  53264  32  5  65535  159792  160  805  0  10  0			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	ns ns 4	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534 11	2:5	12	X	17973	,000 y	61	85	X 76·	5
INT5_pipeline_3[15:0]     Iame	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	ns ns 4	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534	2:5	12	X	17973	,000 y	61	85	X 76·	5
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	ns ns 4	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534 4	2:5	12	X	17973	,000 y	61	85	X 76·	5
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	ns ns 4	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534	2:5	12	X	17973	,000 y	61	85	X 76·	5
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 nns ns 14 2 2 814	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196605 129483622 6\$534 4	7770	12 X 46 17973	X	17973	,000 y	61	85	X 764	5
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 ns.	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 4 11 4 4 6\$534	2 2	12	X	179733	,000 ; , , , , , , , , , , , , , , , , ,	61	85	X 76.	5 5 176 1776 85
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 nns ns 14 2 2 814	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 4 11 4 4 6\$534	7770	12 X 46 17973	X	17973	,000 ; , , , , , , , , , , , , , , , , ,	61	85	X 76.	5
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 ns.	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 4 11 4 4 6\$534	2 2	12 X 46 17973:	X	179733	,000 ; , , , , , , , , , , , , , , , , ,	61	85	X 76.	5 5 176 176 85
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 ns.	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 4 11 4 4 6\$534	2 2	12 X 46 17973:	X	179733	,000 ; , , , , , , , , , , , , , , , , ,	61	85	X 76.	5 5 176 176 85
INT5_pipeline_3[15:0]	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 ns.	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 196005 129483622 6\$534 11 4	2 2 110	12 X 46 17973:	X	179733	,000 ; , , , , , , , , , , , , , , , , ,	61	85	X 76.	5 5 4742 176 85
Name  Inputs  Lock  First  A (15:0)  C(15:0)  C(	9  Value  0 0 149 19 61961 10 0 53264 32 5 65535 159792 160 805 0 10 0 5 1			35 61685	)	18	X X X X X X X X X X X X X X X X X X X	64255 140	X 24 X 639 3,700	14 22 ns.	6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 6\$535 19605 129483622 6\$534 11 4	2 2 110	12 X 46 17973:	X	179733	,000 ; , , , , , , , , , , , , , , , , ,	61	85	X 760	5 5 4742 176

Name	Value	
Inputs		
¹% clk	0	
¹₀ rst	0	
> 🐴 A[15:0]	149	65535
> 🥞 B[15:0]	19	65535
> N C[15:0]	61961	65535
> 🖥 D[15:0]	10	65535
Output		
> <b>3</b> O[31:0]	0	5 176 75537378 128793 193573 13 1989548 153384 10658 272
Original Internal Signals		
> = INTA[15:0]	53264	65535
> 🔻 INTB[15:0]	32	65535
> = INTC[15:0]	5	65535
> 考 INTD[15:0]	65535	65535
> 🖥 INT1[17:0]	159792	196605
> 🔻 INT2[31:0]	160	4294836225
> 🖥 INT3[31:0]	805	65534
> <b>3</b> INT4[31:0]	0	\( \text{76474260} \) \( 64223 \) \( \text{193563} \) \( 3 \) \( \text{1927582} \) \( \text{91699} \) \( \text{10653} \) \( \text{132} \) \( \text{16692816} \) \( 0 \)
> 考 INT5[15:0]	10	4
> = INTO[31:0]	0	\(\) 176 \(\) 76537378 \(\) 128793 \(\) 193573 \(\) 13 \(\) 1989548 \(\) 153384 \(\) 10658 \(\) 272 \(\) 16756745 \(\)
Internal Pipeline 1 Signals		
> 考 INT3_pipeline_1[31:0]	0	65534
> 考 INT5_pipeline_1[15:0]	5	4
> NTD_pipeline_1[15:0]	1	65535
Internal Pipeline 2 Signals		
> 考 INT4_pipeline_2[31:0]	0	85
> <b>3</b> INT5_pipeline_2[15:0]	0	91 63118 64570 10 61966 61685 5 140 63929 X
Internal Pipeline 3 Signals		
> 🔏 INT1_pipeline_3[17:0]	201	196605
> 🔏 INT2_pipeline_3[31:0]	604	4294836225
> 🔏 INTD_pipeline_3[15:0]	1	65535
> 喝 INT5_pipeline_3[15:0]	9	4

Name	Value	4,800 ns	5,000 ns	5,200 ns   5,
Inputs				
<sup>1</sup> ⊌ clk	0			
¹७ rst	0			
> 🤏 A[15:0]	149		655:	35
> 🥞 B[15:0]	19		655:	35
> NGC[15:0]	61961		655:	35
> N D[15:0]	10		655:	35
Output				
> N O[31:0]	0	10658 272 (16756745)		4
Original Internal Signals				
> 考 INTA[15:0]	53264		655:	35
> 🖥 INTB[15:0]	32		655:	35
> NTC[15:0]	5		655:	35
> 🖥 INTD[15:0]	65535		655:	35
> 😽 INT1[17:0]	159792		1966	05
> 😽 INT2[31:0]	160		429483	6225
> 😽 INT3[31:0]	805		655:	34
> 🖥 INT4[31:0]	0	165920		0
> 考 INT5[15:0]	10		4	
> 🖥 INTO[31:0]	0	272 (16756745)		4
Internal Pipeline 1 Signals				
> 🖥 INT3_pipeline_1[31:0]	0		655:	34
> 🖥 INT5_pipeline_1[15:0]	5		4	
> NTD_pipeline_1[15:0]	1		655:	35
Internal Pipeline 2 Signals				
> 🖥 INT4_pipeline_2[31:0]	0	132 \( 16692816 \)		0
> 3 INT5_pipeline_2[15:0]	0	140 63929		4
Internal Pipeline 3 Signals				
> <b>3</b> INT1_pipeline_3[17:0]	201		1966	05
> <b>3</b> INT2_pipeline_3[31:0]	604		429483	6225
> <b>3</b> INTD_pipeline_3[15:0]	1		655:	35
> <b>3 INT5_pipeline_3[15:0]</b>	9		4	

```
run 5 us
Error:
test vectors value 0
for inputs
A: 67
B: 151
C: 4
D: 1
for outputs
Actual value
0: 814
Predicted value
0: 814
Time: 3840 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 1
for inputs
A: 53264
B: 32
C: 5
D: 65535
for outputs
Actual value
0: 12
Predicted value
Time: 3920 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 2
for inputs
A: 149
B: 19
C: 61961
D: 10
for outputs
Actual value
O: 179736
Predicted value
O: 179736
Time: 4 us Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 3
for inputs
A: 21
B: 49
C: 61680
D: 65332
for outputs
Actual value
0: 61731
Predicted value
0: 61731
```

```
Time: 4080 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 4
for inputs
A: 0
B: 62819
C: 0
D: 38
for outputs
Actual value
0: 5
Predicted value
0: 5
Time: 4160 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 5
for inputs
A: 37
B: 61664
C: 86
D: 62309
for outputs
Actual value
O: 176
Predicted value
Time: 4240 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 6
for inputs
A: 88
B: 65432
C: 63113
D: 54
for outputs
Actual value
O: 76537378
Predicted value
O: 76537378
Time: 4320 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 7
for inputs
A: 69
B: 65004
C: 64565
D: 65350
for outputs
Actual value
0: 128793
Predicted value
0: 128793
```

```
Time: 4400 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test vectors value 8
for inputs
A: 64506
B: 9
C: 5
D: 1
for outputs
Actual value
0: 193573
Predicted value
0: 193573
Time: 4480 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 9
for inputs
A: 64586
B: 9
C: 5
D: 61845
for outputs
Actual value
0: 13
Predicted value
Time: 4560 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 10
for inputs
A: 63945
B: 308
C: 61961
D: 10
for outputs
Actual value
O: 1989548
Predicted value
O: 1989548
Time: 4640 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 11
for inputs
A: 62385
B: 49
C: 61680
D: 35
for outputs
Actual value
0: 153384
Predicted value
0: 153384
```

```
Time: 4720 ns Iteration: 0 Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test vectors value 12
for inputs
A: 63919
B: 64474
C: 0
D: 18
for outputs
Actual value
O: 10658
Predicted value
O: 10658
Time: 4800 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 13
for inputs
A: 65349
B: 61664
C: 135
D: 64255
for outputs
Actual value
0: 272
Predicted value
O: 272
Time: 4880 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
Error:
test vectors value 14
for inputs
A: 64467
B: 63714
C: 63924
D: 244
for outputs
Actual value
O: 16756745
Predicted value
0: 16756745
Time: 4960 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
test vectors value 15
for inputs
A: 65535
B: 65535
C: 65535
D: 65535
for outputs
Actual value
O: 4
Predicted value
0:4
Time: 5040 ns Iteration: 0 Process: /Algorithm Lab 2A tb/TEST OUTPUT
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
✓ ✓ synth_1	constrs_1	synth_design Complete!								1017	2488	0.00	0	0
✓ impl_1	constrs_1	route_design Complete, Failed Timing!	0.546	0.000	-0.038	-0.195	0.000	0.159	0	989	2406	0.00	0	0

create\_clock -period 12.000 -name clk -waveform {0.000 6.0000} [get\_ports clk]

# 2.2.6

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
✓ ✓ synth_2	constrs_1	synth_design Complete!								681	2374	0.00	0	2
√ impl_2	constrs_1	route_design Complete!	0.128	0.000	0.062	0.000	0.000	0.258	0	664	2292	0.00	0	2

create\_clock -period 4.000 -name clk -waveform {0.000 2.0000} [get\_ports clk]

Clock	Waveform(ns)	Period(ns)	Frequency (MHz)				
clk	<b>{0.000 2.000}</b>	4.000	250.000				

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
use work.DigEng.all;
-- Algorithm entity
-- Synchronous calculator of the equation
-- O <= (A*3 + B*C)/D + C +5
-- 6 inputs, standard clk and reset
-- Inputs A, B, C, D std logic vector inputs of values
-- to computate.
-- output "O" is result of the equation.
-- 4 at innputs one for each value input A, B, C and D
-- 1 at output 0
-- this entity has 5 sets of pipe lined registers
-- 1st Input Register input registers to store inputs
-- 2nd "pipeline 3" results of (3*A), (B*C), D, (5+C) each stored in
registers
-- 3rd "pipeline 1" results of (3*A)+(B*C), D, (5+C) each stored in
registers
-- Note* divider has 34 internal pipelined sections requiring a
-- Pipelined array of (5+C) made up of 34 registers using the FIFO
method
-- 4th "pipeline 2" results of (3*A)+(B*C)/D, (5+C) each stored in
registers
-- 5th output registers results of ((3*A)+(B*C)/D)+(5+C) stored in
register
-- Computation of entire equation takes 41 clk clyes
-- the 41 clk cycles delay the inital result but speed up the
-- entire circuit due to the pipelined sections. They allow
-- the the time resource heavy divide and multiplication processes
-- to compute in 1 clk cycle reducing the time required for processing
-- the entire equation.
entity algorithm is
                          : integer := 16;
    generic (data size
             -- number of registers in pipeline array
             Divider Delay : integer := 34);
    Port ( A : in STD LOGIC VECTOR (data size-1 downto 0);
           B : in STD LOGIC VECTOR (data size-1 downto 0);
           C : in STD LOGIC VECTOR (data size-1 downto 0);
           D: in STD LOGIC VECTOR (data size-1 downto 0);
           O : out STD LOGIC VECTOR (data size*2-1 downto 0);
           clk : in STD LOGIC;
           rst : in STD LOGIC);
end algorithm;
```

```
architecture Behavioral of algorithm is
-- internal input between Input register & Pipeline 3
signal INTA, INTB, INTC, INTD : UNSIGNED (data size-1 downto 0);
signal INT1 : UNSIGNED (data size+1 downto 0);
signal INT2 : UNSIGNED (data size*2-1 downto 0);
signal INT5 : UNSIGNED (data size-1 downto 0);
--signals between pipeline 3 & Pipeline 1
signal INT3 : UNSIGNED (data size*2-1 downto 0);
-- signals outputs of pipeline 3
signal INT1 pipeline 3 : UNSIGNED (data size+1 downto 0);
signal INT2 pipeline 3 : UNSIGNED (data size*2-1 downto 0);
signal INTD pipeline 3 : UNSIGNED (data size-1 downto 0);
signal INT5 pipeline 3 : UNSIGNED (data size-1 downto 0);
--signals between pipeline 1 & Pipeline 2
-- signals outputs of pipeline 1
signal INT3 pipeline 1 : UNSIGNED (data size*2-1 downto 0);
signal INT5 pipeline 1 : UNSIGNED (data size-1 downto 0);
signal INTD pipeline 1 : UNSIGNED (data size-1 downto 0);
-- result of divider
signal INT4 : UNSIGNED (data size*2-1 downto 0);
signal quotient : std logic vector(data size*2-1 downto 0);
--signals between pipeline 2 & output register
-- signals outputs for pipeline 2
signal INT4 pipeline 2 : UNSIGNED (data size*2-1 downto 0);
signal INT5 pipeline 2 : UNSIGNED (data size-1 downto 0);
--signal output to peripheral
signal INTO : UNSIGNED (data size*2-1 downto 0);
-- array of registers for pipline array
-- required due to divider components internal pipline
type Pipeline_Array is array (0 to Divider Delay -1) of UNSIGNED
(Data size -1 downto 0);
signal INT Pipe Array out : Pipeline Array;
-- array of connections between each register of the piplione array
type Pipe reg array Connect is array (0 to Divider Delay + 1) of
UNSIGNED (Data size -1 downto 0);
signal INT bus in : Pipe reg array Connect;
-- component deceleration
-- synchronous divider with 34 internal pipline sections
component divider
port (
clk: in std logic;
sclr: in std_logic;
rfd: out std logic;
dividend: in std logic vector(31 downto 0);
divisor: in std logic vector(15 downto 0);
quotient: out std logic vector(31 downto 0);
fractional: out std logic vector(15 downto 0)
);
end component;
```

```
begin
-- setup for individual input registers for inputs A,B, C & D
-- All Synchronous with reset to zero when reset signal active,
-- NO enable signals required.
input regs: process (clk) is
begin
  if rising edge (clk) then
  -- resets internal signals below to zero
    if rst = '1' then
      INTA <= (others => '0');
      INTB <= (others => '0');
      INTC <= (others => '0');
      INTD \langle = (0 \Rightarrow '1', others \Rightarrow '0'); -- aggregate notation
      INTD <= to unsigned(1,INTD'length); -- type conversion notation</pre>
    -- connects inputs to internal signal values
      INTA <= unsigned(A);</pre>
      INTB <= unsigned(B);</pre>
      INTC <= unsigned(C);</pre>
      INTD <= unsigned(D);</pre>
    end if;
  end if;
end process input regs;
-- equation maths defined per internal signals
--in between input registers and pipline 3
INT1 <= INTA * to unsigned(3, 2);</pre>
INT2 <= INTB * INTC;
INT5 <= INTC + to unsigned(5, INT5'length);</pre>
--in between pipline 3 and pipline 1
INT3 <= INT1_pipeline_3 + INT2_pipeline_3;</pre>
--in between pipline 2 and pipline output registers
INTO <= INT5 pipeline 2 + INT4 pipeline 2;</pre>
-- output register.
-- synchronous.
-- output = 0 at rising clk edge
-- when input reset is active.
-- output = INTO at rising clk edge.
output regs: process (clk) is
begin
  if rising edge (clk) then
    if rst = '1' then
      0 <= (others => '0');
      0 <= std logic vector(INTO);</pre>
    end if;
  end if;
end process output regs;
-- pipline 1 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
```

```
pipeline 1: process (clk) is
begin
  if rising edge (clk) then
    if rst = '1' then
    INT3 pipeline 1 <= (others => '0');
    INT5 pipeline 1 <= (others => '0');
    INTD pipeline 1 <= to unsigned(1,INTD'length); -- type conversion
notation
    else
    INT3 pipeline 1 <= INT3;</pre>
    INT5 pipeline 1 <= INT5 pipeline 3;</pre>
    INTD pipeline 1 <= INTD pipeline 3;</pre>
    end if;
  end if;
end process pipeline 1;
-- pipline 2 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline 2: process (clk) is
begin
  if rising edge (clk) then
    if rst = '1' then
    INT4_pipeline_2 <= (others => '0');
    INT5 pipeline 2 <= (others => '0');
    else
    INT4 pipeline 2 <= INT4;</pre>
    -- final output of pipeline array input to pipeline 2
    INT5 pipeline 2 <= INT Pipe Array out (Divider Delay-1);</pre>
    end if;
  end if;
end process pipeline_2;
-- pipline 3 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline 3: process (clk) is
begin
  if rising edge (clk) then
    if rst = '1' then
    INT1_pipeline_3 <= (others => '0');
INT2_pipeline_3 <= (others => '0');
INT5_pipeline_3 <= (others => '0');
    INTD pipeline 3 <= to unsigned(1,INTD'length); -- type conversion
notation
    else
    INT1_pipeline_3 <= INT1;</pre>
    INT2_pipeline_3 <= INT2;</pre>
    INT5_pipeline_3 <= INT5;</pre>
    INTD pipeline 3 <= INTD;</pre>
    end if;
  end if;
end process pipeline 3;
```

```
--Xilinx piplined (x34) divider
-- synchronous
-- reset high output = 0
-- input dividend / input divisor
-- quotient = output value
my divider : divider
port map (
clk => clk,
sclr => rst,
 dividend => std logic vector(INT3 pipeline 1),
 divisor => std logic vector(INTD pipeline 1),
 quotient => quotient
 );
 -- internal 4 connection to result of divider
INT4 <= unsigned(quotient);</pre>
--Connect input to pipeline array
INT bus in(0) <=INT5 pipeline 1;</pre>
--pipe lined array deceleration
-- array of the registers that make up the pipeline
-- generated to match the 34 pipelined sections inside the
--divider to keep all of the data synchronised
Pipeline Array registers: for i in 0 to Divider Delay - 1 generate
D_type_flip_flop: entity work.D_type_FF
generic map(Data_Size => Data_Size)
Port Map (
         clk => clk,
         rst => rst,
         Data In => INT bus in (i) ,
         Data_Out =>INT_Pipe_Array_out(i)
        );
-- connections between register outputs to next input.
INT bus in(i+1) <= INT Pipe Array out(i) ;</pre>
end generate;
end Behavioral;
```

```
_____
Start RTL Component Statistics
Detailed RTL Component Info :
+---Adders :
        2 Input 32 Bit Adders := 1
2 Input 16 Bit Adders := 1
+---Registers :
                   32 Bit Registers := 2
16 Bit Registers := 43
Finished RTL Component Statistics
Start RTL Hierarchical Component Statistics
______
Hierarchical RTL Component report
Module algorithm
Detailed RTL Component Info :
+---Adders :
        2 Input 32 Bit Adders := 1
2 Input 16 Bit Adders := 1
+---Registers :
                   32 Bit Registers := 2
16 Bit Registers := 9
Module D_type_ff
Detailed RTL Component Info :
+---Registers :
                  16 Bit Registers := 1
Finished RTL Hierarchical Component Statistics
```