Task 1:

1.1.1:

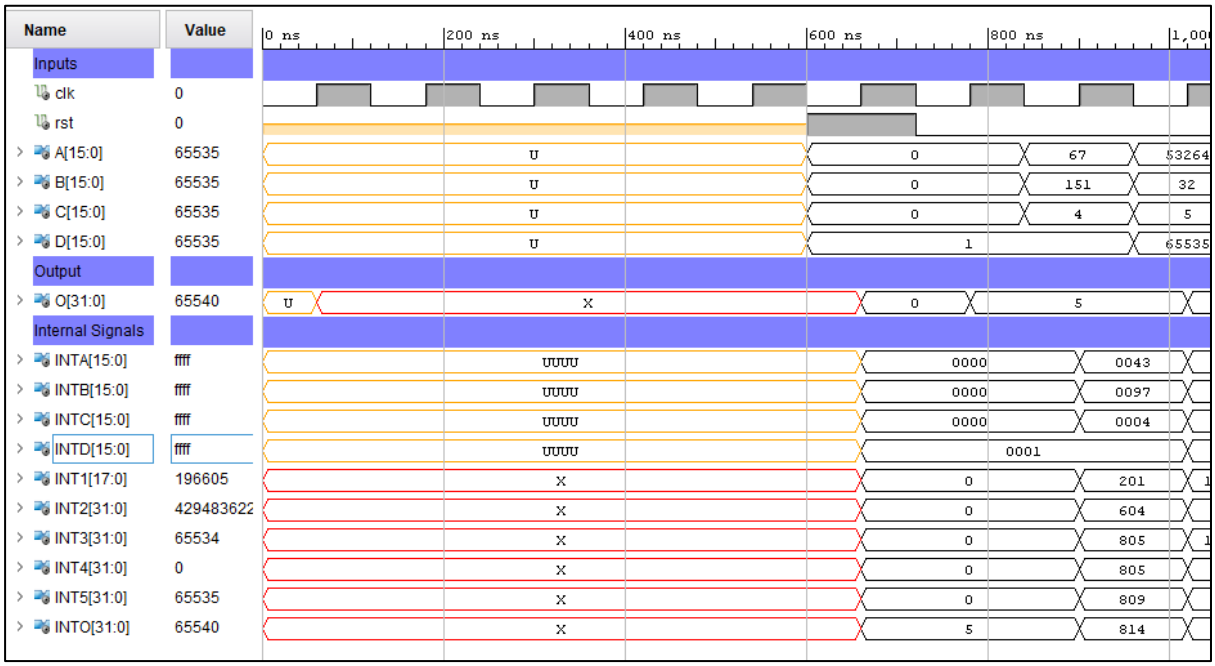
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity Algorithm_Lab_2A_tb is
end Algorithm_Lab_2A_tb;
-- test bench is a 2 stage process
-- input test process resets the circuit and inputs to known
--values, the 16 different iterations of large input values through
-- 4 inputs A,B,C and D are tested and the result is output 2 clk
-- cycles later. The mathematical function that is conducted is:
-- O <= (A*3 + B*C)/D + C +5.
architecture Behavioral of Algorithm_Lab_2A_tb is

-- Constants
constant data_size : integer := 16;
constant wait_period : time := 500ns;
constant clk_period  : time := 120ns;
constant process_two_wait : time := 1000ns;

--input signals
signal clk : STD_LOGIC;
signal rst : STD_LOGIC;
signal A  : STD_LOGIC_VECTOR (data_size-1 downto 0);
signal B  : STD_LOGIC_VECTOR (data_size-1 downto 0);
signal C  : STD_LOGIC_VECTOR (data_size-1 downto 0);
signal D  : STD_LOGIC_VECTOR (data_size-1 downto 0);

--output signals
signal O : STD_LOGIC_VECTOR (data_size*2-1 downto 0);

type test_vector is record
--Input test vectors
A :  STD_LOGIC_VECTOR (data_size-1 downto 0);
B :  STD_LOGIC_VECTOR (data_size-1 downto 0);
C :  STD_LOGIC_VECTOR (data_size-1 downto 0);
D :  STD_LOGIC_VECTOR (data_size-1 downto 0);
-- Output test vectors
O : STD_LOGIC_VECTOR (data_size*2-1 downto 0);
end record;

--test vector inputs and outputs
-- tests each of the 16 different variations
-- of the individual inputs being large or small values
type test_vector_array is array (natural range <>) of test_vector;
constant test_vectors : test_vector_array := (
--    A         B           C             D              O
-- Large D
  (X"0043",  X"0097",    X"0004",     X"0001",        X"0000032E"),
-- Large D
  (X"D010",  X"0020",    X"0005",     X"FFFF",        X"0000000C"),

-- Large C
  (X"0095",  X"0013",    X"F209",     X"000A",        X"0002BE18"),

-- large C large D
  (X"0015",  X"0031",    X"F0F0",     X"FF34",        X"0000F123"),

 -- large B
  (X"0000",  X"F563",    X"0000",     X"0026",        X"00000005"),
```

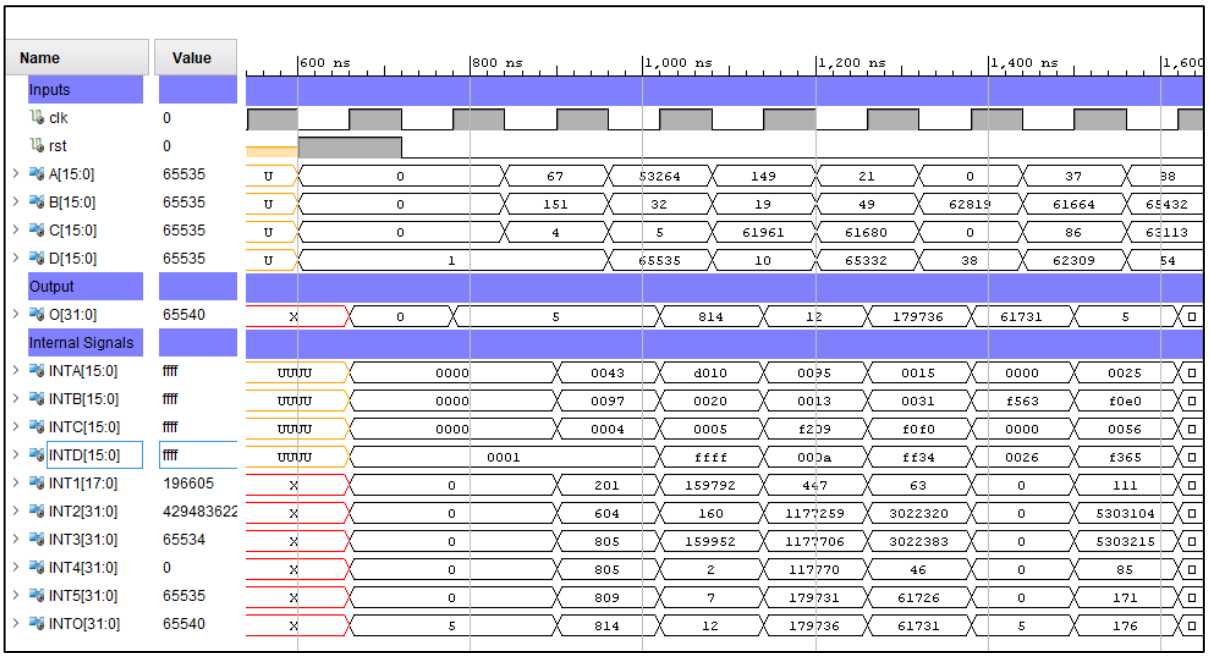
```
-- large B and D
  (X"0025",  X"F0E0",    X"0056",     X"F365",        X"000000B0"),


-- Large B and large C
  (X"0058",  X"FF98",    X"F689",     X"0036",        X"048FDE22"),

-- Large B, large C and large D
  (X"0045",  X"FDEC",    X"FC35",     X"FF46",        X"0001F719"),

-- Large A
  (X"FBFA",  X"0009",    X"0005",     X"0001",        X"0002F425"),

-- Large A, Large D
  (X"FC4A",  X"0009",    X"0005",     X"F195",        X"0000000D"),

-- Large A, Large C
  (X"F9C9",  X"0134",    X"F209",     X"000A",        X"001E5BAC"),

-- Large A, large C large D
  (X"F3B1",  X"0031",    X"F0F0",     X"0023",        X"00025728"),

-- Large A, large B
  (X"F9AF",  X"FBDA",    X"0000",     X"0012",        X"000029A2"),

-- Large A, large B and D
  (X"FF45",  X"F0E0",    X"0087",     X"FAFF",        X"00000110"),

-- Large A, Large B and large C
  (X"FBD3",  X"F8E2",    X"F9B4",     X"00F4",        X"00FFB009"),

-- Large A, Large B, large C and large D
  (X"FFFF",  X"FFFF",    X"FFFF",     X"FFFF",        X"00010004"));

begin

UUT: entity work.algorithm
--maps data size to 16 bits
GENERIC MAP( data_size => data_size)

    PORT MAP (clk  => clk ,
              rst  => rst,
              A    => A,
              B    => B,
              C    => C,
              D    => D,
              O    => O );

-- Clock process
clk_process :process
begin
 clk <= '0';
 wait for clk_period/2;
 clk <= '1';
```

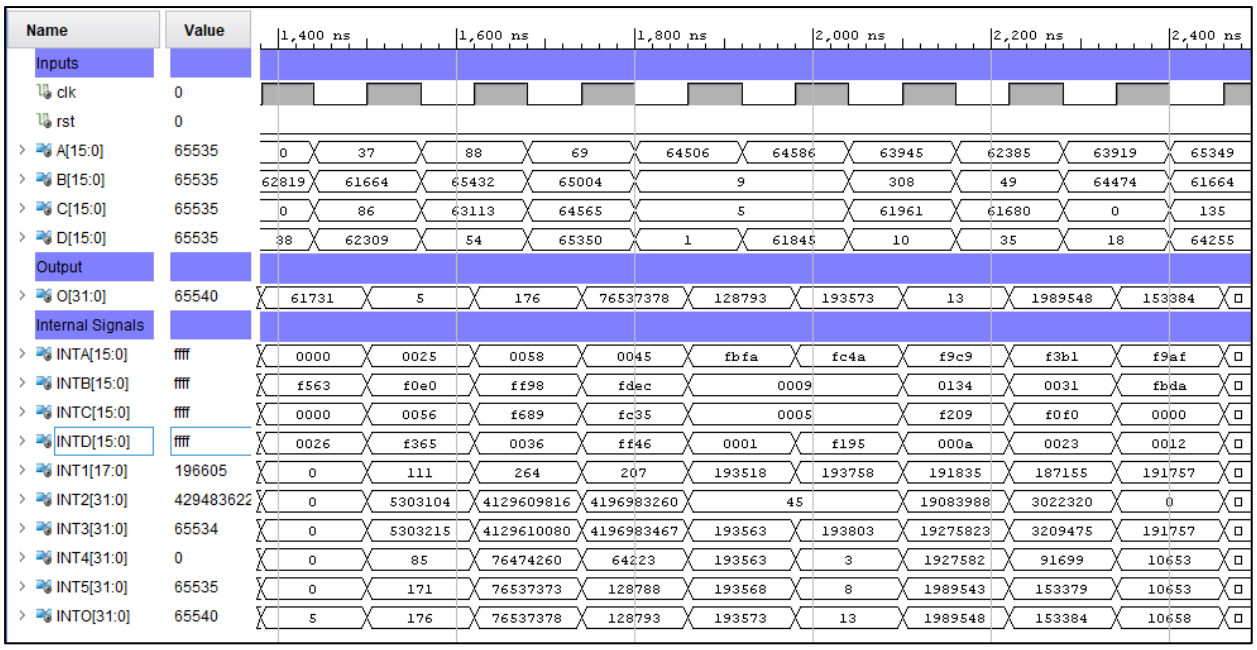
```
-- test process 1
-- resets the circuit and sets inputs to known values
-- inputs all test vectors from test array one set per clk cycle
-- inputs change each clk cycle.
TEST_INPUT : process
begin
-- wait 500 ns for global reset tot finish set by Xilinx
wait for wait_period;
-- waits until falling edge of clock cycle
wait until falling_edge(clk);

-- set inputs to known values and resets system
 rst   <= '1';
 A     <= x"0000";
 B     <= x"0000";
 C     <= x"0000";
 D     <= x"0001";

 wait for clk_period;
 -- stop reset signal
 rst   <= '0';
 wait for clk_period;

-- test all inputs A, B, C, D vectors
-- from test vector array within a loop
-- for loop to assert each line of test vectors array
-- number of iterations of loop matches the size of the test vector
-- array
  for i in test_vectors'range loop

       A  <= test_vectors(i).A;
       B  <= test_vectors(i).B;
       C  <= test_vectors(i).C;
       D  <= test_vectors(i).D;
       wait for clk_period;

   end loop;
 wait; --waits forever

 end process;

 -- test process 2
 -- delays process beginning as the output is delayed by
 -- 2 clk cycles after the inititialisation and reset of system
 -- process begins after this point and tests output values to the
 -- original input vectors.

 TEST_OUTPUT : process
 begin
 -- wait 500 ns for global reset to finish set by Xilinx
 wait for wait_period;

 -- waits until falling clk edge furthest possible point from register
 -- value changes
 wait until falling_edge(clk);
```

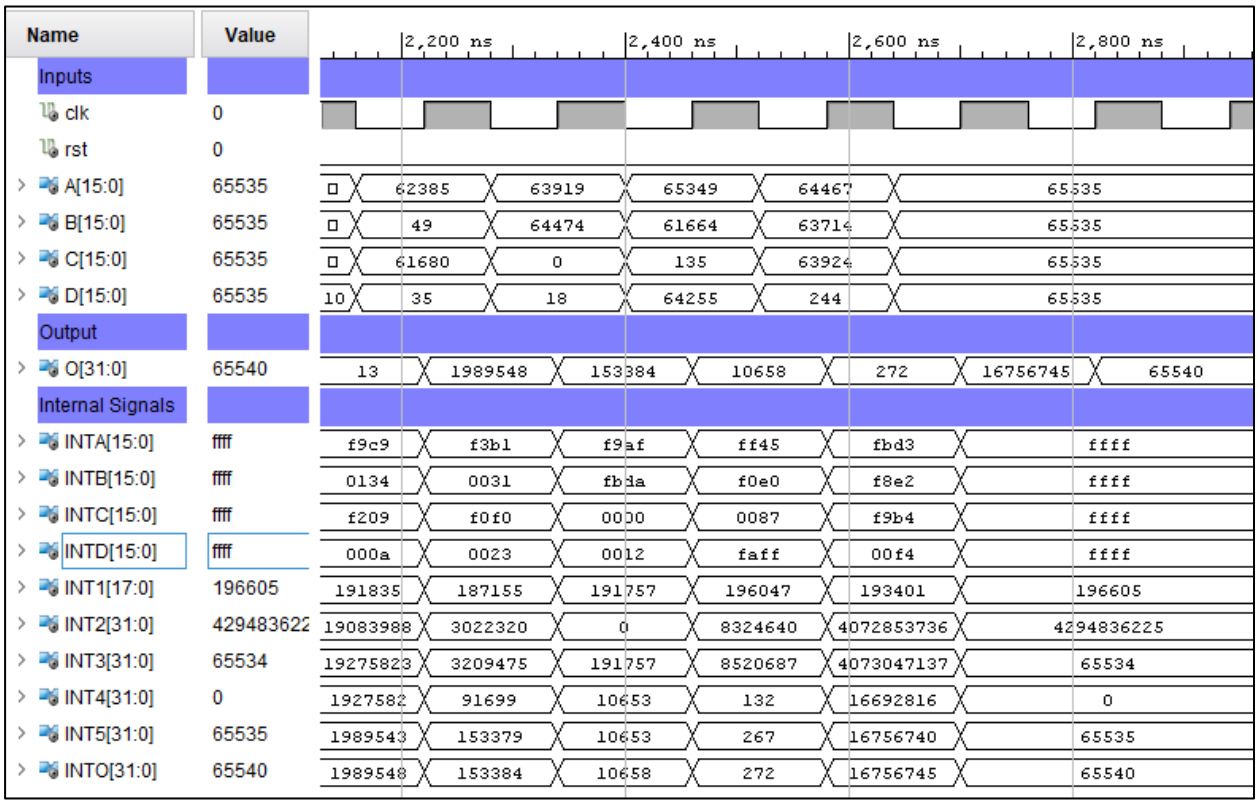
```
--wait for four clock periods two for the reset and initial values to
 --be set to a known value and two for the 2 clk cycle offset due to the
 -- input and output registers.
 wait for clk_period*4;
-- for loop to assert each line of test vectors array
-- number of iterations of loop matches the size of the test vector
-- array

for i in test_vectors'range loop

 assert  ( O <= test_vectors(i).O);
-- report the values of all inputs and outputs in the case of wrong predicted values
with formatting
 report   CR &
 "test_vectors value "    & integer'image(i)  & CR & CR &
 "for inputs"   & CR &
 "A: "          & integer  'image(to_integer(unsigned(test_vectors(i).A))) & CR &
 "B: "          & integer  'image(to_integer(unsigned(test_vectors(i).B))) & CR &
 "C: "          & integer  'image(to_integer(unsigned(test_vectors(i).C))) & CR &
 "D: "          & integer  'image(to_integer(unsigned(test_vectors(i).D))) & CR & CR
&

 "for outputs"     & CR &
 "Actual value"    & CR &
 "O: "             & integer  'image(to_integer(unsigned(O))) & CR &
 "Predicted value" & CR &
 "O: "             & integer  'image(to_integer(unsigned(test_vectors(i).O))) & CR
  severity error; -- only reports errors does NOT stop the program if errors detected

  -- allows next values to be held in input and output registers
  wait for clk_period;
   end loop;

  wait; --waits forever

 end process;
end Behavioral;
```

1.1.2


Name
Value
0 ns
200 ns
400 ns
600 ns
800 ns
Inputs
clk 0
rst 0
A[15:0] 65535
B[15:0] 65535
C[15:0] 65535
D[15:0] 65535
Output
O[31:0] 65540
Internal Signals
INTA[15:0] ffff
INTB[15:0] ffff
INTC[15:0] ffff
INTD[15:0] ffff
INT1[17:0] 196605
INT2[31:0] 429483622
INT3[31:0] 65534
INT4[31:0] 0
INT5[31:0] 65535
INTO[31:0] 65540


Name
Value
600 ns
800 ns
1,000 ns
1,200 ns
1,400 ns
Inputs
clk 0
rst 0
A[15:0] 65535
B[15:0] 65535
C[15:0] 65535
D[15:0] 65535
Output
O[31:0] 65540
Internal Signals
INTA[15:0] ffff
INTB[15:0] ffff
INTC[15:0] ffff
INTD[15:0] ffff
INT1[17:0] 196605
INT2[31:0] 429483622
INT3[31:0] 65534
INT4[31:0] 0
INT5[31:0] 65535
INTO[31:0] 65540


Name
Value
1,400 ns
1,600 ns
1,800 ns
2,000 ns
2,200 ns
2,400 ns
Inputs
clk 0
rst 0
A[15:0] 65535 0 37 88 69 64506 64586 63945 62385 63919 65349
B[15:0] 65535 62819 61664 65432 65004 9 308 49 64474 61664
C[15:0] 65535 0 86 63113 64565 5 61961 61680 0 135
D[15:0] 65535 38 62309 54 65350 1 61845 10 35 18 64255
Output
O[31:0] 65540 61731 5 176 76537378 128793 193573 13 1989548 153384
Internal Signals
INTA[15:0] ffff 0000 0025 0058 0045 fbfa fc4a f9c9 f3b1 f9af
INTB[15:0] ffff f563 f0e0 ff98 fdec 0009 0134 0031 fbda
INTC[15:0] ffff 0000 0056 f689 fc35 0005 f209 f0f0 0000
INTD[15:0] ffff 0026 f365 0036 ff46 0001 f195 000a 0023 0012
INT1[17:0] 196605 0 111 264 207 193518 193758 191835 187155 191757
INT2[31:0] 429483622 0 5303104 4129609816 4196983260 45 19083988 3022320 0
INT3[31:0] 65534 0 5303215 4129610080 4196983467 193563 193803 19275823 3209475 191757
INT4[31:0] 0 0 85 76474260 64223 193563 3 1927582 91699 10653
INT5[31:0] 65535 0 171 76537373 128788 193568 8 1989543 153379 10653
INTO[31:0] 65540 5 176 76537378 128793 193573 13 1989548 153384 10658


Name
Value
2,200 ns
2,400 ns
2,600 ns
2,800 ns
Inputs
clk 0
rst 0
A[15:0] 65535 62385 63919 65349 64467 65535
B[15:0] 65535 49 64474 61664 63714 65535
C[15:0] 65535 61680 0 135 63924 65535
D[15:0] 65535 10 35 18 64255 244 65535
Output
O[31:0] 65540 13 1989548 153384 10658 272 16756745 65540
Internal Signals
INTA[15:0] ffff f9c9 f3b1 f9af ff45 fbd3 ffff
INTB[15:0] ffff 0134 0031 fbda f0e0 f8e2 ffff
INTC[15:0] ffff f209 f0f0 0000 0087 f9b4 ffff
INTD[15:0] ffff 000a 0023 0012 faff 00f4 ffff
INT1[17:0] 196605 191835 187155 191757 196047 193401 196605
INT2[31:0] 429483622 19083988 3022320 0 8324640 4072853736 4294836225
INT3[31:0] 65534 19275823 3209475 191757 8520687 4073047137 65534
INT4[31:0] 0 1927582 91699 10653 132 16692816 0
INT5[31:0] 65535 1989543 153379 10653 267 16756740 65535
INTO[31:0] 65540 1989548 153384 10658 272 16756745 65540

```
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 1080 ns  Iteration: 1  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 1320 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT

Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 1440 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 1560 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 1680 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 1800 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793
```

```
Time: 1920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 2040 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 2160 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548

Time: 2280 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153384
Predicted value
O: 153384
```

```
Time: 2400 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 2520 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 2640 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745

Time: 2760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 65540
Predicted value
O: 65540

Time: 2880 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

1.1.3

Tcl Console | Messages | Log | Reports | **Design Runs** ×

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete!	29.183	0.000	0.610	0.000	0.000	0.108	0	886	96	0.00	0	0

Figure 1 designs run tab up to dsp

1.1.3: Print out a screenshot of the "Design Runs" tab, showing all columns up to "DSP".

In your own words, and in relation to the lecture material, explain how the WNS is calculated. What is the maximum frequency at which the circuit can run, according to the tools?

Worst negative slack is the time left over from the time period asked for by the user (time asked for 120ns - time taken to complete circuit) the time taken for the circuit to process through the critical path i.e. the longest path through the circuit.

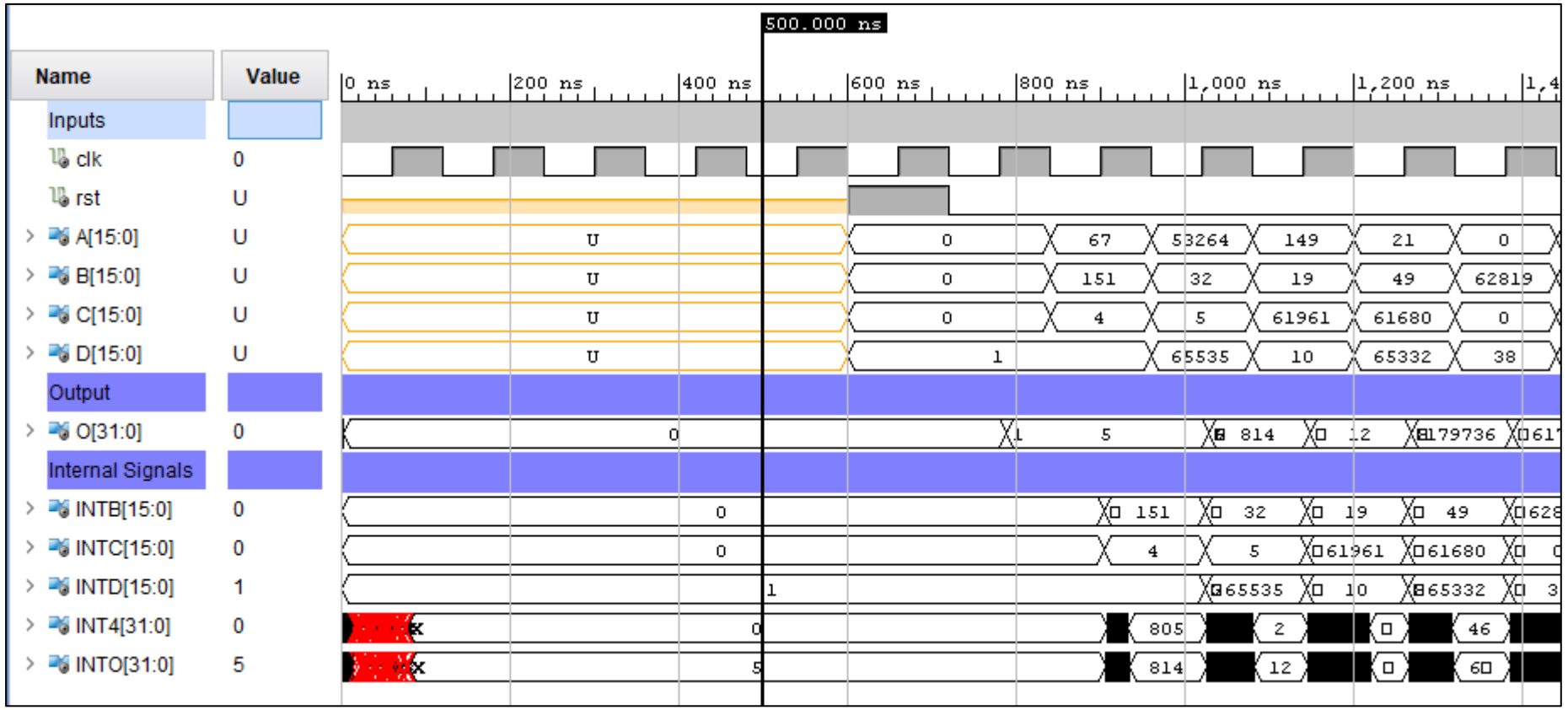
Time asked for = 120ns

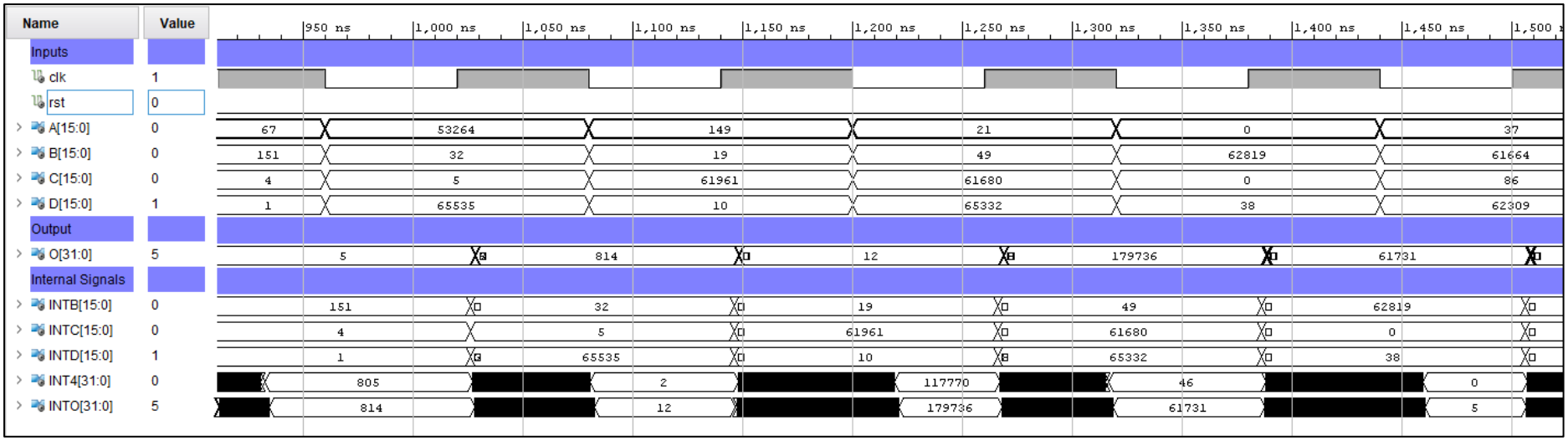
Worst Time Slack = 29.183ns

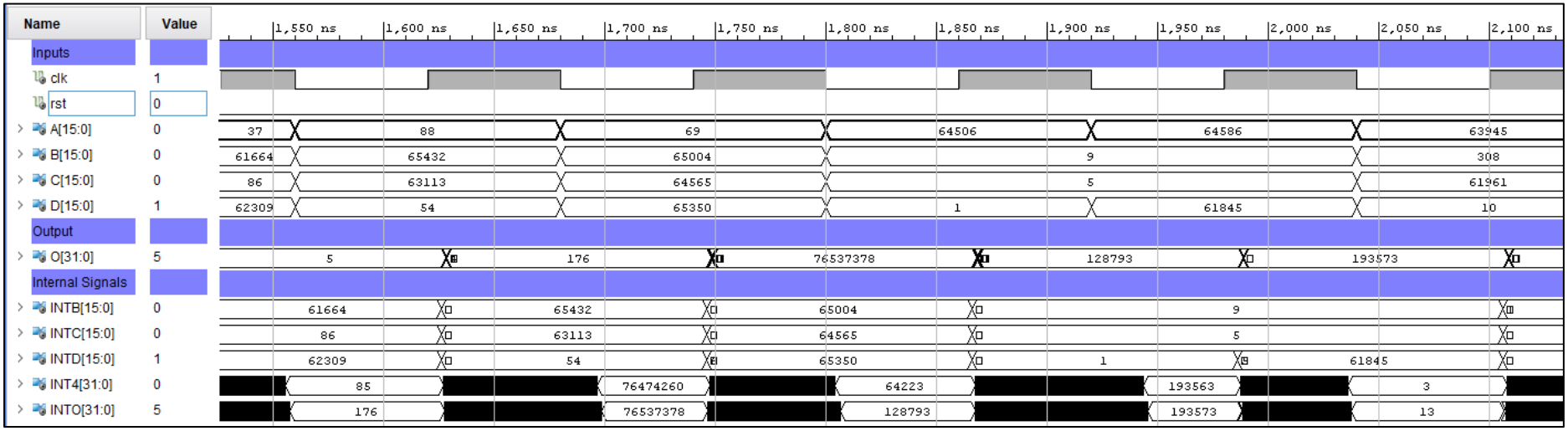
Critical path time = 90.817ns = 120ns - 29.183ns

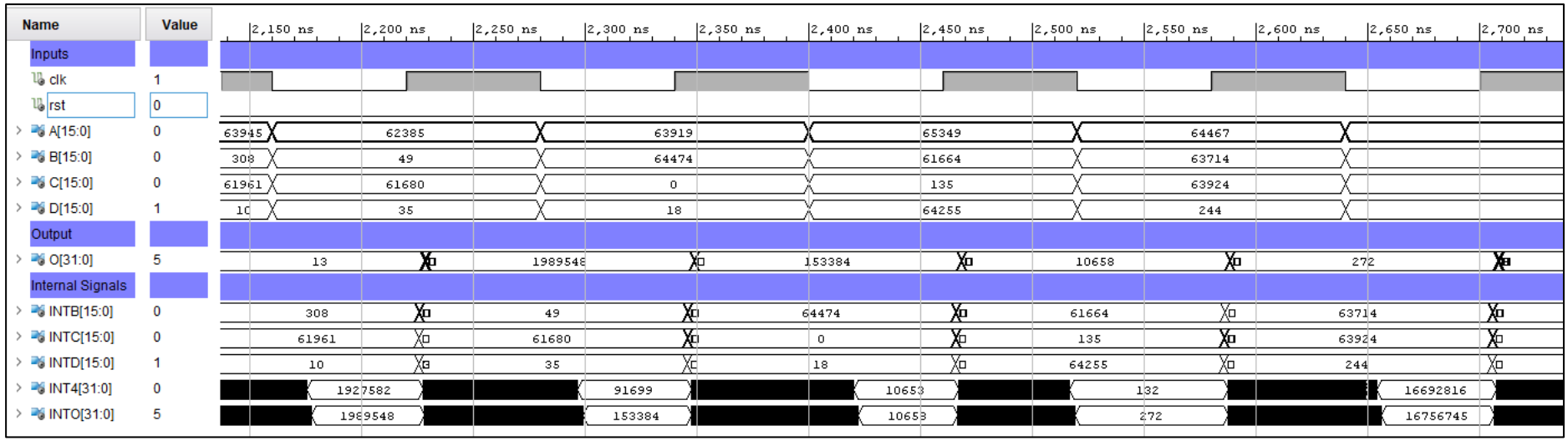
Maximum frequency = $\frac{1}{Critical\ path\ Time}$ = $\frac{1}{90.817ns}$ = 190,817,000,000Hz

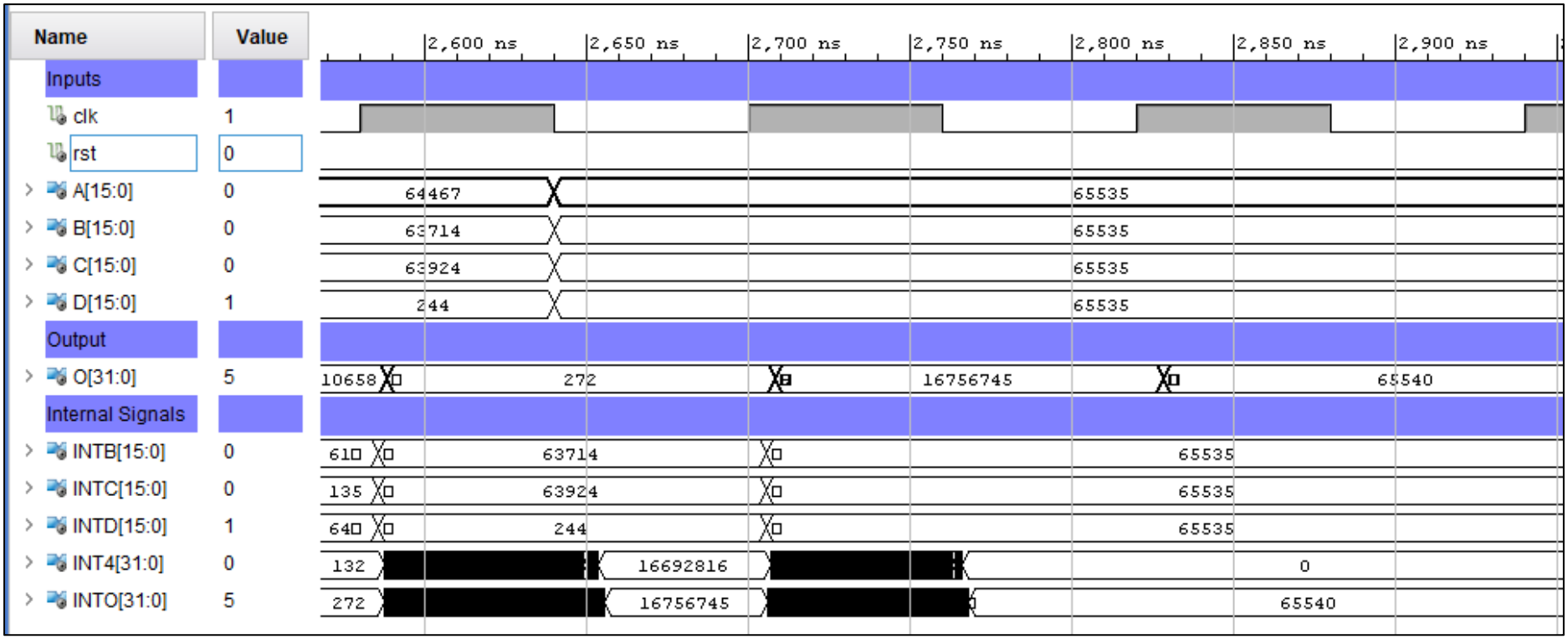
1.1.4


500.000 ns
Name
Value
0 ns
200 ns
400 ns
600 ns
800 ns
1,000 ns
1,200 ns
Inputs
clk 0
rst U
A[15:0] U
B[15:0] U
C[15:0] U
D[15:0] U
Output
O[31:0] 0
Internal Signals
INTB[15:0] 0
INTC[15:0] 0
INTD[15:0] 1
INT4[31:0] 0
INTO[31:0] 5


Name
Value
950 ns
1,000 ns
1,050 ns
1,100 ns
1,150 ns
1,200 ns
1,250 ns
1,300 ns
1,350 ns
1,400 ns
1,450 ns
Inputs
clk 1
rst 0
A[15:0] 0 67 53264 149 21 0 37
B[15:0] 0 151 32 19 49 62819 61664
C[15:0] 0 4 5 61961 61680 0 86
D[15:0] 1 1 65535 10 65332 38 62309
Output
O[31:0] 5 5 814 12 179736 61731
Internal Signals
INTB[15:0] 0 151 32 19 49 62819
INTC[15:0] 0 4 5 61961 61680 0
INTD[15:0] 1 1 65535 10 65332 38
INT4[31:0] 0 805 2 117770 46 0
INTO[31:0] 5 814 12 179736 61731 5


Name
Value
1,550 ns
1,600 ns
1,650 ns
1,700 ns
1,750 ns
1,800 ns
1,850 ns
1,900 ns
1,950 ns
2,000 ns
2,050 ns
2,100 ns
Inputs
clk 1
rst 0
A[15:0] 0 37 88 69 64506 64586 63945
B[15:0] 0 61664 65432 65004 9 308
C[15:0] 0 86 63113 64565 5 61961
D[15:0] 1 62309 54 65350 1 61845 10
Output
O[31:0] 5 5 176 76537378 128793 193573
Internal Signals
INTB[15:0] 0 61664 65432 65004 9
INTC[15:0] 0 86 63113 64565 5
INTD[15:0] 1 62309 54 65350 1 61845
INT4[31:0] 0 85 76474260 64223 193563 3
INTO[31:0] 5 176 76537378 128793 193573 13


Name
Value
2,150 ns
2,200 ns
2,250 ns
2,300 ns
2,350 ns
2,400 ns
2,450 ns
2,500 ns
2,550 ns
2,600 ns
2,650 ns
2,700 ns
Inputs
clk 1
rst 0
A[15:0] 0 63945 62385 63919 65349 64467
B[15:0] 0 308 49 64474 61664 63714
C[15:0] 0 61961 61680 0 135 63924
D[15:0] 1 10 35 18 64255 244
Output
O[31:0] 5 13 1989548 153384 10658 272
Internal Signals
INTB[15:0] 0 308 49 64474 61664 63714
INTC[15:0] 0 61961 61680 0 135 63924
INTD[15:0] 1 10 35 18 64255 244
INT4[31:0] 0 1927582 91699 10653 132 16692816
INTO[31:0] 5 1989548 153384 10653 272 16756745


Name
Value
2,600 ns
2,650 ns
2,700 ns
2,750 ns
2,800 ns
2,850 ns
2,900 ns
Inputs
clk
1
rst
0
A[15:0]
0
64467
65535
B[15:0]
0
63714
65535
C[15:0]
0
63924
65535
D[15:0]
1
244
65535
Output
O[31:0]
5
10658
272
16756745
65540
Internal Signals
INTB[15:0]
0
61
63714
65535
INTC[15:0]
0
135
63924
65535
INTD[15:0]
1
64
244
65535
INT4[31:0]
0
132
16692816
0
INTO[31:0]
5
272
16756745
65540

```
run 5 us
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 1080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 1320 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 1440 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 1560 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 1680 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 1800 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793
```

```
Time: 1920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 2040 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 2160 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548

Time: 2280 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153384
Predicted value
O: 153384
```

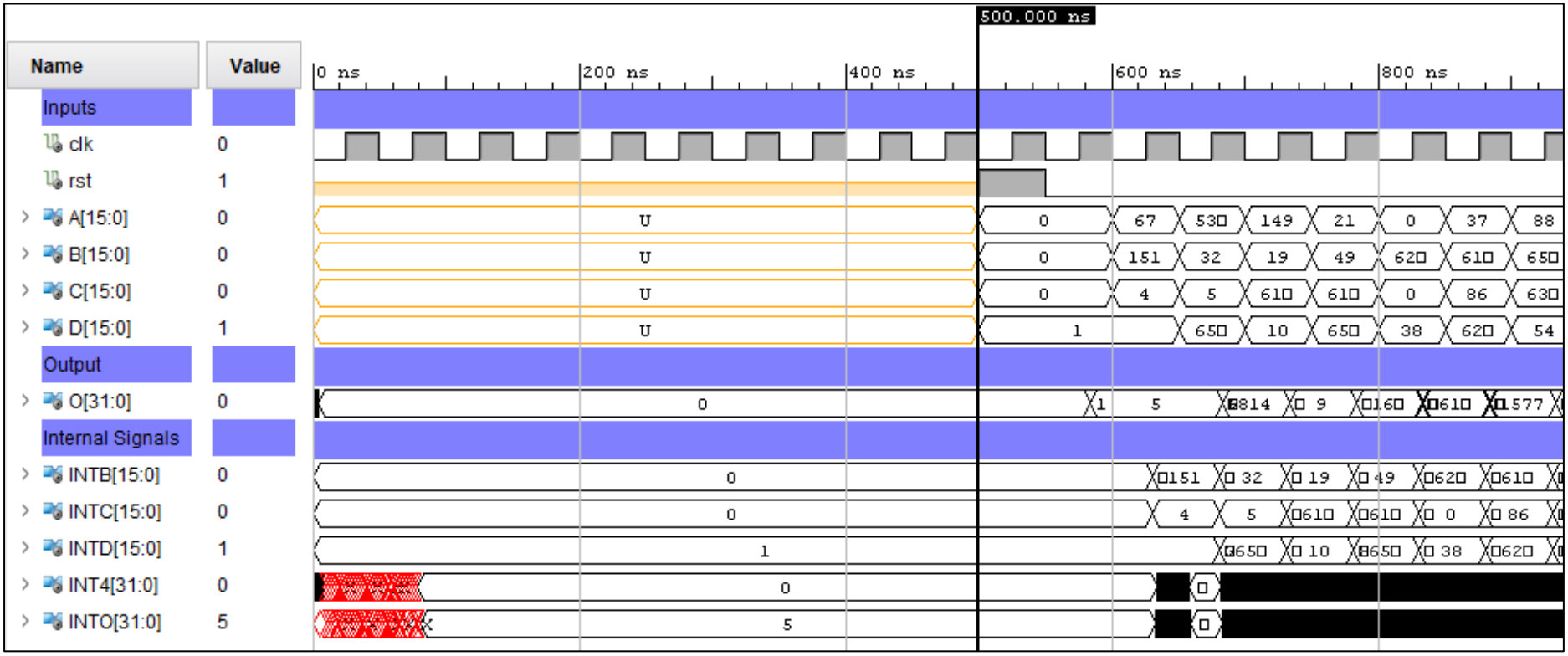
```
Time: 2400 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 2520 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 2640 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745

Time: 2760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 65540
Predicted value
O: 65540

Time: 2880 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

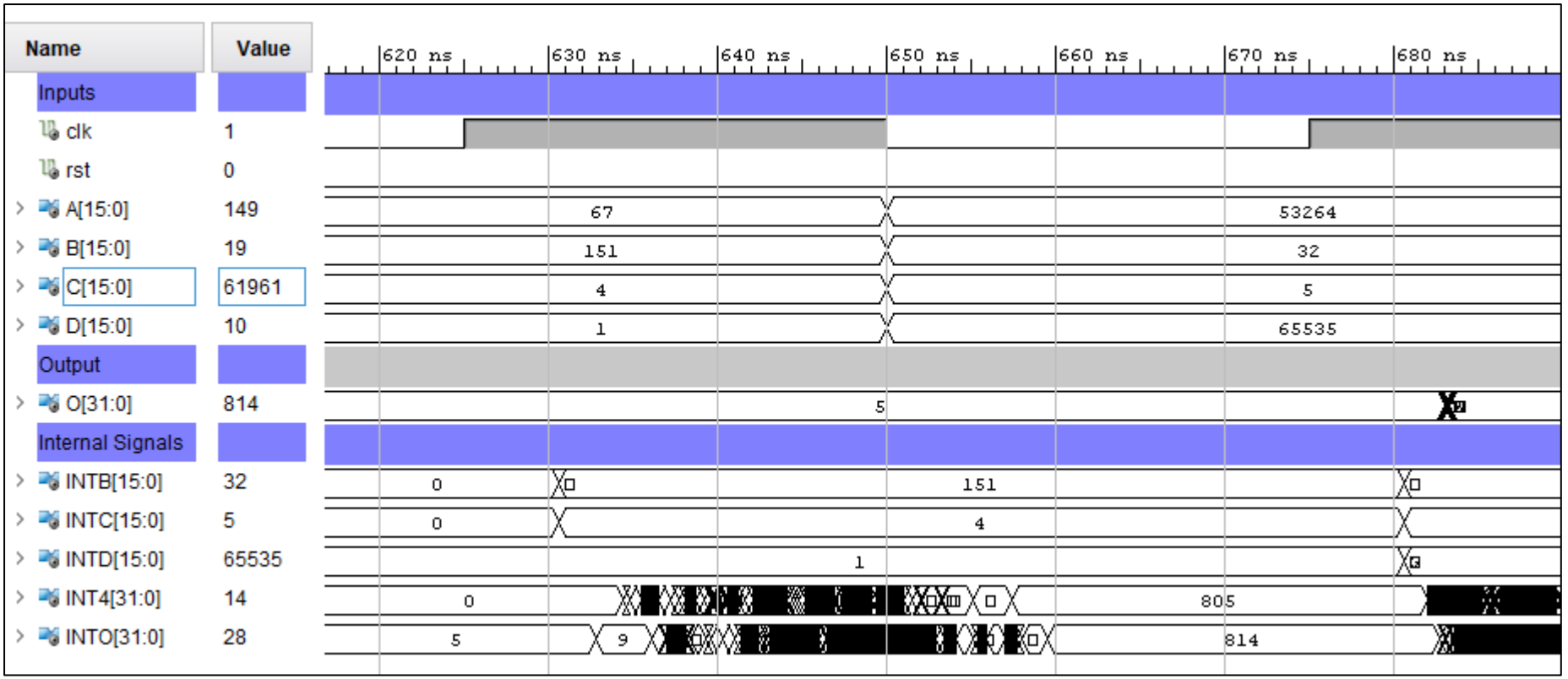
1.1.5:

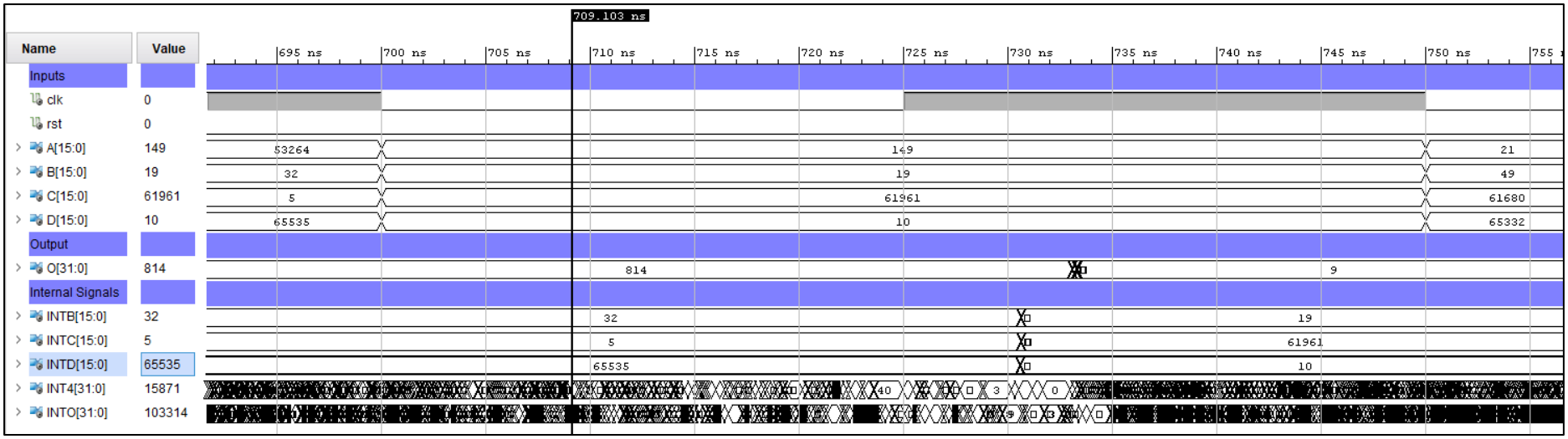
Try to explain why some internal signals are not available for observation and why some are. Comment on and explain the output of the simulation, particularly the behaviour of INTO and of the output, relating it to the material covered in the lectures.

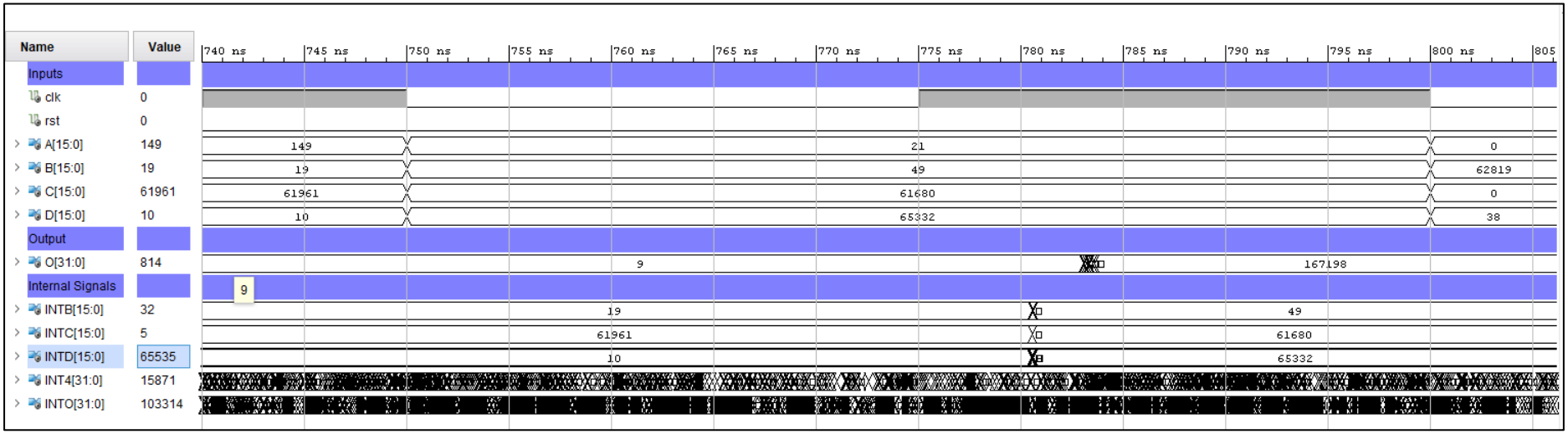
The missing internal signals 1-5 have been optimised out of the circuit for efficiency to meet the timing requested by the user through the running of the implementation onto the virtual circuit. The Internal signals that have not been optimised are the ones connected to the inputs and outputs meaning they are required to connected the internal circuit to the ports. The INTO and the output O are the same value but the output is delayed by 1 clock cycle this is due to them being within different cut sets and requiring a register between so that the function of the circuit is realised but the output value is held for 1 clock cycle. The means that the entire circuit has a delay but the makes the inputs and outputs more stable.

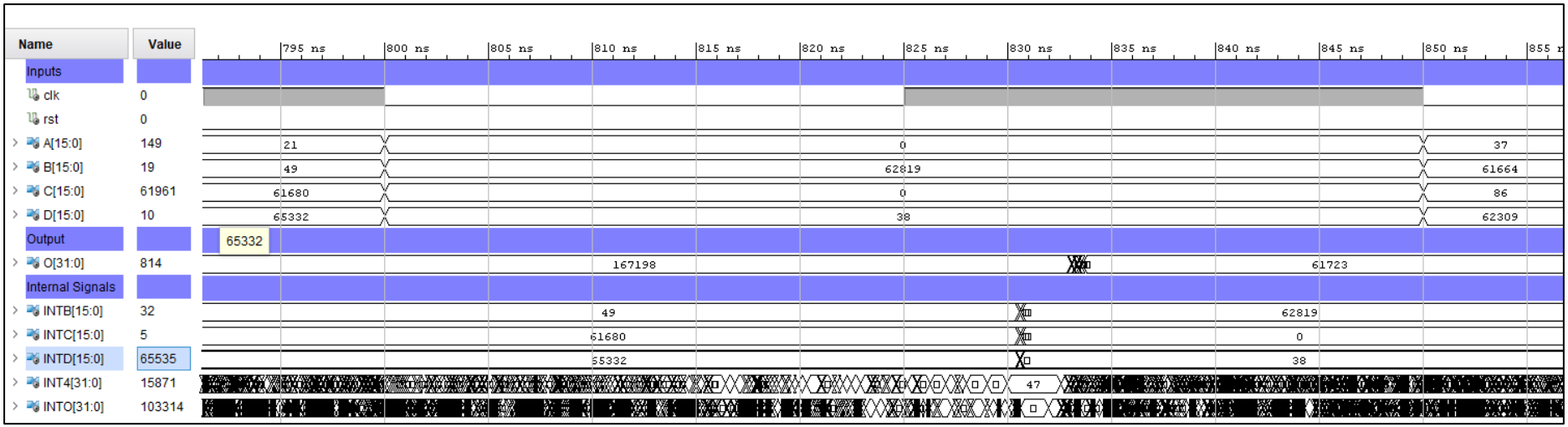
1.1.6 Print out a screenshot of the timing simulation window, zoomed in to display, in readable format, all inputs and the outputs, as well as INTO, in unsigned decimal format. Include the console output

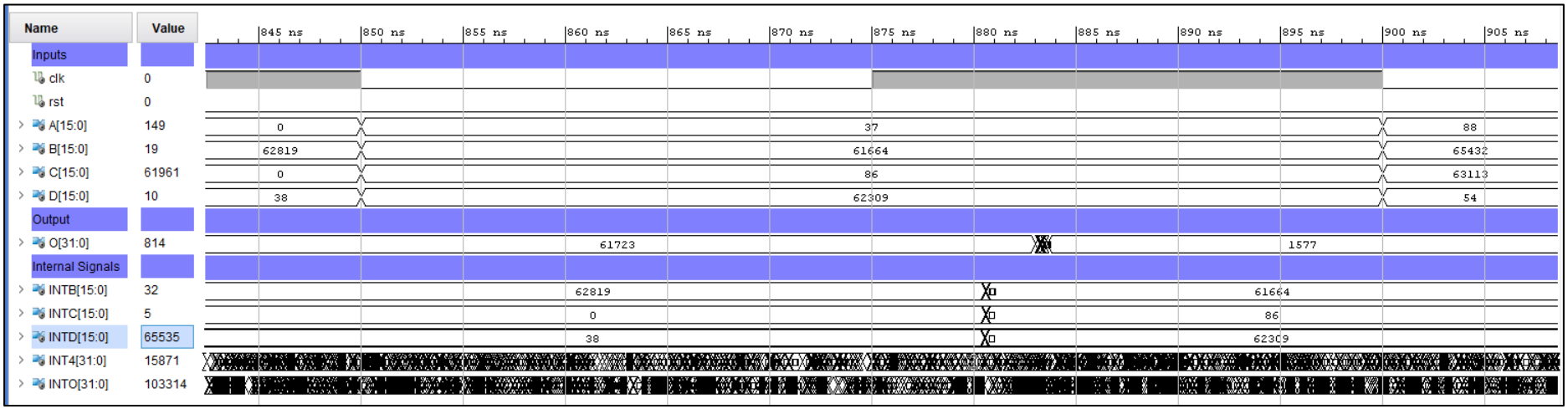


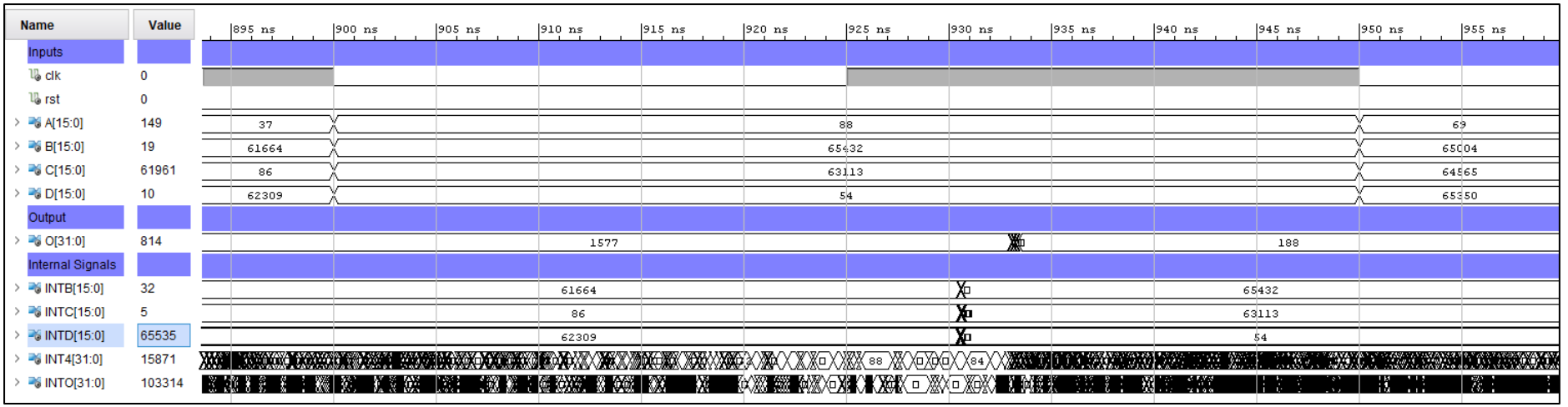

Name
Value
620 ns
630 ns
640 ns
650 ns
660 ns
670 ns
680 ns
Inputs
clk
1
rst
0
A[15:0]
149
67
53264
B[15:0]
19
151
32
C[15:0]
61961
4
5
D[15:0]
10
1
65535
Output
O[31:0]
814
5
Internal Signals
INTB[15:0]
32
0
151
INTC[15:0]
5
0
4
INTD[15:0]
65535
1
INT4[31:0]
14
0
805
INTO[31:0]
28
5
9
814

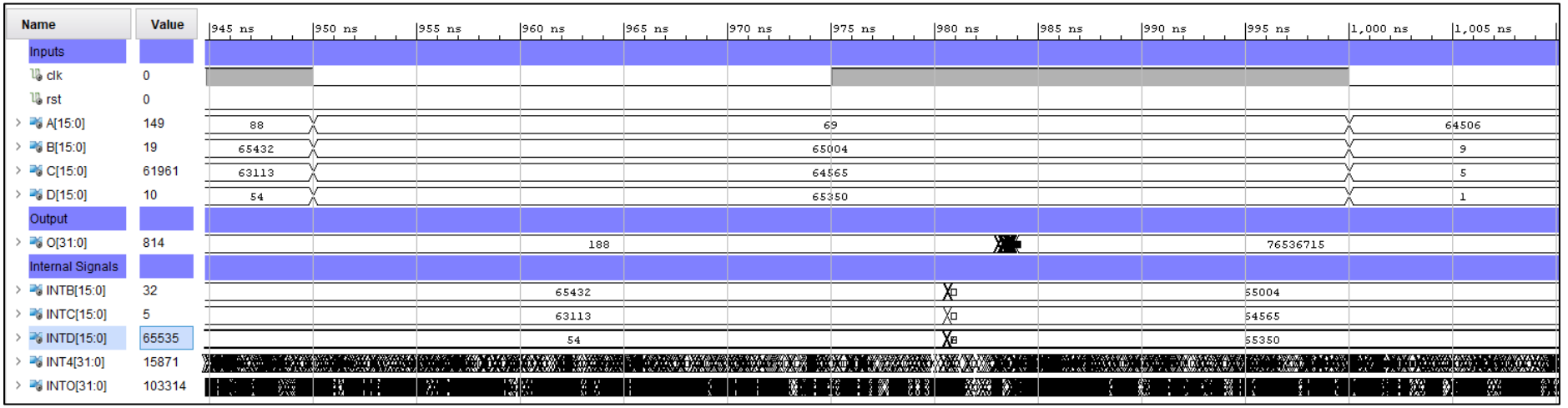

709.103 ns
Name
Value
695 ns
700 ns
705 ns
710 ns
715 ns
720 ns
725 ns
730 ns
735 ns
740 ns
745 ns
750 ns
Inputs
clk 0
rst 0
A[15:0] 149 53264 149 21
B[15:0] 19 32 19 49
C[15:0] 61961 5 61961 61680
D[15:0] 10 65535 10 65332
Output
O[31:0] 814 814 9
Internal Signals
INTB[15:0] 32 32 19
INTC[15:0] 5 5 61961
INTD[15:0] 65535 65535 10
INT4[31:0] 15871
INTO[31:0] 103314

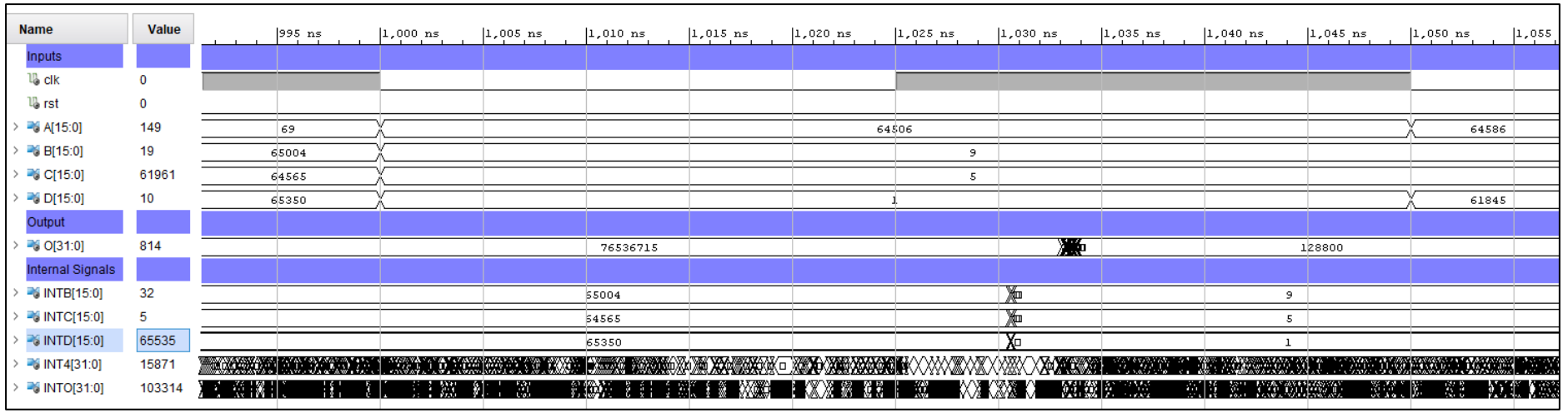

Name
Value
740 ns
745 ns
750 ns
755 ns
760 ns
765 ns
770 ns
775 ns
780 ns
785 ns
790 ns
795 ns
800 ns
Inputs
clk 0
rst 0
A[15:0] 149 149 21 0
B[15:0] 19 19 49 62819
C[15:0] 61961 61961 61680 0
D[15:0] 10 10 65332 38
Output
O[31:0] 814 9 167198
Internal Signals
9
INTB[15:0] 32 19 49
INTC[15:0] 5 61961 61680
INTD[15:0] 65535 10 65332
INT4[31:0] 15871
INTO[31:0] 103314

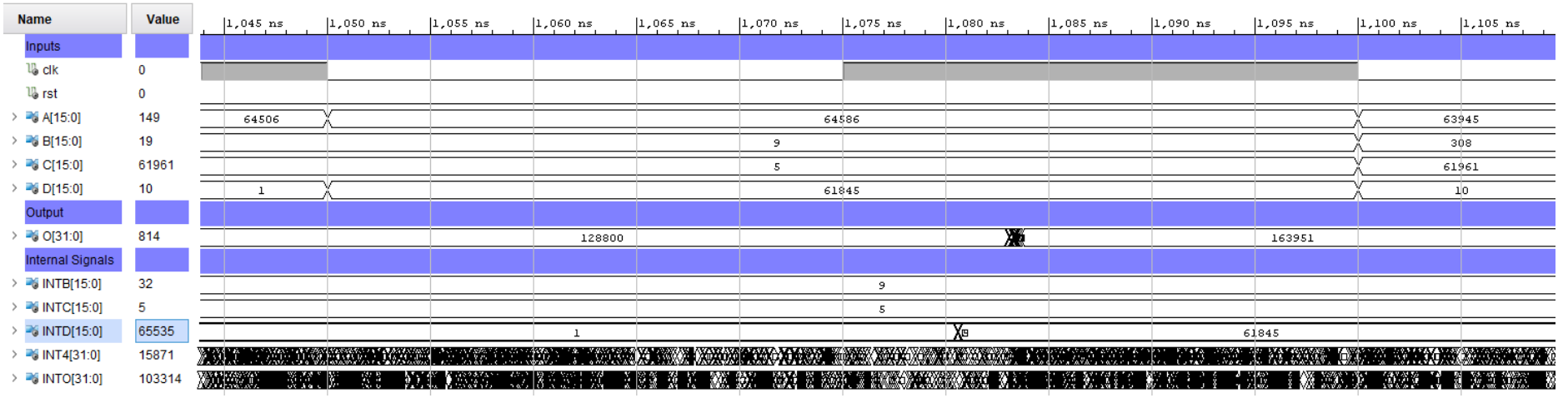

Name
Value
795 ns
800 ns
805 ns
810 ns
815 ns
820 ns
825 ns
830 ns
835 ns
840 ns
845 ns
850 ns
Inputs
clk 0
rst 0
A[15:0] 149
21
0
37
B[15:0] 19
49
62819
61664
C[15:0] 61961
61680
0
86
D[15:0] 10
65332
38
62309
Output
65332
O[31:0] 814
167198
61723
Internal Signals
INTB[15:0] 32
49
62819
INTC[15:0] 5
61680
0
INTD[15:0] 65535
65332
38
INT4[31:0] 15871
47
INTO[31:0] 103314

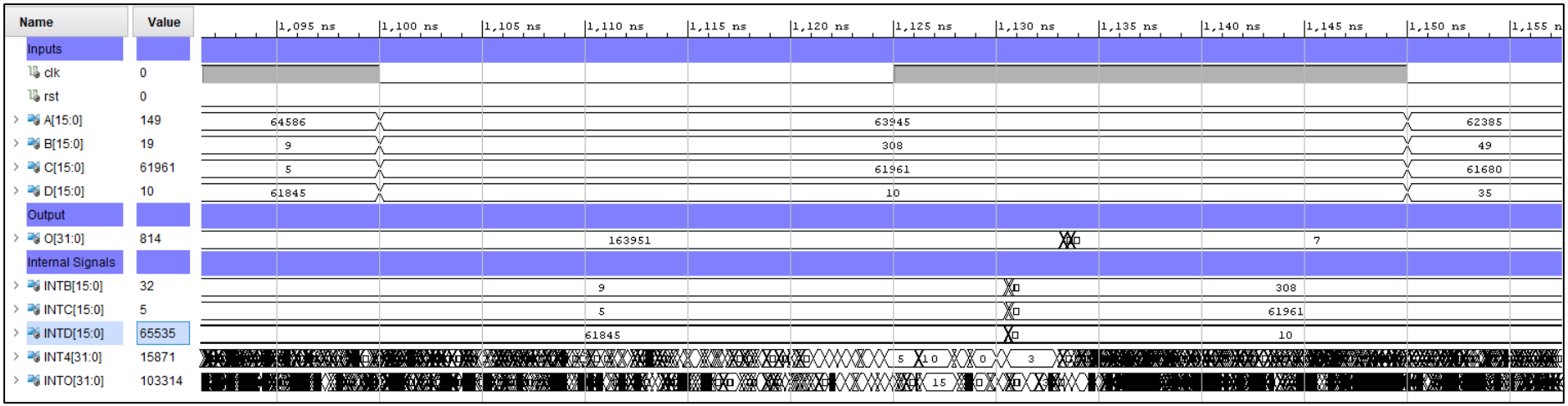

Name
Value
845 ns
850 ns
855 ns
860 ns
865 ns
870 ns
875 ns
880 ns
885 ns
890 ns
895 ns
900 ns
905 ns
Inputs
clk 0
rst 0
A[15:0] 149
0
37
88
B[15:0] 19
62819
61664
65432
C[15:0] 61961
0
86
63113
D[15:0] 10
38
62309
54
Output
O[31:0] 814
61723
1577
Internal Signals
INTB[15:0] 32
62819
61664
INTC[15:0] 5
0
86
INTD[15:0] 65535
38
62309
INT4[31:0] 15871
INTO[31:0] 103314

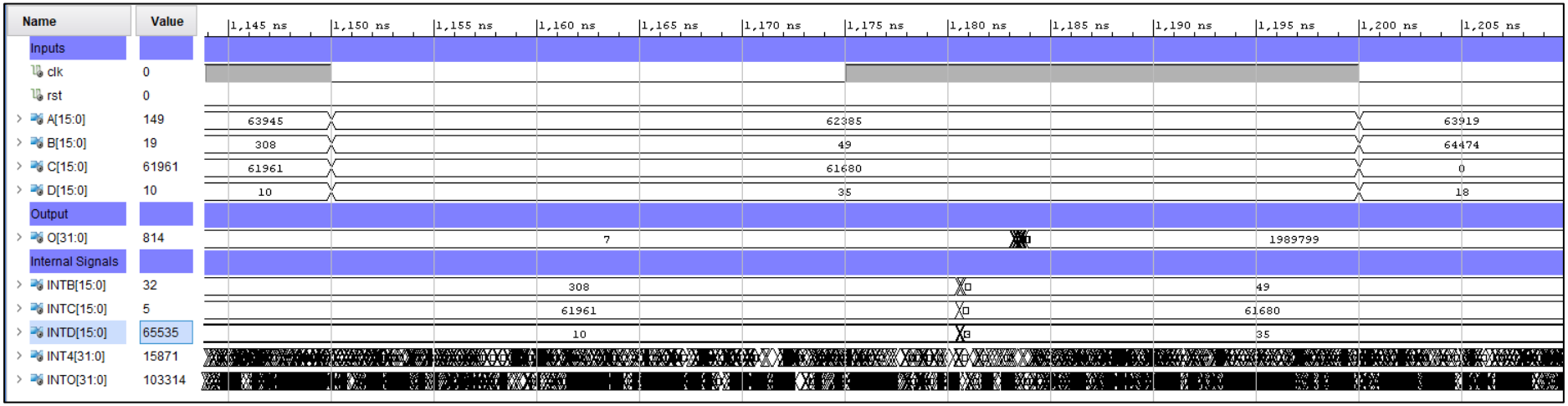

Name
Value
895 ns
900 ns
905 ns
910 ns
915 ns
920 ns
925 ns
930 ns
935 ns
940 ns
945 ns
950 ns
955 ns
Inputs
clk 0
rst 0
A[15:0] 149
37
88
69
B[15:0] 19
61664
65432
65004
C[15:0] 61961
86
63113
64565
D[15:0] 10
62309
54
65350
Output
O[31:0] 814
1577
188
Internal Signals
INTB[15:0] 32
61664
65432
INTC[15:0] 5
86
63113
INTD[15:0] 65535
62309
54
INT4[31:0] 15871
INTO[31:0] 103314

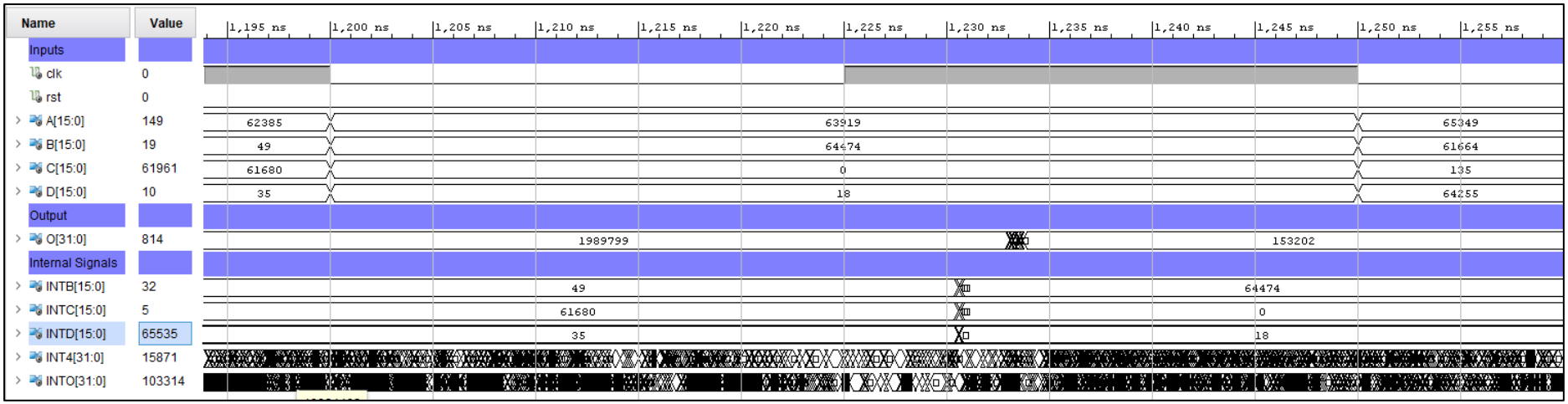

Name
Value
945 ns
950 ns
955 ns
960 ns
965 ns
970 ns
975 ns
980 ns
985 ns
990 ns
995 ns
1,000 ns
1,005 ns
Inputs
clk 0
rst 0
A[15:0] 149
88
69
64506
B[15:0] 19
65432
65004
9
C[15:0] 61961
63113
64565
5
D[15:0] 10
54
65350
1
Output
O[31:0] 814
188
76536715
Internal Signals
INTB[15:0] 32
65432
55004
INTC[15:0] 5
63113
64565
INTD[15:0] 65535
54
55350
INT4[31:0] 15871
INTO[31:0] 103314

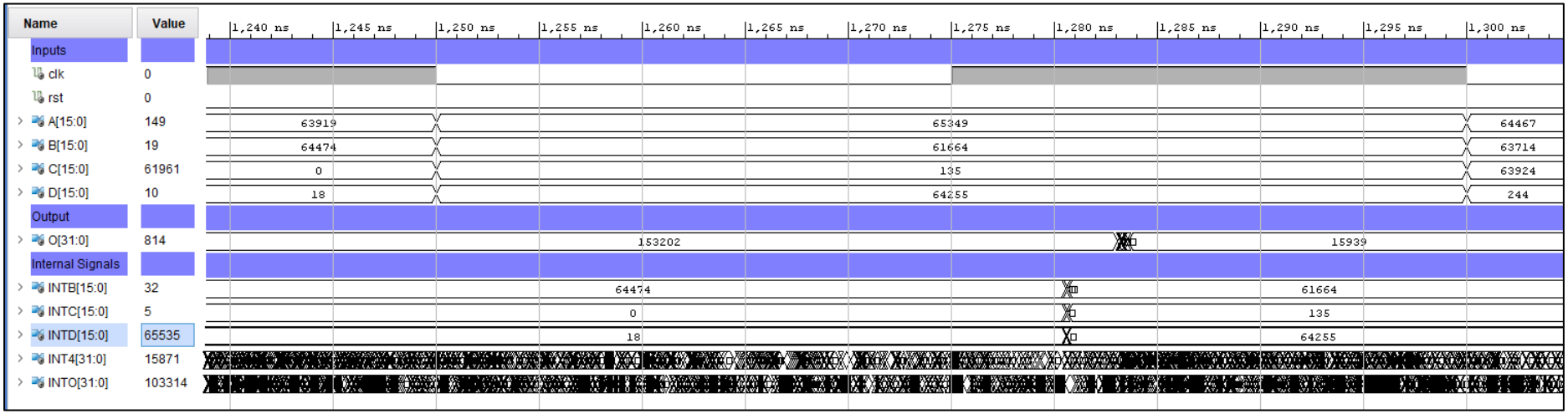

Name
Value
995 ns
1,000 ns
1,005 ns
1,010 ns
1,015 ns
1,020 ns
1,025 ns
1,030 ns
1,035 ns
1,040 ns
1,045 ns
1,050 ns
1,055
Inputs
clk 0
rst 0
A[15:0] 149 69 64506 64586
B[15:0] 19 65004 9
C[15:0] 61961 64565 5
D[15:0] 10 65350 1 61845
Output
O[31:0] 814 76536715 128800
Internal Signals
INTB[15:0] 32 65004 9
INTC[15:0] 5 64565 5
INTD[15:0] 65535 65350 1
INT4[31:0] 15871
INTO[31:0] 103314

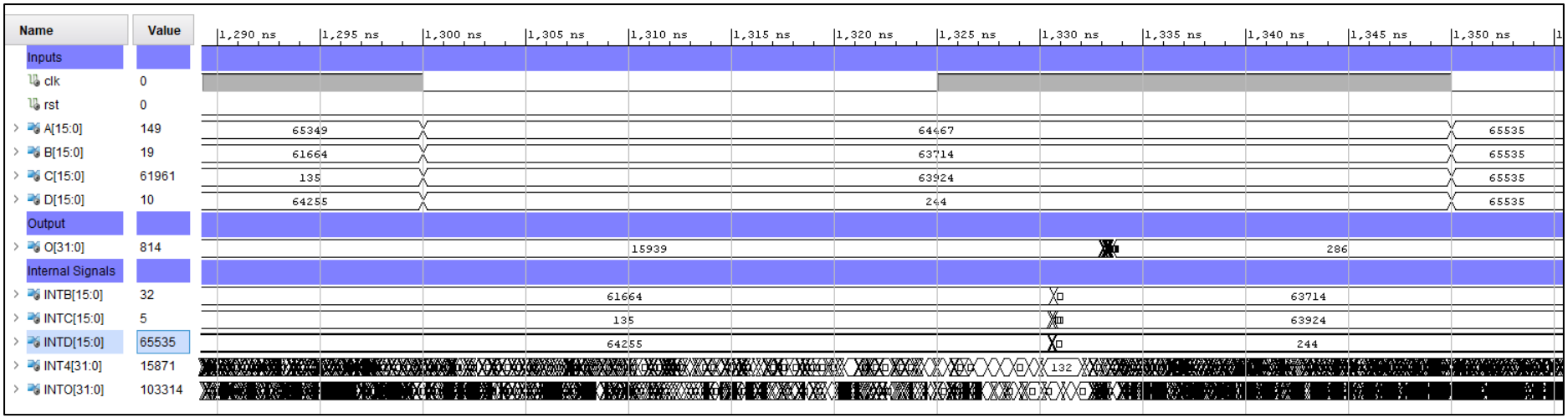

Name
Value
1,045 ns
1,050 ns
1,055 ns
1,060 ns
1,065 ns
1,070 ns
1,075 ns
1,080 ns
1,085 ns
1,090 ns
1,095 ns
1,100 ns
1,105 ns
Inputs
clk 0
rst 0
A[15:0] 149 64506 64586 63945
B[15:0] 19 9 308
C[15:0] 61961 5 61961
D[15:0] 10 1 61845 10
Output
O[31:0] 814 128800 163951
Internal Signals
INTB[15:0] 32 9
INTC[15:0] 5 5
INTD[15:0] 65535 1 61845
INT4[31:0] 15871
INTO[31:0] 103314

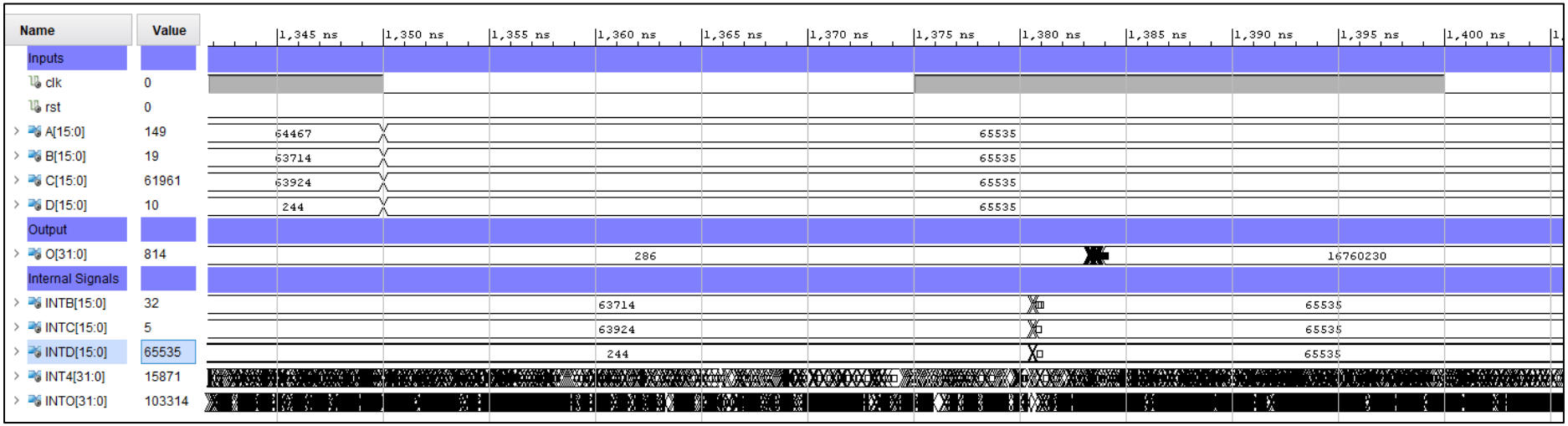

Name
Value
1,095 ns
1,100 ns
1,105 ns
1,110 ns
1,115 ns
1,120 ns
1,125 ns
1,130 ns
1,135 ns
1,140 ns
1,145 ns
1,150 ns
Inputs
clk 0
rst 0
A[15:0] 149 64586 63945 62385
B[15:0] 19 9 308 49
C[15:0] 61961 5 61961 61680
D[15:0] 10 61845 10 35
Output
O[31:0] 814 163951 7
Internal Signals
INTB[15:0] 32 9 308
INTC[15:0] 5 5 61961
INTD[15:0] 65535 61845 10
INT4[31:0] 15871
INTO[31:0] 103314

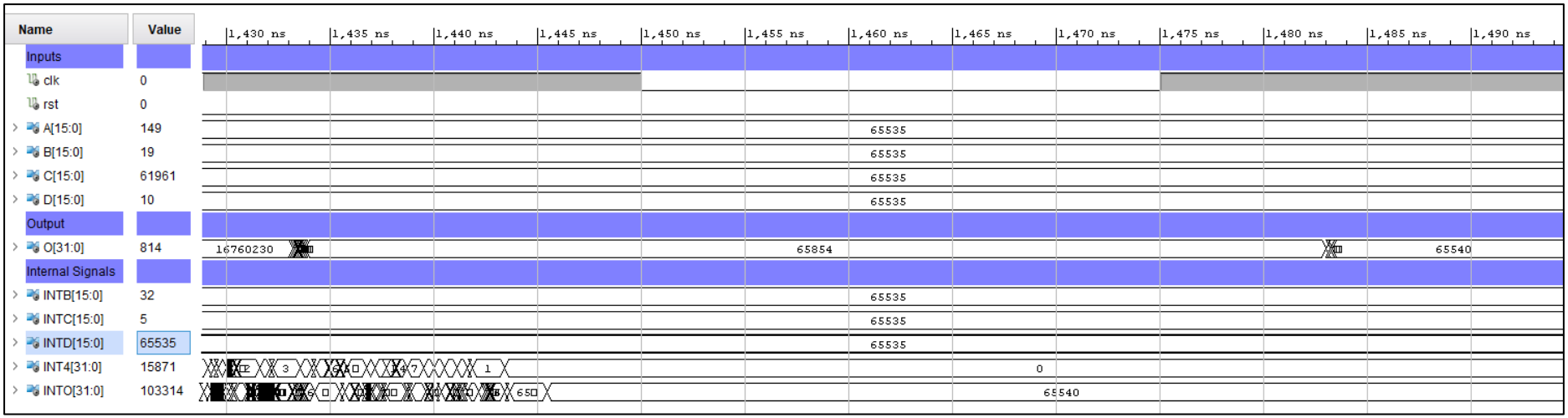

Name
Value
1,145 ns
1,150 ns
1,155 ns
1,160 ns
1,165 ns
1,170 ns
1,175 ns
1,180 ns
1,185 ns
1,190 ns
1,195 ns
1,200 ns
1,205 ns
Inputs
clk 0
rst 0
A[15:0] 149 63945 62385 63919
B[15:0] 19 308 49 64474
C[15:0] 61961 61961 61680 0
D[15:0] 10 10 35 18
Output
O[31:0] 814 7 1989799
Internal Signals
INTB[15:0] 32 308 49
INTC[15:0] 5 61961 61680
INTD[15:0] 65535 10 35
INT4[31:0] 15871
INTO[31:0] 103314

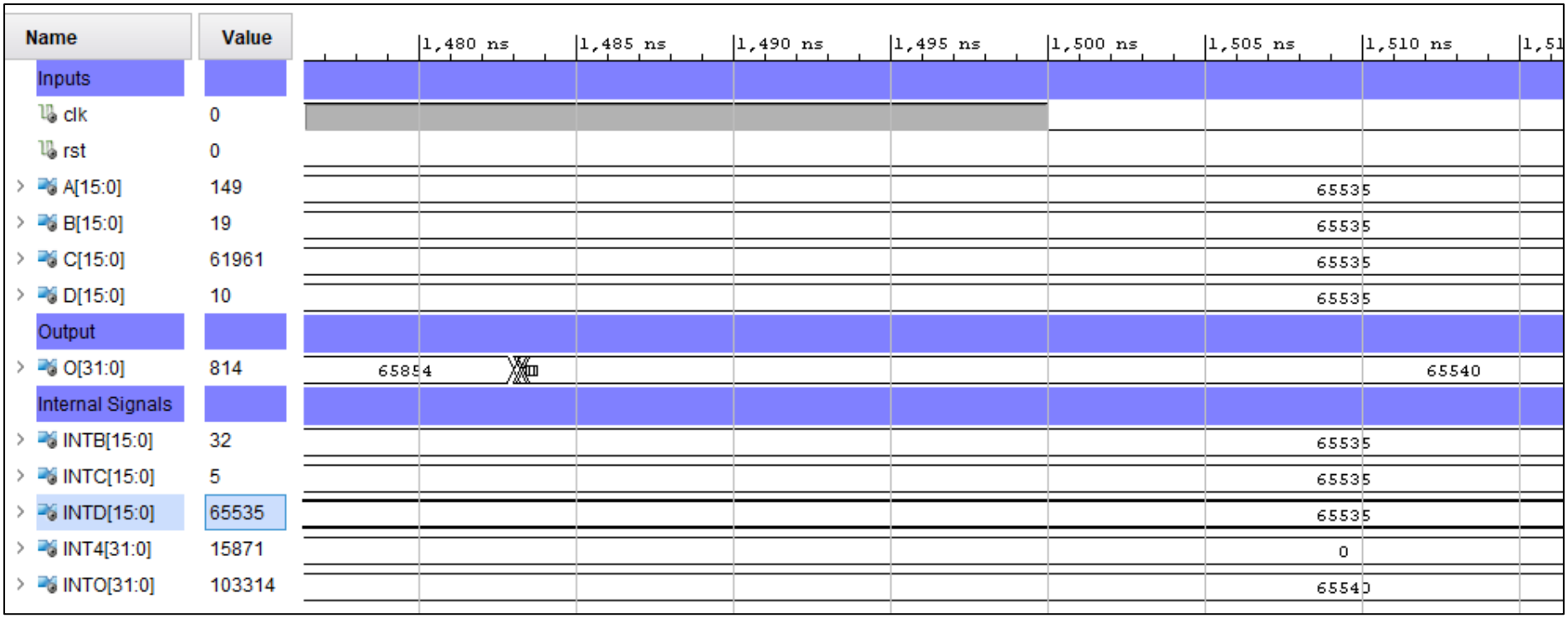

Name
Value
1,195 ns
1,200 ns
1,205 ns
1,210 ns
1,215 ns
1,220 ns
1,225 ns
1,230 ns
1,235 ns
1,240 ns
1,245 ns
1,250 ns
1,255 ns
Inputs
clk 0
rst 0
A[15:0] 149 62385 63919 65349
B[15:0] 19 49 64474 61664
C[15:0] 61961 61680 0 135
D[15:0] 10 35 18 64255
Output
O[31:0] 814 1989799 153202
Internal Signals
INTB[15:0] 32 49 64474
INTC[15:0] 5 61680 0
INTD[15:0] 65535 35 18
INT4[31:0] 15871
INTO[31:0] 103314


Name
Value
1,240 ns
1,245 ns
1,250 ns
1,255 ns
1,260 ns
1,265 ns
1,270 ns
1,275 ns
1,280 ns
1,285 ns
1,290 ns
1,295 ns
1,300 ns
Inputs
clk 0
rst 0
A[15:0] 149 63919 65349 64467
B[15:0] 19 64474 61664 63714
C[15:0] 61961 0 135 63924
D[15:0] 10 18 64255 244
Output
O[31:0] 814 153202 15939
Internal Signals
INTB[15:0] 32 64474 61664
INTC[15:0] 5 0 135
INTD[15:0] 65535 18 64255
INT4[31:0] 15871
INTO[31:0] 103314


Name
Value
1,290 ns
1,295 ns
1,300 ns
1,305 ns
1,310 ns
1,315 ns
1,320 ns
1,325 ns
1,330 ns
1,335 ns
1,340 ns
1,345 ns
1,350 ns
Inputs
clk 0
rst 0
A[15:0] 149 65349 64467 65535
B[15:0] 19 61664 63714 65535
C[15:0] 61961 135 63924 65535
D[15:0] 10 64255 244 65535
Output
O[31:0] 814 15939 286
Internal Signals
INTB[15:0] 32 61664 63714
INTC[15:0] 5 135 63924
INTD[15:0] 65535 64255 244
INT4[31:0] 15871 132
INTO[31:0] 103314


Name
Value
1,345 ns
1,350 ns
1,355 ns
1,360 ns
1,365 ns
1,370 ns
1,375 ns
1,380 ns
1,385 ns
1,390 ns
1,395 ns
1,400 ns
Inputs
clk 0
rst 0
A[15:0] 149 64467 65535
B[15:0] 19 63714 65535
C[15:0] 61961 63924 65535
D[15:0] 10 244 65535
Output
O[31:0] 814 286 16760230
Internal Signals
INTB[15:0] 32 63714 65535
INTC[15:0] 5 63924 65535
INTD[15:0] 65535 244 65535
INT4[31:0] 15871
INTO[31:0] 103314


Name
Value
1,430 ns
1,435 ns
1,440 ns
1,445 ns
1,450 ns
1,455 ns
1,460 ns
1,465 ns
1,470 ns
1,475 ns
1,480 ns
1,485 ns
1,490 ns
Inputs
clk 0
rst 0
A[15:0] 149
B[15:0] 19
C[15:0] 61961
D[15:0] 10
Output
O[31:0] 814
Internal Signals
INTB[15:0] 32
INTC[15:0] 5
INTD[15:0] 65535
INT4[31:0] 15871
INTO[31:0] 103314
65535
16760230
65854
65540
0


Name
Value
1,480 ns
1,485 ns
1,490 ns
1,495 ns
1,500 ns
1,505 ns
1,510 ns
Inputs
clk 0
rst 0
A[15:0] 149
B[15:0] 19
C[15:0] 61961
D[15:0] 10
Output
O[31:0] 814
Internal Signals
INTB[15:0] 32
INTC[15:0] 5
INTD[15:0] 65535
INT4[31:0] 15871
INTO[31:0] 103314
65535
65535
65535
65535
65535
65535
65535
0
65540
65540

```
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 700 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 9
Predicted value
O: 12

Time: 750 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 167198
Predicted value
O: 179736

Time: 800 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61723
Predicted value
O: 61731
```

```
Time: 850 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
Error: Assertion violation
Time: 900 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 1577
Predicted value
O: 5

Time: 900 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error: Assertion violation
Time: 950 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 188
Predicted value
O: 176

Time: 950 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76536715
Predicted value
O: 76537378

Time: 1 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Algorithm_Lab_2A_tb_time_impl' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:46 ; elapsed = 00:01:06 . Memory (MB): peak = 1801.133 ; gain
= 1000.711
run 5 us
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
Error: Assertion violation
Time: 1050 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test_vectors value 7
```

```
for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128800
Predicted value
O: 128793

Time: 1050 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 163951
Predicted value
O: 193573

Time: 1100 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 7
Predicted value
O: 13

Time: 1150 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error: Assertion violation
Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989799
Predicted value
O: 1989548

Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error:
test_vectors value 11
```

```
for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153202
Predicted value
O: 153384

Time: 1250 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
Error: Assertion violation
Time: 1300 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 15939
Predicted value
O: 10658

Time: 1300 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error: Assertion violation
Time: 1350 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 286
Predicted value
O: 272

Time: 1350 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 145: Timing violation in
scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error: Assertion violation
Time: 1400 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16760230
Predicted value
O: 16756745
```

```
Time: 1400 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
WARNING: "C:\Xilinx\Vivado\2017.4\data/verilog/src/unisims/FDRE.v" Line 142: Timing violation in scope
Error: Assertion violation
Time: 1450 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 65854
Predicted value
O: 65540

Time: 1450 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

1.1.7

Comment on and explain the output of the simulation, particularly the behaviour of INTO and of the output, relating it to the material covered in the lectures.

The Combinational logic that leads the computation of the equation does not have enough time to process all of the larger sums this is due to the critical paths minimum time required is not met due to the simulated clock period being to low. This low timing value forces the output register to input (INTO)the current value of the combinational logic which is not correct in most cases this causes the output of the register to be incorrect causing the circuit to be invalid. These incorrect values held within the registers cause setup and hold time violations.

Task 2

1.2.1

Tcl Console | Messages | Log | Reports | **Design Runs** | Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete!	3.414	0.000	0.700	0.000	0.000	0.110	0	886	96	0.00	0	0

Figure 2 85ns period xdc file

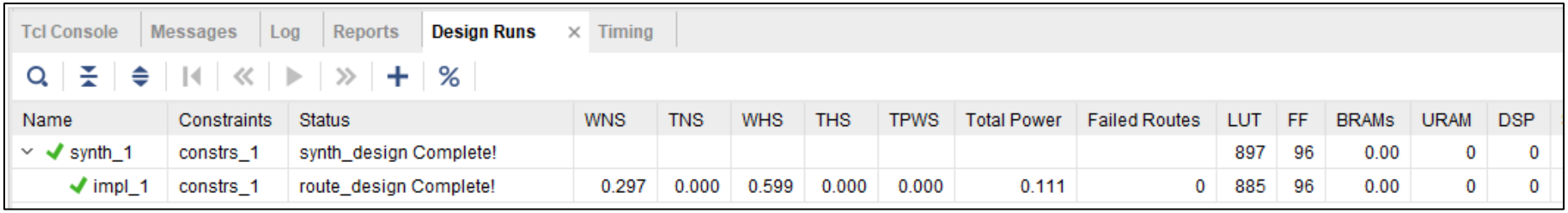
Time asked for = 85ns

Worst Time Slack = 3.414

Critical path time = 81.586ns= 85ns - 3.414ns

Maximum frequency = $\frac{1}{Critical\ Path\ Time} = \frac{1}{81.586ns}$ = 12257005 Hz

Calculate frequency



Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.297	0.000	0.599	0.000	0.000	0.111	0	885	96	0.00	0	0

Figure 3 80ns period xdc file

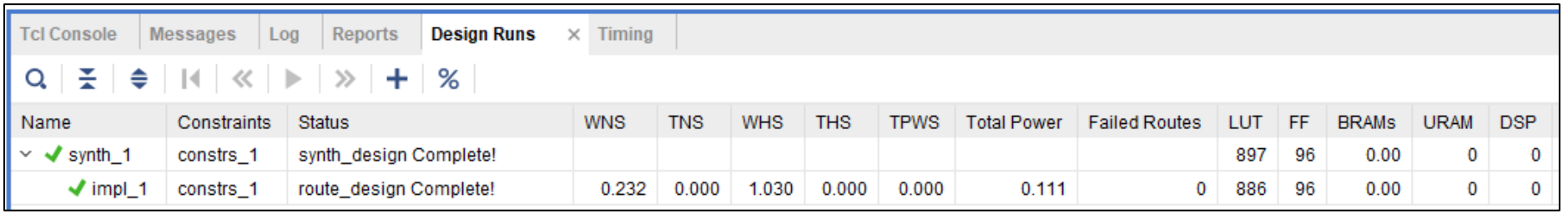
Calculate frequency

Time asked for = 80ns

Worst Time Slack = 0.297

Critical path time = 79.703 = 80ns – 0.297ns

Maximum frequency = $\frac{1}{Critical\ Path\ Time} = \frac{1}{79.703ns}$ = 1254579 Hz



Tcl Console | Messages | Log | Reports | **Design Runs** | Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.232	0.000	1.030	0.000	0.000	0.111	0	886	96	0.00	0	0

Figure 4 75ns period xdc file

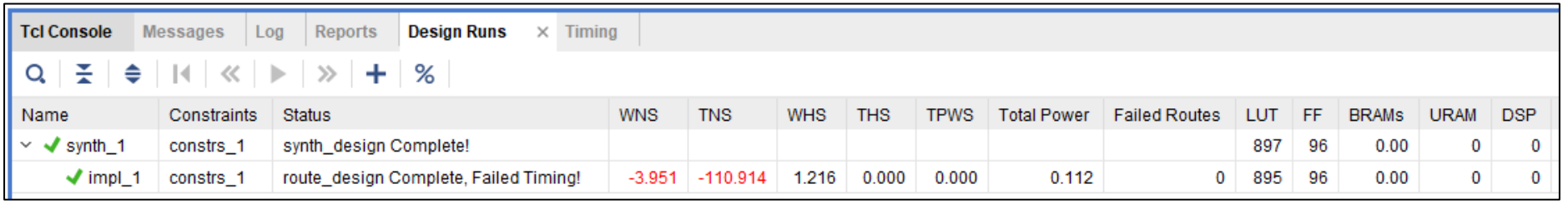
Calculate frequency

Time asked for = 75ns

Worst Time Slack = 0.232

Critical path time = 74.768 = 75ns – 0.232ns

Maximum frequency = $\frac{1}{Critical\ Path\ Time} = \frac{1}{74.768ns}$ = 13374705 Hz



Tcl Console | Messages | Log | Reports | **Design Runs** | Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete, Failed Timing!	-3.951	-110.914	1.216	0.000	0.000	0.112	0	895	96	0.00	0	0

Figure 5 70ns period xdc file

Failed to process due to timing constraints.

why the WNS changes and what happens when the timing requirements are not met

Relate this to what you see in the timing simulations.

THE Worst Negative Slack changes because the implementation of the gates on the chip, as you request less time the software is required to be more efficient, in this case the physical position of the gates move closer together reducing the length of the connections optimizing the circuit further than previously within the combinational logic specifically. When the Timing requirements are not met the WNS & TNS give negative values as in Figure 5 70ns period xdc filethis means that the circuit cannot be optimised for the desired time.

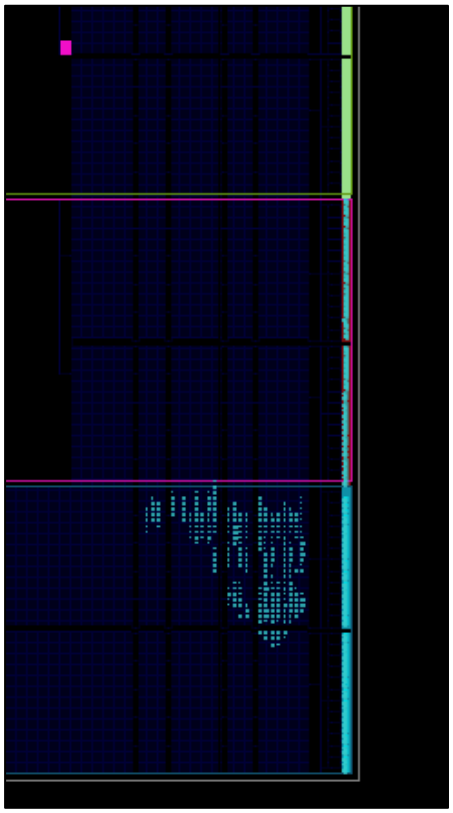


Figure 7 85 ns

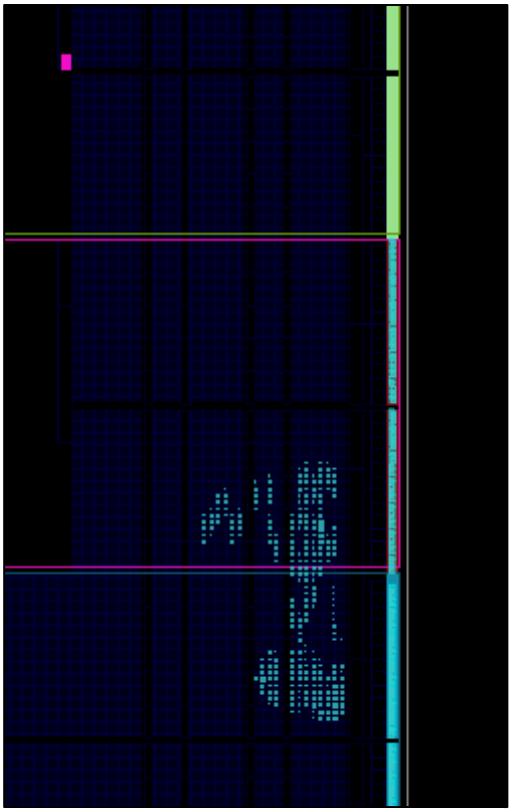


Figure 6 75ns

In the timing simulations such as section 1.1.6 show what can happen when the timing simulations do not have enough time to process the values through the combinational circuit. Unfortunately, the time is not enough in most cases so the output register takes in the current value of the internal output value at the time of the rising clock edge but that value is not currently stable as the combinational circuit is still processing the correct values. This causes the output register to output the wrong values making the circuit invalid.

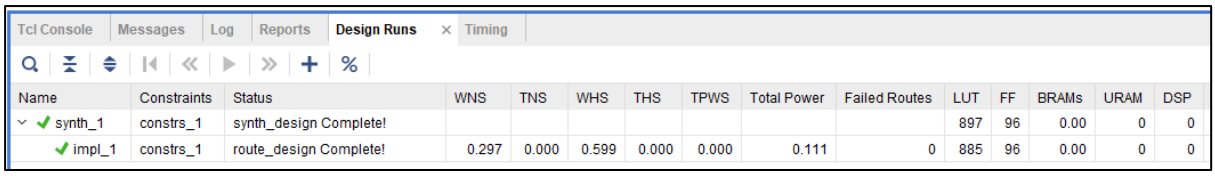
Task 3

1.3.1 Print out the modified VHDL code. Add comments within the VHDL to illustrate its operation and your modifications (in particular, their effect on the critical path). Print out a screenshot of the "Design Runs" tab, showing all columns up to "DSP", and comment on the comparison between the WNS value here and in the pre-modification case

```
-- Company: University of York
-- Engineer: Gianluca Tempesti
--
-- Create Date:    11:57:50 10/25/2012
-- Design Name:
-- Module Name:    Algorithm - Behavioral
-- Project Name:   Digital Engineering Labs 2-3
-- Target Devices: Any device - Tested on XC6SLX45-3CSG32
-- Tool versions:  Tested on ISE 14.2 / Vivado 2017.4.1
-- Description:    Base circuit for pipeline labs
--
-- Revision:
-- Revision 0.01 - File Created
-- Revision 0.02 - File updated 04/12/2015
-- Revision 0.03 - Vivado update and test
-- Revision 0.04 - re-arranged of first and final additions30/01/2020 OAF-S
-- Additional Comments:
----------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use work.DigEng.all;
-- Algorithm entity
-- Synchronous calculator of the equation
-- O <= (A*3 + B*C)/D + C +5
-- 6 inputs, standard clk and reset
-- Inputs A, B, C, D std logic vector inputs of values
-- to computate.
-- output O is result of the equation.
-- 5 registers total
-- 4 at innputs one for each value input A, B, C and D
-- 1 at output O
-- Computation of equation takes 2 clk clyes
-- first to register inputs
-- second to register at output
--UPDATE reduces critical path length:
-- old critical path had 2 additions in sequential order
--before output reg while the new crtitcal path moves one
-- of the additions from the the critical path and is
-- computed earlier
entity algorithm is
    generic (data_size : integer := 16);
    Port ( A : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           B : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           C : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           D : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           O : out  STD_LOGIC_VECTOR (data_size*2-1 downto 0);
           clk : in  STD_LOGIC;
           rst : in  STD_LOGIC);
end algorithm;
```

```
architecture Behavioral of algorithm is
-- internal input signals "data_size" bits long to match inputs
signal INTA, INTB, INTC, INTD : UNSIGNED (data_size-1 downto 0);
-- internal input signals "data_size" +1 bits long
-- extra bit to account for multiplication of INTA by 3
signal INT1 : UNSIGNED (data_size+1 downto 0);
-- internal input signals "data_size"-1 bits long
-- this allows for multiplication and division of
-- any value of the same vector size
signal INT2 : UNSIGNED (data_size*2-1 downto 0);
signal INT3 : UNSIGNED (data_size*2-1 downto 0);
signal INT4 : UNSIGNED (data_size*2-1 downto 0);
-- original INT5 signal
--signal INT5 : UNSIGNED (data_size*2-1 downto 0);
--#################################
-- modified INT5 signal
-- INT5 data size reduced from 32 bit to the required 17 bits
signal INT5 : UNSIGNED (data_size downto 0);
--#################################
signal INTO : UNSIGNED (data_size*2-1 downto 0);

begin

-- setup for individual input registers for inputs A,B, C & D
-- All Synchronous with reset to zero when reset signal active,
-- NO enable signals required.
input_regs: process (clk) is
begin
  if rising_edge(clk) then
  -- resets internal signals below to zero
    if rst = '1' then
      INTA <= (others => '0');
      INTB <= (others => '0');
      INTC <= (others => '0');
--    INTD <= (0 => '1', others => '0');  -- aggregate notation
      INTD <= to_unsigned(1,INTD'length); -- type conversion notation
    else
    -- connects inputs to internal signal values
      INTA <= unsigned(A);
      INTB <= unsigned(B);
      INTC <= unsigned(C);
      INTD <= unsigned(D);
    end if;
  end if;
end process input_regs;

-- equation maths defined per internal signals
-- INT1 result of INTA multiplied by 3
INT1 <= INTA * to_unsigned(3, 2);
-- INT2 result of INTB multiplied INTC
INT2 <= INTB * INTC;
-- INT3 equal to sum of  INT1 & INT2
INT3 <= INT1 + INT2;
-- INT4 result of  INT3 divided by INTD
INT4 <= INT3 / INTD;
```

```
-- original INT5 connection
--INT5 <= INTC + INT4;
--INTO <= INT5 + to_unsigned(5, INT5'length);

--###################################
-- modified INT5 signal connection
-- edited to match Task 3
-- unsigned value 5 added to C
INT5 <= INTC + to_unsigned(5, INT5'length);
--###################################
--result of usigned 5 + INTC added to INT5
INTO <= INT5 + INT4;

-- output register.
-- synchronous.
-- output = 0 at rising clk edge
-- when input reset is active.
-- output = INTO at rising clk edge.
output_regs: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
      O <= (others => '0');
    else
      O <= std_logic_vector(INTO);
    end if;
  end if;
end process output_regs;

end Behavioral;
```



Tcl Console | Messages | Log | Reports | **Design Runs** | Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.297	0.000	0.599	0.000	0.000	0.111	0	885	96	0.00	0	0

and comment on the comparison between the WNS value here and in the pre-modification case.

No change in any of the values this is most likely due to the fact that adders are extremely fast in processing the circuit. If it was a divider or a multiplier that had moved from the critical path the WNS value would change.