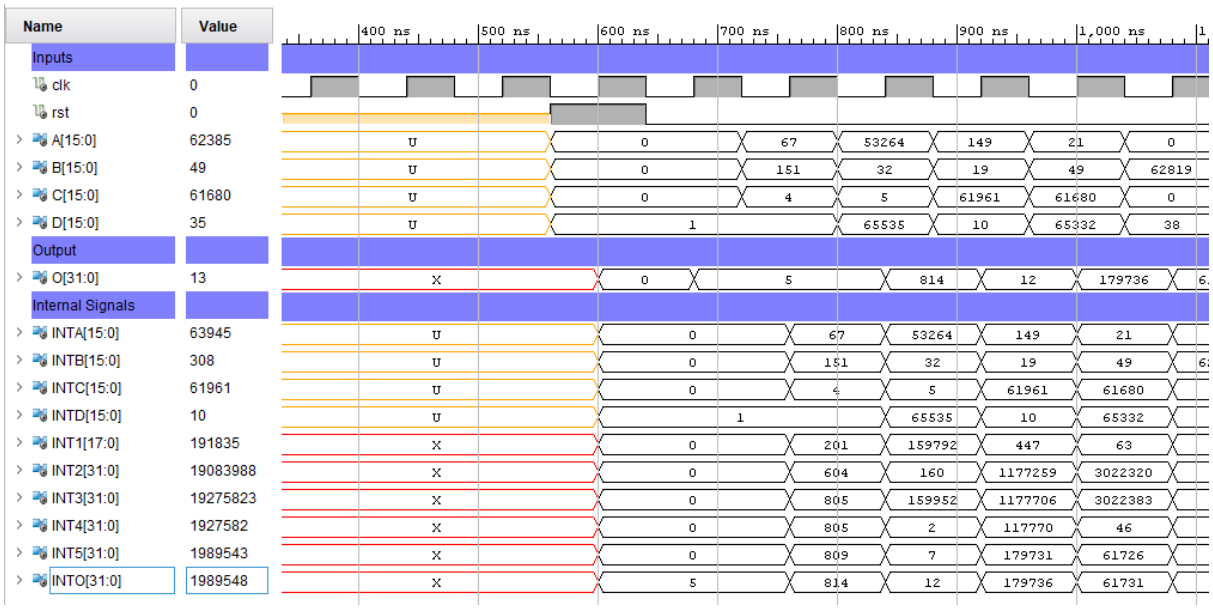
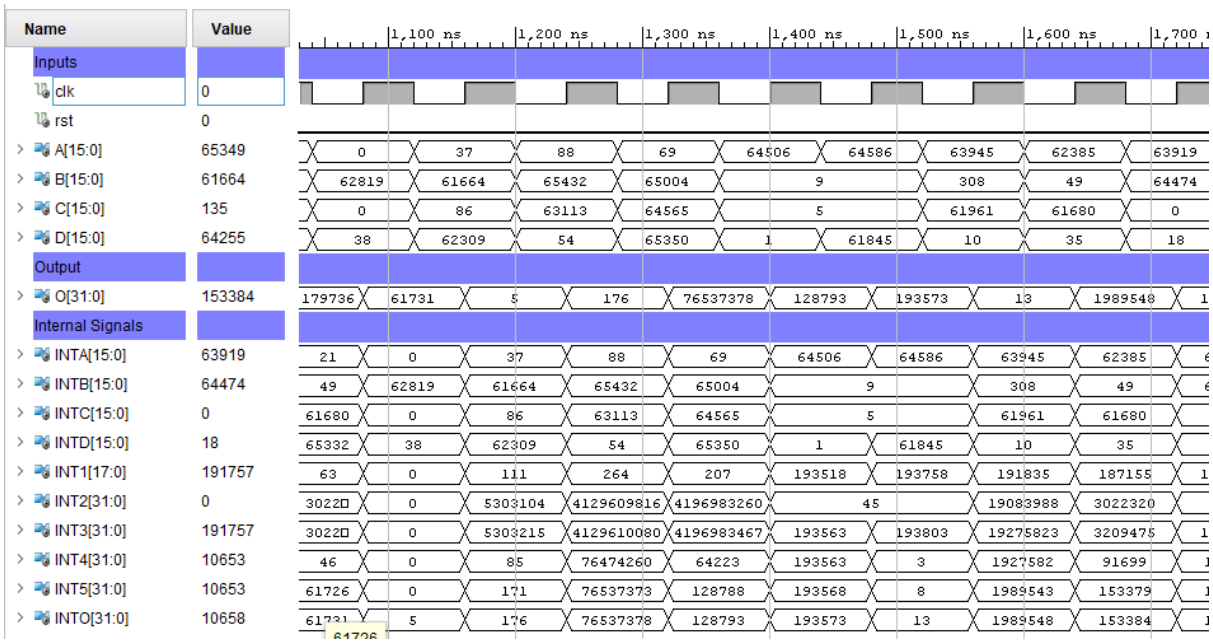
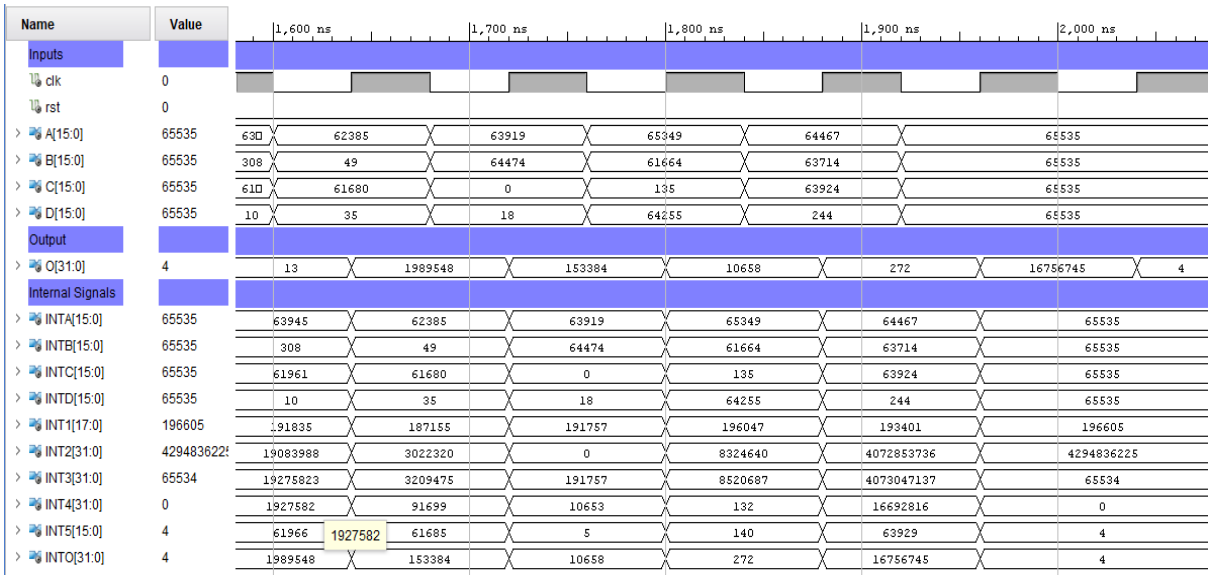
Lab 3 Task 1

2.1.1






Name
Value
1,600 ns
1,700 ns
1,800 ns
1,900 ns
2,000 ns
Inputs
clk 0
rst 0
A[15:0] 65535 63□ 62385 63919 65349 64467 65535
B[15:0] 65535 308 49 64474 61664 63714 65535
C[15:0] 65535 61□ 61680 0 135 63924 65535
D[15:0] 65535 10 35 18 64255 244 65535
Output
O[31:0] 4 13 1989548 153384 10658 272 16756745 4
Internal Signals
INTA[15:0] 65535 63945 62385 63919 65349 64467 65535
INTB[15:0] 65535 308 49 64474 61664 63714 65535
INTC[15:0] 65535 61961 61680 0 135 63924 65535
INTD[15:0] 65535 10 35 18 64255 244 65535
INT1[17:0] 196605 191835 187155 191757 196047 193401 196605
INT2[31:0] 4294836225 19083988 3022320 0 8324640 4072853736 4294836225
INT3[31:0] 65534 19275823 3209475 191757 8520687 4073047137 65534
INT4[31:0] 0 1927582 91699 10653 132 16692816 0
INT5[15:0] 4 61966 1927582 61685 5 140 63929 4
INTO[31:0] 4 1989548 153384 10658 272 16756745 4

```
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 880 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 960 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
INFO: [USF-XSim-96] XSim completed. Design snapshot
'Algorithm_Lab_2A_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:04 ; elapsed = 00:00:05 .
Memory (MB): peak = 826.105 ; gain = 4.074
run 5 us
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736
```

```
Time: 1040 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731

Time: 1120 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 1280 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378
```

```
Time: 1360 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793

Time: 1440 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 1520 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 1600 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548
```

```
Time: 1680 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153384
Predicted value
O: 153384

Time: 1760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 1840 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 1920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745
```

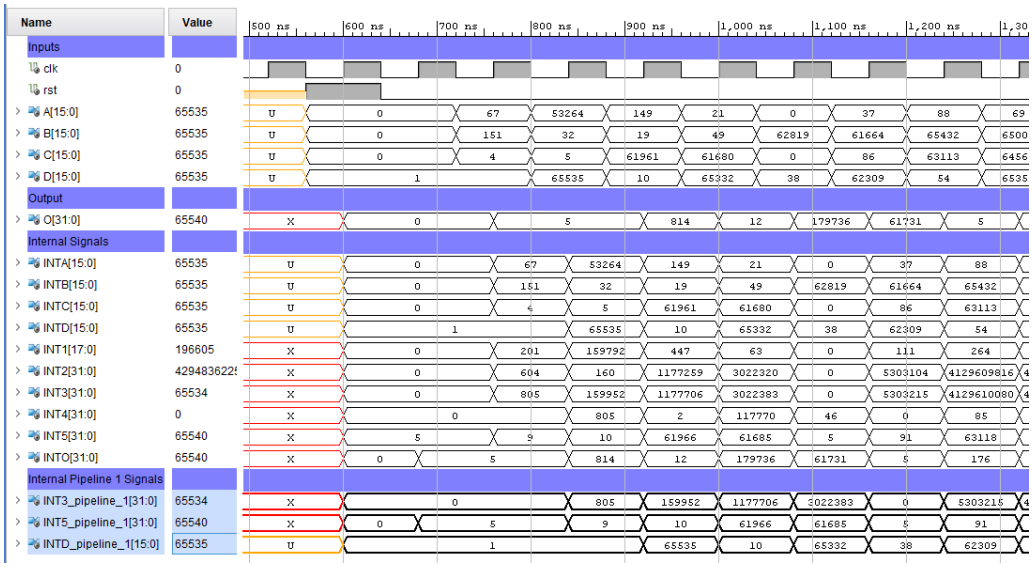
```
Time: 2 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4

Time: 2080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

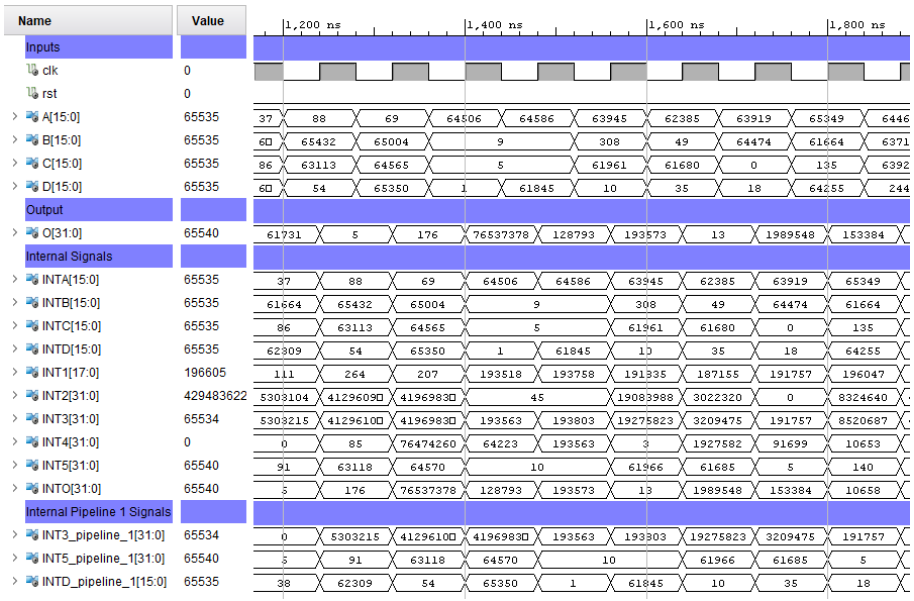
2.1.2

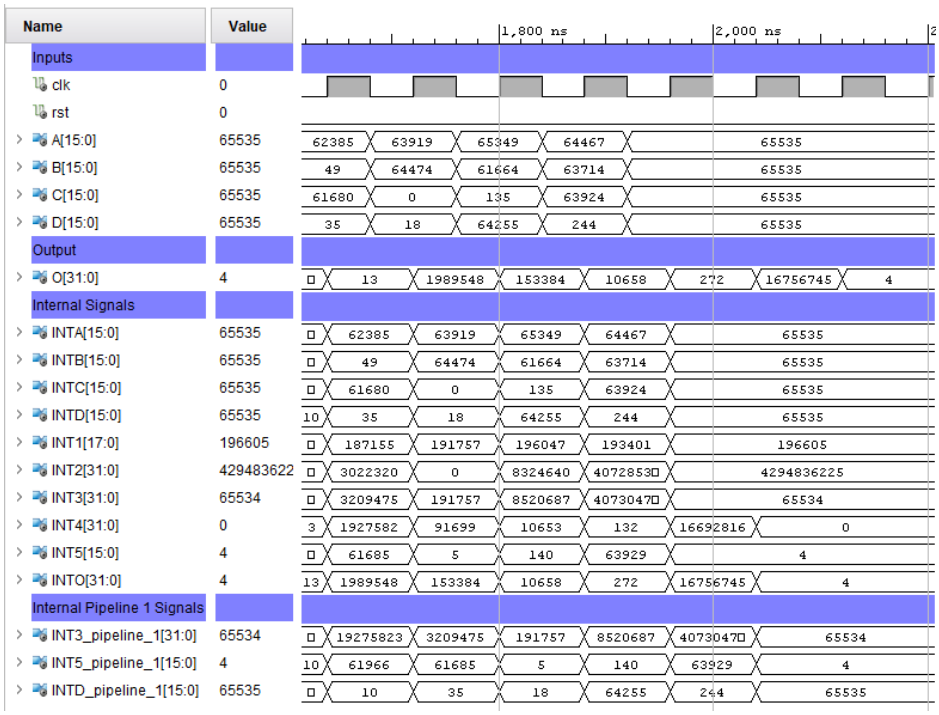
```
create_clock -period 106.000 -name clk -waveform {0.000 53.000} [get_ports clk]
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	96	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.318	0.000	0.476	0.000	0.000	0.109	0	887	96	0.00	0	0

2.1.3




Name
Value
1,200 ns
1,400 ns
1,600 ns
1,800 ns
Inputs
clk 0
rst 0
A[15:0] 65535 37 88 69 64506 64586 63945 62385 63919 65349 6446
B[15:0] 65535 60 65432 65004 9 308 49 64474 61664 6371
C[15:0] 65535 86 63113 64565 5 61961 61680 0 135 6392
D[15:0] 65535 60 54 65350 1 61845 10 35 18 64255 244
Output
O[31:0] 65540 61731 5 176 76537378 128793 193573 13 1989548 153384
Internal Signals
INTA[15:0] 65535 37 88 69 64506 64586 63945 62385 63919 65349
INTB[15:0] 65535 61664 65432 65004 9 308 49 64474 61664
INTC[15:0] 65535 86 63113 64565 5 61961 61680 0 135
INTD[15:0] 65535 62309 54 65350 1 61845 10 35 18 64255
INT1[17:0] 196605 111 264 207 193518 193758 191335 187155 191757 196047
INT2[31:0] 429483622 5303104 41296090 41969830 45 19083988 3022320 0 8324640
INT3[31:0] 65534 5303215 41296100 41969830 193563 193803 19275823 3209475 191757 8520687
INT4[31:0] 0 0 85 76474260 64223 193563 3 1927582 91699 10653
INT5[31:0] 65540 91 63118 64570 10 61966 61685 5 140
INTO[31:0] 65540 5 176 76537378 128793 193573 13 1989548 153384 10658
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 65534 0 5303215 41296100 41969830 193563 193803 19275823 3209475 191757
INT5_pipeline_1[31:0] 65540 5 91 63118 64570 10 61966 61685 5
INTD_pipeline_1[15:0] 65535 38 62309 54 65350 1 61845 10 35 18


Name
Value
1,800 ns
2,000 ns
Inputs
clk 0
rst 0
A[15:0] 65535 62385 63919 65349 64467 65535
B[15:0] 65535 49 64474 61664 63714 65535
C[15:0] 65535 61680 0 135 63924 65535
D[15:0] 65535 35 18 64255 244 65535
Output
O[31:0] 4 13 1989548 153384 10658 272 16756745 4
Internal Signals
INTA[15:0] 65535 62385 63919 65349 64467 65535
INTB[15:0] 65535 49 64474 61664 63714 65535
INTC[15:0] 65535 61680 0 135 63924 65535
INTD[15:0] 65535 35 18 64255 244 65535
INT1[17:0] 196605 187155 191757 196047 193401 196605
INT2[31:0] 429483622 3022320 0 8324640 40728530 4294836225
INT3[31:0] 65534 3209475 191757 8520687 40730470 65534
INT4[31:0] 0 3 1927582 91699 10653 132 16692816 0
INT5[15:0] 4 61685 5 140 63929 4
INTO[31:0] 4 13 1989548 153384 10658 272 16756745 4
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 65534 19275823 3209475 191757 8520687 40730470 65534
INT5_pipeline_1[15:0] 4 61966 61685 5 140 63929 4
INTD_pipeline_1[15:0] 65535 10 35 18 64255 244 65535

```
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 960 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12


Time: 1040 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 1120 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 1280 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176


Time: 1360 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 1440 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793
```

```
Time: 1520 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 1600 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 1680 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548


Time: 1760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35
```

```
for outputs
Actual value
O: 153384
Predicted value
O: 153384

Time: 1840 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 1920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 2 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745

Time: 2080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15
```

```
for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4

Time: 2160 ns  Iteration: 0
```

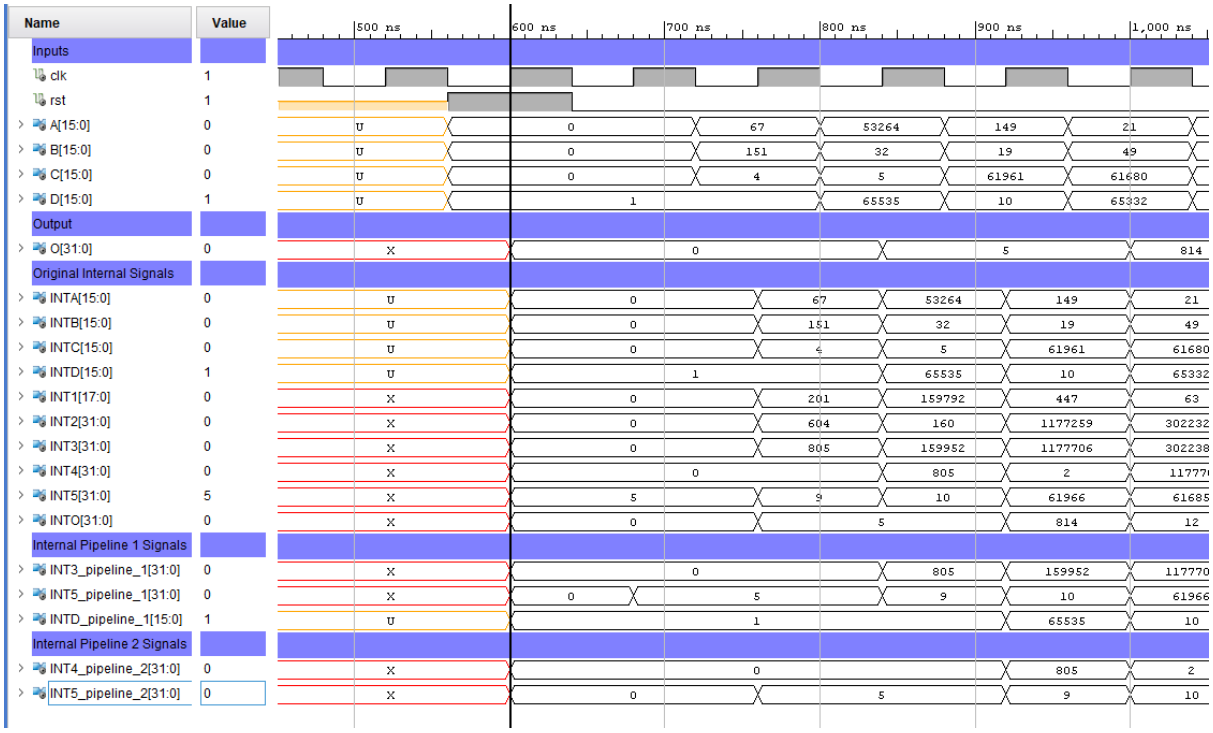
2.1.4

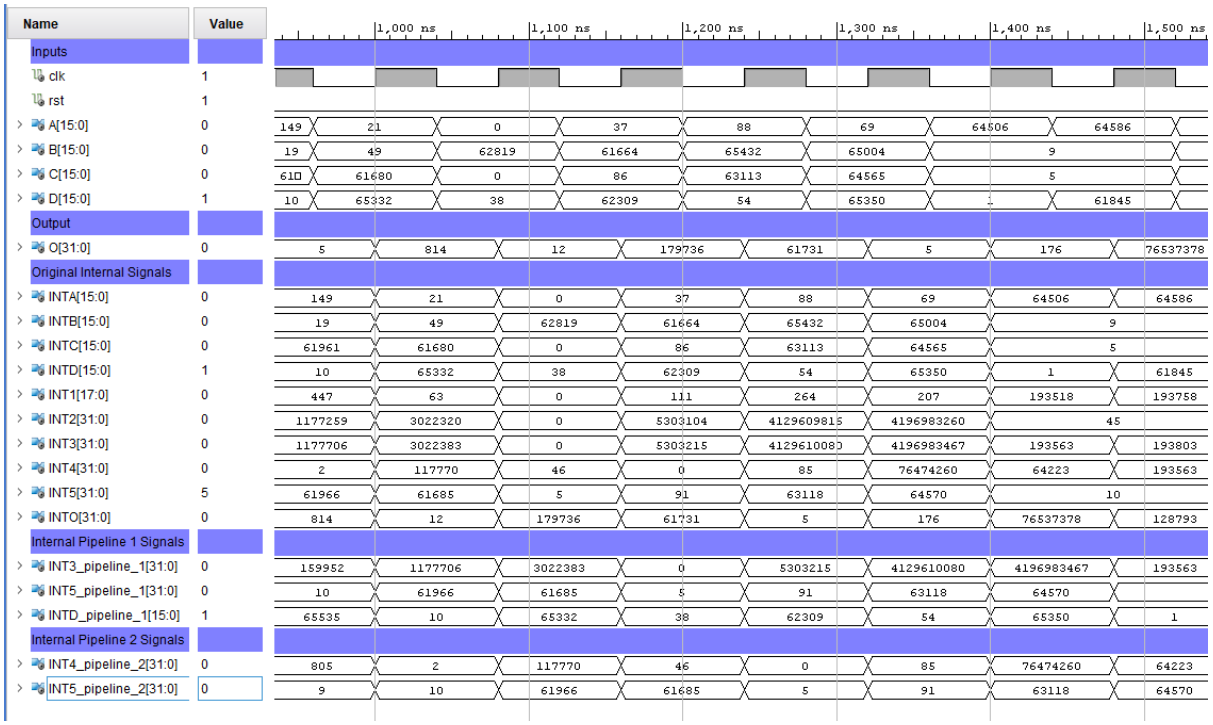
```
create_clock -period 98.000 -name clk -waveform {0.000 49.000} [get_ports clk]
```

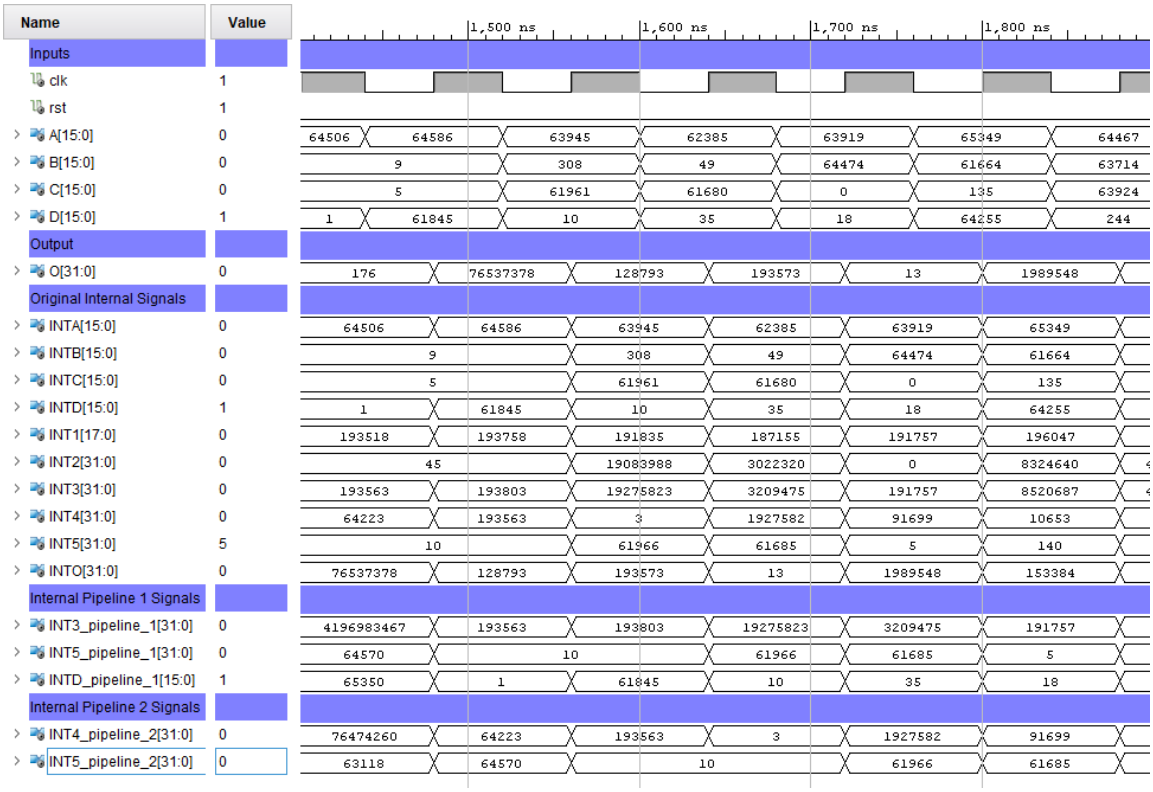
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	161	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.634	0.000	0.166	0.000	0.000	0.109	0	887	161	0.00	0	0

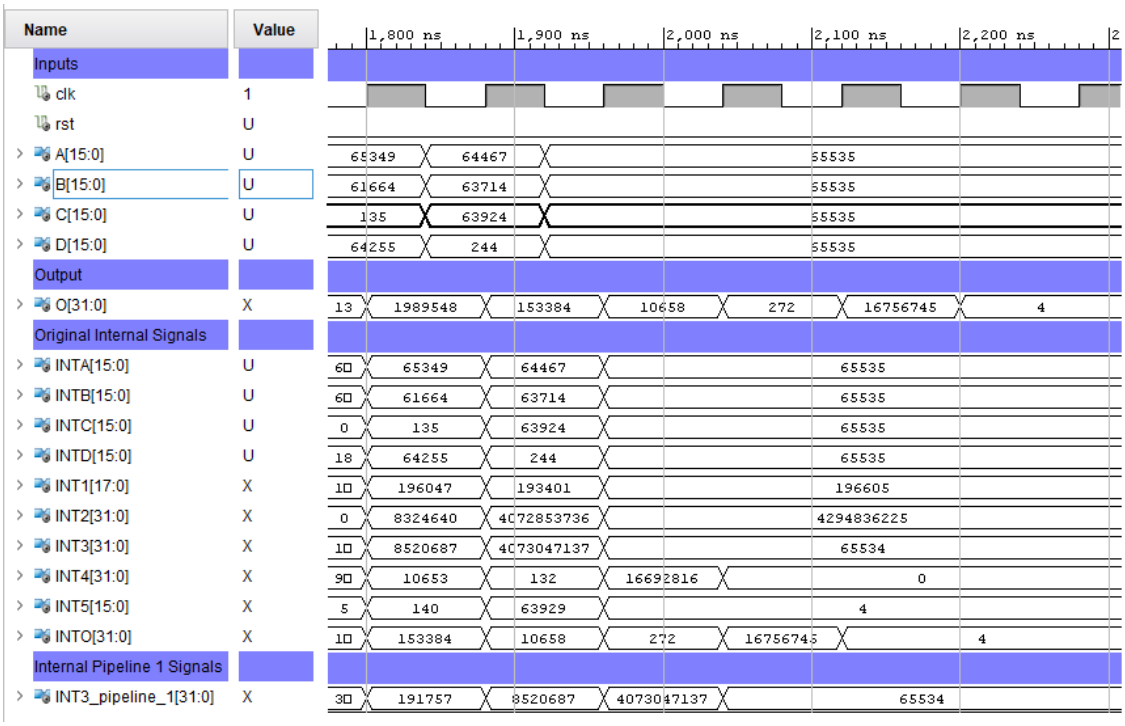
The circuit is expected to reduce the critical paths length and in turn reduce total transition time for all of the combinational logic. The addition of pipeline 1 allows the multiplication's and the division sections of the equation to take place in two separate clock cycles. The multiplication and division are the most time-consuming sections of the combinational logic, the separation of these allows the clock period to be reduced thus increasing the maximum frequency. This happens because the time taken for the multiplication can happen in one clock cycle pre-pipeline 1 and then the division can happen in the next clock cycle separating the total time for each rather than it being a total of both which is what would happens pre including pipeline 1. The practice does match the theory that decreasing the length of the critical path increases the maximum frequency of the circuit.

2.1.5


Name
Value
500 ns
600 ns
700 ns
800 ns
900 ns
1,000 ns
Inputs
clk 1
rst 1
A[15:0] 0 U 0 67 53264 149 21
B[15:0] 0 U 0 151 32 19 49
C[15:0] 0 U 0 4 5 61961 61680
D[15:0] 1 U 1 65535 10 65332
Output
O[31:0] 0 X 0 5 814
Original Internal Signals
INTA[15:0] 0 U 0 67 53264 149 21
INTB[15:0] 0 U 0 151 32 19 49
INTC[15:0] 0 U 0 4 5 61961 61680
INTD[15:0] 1 U 1 65535 10 65332
INT1[17:0] 0 X 0 201 159792 447 63
INT2[31:0] 0 X 0 604 160 1177259 302232
INT3[31:0] 0 X 0 805 159952 1177706 302238
INT4[31:0] 0 X 0 805 2
INT5[31:0] 5 X 5 9 10 61966 61685
INTO[31:0] 0 X 0 5 814 12
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 X 0 805 159952 117770
INT5_pipeline_1[31:0] 0 X 0 5 9 10 61966
INTD_pipeline_1[15:0] 1 U 1 65535 10
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 X 0 805 2
INT5_pipeline_2[31:0] 0 X 0 5 9 10


Name
Value
1,000 ns
1,100 ns
1,200 ns
1,300 ns
1,400 ns
1,500 ns
Inputs
clk 1
rst 1
A[15:0] 0 149 21 0 37 88 69 64506 64586
B[15:0] 0 19 49 62819 61664 65432 65004 9
C[15:0] 0 61680 0 86 63113 64565 5
D[15:0] 1 10 65332 38 62309 54 65350 1 61845
Output
O[31:0] 0 5 814 12 179736 61731 5 176 76537378
Original Internal Signals
INTA[15:0] 0 149 21 0 37 88 69 64506 64586
INTB[15:0] 0 19 49 62819 61664 65432 65004 9
INTC[15:0] 0 61961 61680 0 86 63113 64565 5
INTD[15:0] 1 10 65332 38 62309 54 65350 1 61845
INT1[17:0] 0 447 63 0 111 264 207 193518 193758
INT2[31:0] 0 1177259 3022320 0 5303104 4129609815 4196983260 45
INT3[31:0] 0 1177706 3022383 0 5303215 4129610080 4196983467 193563 193803
INT4[31:0] 0 2 117770 46 0 85 76474260 64223 193563
INT5[31:0] 5 61966 61685 5 91 63118 64570 10
INTO[31:0] 0 814 12 179736 61731 5 176 76537378 128793
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 159952 1177706 3022383 0 5303215 4129610080 4196983467 193563
INT5_pipeline_1[31:0] 0 10 61966 61685 5 91 63118 64570
INTD_pipeline_1[15:0] 1 65535 10 65332 38 62309 54 65350 1
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 805 2 117770 46 0 85 76474260 64223
INT5_pipeline_2[31:0] 0 9 10 61966 61685 5 91 63118 64570


Name
Value
1,500 ns
1,600 ns
1,700 ns
1,800 ns
Inputs
clk 1
rst 1
A[15:0] 0 64506 64586 63945 62385 63919 65349 64467
B[15:0] 0 9 308 49 64474 61664 63714
C[15:0] 0 5 61961 61680 0 135 63924
D[15:0] 1 1 61845 10 35 18 64255 244
Output
O[31:0] 0 176 76537378 128793 193573 13 1989548
Original Internal Signals
INTA[15:0] 0 64506 64586 63945 62385 63919 65349
INTB[15:0] 0 9 308 49 64474 61664
INTC[15:0] 0 5 61961 61680 0 135
INTD[15:0] 1 1 61845 10 35 18 64255
INT1[17:0] 0 193518 193758 191835 187155 191757 196047
INT2[31:0] 0 45 19083988 3022320 0 8324640
INT3[31:0] 0 193563 193803 19275823 3209475 191757 8520687
INT4[31:0] 0 64223 193563 3 1927582 91699 10653
INT5[31:0] 5 10 61966 61685 5 140
INTO[31:0] 0 76537378 128793 193573 13 1989548 153384
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 4196983467 193563 193803 19275823 3209475 191757
INT5_pipeline_1[31:0] 0 64570 10 61966 61685 5
INTD_pipeline_1[15:0] 1 65350 1 61845 10 35 18
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 76474260 64223 193563 3 1927582 91699
INT5_pipeline_2[31:0] 0 63118 64570 10 61966 61685


Name
Value
1,800 ns
1,900 ns
2,000 ns
2,100 ns
2,200 ns
Inputs
clk 1
rst U
A[15:0] U 65349 64467 65535
B[15:0] U 61664 63714 65535
C[15:0] U 135 63924 65535
D[15:0] U 64255 244 65535
Output
O[31:0] X 13 1989548 153384 10658 272 16756745 4
Original Internal Signals
INTA[15:0] U 65349 64467 65535
INTB[15:0] U 61664 63714 65535
INTC[15:0] U 0 135 63924 65535
INTD[15:0] U 18 64255 244 65535
INT1[17:0] X 196047 193401 196605
INT2[31:0] X 8324640 4072853736 4294836225
INT3[31:0] X 8520687 4073047137 65534
INT4[31:0] X 10653 132 16692816 0
INT5[15:0] X 140 63929 4
INTO[31:0] X 153384 10658 272 16756745 4
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] X 191757 8520687 4073047137 65534

```
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 1040 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 1120 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332
```

```
for outputs
Actual value
O: 61731
Predicted value
O: 61731

Time: 1280 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 1360 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 1440 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 1520 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350
```

```
for outputs
Actual value
O: 128793
Predicted value
O: 128793

Time: 1600 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 1680 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 1760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548

Time: 1840 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35
```

```
for outputs
Actual value
O: 153384
Predicted value
O: 153384

Time: 1920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 2 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 2080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745
```

```
Time: 2160 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4

Time: 2240 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

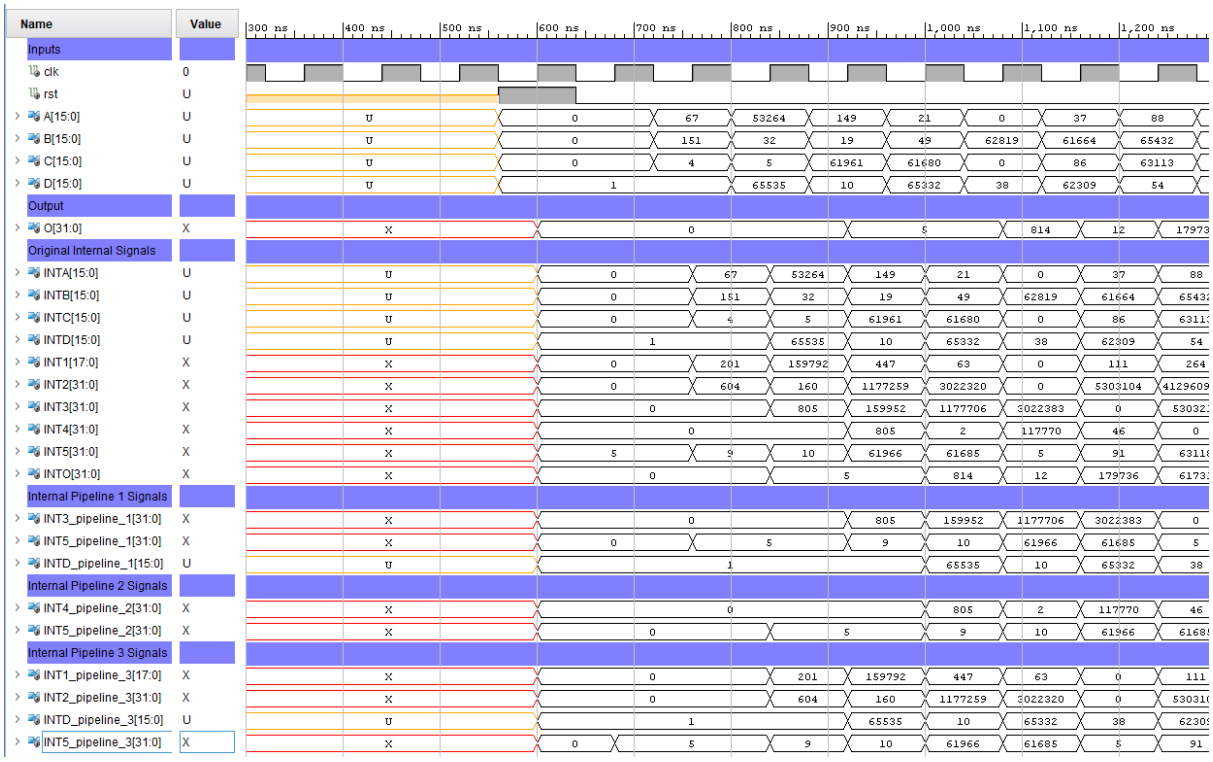
2.1.6

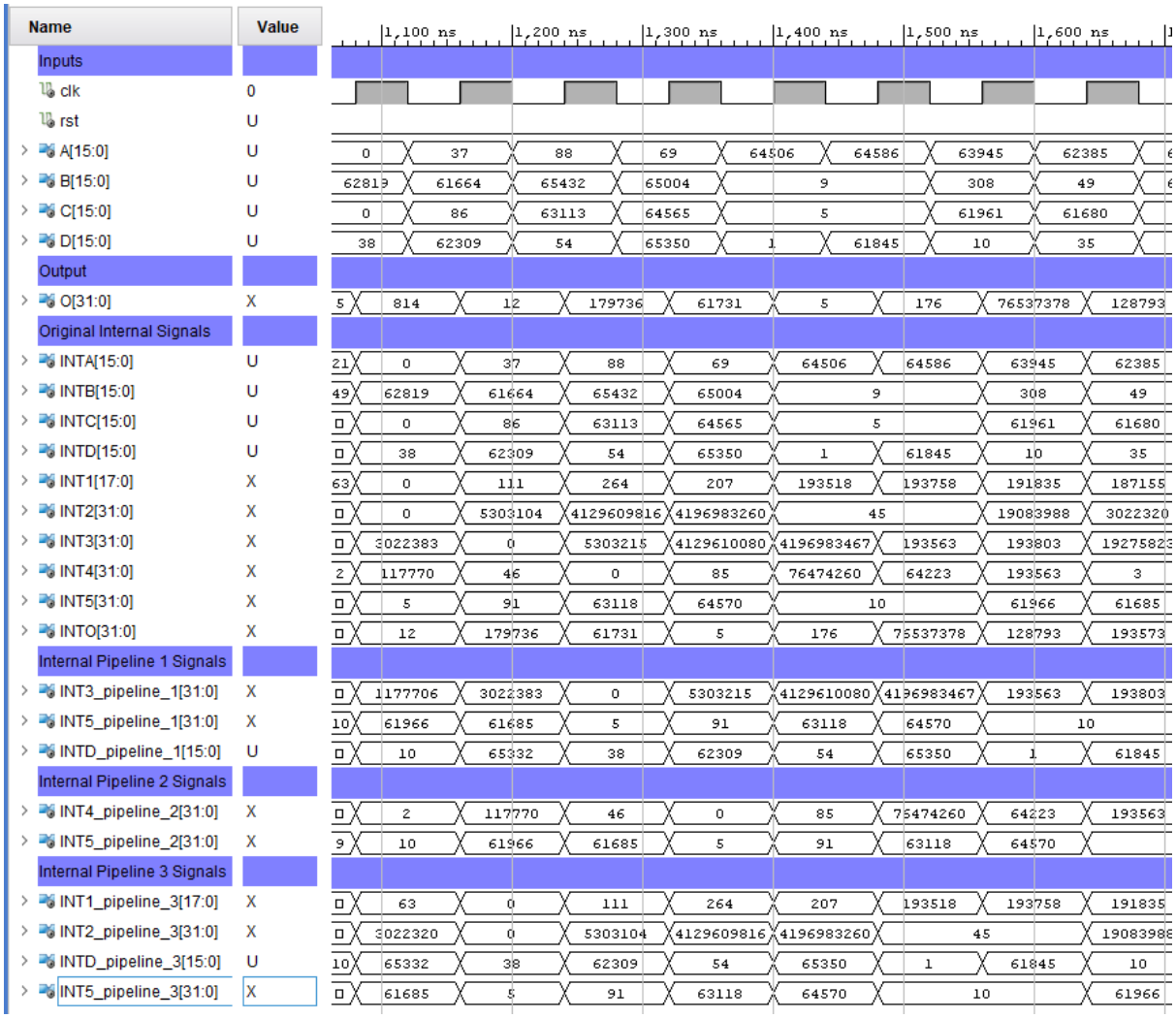
```
create_clock -period 93.000 -name clk -waveform {0.000 46.500} [get_ports clk]
```

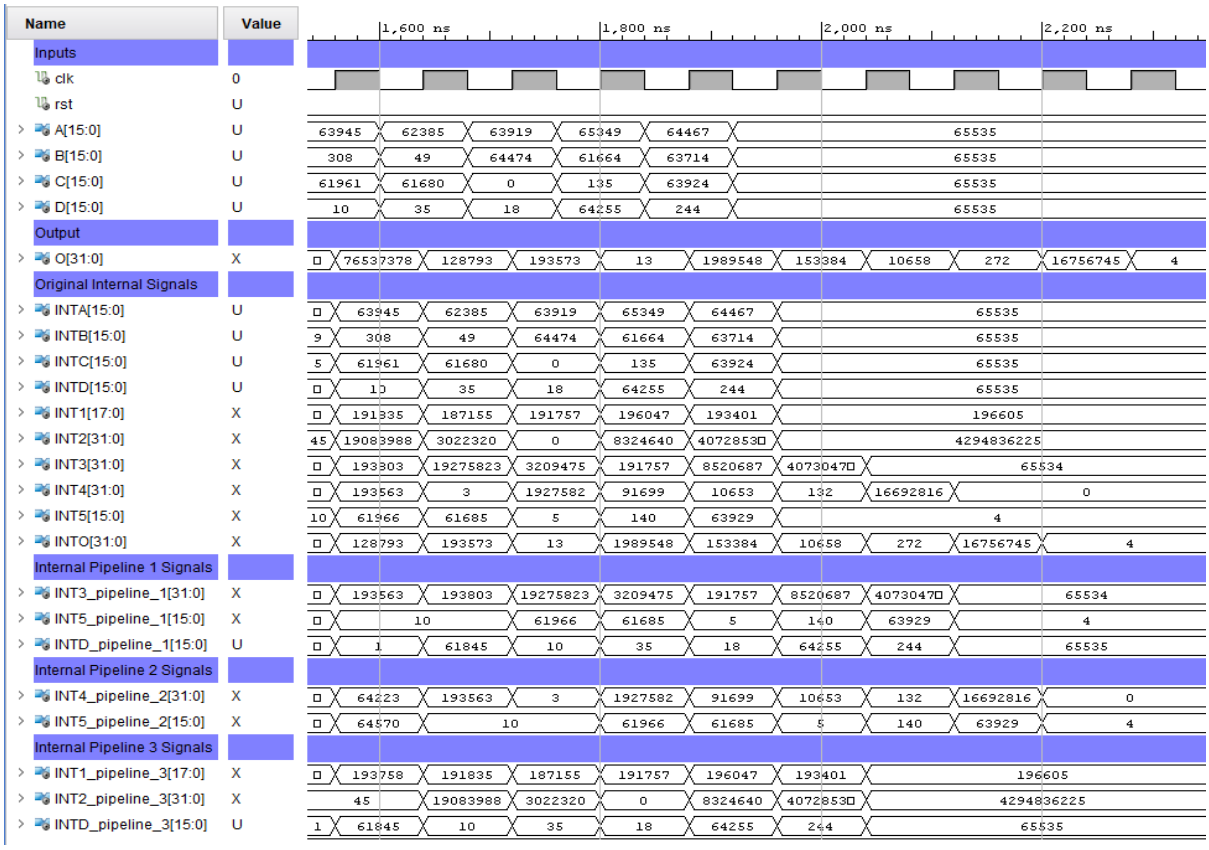
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	210	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.802	0.000	0.122	0.000	0.000	0.110	0	887	210	0.00	0	0

The expectation of the maximum frequency after the inclusion of pipeline 2 is an increase due to the isolation of the division between the pipelines 1 & 2. Previously the time taken to process the division and the addition was the critical path, the isolation of the combinational logic of the divider between the pipelines means that the critical path is once more reduced. This reduction of the critical path also reduces the time for the combinational logic as it is only the time for the divider to process and not the result of the divider and addition to process. This means the critical paths time is reduced and increasing the frequency of the circuit over all. Without the pipeline 2 the maximum frequency would be lower as the time taken to process the divider and addition is higher than the time to process just the divider.

2.1.7


Name
Value
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1,000 ns
1,100 ns
1,200 ns
Inputs
clk
rst
A[15:0]
B[15:0]
C[15:0]
D[15:0]
Output
O[31:0]
Original Internal Signals
INTA[15:0]
INTB[15:0]
INTC[15:0]
INTD[15:0]
INT1[17:0]
INT2[31:0]
INT3[31:0]
INT4[31:0]
INT5[31:0]
INT0[31:0]
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0]
INT5_pipeline_1[31:0]
INTD_pipeline_1[15:0]
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0]
INT5_pipeline_2[31:0]
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0]
INT2_pipeline_3[31:0]
INTD_pipeline_3[15:0]
INT5_pipeline_3[31:0]


Name
Value
1,100 ns
1,200 ns
1,300 ns
1,400 ns
1,500 ns
1,600 ns
Inputs
clk 0
rst U
A[15:0] U 0 37 88 69 64506 64586 63945 62385
B[15:0] U 62819 61664 65432 65004 9 308 49
C[15:0] U 0 86 63113 64565 5 61961 61680
D[15:0] U 38 62309 54 65350 1 61845 10 35
Output
O[31:0] X 5 814 12 179736 61731 5 176 76537378 128793
Original Internal Signals
INTA[15:0] U 21 0 37 88 69 64506 64586 63945 62385
INTB[15:0] U 49 62819 61664 65432 65004 9 308 49
INTC[15:0] U 0 86 63113 64565 5 61961 61680
INTD[15:0] U 38 62309 54 65350 1 61845 10 35
INT1[17:0] X 63 0 111 264 207 193518 193758 191835 187155
INT2[31:0] X 0 5303104 4129609816 4196983260 45 19083988 3022320
INT3[31:0] X 3022383 0 5303215 4129610080 4196983467 193563 193803 19275823
INT4[31:0] X 2 117770 46 0 85 76474260 64223 193563 3
INT5[31:0] X 5 91 63118 64570 10 61966 61685
INTO[31:0] X 12 179736 61731 5 176 76537378 128793 193573
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] X 1177706 3022383 0 5303215 4129610080 4196983467 193563 193803
INT5_pipeline_1[31:0] X 10 61966 61685 5 91 63118 64570 10
INTD_pipeline_1[15:0] U 10 65332 38 62309 54 65350 1 61845
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] X 2 117770 46 0 85 76474260 64223 193563
INT5_pipeline_2[31:0] X 9 10 61966 61685 5 91 63118 64570
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] X 63 0 111 264 207 193518 193758 191835
INT2_pipeline_3[31:0] X 3022320 0 5303104 4129609816 4196983260 45 19083988
INTD_pipeline_3[15:0] U 10 65332 38 62309 54 65350 1 61845 10
INT5_pipeline_3[31:0] X 61685 5 91 63118 64570 10 61966


Name
Value
1,600 ns
1,800 ns
2,000 ns
2,200 ns
Inputs
clk 0
rst U
A[15:0] U 63945 62385 63919 65349 64467 65535
B[15:0] U 308 49 64474 61664 63714 65535
C[15:0] U 61961 61680 0 135 63924 65535
D[15:0] U 10 35 18 64255 244 65535
Output
O[31:0] X 76537378 128793 193573 13 1989548 153384 10658 272 16756745 4
Original Internal Signals
INTA[15:0] U 63945 62385 63919 65349 64467 65535
INTB[15:0] U 9 308 49 64474 61664 63714 65535
INTC[15:0] U 5 61961 61680 0 135 63924 65535
INTD[15:0] U 10 35 18 64255 244 65535
INT1[17:0] X 191335 187155 191757 196047 193401 196605
INT2[31:0] X 45 19083988 3022320 0 8324640 4072853 4294836225
INT3[31:0] X 193303 19275823 3209475 191757 8520687 4073047 65534
INT4[31:0] X 193563 3 1927582 91699 10653 132 16692816 0
INT5[15:0] X 10 61966 61685 5 140 63929 4
INTO[31:0] X 128793 193573 13 1989548 153384 10658 272 16756745 4
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] X 193563 193803 19275823 3209475 191757 8520687 4073047 65534
INT5_pipeline_1[15:0] X 10 61966 61685 5 140 63929 4
INTD_pipeline_1[15:0] U 1 61845 10 35 18 64255 244 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] X 64223 193563 3 1927582 91699 10653 132 16692816 0
INT5_pipeline_2[15:0] X 64570 10 61966 61685 5 140 63929 4
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] X 193758 191835 187155 191757 196047 193401 196605
INT2_pipeline_3[31:0] X 45 19083988 3022320 0 8324640 4072853 4294836225
INTD_pipeline_3[15:0] U 1 61845 10 35 18 64255 244 65535

```
run 5 us
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 1120 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 1200 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 1280 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 1360 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 1440 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 1520 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 1600 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793
```

```
Time: 1680 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 1760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 1840 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548

Time: 1920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153384
Predicted value
O: 153384
```

```
Time: 2 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 2080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 2160 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745

Time: 2240 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4

Time: 2320 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

2.1.8

```
create_clock -period 92.000 -name clk -waveform {0.000 46.000} [get_ports clk]
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								897	293	0.00	0	0
impl_1	constrs_1	route_design Complete!	0.737	0.000	0.095	0.000	0.000	0.110	0	887	293	0.00	0	0

The addition of pipeline 3 is not expected to increase the maximum frequency but it does as it separates the multiplications and the preceding addition. The increase in the frequency was not expected as the multiplications are separated from the extra addition but the critical path is still located in the divider so the small increase in the maximum frequency is a surprise as it does match the theory that pipelining increases the maximum frequency but does not match the theory in that the critical path was not affected this time and still the maximum frequency increased.

2.1.9

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use work.DigEng.all;

-- Algorithm entity
-- Synchronous calculator of the equation
-- O <= (A*3 + B*C)/D + C +5
-- 6 inputs, including standard clk and reset
-- Inputs A, B, C, D  16 bit std logic vector inputs of values
--
-- to computate.
-- output O is result of the equation.
-- 5 registered pipelined sections including input and outputs
-- Computation of equation takes 5 clk clyes from input to output
-- 1st Input Register input registers to store inputs
-- 2nd "pipeline 3" results of (3*A),(B*C),D,(5+C) each stored in
registers
-- 3rd "pipeline 1" results of(3*A)+(B*C), D,(5+C) each stored in
registers
-- Note* divider has 34 internal pipelined sections requiring a
-- Pipelined array of (5+C) made up of 34 registers using the FIFO
method
-- 4th "pipeline 2" results of(3*A)+(B*C)/ D,(5+C) each stored in
registers
-- 5th output registers results of((3*A)+(B*C)/ D)+(5+C) stored in
register

entity algorithm is
    generic (data_size : integer := 16);
    Port ( A : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           B : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           C : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           D : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           O : out  STD_LOGIC_VECTOR (data_size*2-1 downto 0);
           clk : in  STD_LOGIC;
           rst : in  STD_LOGIC);
end algorithm;

architecture Behavioral of algorithm is
-- internal input signals
signal INTA, INTB, INTC, INTD : UNSIGNED (data_size-1 downto 0);

-- internal signals connecting signals to modify via math functions
signal INT1 : UNSIGNED (data_size+1 downto 0);
signal INT2 : UNSIGNED (data_size*2-1 downto 0);
signal INT3 : UNSIGNED (data_size*2-1 downto 0);
signal INT4 : UNSIGNED (data_size*2-1 downto 0);
signal INT5 : UNSIGNED (data_size-1 downto 0);
signal INTO : UNSIGNED (data_size*2-1 downto 0);

-- signals added for pipeline 1
signal INT3_pipeline_1 : UNSIGNED (data_size*2-1 downto 0);
signal INT5_pipeline_1 : UNSIGNED (data_size-1 downto 0);
signal INTD_pipeline_1 : UNSIGNED (data_size-1 downto 0);
```

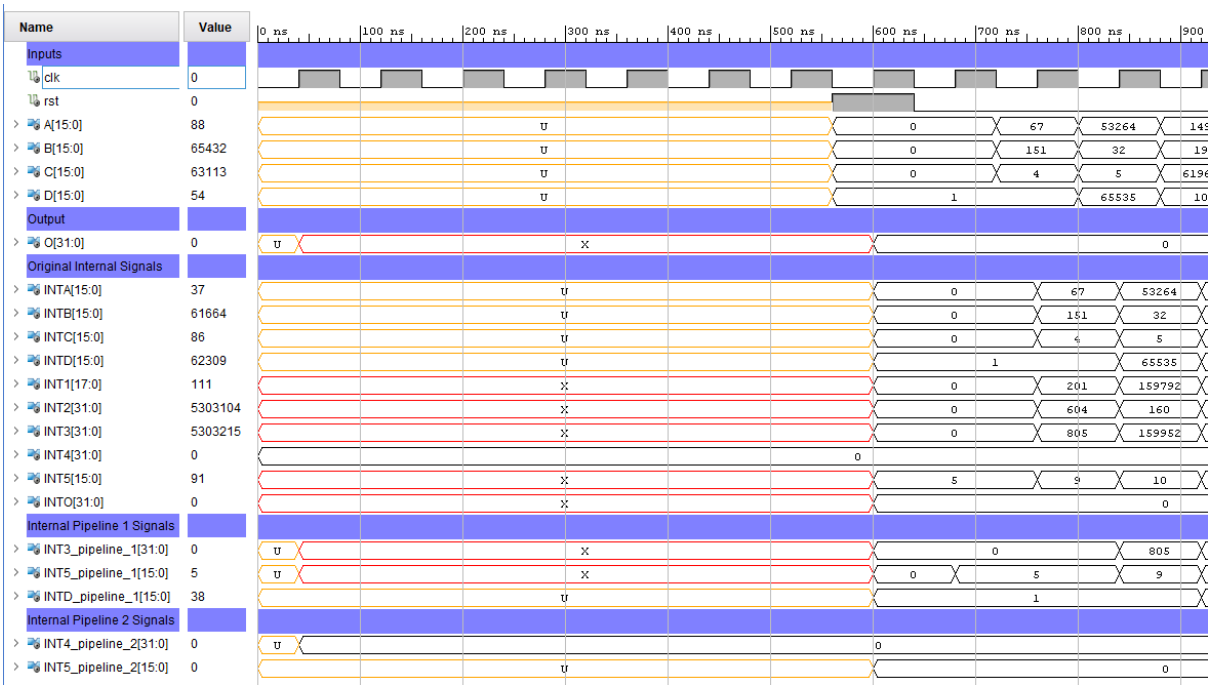
```
-- signals added for pipeline 2
signal INT4_pipeline_2 : UNSIGNED (data_size*2-1 downto 0);
signal INT5_pipeline_2 : UNSIGNED (data_size-1 downto 0);

-- signals added for pipeline 3
signal INT1_pipeline_3 : UNSIGNED (data_size+1 downto 0);
signal INT2_pipeline_3 : UNSIGNED (data_size*2-1 downto 0);
signal INTD_pipeline_3 : UNSIGNED (data_size-1 downto 0);
signal INT5_pipeline_3 : UNSIGNED (data_size-1 downto 0);


begin

-- setup for individual input registers for inputs A,B, C & D
-- All Synchronous with reset to zero when reset signal active,
-- NO enable signals required.
input_regs: process (clk) is
begin
  if rising_edge(clk) then
  -- resets internal signals below to zero
    if rst = '1' then
      INTA <= (others => '0');
      INTB <= (others => '0');
      INTC <= (others => '0');
--    INTD <= (0 => '1', others => '0');  -- aggregate notation
      INTD <= to_unsigned(1,INTD'length); -- type conversion notation
    else
    -- connects inputs to internal signal values
      INTA <= unsigned(A);
      INTB <= unsigned(B);
      INTC <= unsigned(C);
      INTD <= unsigned(D);
    end if;
  end if;
end process input_regs;

-- equation maths defined per internal signals
-- INT1 result of INTA multiplied by 3
INT1 <= INTA * to_unsigned(3, 2);
INT2 <= INTB * INTC;
INT5 <= INTC + to_unsigned(5, INT5'length);
--in between pipline 3 and pipline 1
INT3 <= INT1_pipeline_3 + INT2_pipeline_3;
--in between pipline 1 and pipline 2
INT4 <= INT3_pipeline_1 / INTD_pipeline_1;
--in between pipline 2 and pipline output registers
INTO <= INT5_pipeline_2 + INT4_pipeline_2;

-- output register.
-- synchronous.
-- NO enable
-- output = 0 at rising clk edge
-- when input reset is active.
-- output = INTO at rising clk edge.
output_regs: process (clk) is
begin
```

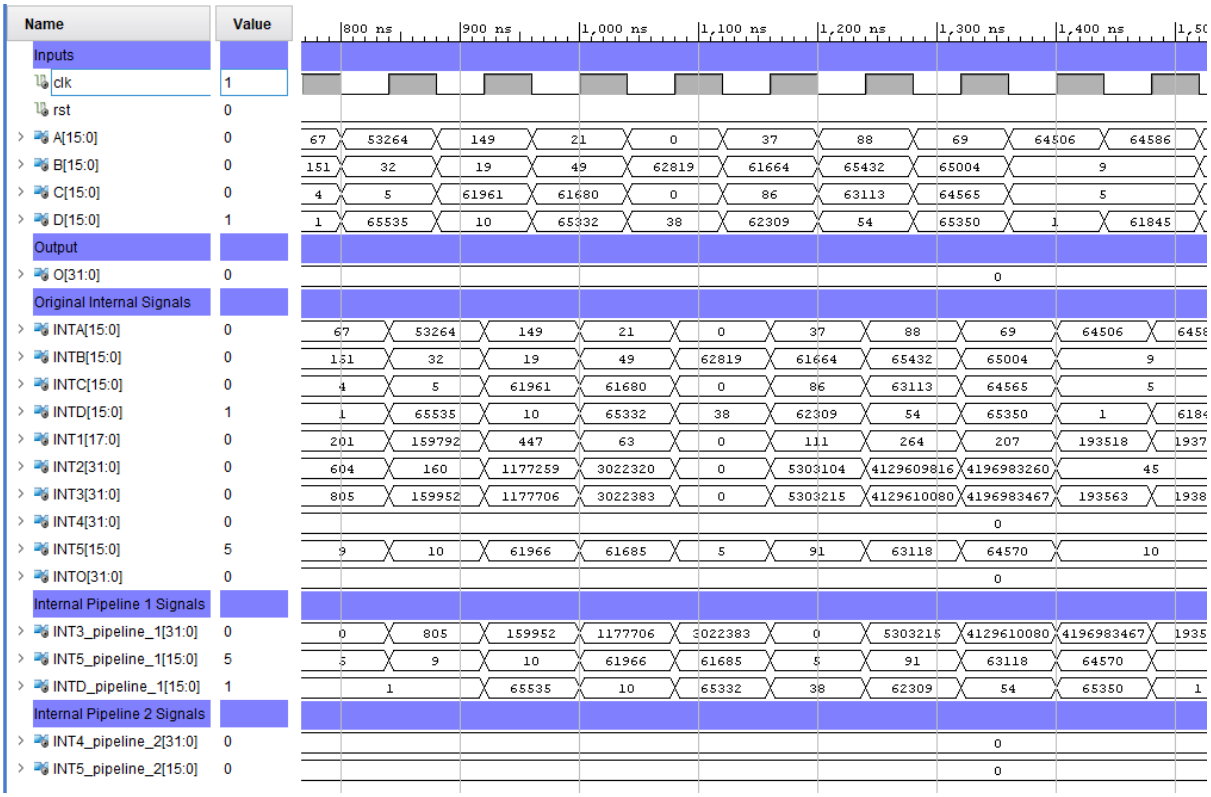
```
if rising_edge(clk) then
    if rst = '1' then
      O <= (others => '0');
    else
      O <= std_logic_vector(INTO);
    end if;
  end if;
end process output_regs;

-- pipline 1 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline_1: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT3_pipeline_1 <= (others => '0');
    INT5_pipeline_1 <= (others => '0');
    INTD_pipeline_1 <= to_unsigned(1,INTD'length); -- type conversion
notation
    else
    INT3_pipeline_1 <= INT3;
    INT5_pipeline_1 <= INT5_pipeline_3;
    INTD_pipeline_1 <= INTD_pipeline_3;
    end if;
  end if;
end process pipeline_1;

-- pipeline 2
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline_2: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT4_pipeline_2 <= (others => '0');
    INT5_pipeline_2 <= (others => '0');
    else
    INT4_pipeline_2 <= INT4;
    INT5_pipeline_2 <= INT5_pipeline_1;
    end if;
  end if;
end process pipeline_2;
-- pipeline 3
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
```

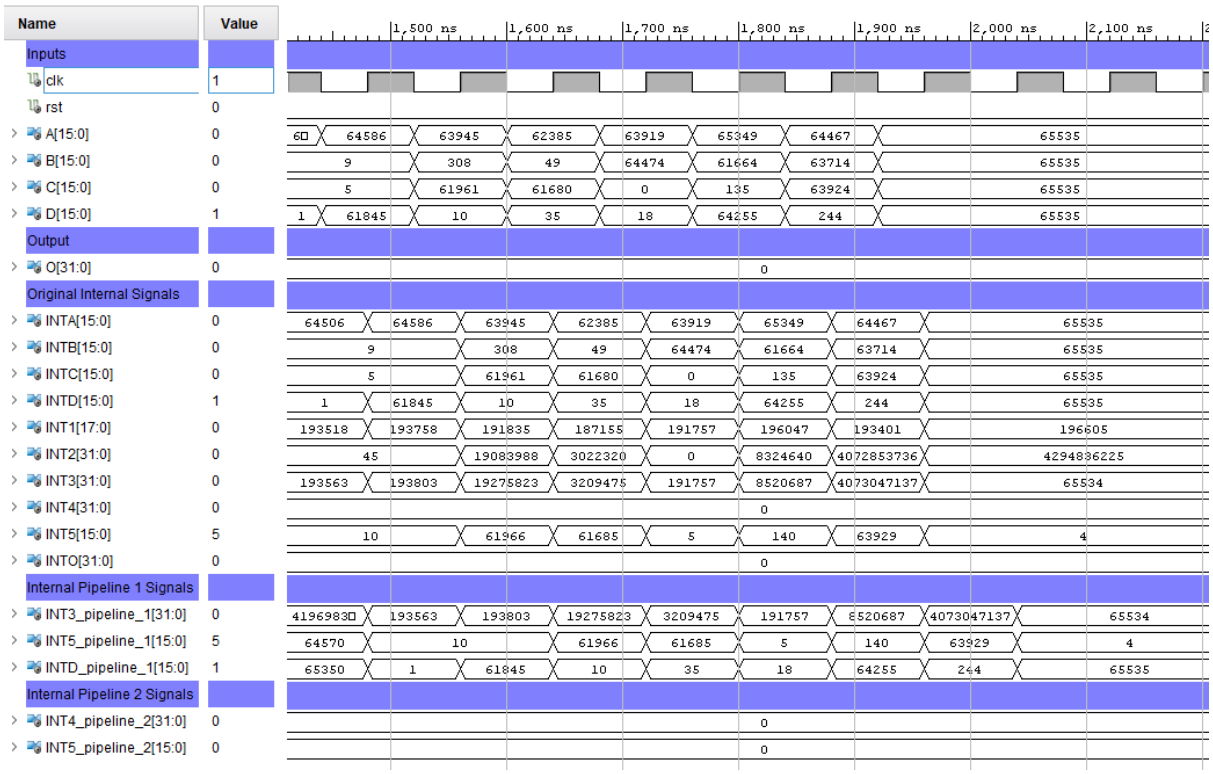
```
pipeline_3: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT1_pipeline_3 <= (others => '0');
    INT2_pipeline_3 <= (others => '0');
    INT5_pipeline_3 <= (others => '0');
    INTD_pipeline_3 <= to_unsigned(1,INTD'length); -- type conversion
notation
    else
    INT1_pipeline_3 <= INT1;
    INT2_pipeline_3 <= INT2;
    INT5_pipeline_3 <= INT5;
    INTD_pipeline_3 <= INTD;

    end if;
  end if;
end process pipeline_3;

end Behavioral;
```

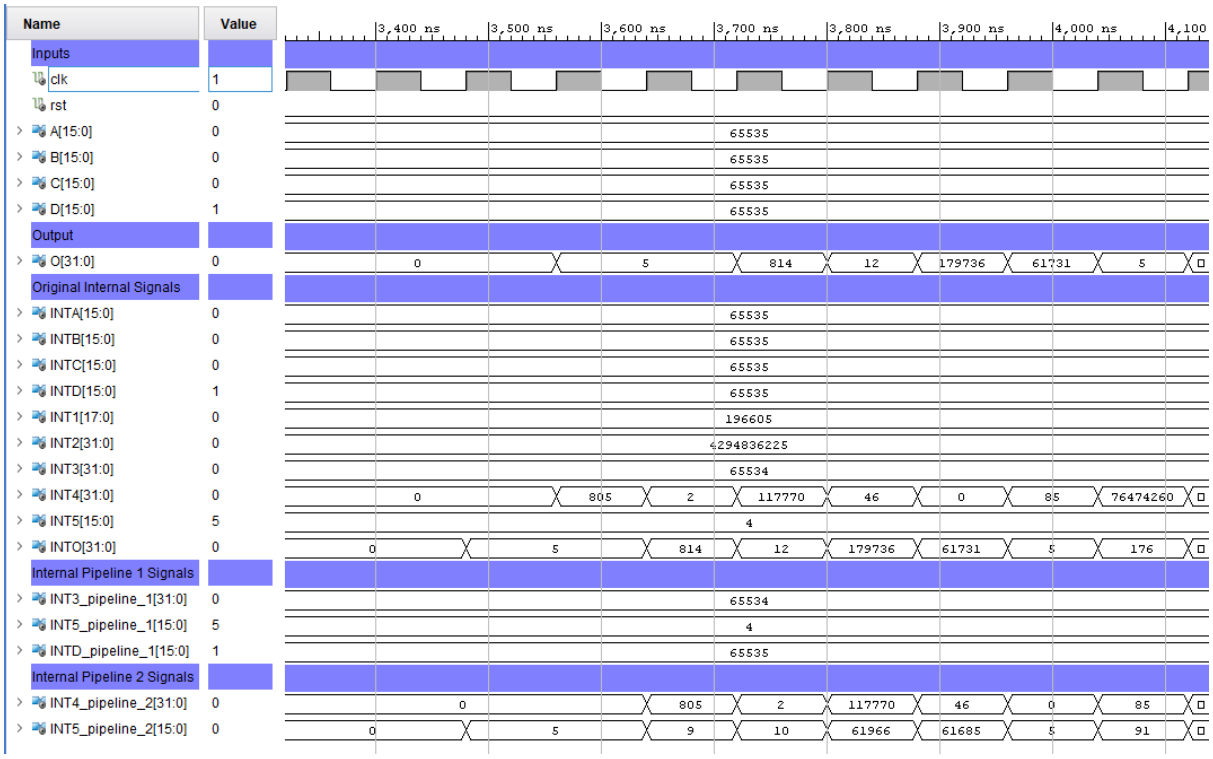
Lab 3 Task 2

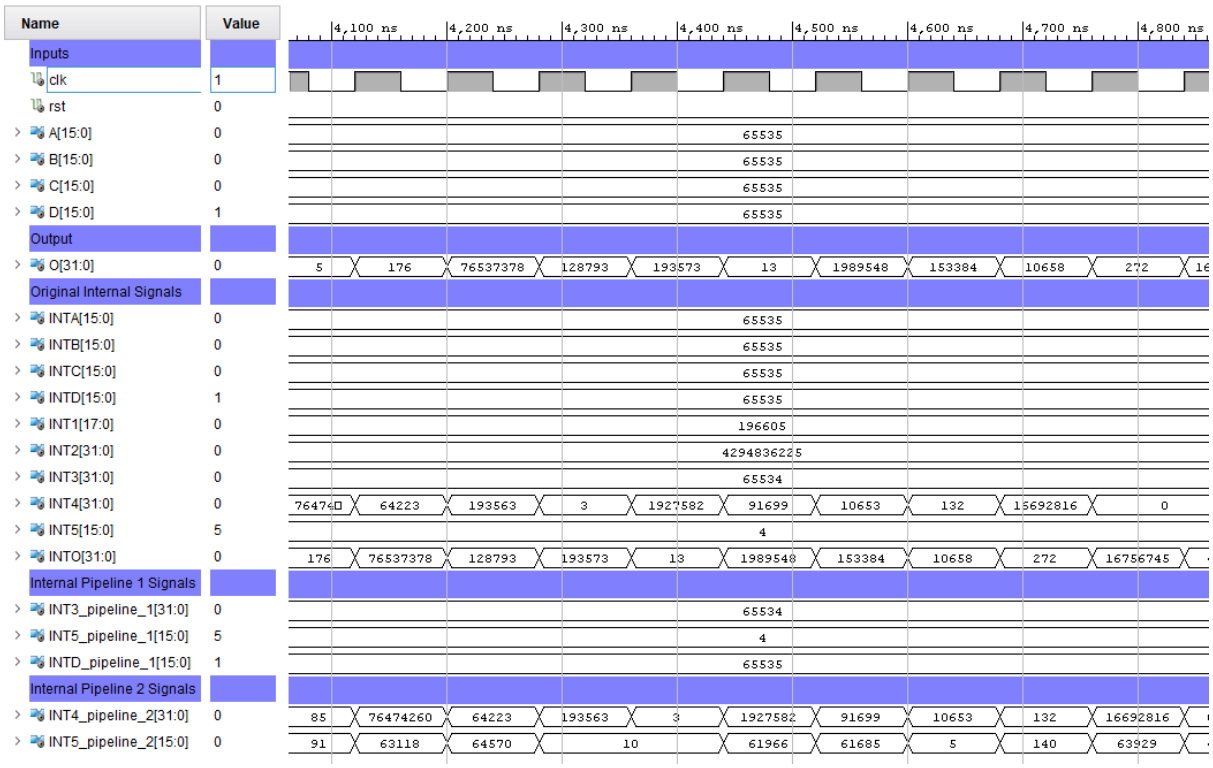
2.2.1

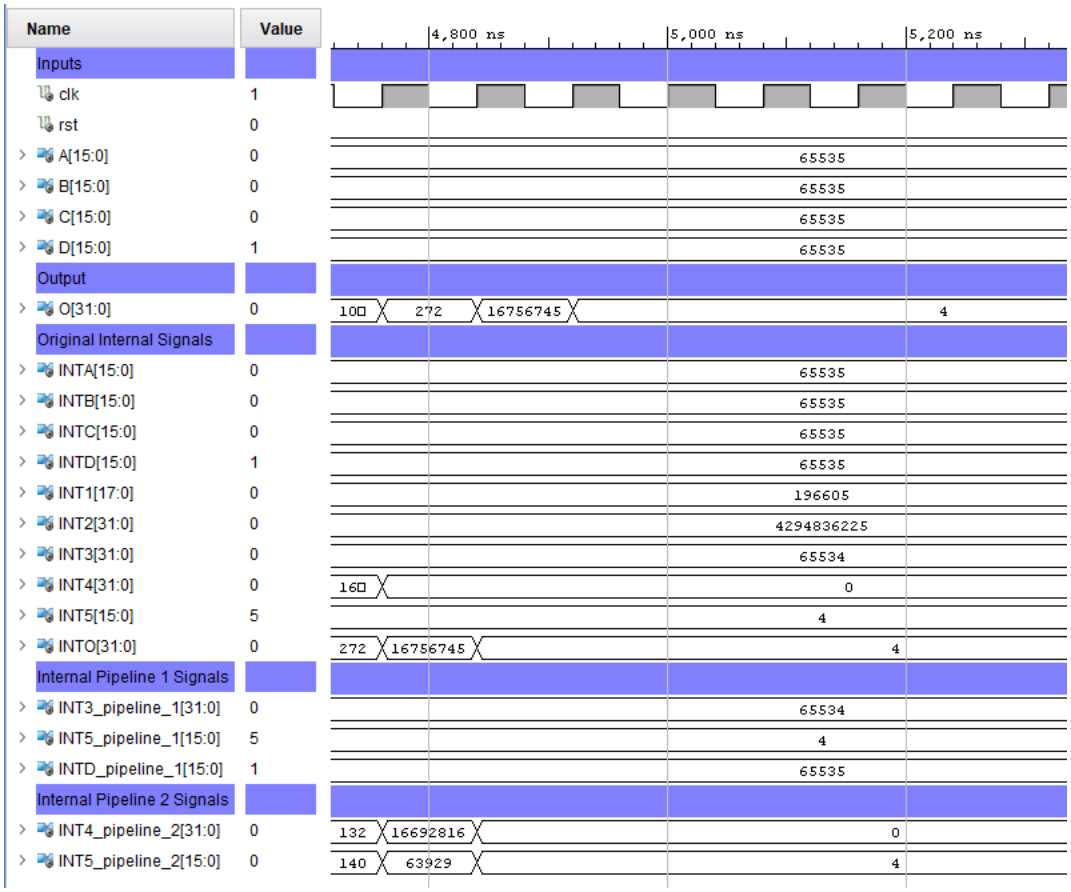





Name
Value
1,500 ns
1,600 ns
1,700 ns
1,800 ns
1,900 ns
2,000 ns
2,100 ns
Inputs
clk 1
rst 0
A[15:0] 0 64586 63945 62385 63919 65349 64467 65535
B[15:0] 0 9 308 49 64474 61664 63714 65535
C[15:0] 0 5 61961 61680 0 135 63924 65535
D[15:0] 1 61845 10 35 18 64255 244 65535
Output
O[31:0] 0 0
Original Internal Signals
INTA[15:0] 0 64506 64586 63945 62385 63919 65349 64467 65535
INTB[15:0] 0 9 308 49 64474 61664 63714 65535
INTC[15:0] 0 5 61961 61680 0 135 63924 65535
INTD[15:0] 1 61845 10 35 18 64255 244 65535
INT1[17:0] 0 193758 191835 187155 191757 196047 193401 196605
INT2[31:0] 0 45 19083988 3022320 0 8324640 4072853736 4294836225
INT3[31:0] 0 193803 19275823 3209475 191757 8520687 4073047137 65534
INT4[31:0] 0 0
INT5[15:0] 5 10 61966 61685 5 140 63929 4
INTO[31:0] 0 0
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 193563 193803 19275823 3209475 191757 8520687 4073047137 65534
INT5_pipeline_1[15:0] 5 10 61966 61685 5 140 63929 4
INTD_pipeline_1[15:0] 1 64570 1 61845 10 35 18 64255 244 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 0
INT5_pipeline_2[15:0] 0 0


Name
Value
3,400 ns
3,500 ns
3,600 ns
3,700 ns
3,800 ns
3,900 ns
4,000 ns
Inputs
clk 1
rst 0
A[15:0] 0 65535
B[15:0] 0 65535
C[15:0] 0 65535
D[15:0] 1 65535
Output
O[31:0] 0 0 5 814 12 179736 61731 5
Original Internal Signals
INTA[15:0] 0 65535
INTB[15:0] 0 65535
INTC[15:0] 0 65535
INTD[15:0] 1 65535
INT1[17:0] 0 196605
INT2[31:0] 0 4294836225
INT3[31:0] 0 65534
INT4[31:0] 0 0 805 2 117770 46 0 85 76474260
INT5[15:0] 5 4
INTO[31:0] 0 0 5 814 12 179736 61731 5 176
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 65534
INT5_pipeline_1[15:0] 5 4
INTD_pipeline_1[15:0] 1 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 0 805 2 117770 46 0 85
INT5_pipeline_2[15:0] 0 0 5 9 10 61966 61685 5 91


Name
Value
4,100 ns
4,200 ns
4,300 ns
4,400 ns
4,500 ns
4,600 ns
4,700 ns
4,800 ns
Inputs
clk 1
rst 0
A[15:0] 0
B[15:0] 0
C[15:0] 0
D[15:0] 1
Output
O[31:0] 0
Original Internal Signals
INTA[15:0] 0
INTB[15:0] 0
INTC[15:0] 0
INTD[15:0] 1
INT1[17:0] 0
INT2[31:0] 0
INT3[31:0] 0
INT4[31:0] 0
INT5[15:0] 5
INTO[31:0] 0
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0
INT5_pipeline_1[15:0] 5
INTD_pipeline_1[15:0] 1
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0
INT5_pipeline_2[15:0] 0


Name
Value
4,800 ns
5,000 ns
5,200 ns
Inputs
clk 1
rst 0
A[15:0] 0
B[15:0] 0
C[15:0] 0
D[15:0] 1
Output
O[31:0] 0
Original Internal Signals
INTA[15:0] 0
INTB[15:0] 0
INTC[15:0] 0
INTD[15:0] 1
INT1[17:0] 0
INT2[31:0] 0
INT3[31:0] 0
INT4[31:0] 0
INT5[15:0] 5
INTO[31:0] 0
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0
INT5_pipeline_1[15:0] 5
INTD_pipeline_1[15:0] 1
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0
INT5_pipeline_2[15:0] 0

```
run 5 us
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 3760 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 3840 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 3920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 4 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 4080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 4160 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 4240 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793
```

```
Time: 4320 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 4400 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 4480 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548

Time: 4560 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153384
Predicted value
O: 153384
```

```
Time: 4640 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 4720 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 4800 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745

Time: 4880 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4

Time: 4960 ns
```

2.2.2

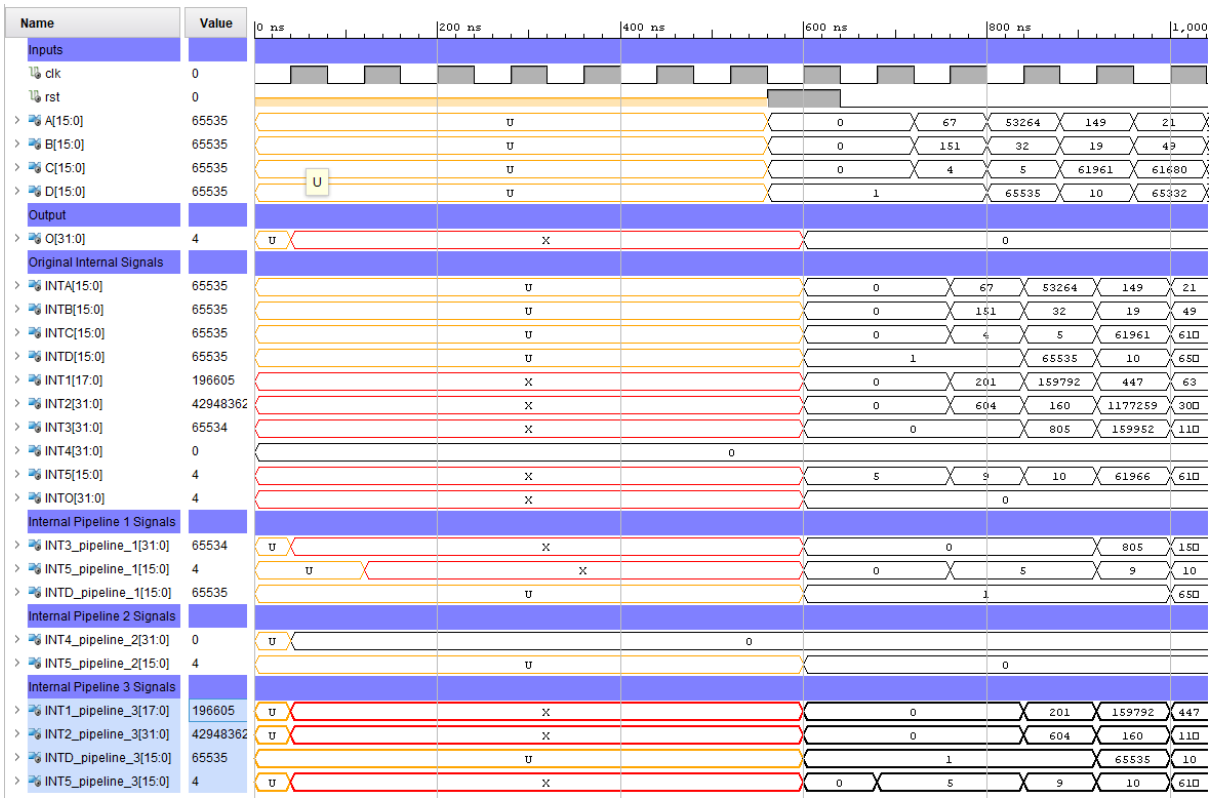
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								1015	2421	0.00	0	0
impl_1	constrs_1	route_design Complete, Failed Timing!	0.356	0.000	-0.050	-0.131	0.000	0.148	0	987	2339	0.00	0	0

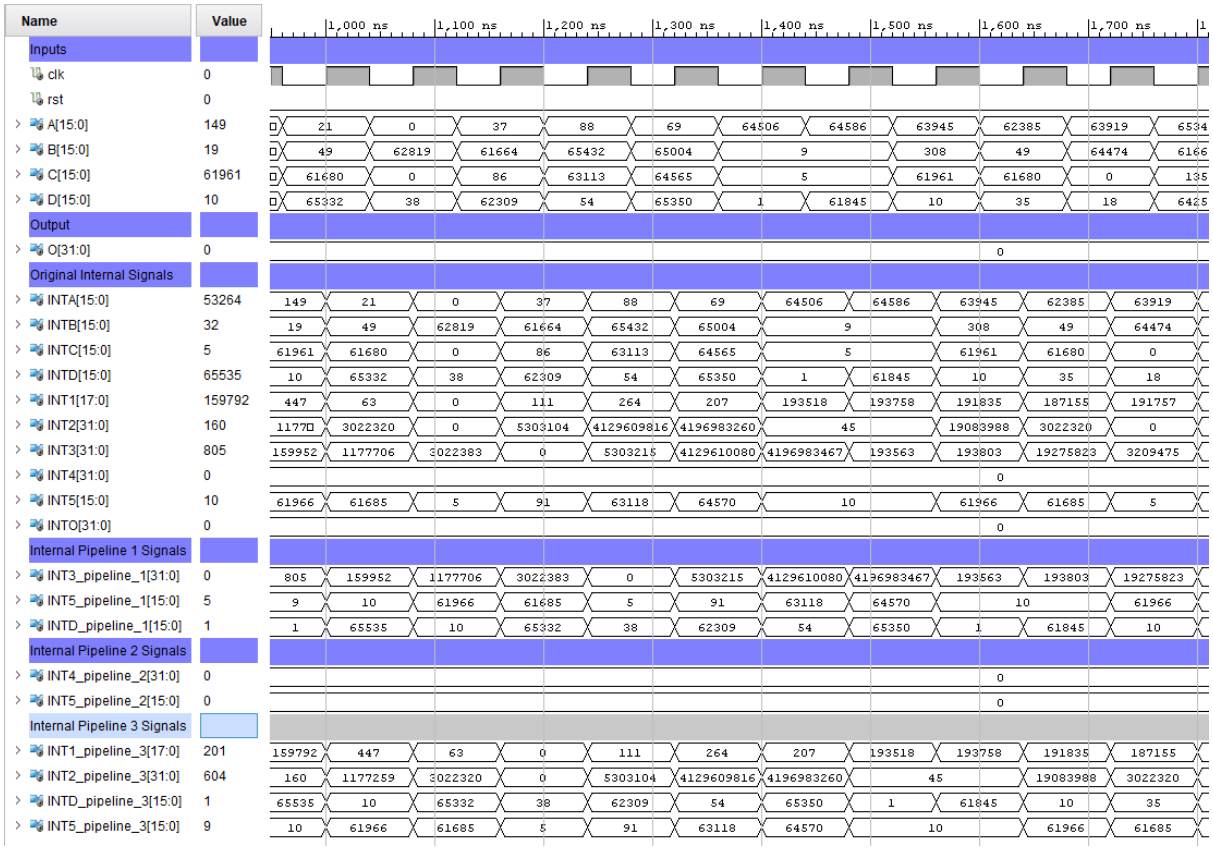
```
create_clock -period 15.000 -name clk -waveform {0.000 7.5000} [get_ports clk]
```

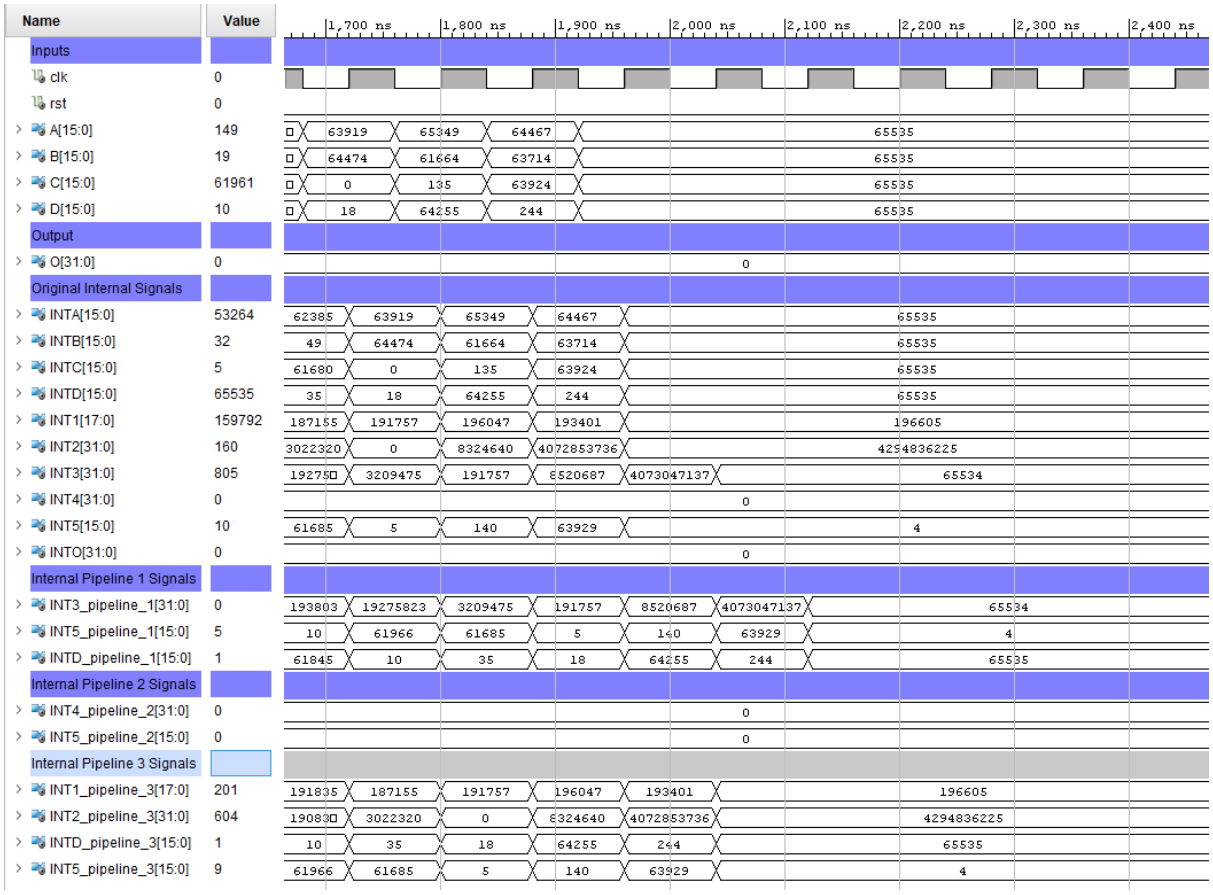
2.2.3

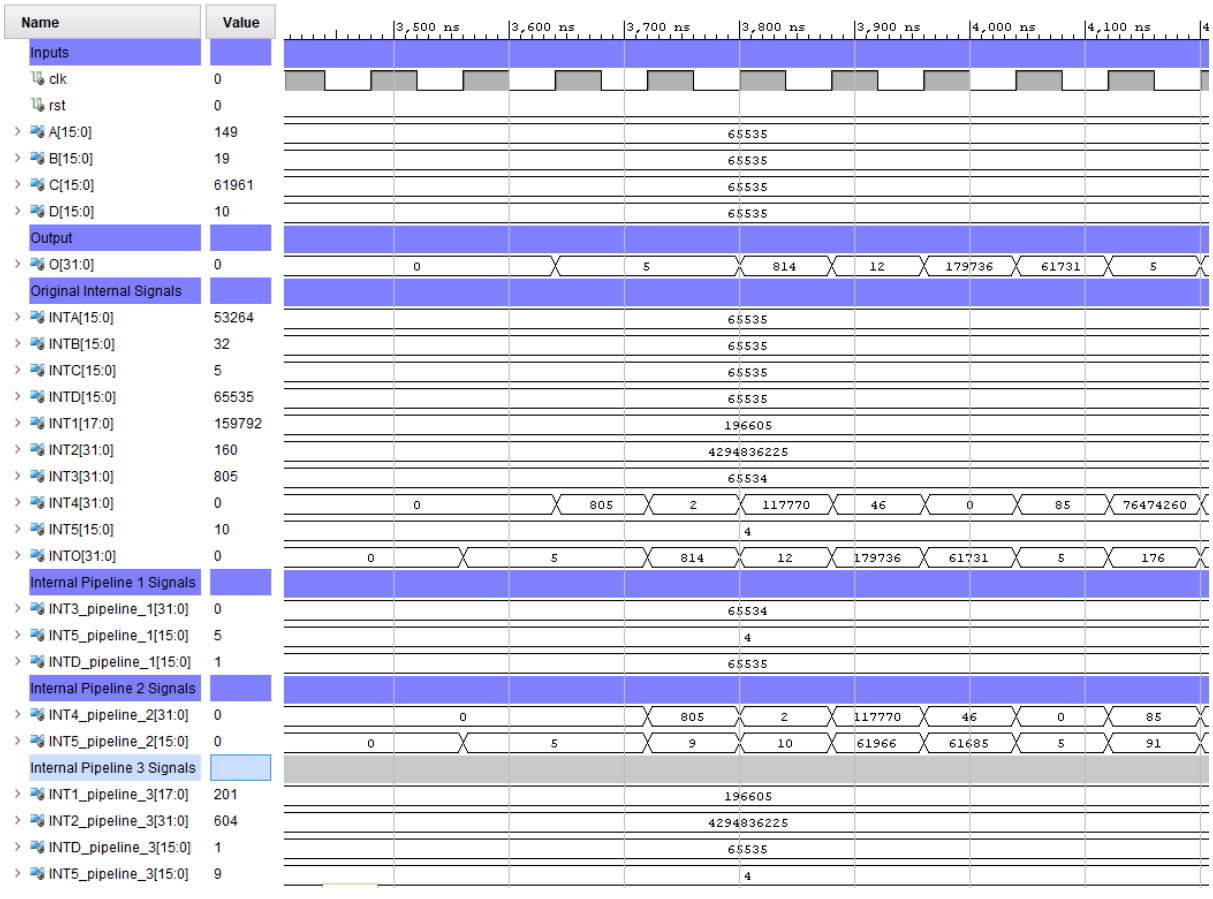
A setup violation occurs when the circuit cannot meet the setup criteria specified by the designer, in this case the setup violations that occurred from testing were the clock period being defined as above. When the circuit could not meet the specified clock period a violation occurs.

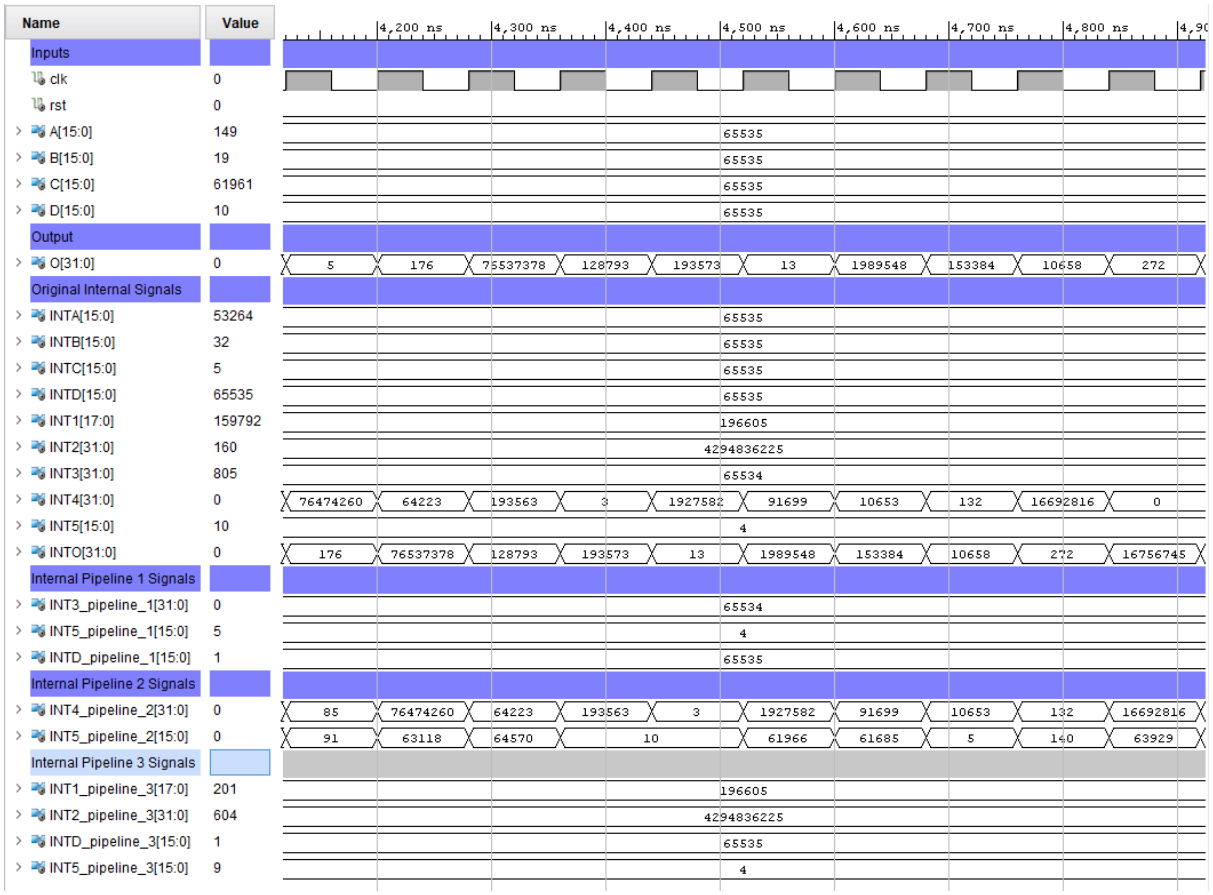
2.2.4

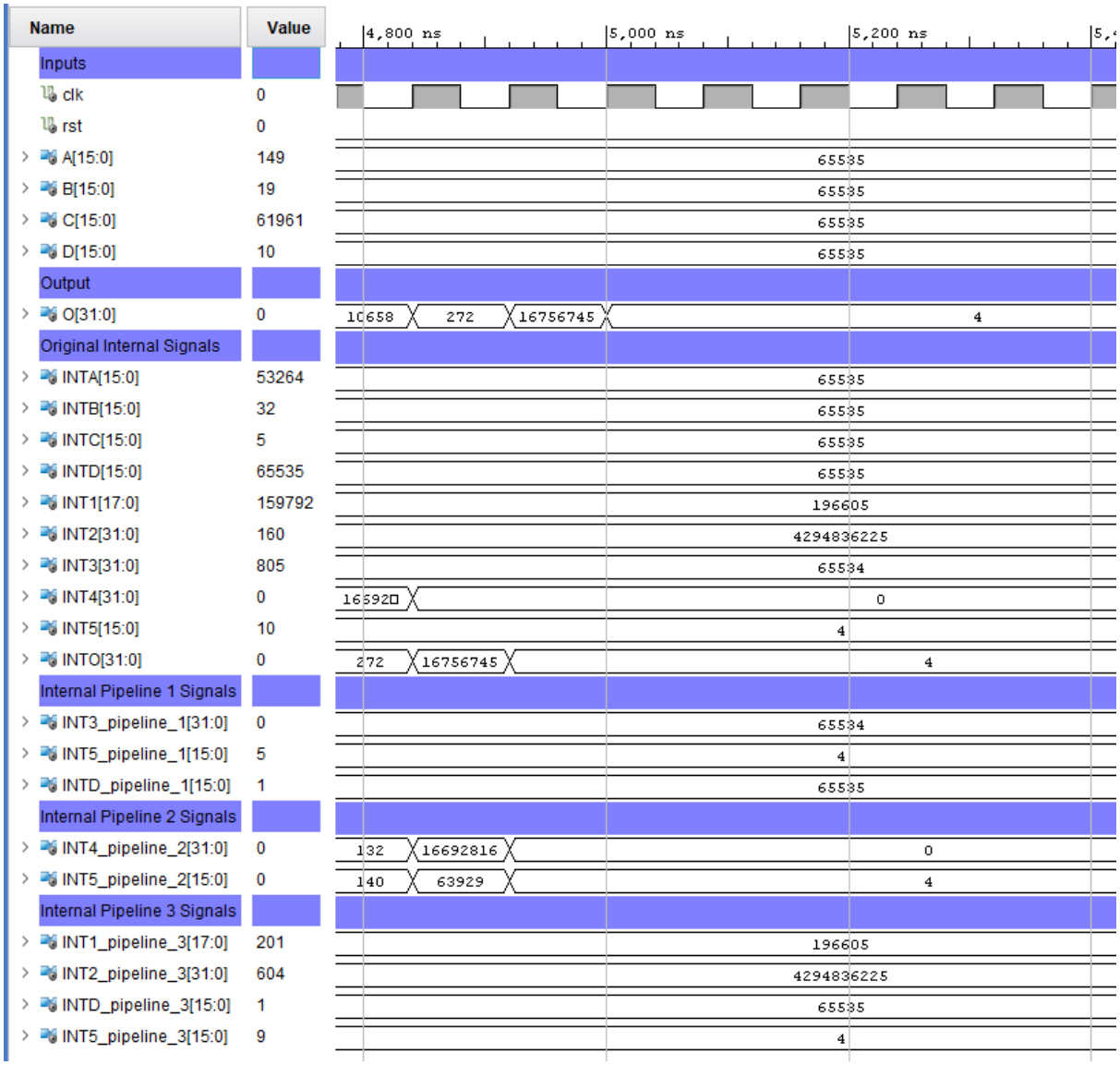

Name
Value
0 ns
200 ns
400 ns
600 ns
800 ns
1,000
Inputs
clk 0
rst 0
A[15:0] 65535
B[15:0] 65535
C[15:0] 65535
D[15:0] 65535
Output
O[31:0] 4
Original Internal Signals
INTA[15:0] 65535
INTB[15:0] 65535
INTC[15:0] 65535
INTD[15:0] 65535
INT1[17:0] 196605
INT2[31:0] 42948362
INT3[31:0] 65534
INT4[31:0] 0
INT5[15:0] 4
INTO[31:0] 4
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 65534
INT5_pipeline_1[15:0] 4
INTD_pipeline_1[15:0] 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0
INT5_pipeline_2[15:0] 4
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] 196605
INT2_pipeline_3[31:0] 42948362
INTD_pipeline_3[15:0] 65535
INT5_pipeline_3[15:0] 4


Name
Value
1,000 ns
1,100 ns
1,200 ns
1,300 ns
1,400 ns
1,500 ns
1,600 ns
1,700 ns
Inputs
clk 0
rst 0
A[15:0] 149
B[15:0] 19
C[15:0] 61961
D[15:0] 10
Output
O[31:0] 0
Original Internal Signals
INTA[15:0] 53264
INTB[15:0] 32
INTC[15:0] 5
INTD[15:0] 65535
INT1[17:0] 159792
INT2[31:0] 160
INT3[31:0] 805
INT4[31:0] 0
INT5[15:0] 10
INTO[31:0] 0
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0
INT5_pipeline_1[15:0] 5
INTD_pipeline_1[15:0] 1
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0
INT5_pipeline_2[15:0] 0
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] 201
INT2_pipeline_3[31:0] 604
INTD_pipeline_3[15:0] 1
INT5_pipeline_3[15:0] 9


Name
Value
1,700 ns
1,800 ns
1,900 ns
2,000 ns
2,100 ns
2,200 ns
2,300 ns
2,400 ns
Inputs
clk 0
rst 0
A[15:0] 149 63919 65349 64467 65535
B[15:0] 19 64474 61664 63714 65535
C[15:0] 61961 0 135 63924 65535
D[15:0] 10 18 64255 244 65535
Output
O[31:0] 0 0
Original Internal Signals
INTA[15:0] 53264 62385 63919 65349 64467 65535
INTB[15:0] 32 49 64474 61664 63714 65535
INTC[15:0] 5 61680 0 135 63924 65535
INTD[15:0] 65535 35 18 64255 244 65535
INT1[17:0] 159792 187155 191757 196047 193401 196605
INT2[31:0] 160 3022320 0 8324640 4072853736 4294836225
INT3[31:0] 805 19275 3209475 191757 8520687 4073047137 65534
INT4[31:0] 0 0
INT5[15:0] 10 61685 5 140 63929 4
INTO[31:0] 0 0
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 193803 19275823 3209475 191757 8520687 4073047137 65534
INT5_pipeline_1[15:0] 5 10 61966 61685 5 140 63929 4
INTD_pipeline_1[15:0] 1 61845 10 35 18 64255 244 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 0
INT5_pipeline_2[15:0] 0 0
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] 201 191835 187155 191757 196047 193401 196605
INT2_pipeline_3[31:0] 604 19083 3022320 0 8324640 4072853736 4294836225
INTD_pipeline_3[15:0] 1 10 35 18 64255 244 65535
INT5_pipeline_3[15:0] 9 61966 61685 5 140 63929 4


Name
Value
3,500 ns
3,600 ns
3,700 ns
3,800 ns
3,900 ns
4,000 ns
4,100 ns
Inputs
clk 0
rst 0
A[15:0] 149 65535
B[15:0] 19 65535
C[15:0] 61961 65535
D[15:0] 10 65535
Output
O[31:0] 0 0 5 814 12 179736 61731 5
Original Internal Signals
INTA[15:0] 53264 65535
INTB[15:0] 32 65535
INTC[15:0] 5 65535
INTD[15:0] 65535 65535
INT1[17:0] 159792 196605
INT2[31:0] 160 4294836225
INT3[31:0] 805 65534
INT4[31:0] 0 0 805 2 117770 46 0 85 76474260
INT5[15:0] 10 4
INTO[31:0] 0 0 5 814 12 179736 61731 5 176
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 65534
INT5_pipeline_1[15:0] 5 4
INTD_pipeline_1[15:0] 1 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 0 805 2 117770 46 0 85
INT5_pipeline_2[15:0] 0 0 5 9 10 61966 61685 5 91
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] 201 196605
INT2_pipeline_3[31:0] 604 4294836225
INTD_pipeline_3[15:0] 1 65535
INT5_pipeline_3[15:0] 9 4


Name
Value
4,200 ns
4,300 ns
4,400 ns
4,500 ns
4,600 ns
4,700 ns
4,800 ns
Inputs
clk 0
rst 0
A[15:0] 149 65535
B[15:0] 19 65535
C[15:0] 61961 65535
D[15:0] 10 65535
Output
O[31:0] 0 5 176 75537378 128793 193573 13 1989548 153384 10658 272
Original Internal Signals
INTA[15:0] 53264 65535
INTB[15:0] 32 65535
INTC[15:0] 5 65535
INTD[15:0] 65535 65535
INT1[17:0] 159792 196605
INT2[31:0] 160 4294836225
INT3[31:0] 805 65534
INT4[31:0] 0 76474260 64223 193563 3 1927582 91699 10653 132 16692816 0
INT5[15:0] 10 4
INTO[31:0] 0 176 76537378 128793 193573 13 1989548 153384 10658 272 16756745
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0 65534
INT5_pipeline_1[15:0] 5 4
INTD_pipeline_1[15:0] 1 65535
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0 85 76474260 64223 193563 3 1927582 91699 10653 132 16692816
INT5_pipeline_2[15:0] 0 91 63118 64570 10 61966 61685 5 140 63929
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] 201 196605
INT2_pipeline_3[31:0] 604 4294836225
INTD_pipeline_3[15:0] 1 65535
INT5_pipeline_3[15:0] 9 4


Name
Value
4,800 ns
5,000 ns
5,200 ns
Inputs
clk 0
rst 0
A[15:0] 149
B[15:0] 19
C[15:0] 61961
D[15:0] 10
Output
O[31:0] 0
Original Internal Signals
INTA[15:0] 53264
INTB[15:0] 32
INTC[15:0] 5
INTD[15:0] 65535
INT1[17:0] 159792
INT2[31:0] 160
INT3[31:0] 805
INT4[31:0] 0
INT5[15:0] 10
INTO[31:0] 0
Internal Pipeline 1 Signals
INT3_pipeline_1[31:0] 0
INT5_pipeline_1[15:0] 5
INTD_pipeline_1[15:0] 1
Internal Pipeline 2 Signals
INT4_pipeline_2[31:0] 0
INT5_pipeline_2[15:0] 0
Internal Pipeline 3 Signals
INT1_pipeline_3[17:0] 201
INT2_pipeline_3[31:0] 604
INTD_pipeline_3[15:0] 1
INT5_pipeline_3[15:0] 9
65535
10658
272
16756745
4
16592
0
65534
16692816
132
140
63929
196605
4294836225

```
run 5 us
Error:
test_vectors value 0

for inputs
A: 67
B: 151
C: 4
D: 1

for outputs
Actual value
O: 814
Predicted value
O: 814

Time: 3840 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 1

for inputs
A: 53264
B: 32
C: 5
D: 65535

for outputs
Actual value
O: 12
Predicted value
O: 12

Time: 3920 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 2

for inputs
A: 149
B: 19
C: 61961
D: 10

for outputs
Actual value
O: 179736
Predicted value
O: 179736

Time: 4 us  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 3

for inputs
A: 21
B: 49
C: 61680
D: 65332

for outputs
Actual value
O: 61731
Predicted value
O: 61731
```

```
Time: 4080 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 4

for inputs
A: 0
B: 62819
C: 0
D: 38

for outputs
Actual value
O: 5
Predicted value
O: 5

Time: 4160 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 5

for inputs
A: 37
B: 61664
C: 86
D: 62309

for outputs
Actual value
O: 176
Predicted value
O: 176

Time: 4240 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 6

for inputs
A: 88
B: 65432
C: 63113
D: 54

for outputs
Actual value
O: 76537378
Predicted value
O: 76537378

Time: 4320 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 7

for inputs
A: 69
B: 65004
C: 64565
D: 65350

for outputs
Actual value
O: 128793
Predicted value
O: 128793
```

```
Time: 4400 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 8

for inputs
A: 64506
B: 9
C: 5
D: 1

for outputs
Actual value
O: 193573
Predicted value
O: 193573

Time: 4480 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 9

for inputs
A: 64586
B: 9
C: 5
D: 61845

for outputs
Actual value
O: 13
Predicted value
O: 13

Time: 4560 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 10

for inputs
A: 63945
B: 308
C: 61961
D: 10

for outputs
Actual value
O: 1989548
Predicted value
O: 1989548

Time: 4640 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 11

for inputs
A: 62385
B: 49
C: 61680
D: 35

for outputs
Actual value
O: 153384
Predicted value
O: 153384
```

```
Time: 4720 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 12

for inputs
A: 63919
B: 64474
C: 0
D: 18

for outputs
Actual value
O: 10658
Predicted value
O: 10658

Time: 4800 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 13

for inputs
A: 65349
B: 61664
C: 135
D: 64255

for outputs
Actual value
O: 272
Predicted value
O: 272

Time: 4880 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 14

for inputs
A: 64467
B: 63714
C: 63924
D: 244

for outputs
Actual value
O: 16756745
Predicted value
O: 16756745

Time: 4960 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
Error:
test_vectors value 15

for inputs
A: 65535
B: 65535
C: 65535
D: 65535

for outputs
Actual value
O: 4
Predicted value
O: 4

Time: 5040 ns  Iteration: 0  Process: /Algorithm_Lab_2A_tb/TEST_OUTPUT
```

2.2.5

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								1017	2488	0.00	0	0
impl_1	constrs_1	route_design Complete, Failed Timing!	0.546	0.000	-0.038	-0.195	0.000	0.159	0	989	2406	0.00	0	0

```
create_clock -period 12.000 -name clk -waveform {0.000 6.0000} [get_ports clk]
```

2.2.6

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_2	constrs_1	synth_design Complete!								681	2374	0.00	0	2
impl_2	constrs_1	route_design Complete!	0.128	0.000	0.062	0.000	0.000	0.258	0	664	2292	0.00	0	2

```
create_clock -period 4.000 -name clk -waveform {0.000 2.0000} [get_ports clk]
```

```
Clock  Waveform(ns)          Period(ns)      Frequency(MHz)
-----  ------------          ----------      --------------
clk    {0.000 2.000}         4.000           250.000
```

2.2.7

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use work.DigEng.all;

-- Algorithm entity
-- Synchronous calculator of the equation
-- O <= (A*3 + B*C)/D + C +5
-- 6 inputs, standard clk and reset
-- Inputs A, B, C, D std logic vector inputs of values
-- to computate.
-- output "O" is result of the equation.
-- 4 at innputs one for each value input A, B, C and D
-- 1 at output O
-- this entity has 5 sets of pipe lined registers

-- 1st Input Register input registers to store inputs
-- 2nd "pipeline 3" results of (3*A),(B*C),D,(5+C) each stored in
registers
-- 3rd "pipeline 1" results of(3*A)+(B*C), D,(5+C) each stored in
registers
-- Note* divider has 34 internal pipelined sections requiring a
-- Pipelined array of (5+C) made up of 34 registers using the FIFO
method
-- 4th "pipeline 2" results of(3*A)+(B*C)/ D,(5+C) each stored in
registers
-- 5th output registers results of((3*A)+(B*C)/ D)+(5+C) stored in
register

-- Computation of entire equation takes 41 clk clyes
-- the 41 clk cycles delay the inital result but speed up the
-- entire circuit due to the pipelined sections. They allow
-- the the time resource heavy divide and multiplication processes
-- to compute in 1 clk cycle reducing the time required for processing
-- the entire equation.
entity algorithm is
    generic (data_size     : integer := 16;
             -- number of registers in pipeline array
             Divider_Delay : integer := 34);
    Port ( A : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           B : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           C : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           D : in  STD_LOGIC_VECTOR (data_size-1 downto 0);
           O : out  STD_LOGIC_VECTOR (data_size*2-1 downto 0);
           clk : in  STD_LOGIC;
           rst : in  STD_LOGIC);
end algorithm;
```

```
architecture Behavioral of algorithm is
-- internal input between Input register & Pipeline 3
signal INTA, INTB, INTC, INTD : UNSIGNED (data_size-1 downto 0);
signal INT1 : UNSIGNED (data_size+1 downto 0);
signal INT2 : UNSIGNED (data_size*2-1 downto 0);
signal INT5 : UNSIGNED (data_size-1 downto 0);

--#########################################################
--signals between pipeline 3 & Pipeline 1
signal INT3 : UNSIGNED (data_size*2-1 downto 0);
-- signals outputs of pipeline 3
signal INT1_pipeline_3 : UNSIGNED (data_size+1 downto 0);
signal INT2_pipeline_3 : UNSIGNED (data_size*2-1 downto 0);
signal INTD_pipeline_3 : UNSIGNED (data_size-1 downto 0);
signal INT5_pipeline_3 : UNSIGNED (data_size-1 downto 0);
--#########################################################
--signals between pipeline 1 & Pipeline 2
-- signals outputs of pipeline 1
signal INT3_pipeline_1 : UNSIGNED (data_size*2-1 downto 0);
signal INT5_pipeline_1 : UNSIGNED (data_size-1 downto 0);
signal INTD_pipeline_1 : UNSIGNED (data_size-1 downto 0);
-- result of divider
signal INT4 : UNSIGNED (data_size*2-1 downto 0);
signal quotient : std_logic_vector(data_size*2-1 downto 0);
--#########################################################

--signals between pipeline 2 & output register
-- signals outputs for pipeline 2
signal INT4_pipeline_2 : UNSIGNED (data_size*2-1 downto 0);
signal INT5_pipeline_2 : UNSIGNED (data_size-1 downto 0);

--#########################################################
--signal output to peripheral
signal INTO : UNSIGNED (data_size*2-1 downto 0);
--#########################################################


-- array of registers for pipline array
-- required due to divider components internal pipline
type Pipeline_Array is array (0 to Divider_Delay -1) of UNSIGNED
(Data_size -1 downto 0);
signal INT_Pipe_Array_out : Pipeline_Array;

-- array of connections between each register of the piplione array
type Pipe_reg_array_Connect is array (0 to Divider_Delay + 1) of
UNSIGNED (Data_size -1 downto 0);
signal INT_bus_in : Pipe_reg_array_Connect;

-- component deceleration
-- synchronous divider with 34 internal pipline sections
component divider
port (
 clk: in std_logic;
 sclr: in std_logic;
 rfd: out std_logic;
 dividend: in std_logic_vector(31 downto 0);
 divisor: in std_logic_vector(15 downto 0);
 quotient: out std_logic_vector(31 downto 0);
 fractional: out std_logic_vector(15 downto 0)
 );
 end component;
```

```
begin
-- setup for individual input registers for inputs A,B, C & D
-- All Synchronous with reset to zero when reset signal active,
-- NO enable signals required.
input_regs: process (clk) is
begin
  if rising_edge(clk) then
  -- resets internal signals below to zero
    if rst = '1' then
      INTA <= (others => '0');
      INTB <= (others => '0');
      INTC <= (others => '0');
--    INTD <= (0 => '1', others => '0');  -- aggregate notation
      INTD <= to_unsigned(1,INTD'length); -- type conversion notation
    else
    -- connects inputs to internal signal values
      INTA <= unsigned(A);
      INTB <= unsigned(B);
      INTC <= unsigned(C);
      INTD <= unsigned(D);
    end if;
  end if;
end process input_regs;

-- equation maths defined per internal signals
--in between input registers and pipline 3
INT1 <= INTA * to_unsigned(3, 2);
INT2 <= INTB * INTC;
INT5 <= INTC + to_unsigned(5, INT5'length);
--in between pipline 3 and pipline 1
INT3 <= INT1_pipeline_3 + INT2_pipeline_3;
--in between pipline 2 and pipline output registers
INTO <= INT5_pipeline_2 + INT4_pipeline_2;

-- output register.
-- synchronous.
-- output = 0 at rising clk edge
-- when input reset is active.
-- output = INTO at rising clk edge.

output_regs: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
      O <= (others => '0');
    else
      O <= std_logic_vector(INTO);
    end if;
  end if;
end process output_regs;

-- pipline 1 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
```

```
pipeline_1: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT3_pipeline_1 <= (others => '0');
    INT5_pipeline_1 <= (others => '0');
    INTD_pipeline_1 <= to_unsigned(1,INTD'length); -- type conversion
notation
    else
    INT3_pipeline_1 <= INT3;
    INT5_pipeline_1 <= INT5_pipeline_3;
    INTD_pipeline_1 <= INTD_pipeline_3;
    end if;
  end if;
end process pipeline_1;

-- pipline 2 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.
pipeline_2: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT4_pipeline_2 <= (others => '0');
    INT5_pipeline_2 <= (others => '0');
    else
    INT4_pipeline_2 <= INT4;
    -- final output of pipeline array input to pipeline 2
    INT5_pipeline_2 <=  INT_Pipe_Array_out(Divider_Delay-1);
    end if;
  end if;
end process pipeline_2;

-- pipline 3 registers
-- synchronous.
-- NO enable
-- outputs = 0 at rising clk edge
-- when input reset is active.
-- output data = input data at rising clk edge.

pipeline_3: process (clk) is
begin
  if rising_edge(clk) then
    if rst = '1' then
    INT1_pipeline_3 <= (others => '0');
    INT2_pipeline_3 <= (others => '0');
    INT5_pipeline_3 <= (others => '0');
    INTD_pipeline_3 <= to_unsigned(1,INTD'length); -- type conversion
notation
    else
    INT1_pipeline_3 <= INT1;
    INT2_pipeline_3 <= INT2;
    INT5_pipeline_3 <= INT5;
    INTD_pipeline_3 <= INTD;

    end if;
  end if;
end process pipeline_3;
```

```
--Xilinx piplined (x34)divider
-- synchronous
-- reset high output = 0
-- input dividend / input divisor
-- quotient = output value
my_divider : divider
 port map (
 clk => clk,
 sclr => rst,
 dividend => std_logic_vector(INT3_pipeline_1),
 divisor => std_logic_vector(INTD_pipeline_1),
 quotient => quotient
 );

 -- internal 4 connection to result of divider
 INT4 <= unsigned(quotient);
--Connect input to pipeline array
 INT_bus_in(0) <=INT5_pipeline_1;


--pipe lined array deceleration
-- array of the registers that make up the pipeline
-- generated to match the 34 pipelined sections inside the
--divider to keep all of the data synchronised
Pipeline_Array_registers: for i in 0 to Divider_Delay - 1 generate
D_type_flip_flop: entity work.D_type_FF
generic map(Data_Size => Data_Size)
Port Map(
         clk => clk,
         rst => rst,
         Data_In => INT_bus_in (i) ,
         Data_Out =>INT_Pipe_Array_out(i)
        );
-- connections between register outputs to next input.
INT_bus_in(i+1) <= INT_Pipe_Array_out(i)  ;
end generate;

end Behavioral;
```

```
---------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
          2 Input     32 Bit       Adders := 1
          2 Input     16 Bit       Adders := 1
+---Registers :
                      32 Bit     Registers := 2
                      16 Bit     Registers := 43
---------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------
---------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
Hierarchical RTL Component report
Module algorithm
Detailed RTL Component Info :
+---Adders :
          2 Input     32 Bit       Adders := 1
          2 Input     16 Bit       Adders := 1
+---Registers :
                      32 Bit     Registers := 2
                      16 Bit     Registers := 9
Module D_type_ff
Detailed RTL Component Info :
+---Registers :
                      16 Bit     Registers := 1
---------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
```