FRONT PAGE

ENGINEERING TRIPOS PART IIA

ELECTRICAL AND INFORMATION ENGINEERING TEACHING LABORATORY

EXPERIMENT 3B5

THE SCHOTTKY BARRIER DIODE

You should read this handout and understand the theory BEFORE the lab session. If you can, please bring your laptop to the lab with Excel installed, as this will allow you to enter/process data directly using the Excel data template file on the 3B5 Moodle page. Please be aware how to obtain uncertainty measures on slope and intercept of a Least Squares Fit (see Moodle link on this).

To book a lab session, please use the online booking page at http://to.eng.cam.ac.uk/teaching/apps/cuedle/index.php?context=3B5

INTRODUCTION

The Schottky barrier diode (SBD) is the simplest form of solid-state device. It is a two-terminal device made from a junction between a metal and a semiconductor. It is used for radio frequency and high-power applications and, of great importance for this experiment, for the characterisation of semiconducting materials.

Rectification for metal-semiconductor contacts was discovered by Ferdinand Braun in 1874. A basic model for such interfaces was formulated more than 60 years later by Walter Schottky. You might be familiar with solid state diodes as an electronic building block already, but the objective of this experiment is to explore their inner life and learn about the fundamental differences between a Schottky barrier diode and a standard p-n junction diode.

You will discuss basic aspects of SBD fabrication with your lab demonstrator. You will use an oscillator circuit to investigate the voltage dependence of the diode capacitance. This allows an estimation of the doping density of the semiconductor (Part I – allow approx. 1h). You will compare the current-voltage characteristics of Schottky and p-n diodes and confirm experimentally the theory given in lectures and assess the degree to which a diode can be regarded as ideal (Part II – also approx. 1h).

BACKGROUND TO SEMICONDUCTOR DIODES

This lab might precede the module 3B5 lectures that introduce semiconductor band theory; hence this section is meant to give you some background knowledge. It is strongly recommended that you additionally read literature, e.g. the corresponding paragraphs in Streetman B.G. "*Solid state electronic devices*", BEFORE you start the experiment.

For an ideal interface, the contact behaviour is determined by the difference in work functions. The work function is analogous to the material's "hold" on an electron; a metal with a large work function has a stronger "grip" on its electrons. When two metals A and B with work functions $\Phi_A < \Phi_B$ are brought in contact,

electrons will flow towards B until a contact potential $V_C = (\Phi_A - \Phi_B)/e$ builds up that will oppose this flow.

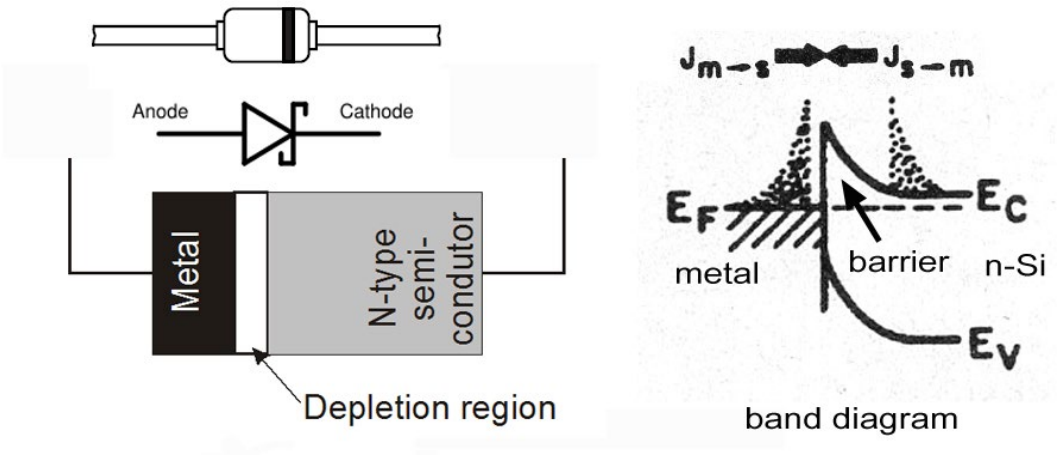


Figure 1 *Schematic of Schottky barrier diode and corresponding band diagram with no bias applied.*

The properties of a metal(m)-semiconductor(sc) junction depend on the type of semiconductor (n- or p-type) and the work functions, Φ_m and Φ_{SC} respectively. For the purposes of this experiment, only the case of the metal in contact with an n-type semiconductor is considered. In this case, if $\Phi_m > \Phi_{SC}$, a transfer of electrons occurs from the semiconductor to the metal. This creates a potential difference – the **built in potential** of the junction V_0 – which balances the difference in the work functions, so that

$$V_0 = \frac{\Phi_m - \Phi_{sc}}{e} \qquad \text{(L.1)}$$

where *e* is the magnitude of the electronic charge.

Compared to a metal, a semiconductor has a small electron density and hence the charge transfer creates a **depletion region** in the semiconductor at the interface with the metal (see Fig.1). Note that depletion in the metal is negligible, hence a contact between two metals is ohmic. *Think how you would create an ohmic contact to a semiconductor, noting that the contact to the other end of the semiconductor in the SBD is ohmic.*

The *depletion* region behaves like an insulator as there are no free carriers present – all of the n-type dopants have been stripped of their free electron to form positively charged ions that are locked in the crystalline lattice and cannot move. Hence, the SBD has a capacitance associated with it, which (in analogy to a parallel plate capacitor) varies inversely with the width of this depletion (or insulating) region.

The work function difference $\Phi_m - \Phi_{SC}$ represents a barrier to electron flow from the semiconductor to the metal (see Fig.1). This barrier will vary with an externally applied bias. For electron flow in the other direction, i.e. from the metal to the semiconductor, the barrier is (slightly) higher and more importantly *does **not** vary* with applied bias.

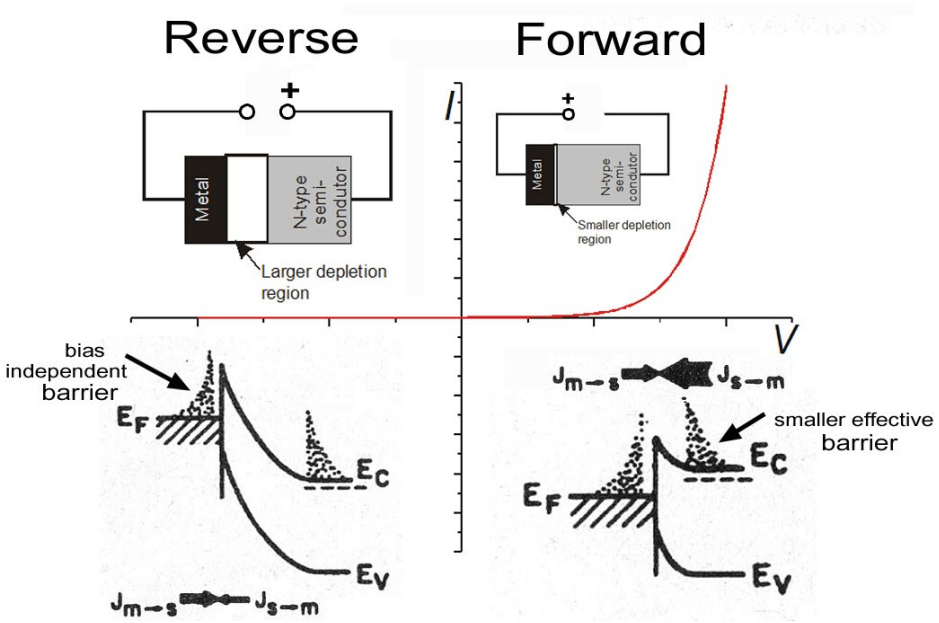


Figure 2 *Schottky barrier diode under bias. Note the variation in depletion width and the change in effective barrier height for electron flow from the semiconductor to the metal ($J_{s\text{-}m}$). Note also that $J_{m\text{-}s}$ does not vary with bias.*

Any externally applied bias will appear primarily across the high resistivity depletion region. A positive voltage V on the metal will counteract the built in potential V_0 and will cause the depletion region to decrease in width. Such a forward bias will also lower the barrier for current flow from the semiconductor to the metal (see Fig. 2). On the other hand, a negative voltage V on the metal will enhance the effect of V_0, increase the width of the depletion region and increase the barrier for current flow from the semiconductor to the metal. As the barrier height for electron flow from the metal to the semiconductor is not dependent on bias, only a very small current, called the reverse saturation current, I_s, flows (see Fig. 2).

The ideal expression for current flow, I_F, in the SBD as a function of applied bias, V, looks very similar to the exponential dependence of the p-n junction,

$$I_F = I_s \left[\exp\left(\frac{eV}{kT}\right) - 1\right] \qquad \text{(L.2)}$$

where k is the Boltzmann constant and T is the absolute temperature. However, the current is carried by electrons only, which is why an SBD is called a ***unipolar*** device. In contrast, current flow in a (*bipolar*) p-n junction relies on electrons and holes and their recombination. Therefore, an SBD has generally better high-frequency properties and a higher switching speed than typical p-n diodes.

In practice, the actual current-voltage (IV) characteristics of the SBD do not obey equation L.2, and an **ideality factor**, η, must be introduced into the expression (note the definition here, as some literature defines η differently),

$$I_F = I_s \left[exp\left(\frac{eV}{\eta kT}\right) - 1\right]. \qquad \text{(L.3)}$$

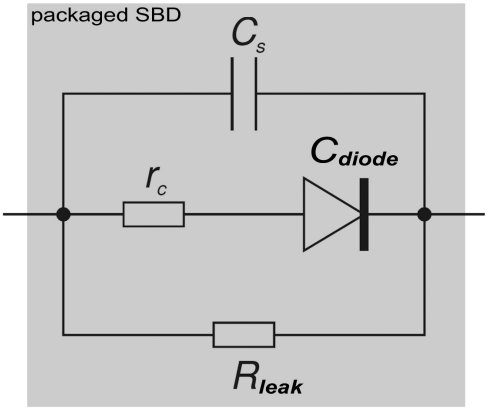


Figure 3 *Equivalent circuit of the SBD package showing the contact resistance, r_c, the stray packaging capacitance, C_s, and the packaging leakage resistance, R_{leak}.*

A further complication is that the semiconductor and the contacts of the SBD package have a series resistance, r_c (see Fig. 3). For small currents the effect of this resistance is negligible. However, for higher currents, a significant part of the applied bias is dropped across this resistance with the result that the voltage across the metal semiconductor junction itself is reduced by Ir_c, so that

$$I_F = I_s\left[exp\left(\frac{e(V-Ir_c)}{\eta kT}\right)-1\right]. \qquad \text{(L.4)}$$

As the width of the depletion region changes with applied bias, V, so does the capacitance (remember the analogy to the parallel plate capacitor). The full expression for the capacitance of the junction is given by

$$C_{diode} = A\left(\frac{\varepsilon_0\varepsilon_r eN_D}{2(V_0-V)}\right)^{1/2} \qquad \text{(L.5)}$$

where A is the cross-sectional area of the device; ε_0 and ε_r are the permittivity of free space and the relative permittivity of the semiconductor, respectively. Under reverse bias, when V is negative, the width of the depletion region is increased (see Fig. 2), and so the capacitance decreases.

Finally, the full equivalent circuit of the diode is shown in Figure 3 which includes a new leakage resistance, R_{leak}. This arises from the packaging in which the diode is mounted. The diode symbol represents the non-linear capacitance, C_{diode}. There is also an additional stray capacitance associated with the physical size and packaging of the diode, C_s. It should be noted that the resistance r_c is so small that negligible error is made if the total capacitance of the equivalent circuit, C_{SBD}, is taken as the sum of C_{diode} and C_s.

APPARATUS

You will characterise the diodes by capacitance-voltage (C-V) and current-voltage (I-V) measurements. The voltage induced changes of capacitance will be very

small (tenths of pF) and therefore an oscillator circuit is used. The circuit diagram is given in the appendix. A pair of fast transistors is configured to give an apparent negative resistance, hence if connected across a parallel LC "tank" circuit, the negative resistance compensates for the circuit resistive losses and the resonant LC oscillations do not die away. The resonant frequency f is given by:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \text{(L.6)}$$

where *L* and *C* are the inductance and capacitance, respectively, of the oscillator circuit. You can find more details on oscillator design in the 3B1 lecture notes and references therein. The oscillator is integrated on a circuit board, which allows you to connect the diode, oscillator supply voltage, bias voltage and meters for the various parts of the experiment. Some components have a pre-set chassis connection (indicated by the flat line) to ease circuit plugging.

Recording data carefully is more important than immediately working out results. If you can work out all the results as you go along, that is good and can pin-point erroneous or insufficient results, but be warned experimental time may run out. Think how many decimal points are relevant when recording and using numerical results.

EXPERIMENT 1: C-V MEASUREMENTS

The following circuit (Fig. 4) allows you to investigate how the capacitance of the SBD varies with an applied reverse bias voltage:

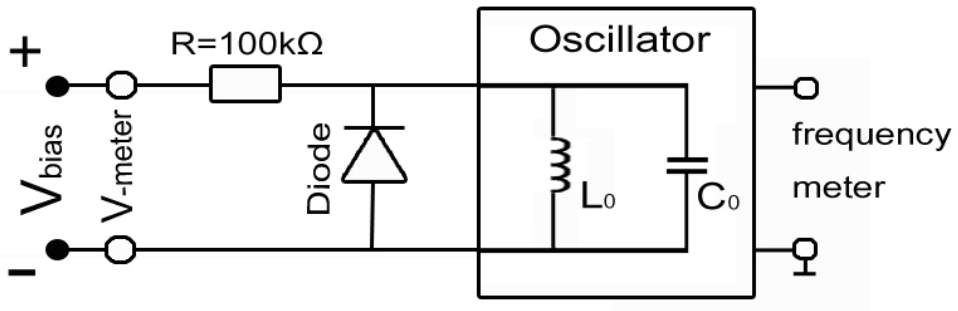


Figure 4 *Circuit diagram for CV measurement*

Follow the instructions given on page 13. You first have to measure the oscillator frequency in open circuit conditions (this does not mean no connections at all! think about bias voltage). Subsequently, measure the frequency using a reference capacitor as load. Afterwards, replace the reference capacitor with the SBD. Check the polarity and make sure that the trigger level on the frequency meter is correctly set (i.e. frequency read-out is steady) and that the oscillator power supply is switched on. Check that a variation in bias from 1 V to 12 V gives a clear frequency shift. Why does this voltage correspond to a reverse bias across the diode? Check the loading from the oscillator probes: 10× divides the signal amplitude by ten, but gives a more stable f reading, i.e. you lose signal but gain stability. Note that the attenuator switch on the frequency meter should be on 1×. Think what can contribute to the oscillator

capacitance. Wave your hands close to the diode connections and check the change in frequency. Make sure that you do a systematic experiment to minimise experimental error. Fill in the results required on pages 13 and 15 (or in the Excel data template).

EXPERIMENT 2: I-V MEASUREMENTS

A. Reverse Bias

The following circuit (Fig. 5) allows you to investigate the reverse saturation current, I_s:

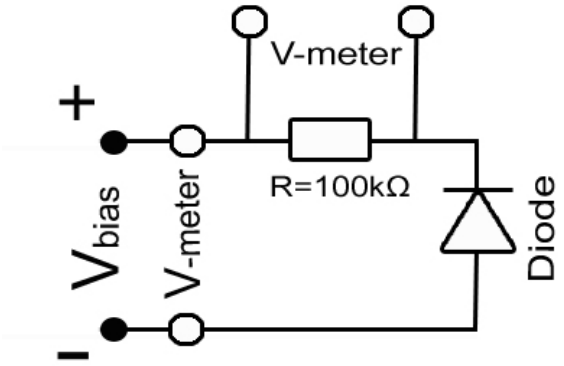


Figure 5 *Circuit diagram for IV measurements in reverse bias*

Connect the circuit and insert the SBD. Think why the meters are at the specified positions. As the reverse current is small, the current in the circuit is measured via the voltage drop across the 100 kΩ resistor. Check your multi-meter setting to get the right current conversion. Complete the column for the SBD in the table below.

Allowing for the leakage current through resistor R_{leak} whilst neglecting the series resistance r_c in Figure 3, Equation (L.4) becomes

$$I_{\text{Rev}} = I_s \left[exp\left(\frac{eV_{\text{Rev}}}{\eta kT}\right) - 1 \right] + \frac{V_{\text{Rev}}}{R_{leak}} \qquad \text{(L.7)}$$

Note, the voltmeter measures the bias voltage which is applied to a series connection of the resistor and diode. Discuss why V_{Rev} is approximately the voltage indicated by the voltmeter. Explain if the voltage drop across the resistor results in a systematic or random error for your measurement. Based on this, estimate the magnitude of error in your measurement.

Fill in the measurement sheets on pages 17 and 19 - 20 (or in the Excel data template). Now replace the SBD with the p-n diode and complete the table and measurements on pages 17 and 19 – 20 (or corresponding entries in Excel file).

B. Weak forward Bias

This regime of operation corresponds to values of eV_F (V_F is the forward voltage across the diode) which are less than about $10kT$ (kT is about 0.025 eV at room temperature). The following circuit (Fig. 6) allows you to investigate the forward current:

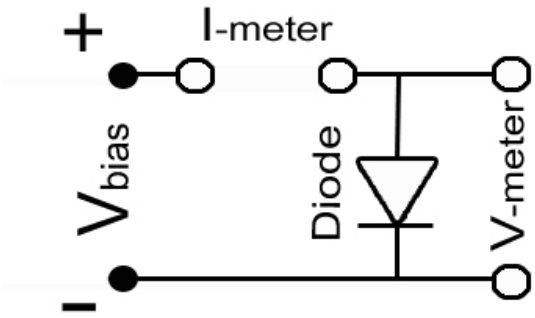


Figure 6 *Circuit diagram for IV measurements in forward bias*

Connect the circuit and insert the SBD. Think why the meters are at the specified positions. Complete the column for the SBD in the table below. Note as usual the pre-filled values for I_F (current flow through the diode) are suggestions only to indicate the range. Trying to replicate exactly will waste your time.

These results should be analysed to find the ideality factor, η. The most straightforward technique is to plot $\ln(I_F/I_S + 1)$ against V_F on the graph below. You will find that it is then possible to extract η if you rearrange equation (L.3). You should assume that the diode is operating at the temperature shown on the thermometer in the lab. ***Touch the diode with your fingers to see what happens for a temperature increase. Explain what parameter(s) in equation L.3 will dominate the temperature behaviour.***

Fill in the measurement record sheet on page 21 (or the Excel data template). Afterwards, replace the SBD with the p-n diode and complete the table and measurements on page 21 (or the Excel data template).

C. Strong forward Bias

This regime of operation corresponds to values of eV_F which are greater than ~10kT. Measurements are made in the same fashion as Experiment 2B, but at much larger currents. Insert the SBD and populate the table on page 23. Note as usual that the pre-filled values for I_F are suggestions only to indicate the range. Plot your SBD data on the graph below.

Under strong forward bias conditions, the factor of unity in equation (L.4) is negligible, and becomes

$$I_F = I_s \, exp\left(\frac{e(V_F - Ir_c)}{\eta kT}\right). \qquad \text{(L.7)}$$

Taking the natural logarithm of both sides and rearranging, gives

$$I_F r_c = V_F - \frac{\eta kT}{e} ln\left(\frac{I_F}{I_s}\right). \qquad \text{(L.8)}$$

Hence, estimate the series resistance r_c of the diode contacts and the semiconductor (see Fig. 3).

Fill in the measurement sheet on page 23 (or the Excel data template). Now replace the SBD with the p-n diode and complete the table and measurements on page 23 (or the Excel data template).

LABORATORY REPORT GUIDELINES

You must all write up this experiment as a ***short report*** for marking. Completed reports must be submitted for marking within 2 weeks of carrying out the experiment. Please see details on 3B5 lab booking pages and IIA guidelines. Short reports must be submitted online on Moodle in pdf format (3B5 course entry; please make sure the submitted file name contains your CRSID). The default latest time for handing in coursework on the deadline date is 4pm.

The report must be submitted with the official IIA coversheet, as provided on the 3B5 Lab Moodle page. The coversheet also highlights the criteria for marking. Please follow general IIA report guidelines and the specific guidelines below. Make sure your report clearly states Name, CRSID, College, Date of write up and Date of lab session.

Short reports should give a clear and concise record of the practical work you have carried out, together with appropriate discussion. The latter should highlight your understanding of the technical content, and ALL the extrapolated values should be put into context of what you expect from theory and literature. No need to repeat lab hand-outs, please focus on presentation and discussion of ALL your data. For ***short reports*** the rules are a maximum of 4 pages [single line spacing, 11 point font, including all plots/diagrams]. Please attach your original lab sheets, i.e. filled pages 13-24 (or data tables if you used your computer in lab), as appendix (this is just for reference, all relevant data should be included in main report). No further appendices are allowed. Excess length will be penalised (0.5 mark penalty per excess page). As general guideline, writing the short report should not take you longer than 3 hours. General skills such as using software to replot and fit your data (incl. statistical analysis) are expected as prior knowledge. Handwritten *short reports* are discouraged.

Experiment 3B5 may also be written up as a **Full Technical Report** (FTR). Please follow the general IIA FTR guidelines and the specific guidelines for FTRs below. The report must be submitted with the official IIA FTR coversheet (see 3B5 Lab Moodle page). The coversheet also highlights the criteria for marking. As a general guideline, the FTR should involve a further 10 hours work. FTR must include data presentation (do not refer to prior short report for data) and emphasis is on quality of the data and its presentation, structure, depth of discussion/understanding, clarity and completeness (discuss all aspects/extrapolated values and how they might link). An FTR should be of the order of, but not exceed, 10 pages of length [single line spacing, 11 point font]. Please include the (marked) short report as appendix for reference. No further appendices are allowed. FTRs must be submitted in pdf format online on Moodle (3B5) by 4 PM on Wednesday 10 December 2025.

SHORT REPORT GUIDELINES

Give a concise and clear record of the practical work and ALL data recorded, together with a data discussion and analysis that highlights your understanding and puts ALL extrapolated values into context. Consider the following core aspects:

- Use software (Excel, or any common package) to (re)plot all of your data. Use least square fitting and give errors for each extrapolated value (use the conventions for error analysis given in the appendix/Moodle). If short of time,

then it is essential to discuss the C-V curves with errors for estimating the donor density N_D.

- Calculate the atomic density of crystalline Si and give N_D as a relative value. Discuss if the magnitude of this doping density is relatively high or low in the context of semiconductor engineering of Si (put N_D for instance in context of impurity concentrations in Si crystals as lower bound; also consider the intrinsic carrier density of Si at room temperature). Explain why this particular N_D is best for a Schottky barrier diode. Outline which dopant material you would use for n-type doping of Si.
- Give a range of metals that would make a Schottky contact with n-type Si and illustrate why. Outline a reasonable choice of materials for the BAT85 SBD cross section below (Fig. 7). How would you make sure a Schottky contact is formed on one side and an Ohmic contact at the other side of the Si.
- Analyse the IV data for the p-n junction as above and compare to the SBD results. How do I_s and V_0 compare? In theory, what information about the doping density could you interpret from CV measurements for a p-n diode? Compare equation L.5 to the corresponding equation for a one-sided p-n junction.

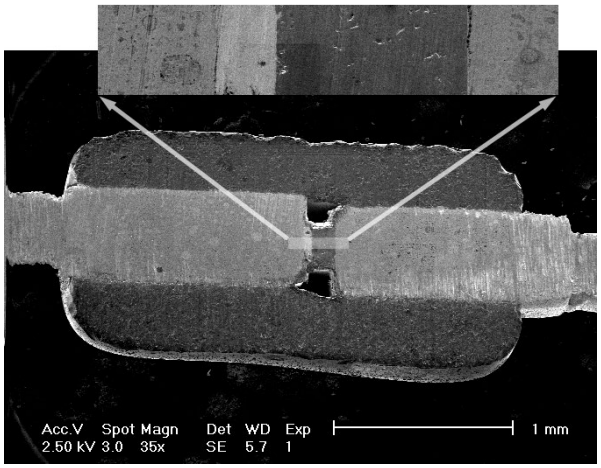


Figure 7 *Cross sectional scanning electron microscopy image of BAT85 SBD*

FULL TECHNICAL REPORT GUIDELINES

1. The FTR must be submitted online on Moodle (3B5 course entry). The FTR must be in pdf format, and please make sure the submitted file name contains your CRSID. Guidance on report writing and important general information on FTRs can be found in the IIA guide of the teaching office website:
http://teaching.eng.cam.ac.uk/information/all/part-iia/content

2. You should not require any further data than that collected during the normal two hour lab. For the FTR, a much higher quality of presentation of all data and in-depth discussion is expected. While the marked short report must be included as appendix, this is only for comparison for the marker and not for showing any results. The FTR must include all result plots, tables and diagrams within the page limit. Data should be presented in a complete, well-structured and insightful way, showing your critical thinking, wider background reading and full understanding of the results. FTR

assessment criteria include quality of presentation and data analysis, and depth of understanding.

3. In particular, for the discussion section consider the following:

a. *Discuss accuracy of measurements*. Consider the best means of extracting parameters from your data. Use a software package to give full error analysis for all your results (use the conventions for error analysis given in the appendix). Suggest complimentary techniques to analyse semiconductor doping and diode parameters.

b. *The theory of the SBD*. Explain rectification with thermionic emission theory and illustrate with band diagrams. Do not just repeat lab hand-outs or lecture notes, but show your own thinking. Compare to theory for double and one-sided p-n junction, in particular derive equations corresponding to L.1, L.2 and L.5. Explain why unipolar devices are preferred for high frequency applications.

c. *Schottky barrier height*. Discuss deviations from the ideal model, which assumes the barrier to be the difference between the work function for the metal and the electron affinity of the semiconductor. Draw band diagrams including surface states. Discuss techniques to confirm that the barrier height is 0.5 eV as assumed for the SBD. Starting with the BAT85 SBD cross section above (Fig. 7), discuss materials choices and fabrication of Schottky contacts in current IC technology.

d. *Ideality*. Discuss what causes the ideality factor to increase for an SBD. Explain the variation of η with N_d as shown in Fig. 8. Consider further how I_s and r_c vary with N_d. With this, discuss the best way to design an SBD. Then discuss differences to non-ideal behaviour of p-n diodes; what is the major reason for IV characteristics of p-n diode to differ from the ideal Shockley equation?

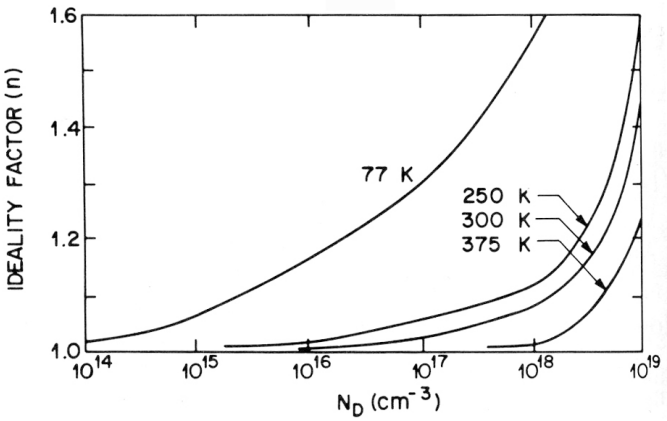


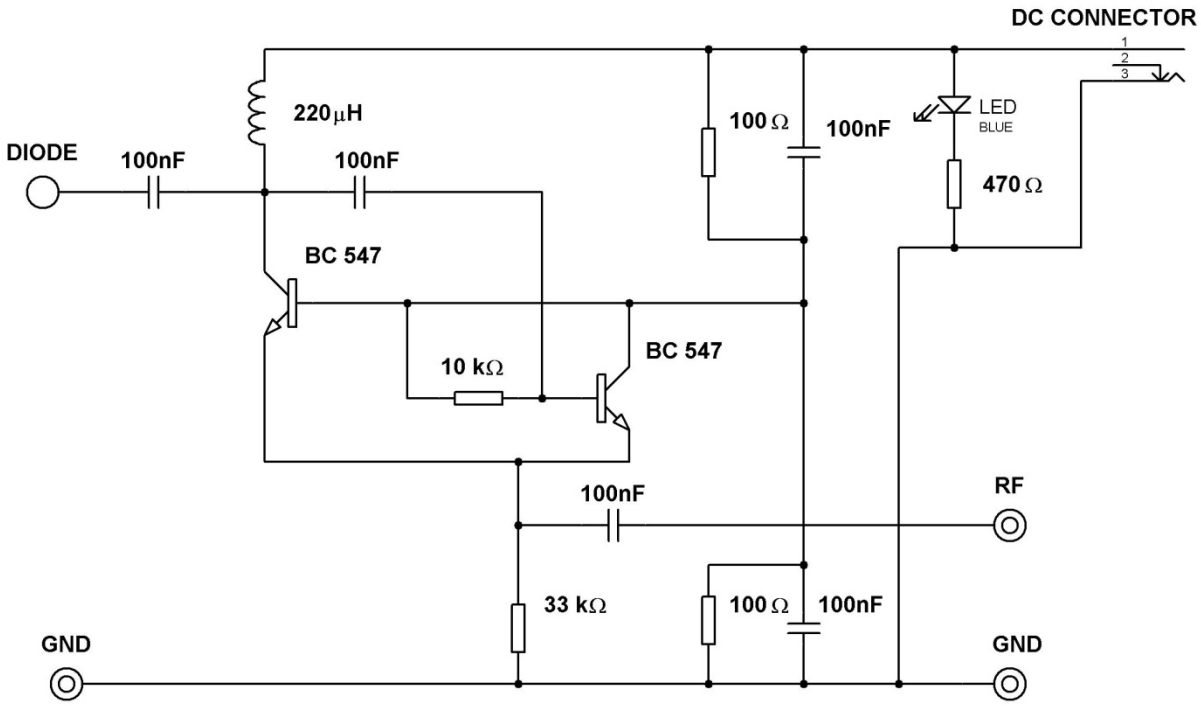
Figure 8 *V*ariation of η with N_d for SBD (from Sze S.M. *"Physics of semiconductor devices"*)

ACKNOWLEDGEMENTS

Acknowledgements to J. E. Carroll, P. Robertson, S. Tappertzhofen, B. C. Bayer, A. J. Flewitt, C. E. Maloney, W. I. Milne and R. R. Thorp. S. Hofmann, October 2024

APPENDIX

A. Oscillator circuit



B. Accuracy and Errors in Experimental Engineering

Remind yourself of the basic ideas of error analysis, see e.g. J. R. Taylor "An Introduction to Error Analysis" or CUED document “Accuracy and Errors in Experimental Engineering”.

As convention for the 3B5 lab, please state absolute errors for every estimated value, e.g. as for a = (0.23 ± 0.02) ms^{-2}.

Please see also the Excel Data Template on 3B5 Moodle

C-V Measurements record (to be attached to report)

You will notice that C_0 (which includes C_s) and L_0 are not given, hence you need two calibration measurements to be able to calculate the capacitance of the packaged SBD. Disconnect the diode and measure the frequency f_0:

f_0 = _____ [kHz]

Collect a "10pF" capacitor C_{10} from the 'box' of capacitors but note that if your wish to make accurate measurements these capacitors are best measured on the Tinsley bridge in the laboratory.

C_{10} = _____ [pf]

Then connect C_{10} and measure the frequency f_{10}:

f_{10} = _____ [kHz]

You may assume the built-in voltage, V_0, to be 0.5 V.

Frequency^2 = $f_r^2 = 1/[4\pi^2 L(C_0+C_d)]$, where the circuit and stray capacitance is C_0 and then C_d is the added capacitance (from the diode) to be measured. With neither extra capacitance nor any diode, the measured resonant frequency is f_0 corresponding to the capacitance C_0. With $C_{10} \approx 10$pF added the measured frequency is f_{10}. With the SB diode in place, then measured frequencies are f_d at reverse bias voltages $-V_{rev}$. The inductance L can be eliminated through ratios:

$(f_s^2/f_{10}^2) - 1 = (C_{10}/C_0)$ (C_{10} and C_0 in pF); $(f_s^2/f_d^2) - 1 = (C_d/C_0)$

The circuit capacitance C_0 [pF] when nothing is added is given from

$C_0 = C_{10}/[(f_0^2/f_{10}^2) - 1]$ [pF].

(NB: check and show how to get this, in your report).

You should plot out your results on the graph below to check how well the SBD satisfies equation L.5. From this graph, you should be able to extract both the stray capacitance of the SBD package, C_s (see Fig. 3), and the doping density of the semiconductor, N_D.

Note this page & all pages that have results on them must be included in your report. ***Suggested values* for reverse bias voltages or currents are always simply guidance about numbers of points to measure. Attempting to replicate these values exactly will take too much 'fiddling' with the voltage and current controls.** Note that the shaded columns always refer to experimental data, i.e. represent the minimum you have to fill in during the laboratory session.

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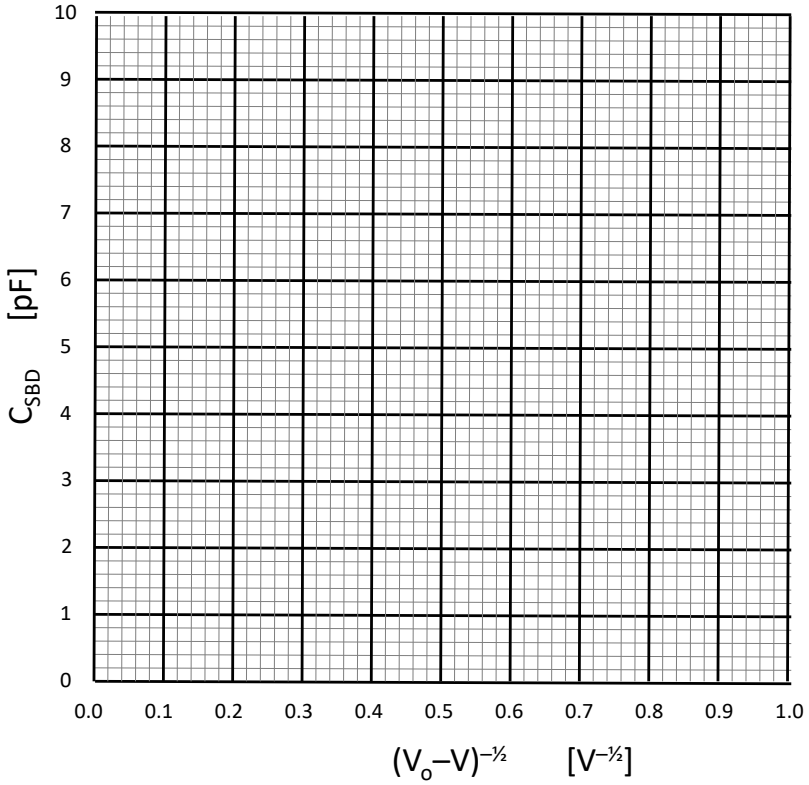
	10 pF as measured on bridge ↓	Take V_o= 0.5 V	Measured Frequency [kHz]	C_r is C_{SBD} corresponding to f_r
(+ 10pF) $V_{rev\ \ none}$	C_{10} = [pF]		f_{10}=	$C_{10}/[(f_0^2/f_{10}^2)-1]$ = ↓
(+ 0 pF) $V_{rev\ \ none}$			f_0=	C_o =
Suggested V_{rev} [V]	Measured V_{rev} [V] ↓	$(V_o-V_{rev})^{-½}$ [$V^{-½}$] ↓	f_r = ↓	C_o $[(f_0^2/f_r^2)-1]$ = C_r ↓
–12.0				
–8.0				
–5.0				
–4.0				
–3.0				
–2.0				
–1.5				
–1.0				



Assume: relative permittivity of the semiconductor, ε_r=12, area of the junction, A = 3×10^{-8} m^2.

C_s = _____pF; N_D = _____m^{-3}.

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I-V Measurements record (to be attached to report): Reverse Bias

Suggested $V_{Reverse}$ [V]	Measured SBD $V_{Reverse}$ [V]	Measured *SBD* I_{Rev} [µA]	Measured p-n $V_{Reverse}$ [V]	Measured *p-n diode* I_{Rev} [µA]
–0.25				
–0.50				
–1.0				
–2.0				
–4.0				
–6.0				
–8.0				
–10.0				
–12.0				

Plot graph next page of I_{Rev} against V_{Rev} and estimate the reverse saturation current and leakage resistance using the most linear part of your plot

I_s = ……µA

R_{leak} = ……MΩ

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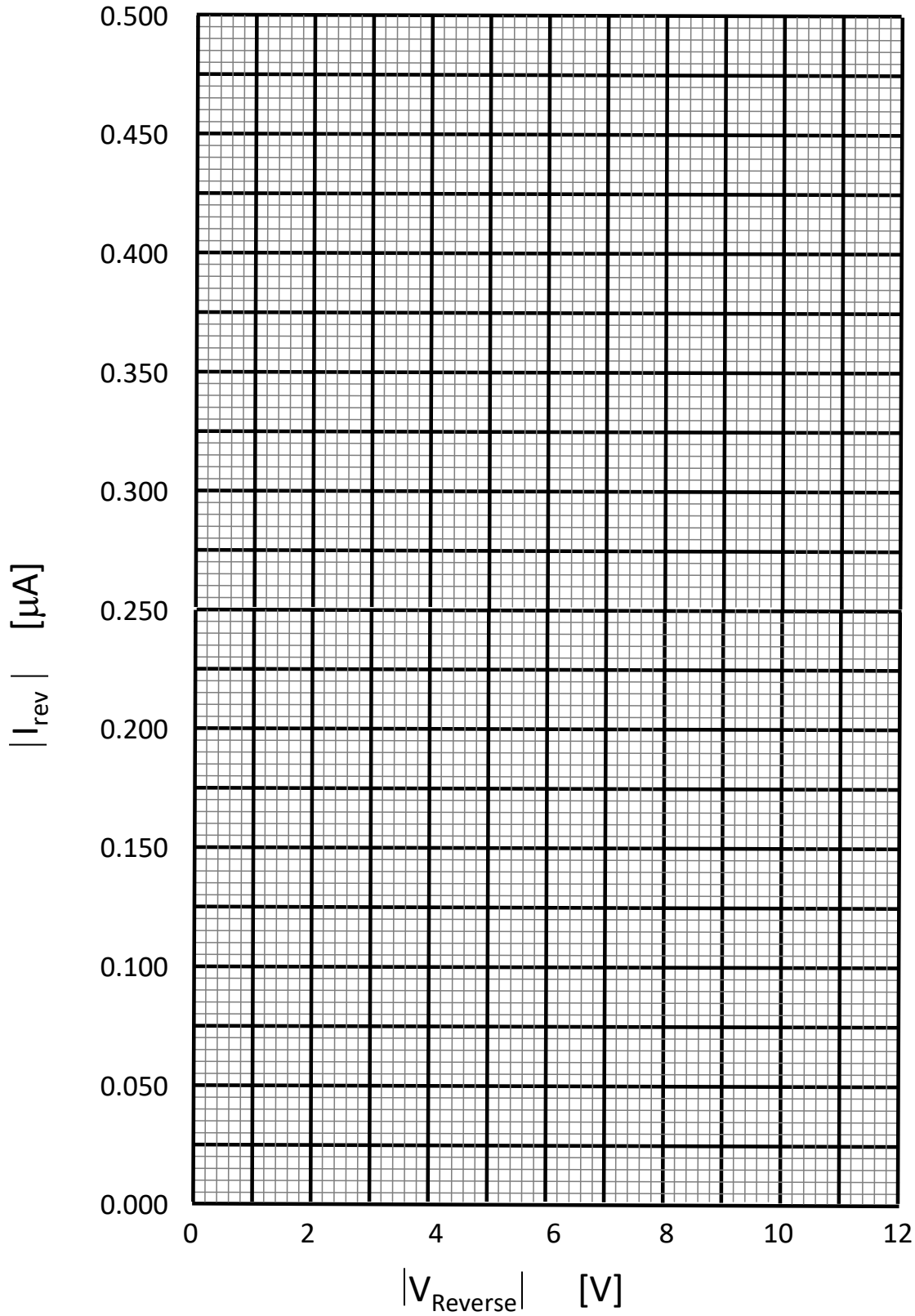
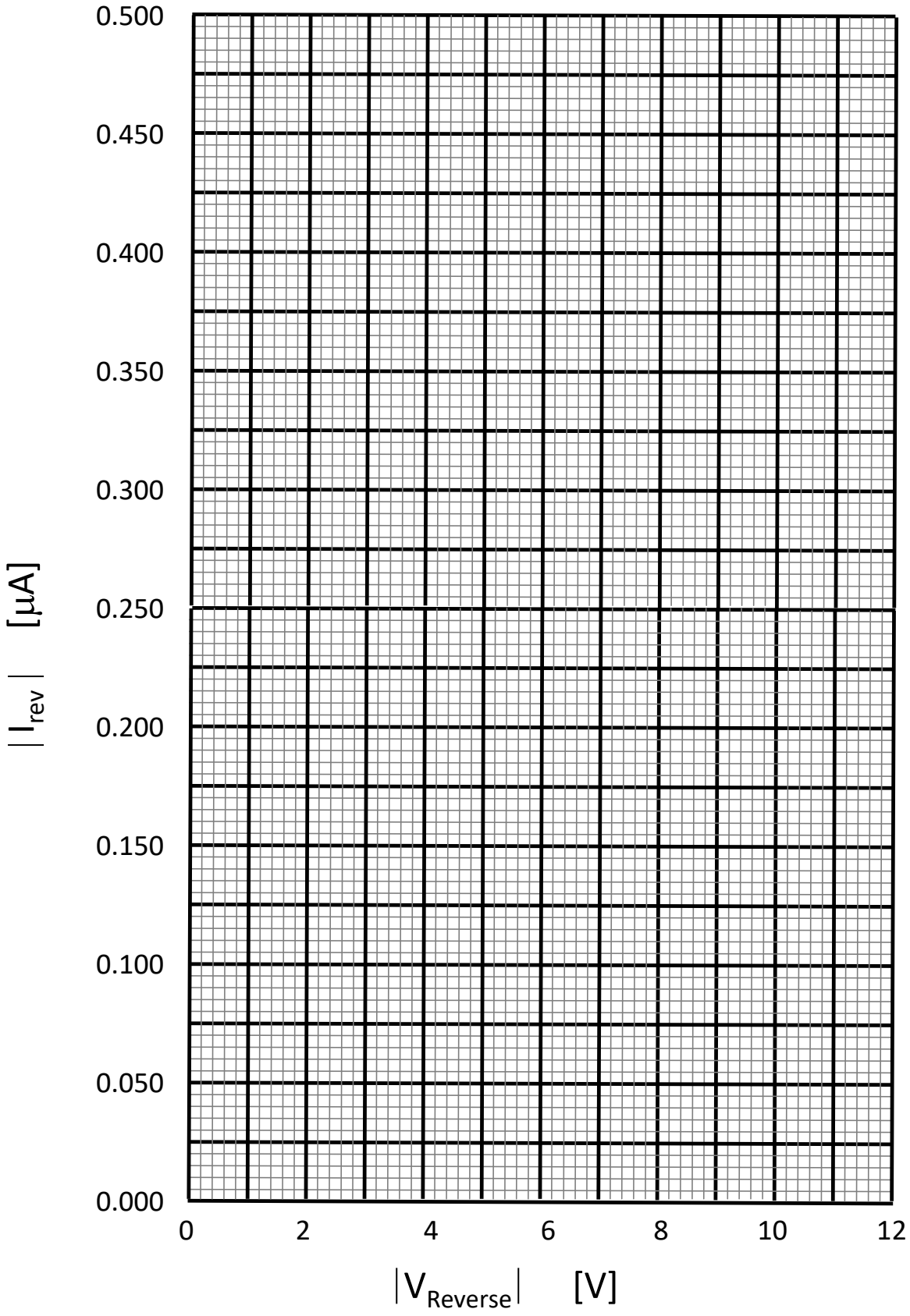


Now replace the SBD with the p-n diode and fill in the appropriate column in the table and plot p-n ***on the same graph*** which is repeated overleaf in case you need an extra copy.

Spare copy – best to have both p-n and SBD on same graph for comparison



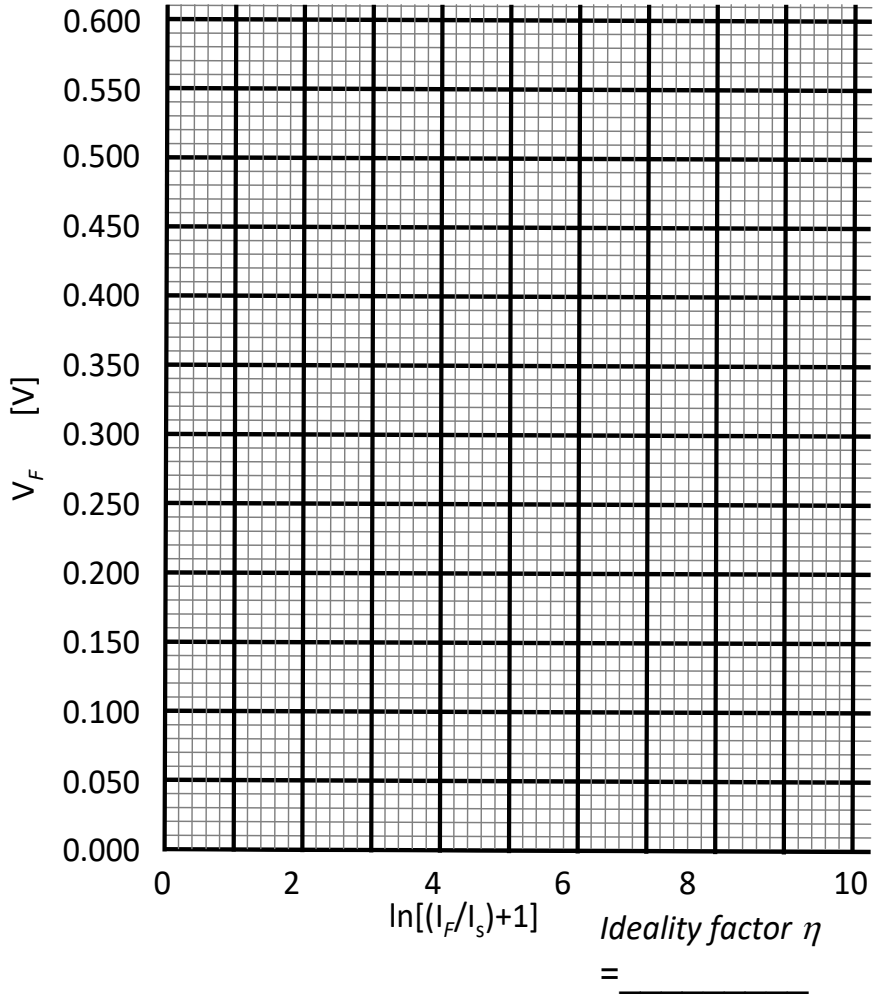
I-V Measurements record (to be attached to report): Weak Forward Bias

Temperature *T* taking temperature from thermometer in laboratory:

T _____ K :

kT/*e* = 25.68 mV at 298 K ↔ 25^0 C **(plot SBD and p-n on same graph)**

	SBD current	SBD forward voltage		p-n current	p-n forward voltage	
Suggested $I_{forward}$ [μA]	Measured $I_{forward}$ [μA]	Measured $V_{forward}$ [V]	$\ln[(I/I_s)+1]$	Measured $I_{forward}$ [μA]	Measured $V_{forward}$ [V]	$\ln[(I/I_s)+1]$
5						
10						
20						
50						
100						
200						
500						
700						



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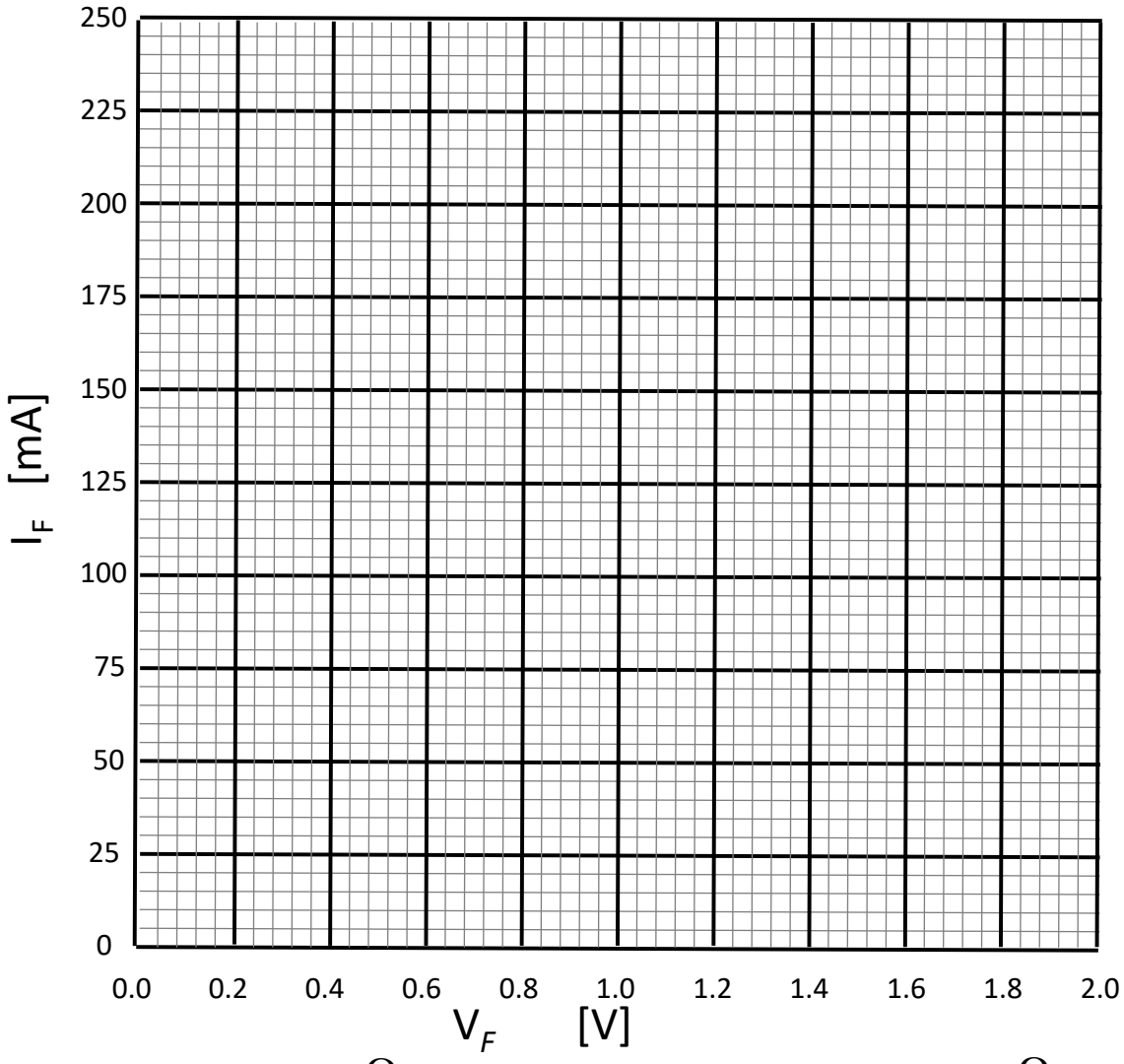
I-V Measurements record (to be attached to report): Strong Forward Bias

	SBD current	SBD forward voltage	p-n current	p-n forward voltage
Suggested $I_{forward}$ [mA]	Measured $I_{forward}$ [mA]	Measured $V_{forward}$ [V]	Measured $I_{forward}$ [mA]	Measured $V_{forward}$ [V]
10				
25				
50				
75				
100				
150				



r_{cSBD}= _____ Ω $r_{cp\text{-}n}$= _____ Ω

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