

Advanced Digital Systems Design - SVM Acceleration

Your name (Your Group)

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Some cool ideas from here[1] and there[2].

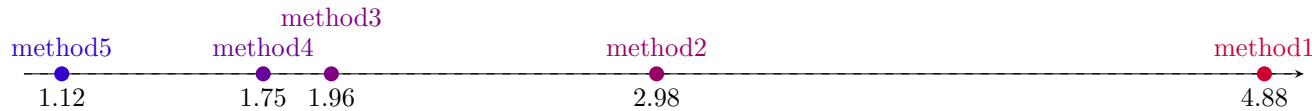


Figure 1: Software time (ms) per image on 2601 image test set

Potential: Could have put some cool text here

Observation: Some cool things occurred
Explanation: I am confidently wrong

Observation: Other cool stuff happened.
Explanation: I know, but I lack conviction

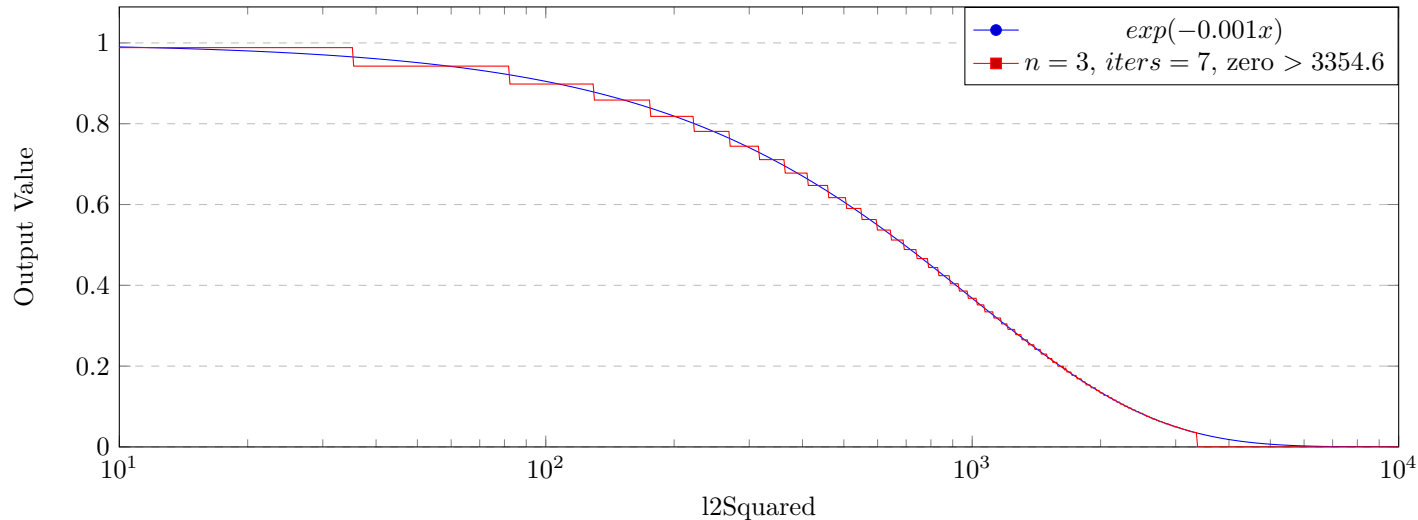


Figure 2: Comparison of Implementations of $\exp(-0.001x)$ and the modified cordic implementation

Observation: Squiggly Lines
Explanation: Maths

Some cool code to distract you

```
FIXED_S(15, 8) l2s_sum = 0;
FIXED_U(17, 2) l2Squared = l2s(vect, 0, x);
svs_index_loop: for (int i=1; i<SVS_DIM_2; i++)
{
    FIXED_U(12, 12) K_root_3 = cordic_exp(l2Squared);
```

```

12s_sum += alpha3(vert, i-1, K_root_3);
12Squared = 12s(vert, i, x);
}

FIXED_U(12, 12) K_root_3 = cordic_exp(12Squared);
12s_sum += alpha3(vert, SVS_DIM_2-1, K_root_3);
return 12s_sum;

```

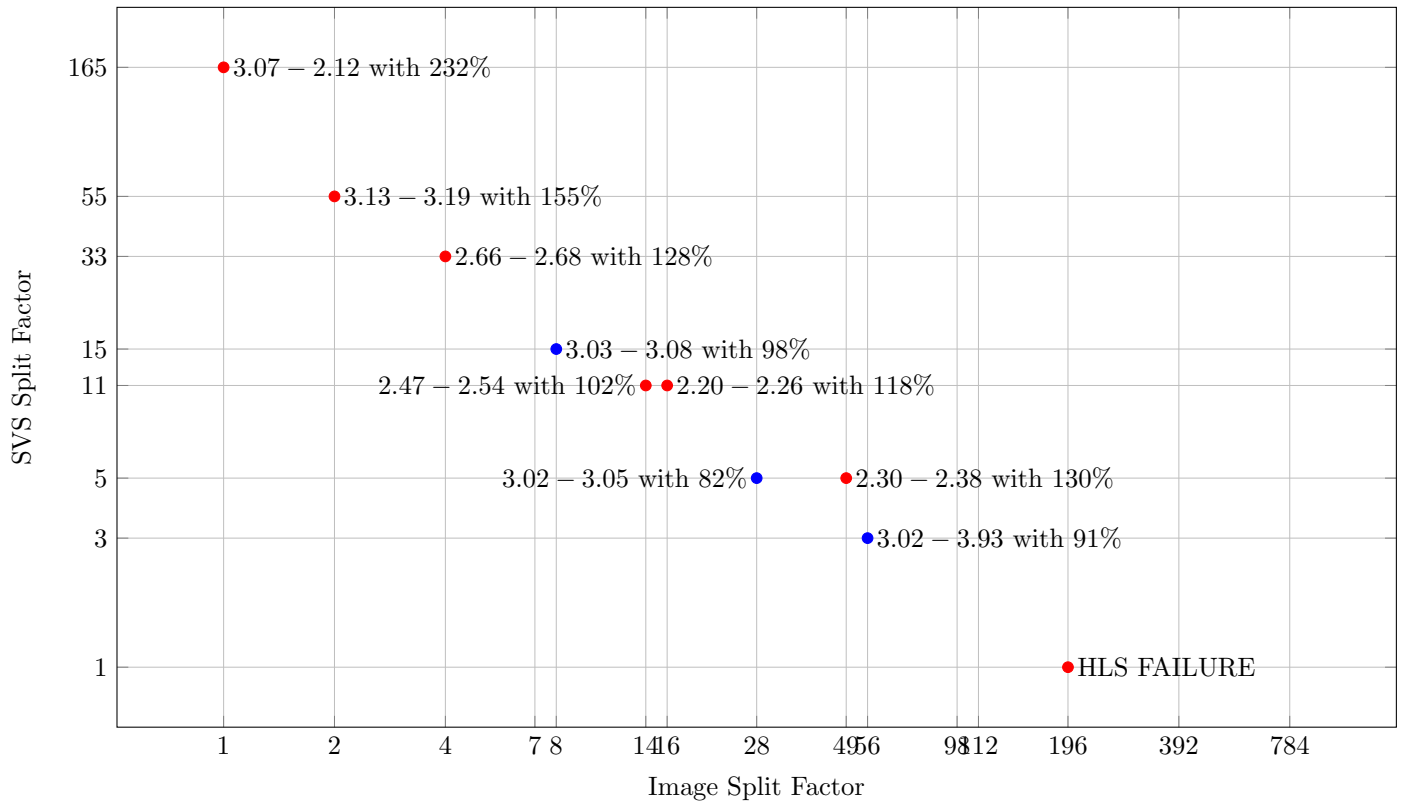


Figure 3: The Space of potential splittings, each with the total estimated latency (over 2601 images, in millions) with the LUT utilisation

Observation: Thing get bigger when other thing be smoller

Explanation: Its always just a trade off between having what you want, and having what you need.



Figure 4: The final design diagram showing parallelism.

Some other ramblings about fpgas.

References

- [1] X. Hu, R.G. Harber, and S.C. Bass. “Expanding the range of convergence of the CORDIC algorithm”. In: *IEEE Transactions on Computers* 40.1 (1991), pp. 13–21. DOI: 10.1109/12.67316.
- [2] *Vivado Design Suite User Guide*. URL: https://www.amd.com/content/dam/xilinx/support/documents/sw_manuals/xilinx2020_2/ug902-vivado-high-level-synthesis.pdf (visited on 02/28/2024).

Name	BRAM	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	167	-
FIFO	-	-	-	-	-
Instance	115	150	9576	29477	-
Memory	0	-	4480	1120	0
Multiplexer	-	-	-	13274	-
Register	-	-	189	-	-
Total	115	150	14245	44038	0
Available	280	220	106400	53200	0
Utilization (%)	41	68	13	82	0

Figure 5: Resource Utilisation