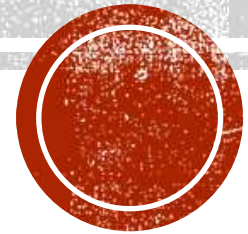
EEE3209:DIGITAL ELECTRONICS II

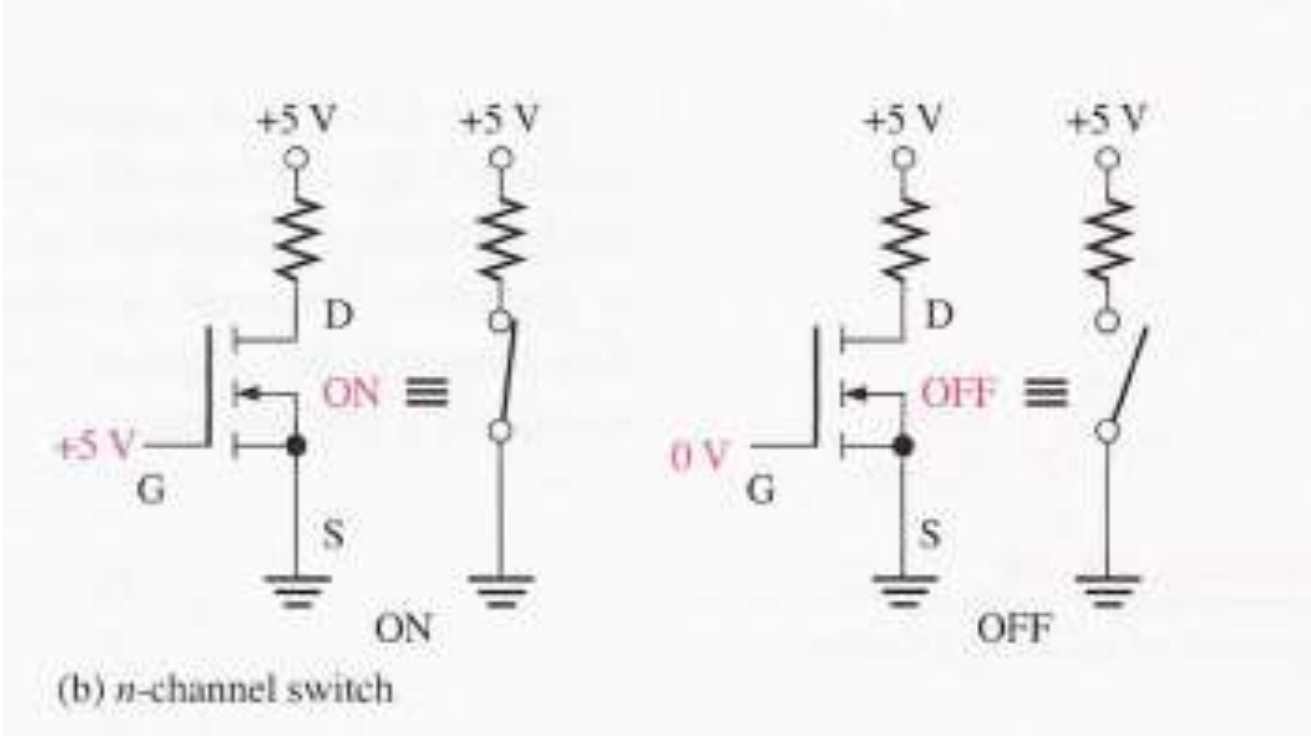
MOS AND ECL TECHNOLOGY



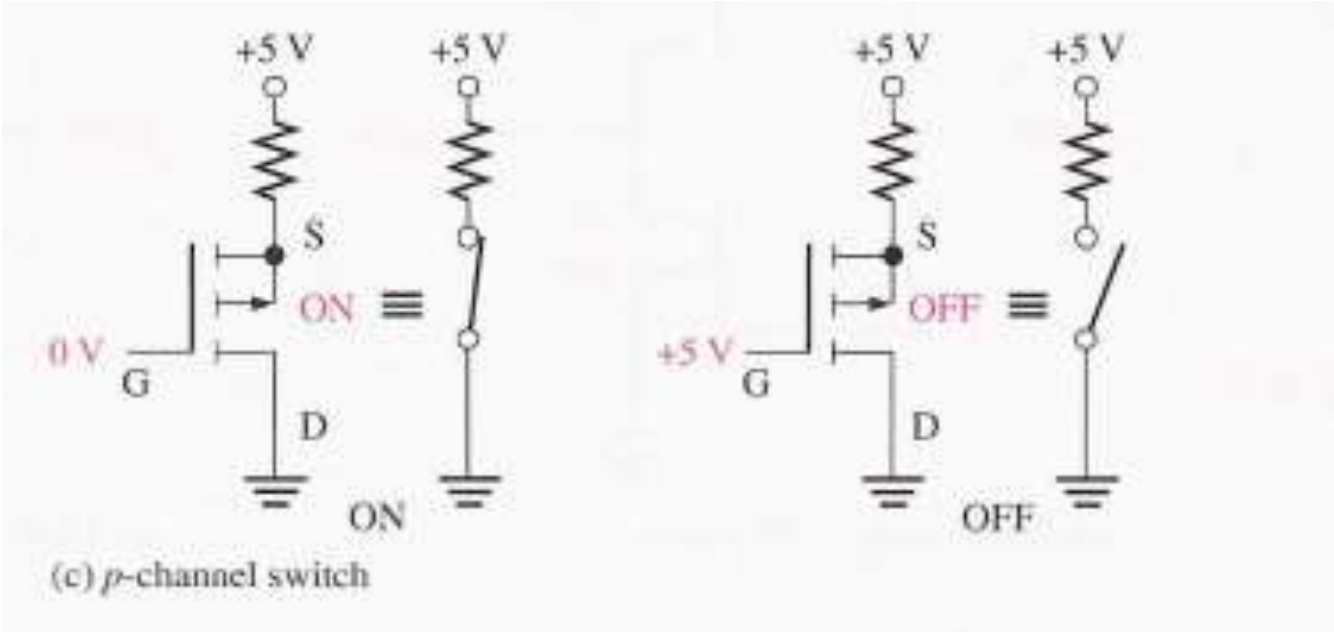
INTRODUCTION

- The most basic element in the design of a large scale integrated circuit is the transistor. Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is the widely used transistor on the market.
- CMOS technology today is the dominant semiconductor technology used for making microprocessors, memory devices and application-specific integrated circuits (ASICs).
- The CMOS logic family, like TTL, has a large number of subfamilies. The basic difference between different CMOS logic subfamilies such as 4000A, 4000B, 4000UB, 74C, 74HC, 74HCT, 74AC and 74ACT is in the fabrication process used and not in the design of the circuits employed to implement the intended logic function.
- These devices differ greatly in construction and internal operation from the BJTs used in TTL circuits, but switching action is basically the same; they function ideally as open or closed switches depending on the input.

- Fig. (b) and (c) show the symbols for both *n-channel* and *p- channel* MOSFETs. The 3 terminals are Gate, Drain and Source.
- When the gate voltage of an n-channel MOSFET is more positive than the source, the MOSFET is on (saturation), and there is ideally a closed switch between the drain and the source.
- When the gate to source is zero, the MOSFET is off (cutoff) and there is ideally an open switch between drain and source.



(b) *n*-channel switch



(c) *p*-channel switch

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR- CMOS

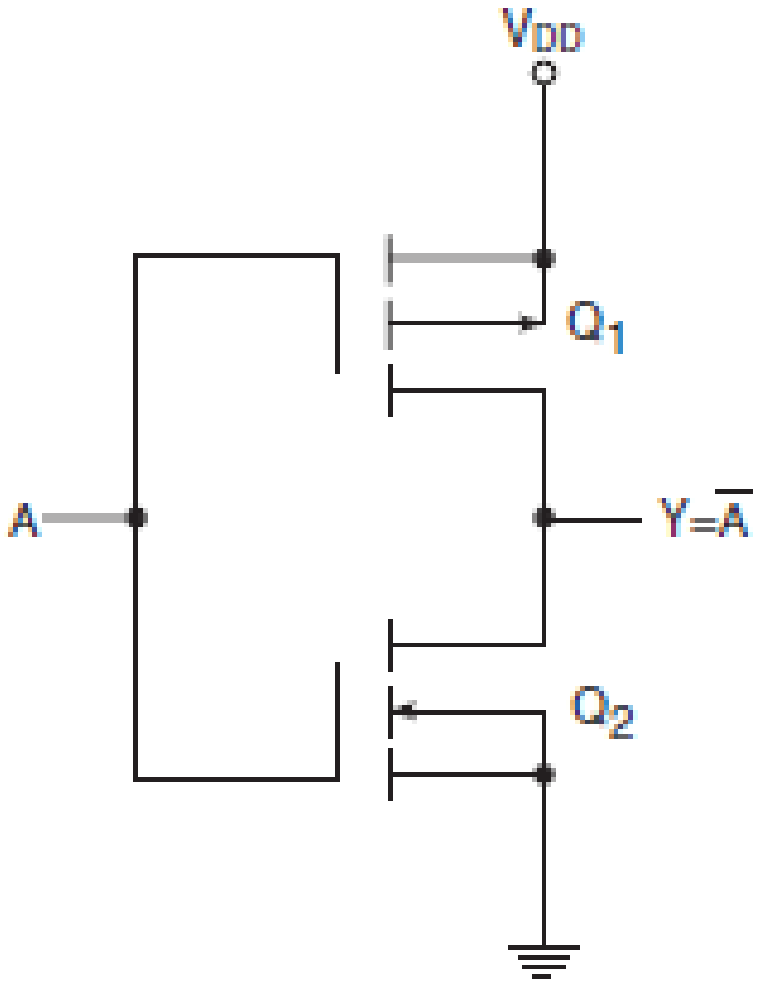
- The CMOS (Complementary Metal Oxide Semiconductor) logic family uses both N-type and P-type MOSFETs (enhancement of MOSFETs, to be more precise) to realize different logic functions.
- The two types of MOSFETs are designed to have matching characteristics i.e, they exhibit identical characteristics in switch-OFF and switch-ON conditions.
- The main advantage of the CMOS logic family over bipolar logic families discussed so far lies in its extremely low power dissipation, which is near-zero in static conditions.
- In fact, CMOS devices draw power only when they are switching.
- This allows integration of a much larger number of CMOS gates on a chip than would have been impossible with bipolar or NMOS (to be discussed later) technology.

CMOS INVERTER

- The inverter is the most fundamental building block of CMOS logic. It consists of a pair of N-channel and P-channel MOSFETs connected in cascade configuration.

The circuit functions as follows;

- When the input is in HIGH state (logic '1'), P-channel MOSFET *Q1* is in the cut-off state while the N-channel MOSFET *Q2* is conducting.
- The conducting MOSFET provides a path from ground to output and the output is LOW (logic '0').
- When the input is in LOW state (logic '0'), *Q1* is in conduction while *Q2* is in cut-off.
- The conducting P-channel device provides a path for V_{DD} to appear at the output, so that the output is in HIGH or logic '1' state.



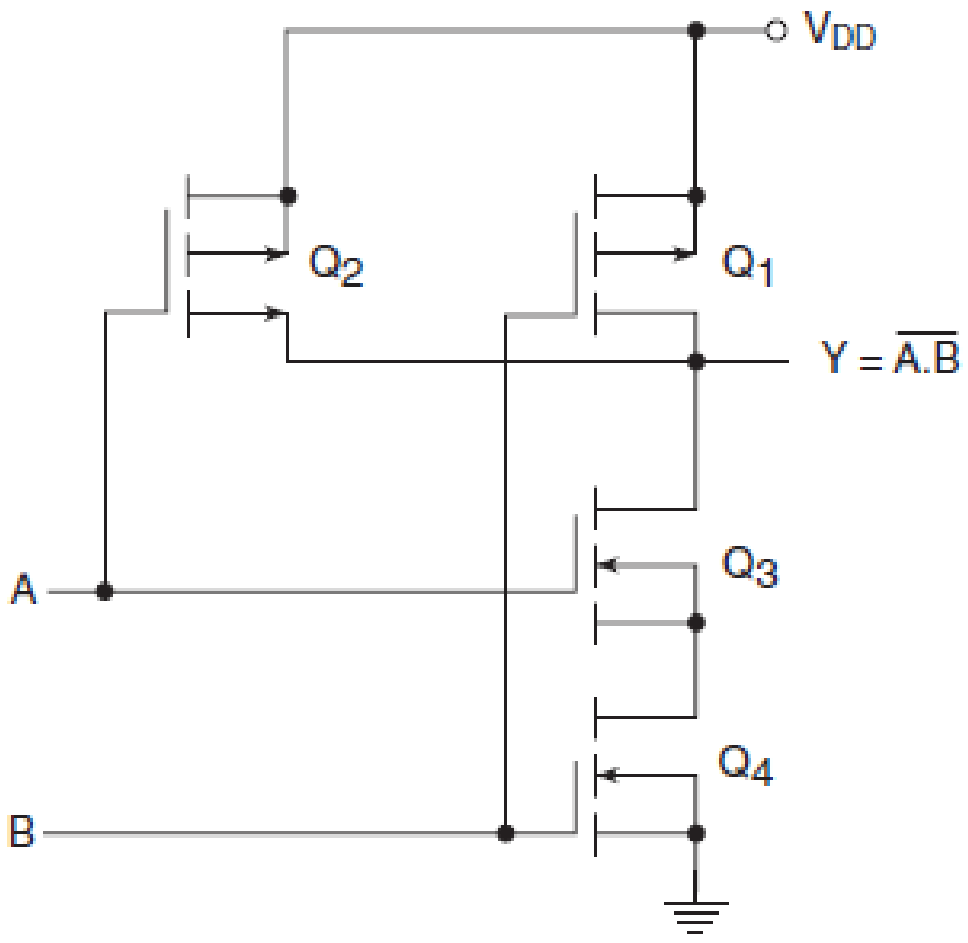
- It is also evident from Fig. that there is no conduction path between VDD and ground in either of the input conditions, that is, when input is in logic ‘1’ and ‘0’ states.
- That is why there is practically zero power dissipation in static conditions. There is only dynamic power dissipation, which occurs during switching operations as the MOSFET gate capacitance is charged and discharged.
- The power dissipated is directly proportional to the switching frequency.

CMOS NAND GATE

- The basic circuit implementation of a two-input NAND. Two P-channel MOSFETs (*Q1* and *Q2* are connected in parallel between *VDD* and the output terminal), and two N-channel MOSFETs (*Q3* and *Q4* are connected in series between ground and output terminal).

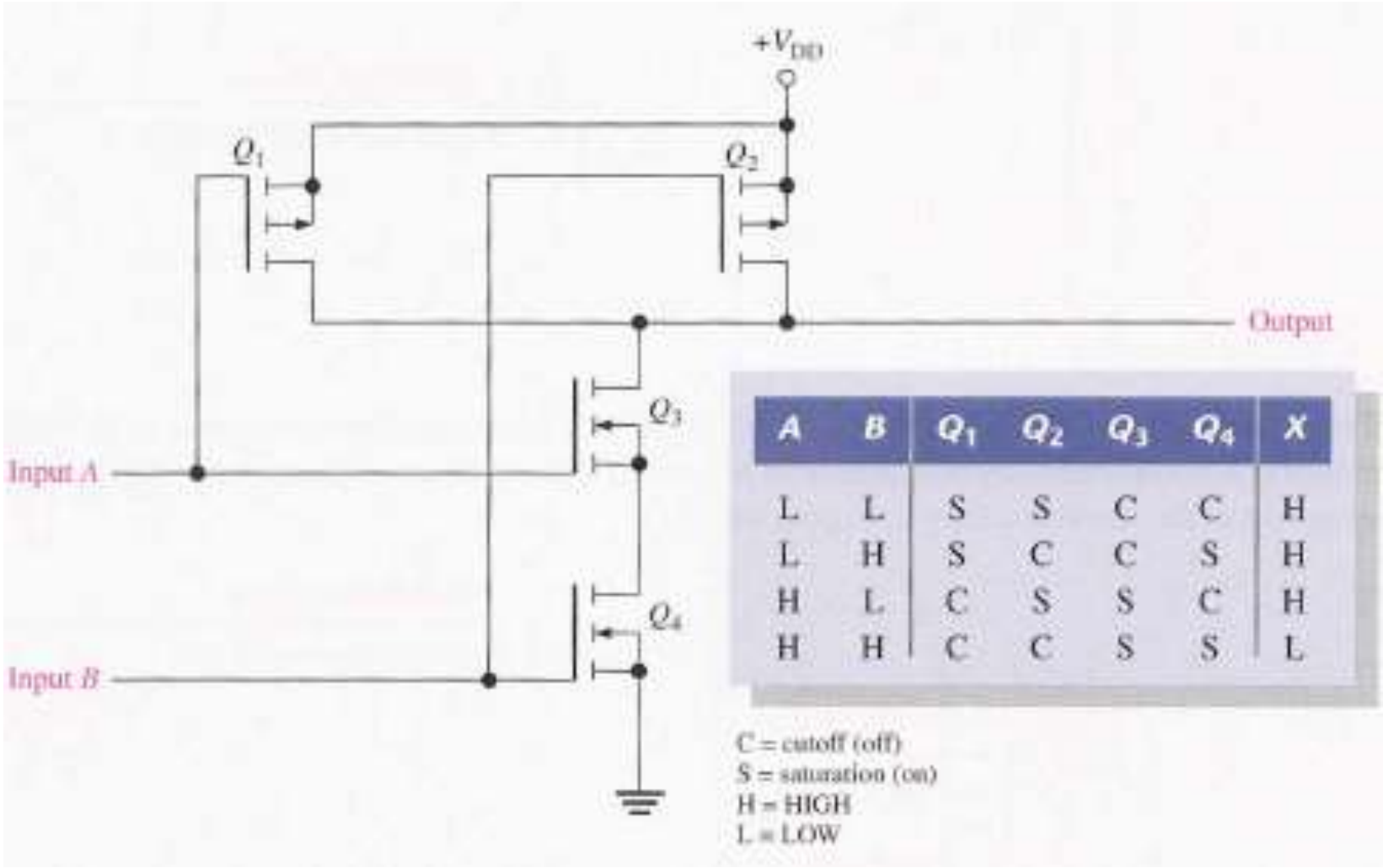
The circuit operates as follows;

- For the output to be in a logic '0' state, it is essential that both the series-connected N-channel devices conduct and both the parallel-connected P-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '1' state.
- This verifies one of the entries of the NAND gate truth table. When both the inputs are in a logic '0' state, both the N-channel devices are nonconducting and both the P-channel devices are conducting, which produces a logic '1' at the output.



OPERATION OF A CMOS NAND GATE

- This verifies another entry of the NAND truth table.
- For the remaining two input combinations, either of the two N-channel devices will be nonconducting and either of the two parallel-connected P-channel devices will be conducting.
- We have either *Q3* OFF and *Q2* ON or *Q4* OFF and *Q1* ON.
- The output in both cases is a logic '1', which verifies the remaining entries of the truth table.



A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	H
H	L	C	S	S	C	H
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

NOR GATE

- The basic circuit implementation of a two-input NOR gate.
- Two P-channel MOSFETs (*Q1* and *Q2* are connected in series between V_{DD} and the output terminal, and two N-channel MOSFETs (Q3 and Q4 are connected in parallel between ground and output terminal).

The circuit operates as follows;

- For the output to be in a logic '1' state, it is essential that both the series-connected P-channel devices conduct and both the parallel-connected N-channel devices remain in the cut-off state.
- This is possible only when both the inputs are in a logic '0' state.
- When both the inputs are in a logic '1' state, both the N-channel devices are conducting and both the P-channel devices are nonconducting, which produces a logic '0' at the output.
- This verifies another entry of the NOR truth table.

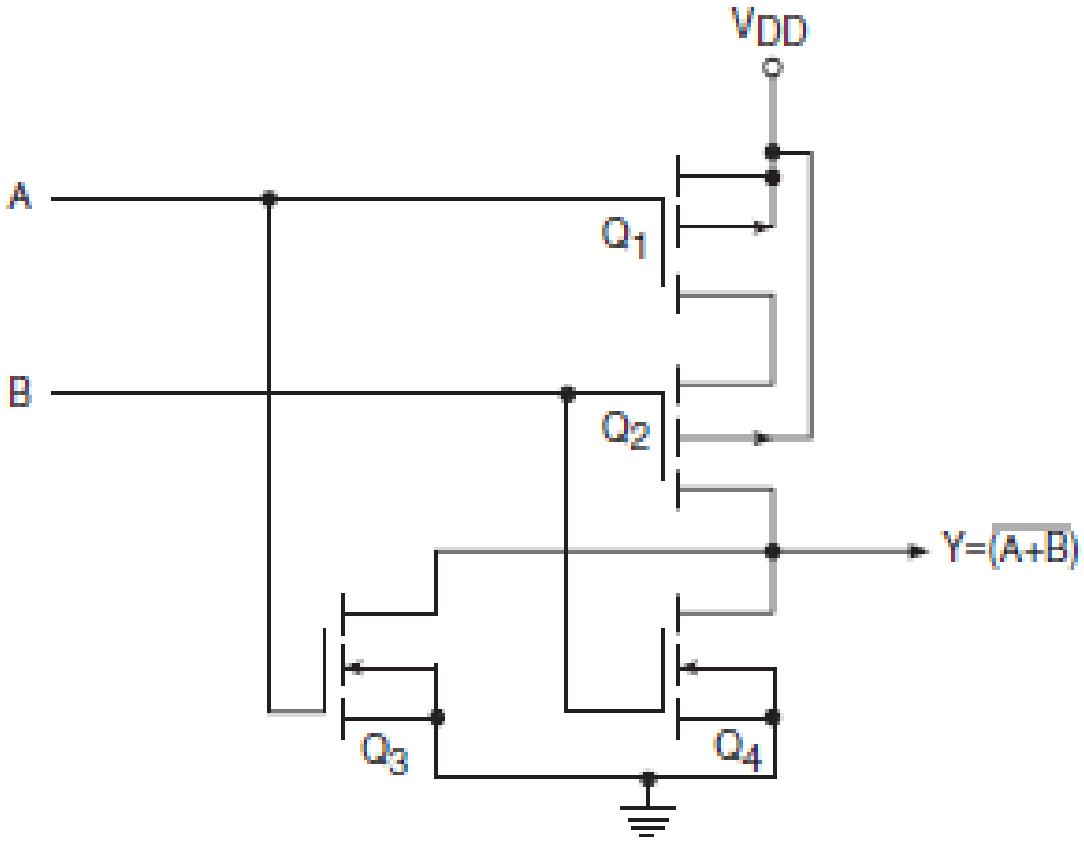


Figure Two-input NOR in CMOS.

- For the remaining two input combinations, either of the two parallel N-channel devices will be conducting and either of the two series-connected P-channel devices will be nonconducting.
- We have either *Q1* OFF and *Q3* ON or *Q2* OFF and *Q4* ON.
- The output in both cases is logic '0', which verifies the remaining entries of the truth table.

Truth table

A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	L
H	L	C	S	S	C	L
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

AND Gate

- An AND gate is nothing but a NAND gate followed by an inverter.
- A buffered AND gate is fabricated by using a NOR gate schematic with inverters at both of its inputs and its output feeding two series-connected inverters.

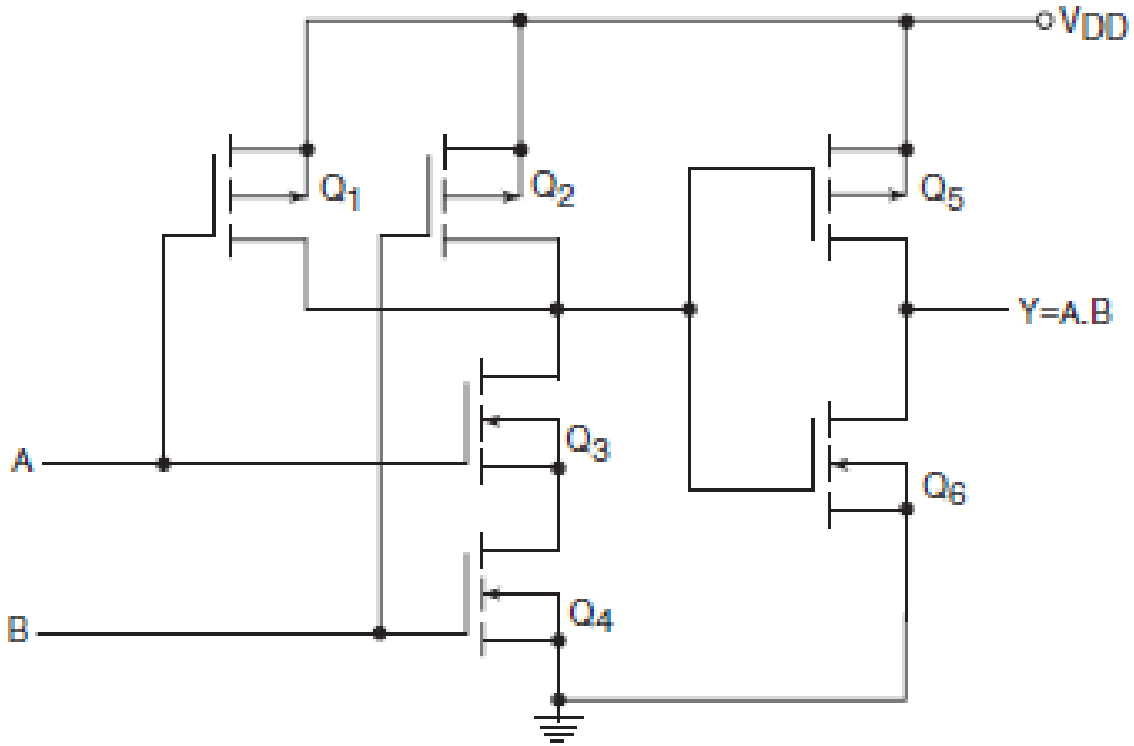


Figure a Two-input AND in CMOS.

OR Gate

- An OR gate is nothing but a NOR gate followed by an inverter.
- A buffered OR gate is fabricated by using a NAND gate schematic with inverters at both of its inputs and its output feeding two series-connected inverters.

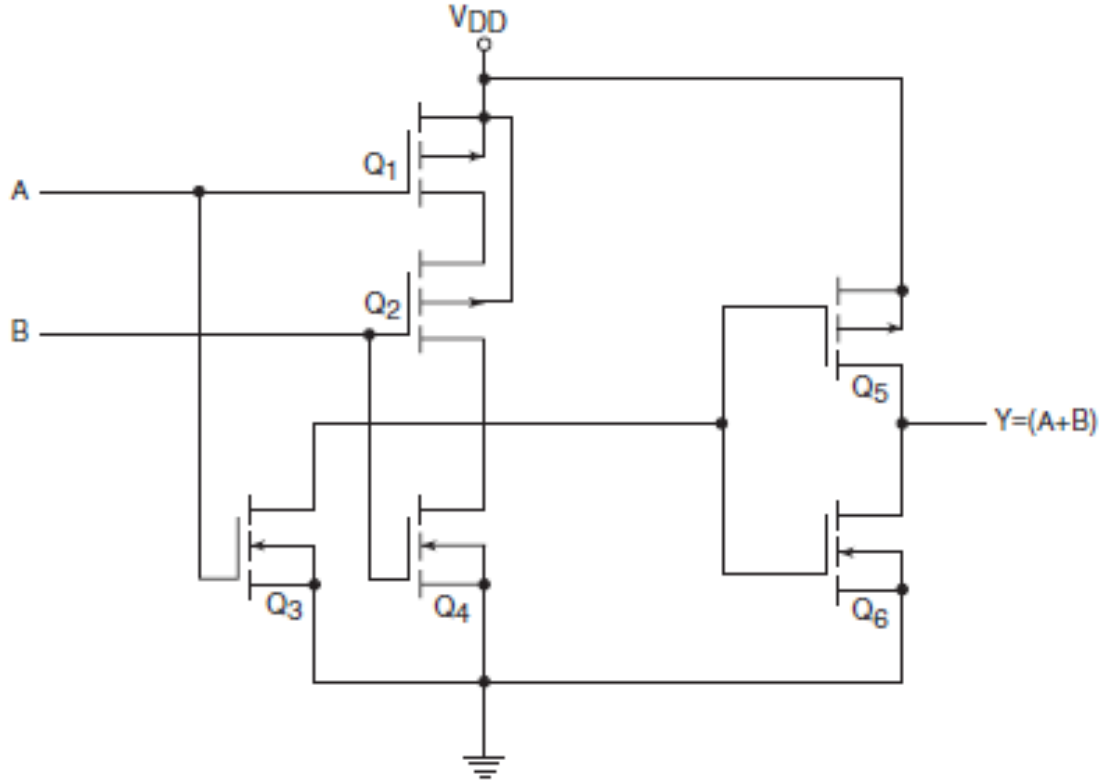


Figure b Two-input OR in CMOS.

EXERCISE

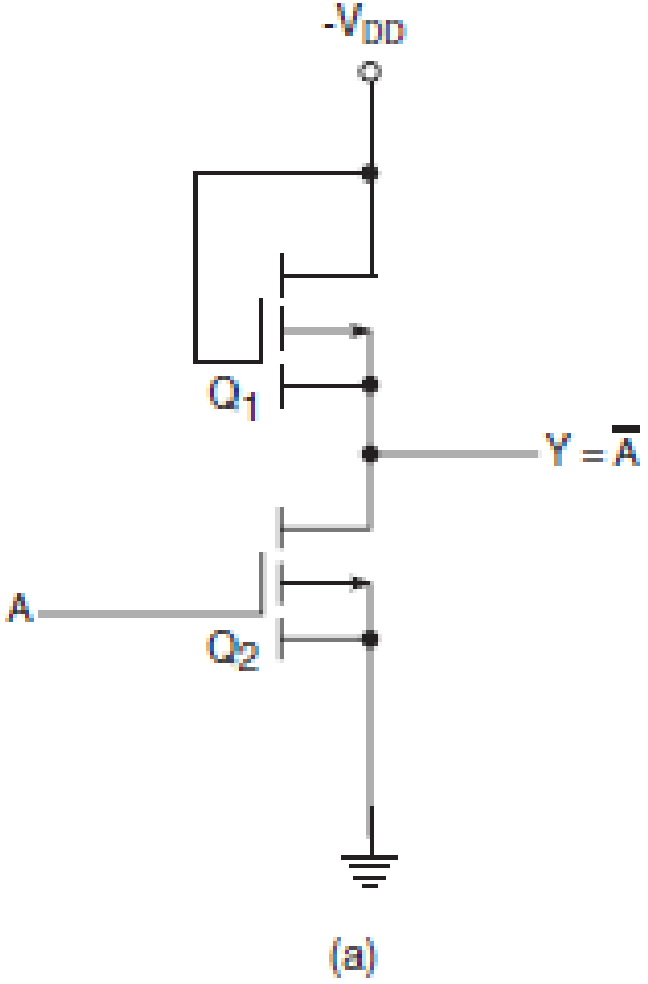
- Discuss the operation of Open-drain gates and give an illustration.
- Discuss the precautions followed when handling CMOS devices.
- Briefly explain a Tristate –Cmos gate. Draw an internal logic of a tristate Cmos inverter circuitry.

- Logic families discussed so far are the ones that are commonly used for implementing discrete logic functions such as logic gates, flip-flops, counters, multiplexers, demultiplexers, etc., in relatively less complex digital ICs belonging to the small-scale integration (SSI) and medium-scale integration (MSI) level of inner circuit complexities.
- The TTL, the CMOS and the ECL logic families are not suitable for implementing digital ICs that have a large-scale integration (LSI) level of inner circuit complexity and above.
- The competitors for LSI-class digital ICs are the PMOS, the NMOS and the integrated injection logic (I2L).

PMOS LOGIC

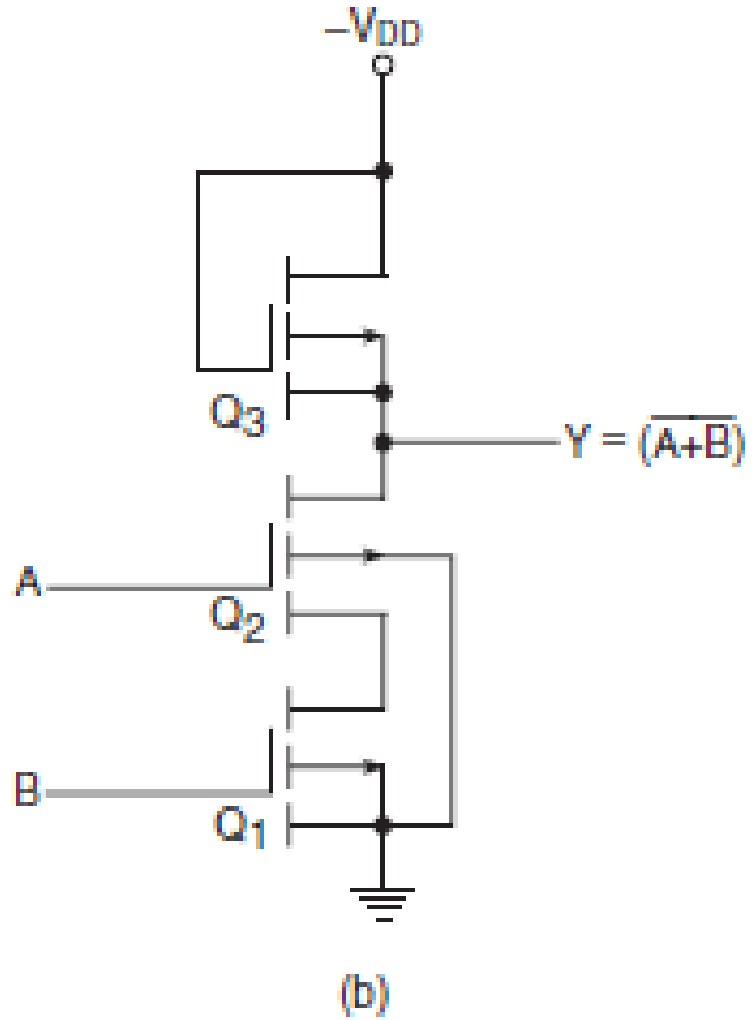
- The PMOS logic family uses P-channel MOSFETS.
- Fig(a) shows an inverter circuit using PMOS logic.
- MOSFET *Q1* acts as an active load for the MOSFET switch *Q2*.
- *Gnd* and $-V_{DD}$ respectively represent a logic '1' and a logic '0' for a positive logic system.
- When the input is grounded (i.e. logic '1'), *Q2* remains in cut-off and $-V_{DD}$ appears at the output through the conducting *Q1*.
- When the input is at $-V_{DD}$ or near $-V_{DD}$, *Q2* conducts and the output goes to near-zero potential (i.e. logic '1').

Inverter Circuit



- Figure (b) shows a PMOS logic based two-input NOR gate.
- In the logic arrangement, the output goes to logic '1' state (i.e. ground potential) only when both Q1 and Q2 are conducting.
- This is possible only when both the inputs are in logic '0' state.
- For all other possible input combinations, the output is in logic '0' state, because, with either Q1 or Q2 nonconducting, the output is nearly $-V_{DD}$ through the conducting Q3.

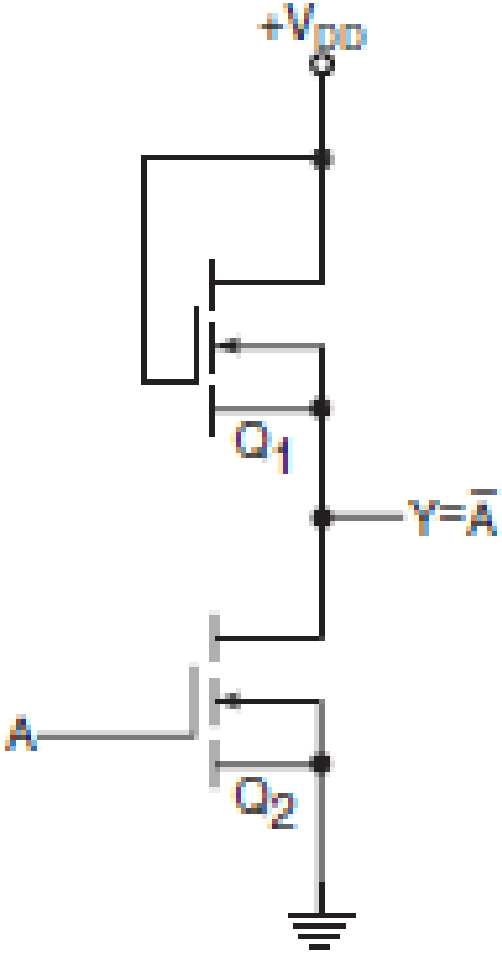
Two-input NOR gate



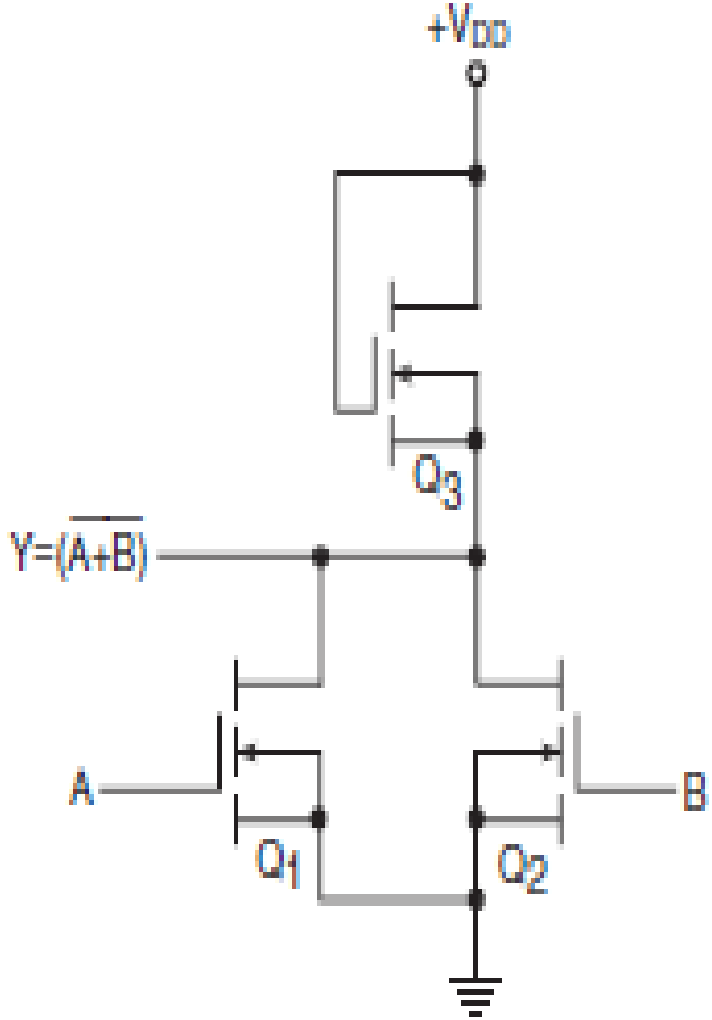
(b)

NMOS LOGIC

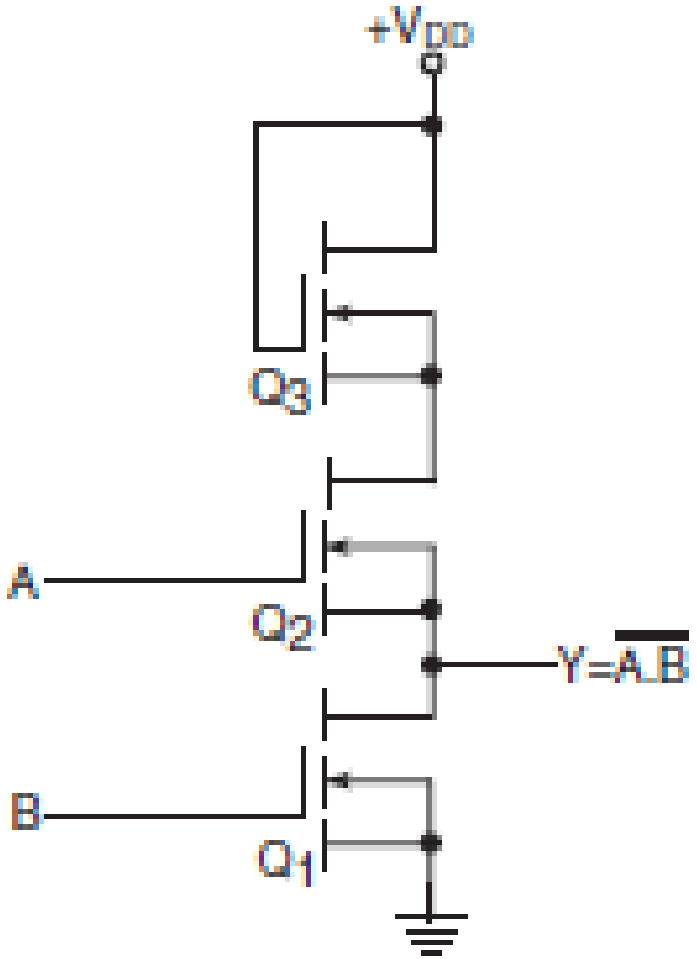
- The NMOS logic family uses N-channel MOSFETS. N-channel MOS devices require a smaller chip area per transistor compared with P-channel devices, with the result that NMOS logic offers a higher density.
- Also, owing to the greater mobility of the charge carriers in N-channel devices, the NMOS logic family offers higher speed too.
- It is for this reason that most of the MOS memory devices and microprocessors employ NMOS logic or some variation of it such as VMOS, DMOS and HMOS.
- VMOS, DMOS and HMOS are only structural variations of NMOS, aimed at further reducing the propagation delay.
- Figures (a), (b) and (c) respectively show an inverter, a two-input NOR and a two-input NAND using NMOS logic. The logic circuits are self-explanatory.



(a)



(b)



(c)

EXERCISE

1. What is the main feature of NMOS and PMOS technology in integrated circuits?
2. Come up with a comparison of CMOS and TTL logic devices in terms of performance characteristics

EMITTER COUPLED LOGIC-ECL

- The first monolithic emitter coupled logic family was introduced by ON Semiconductor, formerly a division of Motorola, with the MECL-I series of devices in 1962, with the MECL-II series following it up in 1966. Both these logic families have become obsolete.
- Currently, popular subfamilies of ECL logic include MECL-III (also called the MC 1600 series), the MECL-10K series, the MECL-10H series and the MECL-10E series (ECLinPS and ECLinPSLite). The MECL-10K series further divided into the 10 100-series and 10 200-series devices.
- With a propagation delay of the order of 1 ns and a flip-flop toggle frequency of 500 MHz, MECL-III is used in high-performance, high-speed systems.

- Emitter- coupled logic, like TTL is bipolar technology. The typical ECL circuit consists of a different amplifier input circuit, a bias circuit, and emitter follower outputs.
- ECL is much faster than TTL because the transistors do not operate in saturation and is used in more specialized high-speed applications.

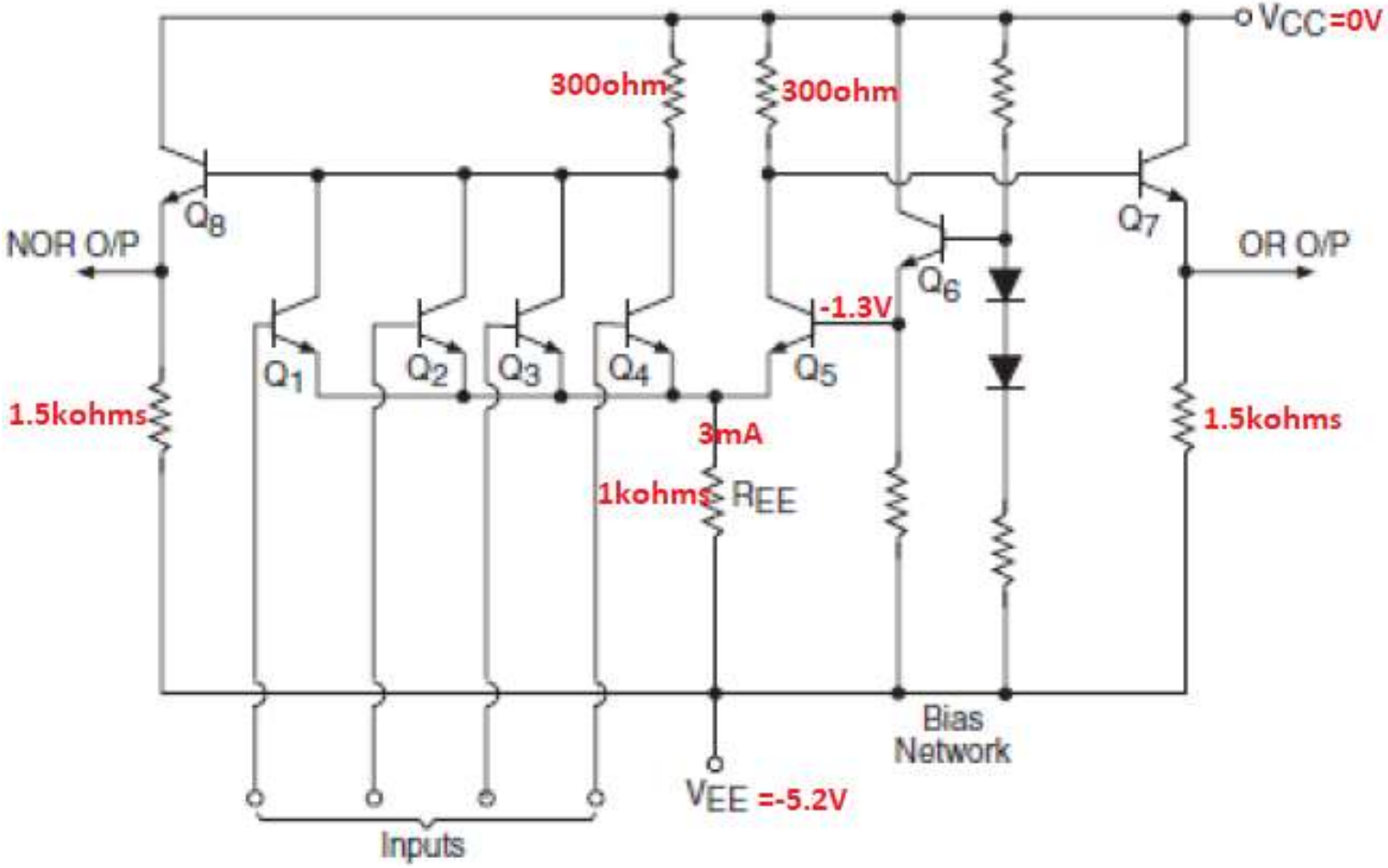
MECL-III Series

The basic characteristic parameters of MECL-III are as follows:

- Gate propagation delay=1 ns;
- Output edge speed (indicative of the rise and fall time of output transition)=1 ns;
- Flip-flop toggle frequency=500 MHz;
- Power dissipation per gate=50 mW;
- Speed–power product=60 pJ;
- Input voltage=0–VEE (VEE is the negative supply voltage);
- Negative power supply range (for VCC=0)=−5.1V to −5.3 V;
- Continuous output source current (max.)=40 mA; s
- Urge output source current (max.) = 80 mA;
- Operating temperature range=−30 °C to +85 °C.

LOGIC GATE IMPLEMENTATION IN ECL

- OR/NOR is the fundamental logic gate of the ECL family. A typical internal schematic of an OR/NOR gate in the 10K-series MECL family is shown.
- The circuit in essence comprises a differential amplifier input circuit with one side of the differential pair having multiple transistors depending upon the number of inputs to the gate, a voltage- and temperature-compensated bias network and emitter follower outputs.
- The internal schematic of the 10H-series gate is similar, except that the bias network is replaced with a voltage regulator circuit and the source resistor *REE* of the differential amplifier is replaced with a constant current source.



OR/NOR in ECL

- Typical values of power supply voltages are V_{CC} = 0 and V_{EE}=−5.2 V. The nominal logic levels are logic LOW=logic '0'=−1.75 V and logic HIGH = logic '1'=−0.9 V, assuming a positive logic system.

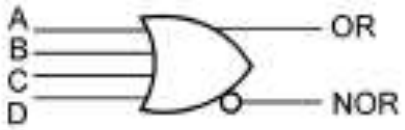
The circuit functions as follows;

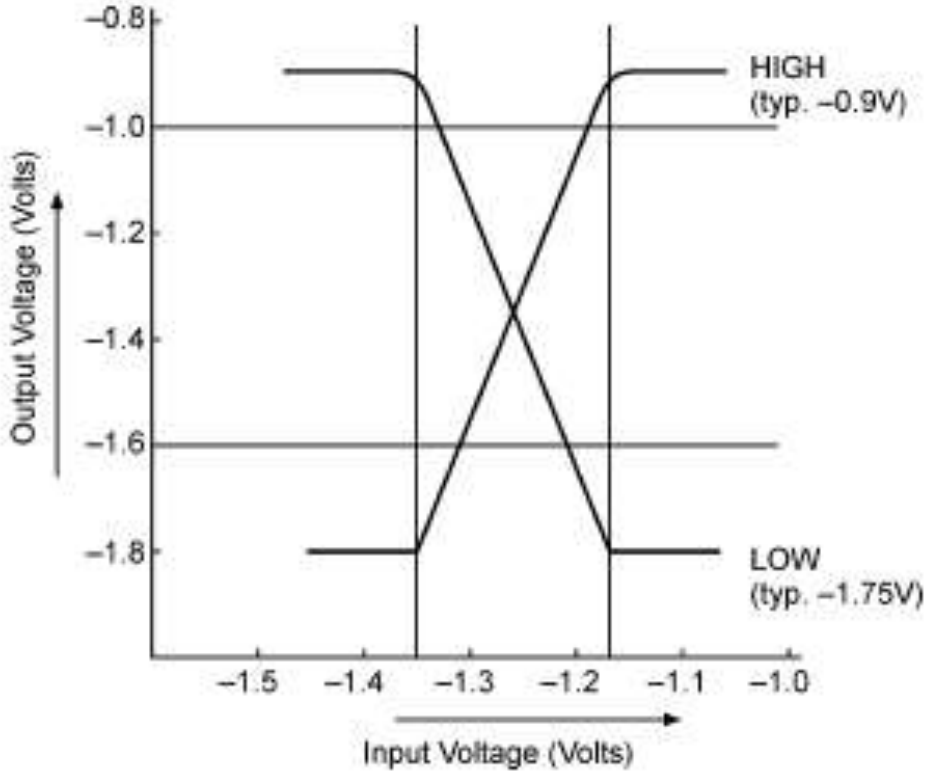
- The bias network configured around transistor *Q6* produces a voltage of typically −1.29V at its emitter terminal.
- This leads to a voltage of −2.09V at the junction of all emitter terminals of various transistors in the differential amplifier, assuming 0.8V to be the required forward-biased P–N junction voltage.
- Now, let us assume that all inputs are in a logic '0' state, that is, the voltage at the base terminals of various input transistors is −1.75 V.
- This means that the transistors *Q1, Q2, Q3 and Q4* will remain in cut-off as their base-emitter junctions are not forward biased by the required voltage.
- This leads us to say that transistor *Q7* is conducting, producing a logic '0' output, and transistor *Q8* is in cut-off, producing a logic '1' output.

- In the next step, let us see what happens if any one or all of the inputs are driven to logic '1' status, that is, a nominal voltage of −0.9V is applied to the inputs.
- The base-emitter voltage differential of transistors *Q1–Q4* exceeds the required forward-biasing threshold, with the result that these transistors start conducting.
- This leads to a rise in voltage at the common-emitter terminal, which now becomes approximately −1.7V as the common-emitter terminal is now 0.8V more negative than the base terminal voltage.
- With rise in the common-emitter terminal voltage, the base-emitter differential voltage of *Q5* becomes 0.31 V, driving *Q5* to cut-off.
- The *Q7* and *Q8* emitter terminals respectively go to logic '1' and logic '0'.

ECL input/output characteristics

- Note that the differential action of the switching transistors (where one section is ON while the other is OFF) leads to simultaneous availability of complementary signals at the output.
- The circuit symbol and switching characteristics of this basic ECL gate are shown in the Fig.
- It may be mentioned here that positive ECL (called PECL) devices operating at +5V and ground are also available.
- When used in PECL mode, ECL devices must have their input/output *DC* parameters adjusted for proper operation.
- PECL *DC* parameters can be computed by adding ECL levels to the new *VCC*.





- Because of the low output impedance of the emitter-follower and the high input impedance of the differential amplifier input, high fan-out operation is possible.
- In this type of circuit, saturation is not possible.
- The lack of saturation results in higher power consumption and limited voltage swing (less than 1V) but it permits high-frequency switching.

- **NOISE MARGIN**: Noise margin of a gate is the measure of its immunity to undesired voltage fluctuations (noise).
- Typical ECL circuits have noise margins from about 0.2V - 0.25V.
- These are less than that for TTL and make ECL less suitable in high noise environments.

COMPARISON OF ECL WITH TTL AND CMOS

	BIPOLAR (TTL) F	CMOS AHC	BIPOLAR (ECL)
Speed			
Gate propagation delay, t_p (ns)	3.3	3.7	0.22–1
FF maximum clock freq. (MHz)	145	170	330–2800
Power Dissipation Per Gate			
Bipolar: 50% dc	8.9 mW		25 mW–73 mW
CMOS: quiescent		2.5 μW	

MAJOR FEATURES OF ECL

1. ECL family devices produce the true and complementary output of the intended function simultaneously at the outputs without the use of any external inverters. This in turn reduces package count, reduces power requirements and also minimizes problems arising out of time delays that would be caused by external inverters.
2. The ECL gate structure inherently has high input impedance and low output impedance, which is very conducive to achieving large fan-out and drive capability.
3. ECL devices with open emitter outputs allow them to have transmission line drive capability. The outputs match any line impedance. Also, the absence of any pull-down resistors saves power.
4. ECL devices produce a near-constant current drain on the power supply, which simplifies power supply design.
5. On account of the differential amplifier design, ECL devices offer a wide performance flexibility, which allows ECL circuits to be used both as linear and as digital circuits.
6. Termination of unused inputs is easy. Resistors of approximately 50k allow unused inputs to remain unconnected.