24 Week 35
August
Wednesday

August

Week	32	33	34	35	36
Monday	1	8	15	22	29
Tuesday	2	9	16	23	30
Wednesday	3	10	17	24	31
Thursday	4	11	18	25	
Friday	5	12	19	26	
Saturday	6	13	20	27	
Sunday	7	14	21	28	

8 AM

9 AM INSTITUTION: DEDAN KIMATHI UNIVERSITY

10 AM NAME: OLIVER KIPKEMEI

11 AM REG NO: E022-01-0278/2018

12 PM TASK CAT 3

1 PM SUBMISSION: 3rd September 2020

2 PM LECTURER: VASANT

3 PM UNIT: DIGITAL ELECTRONICS

4 PM

5 PM

6 PM

Evening

10 August Wednesday

Sunday 7 14 20 21 27 28

8 AM

State DeMorgen's Theorem

9 AM

States that the sum of two

10 AM complement variables is equal

to the product of the two

11 AM complement variables

12 PM $\bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$

1 PM prove with truth table

2 PM

3 PM

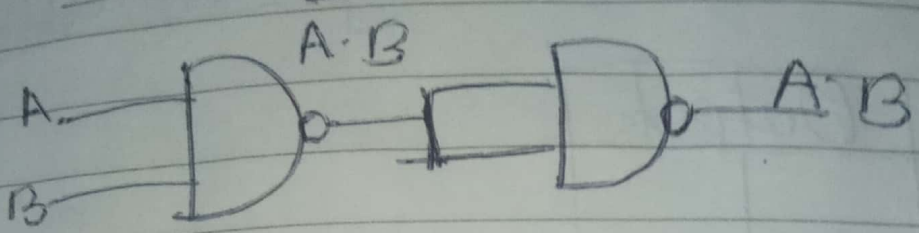
4 PM

5 PM

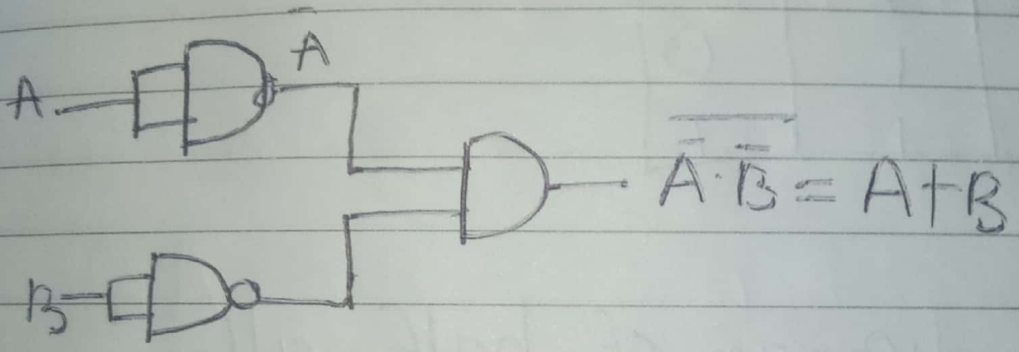
6 PM

Evening

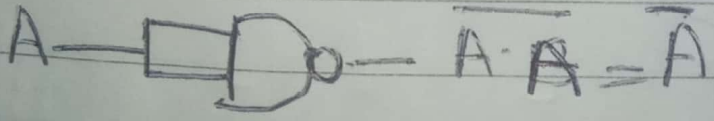
NAND as AND



NAND as OR



NAND as NOT



Evening

12 Week 33
August
Friday

Sunday 7 14 21 28

8 AM

Truth table of binary half adder

9 AM

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

10 AM

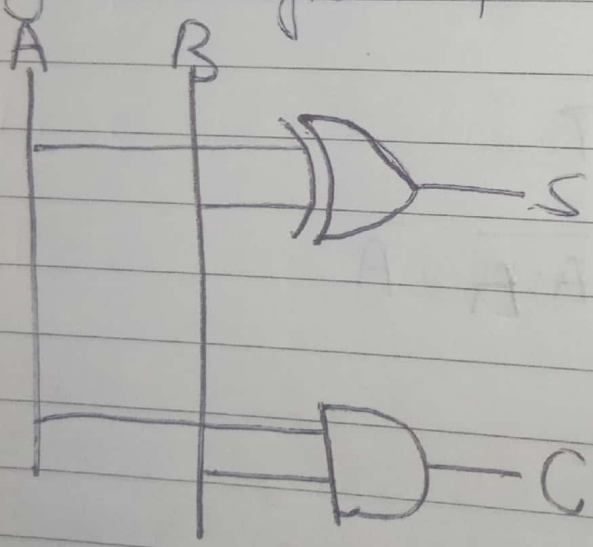
11 AM

12 PM

1 PM

2 PM

Logic diagram of half adder



3 PM

4 PM

5 PM

6 PM

Evening

8 AM

Convert 12 to Binary, BCD & excess 3

(i) To binary

~~12~~ $\frac{12}{2} = 6$ 0

$\frac{6}{2}$ 3 0 1100

11 AM

$\frac{3}{2}$ 1 1

12 PM

$\frac{1}{2}$ 0 1

1 PM

(ii) Excess 3

2 PM

12 = 1100 1111

+ 0011

1111

(iii) BCD

15 Week 34
August
Monday

8 AM

Prove

9 AM

$A \cdot \bar{B} + B \cdot \bar{C} + C \cdot \bar{A} = \bar{A} \cdot B + \bar{B} \cdot C + \bar{C} \cdot A$

10 AM

soln

11 AM

$A \cdot \bar{B} \cdot (C + \bar{C}) + (A + \bar{A}) B \cdot \bar{C} + \bar{A} (B + \bar{B}) \cdot C$

12 PM

$A \cdot \bar{B} \cdot C + A \cdot \bar{B} \cdot \bar{C} + A \cdot B \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + \bar{A} \cdot B \cdot C + \bar{A} \cdot \bar{B} \cdot C$

1 PM

$= A \cdot \bar{B} \cdot C + \bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C}$

2 PM

$+ \bar{A} \cdot B \cdot C$

3 PM

$= \bar{B} \cdot C (A + \bar{A}) + A \cdot \bar{C} (\bar{B} + B) + \bar{A} \cdot B (\bar{C} + C)$

4 PM

$= \bar{B} \cdot C + A \cdot \bar{C} + \bar{A} \cdot B = LHS$

5 PM

Explain operation of 'J-K' & T & D flip flop

6 PM

Evening

JK flip flop

The flipflop has two inputs J & K, the input corresponding to S(set) input & K input corresponding to R (rest) input

when JK = 11, the output will be complemat to each other, but this will not give

The inputs JK were 10 & flip was in set mode & Q was equal to 1. , changing the input RS becomes 10 which will reset the latch. That's the content of the latch is complemtnt.e the output Q $\bar{Q}$ change 01 to 10. But Did a

D flip-flop

Has only one input in addition to clock pulse

The R & S input of RS flipflop

Evening

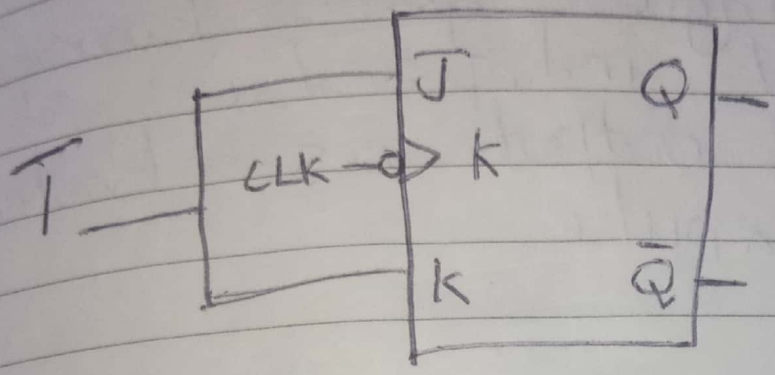
are not used in some applications when both the inputs are 00 or 11. This condition also eliminate the condition of RS = 11. So in D flip-flop RS input are always kept complemat of each other and D input is applied to S input and complemat of S is applied to R input

T flip flop

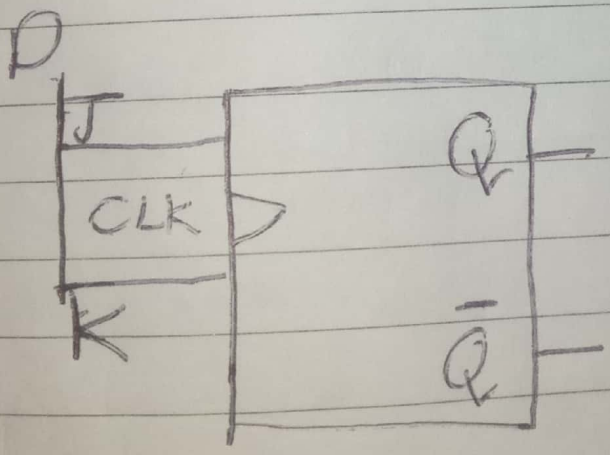
comes when JK inputs at an edge trigger flip flop are connat together to form single input

has only two options. When T = 0 the flip flop will be in store mode & gives no change in input. when T = 1, the flip flop will be in complemad mode i.e it toggle or give complemate output of previous value at trailing edge of clock pls.

T flip flop logic diagram



D flip flop



Evening

19 Week 34
August
Friday

Thursday 4 11 18 25
Friday 5 12 19 26
Saturday 6 13 20 27
Sunday 7 14 21 28

8 AM

9 AM Combinational circuit, are the network of logic gates having a

10 AM set of input independent Variable and outputs as a Boolea

11 AM function of inputs

12 PM

1 PM

2 PM

3 PM

4 PM

5 PM

6 PM

Evening

Shift register register used to manipulate data for computational purpose by shifting the data in a register in either the left or right direction

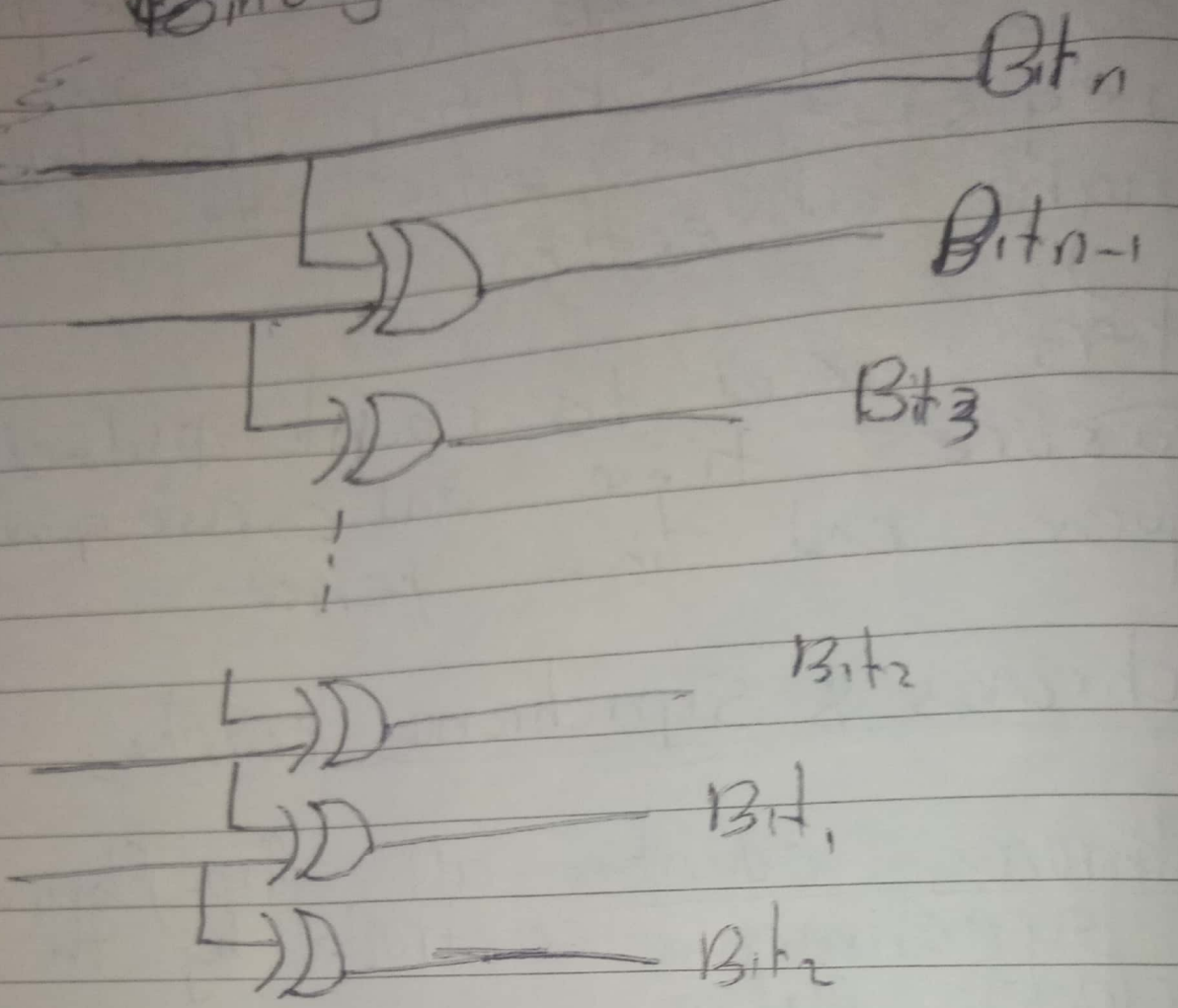
Counters used to count pulses measure time and consequently frequency and time period

Asynchronous & Synchronous counters

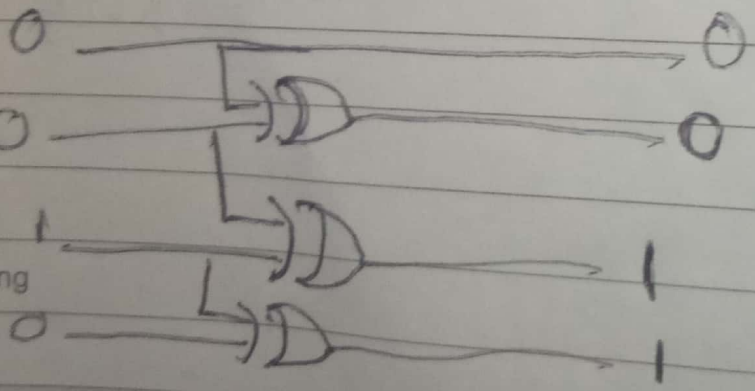
Asynchronous counters all flip-flops are not synchronous controlled by the same clock pulse

Synchronous counters all flip flop are synchronous controlled by same clock pulse

Binary to g



2 = 0010

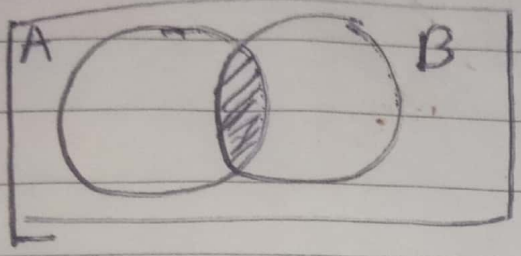


= 0011

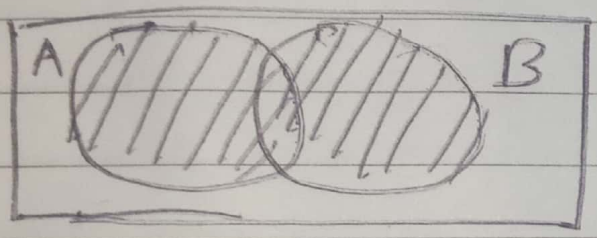
Evening

Venn Diagram

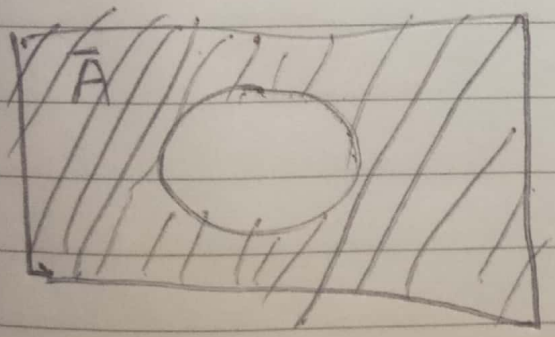
AND



OR



NOT



Evening