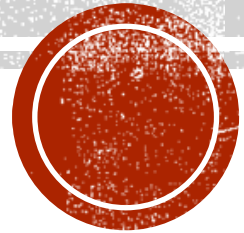
EEE3209:DIGITAL ELECTRONICS II

BIPOLAR TTL FAMILY



GATES WITH OPEN COLLECTOR/DRAIN OUTPUTS

- The TTL gates described in the previous sections all had the totem-pole output circuit.
- Open Collector/Drain output gates connect an external resistor, called the pull-up resistor, between the output and the DC power supply to make the logic gate perform the intended logic function.
- Depending on the logic family used to construct the logic gate, they are referred to as gates with open collector output (in the case of the TTL logic family) or open drain output (in the case of the MOS logic family).

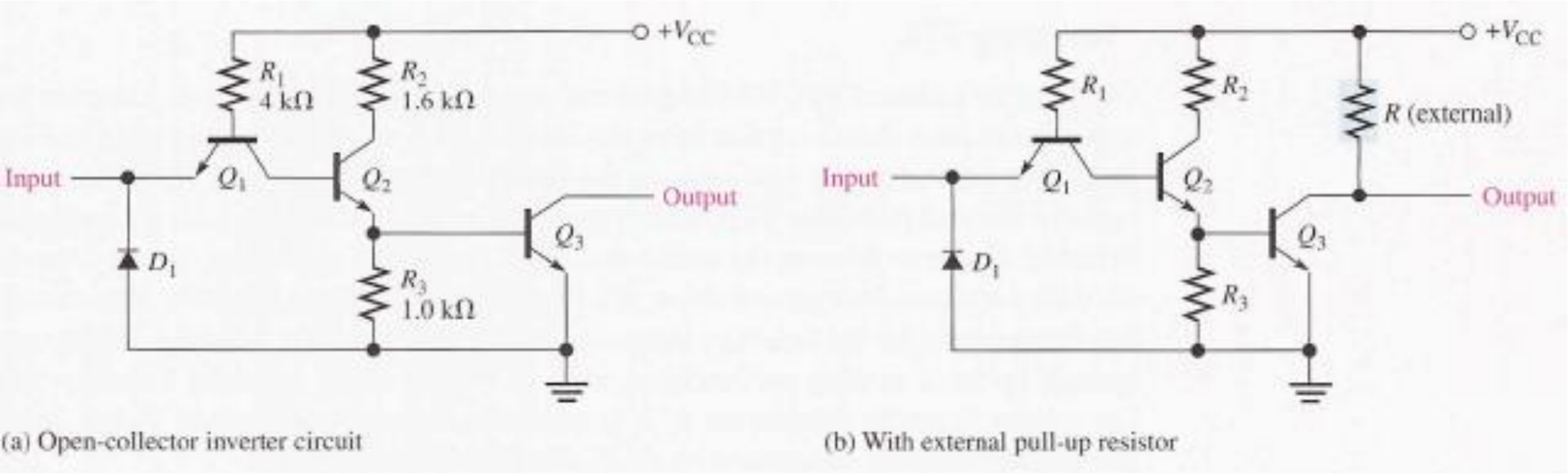
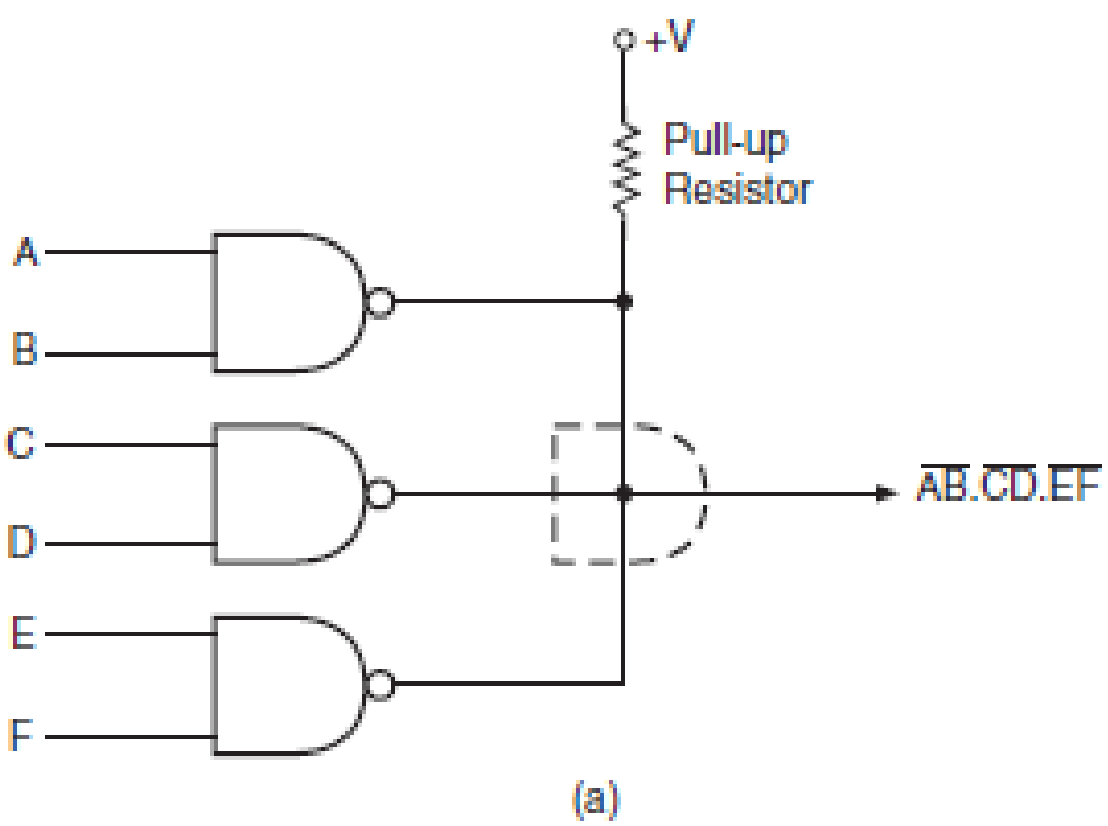

+V_{CC}
R_1
4 kΩ
R_2
1.6 kΩ
Input
Q_1
Q_2
Output
Q_3
D_1
R_3
1.0 kΩ
(a) Open-collector inverter circuit
+V_{CC}
R_1
R_2
R (external)
Input
Q_1
Q_2
Output
Q_3
D_1
R_3
(b) With external pull-up resistor

Figure 10

- A standard TTL inverter with an open-collector is shown in Fig. 10(a).
- The output is the collector of transistor *Q3* with nothing connected to it, hence the name *open collector*.
- In order to get the proper HIGH and LOW logic levels out of the circuit, an external pull-up resistor must be connected to *Vcc* from the collector of *Q3* as shown in Fig. 10(b).
- When *Q3* is off, the output is pulled up to *Vcc* through the external resistor.
- When *Q3* is on the output is connected to the near ground through the saturated transistor.

- The advantage of using open collector/open drain gates lies in their capability of providing an ANDing operation when outputs of several gates are tied together through a common pull-up resistor, without having to use an AND gate for the purpose.
- This connection is also referred to as *WIRE-AND connection*.
- Figure 11(a) shows such a connection for open collector NAND gates.
- Figure 11(b) shows a similar arrangement for NOT gates.
- The disadvantage is that they are relatively slower and noisier.
- Open collector/drain devices are therefore not recommended for applications where speed is an important consideration.


+V
Pull-up
Resistor
A
B
C
D
E
F
$\overline{AB}.\overline{CD}.\overline{EF}$
(a)

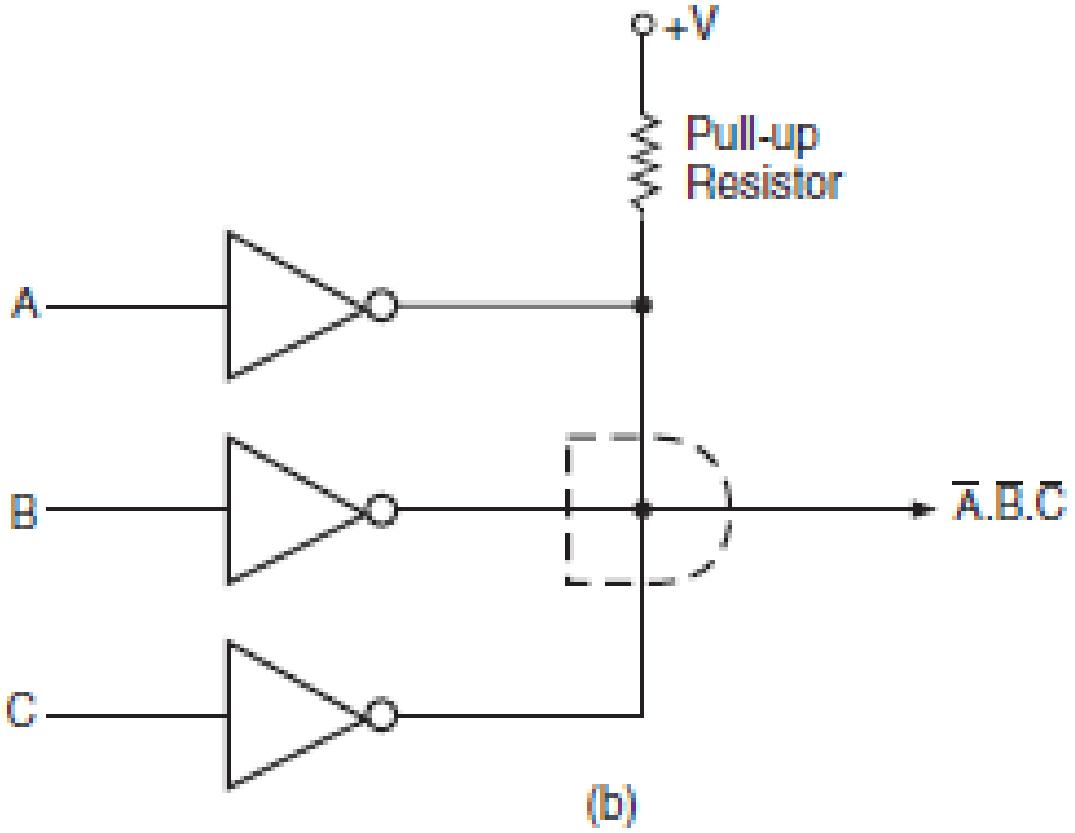
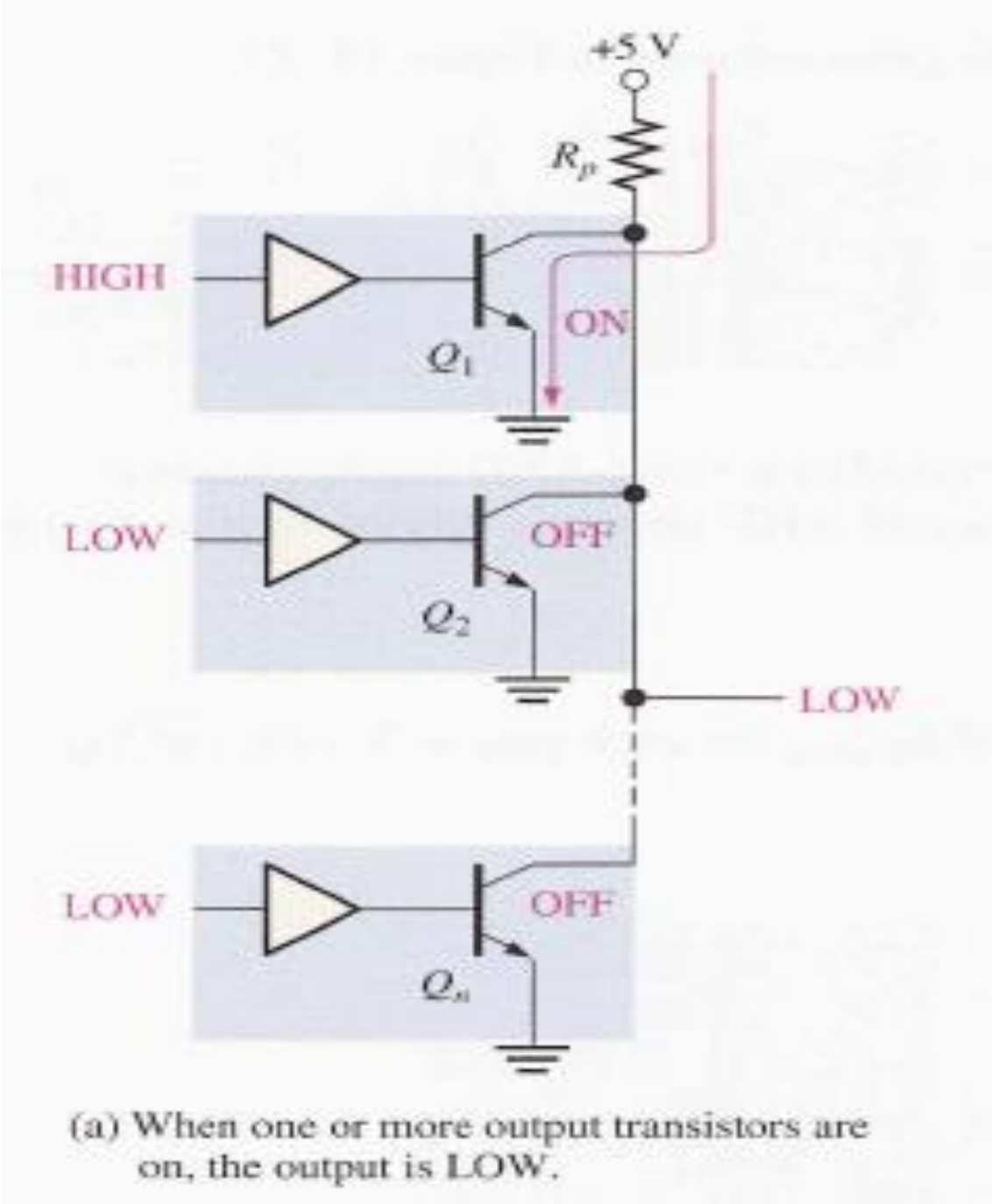

+V
Pull-up
Resistor
A
B
C
$\overline{A}.\overline{B}.\overline{C}$
(b)

Figure 11

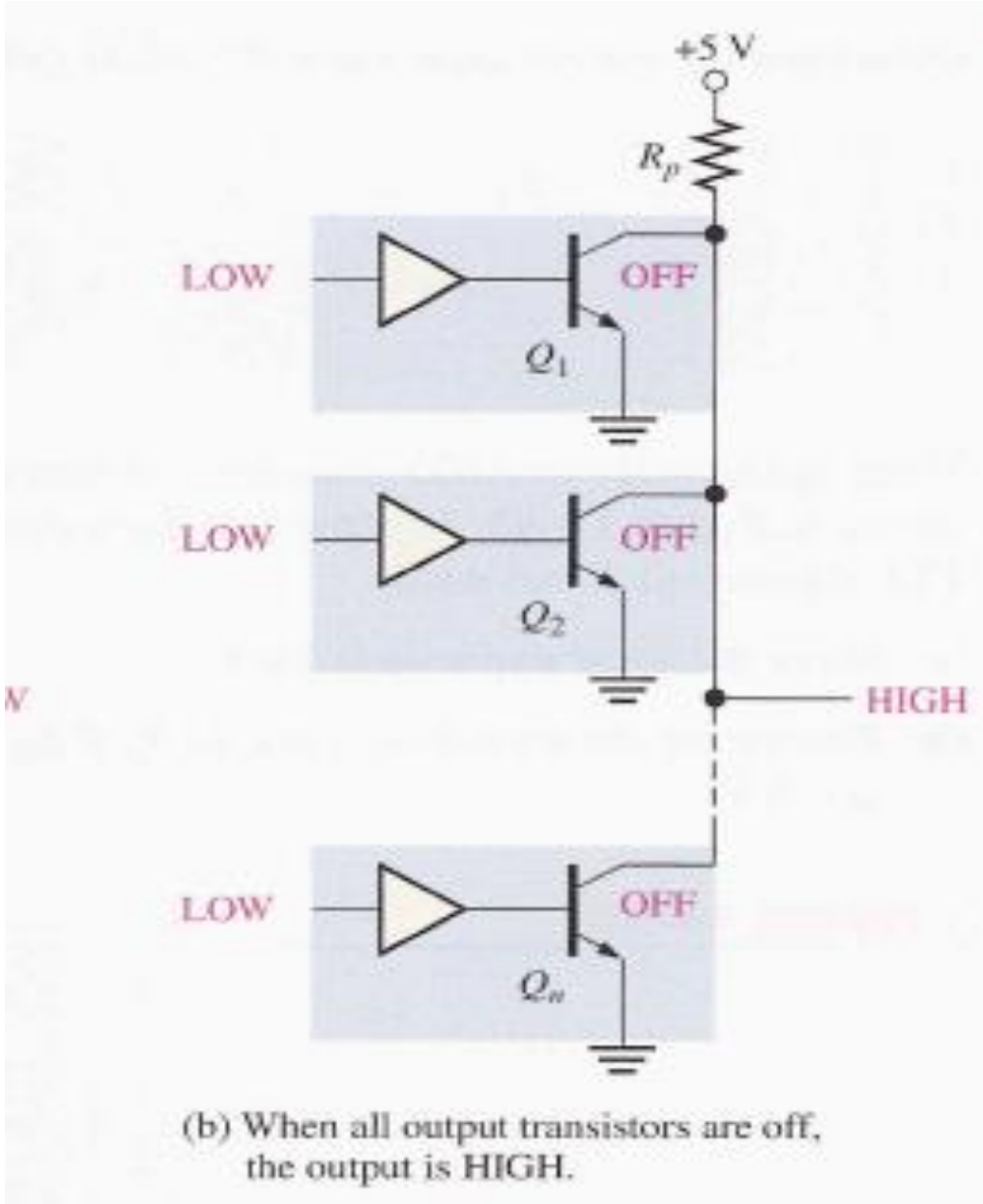


(a) When one or more output transistors are on, the output is LOW.

- When one or more of the inverter inputs is HIGH, the output *X* is pulled because an output transistor is on and acts as a closed switch to ground as illustrated.
- In case only one inverter has a HIGH input, but this is sufficient to pull the output LOW through the saturated output transistor *Q1* as indicated.

- For the output *X* to be HIGH, all inverter inputs must be LOW so that all the open-collector output transistors are off as indicated.
- When this condition exists, the output *X* is HIGH only when all the inputs are LOW. Therefore, we have a negative-AND function as expressed in the following equation:

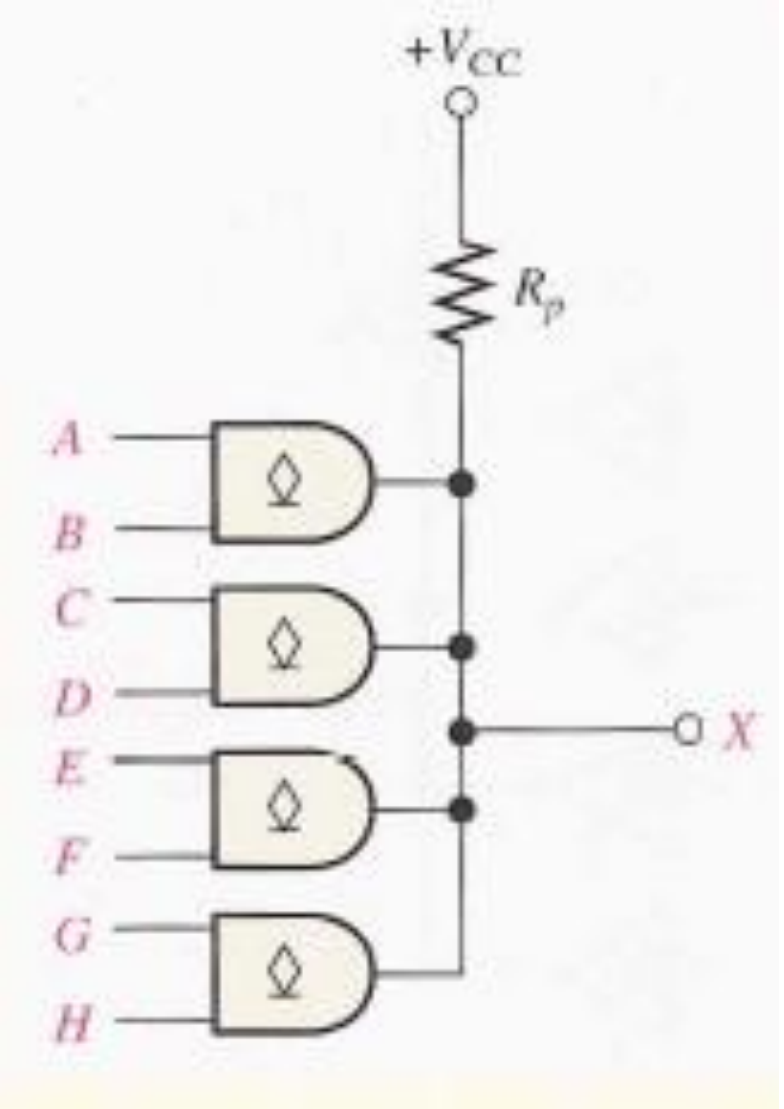
$$X = \overline{A}\,\overline{B}\,\overline{C}$$



(b) When all output transistors are off, the output is HIGH.

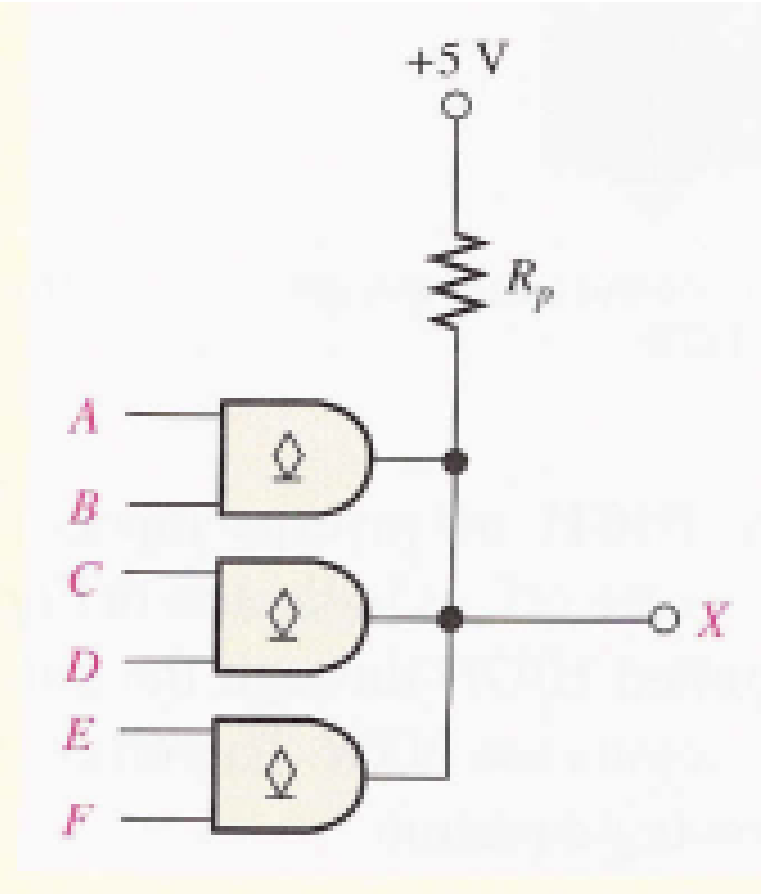
EXERCISE 1

1. Illustrate the difference between a totem pole output arrangement and an open collector output?
2. Write the output expression for the wired-AND configuration of the open-collector AND gates in the following fig.

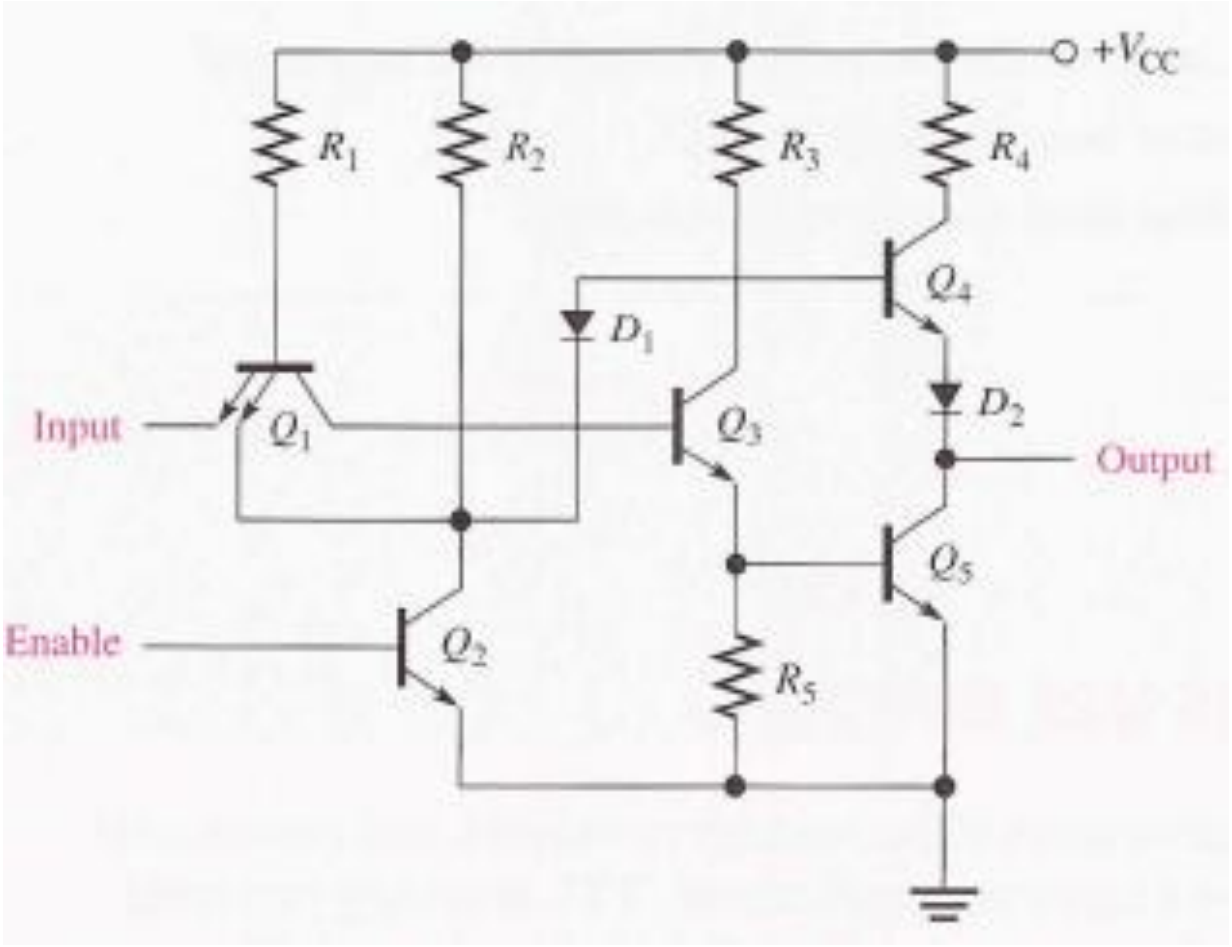


Exercise 2

1. Three open-collector AND gates are connected in a wired-AND configuration as shown. Assume that the wired-AND circuit is driving four standard TTL inputs (-1.6mA each).
   a) Write the logic expression for X
   b) Determine the minimum value of *Rp* if current, $I_{OL(max)}$ for each gate is 30mA and voltage, $V_{OL(max)}$ is 0.4V.



TRISTATE TTL GATES



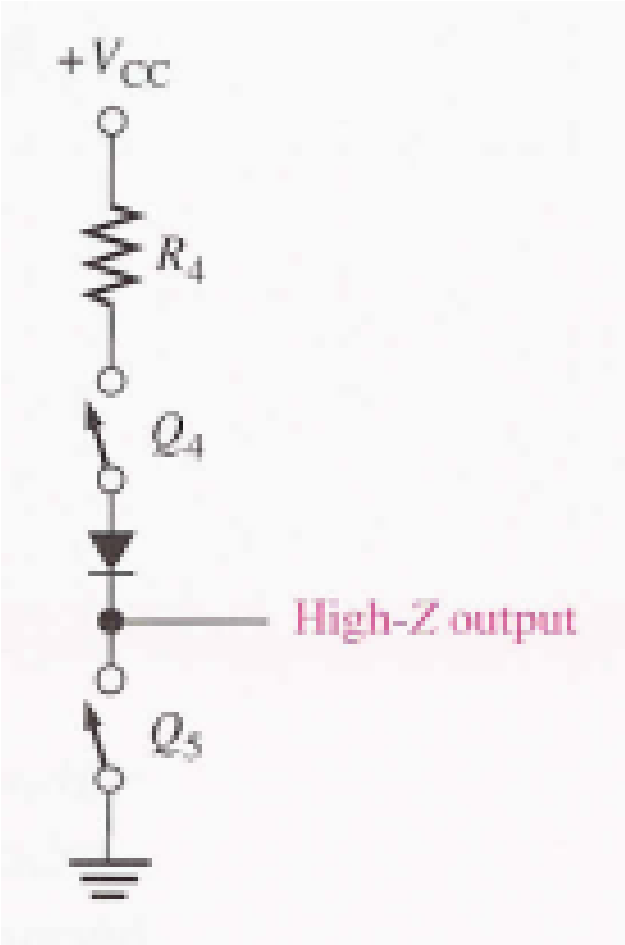
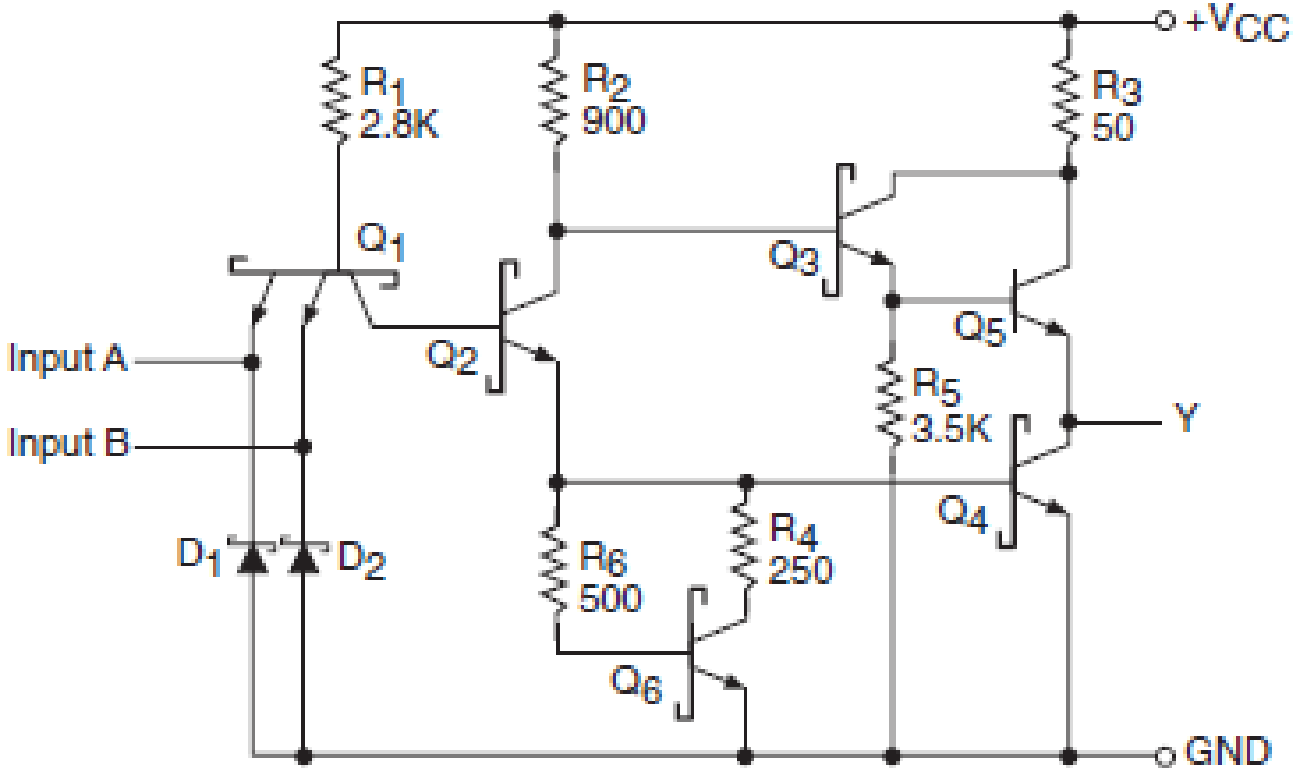


Figure 12

- **Fig. 12** shows the basic circuit for a TTL tristate inverter. Tristate gate has three output states, namely the logic LOW state, the logic HIGH state and the high-impedance state.
- An external **Enable** input decides whether the logic gate works according to its truth table or is in the high-impedance state.
- When the **Enable** input is LOW, *Q2* is off and the output circuit operates as a normal totem-pole configuration in which output state depends on the input state.
- When the **Enable** input is a HIGH, *Q2* is on. There is thus a LOW on the second emitter of *Q1* causing *Q3* and *Q5* to turn off.
- When both totem-pole transistors are off, they are effectively open, and the output is completely disconnected from the internal circuitry.

SCHOTTKY TTL

- The basic TTL NAND gate circuit discussed earlier is modified with a current- sinking type of logic that draws current from the load when in the LOW output state and sources negligible current to the load when the HIGH output state.
- Most TTL logic used today is some form of **Schottky TTL**, which provides faster switching time by incorporating Schottky diodes to prevent the transistor from going into saturation, thereby decreasing the time for a transistor to turn on and off.
- Schottky devices are designated by the symbols *S*



- The transistors used in the circuit are all Schottky transistors with the exception of *Q5*. A Schottky *Q5* would serve no purpose, with *Q4* being a Schottky transistor.
- A Schottky transistor is nothing but a conventional bipolar transistor with a Schottky diode connected between its base and collector terminals.
- The Schottky diode with its metal–semiconductor junction not only is it faster but also offers a lower forward voltage drop of 0.4V as against 0.7V for a P–N junction diode for the same value of forward current.
- The presence of a Schottky diode does not allow the transistor to go to deep saturation.
- The moment the collector voltage of the transistor tends to go below about 0.3 V, the Schottky diode becomes forward biased and bypasses part of the base current through it.
- The collector voltage is thus not allowed to go to the saturation value of 0.1V and gets clamped around 0.3 V.
- While the power consumption of a Schottky TTL gate is almost the same as that of a high-power TTL gate owing to nearly the same values of the resistors used in the circuit, the Schottky TTL offers a higher speed on account of the use of Schottky transistors.

Characteristic features of TTL family

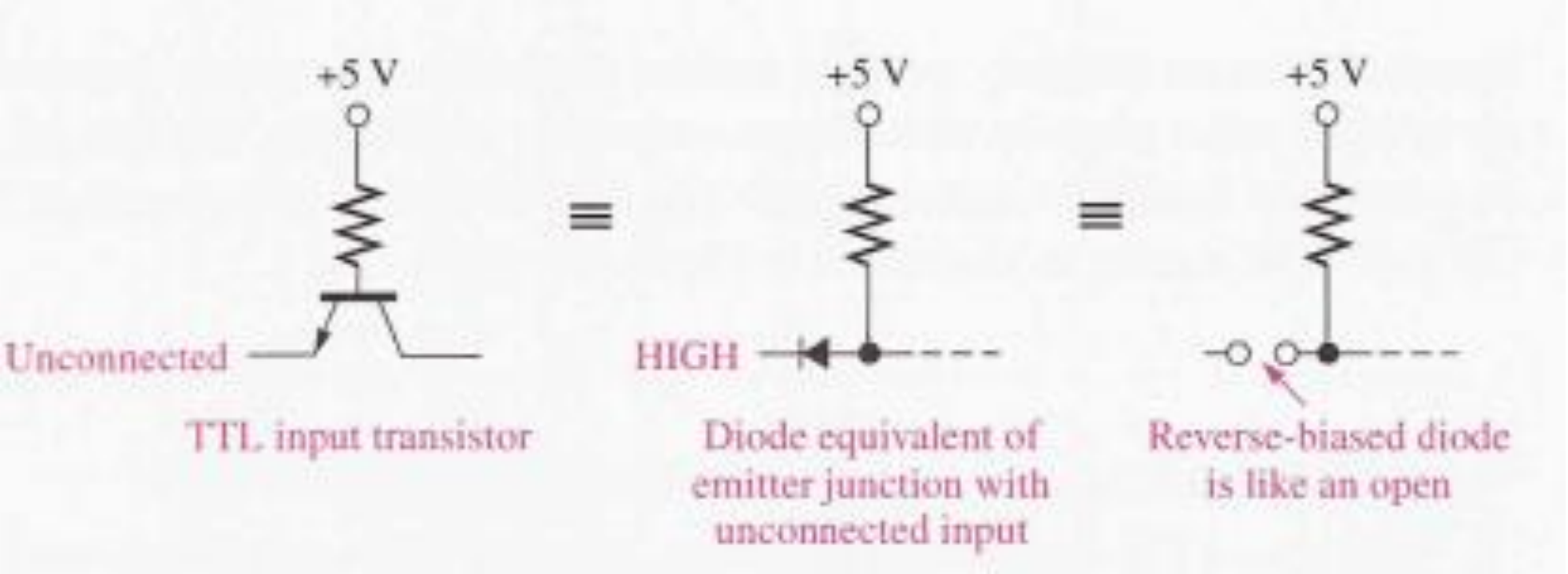
Characteristic features of this family are summarized as follows: $V_{IH} = 2\,V$; $V_{IL} = 0.8\,V$; $I_{IH} = 50\,\mu A$; $I_{IL} = 2\,mA$; $V_{OH} = 2.7\,V$; $V_{OL} = 0.5\,V$; $I_{OH} = 1\,mA$; $I_{OL} = 20\,mA$; $V_{CC} = 4.75–5.25\,V$ (74-series) and 4.5–5.5 V (54-series); propagation delay (for a load resistance of 280 Ω, a load capacitance of 15 pF, $V_{CC} = 5\,V$ and an ambient temperature of 25 °C) = 5 ns (max.) for LOW-to-HIGH and 4.5 ns (max.) for HIGH-to-LOW output transitions; worst-case noise margin = 0.3 V; fan-out = 10; I_{CCH} (for all four gates) = 16 mA; I_{CCL} (for all four gates) = 36 mA; operating temperature range = 0–70 °C (74-series) and −55 to +125 °C (54-series); speed–power product = 57 pJ; maximum flip-flop toggle frequency = 125 MHz.

CHARACTERISTICS OF STANDARD TTL

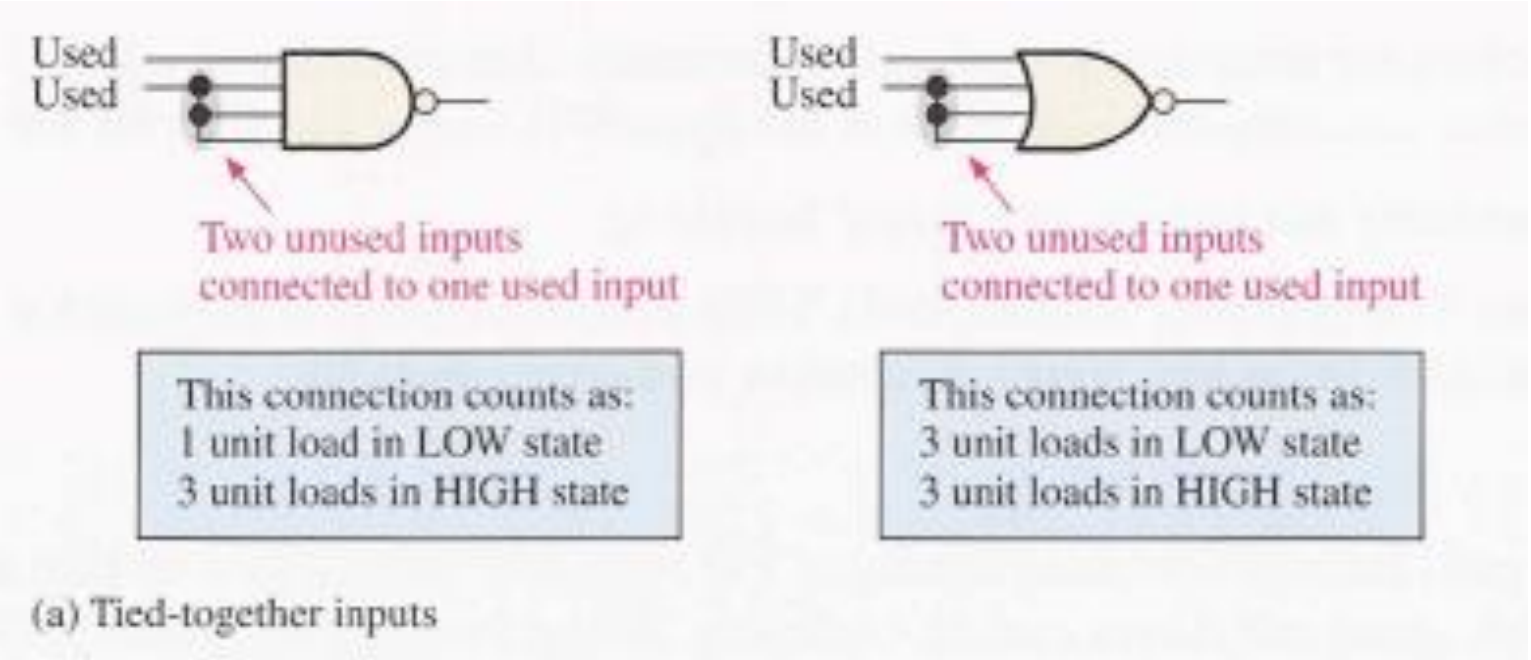
To sum up, the characteristic parameters and features of the standard TTL family of devices include the following: $V_{IL} = 0.8\,V$; $V_{IH} = 2\,V$; $I_{IH} = 40\,\mu A$; $I_{IL} = 1.6\,mA$; $V_{OH} = 2.4\,V$; $V_{OL} = 0.4\,V$; $I_{OH} = 400\,\mu A$; $I_{OL} = 16\,mA$; $V_{CC} = 4.75–5.25\,V$ (74-series) and 4.5–5.5 V (54-series); propagation delay (for a load resistance of $400\,\Omega$, a load capacitance of 15 pF and an ambient temperature of 25 °C) = 22 ns (max.) for LOW-to-HIGH transition at the output and 15 ns (max.) for HIGH-to-LOW output transition; worst-case noise margin = 0.4 V; fan-out = 10; I_{CCH} (for all four gates) = 8 mA; I_{CCL} (for all four gates) = 22 mA; operating temperature range = 0–70 °C (74-series) and −55 to +125 °C (54-series); speed–power product = 100 pJ; maximum flip-flop toggle frequency = 35 MHz.

UNUSED TTL INPUTS

- An unconnected input on a TTL gate acts as a HIGH because an open input results in a reverse-biased emitter junction on the input transistor, just as a HIGH level does as illustrated below.
- However because of the noise sensitivity, it is best not to leave unused TTL inputs unconnected (open).



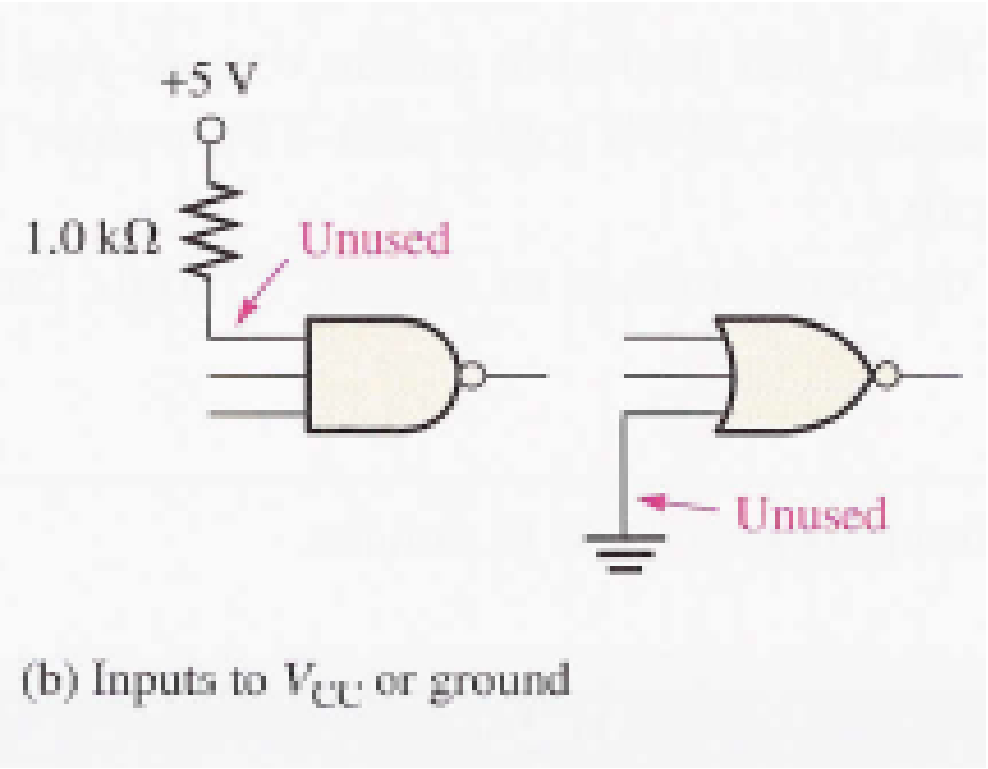
TIED-TOGETHER INPUTS



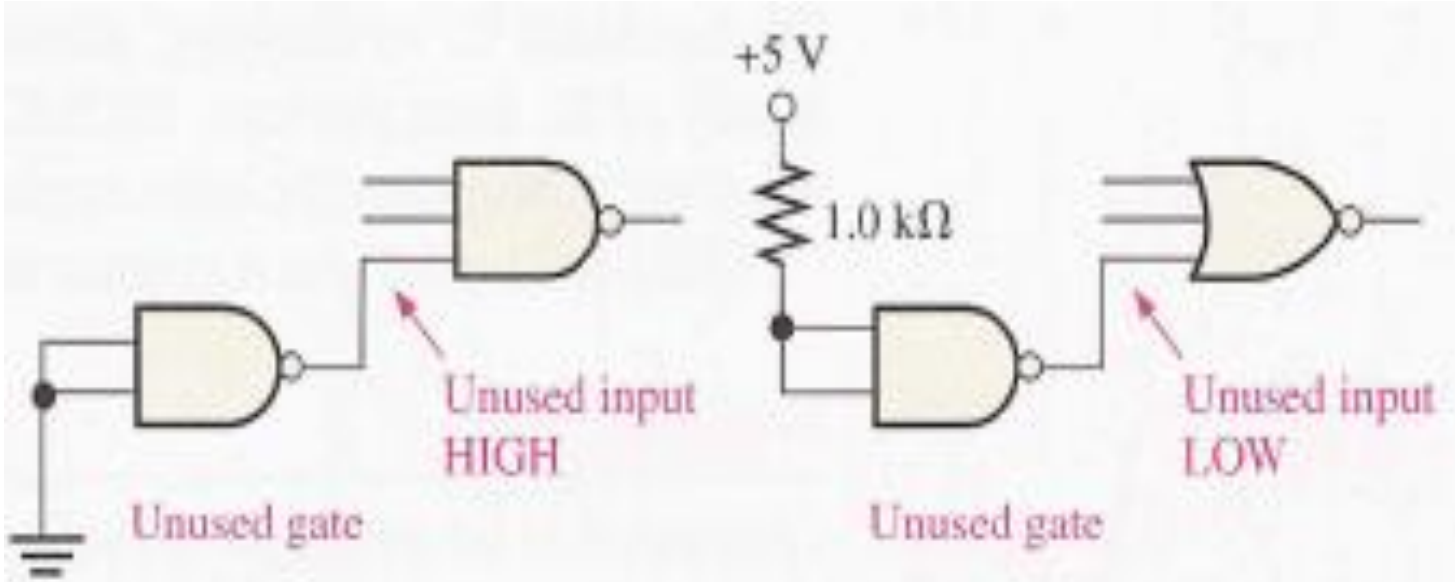
- The most common method for handling unused gate inputs is to connect them to a used input of the same gate.
- For AND gates and NAND gates, all tied-together inputs count as one unit load in the LOW state; but for OR gates and NOR gates each input tied to another input counts as a separate load for all types of TTL gates.

METHODS OF HANDLING UNUSED TTL INPUTS

- The AND and NAND gates present only single unit load no matter how many inputs are tied together, whereas OR and NOR gates present a unit load for each tied together input.
- This is because the NAND gates use multiple-emitter input transistor; so no matter how many inputs are LOW, the total LOW-state current is limited to a fixed value.
- The NOR gate uses a separate transistor for each input; therefore the LOW-state current is the sum of the currents from all the tied-together inputs.



(b) Inputs to V_{CC} or ground



(c) Inputs to unused output

- **Inputs to Vcc/Gnd**: Unused inputs of AND and NAND gates can be connected to Vcc through a ***1k-ohm*** resistor. This connection pulls the unused inputs to a HIGH level. Unused inputs OR and NOR gates can be connected to ground.
- **Inputs to Unused output**: A third method of terminating unused inputs may be appropriate in some cases when an unused gate or inverter is available. The unused gate output must be constant HIGH for used AND and NAND inputs and a constant LOW for unused OR and NOR inputs.

GUIDELINES TO USING TTL DEVICES

Replacing a TTL IC of one TTL subfamily with another belonging to another subfamily (the type numbers remaining the same) should not be done blindly. The designer should ensure that the replacement device is compatible with the existing circuit with respect to parameters such as output drive capability, input loading, speed and so on.

- None of the inputs and outputs of TTL ICs should be driven by more than ***0.5V*** below ground reference.
- Proper grounding techniques should be used while designing the PCB layout. If the grounding is improper, the ground loop currents give rise to voltage drops, with the result that different ICs will not be at the same reference. This effectively reduces the noise immunity.
- The power supply rail must always be properly decoupled with appropriate capacitors so that there is no drop in ***Vcc*** rail as the inputs and outputs make logic transitions.

- Usually, two capacitors are used at the *VCC* point of each IC. A *0.1F* ceramic disc should be used to take care of high-frequency noise, while typically a *10–20F* electrolytic is good enough to eliminate any low frequency variations resulting from variations in *ICC* current drawn from V*CC*, depending upon logic states of inputs and outputs. To be effective, the decoupling capacitors should be wired as close as feasible to the *VCC* pin of the IC.
- The unused inputs should not be left floating. All unused inputs should be tied to logic HIGH in the case of AND and NAND gates, and to ground in the case of OR and NOR gates. An alternative is to connect the unused input to one of the used inputs.
- While using open collector devices, resistive pull-up should be used. The value of pull-up resistance should be determined from the following equations:

$$R_X = [V_{CC}(\text{max.}) - V_{OL}]/[I_{OL} - N_2(\text{LOW}) \times 1.6]$$

$$R_X(\text{max.}) = [V_{CC}(\text{min.}) - V_{OH}]/[N_1 \times I_{OH} + N_2(\text{HIGH}) \times 40]$$

where *RX* is the external pull-up resistor; *RX(max.)* is the maximum value of the external pull-up resistor; *N1* is the number of WIRED-OR outputs; *N2* is the number of unit input loads being driven; *IOH* is the output HIGH leakage current *(in mA); IOL* is the LOW-level output current of the driving element *(in mA); VOL* is the LOW-level output voltage; and *VOH* is the HIGH-level output voltage. One TTL unit load in the HIGH state=40 mA, and one TTL unit load in the LOW-state=1.6 mA.