THIRD YEAR FIRST SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN MECHATRONIC ENGINEERING

EEE 2305: DIGITAL ELECTRONICS I

DATE: MARCH 2015 TIME: 2 HOURS

INSTRUCTIONS: ANSWER QUESTION ONE AND ANY OTHER TWO QUESTIONS

QUESTION ONE (30 MARKS)

a) Derive the Boolean expression for figure 1(a) and simplify. Implement the logic diagram for the simplified expression. (3 marks)

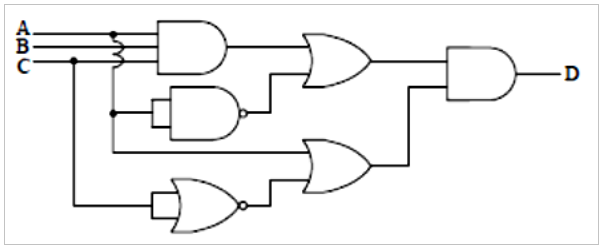

Figure 1(a)

b) What is a full subtractor? Design a full subtractor and implement the design using minimum of logic gates. Assume only 2-input gates are available and NOT gate.

(7 marks)

c) Implement the following Boolean function with a multiplexer (5 marks)

$$F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$$

d) Convert the BCD number 000100000011.0101 to its binary equivalent. (3 marks)

e) A staircase light is controlled by two switches one at the top of the stairs and another at the bottom of stairs. (6 marks)

i. Draw the circuit diagram of the system and create a truth table for this system

ii. Obtain the logic equation representing this system in SOP form.

iii. Realize the circuit using NAND gates only.

f) How is it possible to make a modulo 2^n counter using n-flip-flops? Draw the logic diagram of a mod-8 ripple counter using *JK* flip-flops.
(6 marks)

QUESTION TWO **(20 MARKS)**

a) Figure 2(a) shows four switches that are part of a control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time (they are far apart and the paper cannot cover them at the same time). The LED is to light if two or more switches are closed. Design a combinational logic circuit for the system and implement using NAND gates only.
(10 marks)

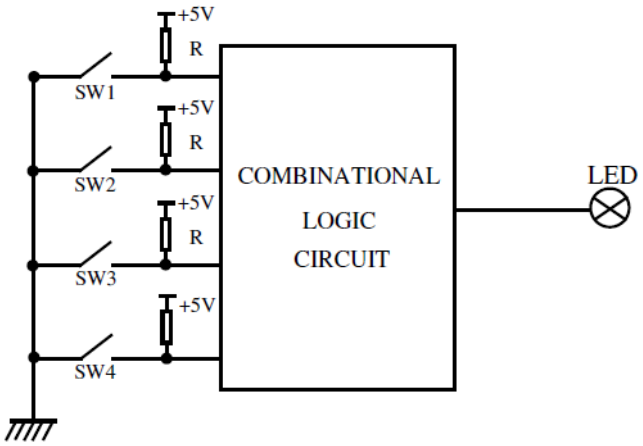

Figure 2(a)

b) Realize a JK flip-flop function using a SR) flip-flop. (5 marks)

c) An 8 X 1 multiplexer has inputs A, B and C connected to the selection inputs S_2, S_1 and S_0, respectively. The data inputs I_0 through I_7 are: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$ and $I_6 = \bar{D}$. Determine the Boolean function that the multiplexer implements. (5 marks)

QUESTION THREE (20 MARKS)

a) Design 4-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number). Show that the circuit can be constructed using OR and exclusive-OR gates only.
(15 marks)

b) A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations:

- A is False, B is True
- A is False, C is True
- A, B, C are False
- A, B, C are True

Represent the inputs and output in a Karnaugh map, simplify the output expression and draw the logic circuit diagram using minimum number of gates. (5 marks)

QUESTION FOUR (20 MARKS)

a) Minimize the logic function

$$Y(A,B,C,D) = \sum_{m}(0,1,2,3,5,7,8,9,11,14)$$

using a Karnaugh map and draw the logic circuit for the simplified function (6 marks)

b) Design a combinational circuit that converts a 4-bit Gray code to a 4-bit binary number. Implement the circuit with exclusive-OR gates only (12 marks)

c) Find the hex sum of $(93)_{16} + (DE)_{16}$

(2 marks)

QUESTION FIVE (20 MARKS)

a) Simplify the expression below using Boolean laws and theorems

$$Y = (A+B)\overline{(A+C)}(B+C)$$ (3 marks)

b) Verify that the NAND operation is not associative.

(4 marks)

c) With the help of clocked JK flip flops and waveforms, explain the working of a three bit binary ripple counter. Write the truth table for clock transitions.
(13 marks)