INSTITUTION: DEDAN KIMATHI UNIVERSITY OF TECHNOLOGY

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TASK: CAT II

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SIGNATURE:

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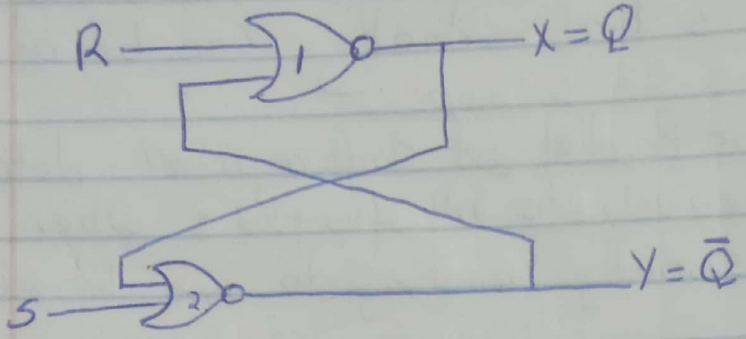
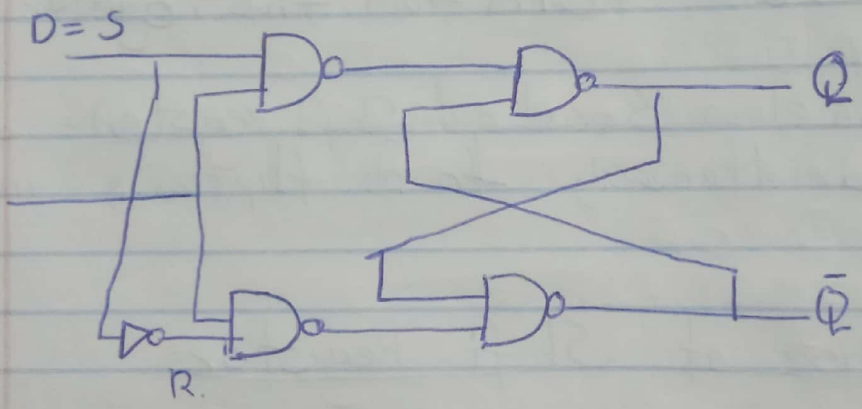
@ Symbols of R-S, J-k, T & D flip flops.

soln.

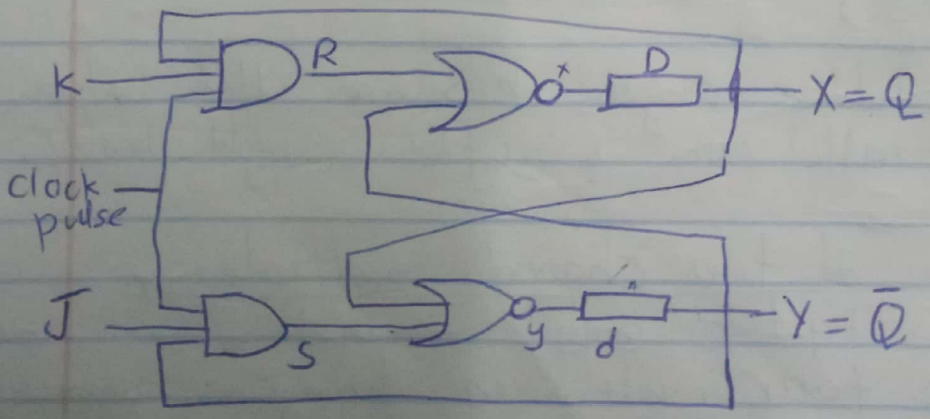
R-S flip flop



D flip flop



J-K flip flop



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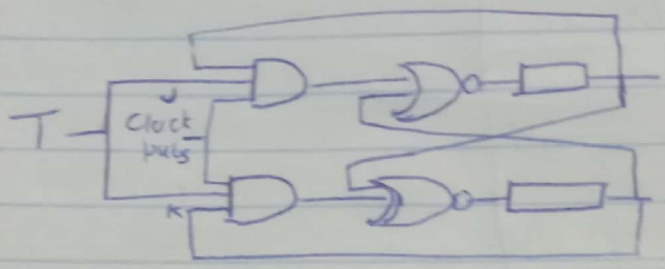
T flip-flop



(ii) Truth table of the flip-flops

J-K flip-flop

J	K	Q	$\bar{Q}$	Comments
0	0	Q_0	$\bar{Q}_0$	No change
0	1	0	1	reset flip-flop
1	0	1	0	set flip-flop
1	1	$-Q_0$	Q_0	JK flipflop toggled

RS flip flop

R	S	Q	-Q	Comments
0	0	Q_0	$-Q_0$	Store current value
1	0	0	1	reset flip flop
0	1	1	0	set flipflop
1	1	0	0	Invalid input condition

T flip-flop

Input T	previous output	Next Output	Mode of Operation
0	0	0	Store
0	1	1	
1	0	1	Complement
1	1	0	

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D flip flop

D_n	Q_n	Q_{n+1}
0	0	1
0	1	0
1	0	1
1	1	1

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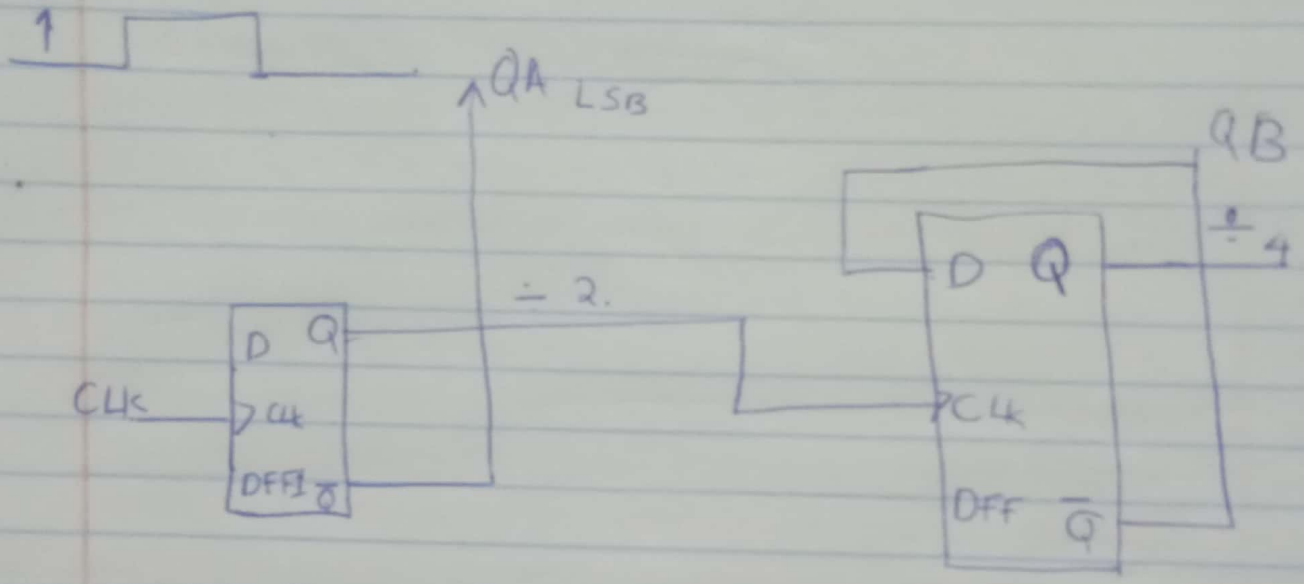
With timing diagrams explain

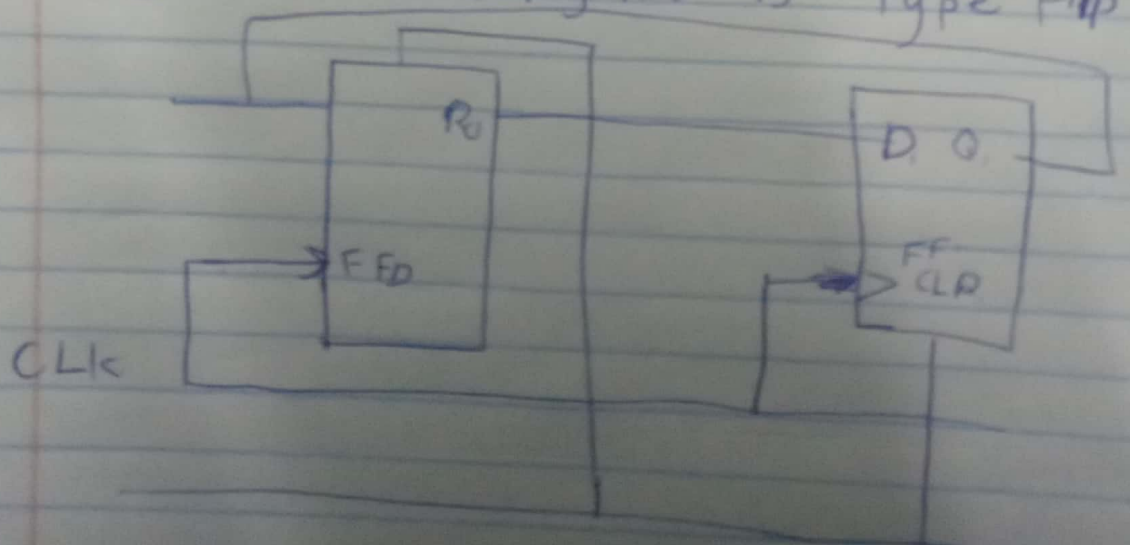
(i) a modulo 4 counter using two T types flip flop



~~a modulo~~

a modulo of counter is the number of different output state a counter can produce. This is the total number of unique states it passes through in a complete country

(ii) Ring counter using two D type flip flops



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What do you nderstand by SISO, PIPO, SIPO, & PISO

(i) SISO (serial in serial out shift register) In SISO, data is loaded serially one bit at a time, and when output is required, data stored in the register data is read serially one bit at a time

(PIPO) (Parallel in Parallel out shift register) data is loaded simultaneously to all flipflops & when read is read serially from register one bit at a time

(SIPO) Serial in parallel out shift register. Data is loaded serially to the shift register and read in parallel form from the register.

(PISO) (Parallel in Serial out Shift register) = data is loaded simultaneously to all flipflops in parallel form.

Applications of Shift Registers

(i) Parity Generator cum Checker → use to generate the parity bit of 4 bit number

(ii) Serial Adder original bits are added bits are loaded parallel form & shifted in right direction

Operation of two channel multiplexer consists of two input multiplexers on single chip The four multiplexers have a common data select lines & a common chip enable terminal. A low signal to the chip enable terminal G allow the selected input data to route to output. Because of the two inputs, a single data select is sufficient