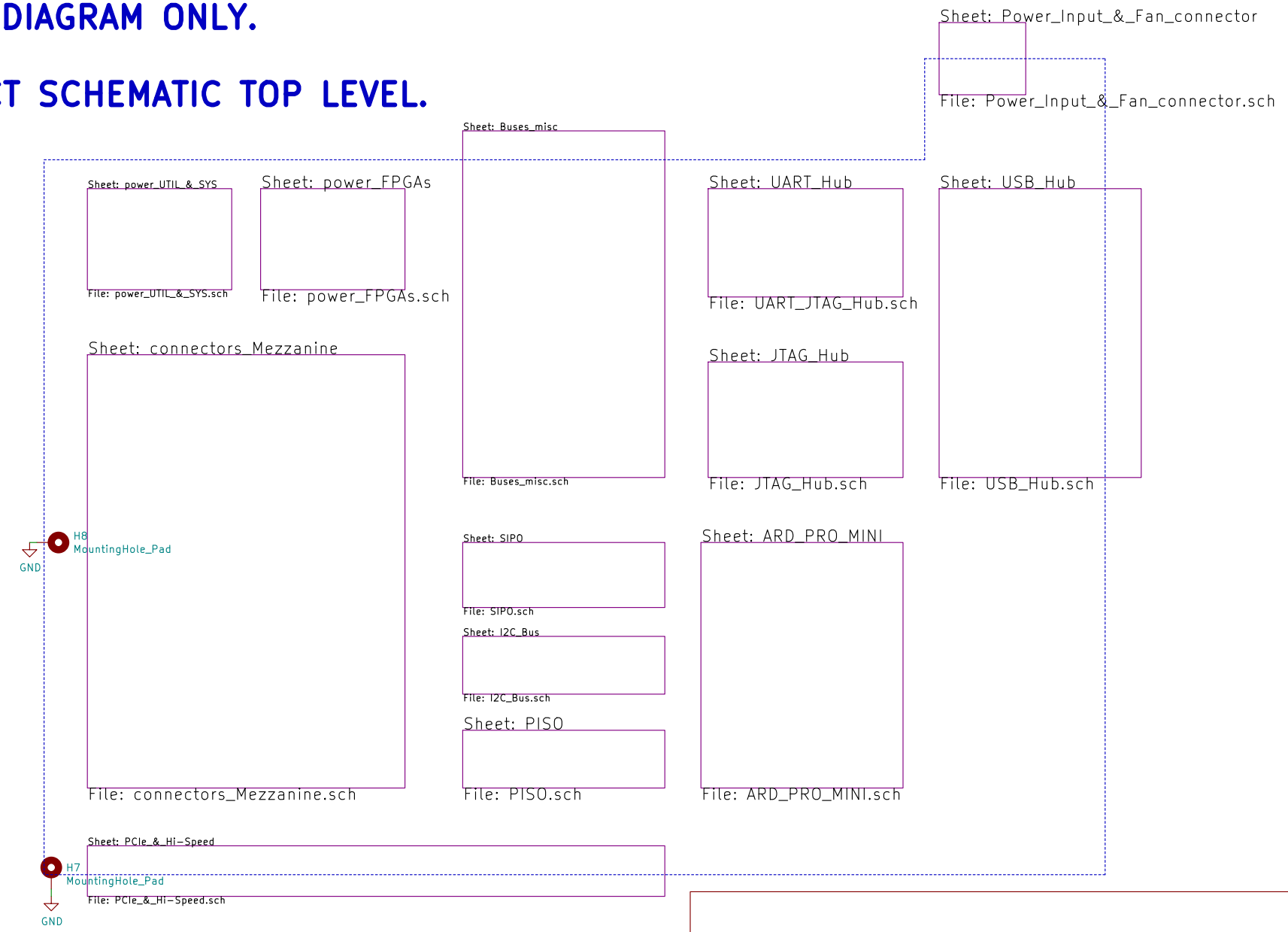
BLOCK DIAGRAM ONLY.

PROJECT SCHEMATIC TOP LEVEL.



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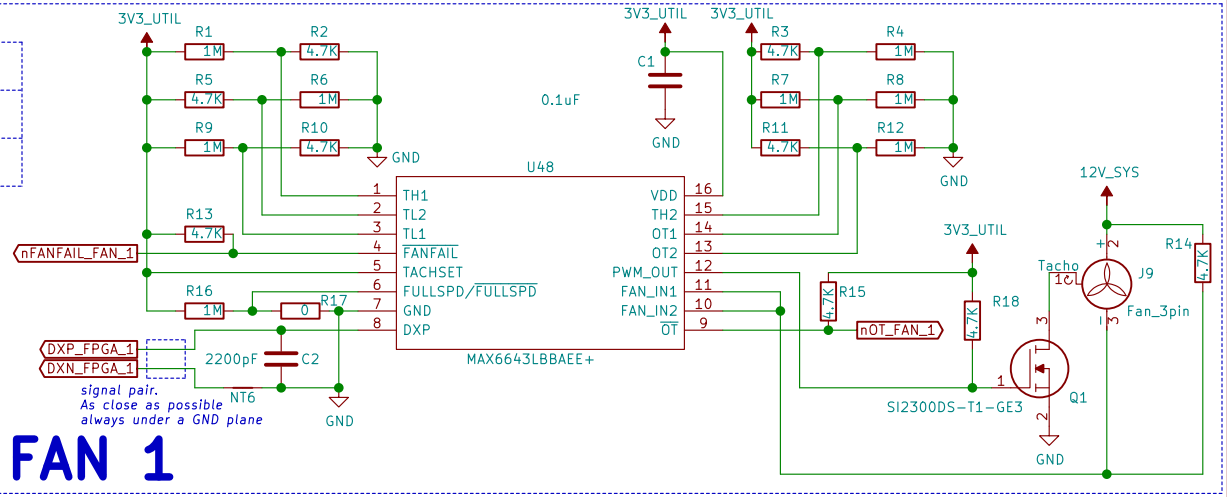
Sheet: /
File: Alto-Ultra+.sch

Title: Alto_Ultra_Plus

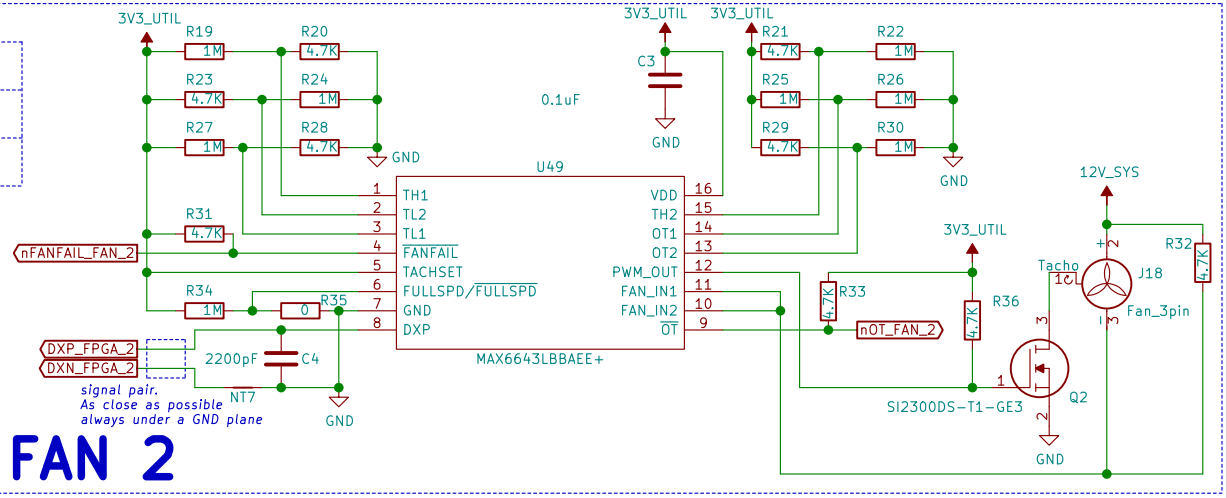
Size: USLetter	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 1/25

TH2: 1	TH1: 0	ThighL: 50Deg	ThighH: 70Deg
TL2: 1	TL1: 0	Tlow: 45Deg	
OT2: 1	OT1: Hi-Z	OT: 95Deg	

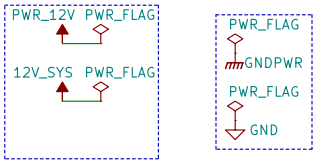


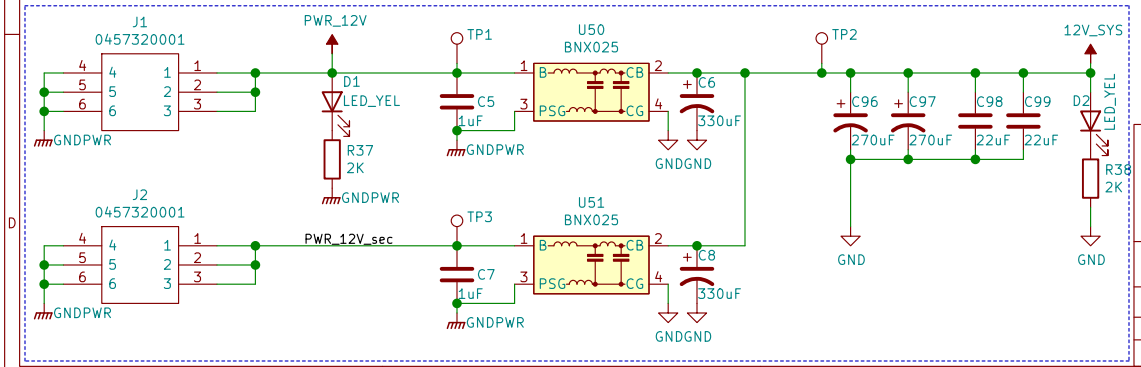
FAN 1

TH2: 1	TH1: 0	ThighL: 50Deg	ThighH: 70Deg
TL2: 1	TL1: 0	Tlow: 45Deg	
OT2: 1	OT1: Hi-Z	OT: 95Deg	



FAN 2





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Sheet: /Power_Input_&_Fan_connector/
File: Power_Input_&_Fan_connector.sch

Title: Alto_Ultra_Plus

Size: USLetter	Date: 2024-01-01	**Rev: 1.0**
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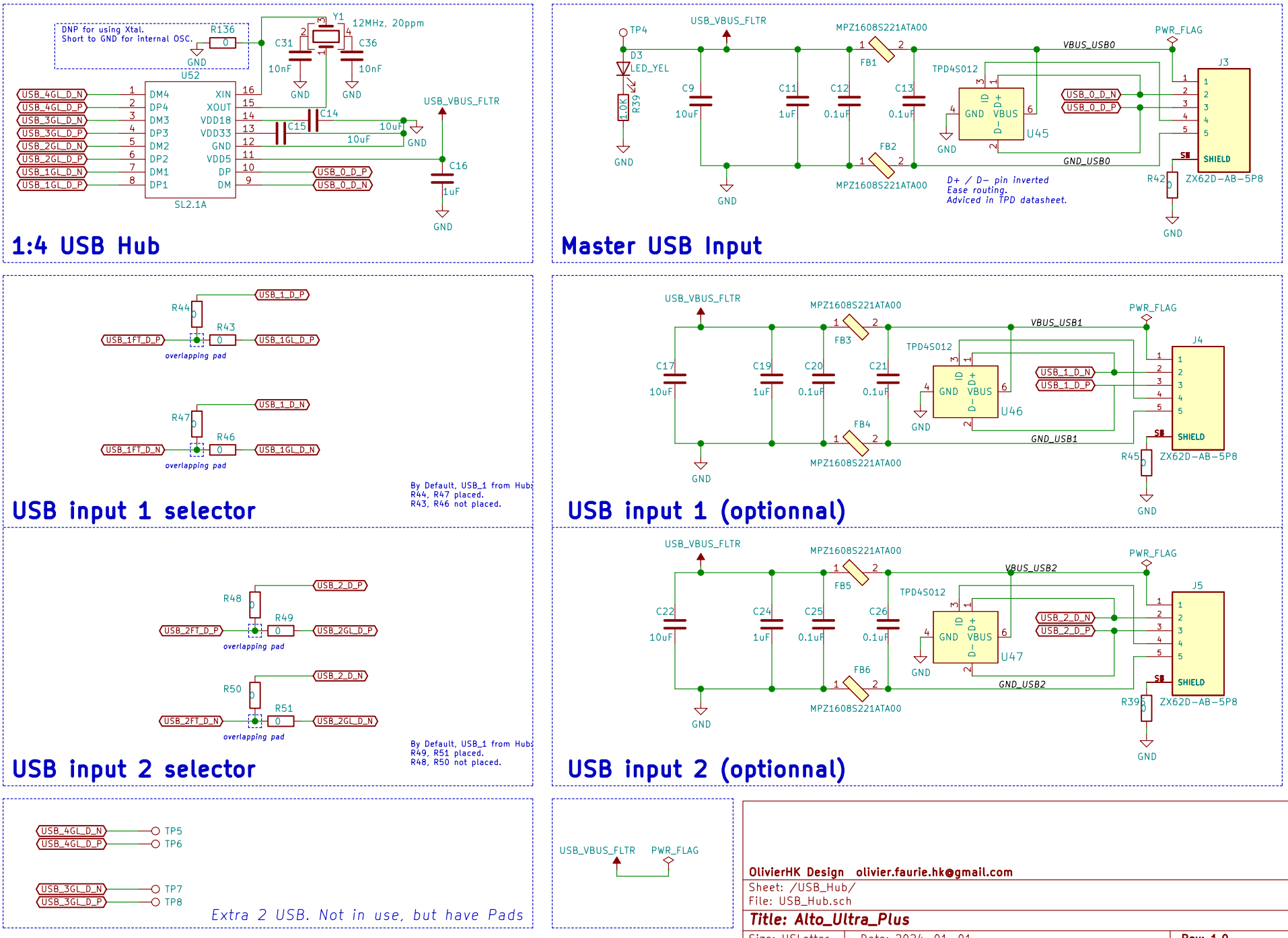
DNP for using Xtal.
Short to GND for internal OSC.
R136
0
GND
Y1
12MHz, 20ppm
C31
10nF
C36
10nF
U52
SL2.1A
USB_4GL_D_N
USB_4GL_D_P
USB_3GL_D_N
USB_3GL_D_P
USB_2GL_D_N
USB_2GL_D_P
USB_1GL_D_N
USB_1GL_D_P
DM4
DP4
DM3
DP3
DM2
DP2
DM1
DP1
XIN
XOUT
VDD18
VDD33
GND
VDD5
DP
DM
C14
C15
10uF
C16
1uF
USB_VBUS_FLTR
USB_0_D_P
USB_0_D_N
1:4 USB Hub
TP4
D3
LED_YEL
1.0K
R39
C9
10uF
C11
1uF
C12
0.1uF
C13
0.1uF
MPZ1608S221ATA00
FB1
FB2
TPD4S012
U45
VBUS_USB0
GND_USB0
PWR_FLAG
J3
SHIELD
R42
ZX62D-AB-5P8
D+ / D- pin inverted
Ease routing.
Adviced in TPD datasheet.
Master USB Input
R44
R43
R47
R46
USB_1FT_D_P
USB_1FT_D_N
USB_1GL_D_P
USB_1GL_D_N
USB_1_D_P
USB_1_D_N
overlapping pad
By Default, USB_1 from Hub
R44, R47 placed.
R43, R46 not placed.
USB input 1 selector
C17
10uF
C19
1uF
C20
0.1uF
C21
0.1uF
FB3
FB4
VBUS_USB1
GND_USB1
J4
R45
USB input 1 (optionnal)
R48
R49
R50
R51
USB_2FT_D_P
USB_2FT_D_N
USB_2GL_D_P
USB_2GL_D_N
USB_2_D_P
USB_2_D_N
By Default, USB_1 from Hub
R49, R51 placed.
R48, R50 not placed.
USB input 2 selector
C22
10uF
C24
1uF
C25
0.1uF
C26
0.1uF
FB5
FB6
VBUS_USB2
GND_USB2
J5
R39
USB input 2 (optionnal)
TP5
TP6
TP7
TP8
Extra 2 USB. Not in use, but have Pads
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Sheet: /USB_Hub/
File: USB_Hub.sch
Title: Alto_Ultra_Plus
Size: USLetter
Date: 2024-01-01
Rev: 1.0
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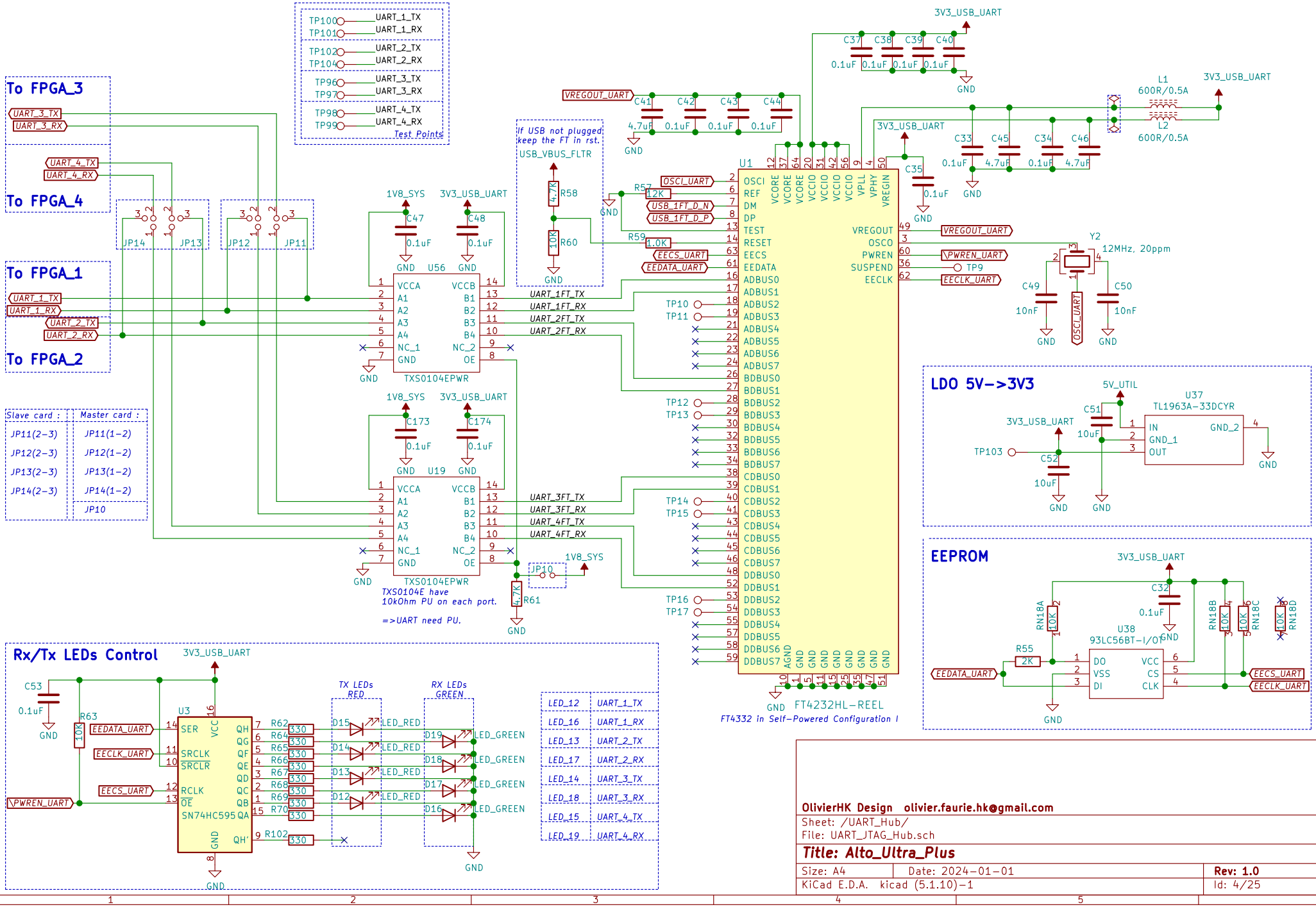
Id: 3/25


To FPGA_3
UART_3_TX
UART_3_RX
To FPGA_4
UART_4_TX
UART_4_RX
To FPGA_1
UART_1_TX
UART_1_RX
To FPGA_2
UART_2_TX
UART_2_RX
TP100 UART_1_TX
TP101 UART_1_RX
TP102 UART_2_TX
TP104 UART_2_RX
TP96 UART_3_TX
TP97 UART_3_RX
TP98 UART_4_TX
TP99 UART_4_RX
Test Points
JP14 JP13 JP12 JP11
Slave card : Master card :
JP11(2-3) JP11(1-2)
JP12(2-3) JP12(1-2)
JP13(2-3) JP13(1-2)
JP14(2-3) JP14(1-2)
JP10
1V8_SYS
3V3_USB_UART
U56 TXS0104EPWR
U19 TXS0104EPWR
VCCA VCCB A1 A2 A3 A4 NC_1 GND B1 B2 B3 B4 NC_2 OE
UART_1FT_TX
UART_1FT_RX
UART_2FT_TX
UART_2FT_RX
UART_3FT_TX
UART_3FT_RX
UART_4FT_TX
UART_4FT_RX
TXS0104E have
10kOhm PU on each port.
=>UART need PU.
If USB not plugged
keep the FT in rst.
USB_VBUS_FLTR
R58 4.7K
R60 10K
R61 4.7K
U1 FT4232HL-REEL
FT4332 in Self-Powered Configuration I
OSCI REF DM DP TEST RESET EECS EEDATA ADBUS0 ADBUS1 ADBUS2 ADBUS3 ADBUS4 ADBUS5 ADBUS6 ADBUS7 BDBUS0 BDBUS1 BDBUS2 BDBUS3 BDBUS4 BDBUS5 BDBUS6 BDBUS7 CDBUS0 CDBUS1 CDBUS2 CDBUS3 CDBUS4 CDBUS5 CDBUS6 CDBUS7 DDBUS0 DDBUS1 DDBUS2 DDBUS3 DDBUS4 DDBUS5 DDBUS6 DDBUS7
VCORE VCCIO VPLL VPHY VREGIN VREGOUT OSCO PWREN SUSPEND EECLK AGND
OSCI_UART
USB_1FT_D_N
USB_1FT_D_P
EECS_UART
EEDATA_UART
VREGOUT_UART
\PWREN_UART
EECLK_UART
R57 1.2K
R59 1.0K
TP9
Y2 12MHz, 20ppm
C49 10nF
C50 10nF
LDO 5V->3V3
U37 TL1963A-33DCYR
5V_UTIL
IN GND_1 OUT GND_2
TP103
EEPROM
U38 93LC56BT-I/OT
DO VSS DI VCC CS CLK
R55 2K
RN18A RN18B RN18C RN18D 10K
Rx/Tx LEDs Control
U3 SN74HC595
SER SRCLK SRCLR RCLK OE QH QG QF QE QD QC QB QA QH'
TX LEDs RED
RX LEDs GREEN
LED_RED
LED_GREEN
R62 R64 R65 R66 R67 R68 R69 R70 R102 330
D15 D14 D13 D12 D19 D18 D17 D16
LED_12 UART_1_TX
LED_16 UART_1_RX
LED_13 UART_2_TX
LED_17 UART_2_RX
LED_14 UART_3_TX
LED_18 UART_3_RX
LED_15 UART_4_TX
LED_19 UART_4_RX
L1 600R/0.5A
L2 600R/0.5A
OlivierHK Design olivier.faurie.hk@gmail.com
Sheet: /UART_Hub/
File: UART_JTAG_Hub.sch
Title: Alto_Ultra_Plus
Size: A4
Date: 2024-01-01
Rev: 1.0
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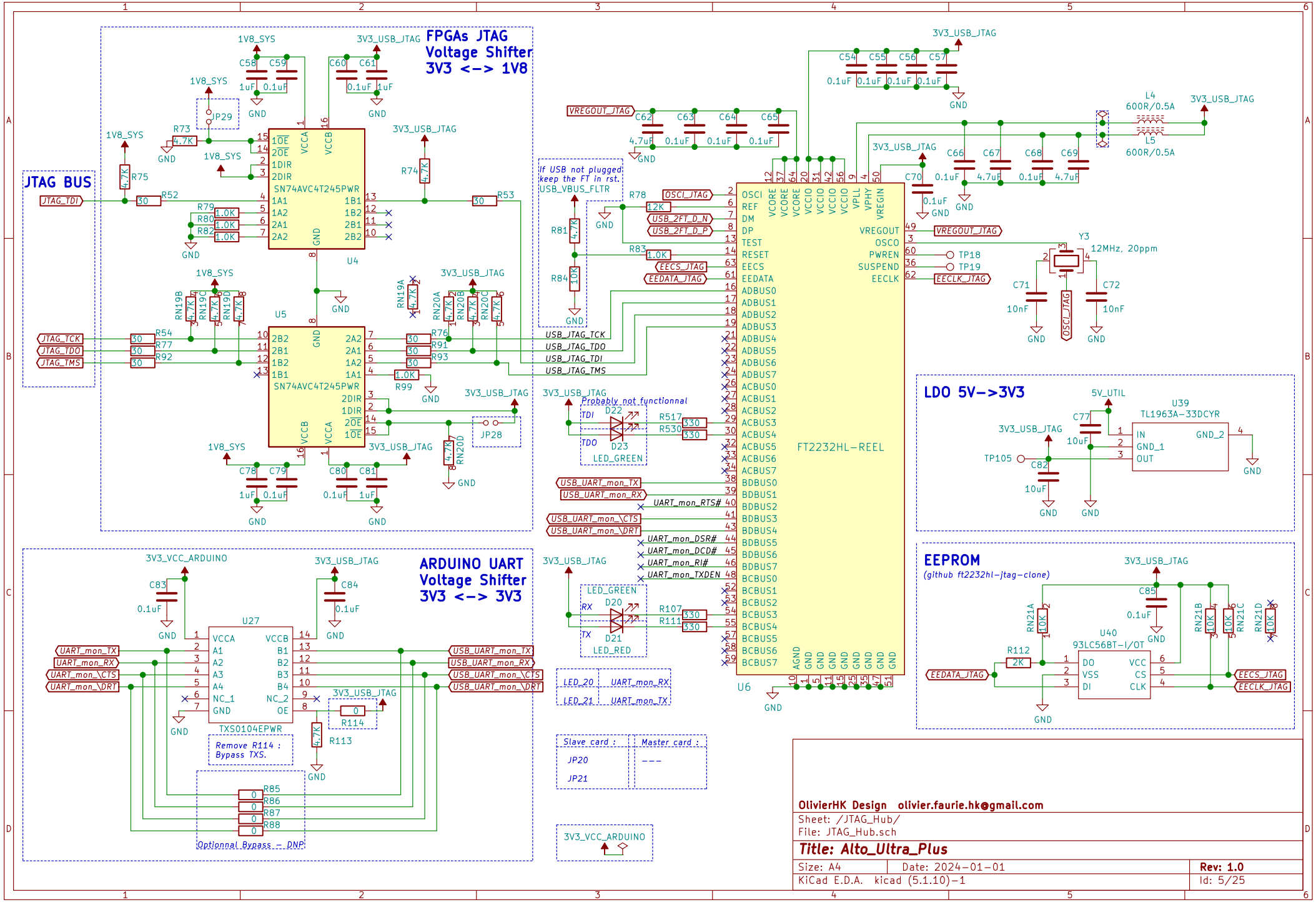
Id: 4/25


FPGAs JTAG
Voltage Shifter
3V3 <-> 1V8
JTAG BUS
SN74AVC4T245PWR
U4
U5
JP29
JP28
If USB not plugged
keep the FT in rst.
USB_VBUS_FLTR
FT2232HL-REEL
U6
Probably not functionnal
LED_GREEN
LED_RED
LDO 5V->3V3
U39
TL1963A-33DCYR
EEPROM
(github ft2232hl-jtag-clone)
U40
93LC56BT-I/OT
ARDUINO UART
Voltage Shifter
3V3 <-> 3V3
U27
TXS0104EPWR
Remove R114 :
Bypass TXS.
Optionnal Bypass - DNP
Slave card :
Master card :
JP20
JP21

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Sheet: /JTAG_Hub/
File: JTAG_Hub.sch
Title: Alto_Ultra_Plus
Size: A4
Date: 2024-01-01
Rev: 1.0
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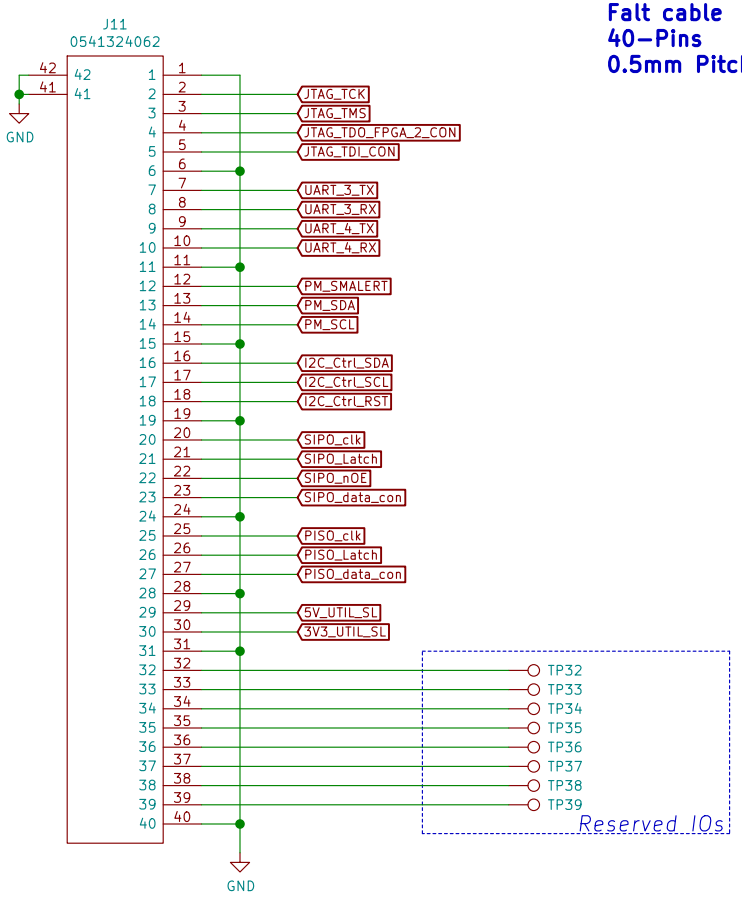
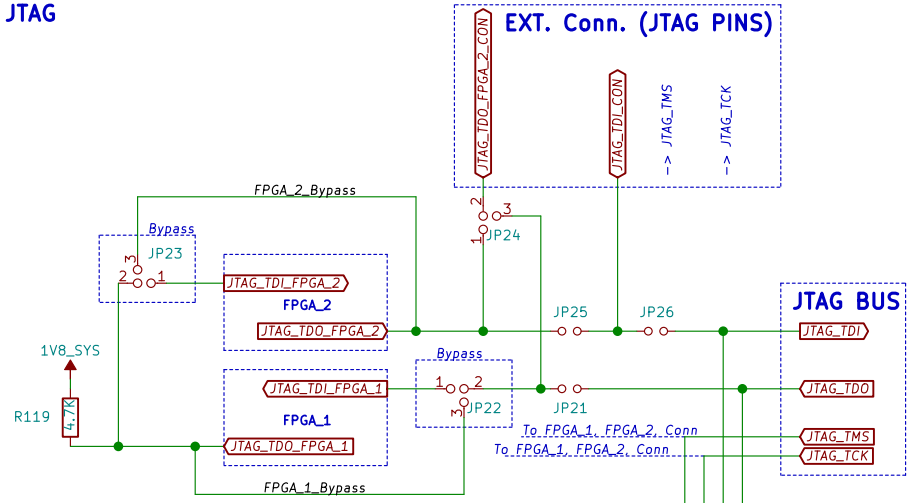
Id: 5/25

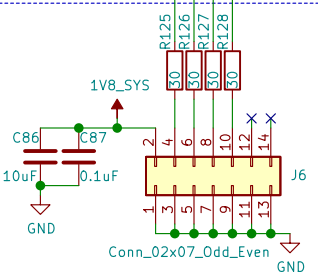
Falt cable 40-Pins 0.5mm Pitch



JTAG



Xilinx programmer cable (J6) [FPGA name -- Conn direction]	
2: 1V8	(Input - Vref)
4: TMS	(Output)
6: TCK	(Output)
8: TDI	(Output - J6_TDO)
10: TDO	(Input - J6_TDI)
1, 3, 5, 7, 9, 11, 13 : GND	
12, 14 : NC	



JTAG SETTING

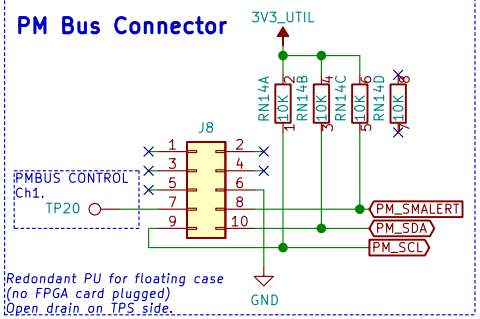
USB JTAG USED		
Master card:	Slave card:	Lone card:
JP21	JP24(2-3)	JP21
JP22(1-2)	JP22(1-2)	JP22(1-2)
JP23(1-2)	JP23(1-2)	JP23(1-2)
JP24(1-2)	JP25	JP25
JP26		JP26
	JP28 (V_Shftr)	
---	JP29 (V_Shftr)	---

JTAGE PROGRAMMER CABLE USED		
Master card:	Slave card:	Lone card:
JP21	JP24(2-3)	JP21
JP22(1-2)	JP22(1-2)	JP22(1-2)
JP23(1-2)	JP23(1-2)	JP23(1-2)
JP24(1-2)	JP25	JP25
JP26		JP26
JP28 (V_Shftr)	JP28 (V_Shftr)	JP28 (V_Shftr)
JP29 (V_Shftr)	JP29 (V_Shftr)	JP29 (V_Shftr)

To Bypass FPGA_1:
JP22(2-3)

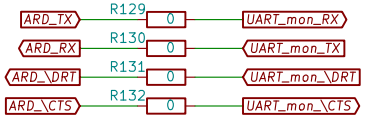
To Bypass FPGA_2:
JP23(2-3)

PM Bus Connector



To be removed If using ext. Programmer for the Arduino:
R129
R130
R131
R132

UART MON/PRG ARDUINO



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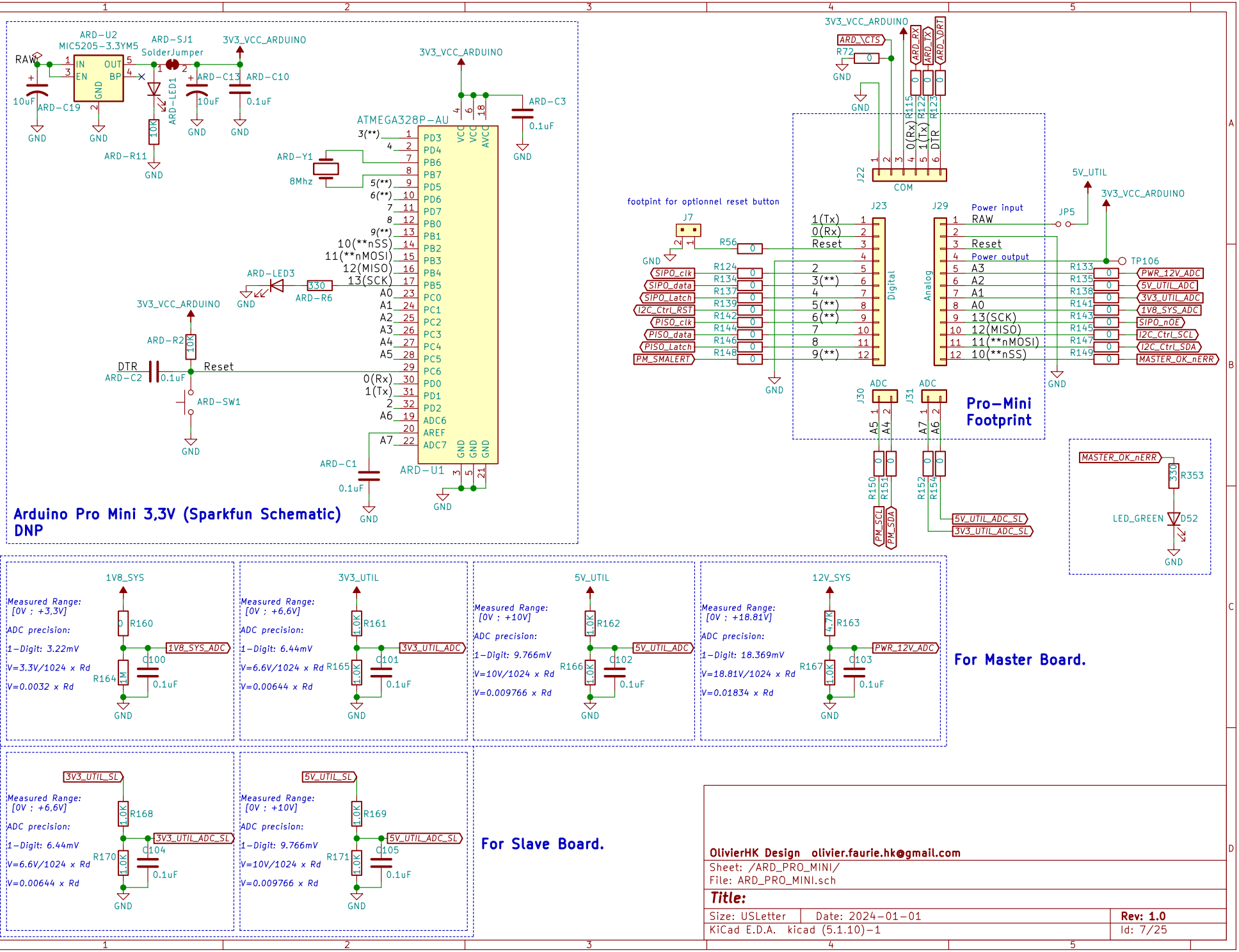
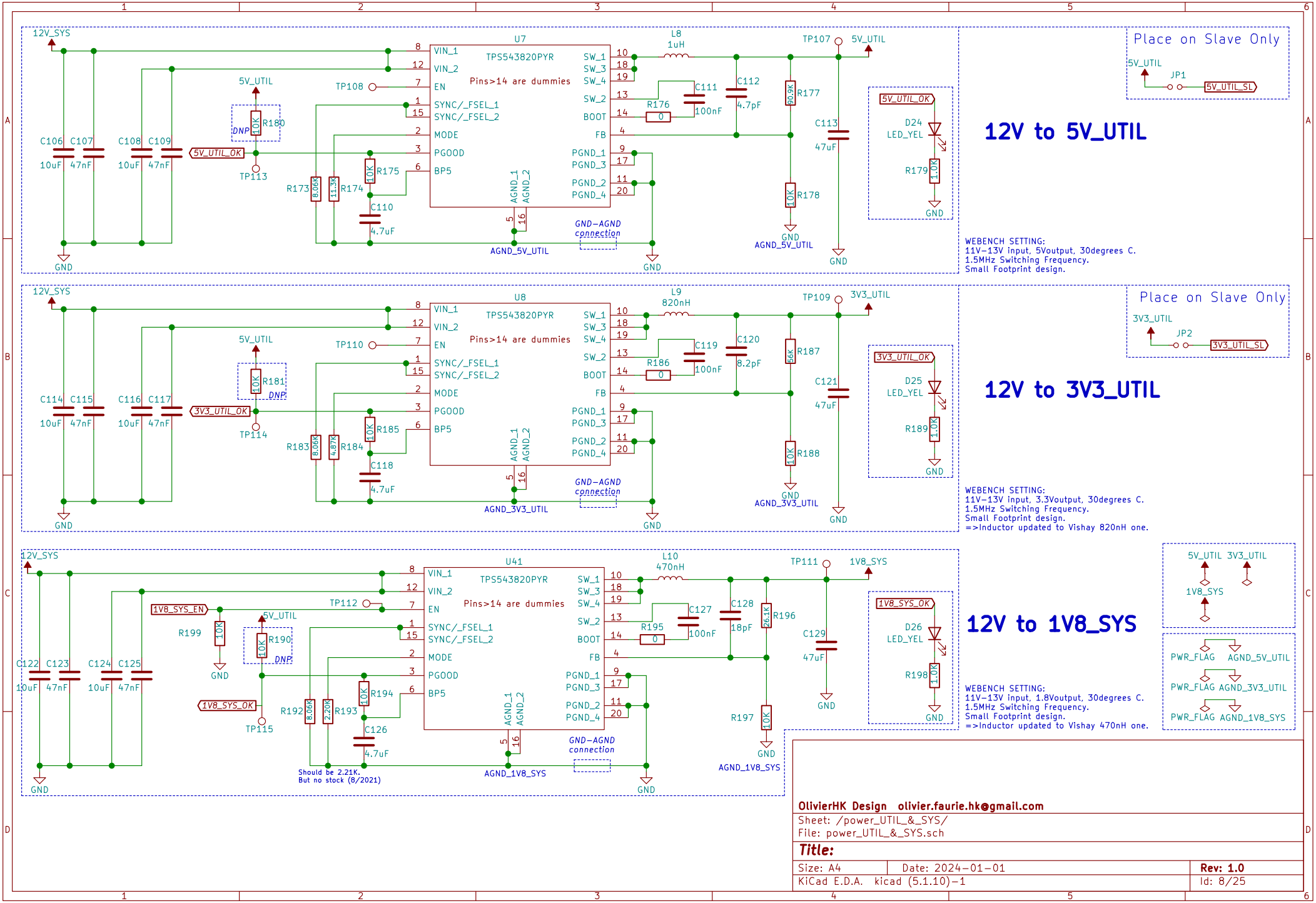
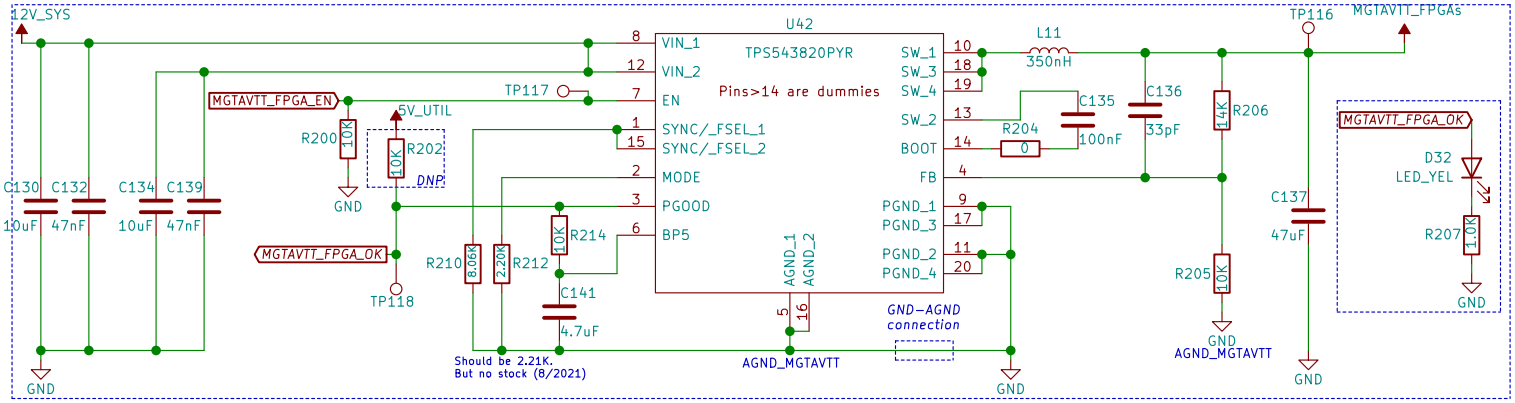
Sheet: /Buses_misc/
File: Buses_misc.sch

Title:

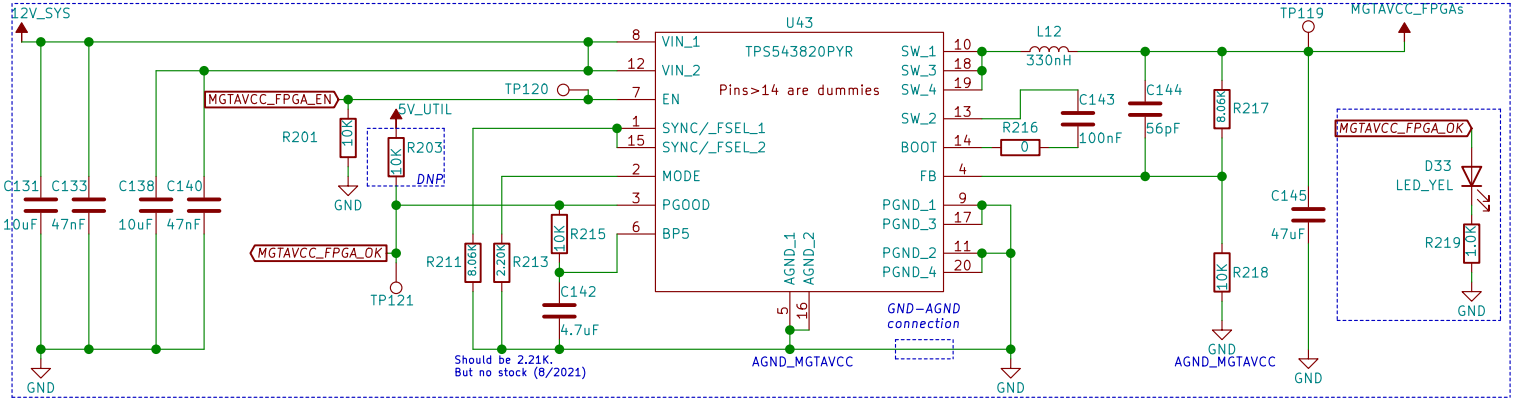
Size: USLetter	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 6/25


Arduino Pro Mini 3,3V (Sparkfun Schematic)
DNP
ARD-U2
MIC5205-3.3YM5
ARD-SJ1
SolderJumper
3V3_VCC_ARDUINO
RAW
10uF
ARD-C19
ARD-C13
ARD-C10
ARD-LED1
ARD-R11
ATMEGA328P-AU
ARD-Y1
8Mhz
ARD-C3
ARD-LED3
ARD-R6
ARD-R2
DTR
ARD-C2
Reset
ARD-SW1
ARD-C1
ARD-U1
GND
ARD_CTS
R72
ARD_RX
ARD_TX
ARD_VDRT
J22
COM
footpint for optionnel reset button
J7
R56
J23
Digital
J29
Power input
Power output
Analog
JP5
5V_UTIL
TP106
J30
J31
ADC
Pro-Mini
Footprint
MASTER_OK_nERR
R353
LED_GREEN
D52
1V8_SYS
3V3_UTIL
5V_UTIL
12V_SYS
Measured Range:
[0V ; +3,3V]
ADC precision:
1-Digit: 3.22mV
V=3.3V/1024 x Rd
V=0.0032 x Rd
R160
R164
C100
1V8_SYS_ADC
[0V ; +6,6V]
1-Digit: 6.44mV
V=6.6V/1024 x Rd
V=0.00644 x Rd
R161
R165
C101
3V3_UTIL_ADC
[0V ; +10V]
1-Digit: 9.766mV
V=10V/1024 x Rd
V=0.009766 x Rd
R162
R166
C102
5V_UTIL_ADC
[0V ; +18.81V]
1-Digit: 18.369mV
V=18.81V/1024 x Rd
V=0.01834 x Rd
R163
R167
C103
PWR_12V_ADC
For Master Board.
3V3_UTIL_SL
R168
R170
C104
3V3_UTIL_ADC_SL
5V_UTIL_SL
R169
R171
C105
5V_UTIL_ADC_SL
For Slave Board.
OlivierHK Design olivier.faurie.hk@gmail.com
Sheet: /ARD_PRO_MINI/
File: ARD_PRO_MINI.sch
Title:
Size: USLetter
Date: 2024-01-01
Rev: 1.0
KiCad E.D.A. kicad (5.1.10)-1
Id: 7/25


12V_SYS
U7
TPS543820PYR
Pins>14 are dummies
VIN_1
VIN_2
EN
SYNC/_FSEL_1
SYNC/_FSEL_2
MODE
PGOOD
BP5
SW_1
SW_3
SW_4
SW_2
BOOT
FB
PGND_1
PGND_3
PGND_2
PGND_4
AGND_1
AGND_2
L8
1uH
TP107
5V_UTIL
TP108
TP113
5V_UTIL_OK
DNP
R180
R173
8.06K
R174
11.3K
R175
10K
C110
4.7uF
C106
C107
C108
C109
10uF
47nF
C111
100nF
R176
0
C112
4.7pF
R177
90.9K
C113
47uF
R178
10K
D24
LED_YEL
R179
1.0K
GND
AGND_5V_UTIL
GND–AGND connection
Place on Slave Only
JP1
5V_UTIL_SL
12V to 5V_UTIL
WEBENCH SETTING:
11V–13V input, 5Voutput, 30degrees C.
1.5MHz Switching Frequency.
Small Footprint design.
U8
L9
820nH
TP109
3V3_UTIL
TP110
TP114
3V3_UTIL_OK
R181
R183
8.06K
4.87K
R184
R185
C118
C114
C115
C116
C117
C119
100nF
R186
C120
8.2pF
R187
56K
C121
R188
D25
R189
AGND_3V3_UTIL
Place on Slave Only
JP2
3V3_UTIL_SL
12V to 3V3_UTIL
WEBENCH SETTING:
11V–13V input, 3.3Voutput, 30degrees C.
1.5MHz Switching Frequency.
Small Footprint design.
=>Inductor updated to Vishay 820nH one.
U41
L10
470nH
TP111
1V8_SYS
TP112
TP115
1V8_SYS_EN
R199
R190
R192
8.06K
2.20K
R193
R194
C126
C122
C123
C124
C125
C127
100nF
R195
C128
18pF
R196
26.1K
C129
R197
D26
R198
AGND_1V8_SYS
Should be 2.21K.
But no stock (8/2021)
12V to 1V8_SYS
WEBENCH SETTING:
11V–13V input, 1.8Voutput, 30degrees C.
1.5MHz Switching Frequency.
Small Footprint design.
=>Inductor updated to Vishay 470nH one.
5V_UTIL
3V3_UTIL
1V8_SYS
PWR_FLAG
AGND_5V_UTIL
AGND_3V3_UTIL
AGND_1V8_SYS
OlivierHK Design olivier.faurie.hk@gmail.com
Sheet: /power_UTIL_&_SYS/
File: power_UTIL_&_SYS.sch
Title:
Size: A4
Date: 2024–01–01
Rev: 1.0
KiCad E.D.A. kicad (5.1.10)–1
Id: 8/25

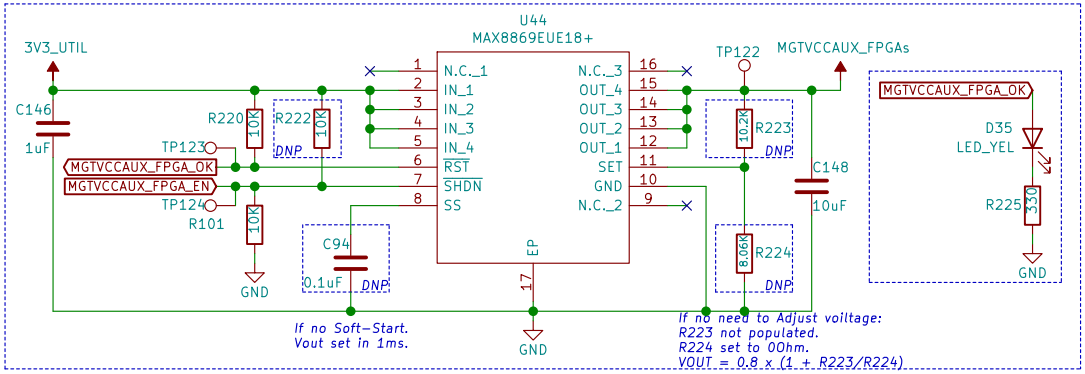


12V to 1V2_FPGA (MGTAVTT_FPGA)

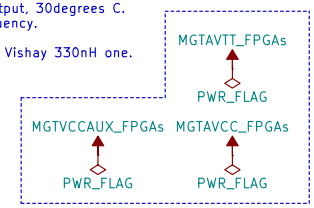


12V to 0V9_FPGA (MGTAVCC_FPGA)

WEBENCH SETTING:
11V–13V input, 0.9Voutput, 30degrees C.
1.5MHz Switching Frequency.
Small Footprint design.
=>Inductor updated to Vishay 330nH one.



3V3 to 1V8_FPGA_AUX (MGTVCCAUX_FPGA)



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Sheet: /power_FPGAs/
File: power_FPGAs.sch

Title:

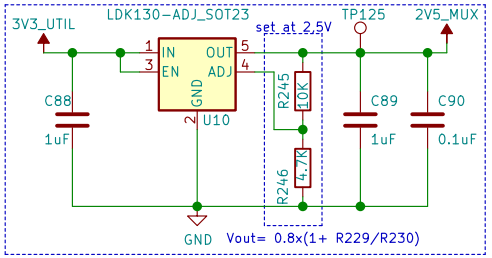
Size: A4	Date: 2024–01–01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)–1		Id: 9/25

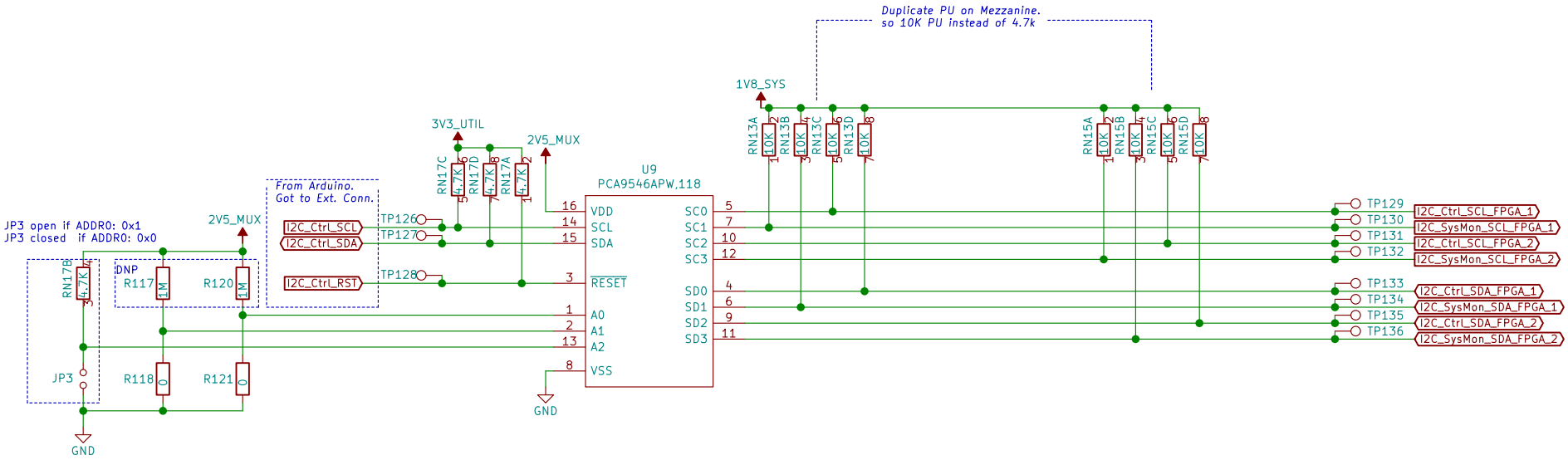
ADDRESS PCA9546APW: [ONLY ONE CHANNEL ACTIVE AT A TIME]

0xE0 (if A0=0x0) [Master Board] – JP3 Closed
0xE2 (if A0=0x1) [Slave Board] – JP3 Open

Command sequence:

1. Select address: (0xE0 or 0xE2) + (0x0 if Writing, 0x1 if reading).
2. Ctrl Register: 0xX || (0x8 +CH.ID)
3. I2C message Rd/Wr as usual.





CH0:	I2C Ctrl FPGA_1
CH1:	I2C SysMon FPGA_1
CH2:	I2C Ctrl FPGA_2
CH3:	I2C SysMon FPGA_2

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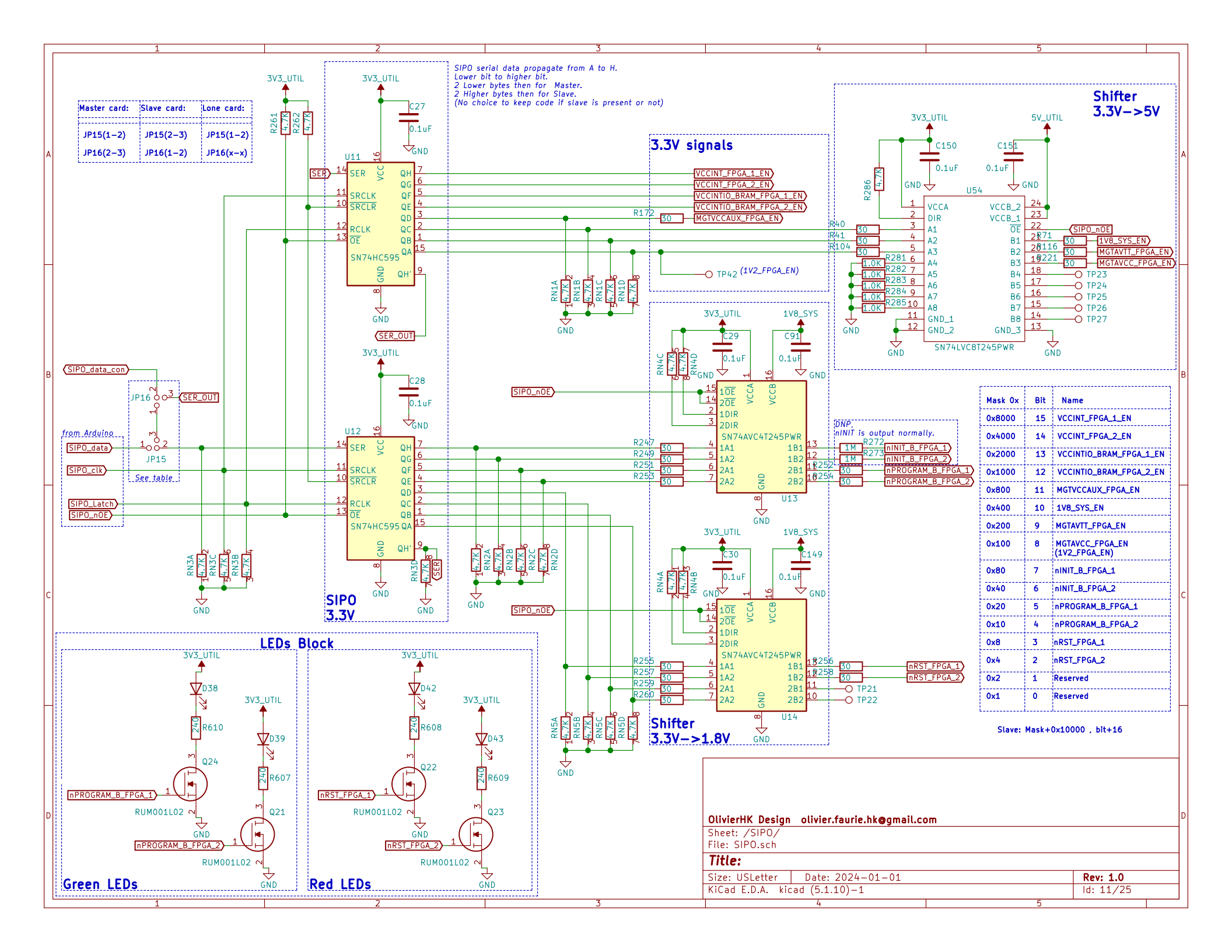
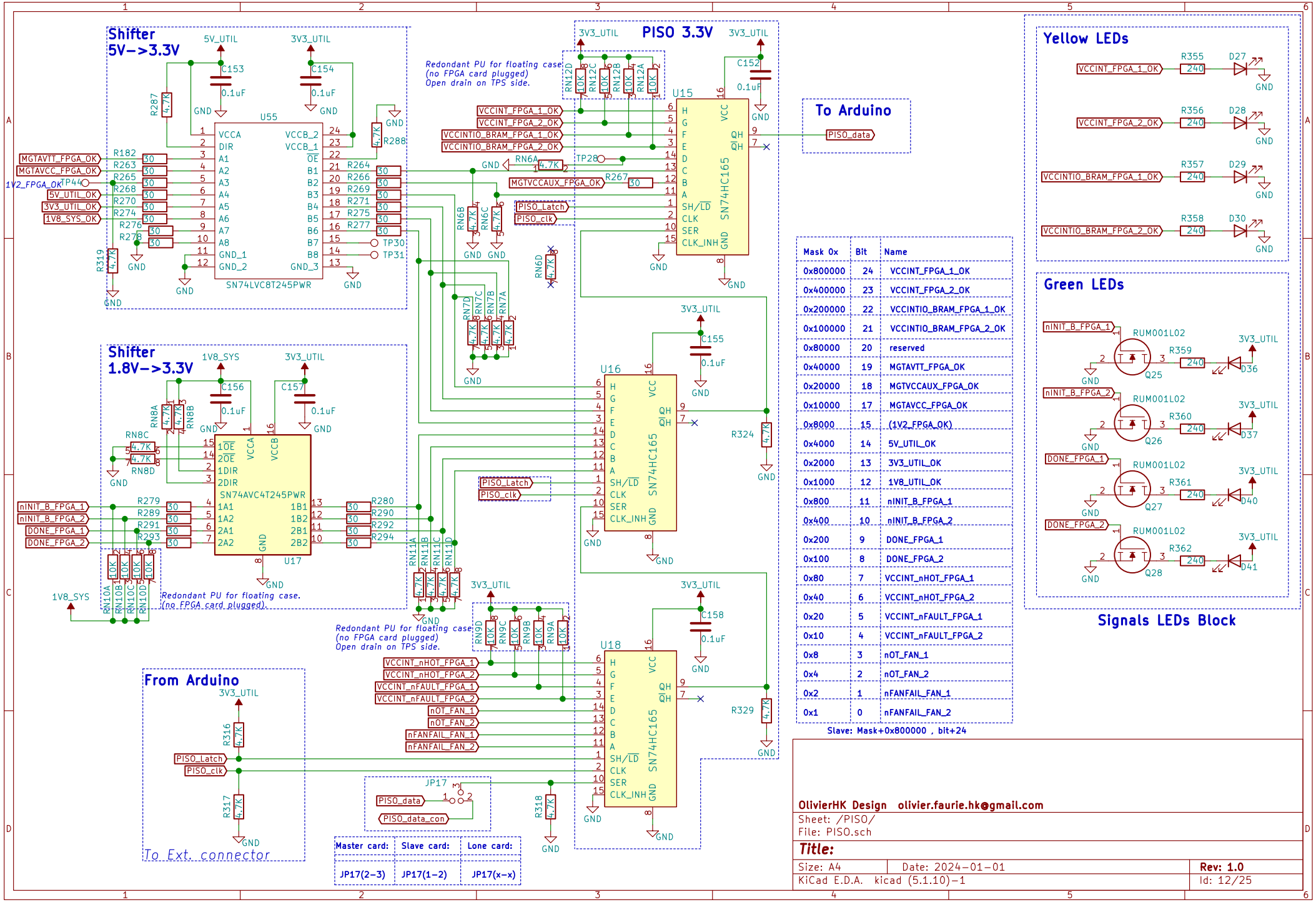
Sheet: /I2C_Bus/
File: I2C_Bus.sch

Title:

Size: USLetter	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 10/25



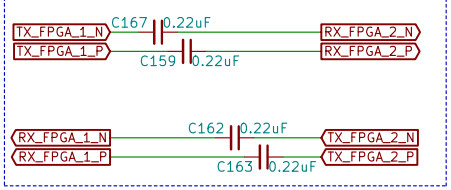
Mask 0x	Bit	Name
0x8000	15	VCCINT_FPGA_1_EN
0x4000	14	VCCINT_FPGA_2_EN
0x2000	13	VCCINTIO_BRAM_FPGA_1_EN
0x1000	12	VCCINTIO_BRAM_FPGA_2_EN
0x800	11	MGTVCCAUX_FPGA_EN
0x400	10	1V8_SYS_EN
0x200	9	MGTAVTT_FPGA_EN
0x100	8	MGTAVCC_FPGA_EN (1V2_FPGA_EN)
0x80	7	nINIT_B_FPGA_1
0x40	6	nINIT_B_FPGA_2
0x20	5	nPROGRAM_B_FPGA_1
0x10	4	nPROGRAM_B_FPGA_2
0x8	3	nRST_FPGA_1
0x4	2	nRST_FPGA_2
0x2	1	Reserved
0x1	0	Reserved



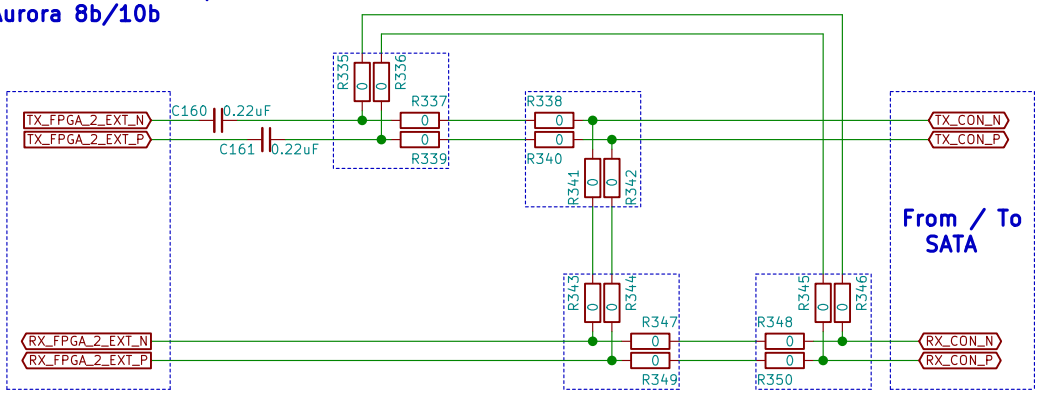
Mask 0x	Bit	Name
0x800000	24	VCCINT_FPGA_1_OK
0x400000	23	VCCINT_FPGA_2_OK
0x200000	22	VCCINTIO_BRAM_FPGA_1_OK
0x100000	21	VCCINTIO_BRAM_FPGA_2_OK
0x80000	20	reserved
0x40000	19	MGTAVTT_FPGA_OK
0x20000	18	MGTVCCAUX_FPGA_OK
0x10000	17	MGTAVCC_FPGA_OK
0x8000	15	(1V2_FPGA_OK)
0x4000	14	5V_UTIL_OK
0x2000	13	3V3_UTIL_OK
0x1000	12	1V8_UTIL_OK
0x800	11	nINIT_B_FPGA_1
0x400	10	nINIT_B_FPGA_2
0x200	9	DONE_FPGA_1
0x100	8	DONE_FPGA_2
0x80	7	VCCINT_nHOT_FPGA_1
0x40	6	VCCINT_nHOT_FPGA_2
0x20	5	VCCINT_nFAULT_FPGA_1
0x10	4	VCCINT_nFAULT_FPGA_2
0x8	3	nOT_FAN_1
0x4	2	nOT_FAN_2
0x2	1	nFANFAIL_FAN_1
0x1	0	nFANFAIL_FAN_2

Slave: Mask+0x800000 , bit+24

Inter-FPGAs Hi-Speed x1 Lane
Aurora 8b/10b

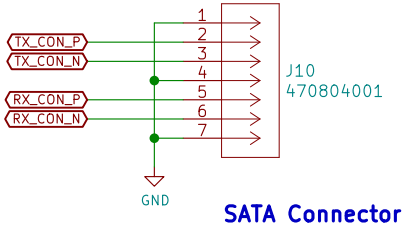


FPGA_2 SATA Hi-Speed x1 Lane
Aurora 8b/10b

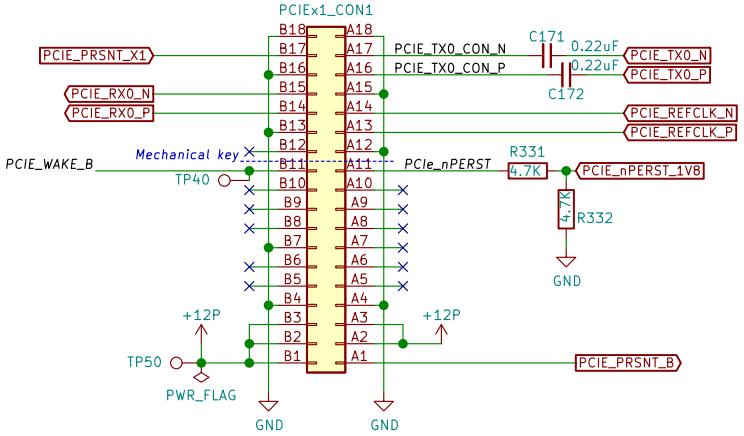


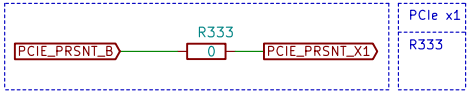
Only one pair of resistors assemblied per node.
Resistors ovelap one pad on top layer PCB for Middle point.
overlapped Resistor placed at 90 degree on top layer, . No stubs.
and via to bottom layer as short as possible to not break impedance.

Master Card	Slave Card	Lone Card.
R337-R339 R338-R340	R335-R336 R341-R342	All can be remove as FPGA_2 is last node.
R348-R350 R347-R349	R345-R346 R343-R344	



PCIe x1 Edge Connector





All hi-speed differential pairs signal follow PCB hi-speed design guideline.

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Sheet: /PCIe_&_Hi-Speed/
File: PCIe_&_Hi-Speed.sch

Title:

Size: A4	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 13/25

Sheet: Mezzanine_1

File: Mezzanine.sch

Connectors For FPGA_1

Connectors For FPGA_2

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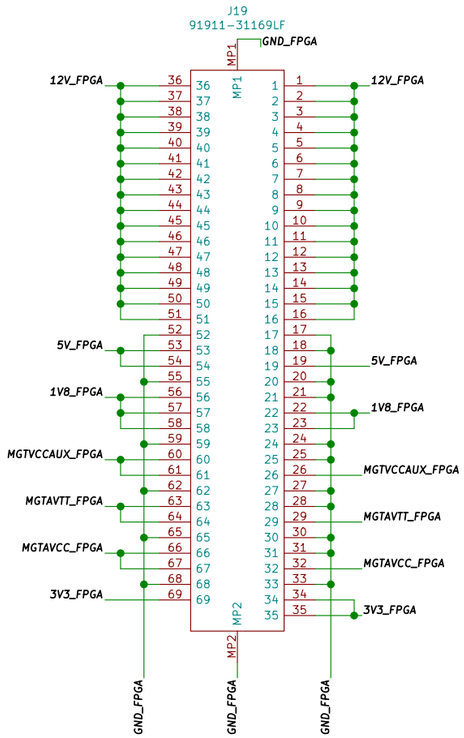
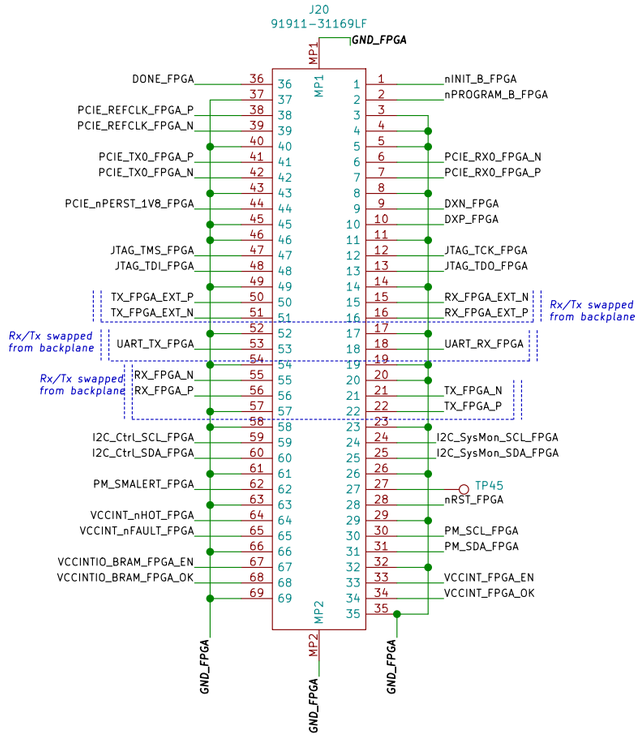
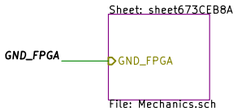
Sheet: /connectors_Mezzanine/
File: connectors_Mezzanine.sch

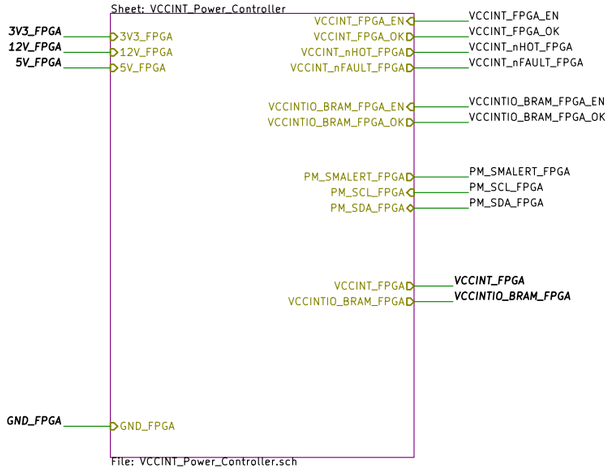
Title:

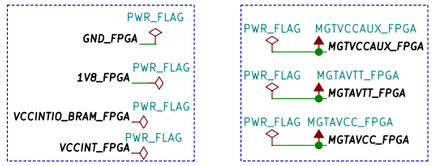
Size: A3	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 14/25

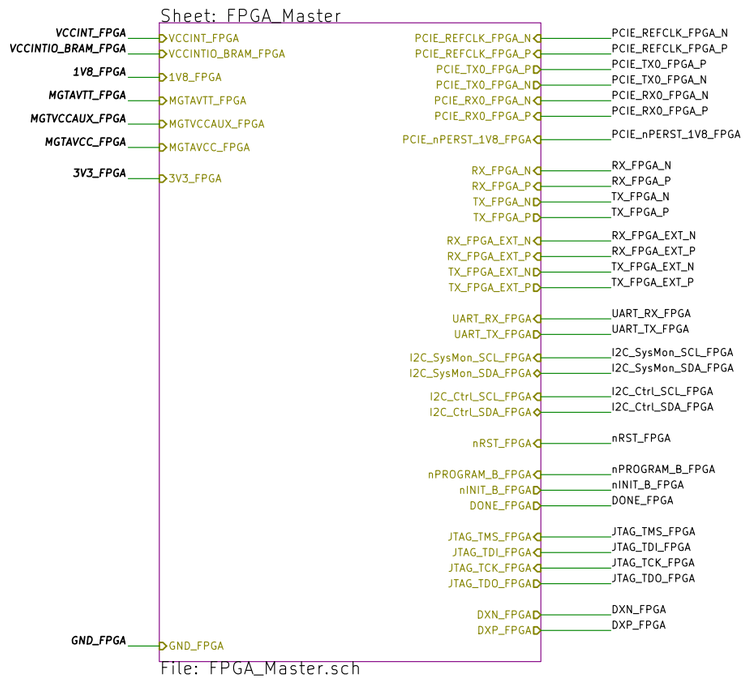












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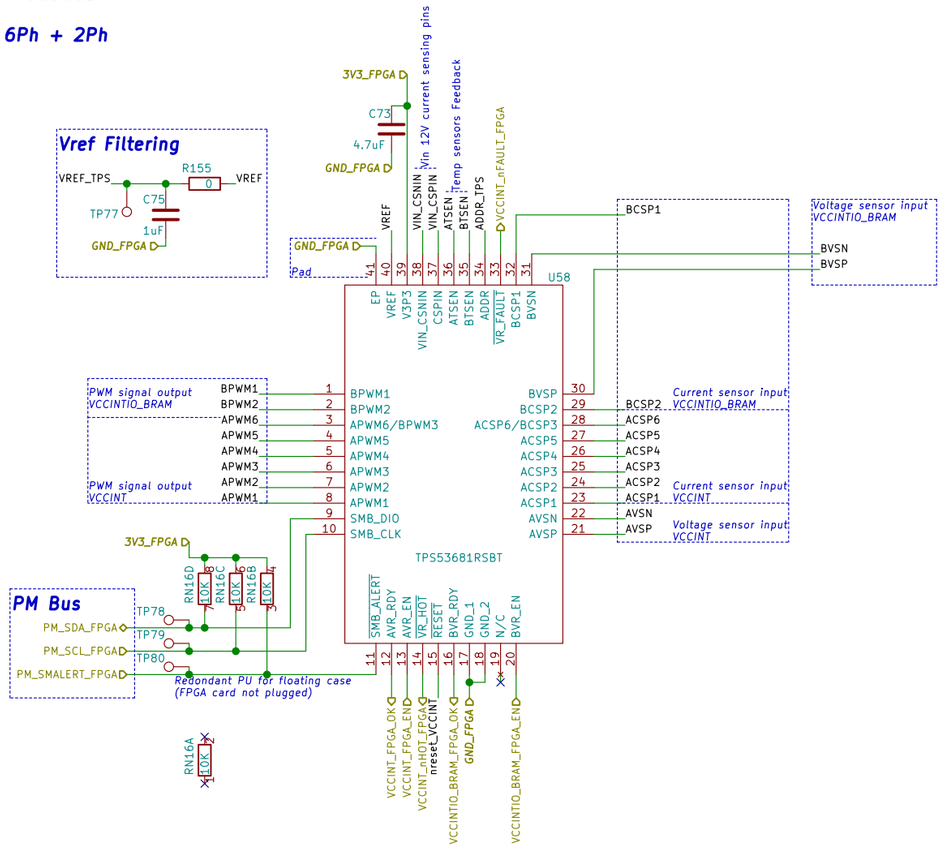
Sheet: /connectors_Mezzanine/Mezzanine_1/
File: Mezzanine.sch

Title:

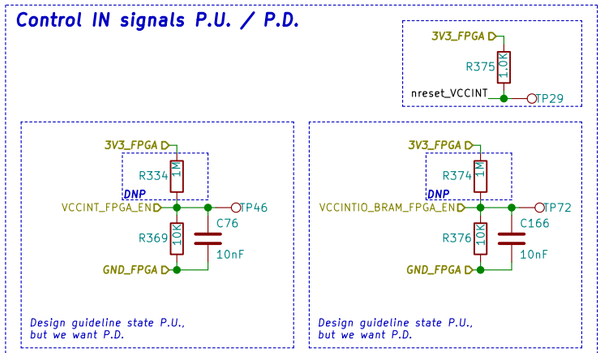
Size: A3	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 15/25

Power Controller
TPS53681

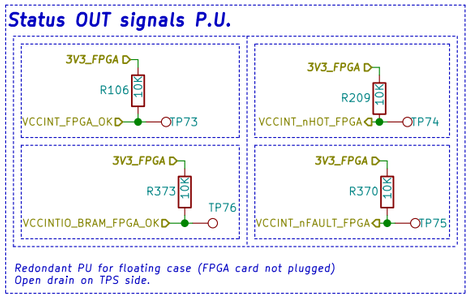
6Ph + 2Ph



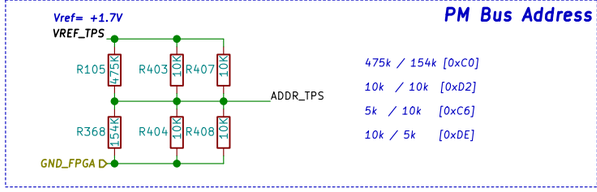
Control IN signals P.U. / P.D.



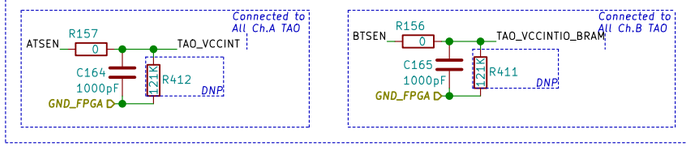
Status OUT signals P.U.



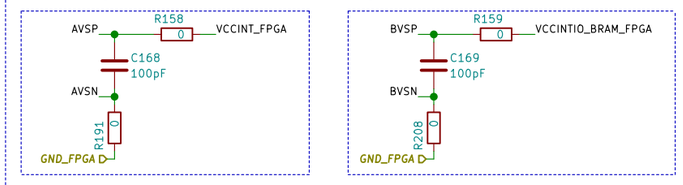
PM Bus Address



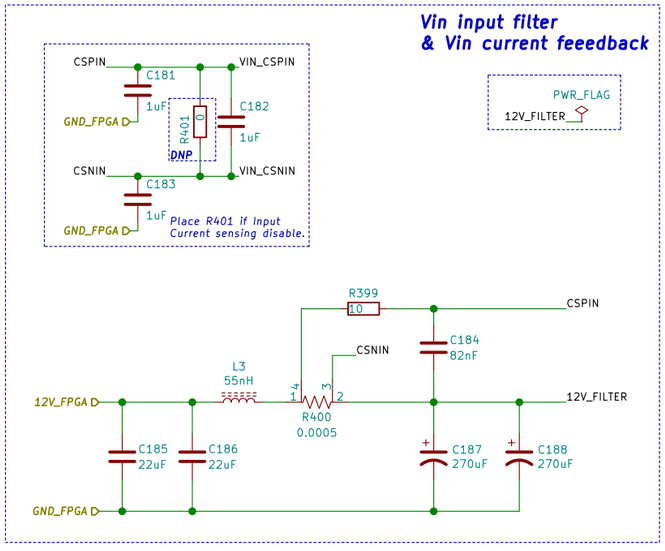
Temperature Feedback Filtering From PowerStages



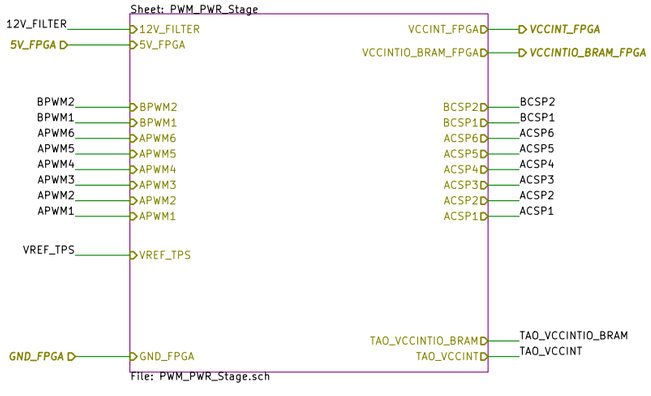
Diff. Voltage Feedback From PowerStages



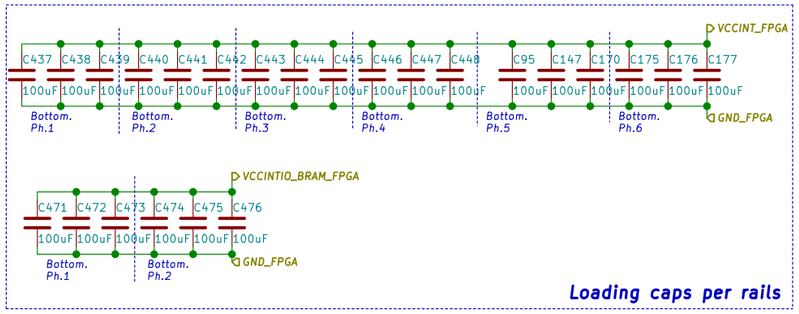
Vin input filter
& Vin current feeedback



Sub-Module for Powerstages



Loading caps per rails



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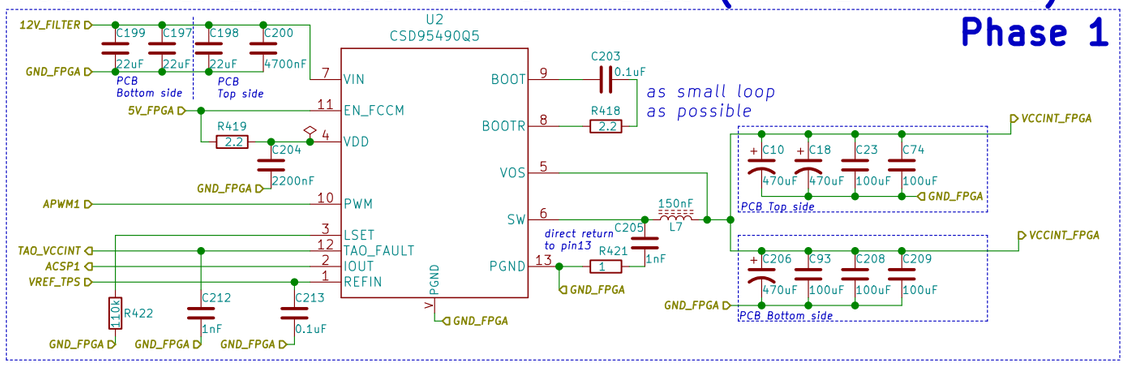
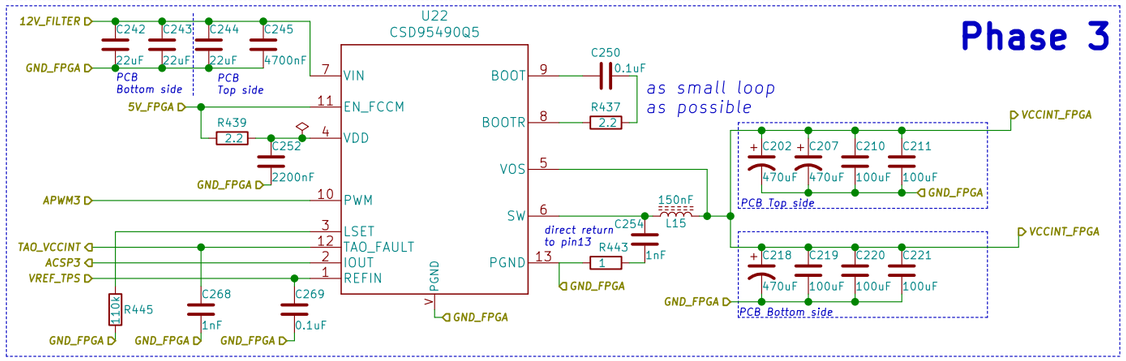
Sheet: /connectors_Mezzanine/Mezzanine_1/VCCINT_Power_Controller/
File: VCCINT_Power_Controller.sch

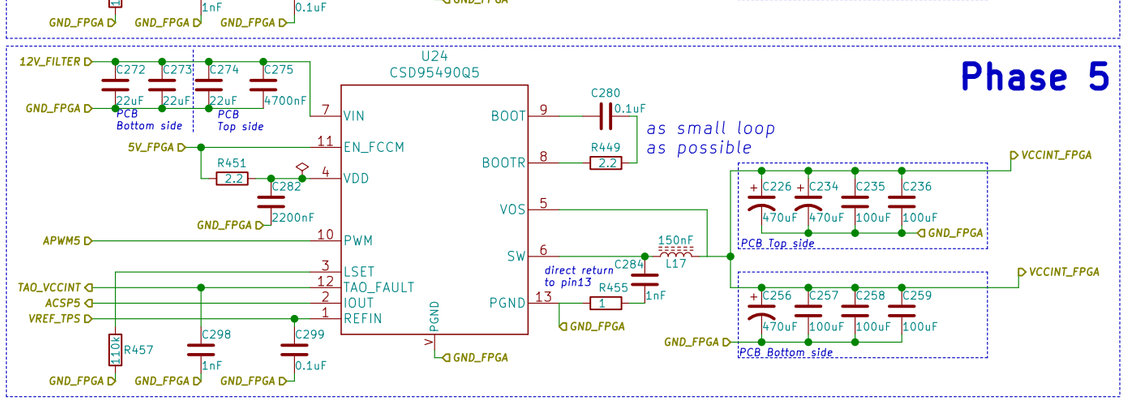
Title:

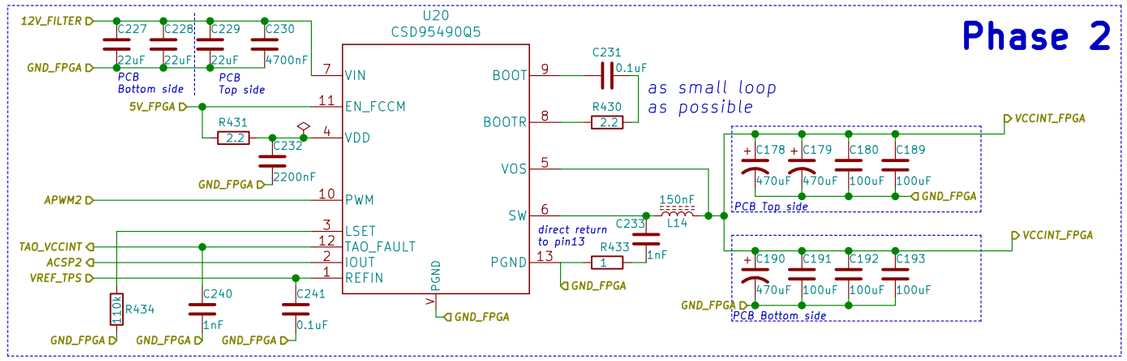
Size: A3	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 16/25

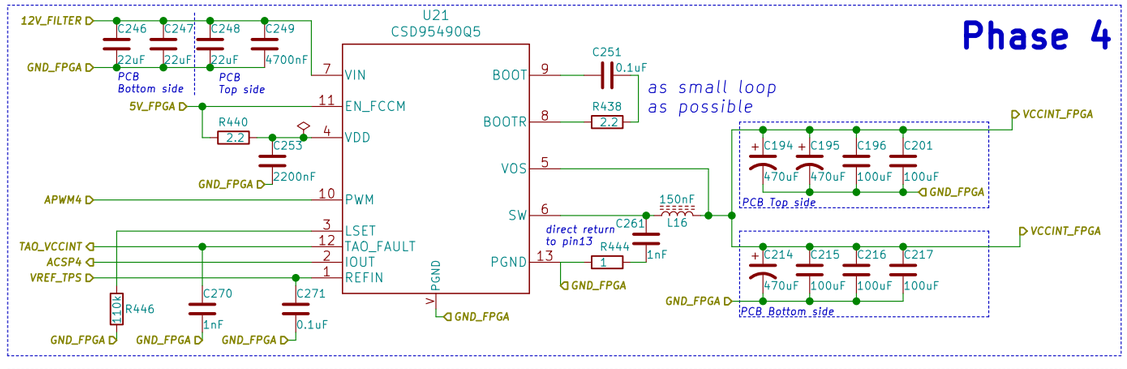
VCCINT Variable 0.85Vdc. 6-Phases (PWM 1 - PWM 6)

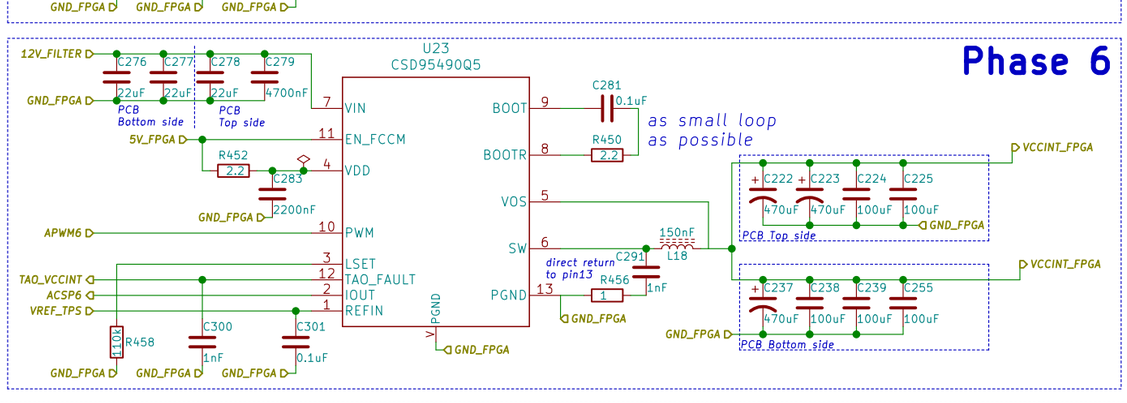




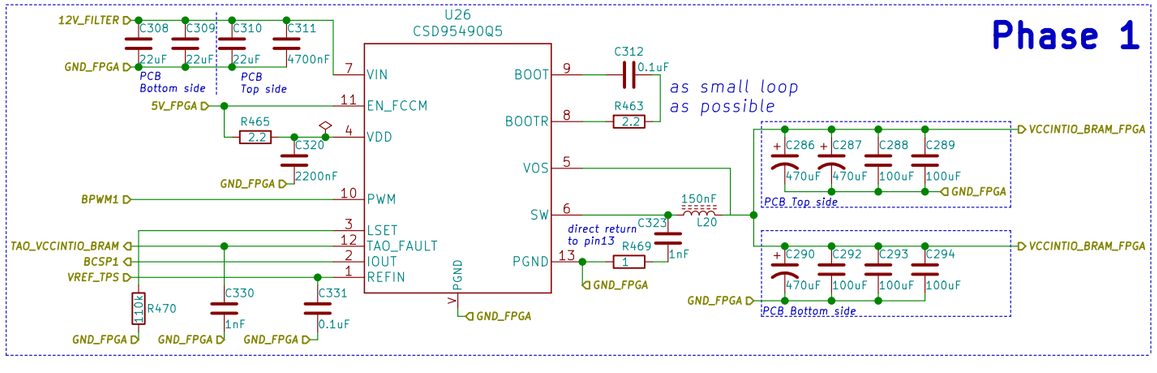


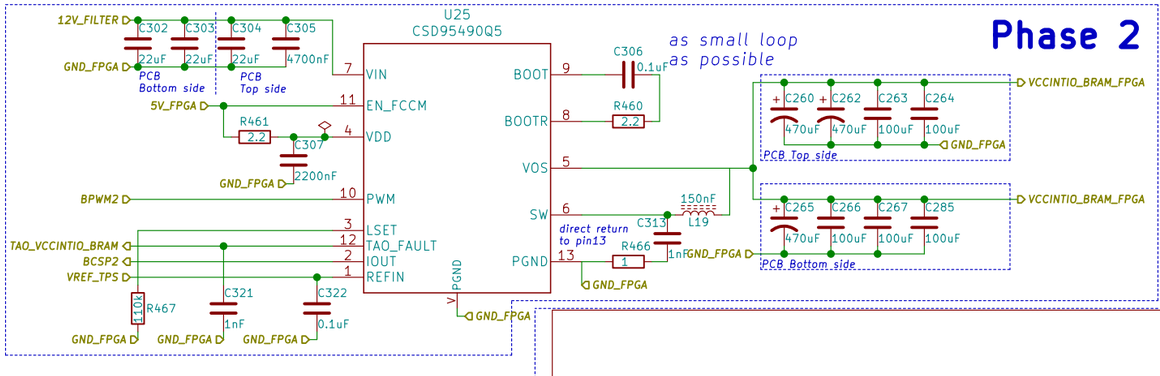






VCCINTIO_BRAM Fixed 0.8Vdc. 2-Phases (PWM 7 - PWM 8)





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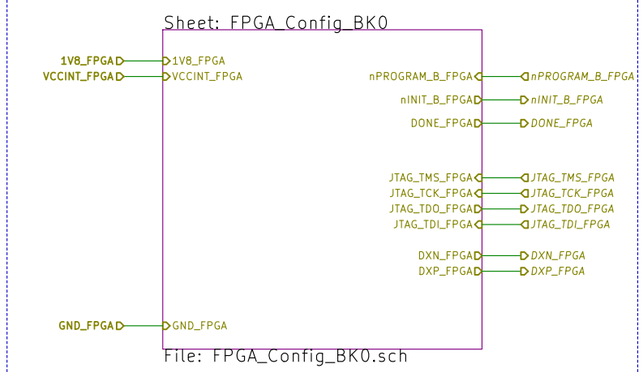
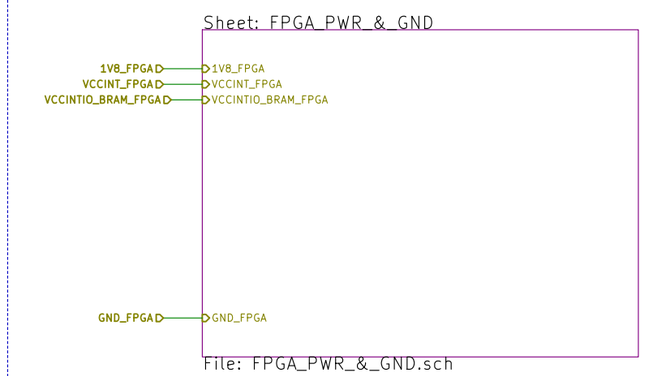
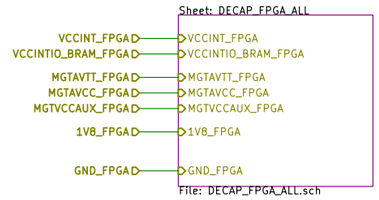
Sheet: /connectors_Mezzanine/Mezzanine_1/VCCINT_Power_Controller/PWM_PWR_Stage/
File: PWM_PWR_Stage.sch

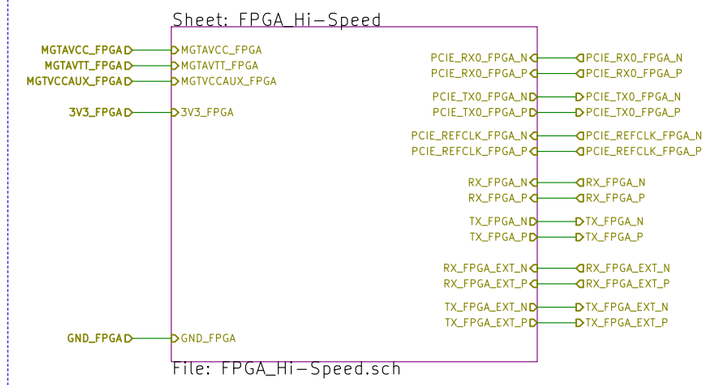
Title:

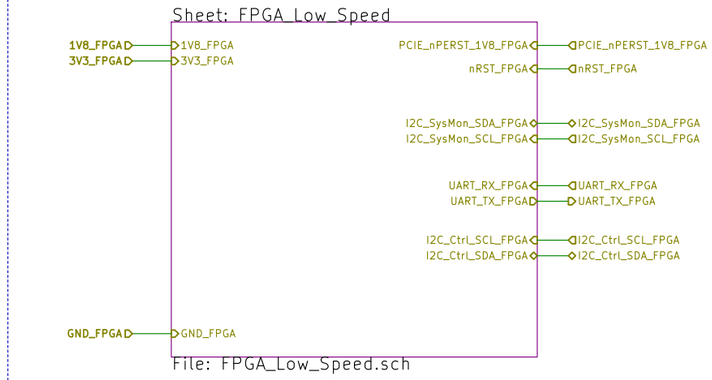
Size: A3	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 17/25

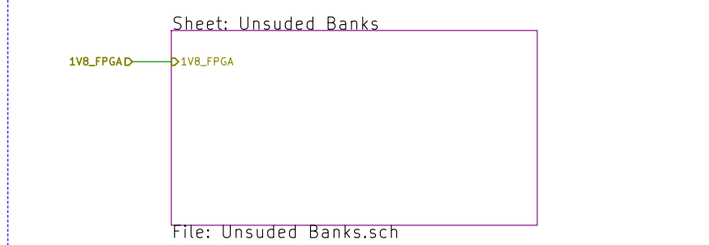












BLOCK DIAGRAM ONLY.

FPGA TOP LEVEL.

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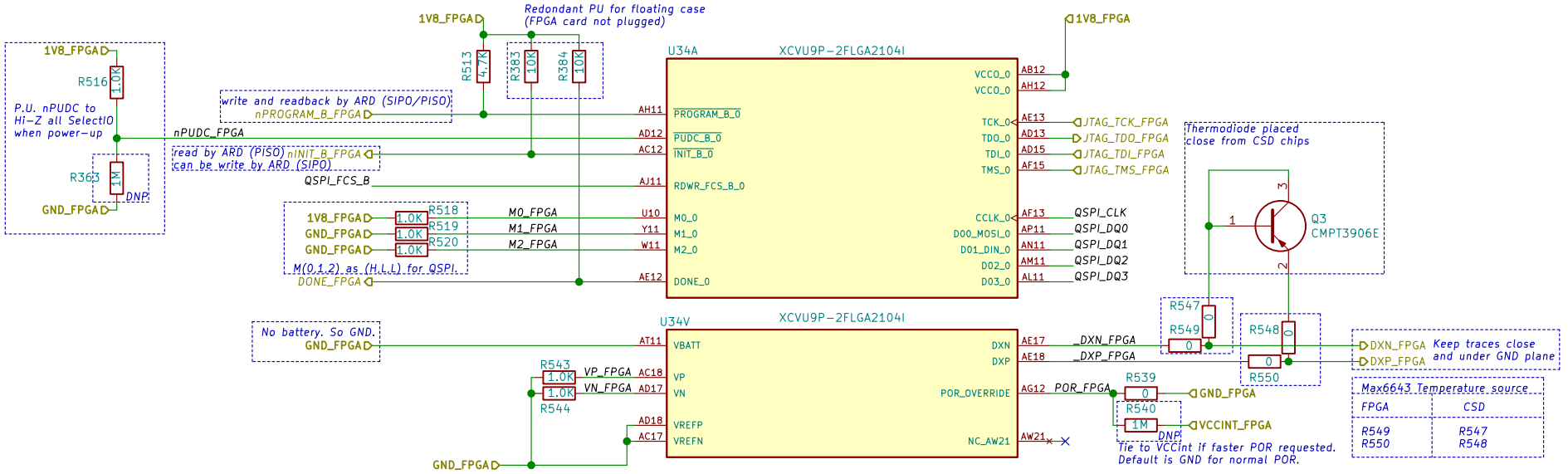
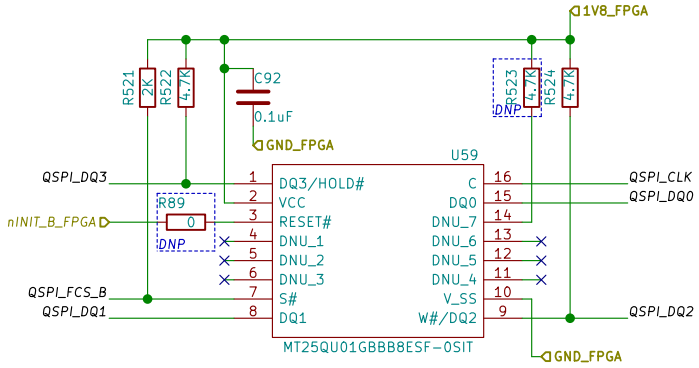
Sheet: /connectors_Mezzanine/Mezzanine_1/FPGA_Master/
File: FPGA_Master.sch

Title:

Size: A3	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 18/25





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Sheet: /connectors_Mezzanine/Mezzanine_1/FPGA_Master/FPGA_Config_BK0/
File: FPGA_Config_BK0.sch

Title:

Size: A4	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 19/25

U34B
XCVU9P-2FLGA2104I

VCCINT_FPGAD
1V8_FPGAD
VCCINTIO_BRAM_FPGAD
PWR_FLAG
sysmon_VCC
600R/0.5A
L28
L29
C500
0.47uF
C295
0.1uF
under BGA
AGND_plane
AGND_FPGA
GND_FPGAD
single point return to GND
SysMon and filtered Analog area.

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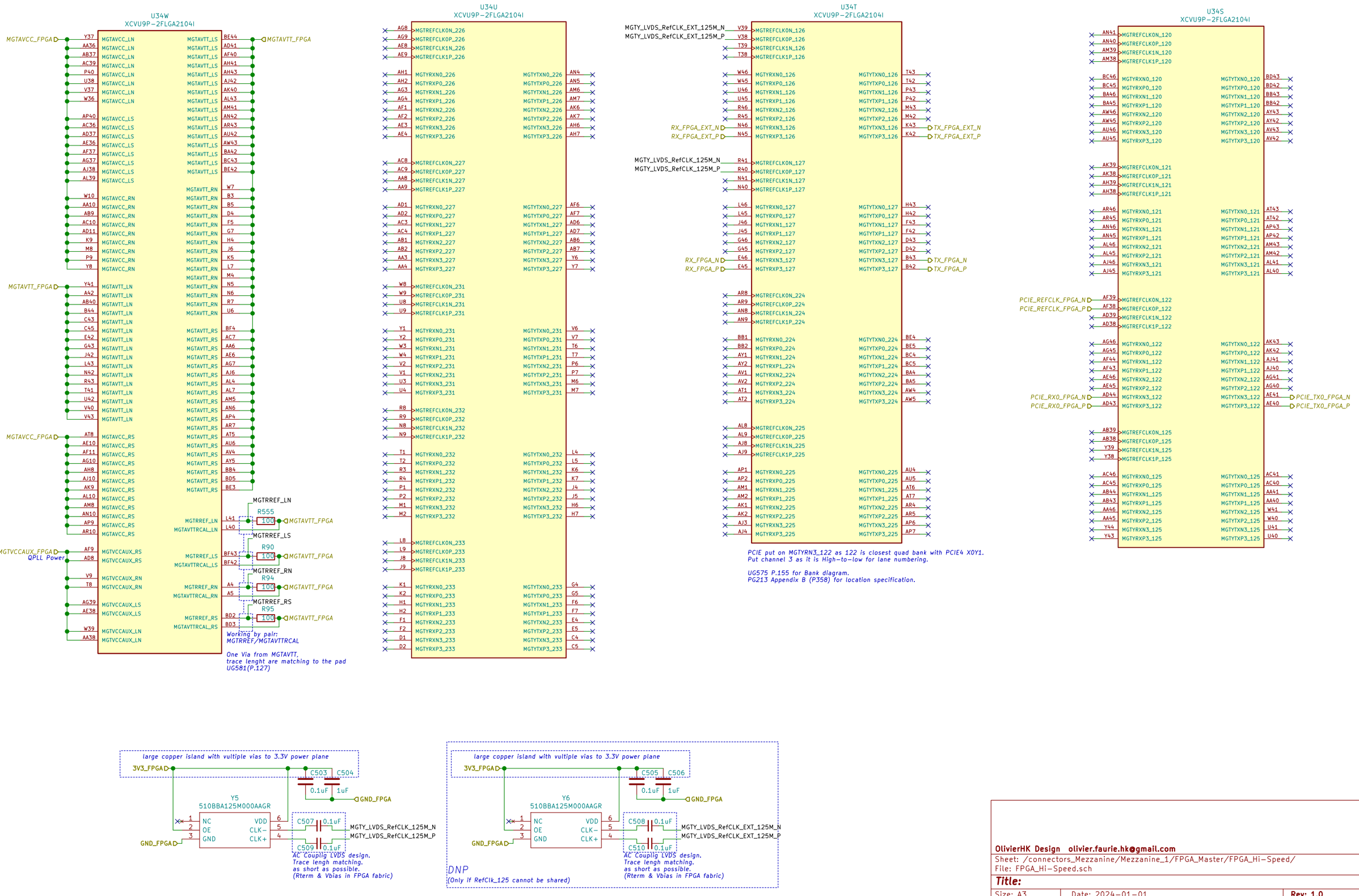
Sheet: /connectors_Mezzanine/Mezzanine_1/FPGA_Master/FPGA_PWR_&_GND/	
File: FPGA_PWR_&_GND.sch	
Title:	
Size: A3	Date: 2024-01-01
KiCad E.D.A. kicad (5.1.10)-1	Id: 20/25

Rev: 1.0



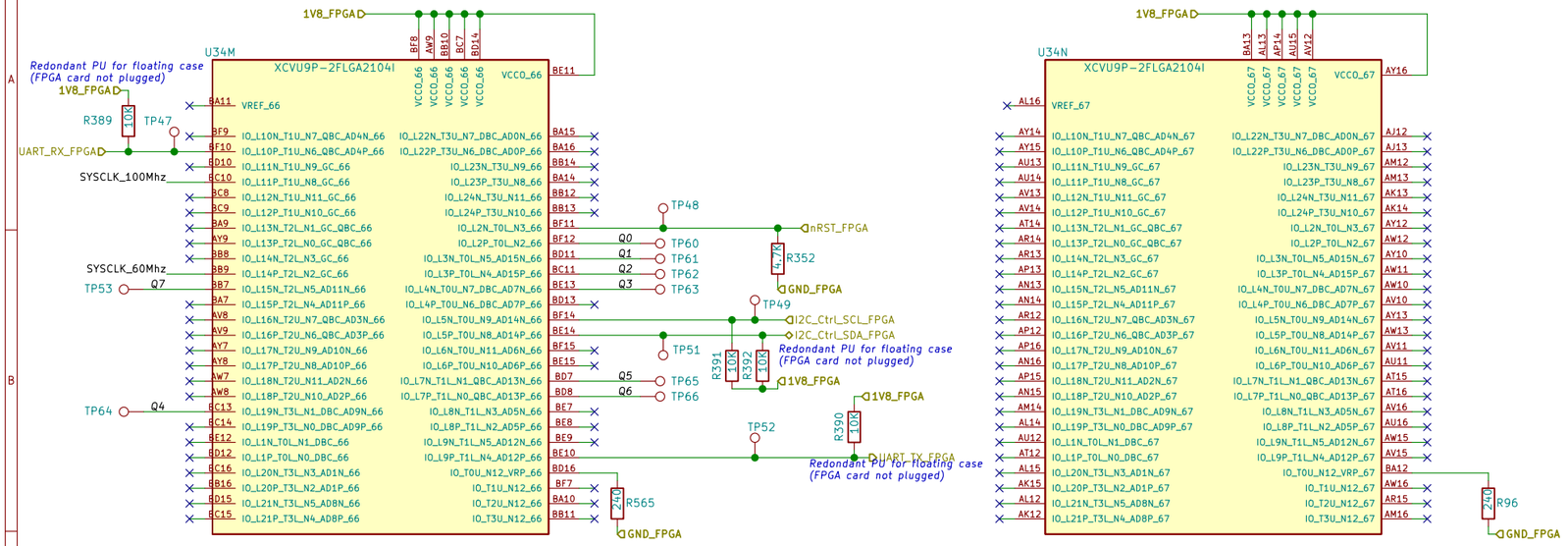
OlivierHK Design olivier.faurie.hk@gmail.com

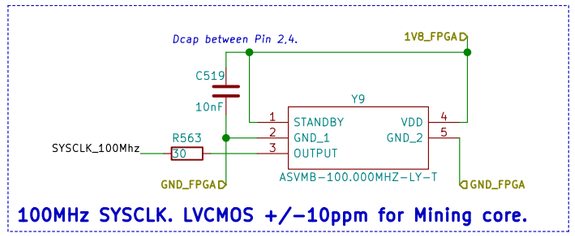
Sheet: /connectors_Mezzanine/Mezzanine_1/FPGA_Master/FPGA_Hi-Speed/
File: FPGA_Hi-Speed.sch

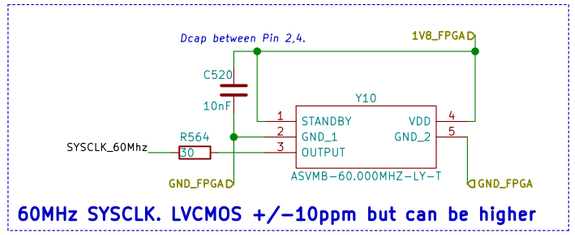
Title:

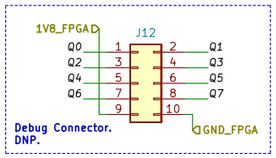
Size: A3	Date: 2024-01-01	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.10)-1		Id: 21/25

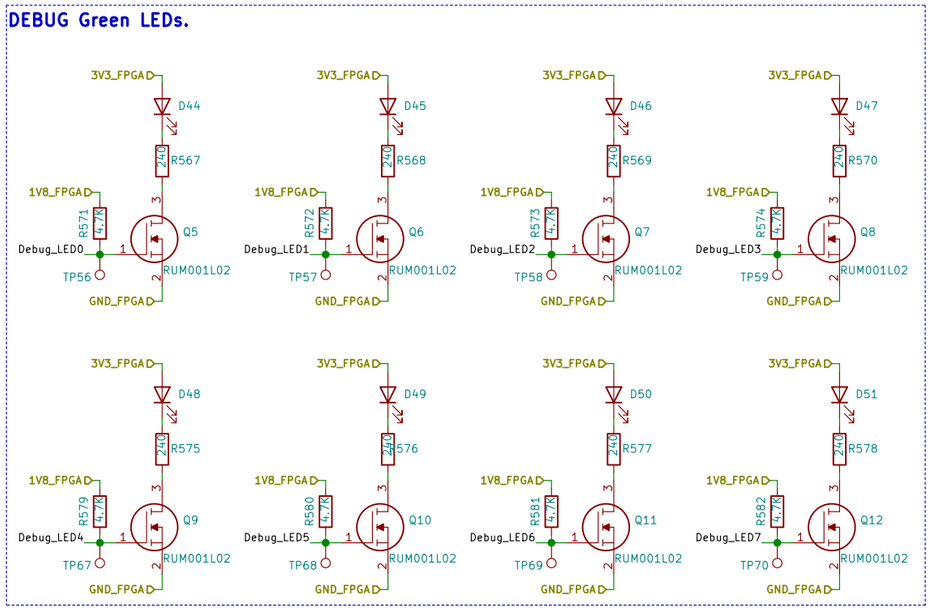
Vref floating. as we use LVCMOS standards level. Vr tied to ground via 240 Ohm resistance, following design example.

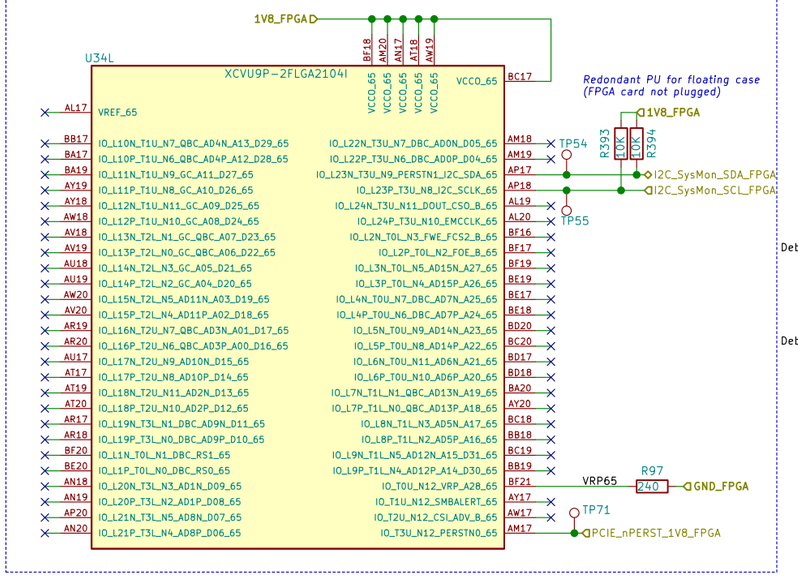


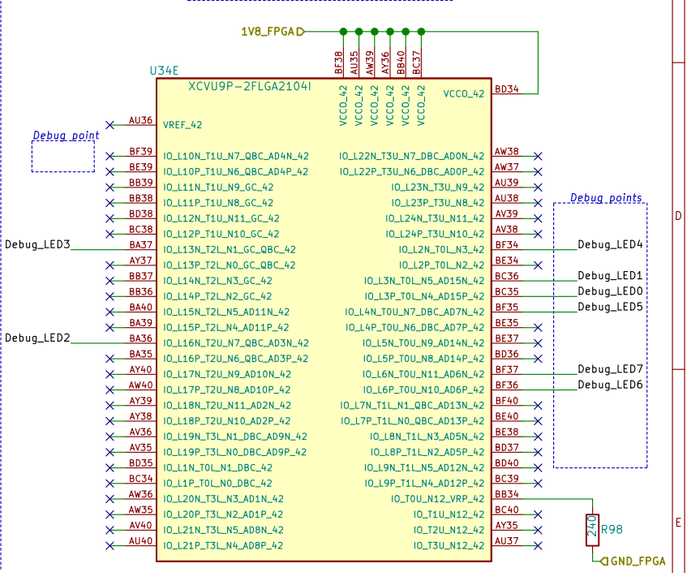












OlivierHK Design olivier.faurie.hk@gmail.com

Sheet: /connectors_Mezzanine/Mezzanine_1/FPGA_Master/FPGA_Low_Speed/
File: FPGA_Low_Speed.sch

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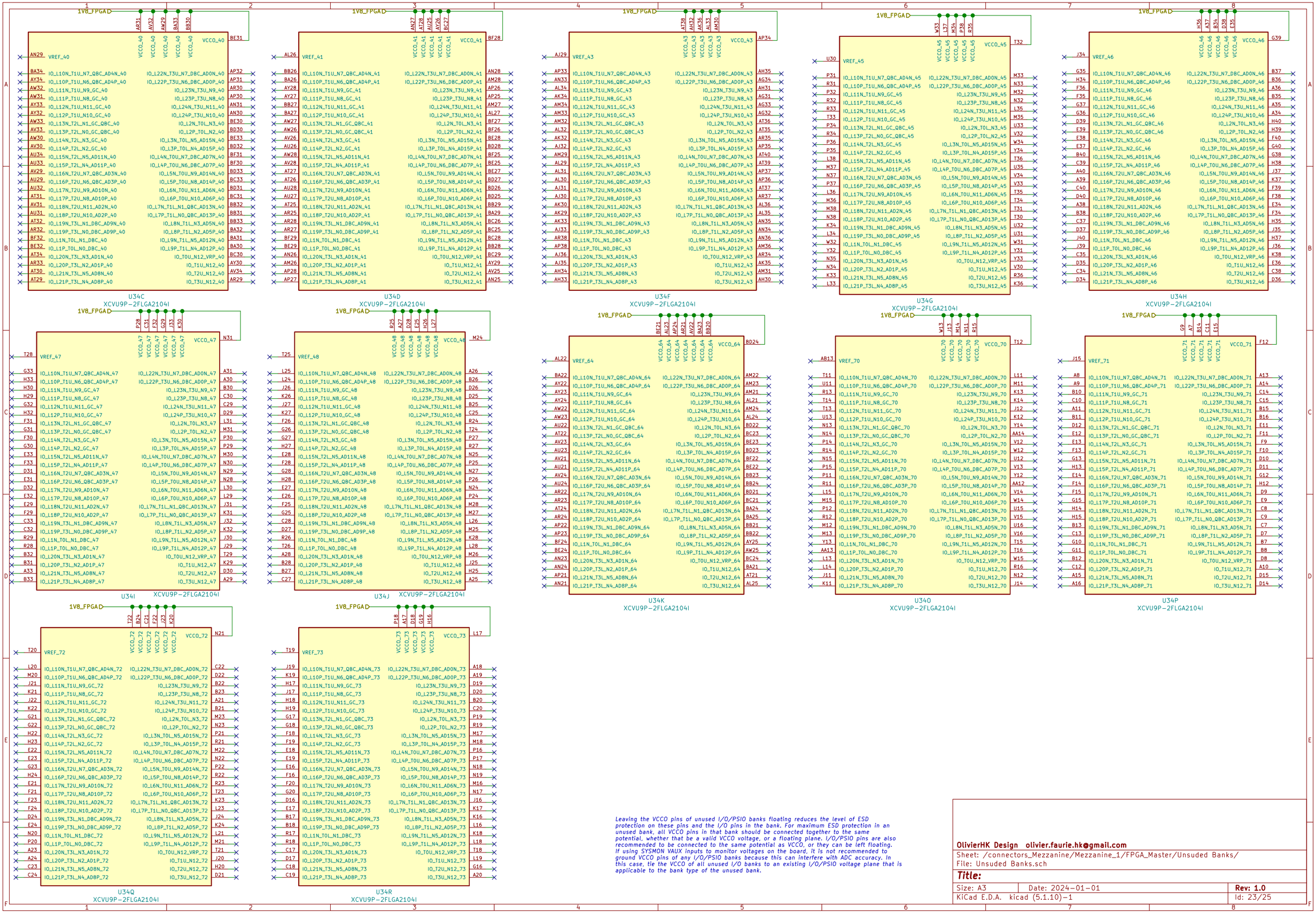
KiCad E.D.A. kicad (5.1.10)-1		Id: 22/25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IO_L15P_T2L_N4_AD11P_48
IO_L16N_T2U_N7_QBC_AD3N_48
IO_L16P_T2U_N6_QBC_AD3P_48
IO_L17N_T2U_N9_AD10N_48
IO_L17P_T2U_N8_AD10P_48
IO_L18N_T2U_N11_AD2N_48
IO_L18P_T2U_N10_AD2P_48
IO_L19N_T3L_N1_DBC_AD9N_48
IO_L19P_T3L_N0_DBC_AD9P_48
IO_L1N_T0L_N1_DBC_48
IO_L1P_T0L_N0_DBC_48
IO_L20N_T3L_N3_AD1N_48
IO_L20P_T3L_N2_AD1P_48
IO_L21N_T3L_N5_AD8N_48
IO_L21P_T3L_N4_AD8P_48
IO_L22N_T3U_N7_DBC_AD0N_48
IO_L22P_T3U_N6_DBC_AD0P_48
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IO_L23P_T3U_N8_48
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IO_L2N_T0L_N3_48
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IO_L3P_T0L_N4_AD15P_48
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IO_L4P_T0U_N6_DBC_AD7P_48
IO_L5N_T0U_N9_AD14N_48
IO_L5P_T0U_N8_AD14P_48
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IO_L6P_T0U_N10_AD6P_48
IO_L7N_T1L_N1_QBC_AD13N_48
IO_L7P_T1L_N0_QBC_AD13P_48
IO_L8N_T1L_N3_AD5N_48
IO_L8P_T1L_N2_AD5P_48
IO_L9N_T1L_N5_AD12N_48
IO_L9P_T1L_N4_AD12P_48
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IO_T2U_N12_48
IO_T3U_N12_48
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IO_L11P_T1U_N8_GC_64
IO_L12N_T1U_N11_GC_64
IO_L12P_T1U_N10_GC_64
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IO_L15P_T2L_N4_AD11P_64
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IO_L16P_T2U_N6_QBC_AD3P_64
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IO_L24P_T3U_N10_64
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IO_L9P_T1L_N4_AD12P_64
IO_T0U_N12_VRP_64
IO_T1U_N12_64
IO_T2U_N12_64
IO_T3U_N12_64
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VREF_70
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VREF_71
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IO_L9P_T1L_N4_AD12P_71
IO_T0U_N12_VRP_71
IO_T1U_N12_71
IO_T2U_N12_71
IO_T3U_N12_71
Leaving the VCCO pins of unused I/O/PSIO banks floating reduces the level of ESD protection on these pins and the I/O pins in the bank. For maximum ESD protection in an unused bank, all VCCO pins in that bank should be connected together to the same potential, whether that be a valid VCCO voltage, or a floating plane. I/O/PSIO pins are also recommended to be connected to the same potential as VCCO, or they can be left floating. If using SYSMON VAUX inputs to monitor voltages on the board, it is not recommended to ground VCCO pins of any I/O/PSIO banks because this can interfere with ADC accuracy. In this case, tie the VCCO of all unused I/O banks to an existing I/O/PSIO voltage plane that is applicable to the bank type of the unused bank.
OlivierHK Design olivier.faurie.hk@gmail.com
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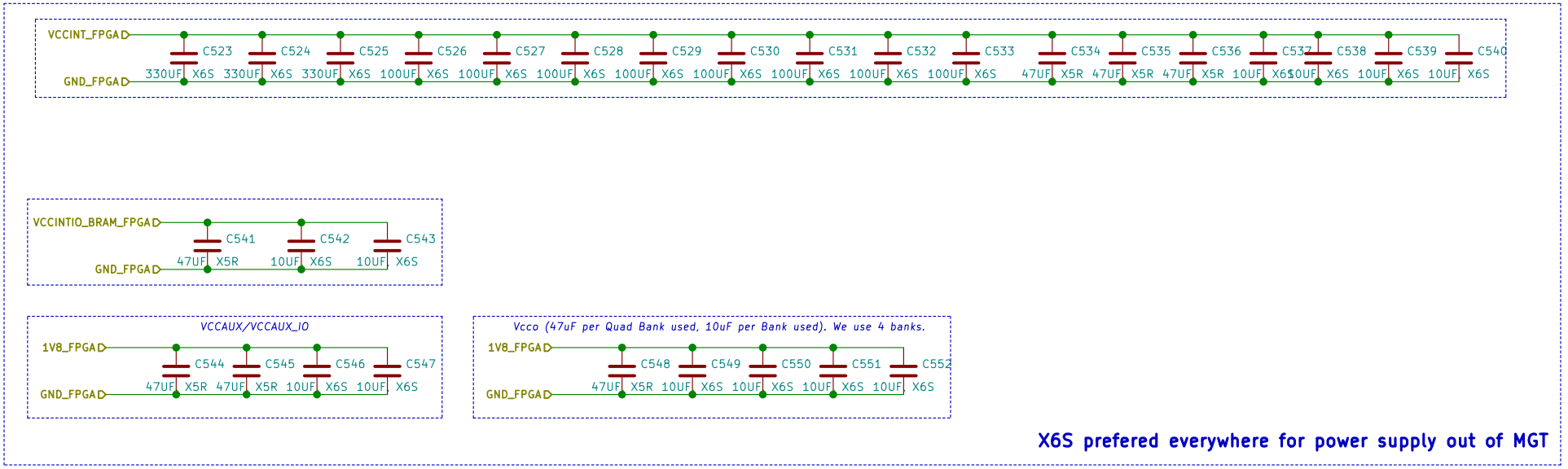
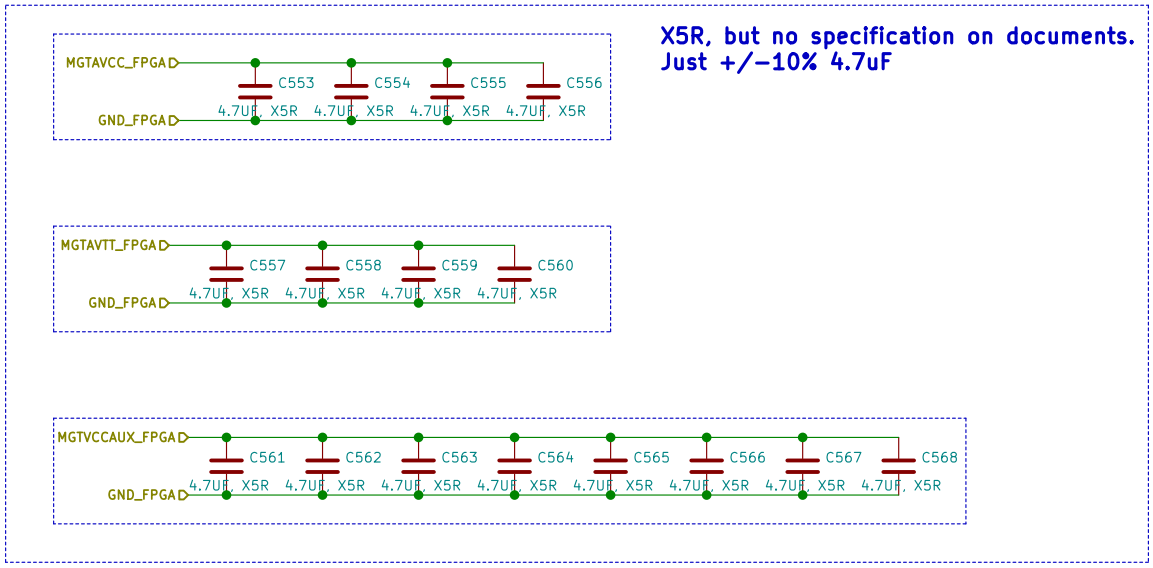
Date: 2024-01-01
Rev: 1.0
KiCad E.D.A. kicad (5.1.10)-1
Id: 23/25





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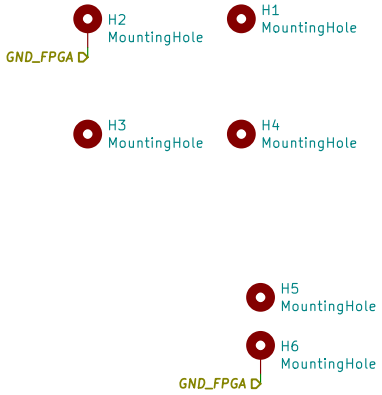

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