

BLOCK DIAGRAM ONLY.

PROJECT SCHEMATIC TOP LEVEL.

A

A

B

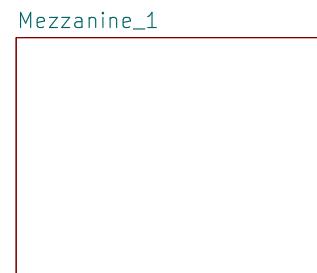
B

C

C

D

D



O.F. Design olivier.faurie.hk@gmail.com

Sheet: /

File: Alto-Ultra+.kicad\_sch

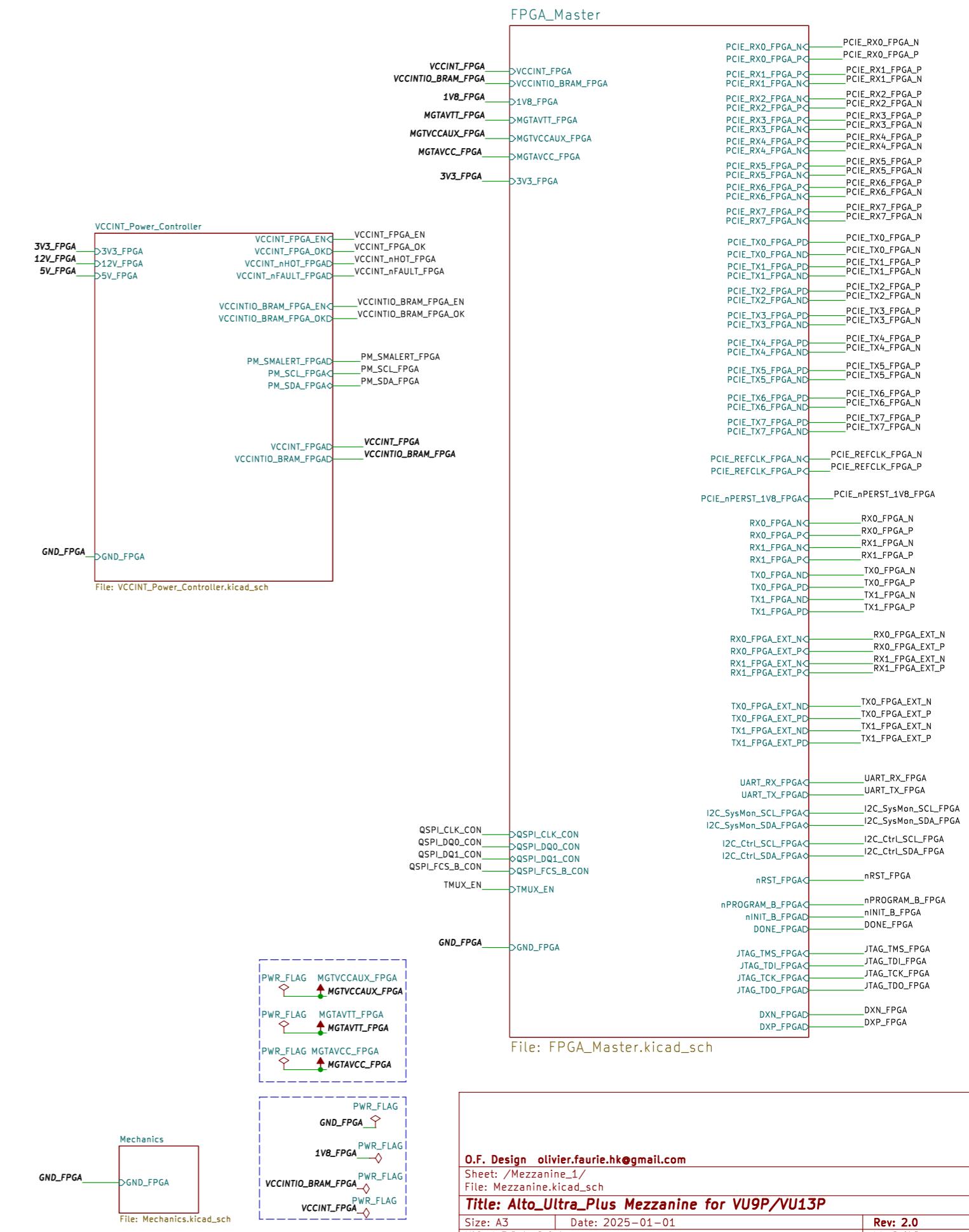
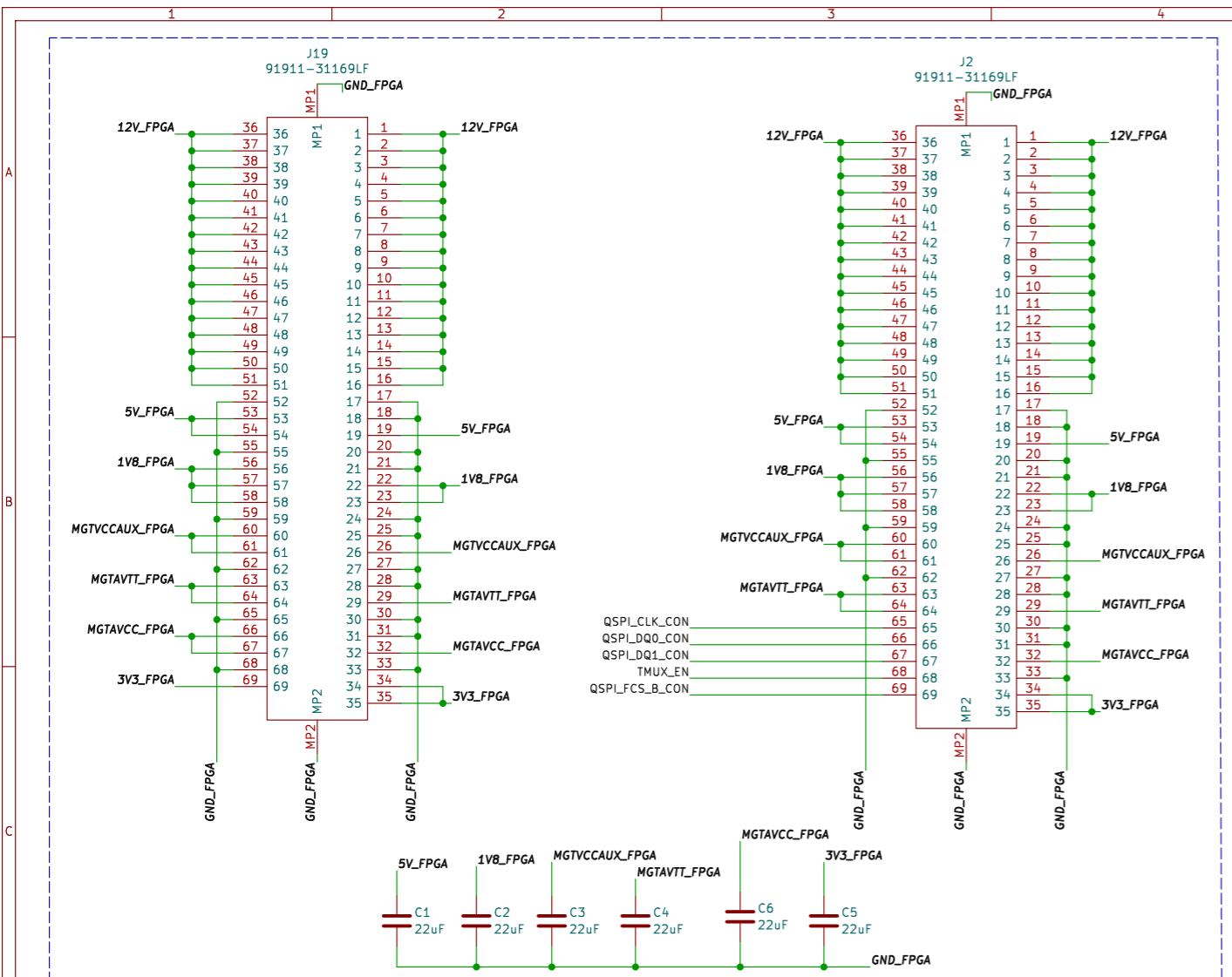
**Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P**

Size: USLetter Date: 2025-01-01

KiCad E.D.A. 8.0.1

**Rev: 2.0**

Id: 1/12



1 2 3 4 5 6

A

A

B

B

C

C

D

D



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Sheet: /Mezzanine\_1/Mechanics/

File: Mechanics.kicad\_sch

**Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P**

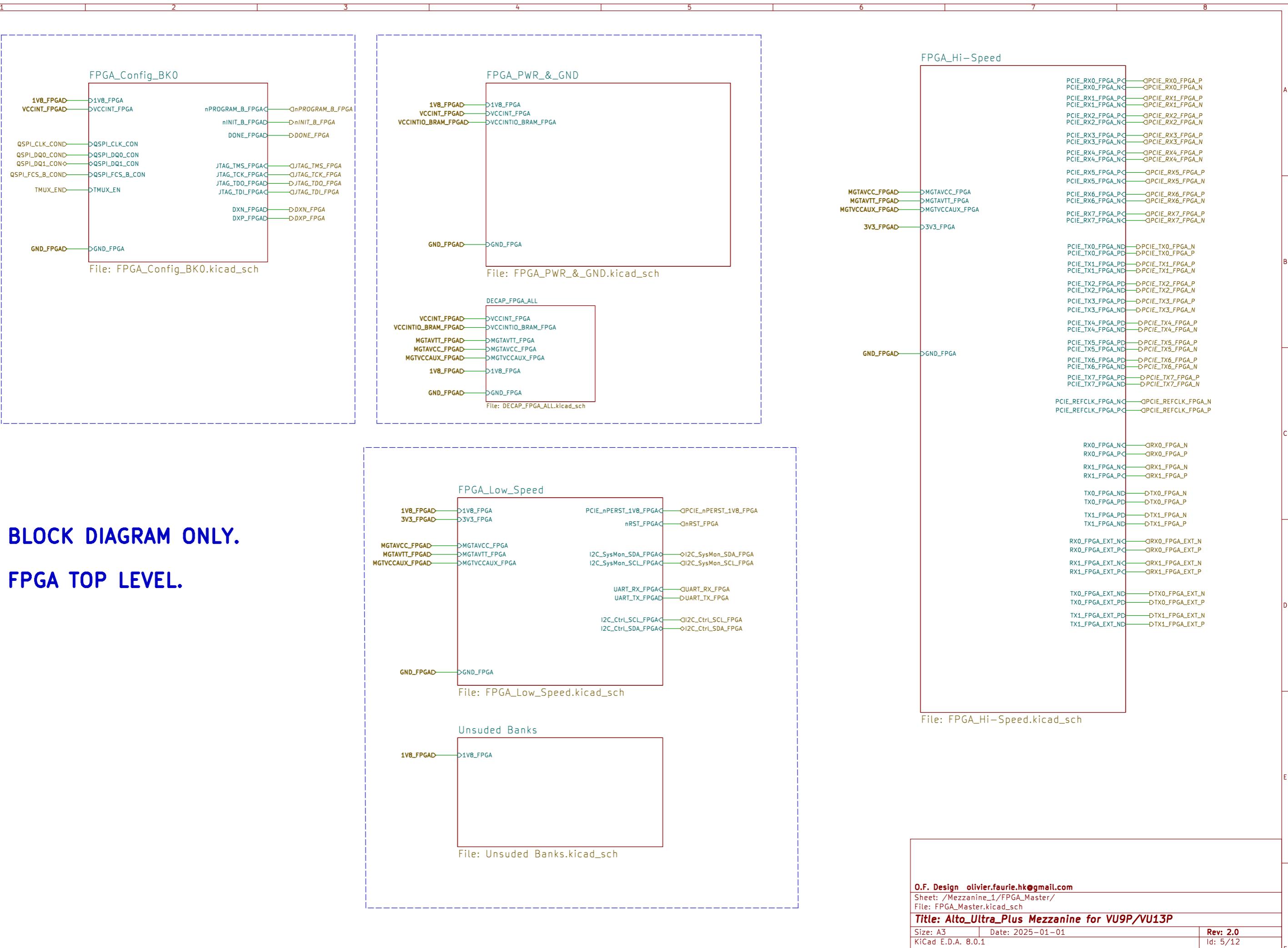
Size: A4 Date: 2025-01-01

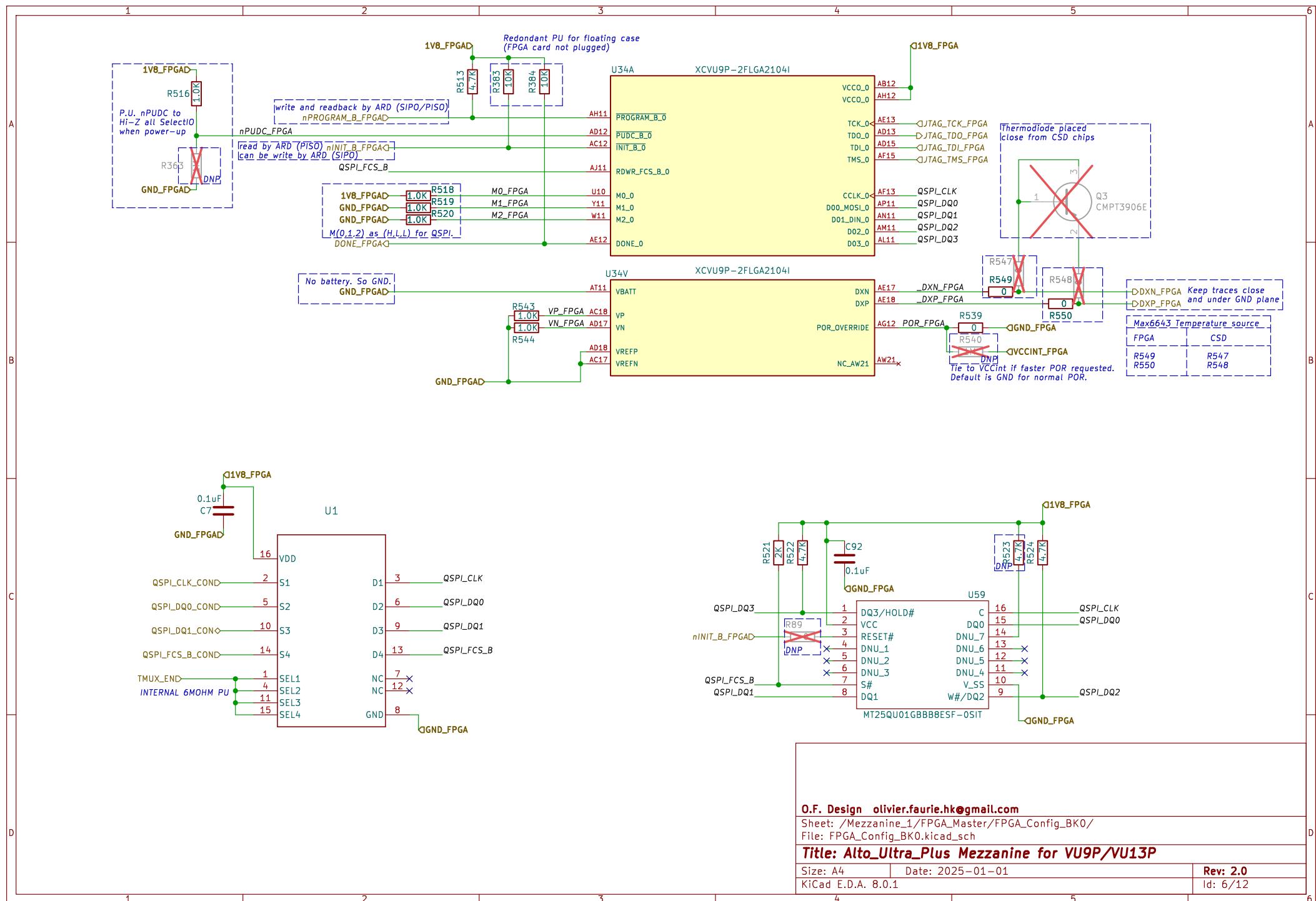
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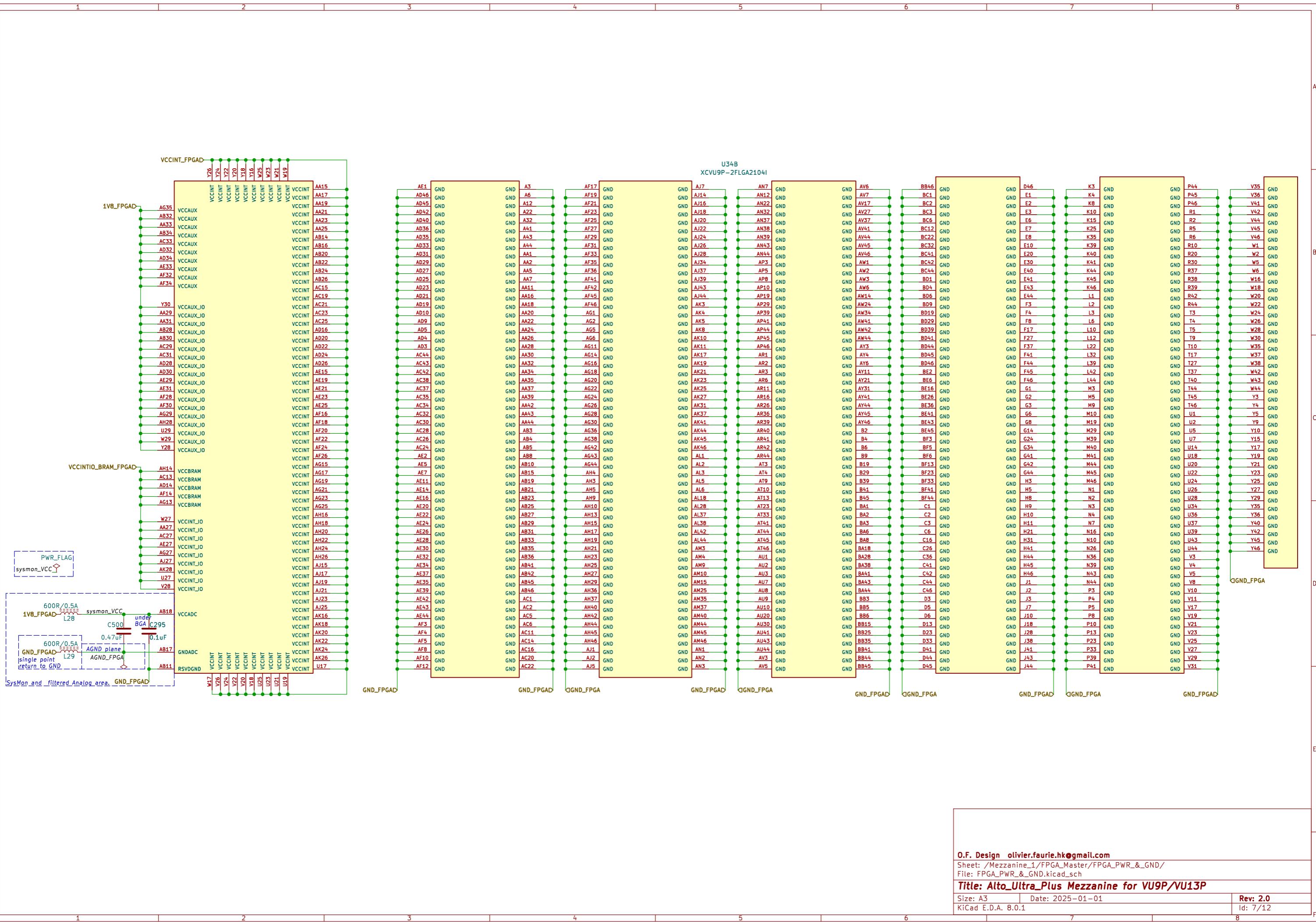
**Rev: 2.0**

Id: 3/12

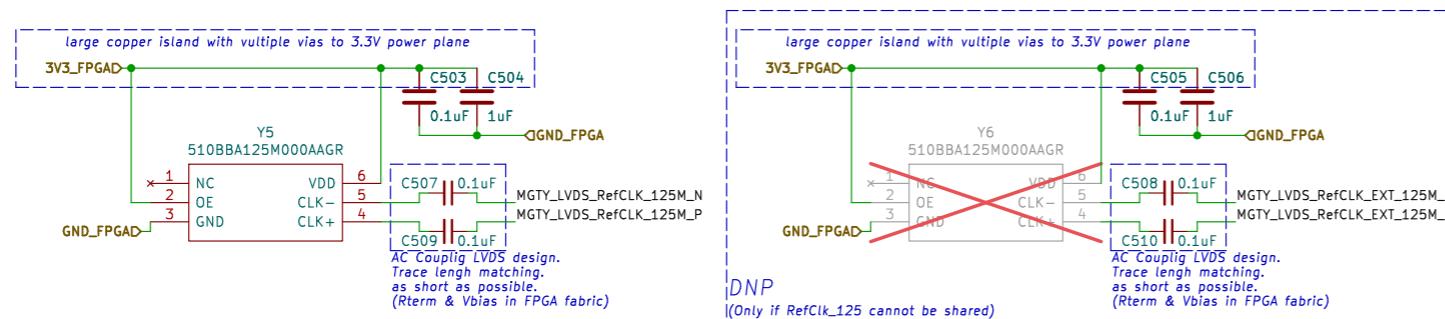
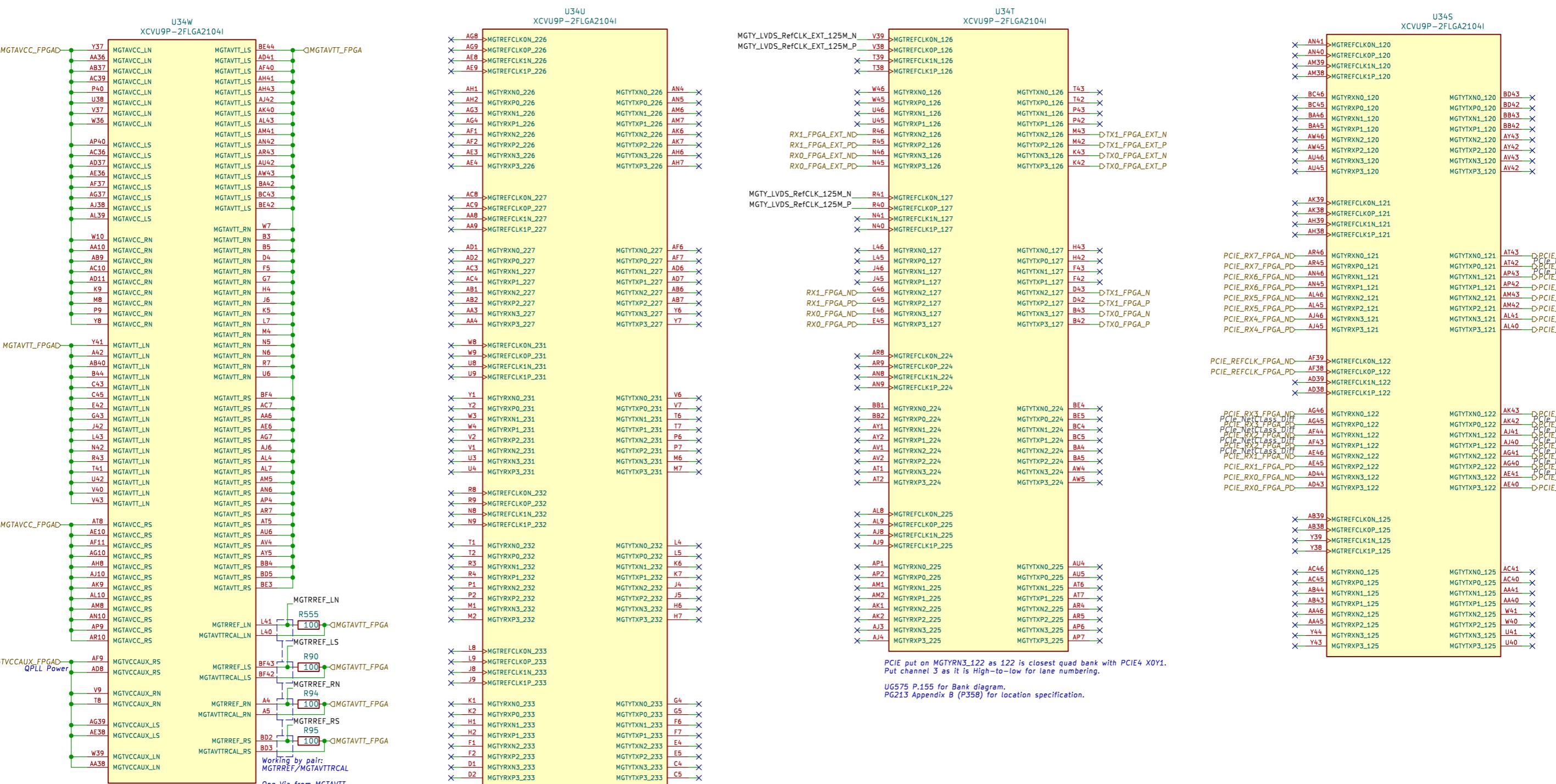
1 2 3 4 5 6







1 2 3 4 5 6 7 8



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Sheet: /Mezzanine\_1/FPGA\_Master/FPGA\_Hi-Speed/  
File: FPGA\_Hi-Speed.kicad\_sch

Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P

Size: A3 Date: 2025-01-01  
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Rev: 2.0  
Id: 8/12



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Sheet: /Mezzanine\_1/FPGA\_Master/DECAP\_FPGA\_ALL/

File: DECAP\_FPGA\_ALL.kicad\_sch

**Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P**

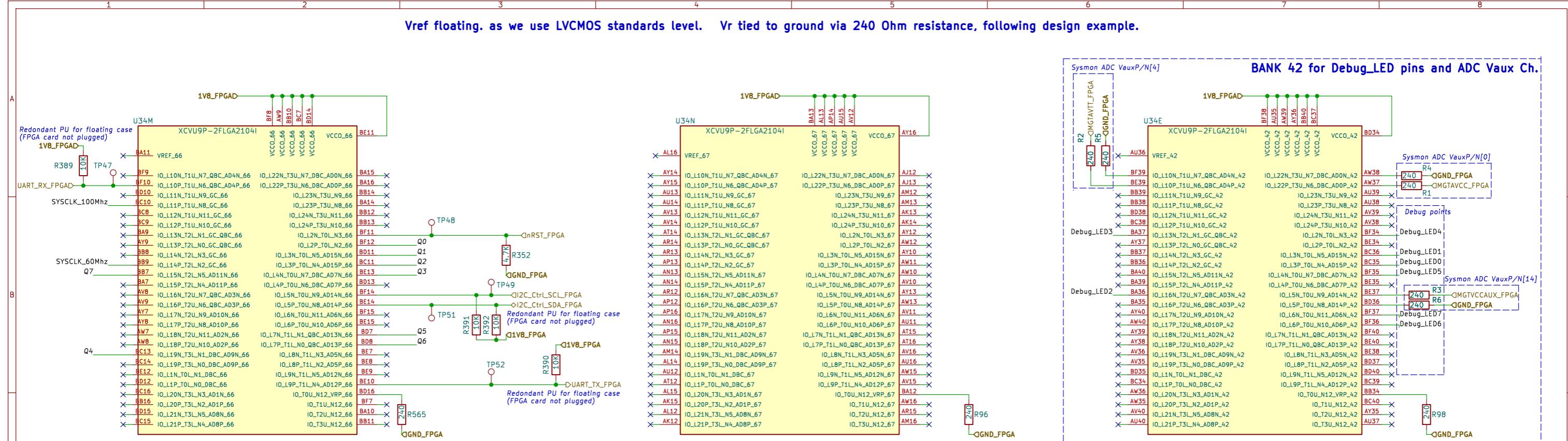
Size: A4 Date: 2025-01-01

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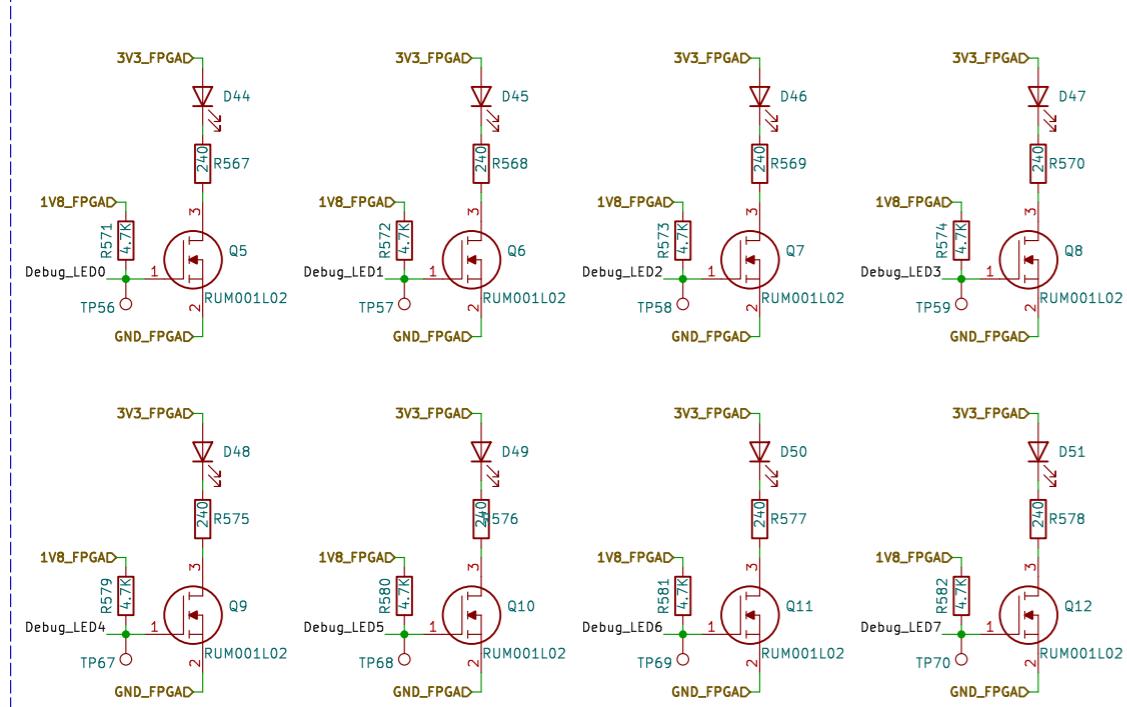
**Rev: 2.0**

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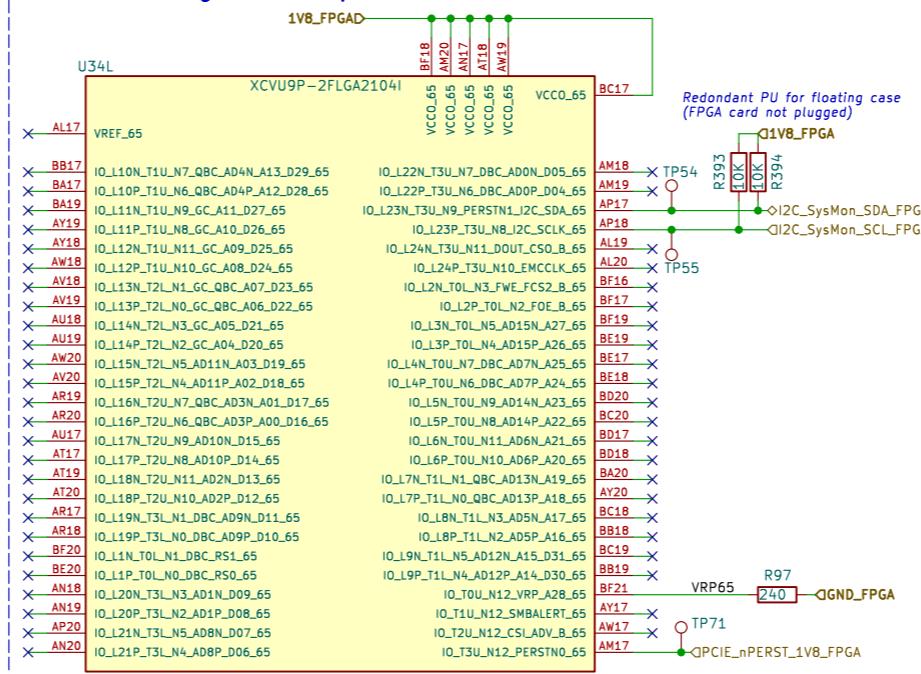
Vref floating, as we use LVCMS standards level. Vr tied to ground via 240 Ohm resistance, following design example.



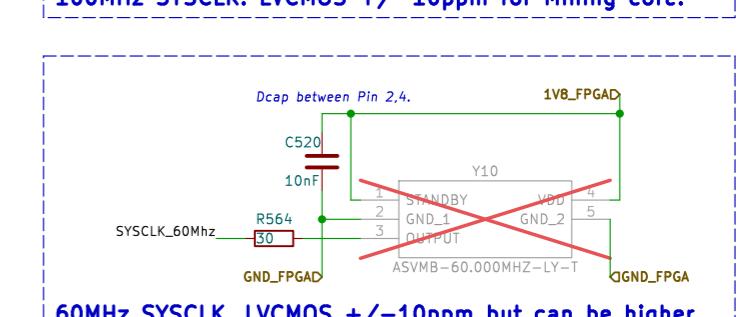
### DEBUG Green LEDs.



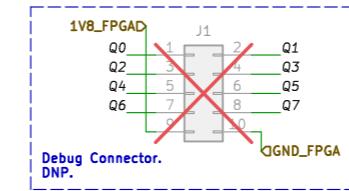
### BANK 65 for Cfg and hard pins.



### 100MHz SYCLK. LVCMS +/-10ppm for Mining core.



### 60MHz SYCLK. LVCMS +/-10ppm but can be higher



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Sheet: /Mezzanine\_1/FPGA\_Master/FPGA\_Low\_Speed/

File: FPGA\_Low\_Speed.kicad\_sch

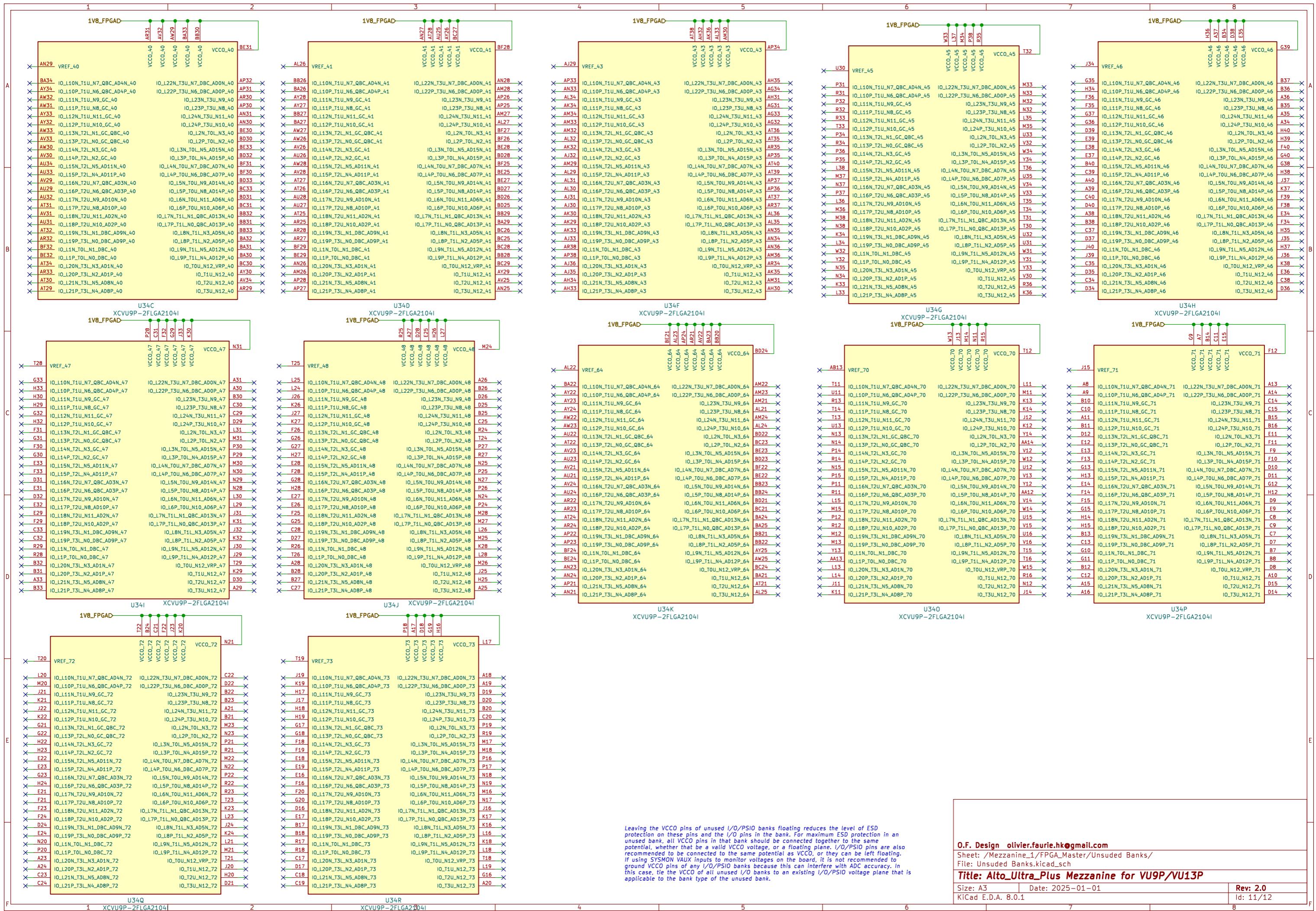
Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P

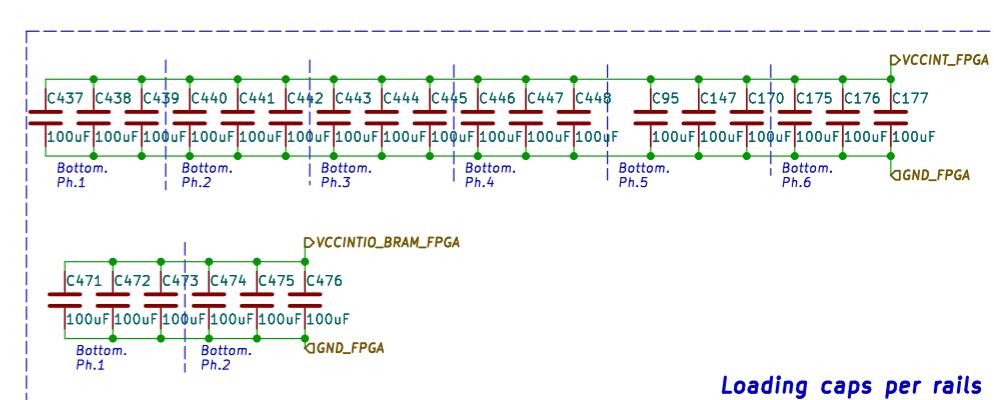
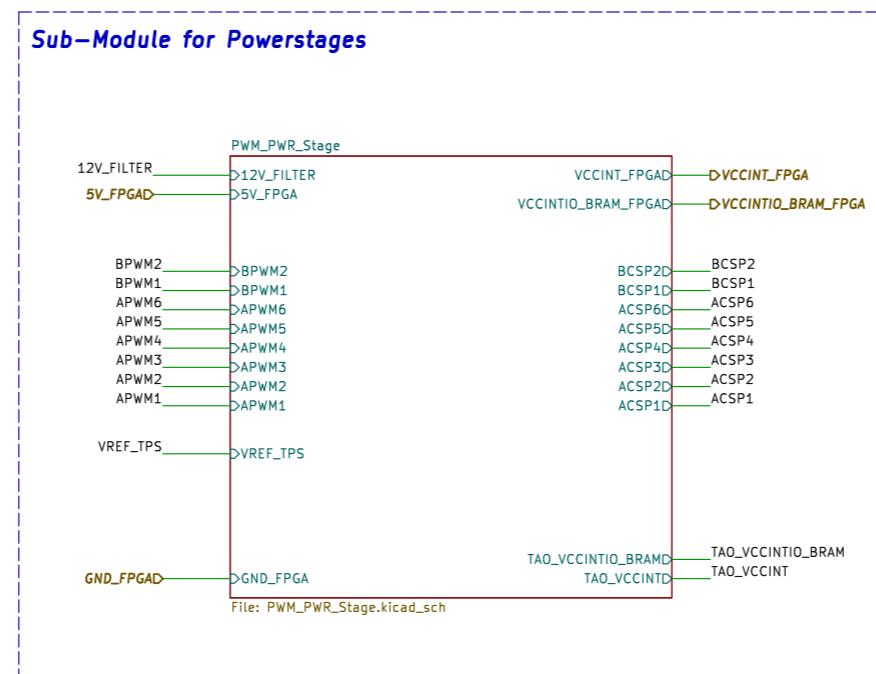
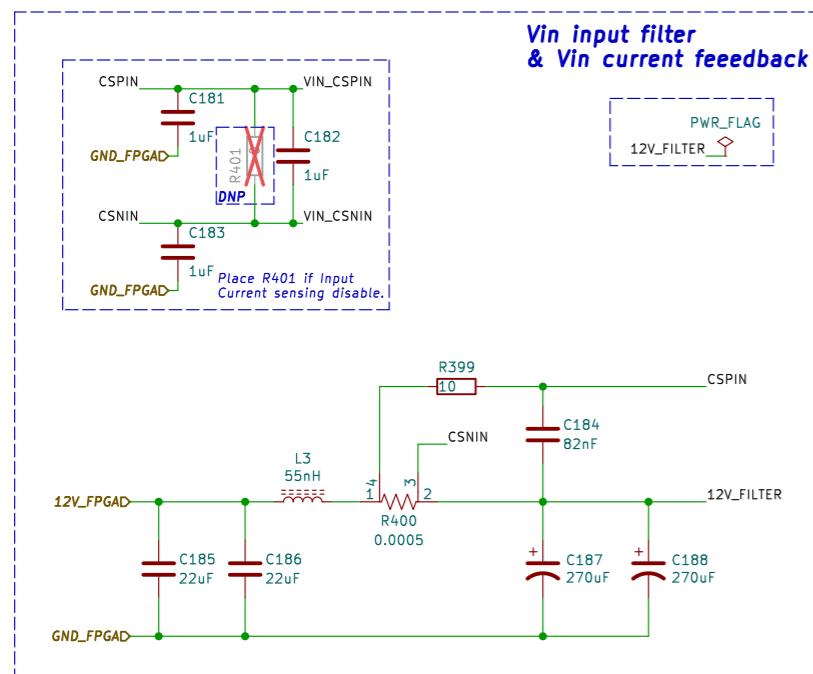
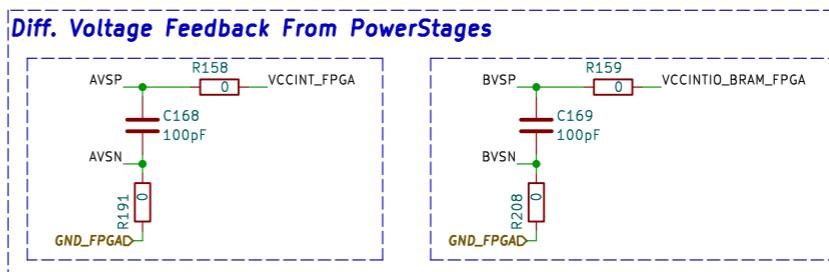
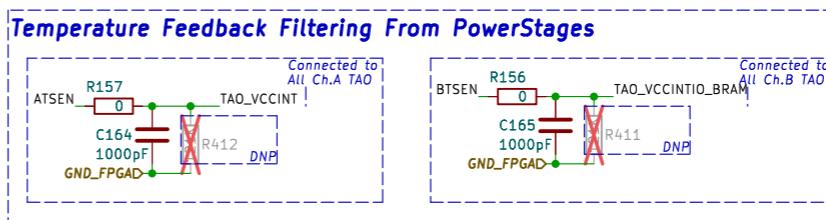
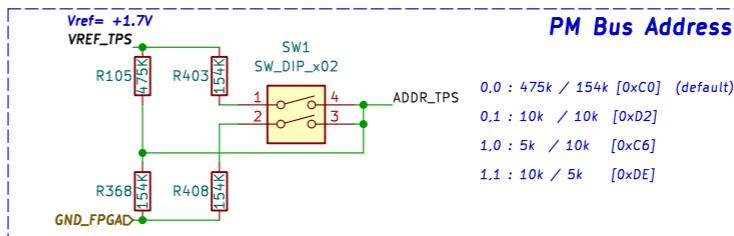
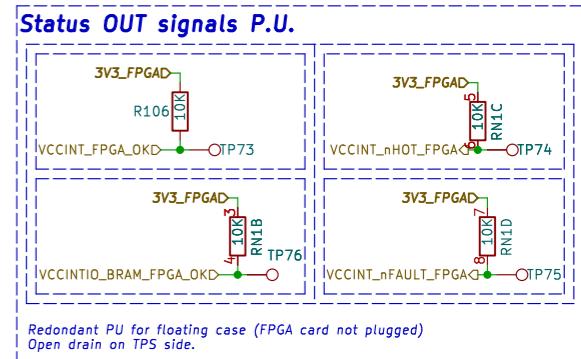
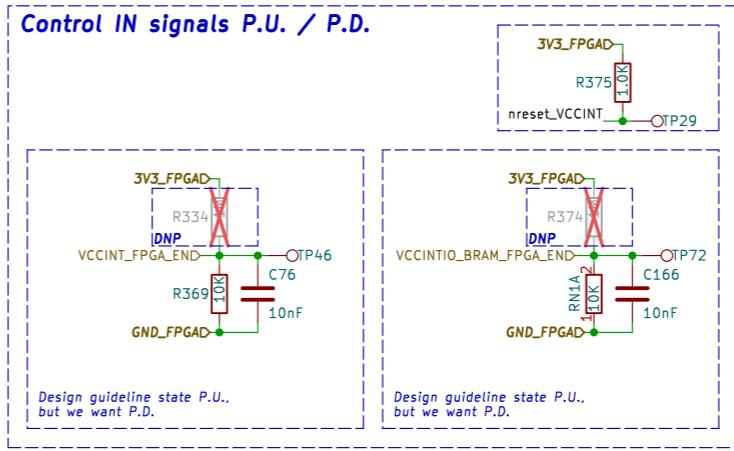
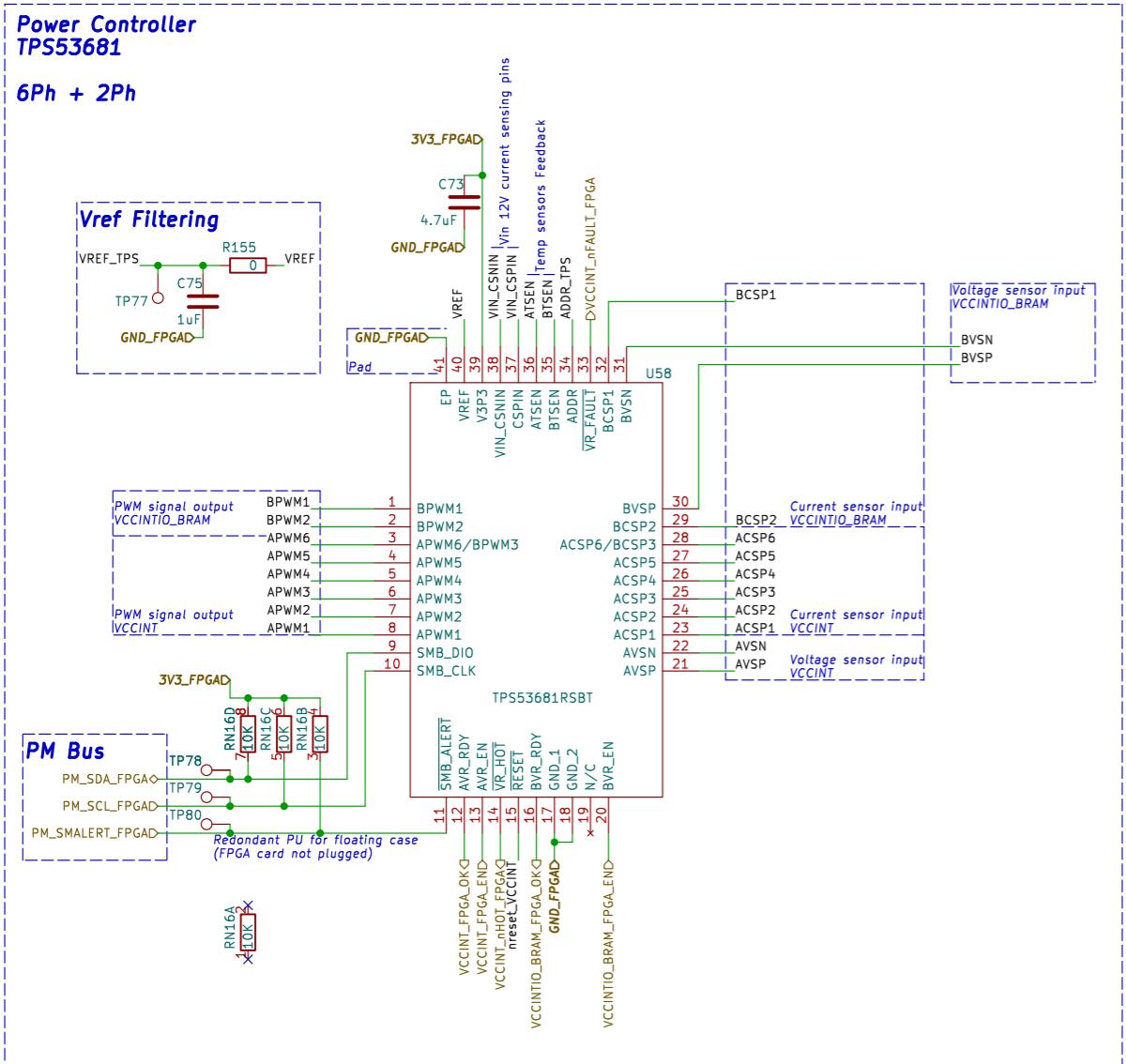
Size: A3 Date: 2025-01-01

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Rev: 2.0

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Sheet: /Mezzanine\_1/VCCINT\_Power\_Controller/  
File: VCCINT\_Power\_Controller.kicad\_sch

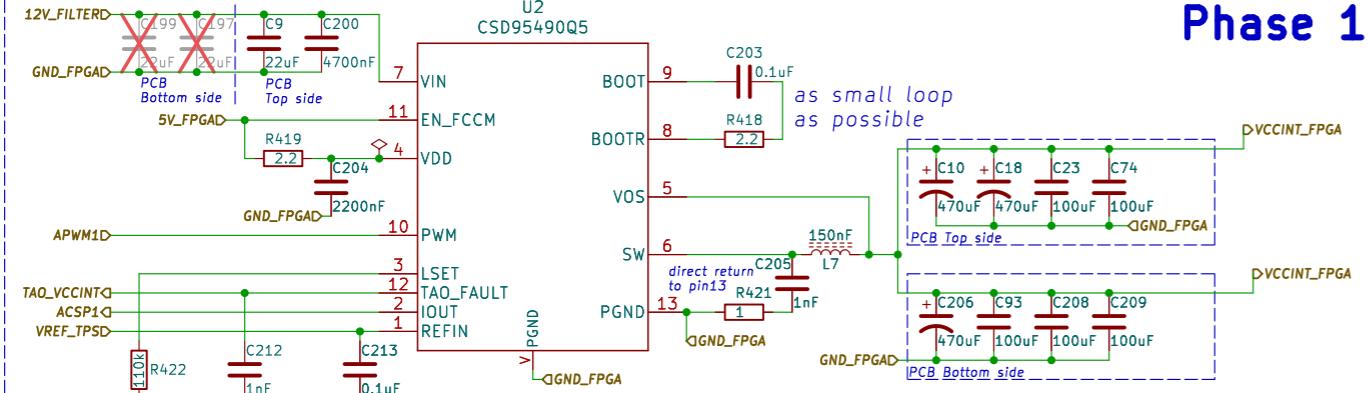
## Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P

Size: A3 Date: 2025-01-01  
KiCad EDA 8.0.1

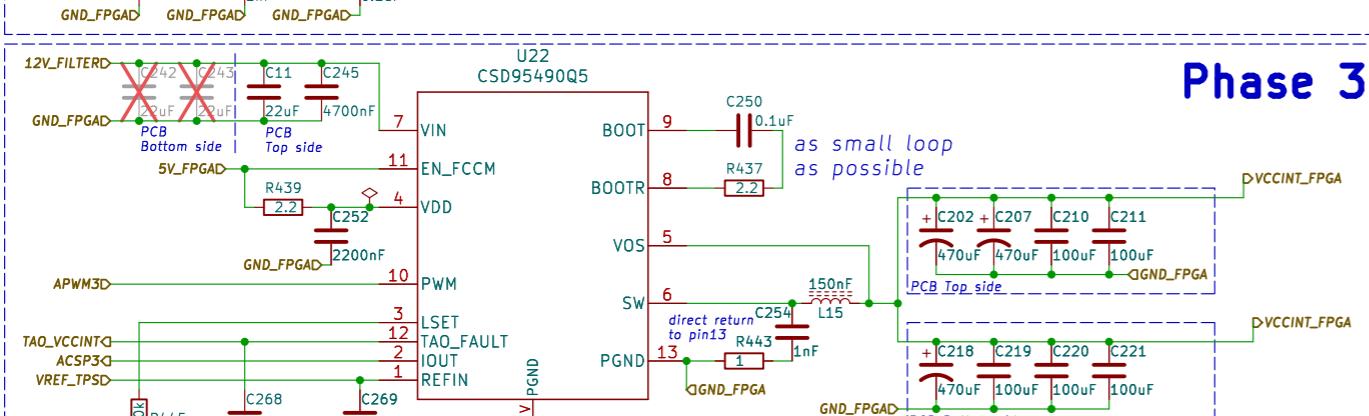
KiCad E.D.A. 8.0.1 | Id: 12/12

# VCCINT Variable 0.85Vdc. 6-Phases (PWM 1 – PWM 6)

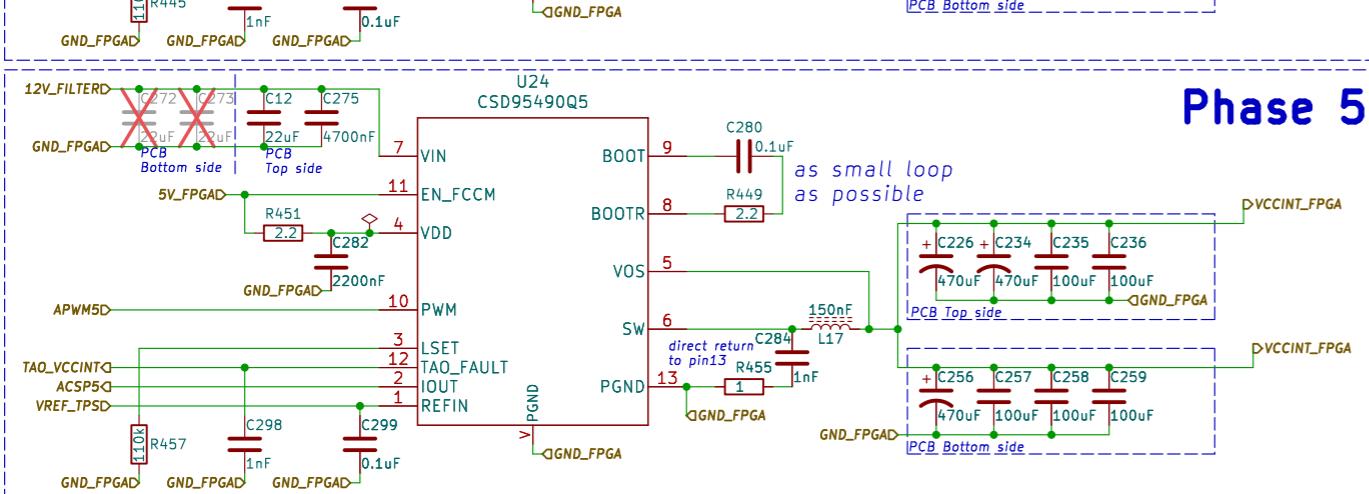
## Phase 1



## Phase 3

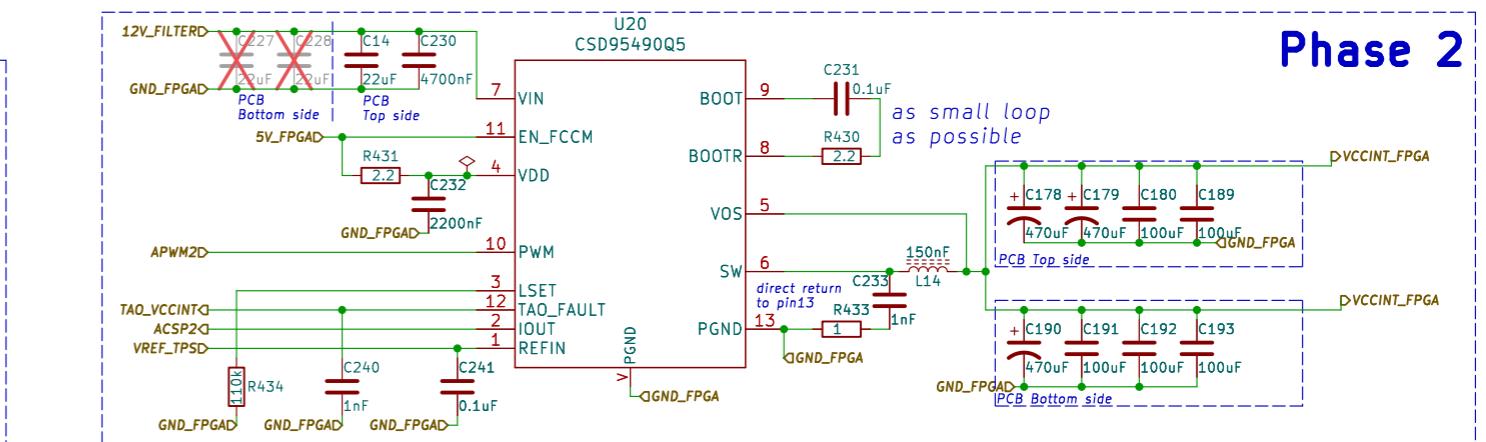
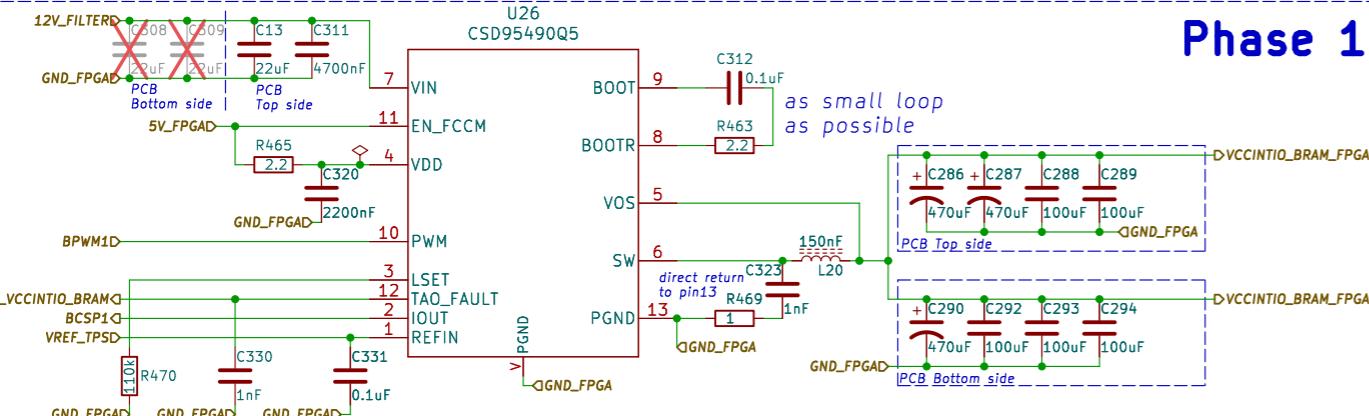


## Phase 5

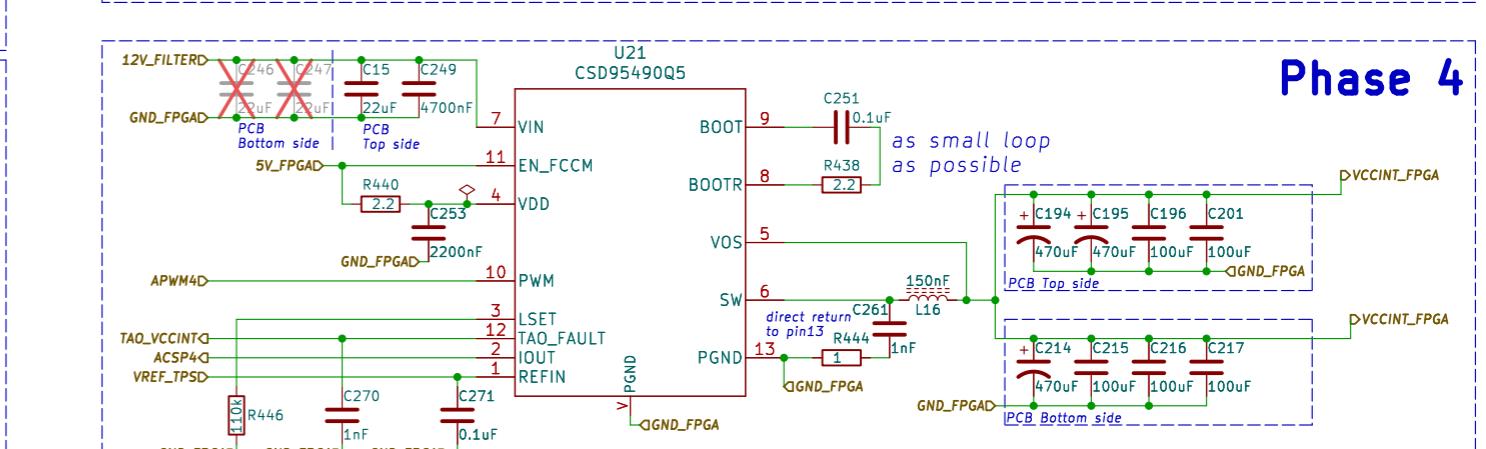


# VCCINTIO\_BRAM Fixed 0.8Vdc. 2-Phases (PWM 7 – PWM 8)

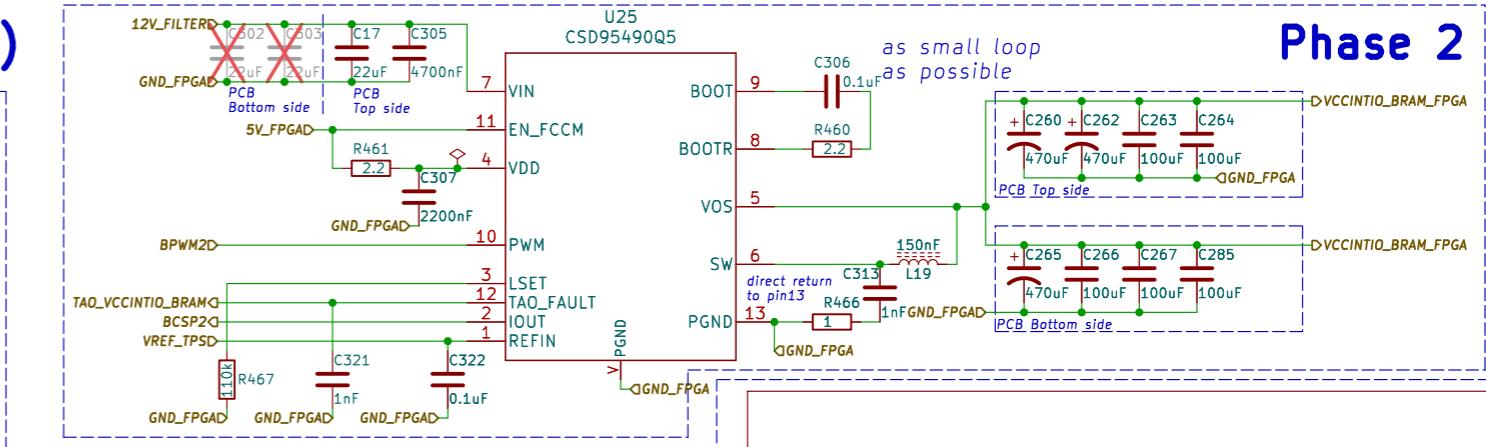
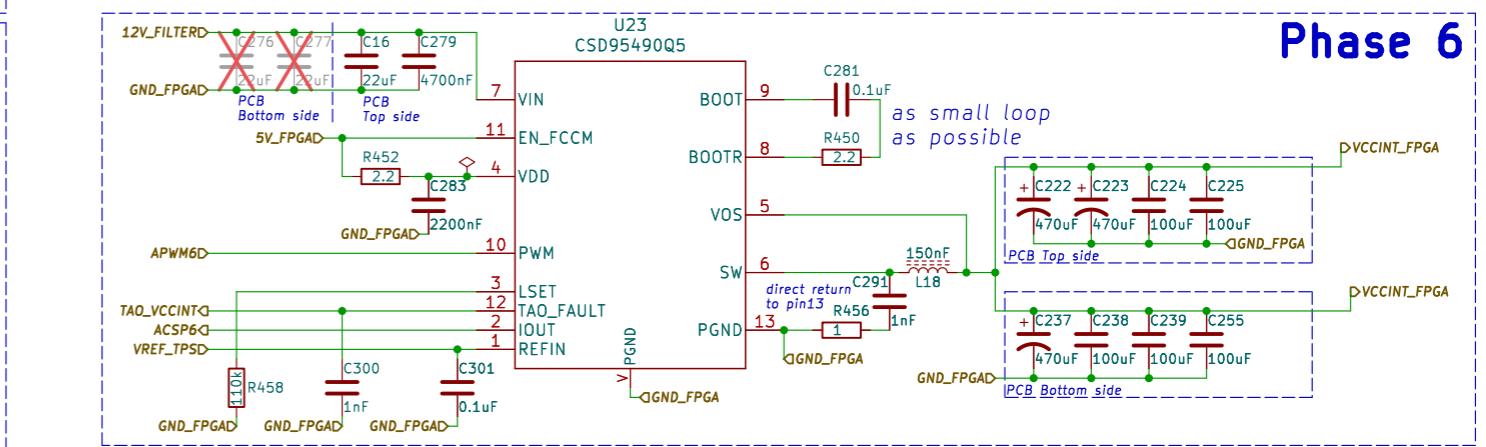
## Phase 1



## Phase 4



## Phase 6



For 8 Phases:  
Bottom Side Input CAP 22uF 0805 DNP  
Top Side Input CAP 0603 22uF Placed.

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Sheet: /mezzanine\_1/VCCINT\_Power\_Controller/PWM\_PWR\_Stage/

File: PWM\_PWR\_Stage.kicad\_sch

Title: Alto\_Ultra\_Plus Mezzanine for VU9P/VU13P

Size: A3 Date: 2025-01-01  
KiCad E.D.A. 8.0.1

Rev: 2.0  
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