First project: Building the beta-machine

Deadline: **Wednesday November 4th, 2020, 13:00** INFO0012 – Computation Structures

You are asked to build a β-machine in Logisim in groups of two.
Requirements:

- Your machine should use 32 bits registers and operations. It must be compatible with the same instruction set, OPCODEs, ALU operation list and function codes as in the course, but you are free to implement the machine as you want. The register addresses will be 5 bits long, it is mandatory to implement at least the 4 first and 4 last registers (r0, r1, r2, r3, r28, r29, r30, r31).
- You must include the necessary control lines and circuits to allow for all the operations seen in the course: ALU operations with and without constants, conditional branch, data memory and jump instructions.
- While the *circuit* must be a complete β-machine, the *control logic* should support the 5 instructions randomly assigned to you on the next page of this assignment. However, feel free to implement additional instructions in your control logic if you want, they may help you debug your machine.
- Your program memory should contain instructions to test each of your 5 operations. For conditional branch operations, test the different possible cases. The parameters and the way you test them are free, but the Instruction Memory must contain all the testing instructions in the submitted file. Please make sure your machine behaves as expected and the instructions are successfully executed. Again, you may program more instructions than necessary if you want to test your machine in more details. Doing more than expected will never hurt your grade.
- Please write a **very short report** (maximum 1 page), showing the instructions you programmed into the Instruction Memory and how you computed the addresses and values of the Control Logic. It will be used if your instructions or the values in your Control Logic are not working properly, in order to find the reason of the issue. Typically, a simple list of assembly instructions, and a truth table for the Control Logic is enough.

If you have any question or issue, do not hesitate to come to the Q/A sessions on Wednesdays at 13:45. You can also ask questions at any time on the eCampus forum.

Please upload a `.zip` archive containing your Logisim file (`.circ`) and your `.pdf` report on Montefiore's submission platform (`submit.montefiore.ulg.ac.be`) before the deadline. Your project will be tested directly in Logisim (`www.cburch.com/logisim`). Note: Logisim sometimes has issues saving the ROM contents. Make sure the ROMs are indeed programmed before sending your project.

Good luck and have fun building your first computer *from scratch* !

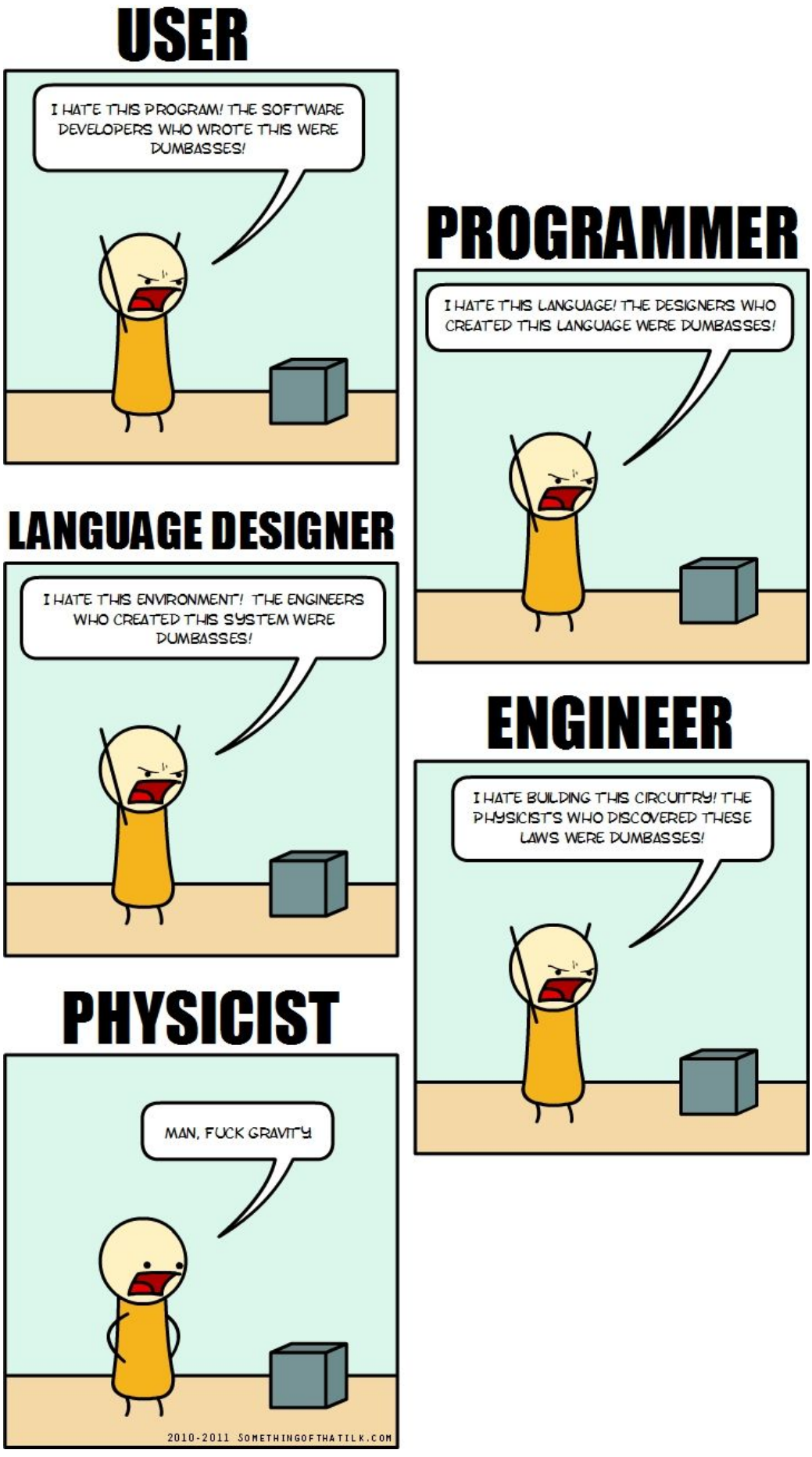
"If you wish to make an apple pie from scratch, you must first invent the universe."

— Carl Sagan, Cosmos

You must take the operations corresponding to the lowest student number of the group (e.g. if your group is s123455 and s123456, take the instructions on the s123455 line)

First student	Operations
s122193	ADDC, SRA, CMPLEC, LD, BNE
s124700	ADDC, OR, SHLC, ST, BEQ
s130985	ADDC, DIV, SHRC, JMP, BEQ
s143467	ADDC, CMPLT, CMPEQC, ST, BNE
s143882	ADDC, CMPEQ, ANDC, LD, BNE
s150353	ADDC, DIV, SRAC, LD, BNE
s150364	ADDC, XOR, CMPLEC, JMP, BEQ
s150651	ADDC, CMPEQ, XORC, JMP, BEQ
s151977	ADDC, CMPLT, DIVC, LD, BEQ
s153466	ADDC, SHR, SRAC, ST, BEQ
s160906	ADDC, XOR, CMPEQC, LD, BEQ
s161028	ADDC, CMPLE, ORC, LD, BNE
s161284	ADDC, OR, SHRC, ST, BNE
s161627	ADDC, SHL, CMPLEC, ST, BNE
s161917	ADDC, DIV, ANDC, LD, BNE
s161968	ADDC, SHL, CMPLTC, LD, BNE
s161987	ADDC, DIV, MULC, JMP, BEQ
s162264	ADDC, CMPLE, DIVC, JMP, BNE
s162407	ADDC, SHL, ORC, ST, BNE
s162655	ADDC, XOR, SHRC, LD, BNE
s162662	ADDC, CMPLE, XORC, JMP, BEQ
s162694	ADDC, SHR, ORC, LD, BEQ
s164004	ADDC, SHR, MULC, JMP, BEQ
s164016	ADDC, SHR, MULC, JMP, BEQ
s165139	ADDC, XOR, CMPEQC, JMP, BEQ
s165152	ADDC, AND, SRAC, ST, BNE
s165274	ADDC, CMPEQ, SHLC, ST, BEQ
s165910	ADDC, CMPLT, CMPLEC, LD, BNE
s170859	ADDC, SHR, MULC, LD, BNE
s170940	ADDC, DIV, XORC, ST, BNE
s170962	ADDC, SHL, XORC, LD, BNE
s171197	ADDC, CMPEQ, SHLC, LD, BEQ
s171233	ADDC, SHL, XORC, ST, BEQ
s171234	ADDC, CMPEQ, SRAC, ST, BNE
s171663	ADDC, MUL, CMPLEC, JMP, BNE
s171695	ADDC, AND, CMPLTC, LD, BEQ
s172475	ADDC, AND, DIVC, LD, BEQ
s172877	ADDC, OR, CMPEQC, LD, BNE
s173169	ADDC, AND, SRAC, JMP, BNE
s173488	ADDC, CMPEQ, SRAC, LD, BEQ
s174788	ADDC, SHR, CMPLEC, LD, BEQ
s174796	ADDC, SRA, CMPLTC, JMP, BEQ
s174912	ADDC, CMPLE, XORC, JMP, BNE
s175043	ADDC, SHL, CMPLEC, ST, BNE
s175048	ADDC, CMPEQ, DIVC, ST, BEQ
s175111	ADDC, AND, CMPLTC, LD, BEQ
s175610	ADDC, CMPLE, ANDC, ST, BNE
s175611	ADDC, XOR, CMPLEC, ST, BEQ
s175615	ADDC, XOR, CMPLEC, LD, BEQ
s180162	ADDC, CMPLT, SHLC, ST, BNE
s180290	ADDC, CMPEQ, CMPLTC, LD, BEQ
s180337	ADDC, MUL, SRAC, LD, BNE

First student	Operations
s180383	ADDC, SHL, SRAC, ST, BNE
s180444	ADDC, SRA, ORC, ST, BNE
s180521	ADDC, AND, CMPLEC, LD, BNE
s180598	ADDC, XOR, MULC, JMP, BEQ
s180703	ADDC, SHR, ORC, JMP, BEQ
s180743	ADDC, DIV, ORC, LD, BEQ
s180746	ADDC, XOR, SHLC, LD, BNE
s180821	ADDC, DIV, MULC, JMP, BNE
s181062	ADDC, XOR, ANDC, ST, BEQ
s181069	ADDC, CMPLE, SHRC, LD, BNE
s181277	ADDC, MUL, ORC, ST, BEQ
s181338	ADDC, AND, SHLC, ST, BEQ
s181356	ADDC, SHL, CMPLEC, LD, BEQ
s181482	ADDC, DIV, CMPEQC, JMP, BNE
s181497	ADDC, CMPEQ, SRAC, ST, BEQ
s181506	ADDC, AND, XORC, ST, BNE
s181538	ADDC, CMPEQ, XORC, JMP, BNE
s181539	ADDC, AND, SHRC, JMP, BEQ
s181669	ADDC, CMPLT, CMPLEC, ST, BNE
s181703	ADDC, OR, CMPLTC, JMP, BEQ
s181779	ADDC, SHL, XORC, ST, BEQ
s181838	ADDC, XOR, SHRC, ST, BEQ
s181912	ADDC, XOR, CMPLEC, LD, BEQ
s181915	ADDC, CMPLE, ANDC, LD, BNE
s181947	ADDC, SHR, DIVC, ST, BNE
s182110	ADDC, DIV, XORC, JMP, BEQ
s182113	ADDC, XOR, SHRC, JMP, BNE
s182281	ADDC, CMPEQ, CMPLTC, JMP, BEQ
s182590	ADDC, AND, CMPEQC, LD, BNE
s182674	ADDC, SHL, XORC, JMP, BEQ
s182756	ADDC, SHL, ANDC, LD, BNE
s182784	ADDC, SRA, DIVC, JMP, BNE
s182844	ADDC, XOR, MULC, ST, BNE
s182909	ADDC, CMPEQ, ANDC, ST, BNE
s183024	ADDC, CMPEQ, SHLC, ST, BNE
s183157	ADDC, DIV, MULC, LD, BNE
s183714	ADDC, CMPEQ, ANDC, LD, BEQ
s183751	ADDC, XOR, SRAC, ST, BNE
s183946	ADDC, SRA, DIVC, LD, BEQ
s184279	ADDC, SHR, MULC, LD, BNE
s184366	ADDC, CMPLE, XORC, ST, BNE
s184373	ADDC, SRA, SHRC, ST, BEQ
s184480	ADDC, SHR, ANDC, ST, BEQ
s185008	ADDC, OR, ANDC, LD, BEQ
s197070	ADDC, MUL, CMPLTC, ST, BEQ
s197206	ADDC, SHR, XORC, JMP, BNE
s202208	ADDC, OR, ANDC, JMP, BEQ
s203876	ADDC, MUL, ANDC, LD, BNE
s204268	ADDC, CMPEQ, CMPLTC, LD, BEQ
s204708	ADDC, OR, SHLC, ST, BEQ
s204863	ADDC, CMPLT, MULC, JMP, BEQ
s205441	ADDC, SHL, SRAC, ST, BEQ


USER
I HATE THIS PROGRAM! THE SOFTWARE DEVELOPERS WHO WROTE THIS WERE DUMBASSES!
PROGRAMMER
I HATE THIS LANGUAGE! THE DESIGNERS WHO CREATED THIS LANGUAGE WERE DUMBASSES!
LANGUAGE DESIGNER
I HATE THIS ENVIRONMENT! THE ENGINEERS WHO CREATED THIS SYSTEM WERE DUMBASSES!
ENGINEER
I HATE BUILDING THIS CIRCUITRY! THE PHYSICIST'S WHO DISCOVERED THESE LAWS WERE DUMBASSES!
PHYSICIST
MAN, FUCK GRAVITY
2010-2011 SOMETHINGOFTHATILK.COM