EE599 Assignment 2

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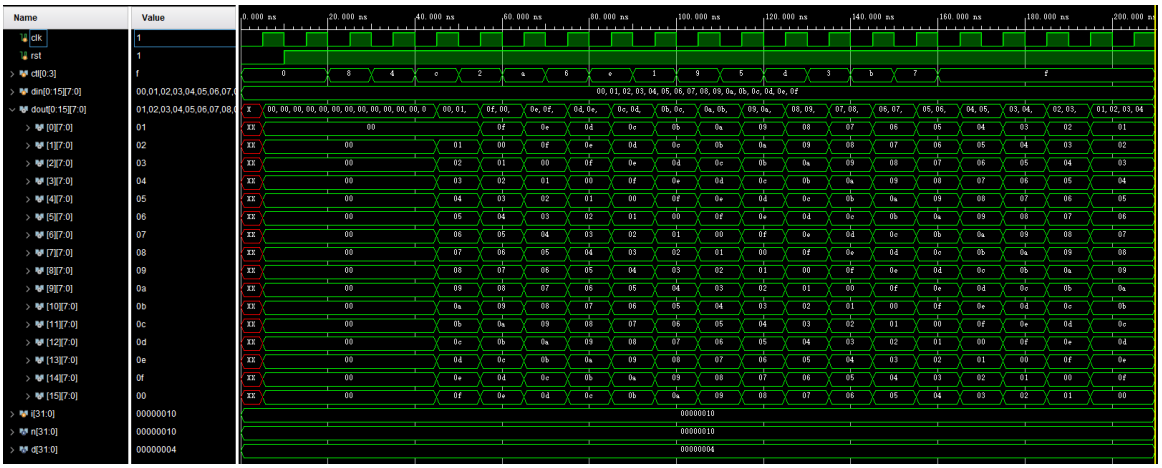
GitHub Link:
https://github.com/Olorin7/EE599_XueningZhao_5741894054/tree/master/Assignment2

1. Barrel Shifter

1.1 16 elements shift

Testbench result:



For n elements design(say $n = 2^k$), we have to build a k-stage design and need a k-bit control signal. In each stage, the corresponding bit of control signal would decide the MUX output. In this testbench, we have to wait for 4 clock cycles to get the output. I test all the 16 types of shifting. The dout shows every result.

Elaborated design and synthesized design are attached at the end of the report.

Time Report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.609 ns	Worst Hold Slack (WHS):	0.140 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	387	Total Number of Endpoints:	387	Total Number of Endpoints:	519

All user specified timing constraints are met.

Resource Report:

Resource	Utilization	Available	Utilization %
LUT	257	14400	1.78
FF	518	28800	1.80
IO	262	54	485.19

1.2 64 elements shift

Elaborated design and synthesized design are attached at the end of the report.

Time Report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.565 ns	Worst Hold Slack (WHS):	0.122 ns	Worst Pulse Width Slack (WPWS):	4.146 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2576	Total Number of Endpoints:	2576	Total Number of Endpoints:	3098

All user specified timing constraints are met.

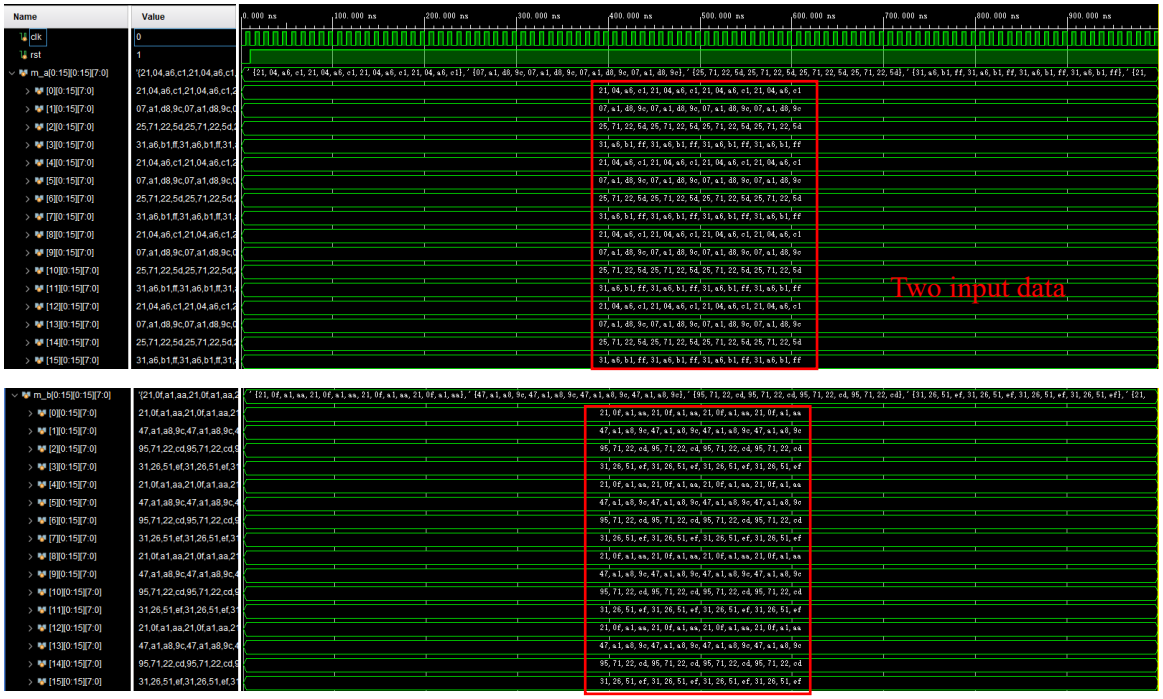
Resource Report:

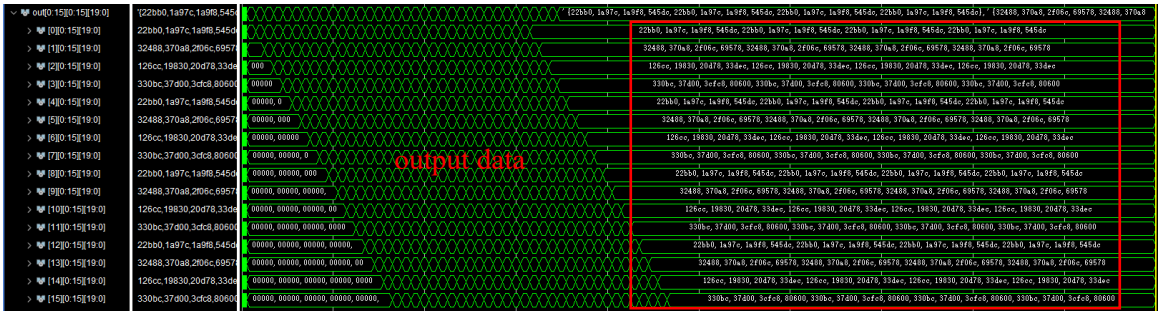
Resource	Utilization	Available	Utilization %
LUT	1541	14400	10.70
LUTRAM	2	6000	0.03
FF	3095	28800	10.75
IO	1032	54	1911.11

2. Systolic Array for Dense Matrix-Matrix Multiplication

2.1 16*16 matrices

Testbench result:





For a 16*16 design, the systolic array needs 32 input data and the output is 20 bits. In testbench, all the matrix data should be sent to array in order. So, in this design, we need 31 + 15 clocks to get the final answer. The testbench would read two txt files to load two input matrixes. Finally, the output matrix is shown in the picture.

Elaborated design and synthesized design are attached at the end of the report.

Time Report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.541 ns	Worst Hold Slack (WHS):	0.115 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8704	Total Number of Endpoints:	8704	Total Number of Endpoints:	8961

All user specified timing constraints are met.

Resource Report:

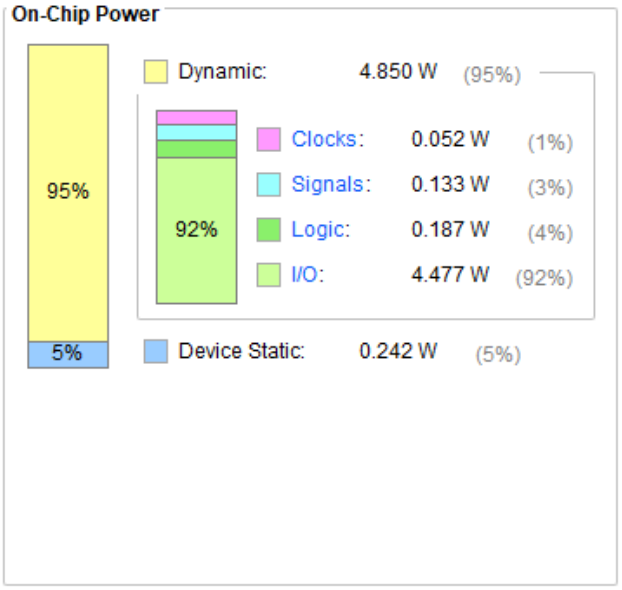
Resource	Utilization	Available	Utilization %
LUT	22015	14400	152.88
FF	8960	28800	31.11
IO	5378	54	9959.26

Power Report:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**5.092 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**83.7°C**
Thermal Margin:	16.3°C (1.3 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



2.2 32*32 matrices

Time Report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.614 ns	Worst Hold Slack (WHS):	0.115 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	36864	Total Number of Endpoints:	36864	Total Number of Endpoints:	37377

All user specified timing constraints are met.

Resource Report:

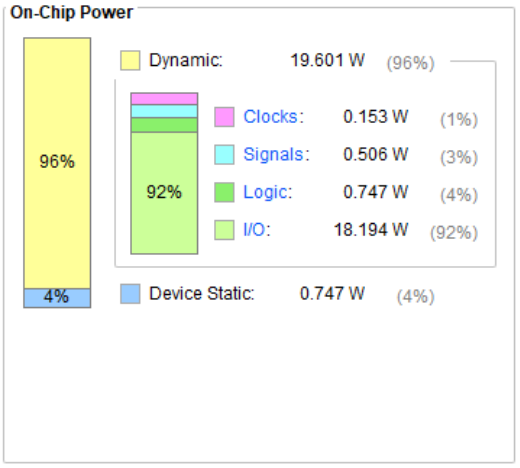
Resource	Utilization	Available	Utilization %
LUT	90051	14400	625.35
FF	37376	28800	129.78
IO	22018	54	40774.07

Power Report:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**20.349 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**125.0°C**
Thermal Margin:	-159.7°C (-13.4 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

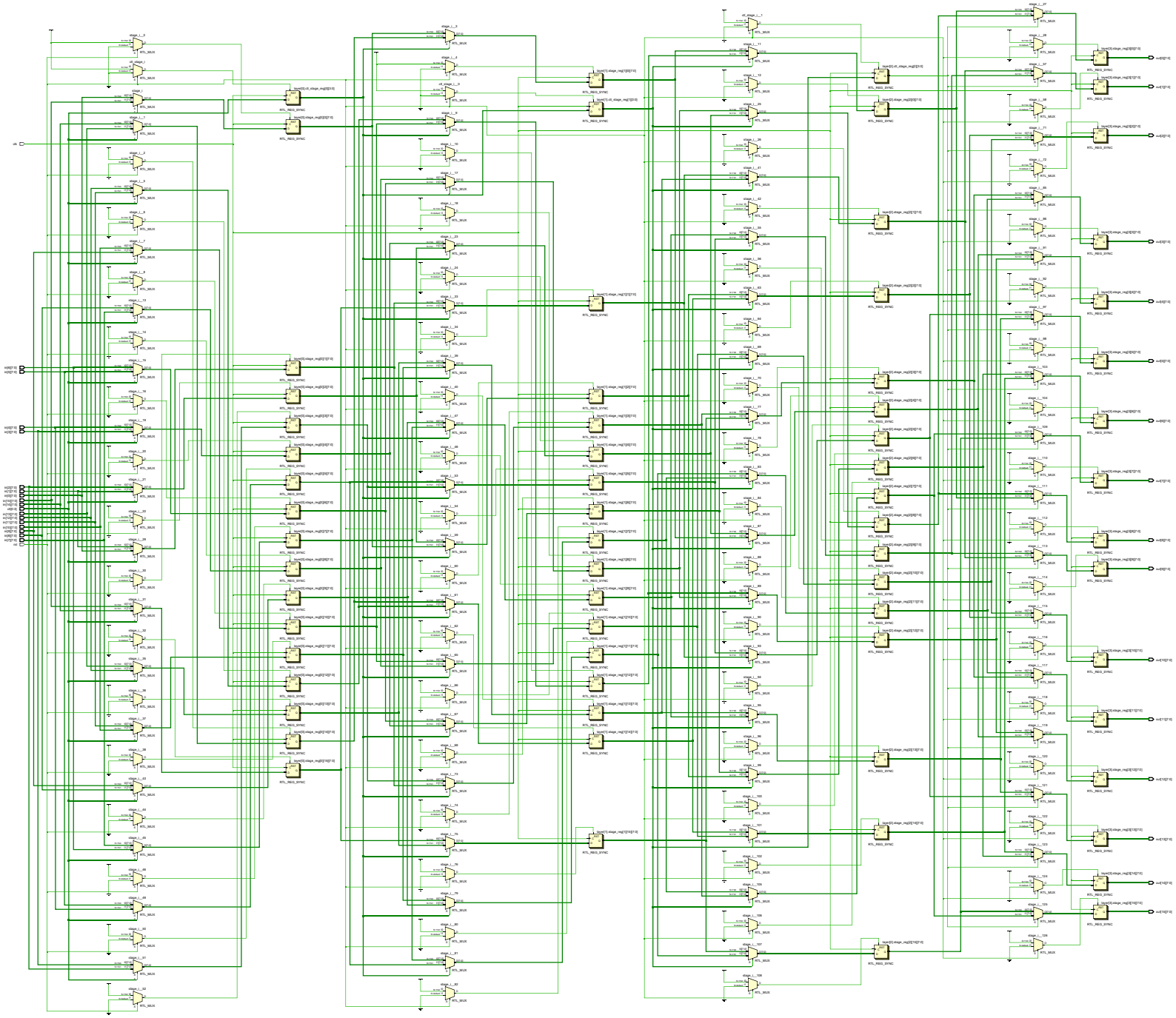


Since it is beyond limitation, this power estimation is unreliable.

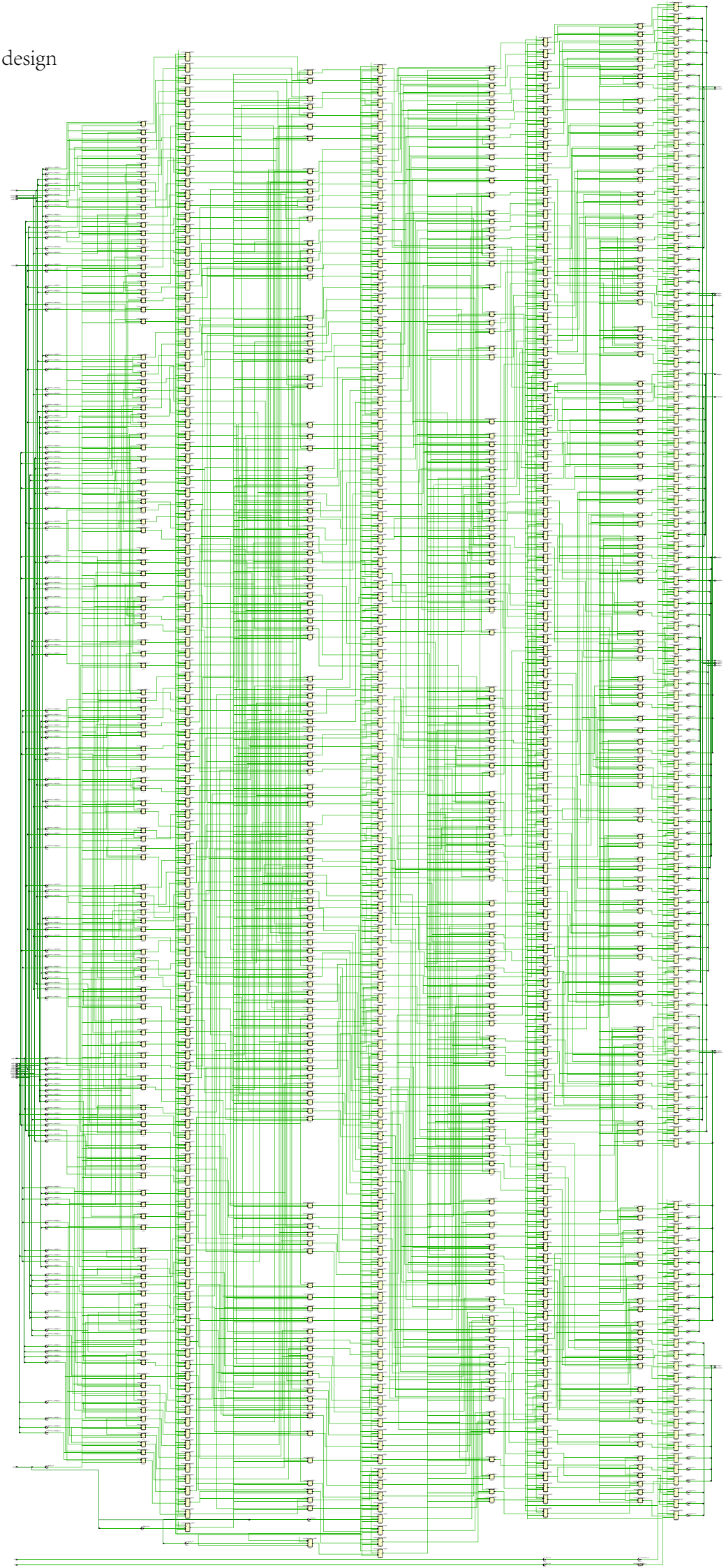
3. Design Schematics

16 elements shift:

elaborated design:

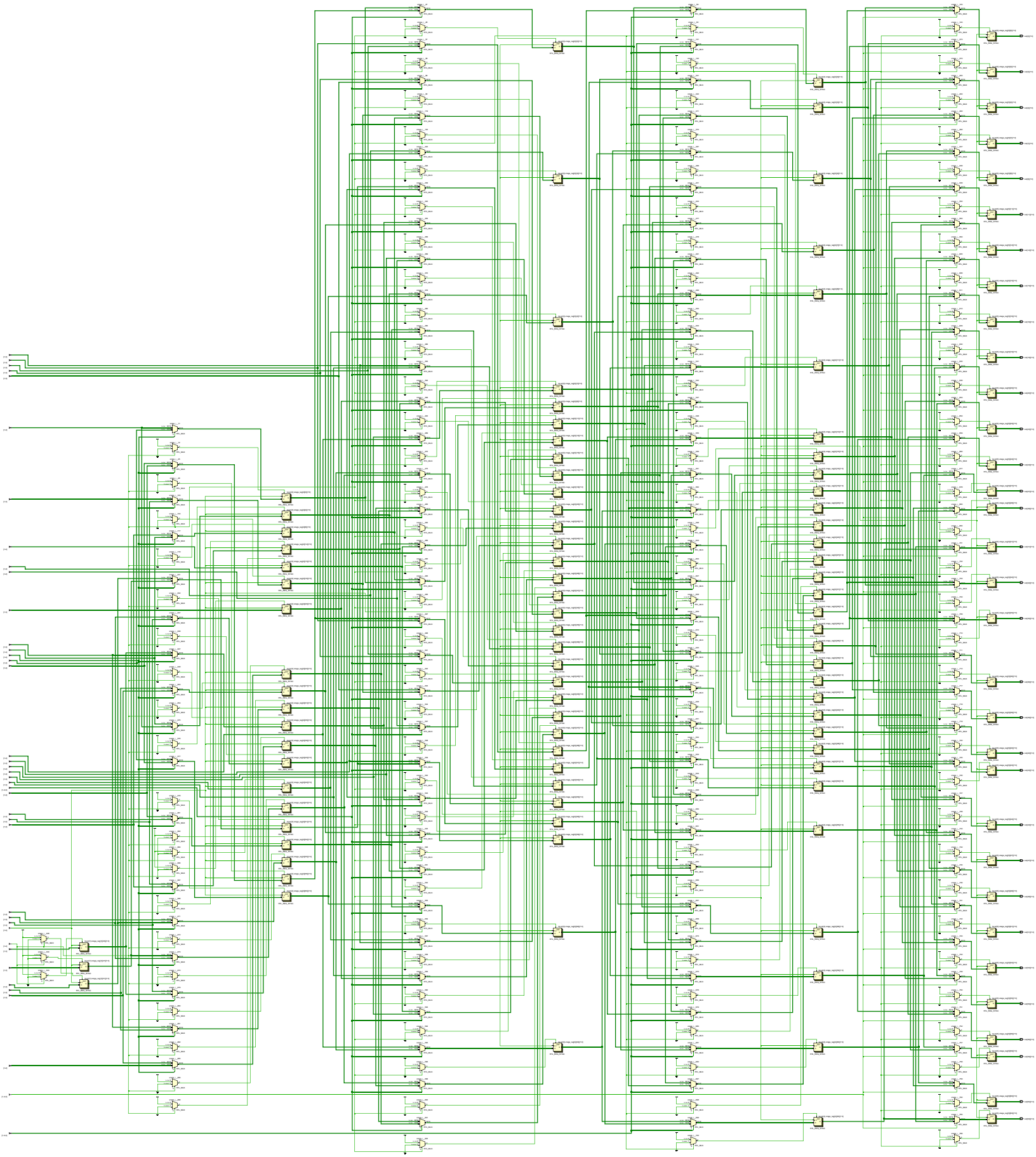


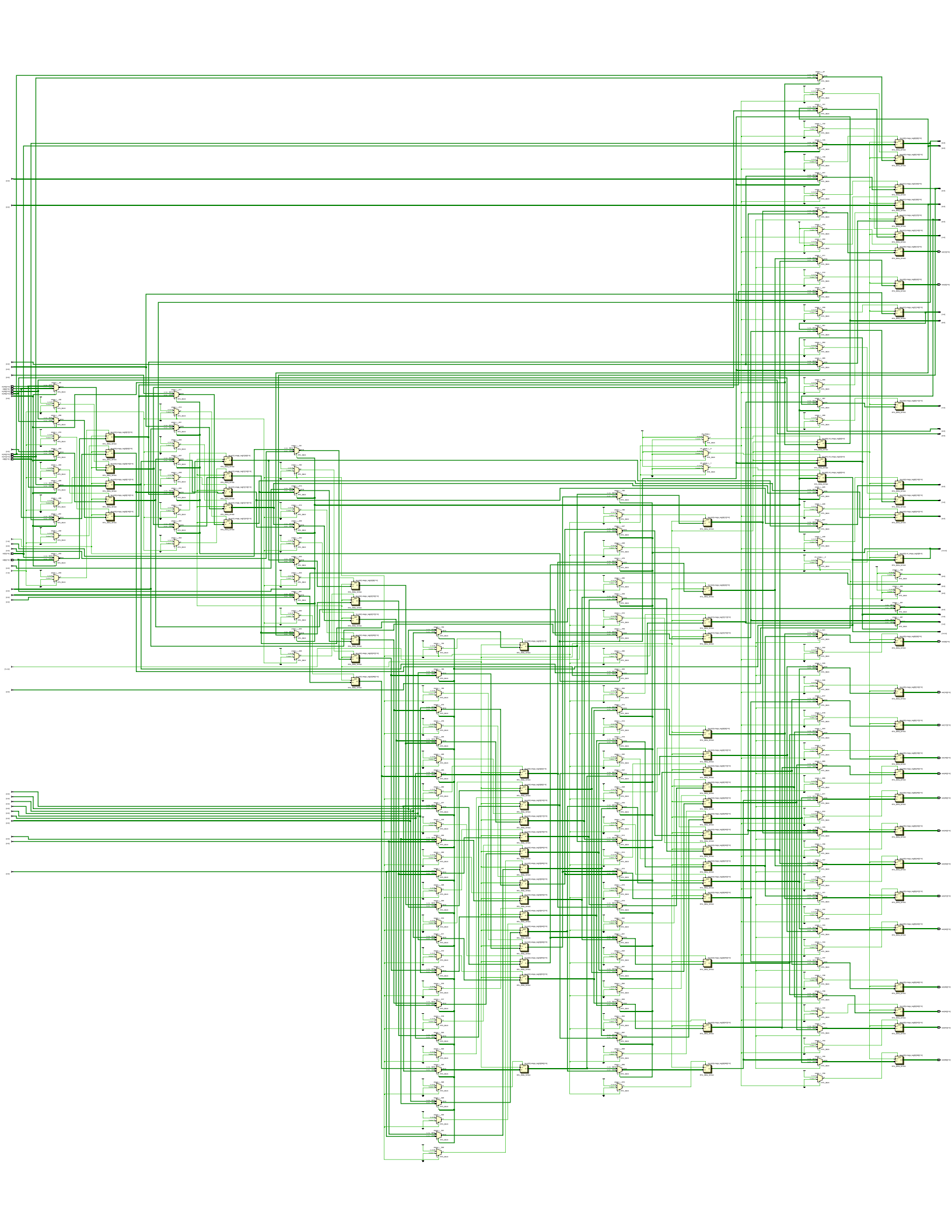
synthesized design

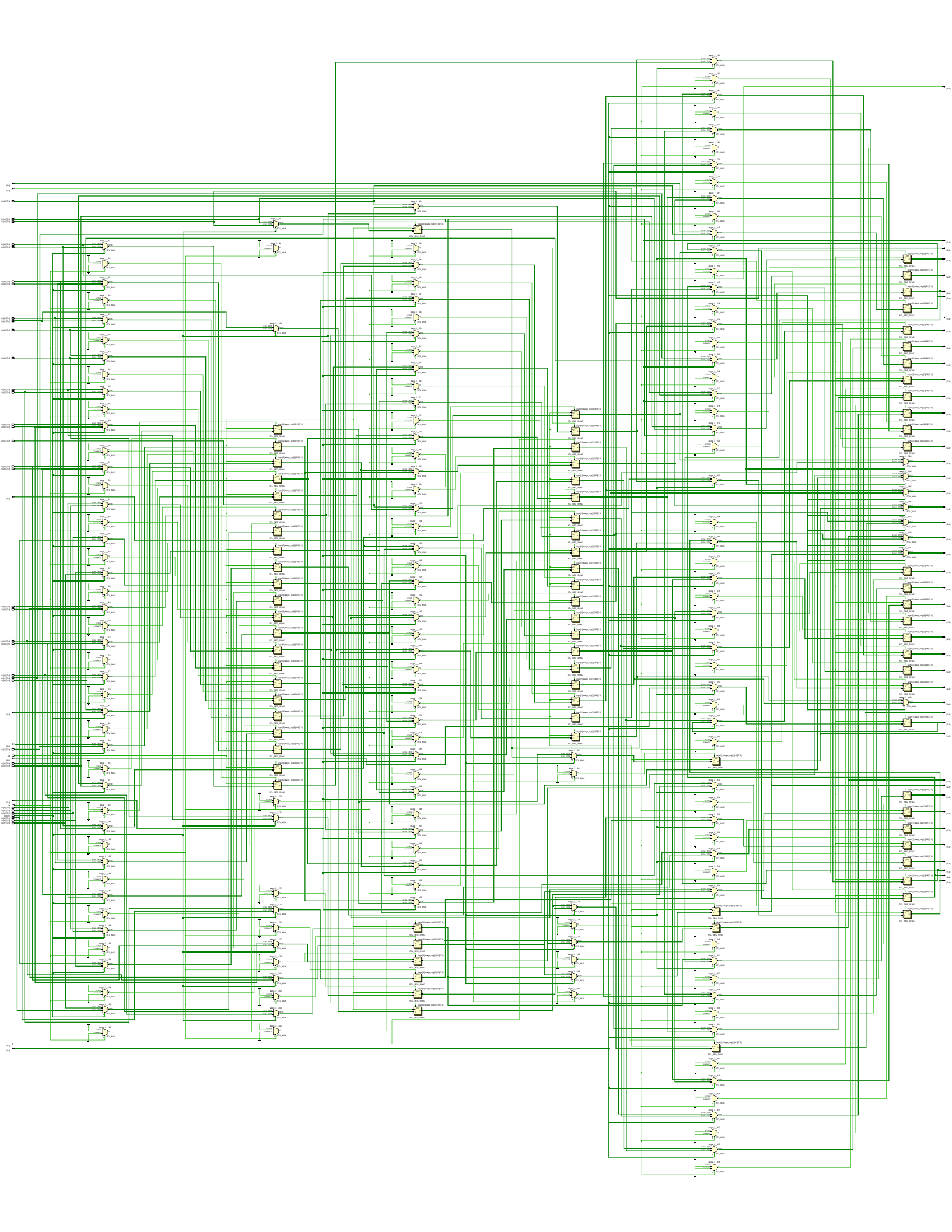


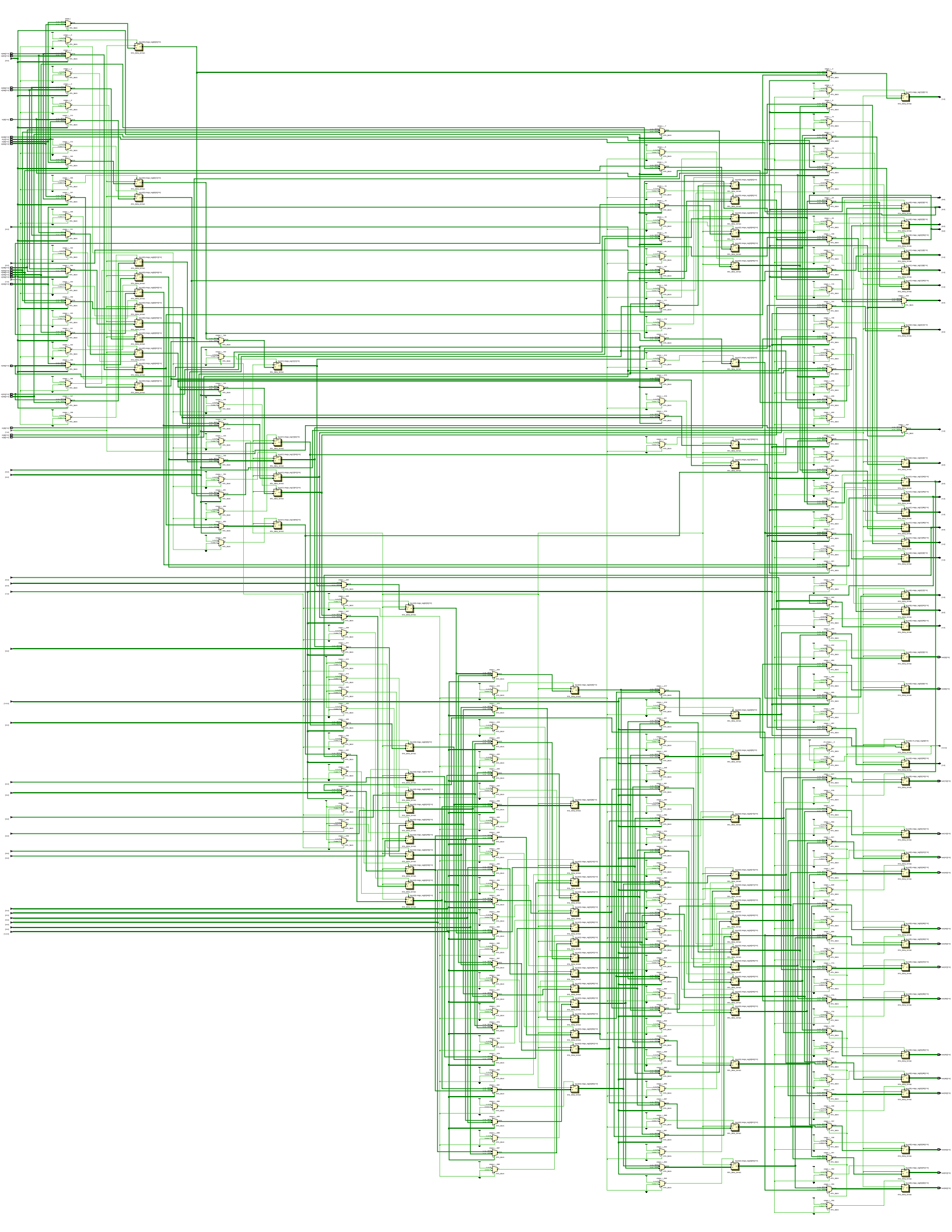
64 elements shift:

elaborated design

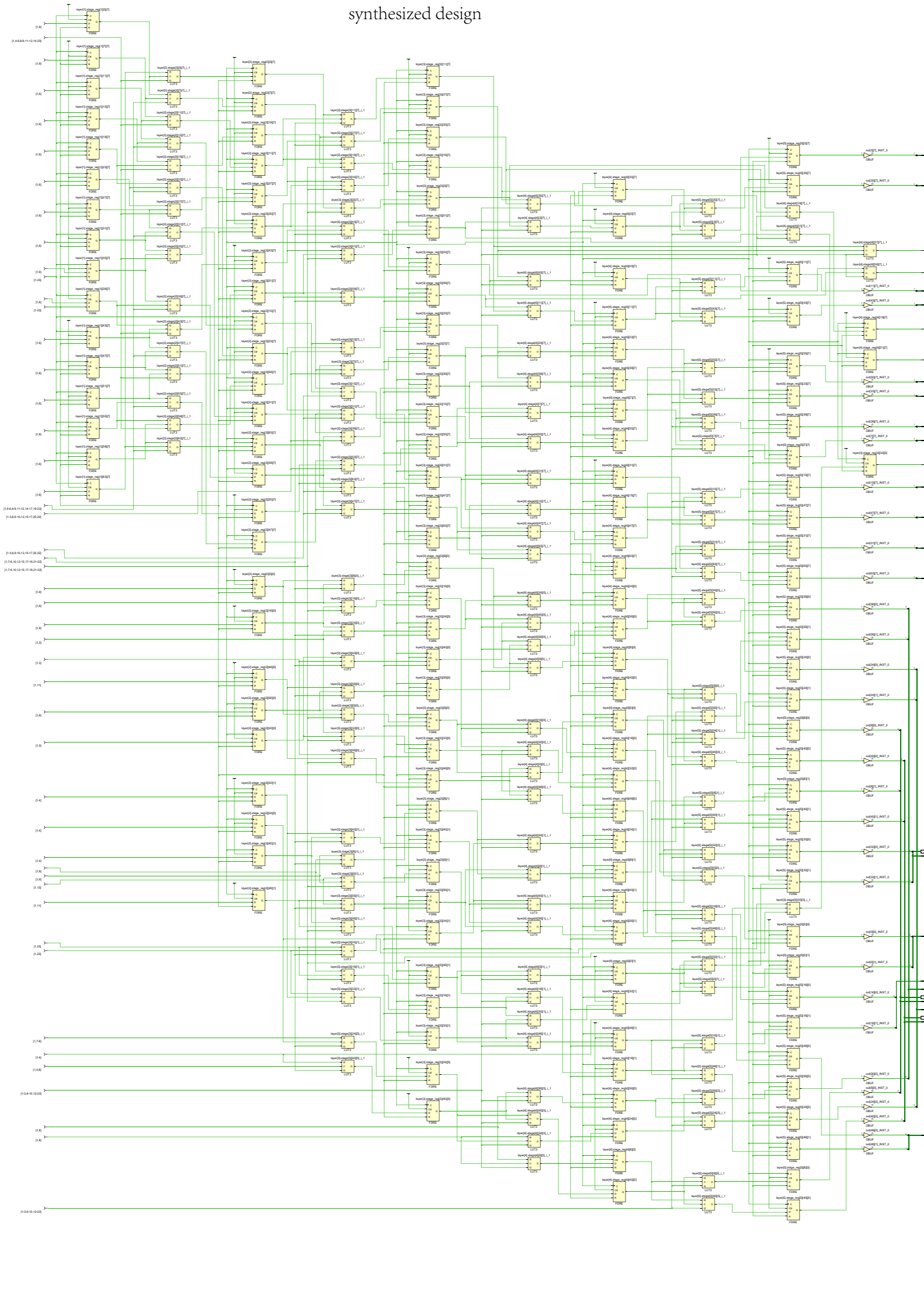


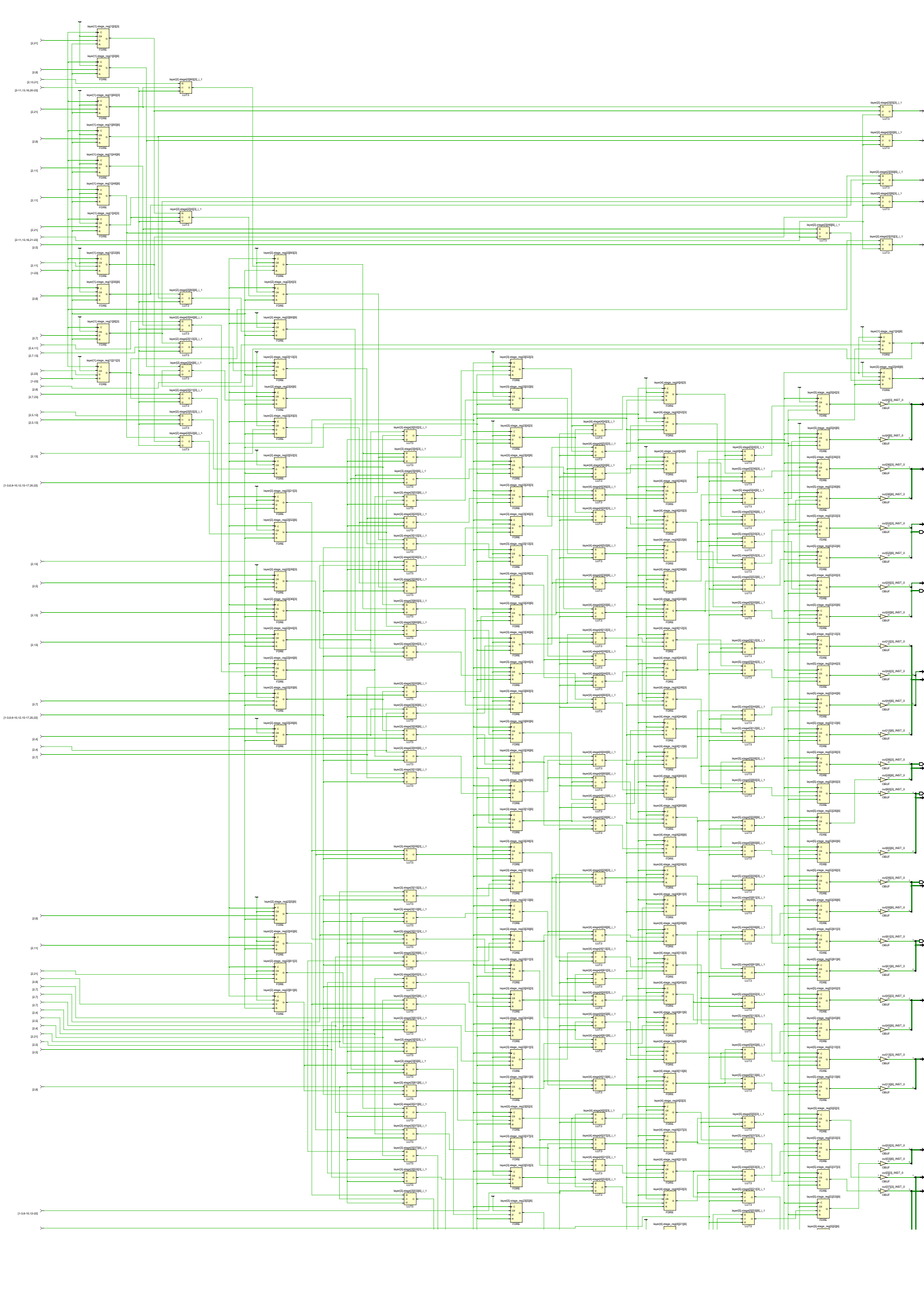


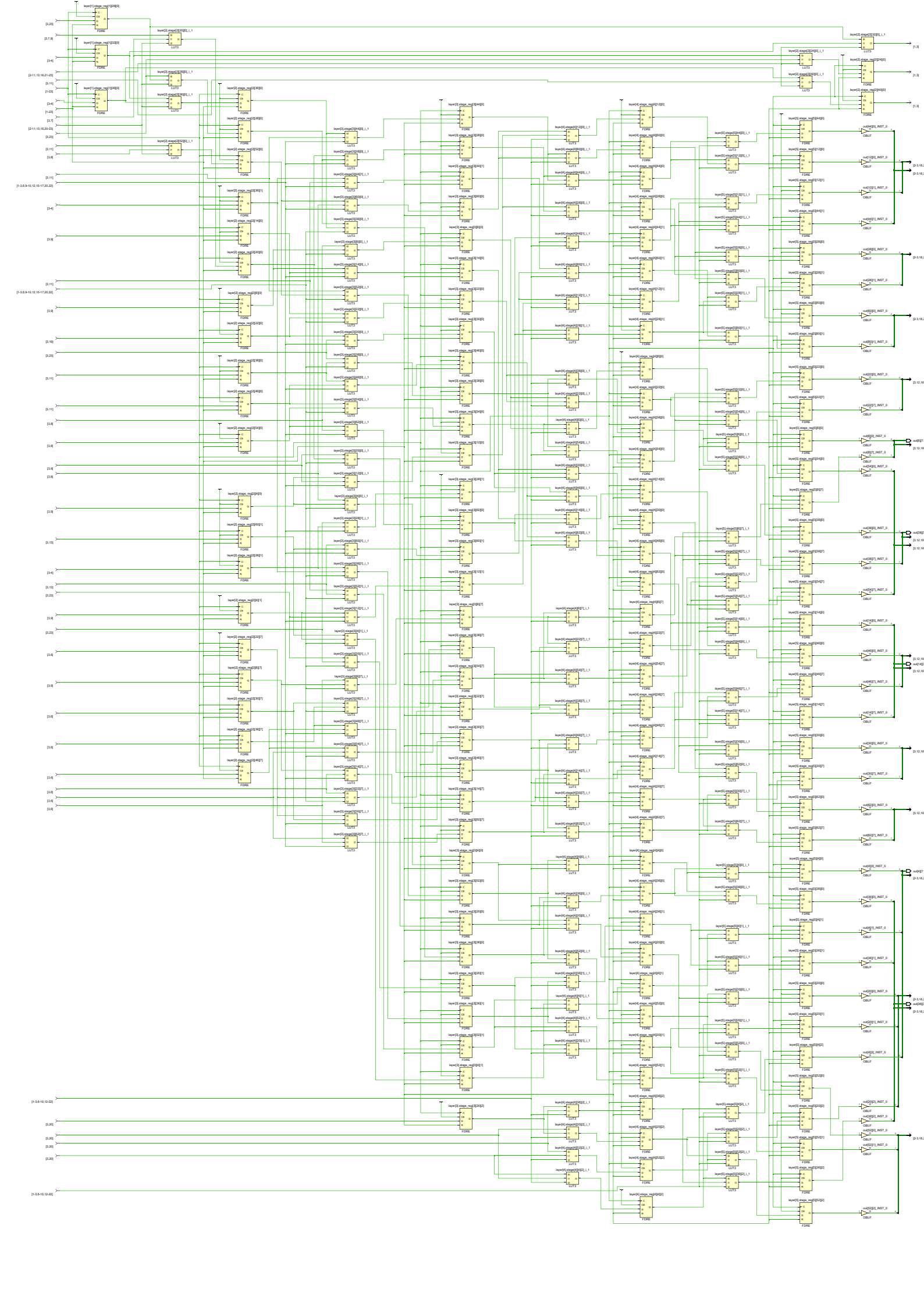


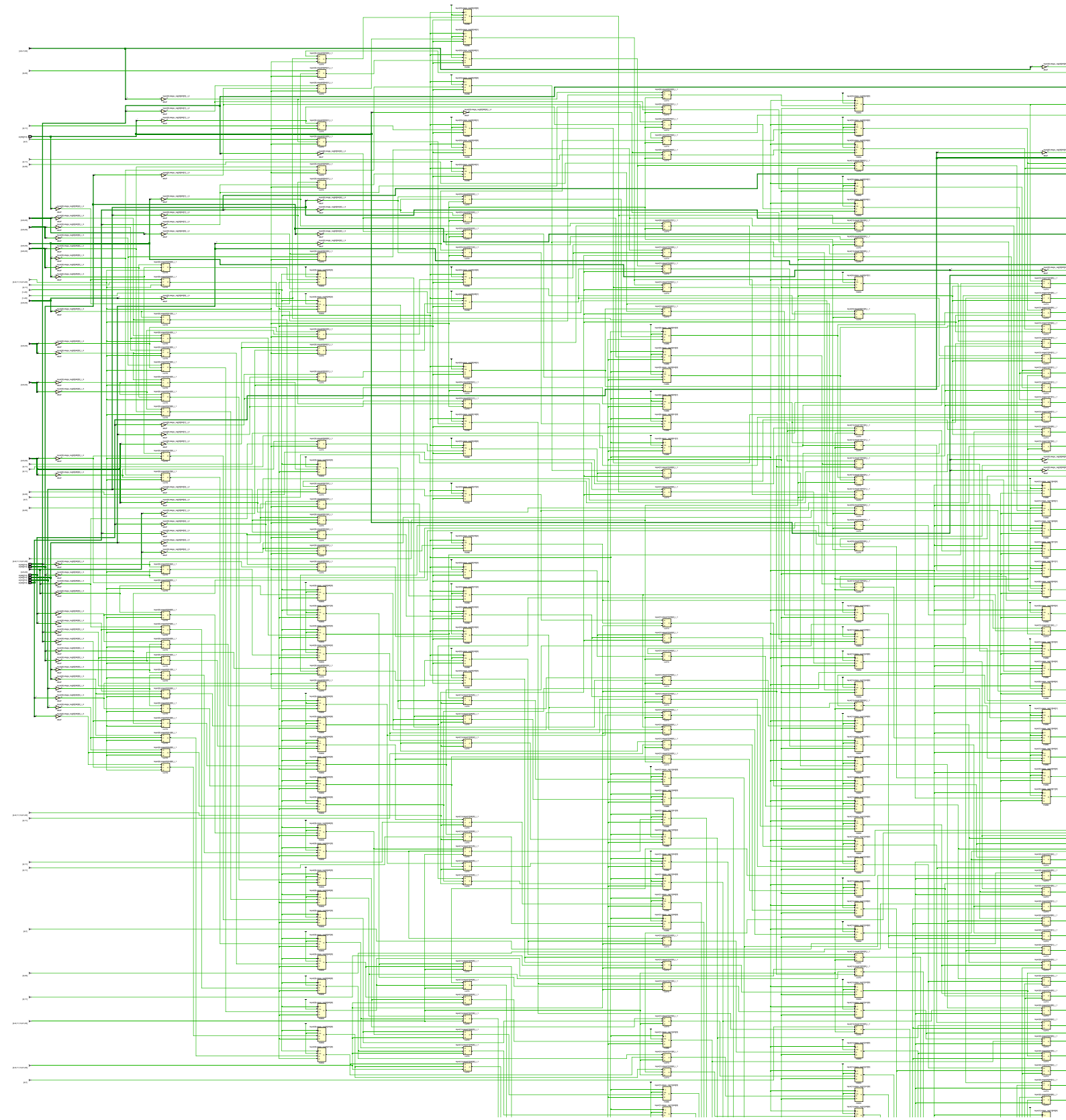


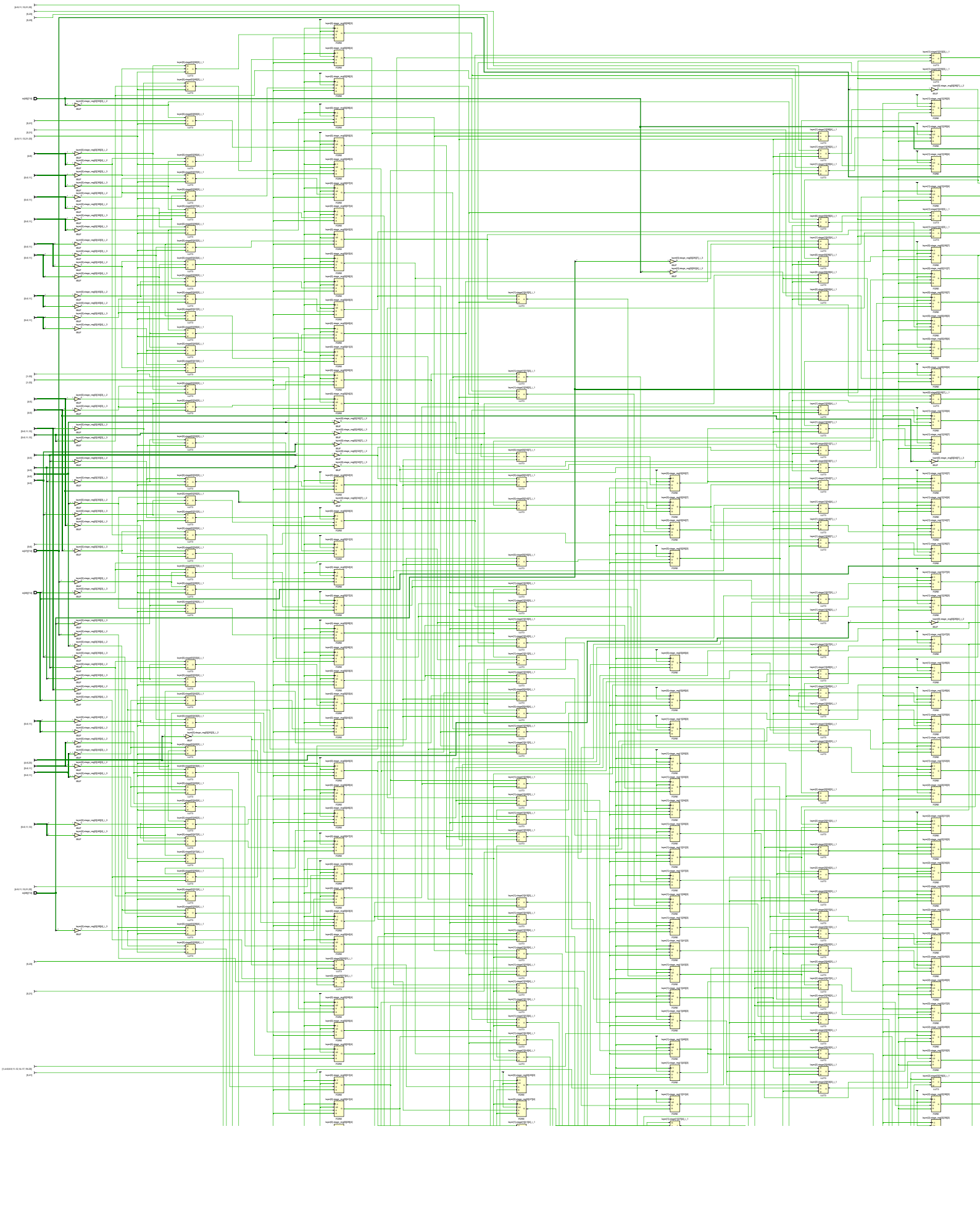
synthesized design

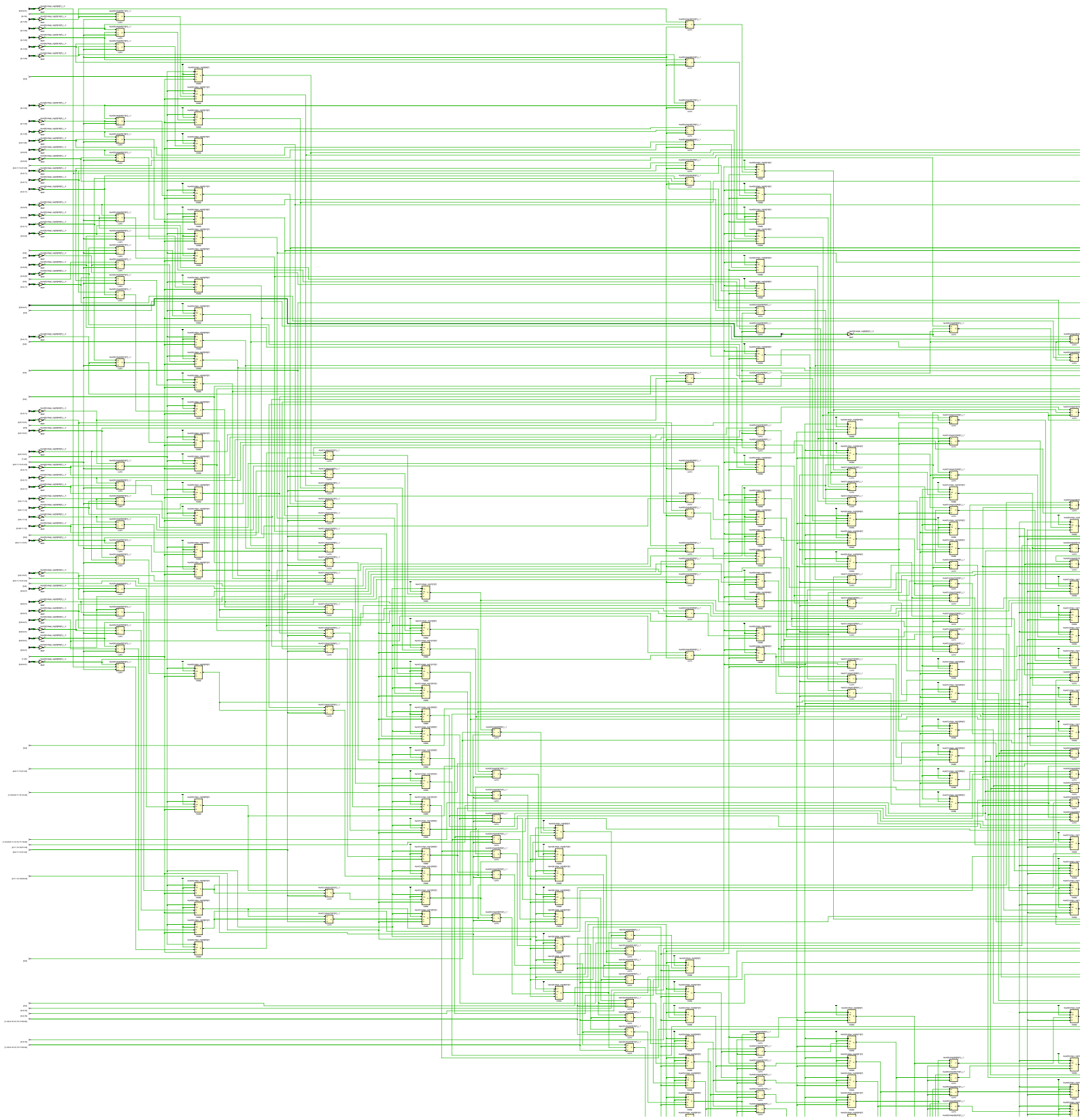


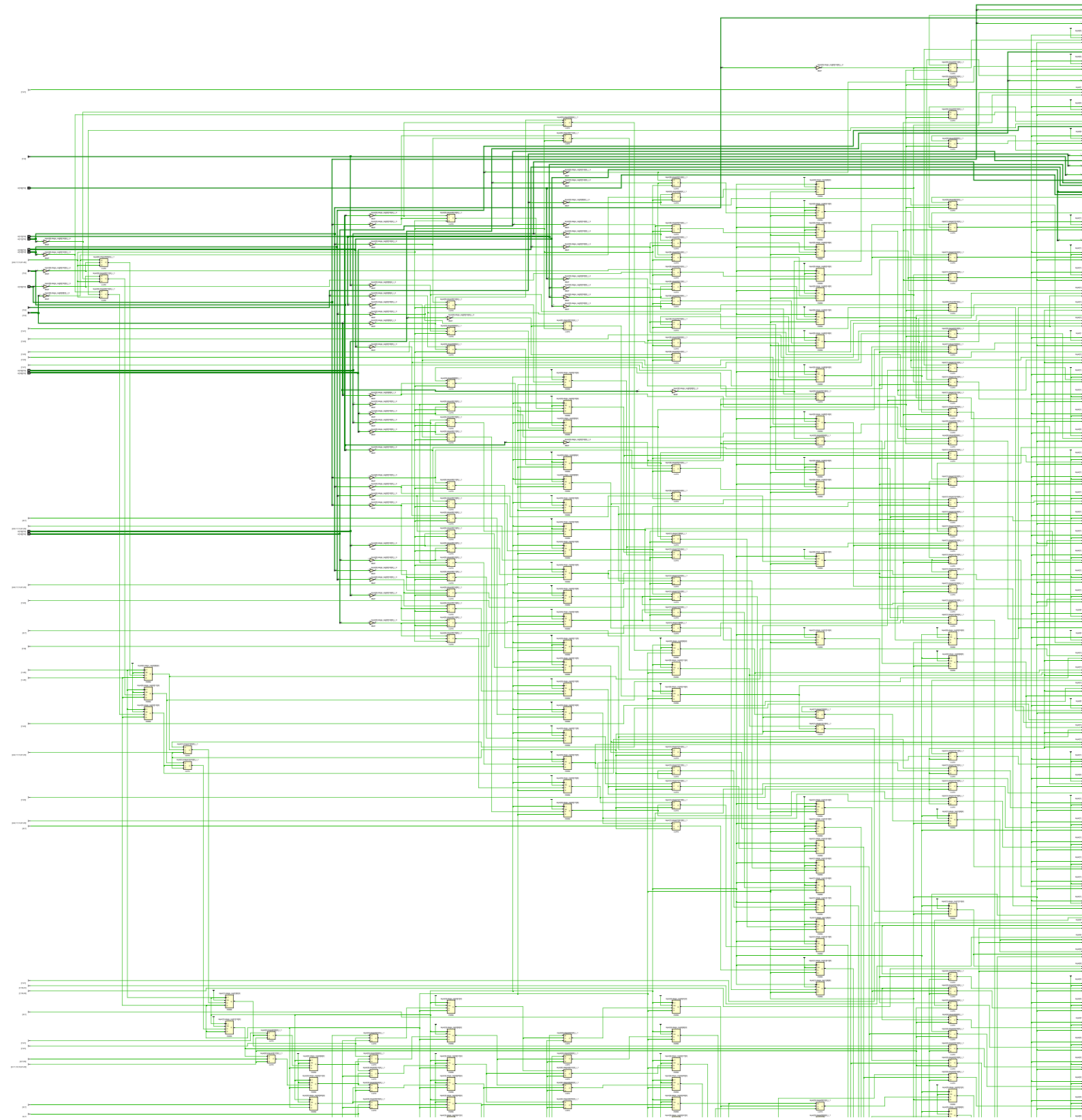


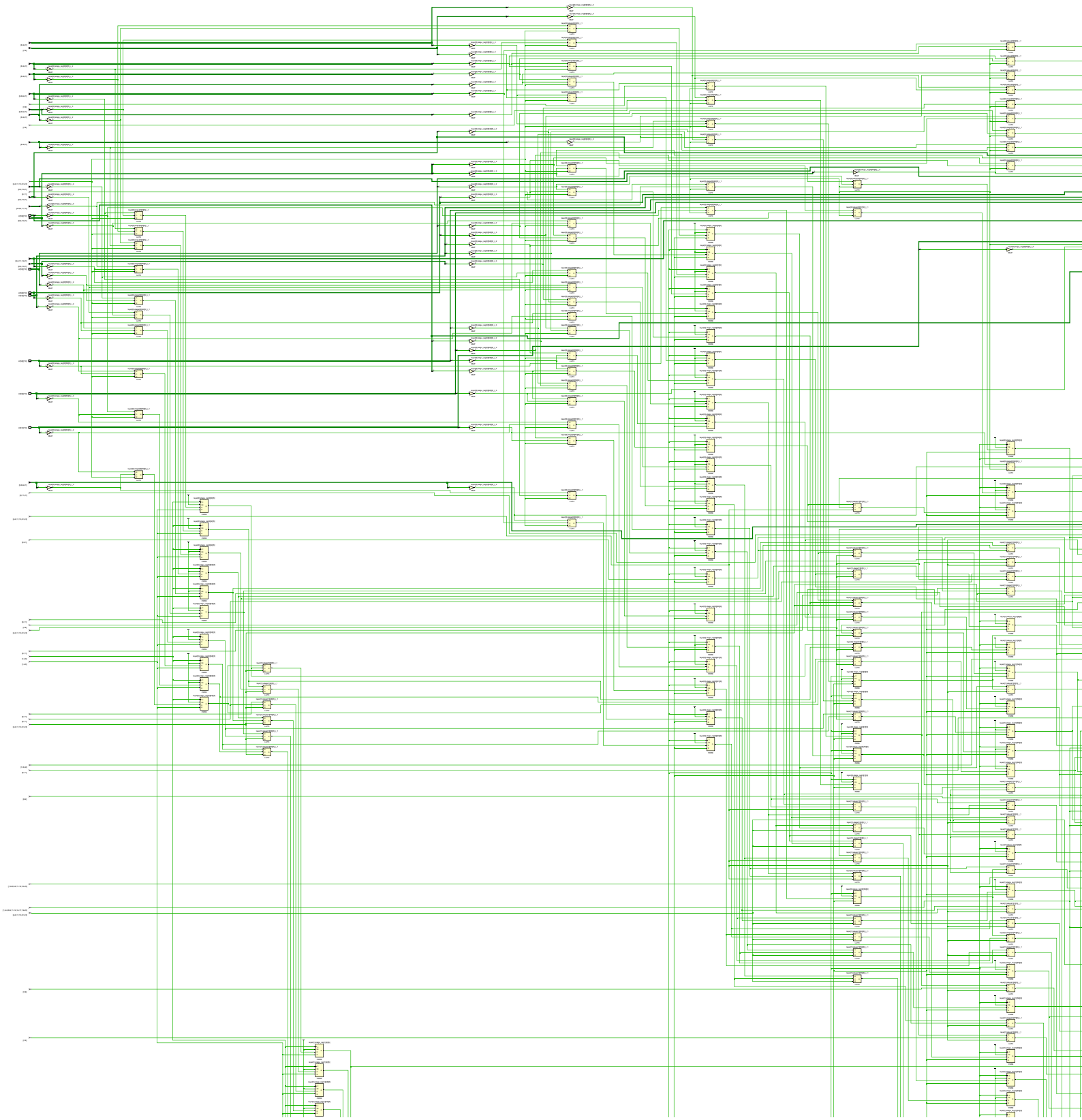


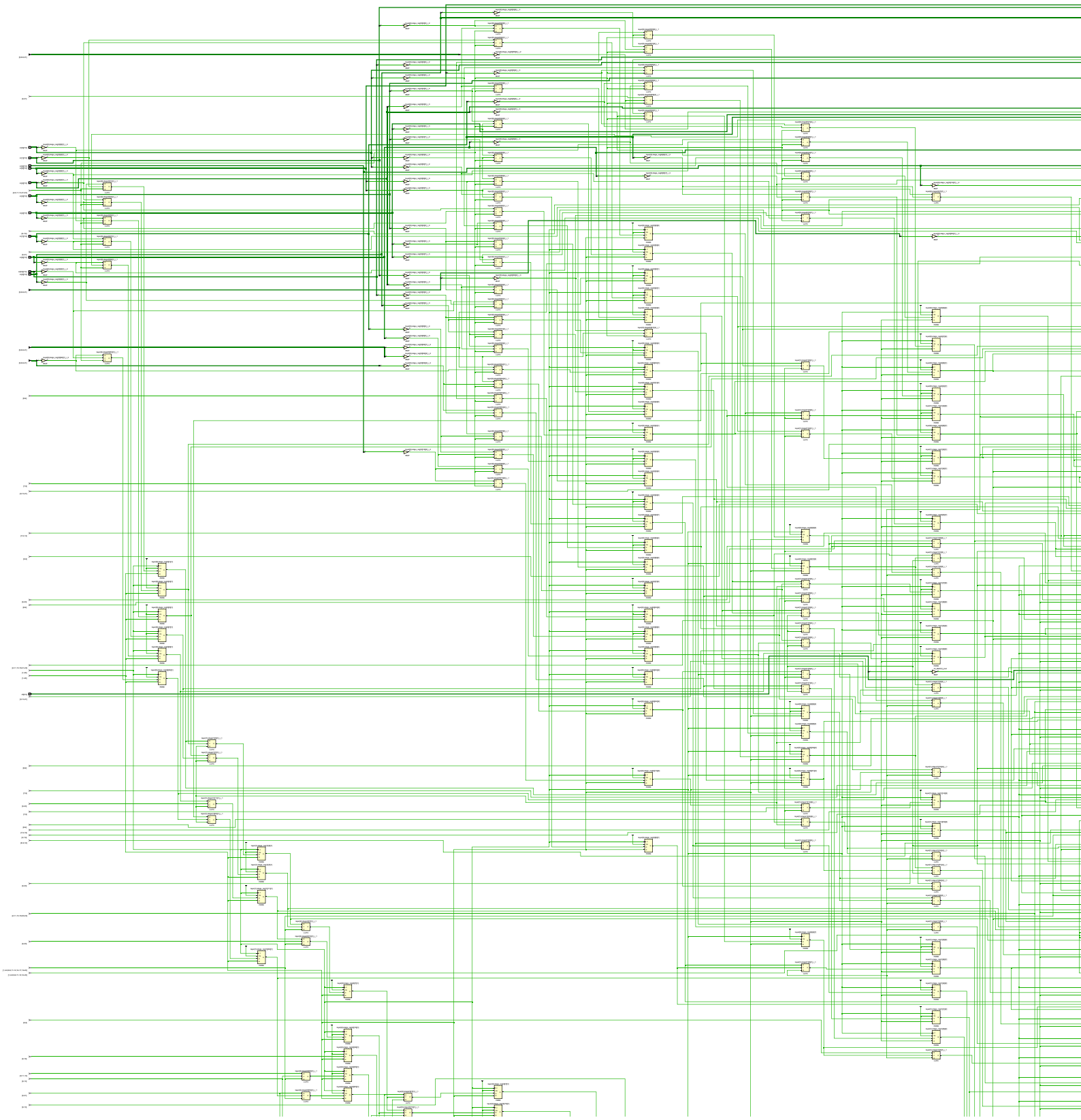


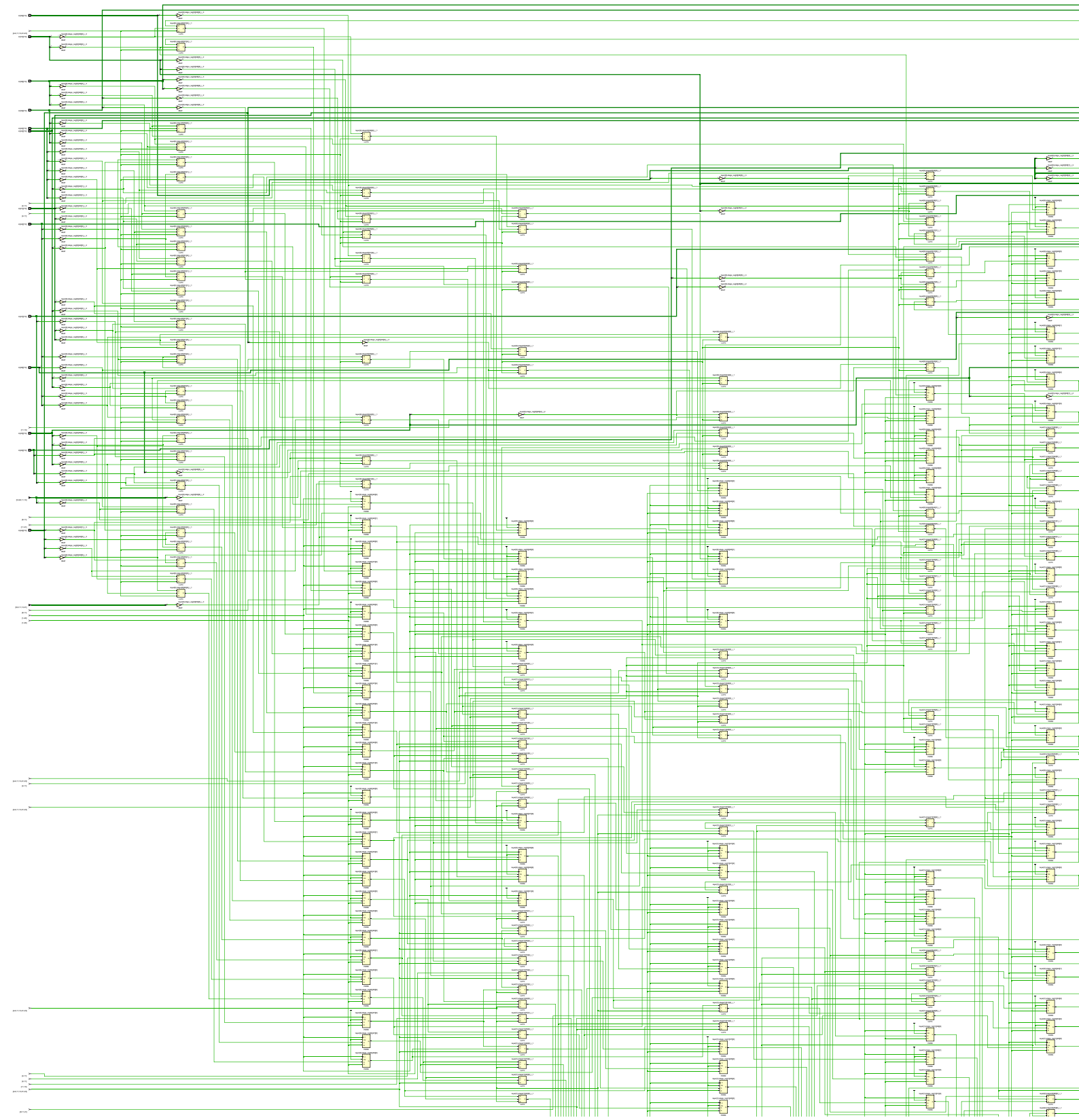


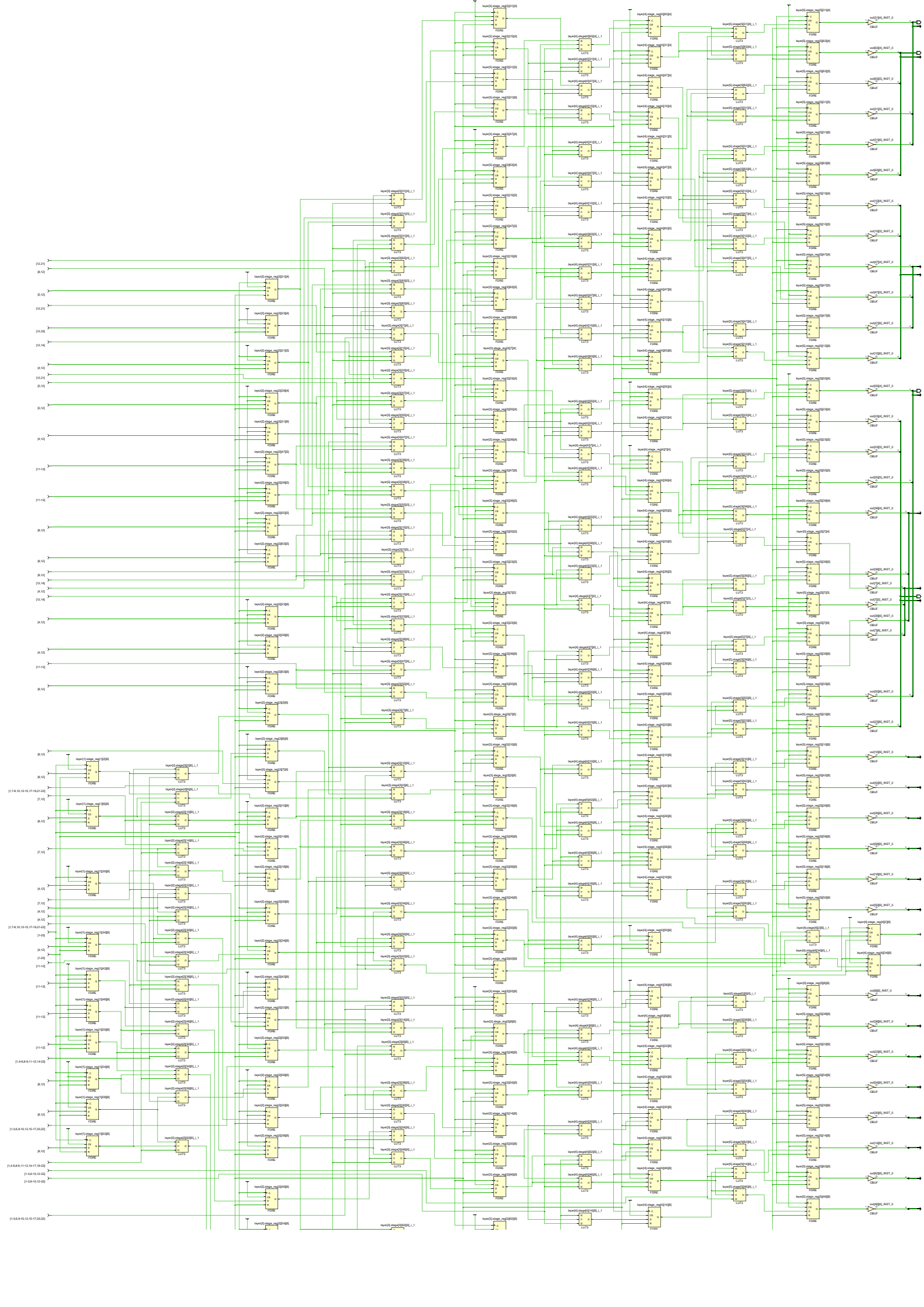


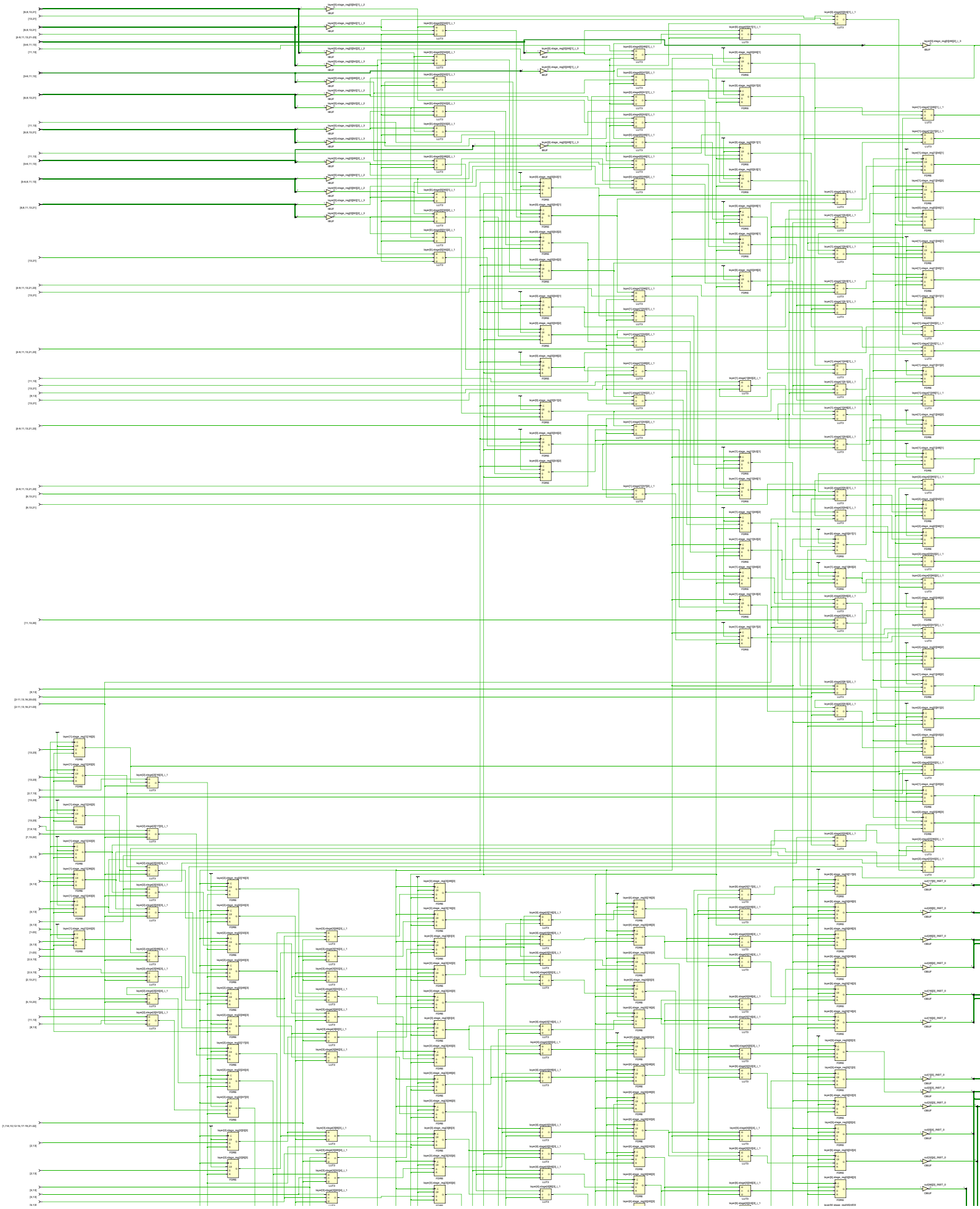


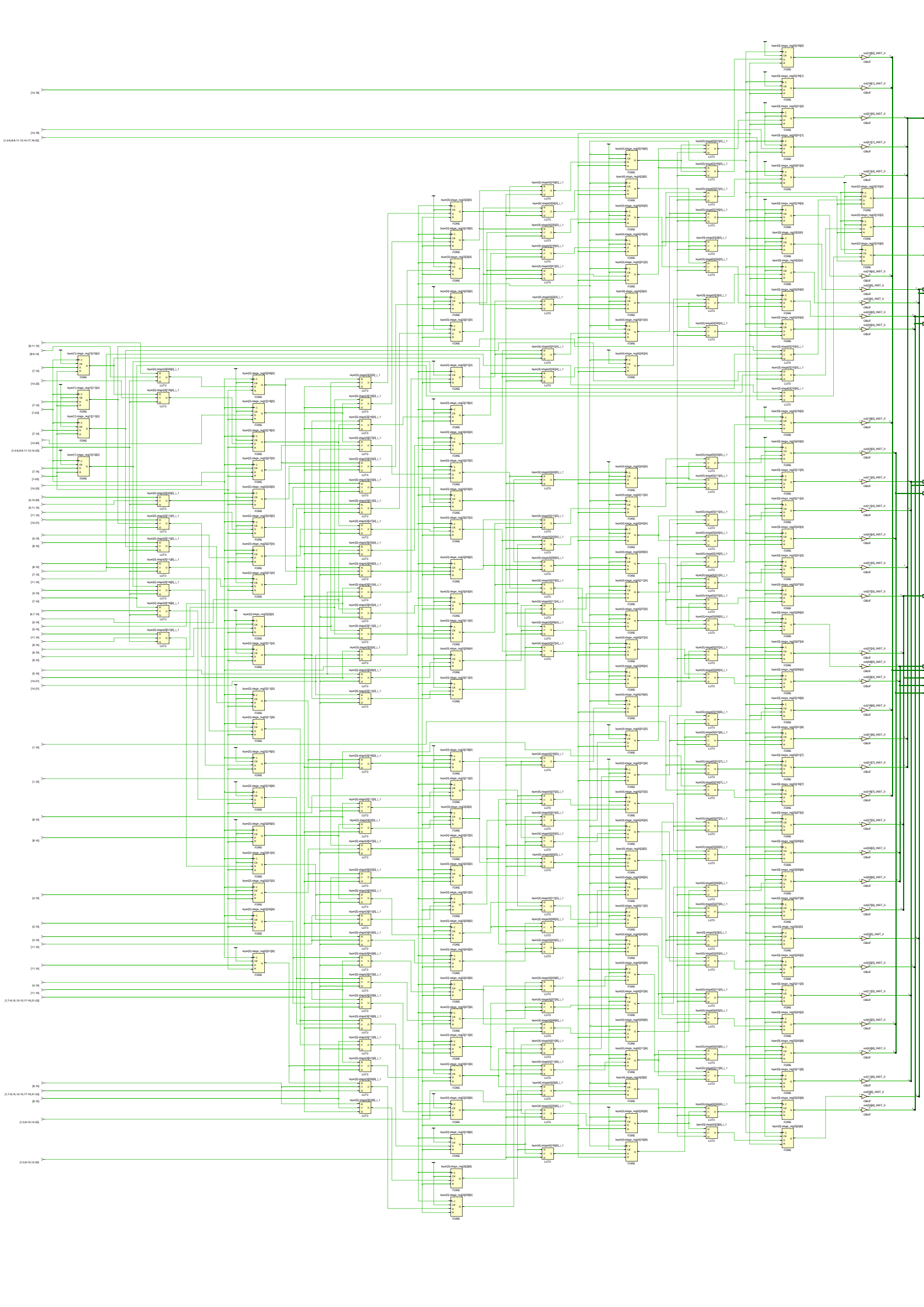


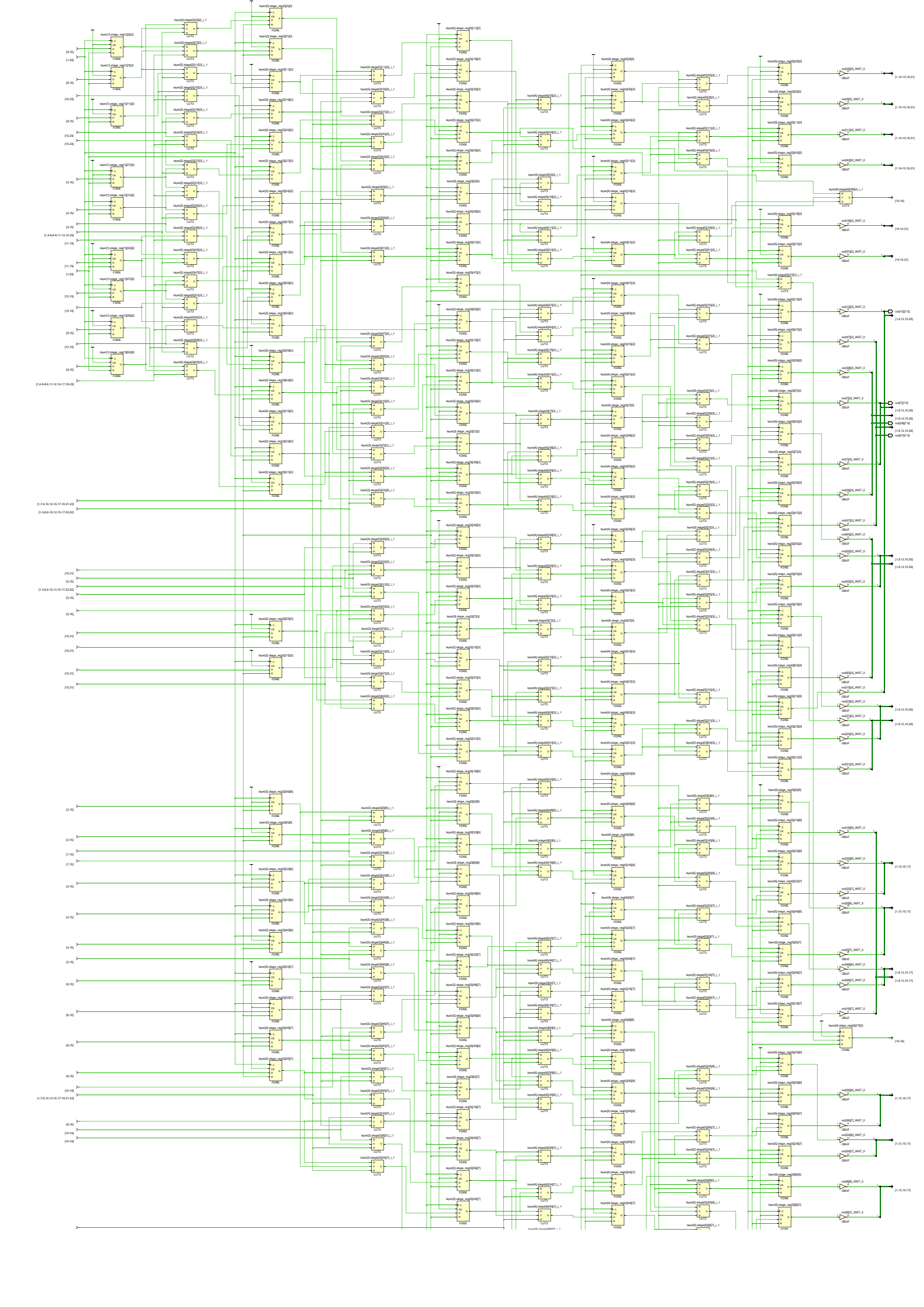


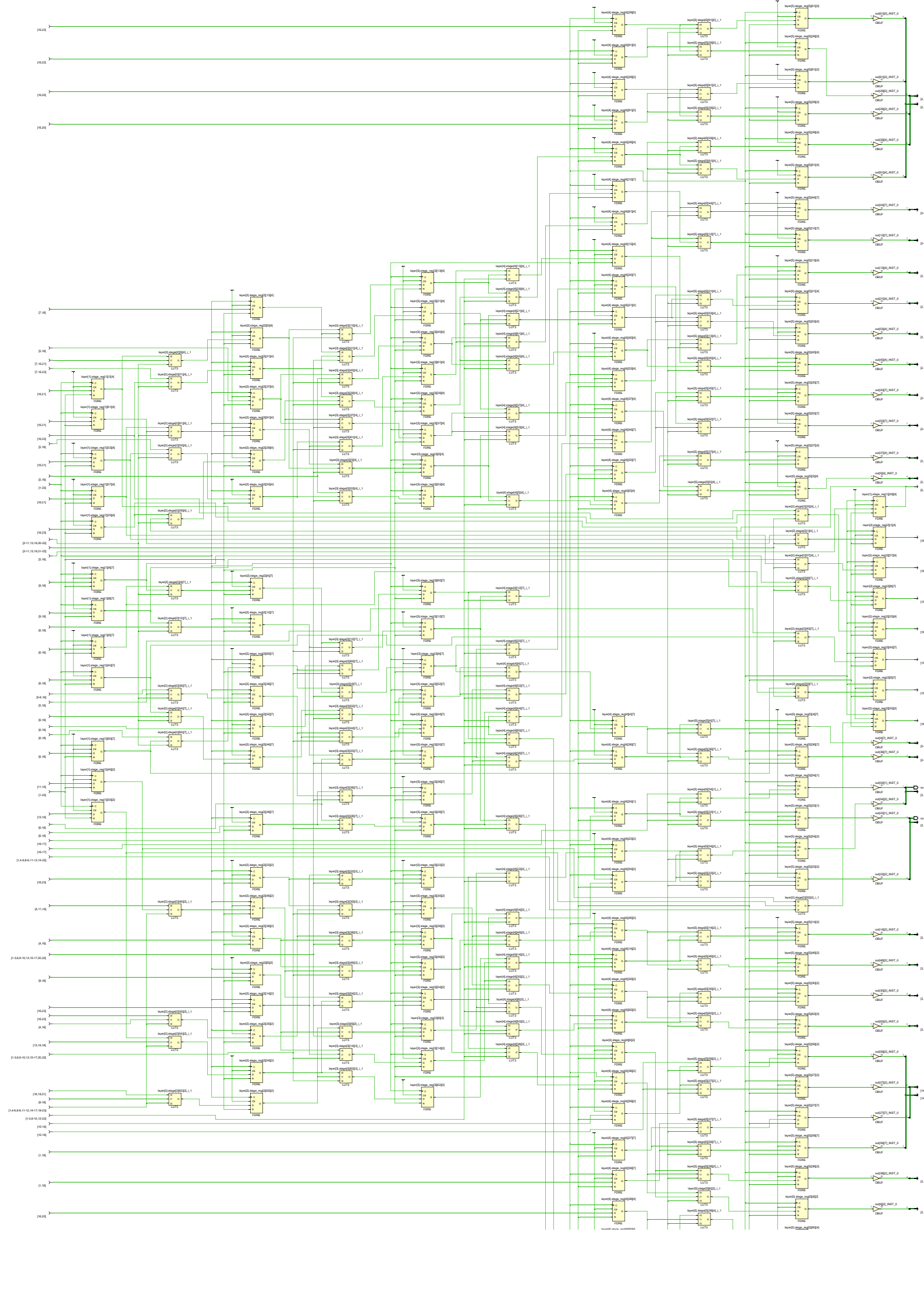


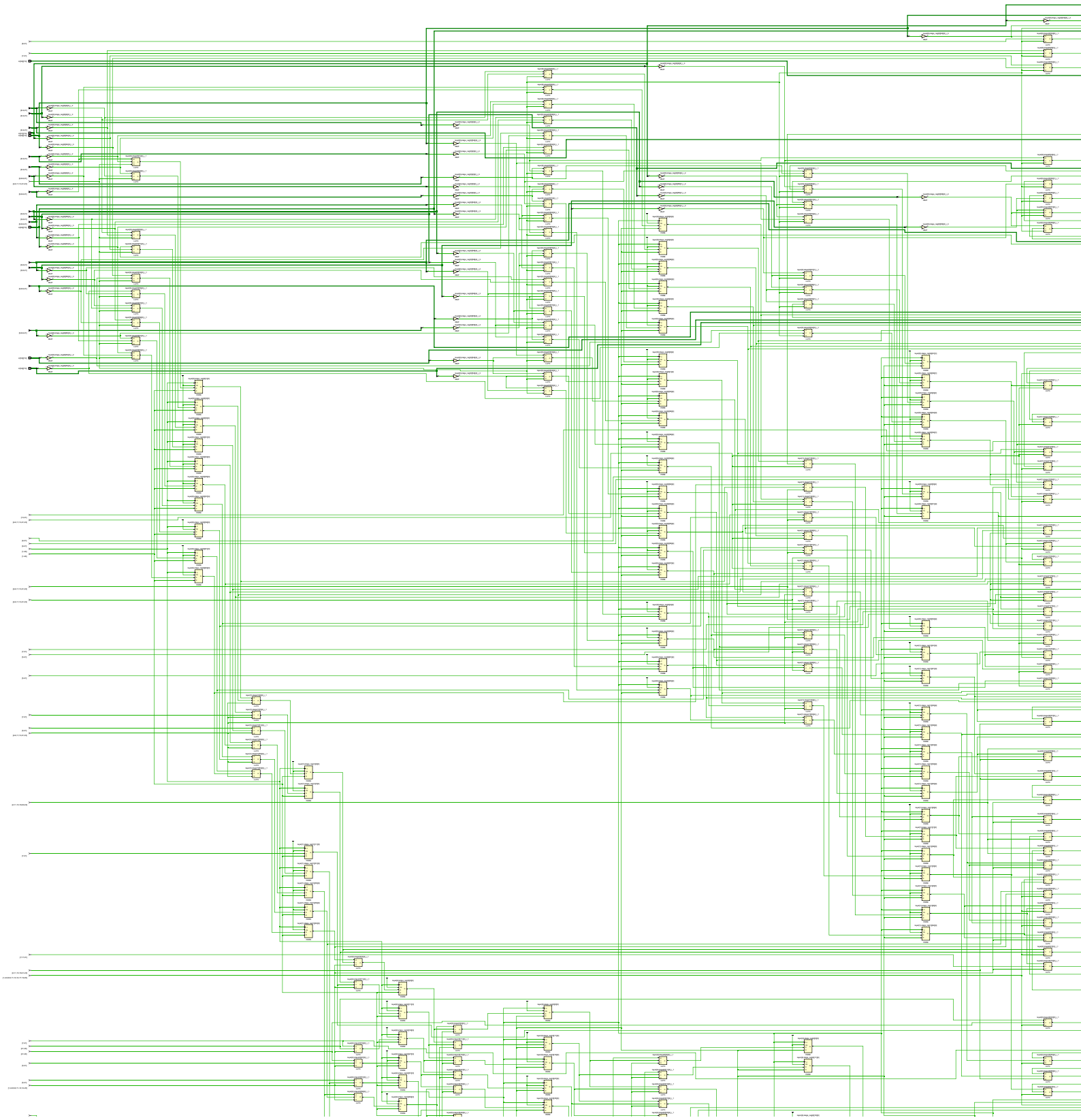


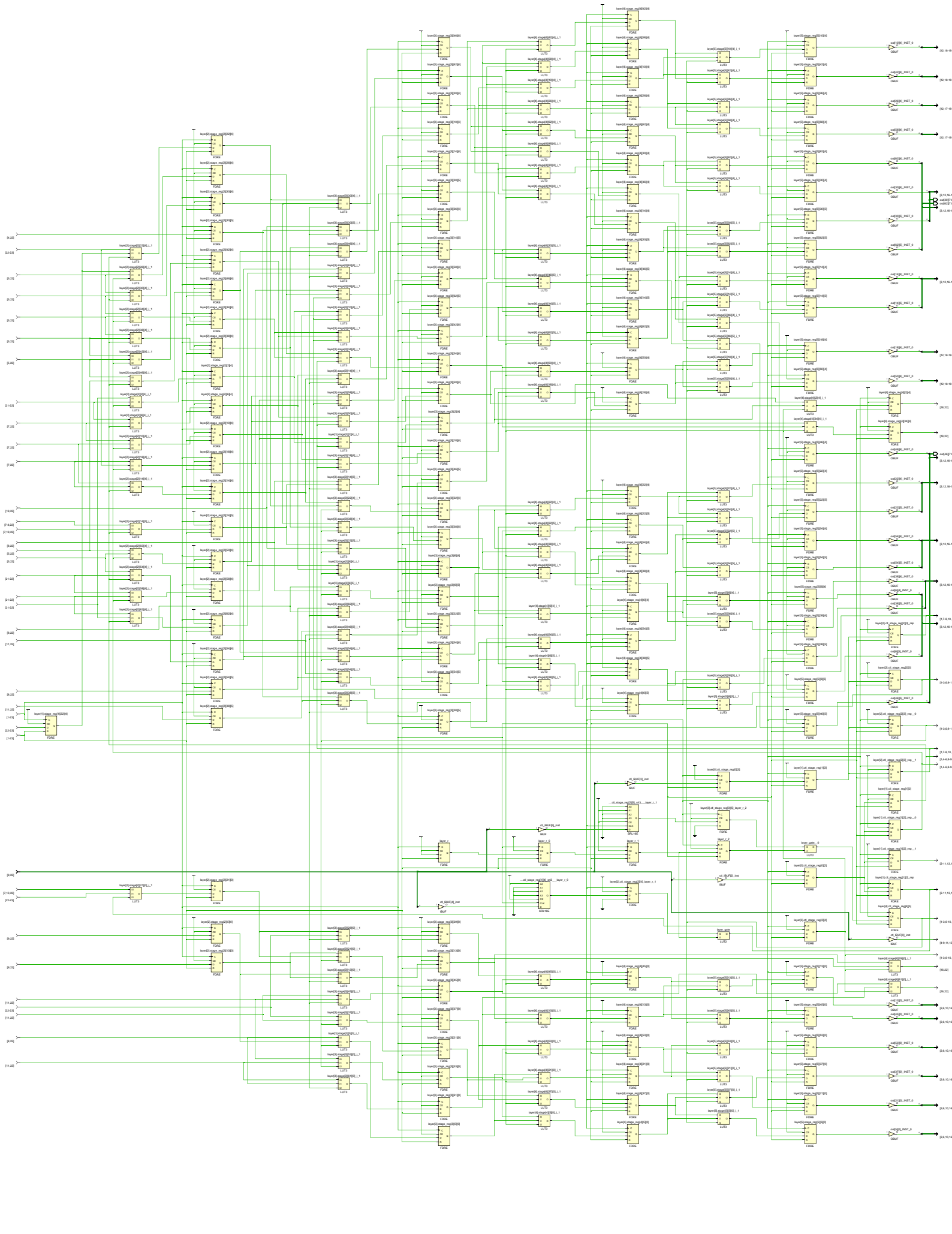


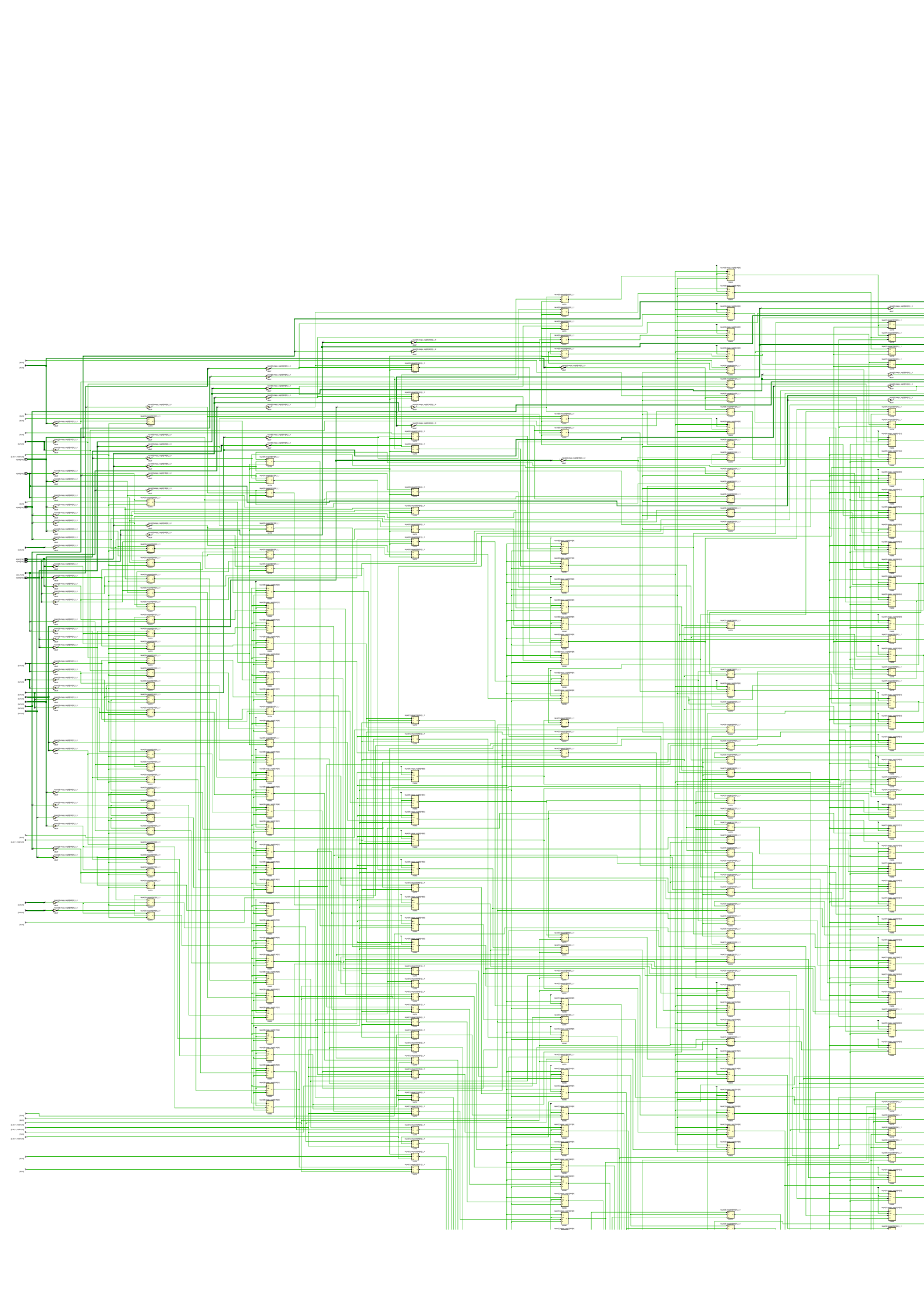




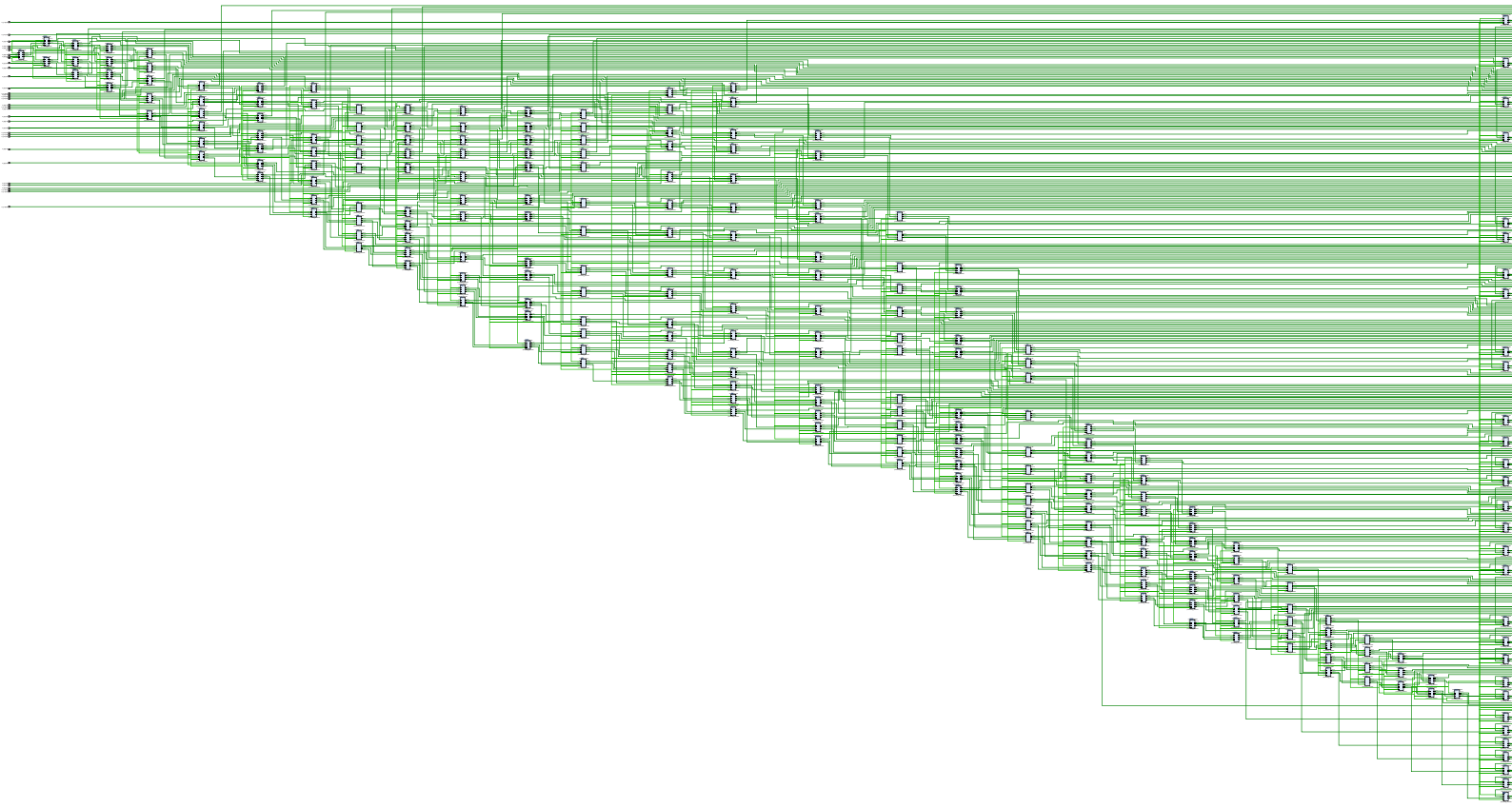








16*16 systolic array:
elaborated design



synthesized design