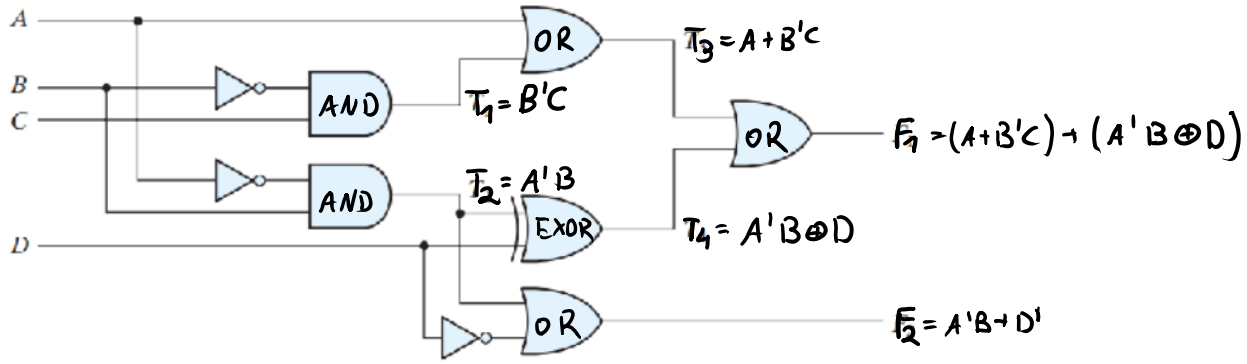
Question 1 Consider the combinational circuit shown in Fig



A) Derive the Boolean expressions for T1 through T4. Evaluate the outputs F1 and F2 as a function of the four inputs.

$$T_1 = B'C$$
$$T_2 = A'B$$
$$T_3 = A + B'C$$
$$T_4 = A'B \oplus D$$

$$F_1 = T_3 + T_4 = (A + B'C) + (A'D \oplus D)$$
$$F_2 = T_2 + D' = A'B + D'$$

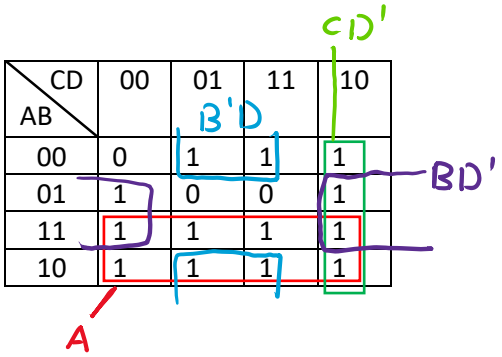
B) List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T1 through T4 and outputs F1 and F2 in the table.

No	A	B	C	D	A'	B'	D'	T_1	T_2	T_3	T_4	F_1	F_2
0	0	0	0	0	1	1	1	0	0	0	0	0	1
1	0	0	0	1	1	1	0	0	0	0	1	1	0
2	0	0	1	0	1	1	1	1	0	1	0	1	1
3	0	0	1	1	1	1	0	1	0	1	1	1	0
4	0	1	0	0	1	0	1	0	1	0	1	1	1
5	0	1	0	1	1	0	0	0	1	0	0	0	1
6	0	1	1	0	1	0	1	0	1	0	1	1	1
7	0	1	1	1	1	0	0	0	1	0	0	0	1
8	1	0	0	0	0	1	1	0	0	1	0	1	1
9	1	0	0	1	0	1	0	0	0	1	1	1	0
10	1	0	1	0	0	1	1	1	0	1	0	1	1
11	1	0	1	1	0	1	0	1	0	1	1	1	0
12	1	1	0	0	0	0	1	0	0	1	0	1	1
13	1	1	0	1	0	0	0	0	0	1	1	1	0
14	1	1	1	0	0	0	1	0	0	1	0	1	1
15	1	1	1	1	0	0	0	0	0	1	1	1	0

C) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).

$For\ the\ fucntion\ F_1$

$$F_1(A,B,C,D) = \sum m(1,2,3,4,6,8,9,10,11,12,13,14,15)$$

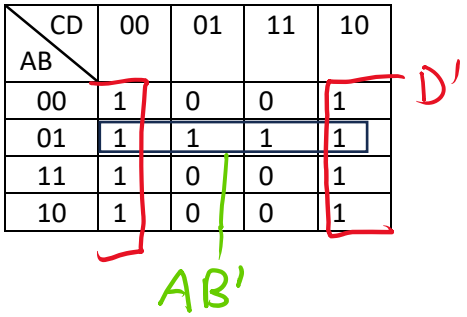


CD / AB	00	01	11	10
00	0	1	1	1
01	1	0	0	1
11	1	1	1	1
10	1	1	1	1

$$F_1(A,B,C,D) = A + BD' + B'D + CD'$$

$For\ the\ fucntion\ F_2$

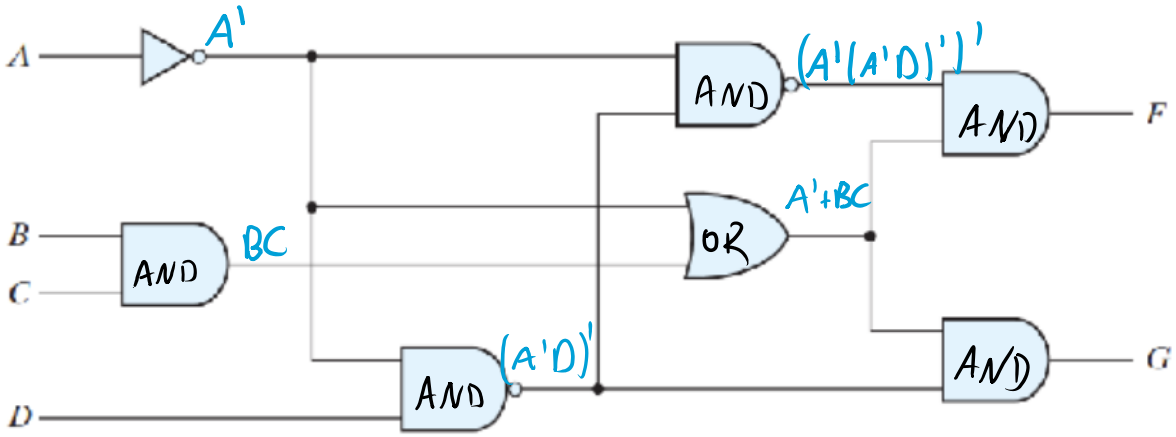
$$F_2(A,B,C,D) = \sum m(0,2,4,5,6,7,8,10,12,14)$$



CD / AB	00	01	11	10
00	1	0	0	1
01	1	1	1	1
11	1	0	0	1
10	1	0	0	1

$$F_2(A,B,C,D) = AB' + D'$$

Question 2 Obtain the simplified Boolean expressions for output F and G in terms of the input variables in the circuit of Fig.



$$F = (A' \times (A'D)')' \times (A' + BC) = (A + A'D) \times (A' + BC) = A'A + ABC + A'DA' + A'DBC =$$
$$= 0 + ABC + A'D + A'DBC = \boldsymbol{ABC + A'D + A'DBC}$$

$$G = (A' + BC) \times (A'D)' = (A' + BC) \times (A + D') = A'A + A'D' + BCA + BCD' =$$
$$= 0 + A'D' + BCA + BCD' = \textbf{A'D'+ABC +BCD'}$$

Question 3 Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise

Cosider A, B, C as inputs and Y as an output

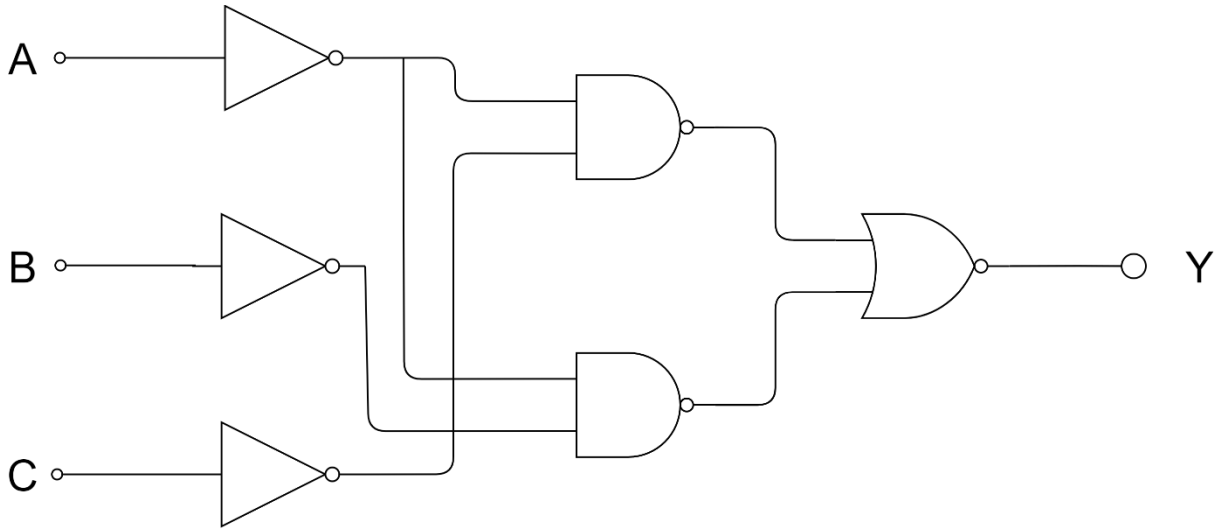
No	A	B	C	Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

$$Y(A,B,C) = \sum m(0,1,2)$$

A \ BC	00	01	11	10
0	1	1	0	1
1	0	0	0	0

$$\mathrm{Y} = \mathrm{A'B'C'} + A'B'C + A'BC'$$

$$Y = A'C' + A'B'$$



Question 4 Design a combinational circuit with three inputs, x , y , and z , and three outputs, A, B , and C . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

No	x	y	z	A	B	C
0	0	0	0	0	1	0
1	0	0	1	0	1	1
2	0	1	0	1	0	0
3	0	1	1	1	0	1
4	1	0	0	0	1	0
5	1	0	1	0	1	1
6	1	1	0	1	0	0
7	1	1	1	1	0	1

Kmap for A

x \ yz	00	01	11	10
0	0	0	1	1
1	0	0	1	1

$A = y$

Kmap for B

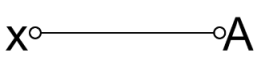
x \ yz	00	01	11	10
0	1	1	0	0
1	1	1	0	0

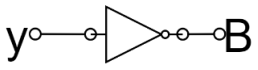
$B = y'$

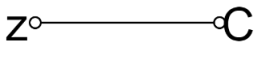
Kmap for C

x \ yz	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$C = z$





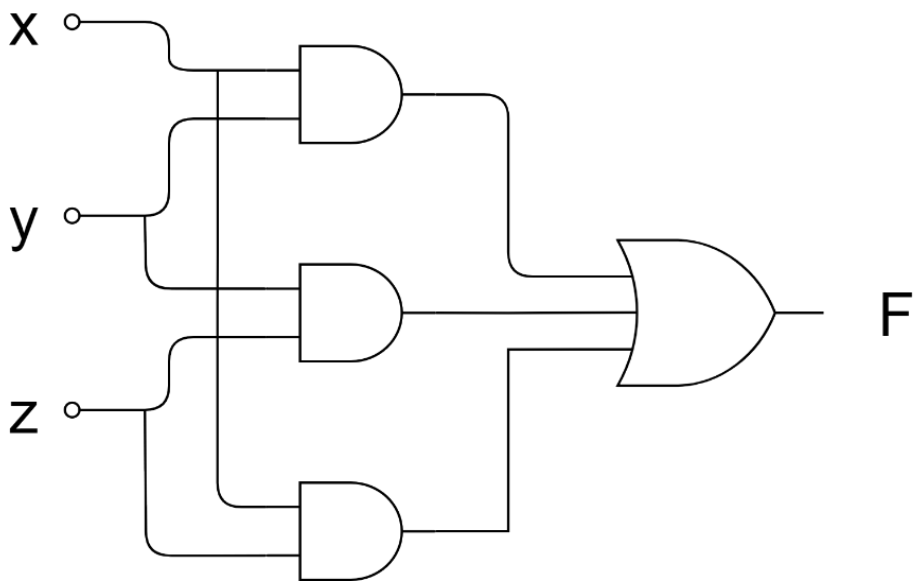


Question 5 A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram

No	x	y	z	F
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

x \ yz	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$F = yz + xz + xy$$



Question 6 Design a code converter that converts a decimal digit from 8, 4, 2, 1 (ABCD variables) code to Gray Code (wxyz variables). Draw the truth tables and K-maps for w,x,y and z of Gray code. Find the simplified form for w,x,y, and z variables

A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Kmap for w

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

$$w = B$$

Kmap for x

AB \ CD	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

$$x = \text{C}$$

Kmap for y

AB \ CD	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

$$y = D$$

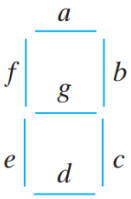
Kmap for z

AB \ CD	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$$\boldsymbol{z = C'D + CD'}$$

Question 7 An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g)

select the corresponding segments in the display, as shown in Fig. (a) . The numeric display chosen to represent the decimal digit is shown in Fig. (b) . Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display



(a) Segment designation

(b) Numerical designation for display

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

Kmap for a

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	0	0	0	0
10	1	1	0	0

$a = A'C + A'BD + AB'C' + B'C'D'$

Kmap for b

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	0	0	0	0
10	1	1	0	0

$b = A'B' + A'C'D' + A'CD + AB'C'$

Kmap for c

AB \ CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	0	0	0	0
10	1	1	0	0

$c = A'B + A'D + AB'C' + B'C'D'$

Kmap for d

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	0	0	0	0
10	1	1	0	0

$d = A'B'C + A'CD' + AB'C' + B'C'D' + A'BC'D$

Kmap for e

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	0	0	0	0
10	1	0	0	0

$e = A'CD' + B'C'D'$

Kmap for f

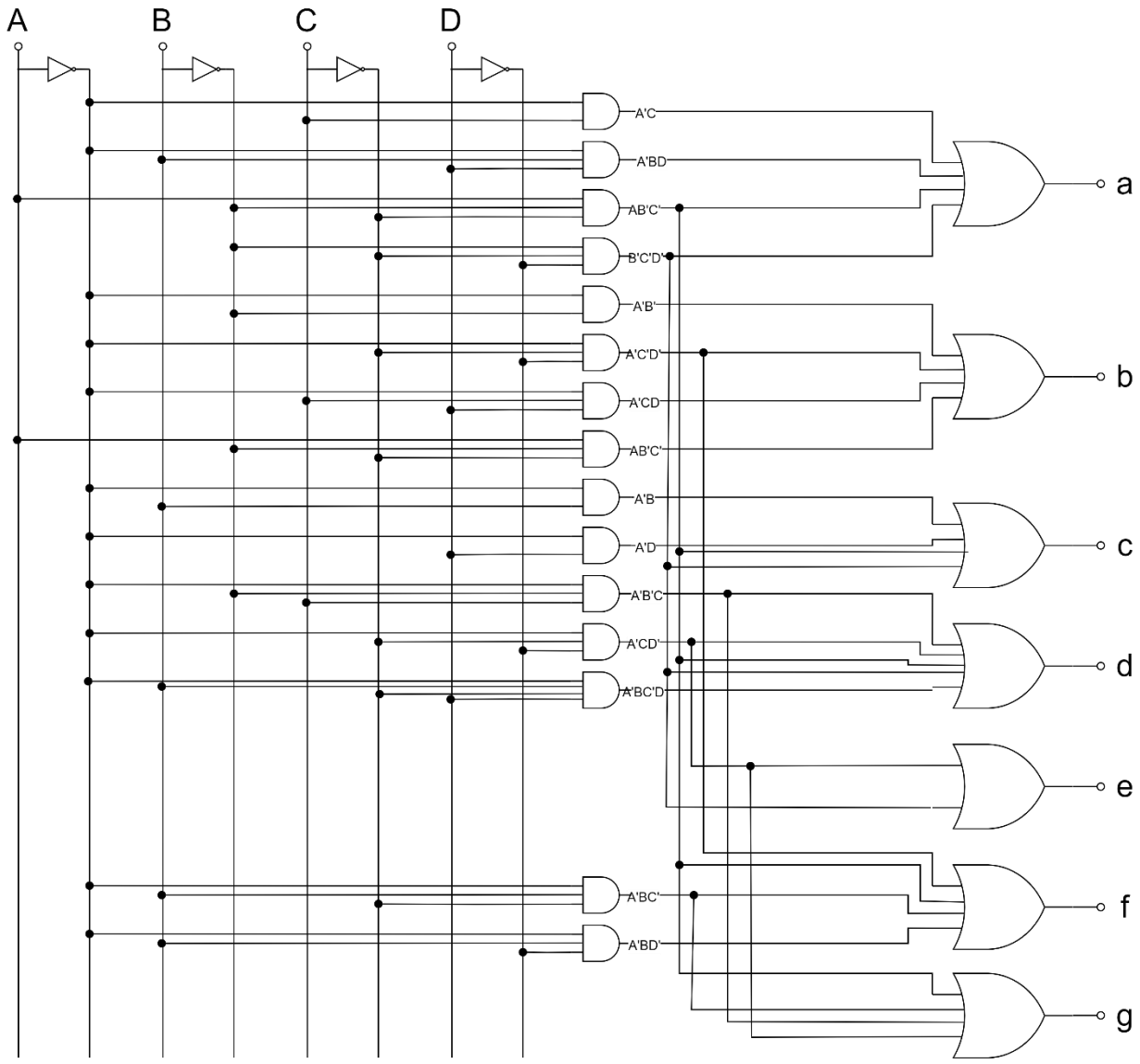
AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	0	0	0	0
10	1	1	0	0

$f = A'C'D' + AB'C' + A'BC' + A'BD'$

Kmap for g

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	0	0	0	0
10	1	1	0	0

$g = AB'C' + A'BC' + A'B'C + A'CD'$


A
B
C
D
A'C
A'BD
AB'C'
B'C'D'
A'B'
A'C'D'
A'CD
AB'C'
A'B
A'D
A'B'C
A'CD'
A'BC'D
A'BC'
A'BD'
a
b
c
d
e
f
g

Question 8 Design a four-bit

combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementer?

Binary				2's complement			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	0
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Kmap for w

CD / AB	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	0	0	0

$w = A'D + A'C + A'B + AB'C'D'$
$= A'(B + C + D) + A(B + C + D)' =$
$= \boldsymbol{A} \oplus (\boldsymbol{B} + \boldsymbol{C} + \boldsymbol{D})$

Kmap for x

CD / AB	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	1	0	0	0
10	0	1	1	1

x =BC'D'+B'D + B'C =
=B(C+D)' +B'(C+D) =
=**B**$\oplus$ $(\boldsymbol{C} + \boldsymbol{D})$

Kmap for y

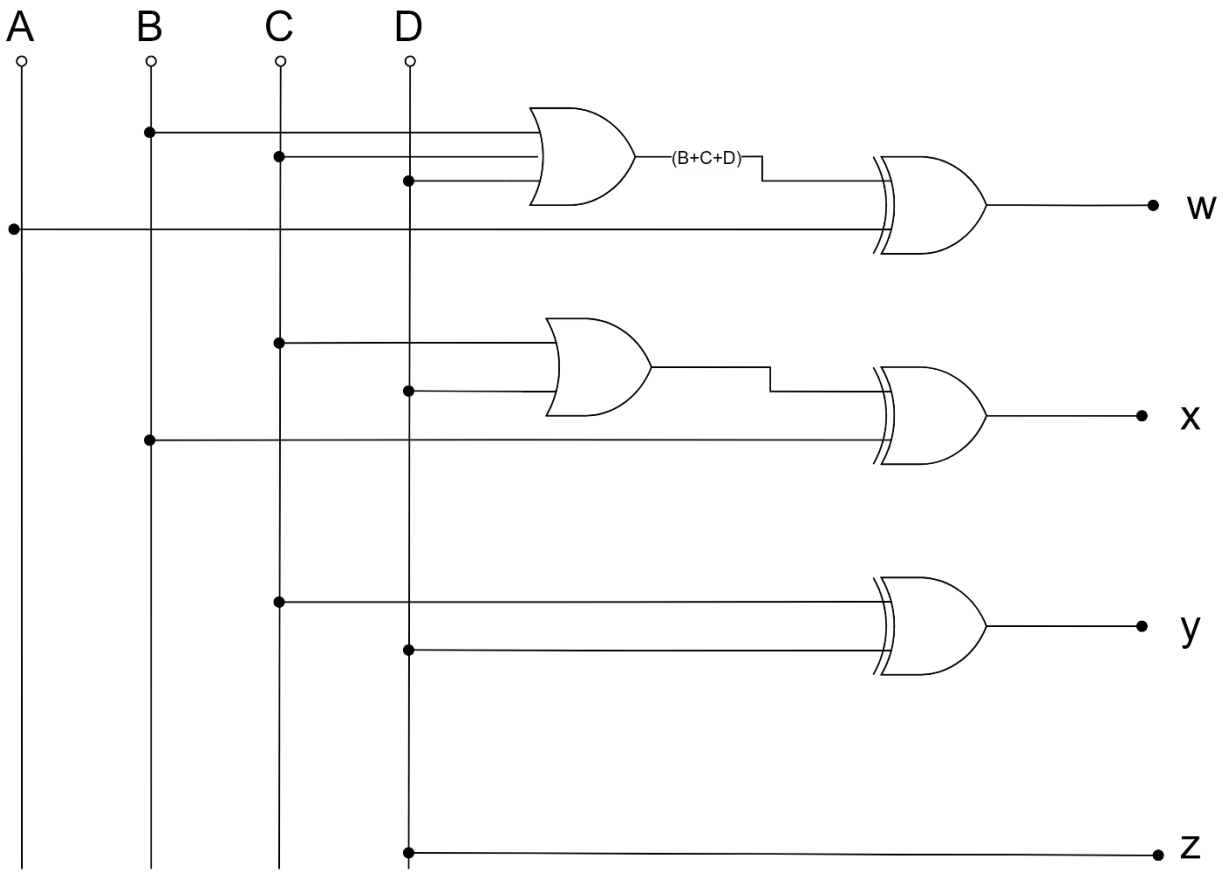
CD / AB	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$y = C'D + CD' =$
$= \boldsymbol{C} \oplus \boldsymbol{D}$

Kmap for z

CD / AB	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

$\boldsymbol{z = D}$



Logic circuits were drawn using draw.io