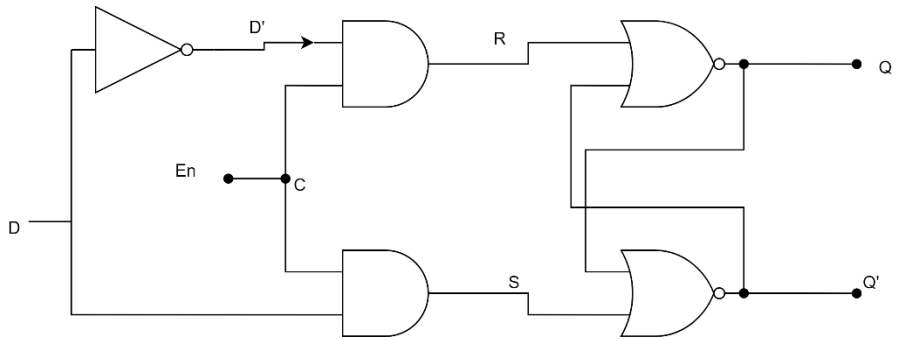
Question 1

Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.

(a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.

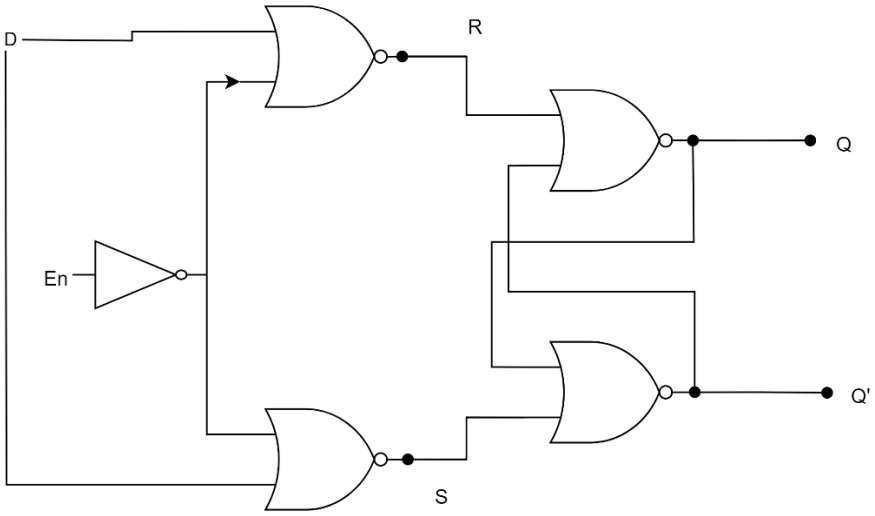


$$R = D'C$$

$$S = DC$$

En	D	Next state
0	X	No change
1	0	0 – reset state
1	1	1 – set state

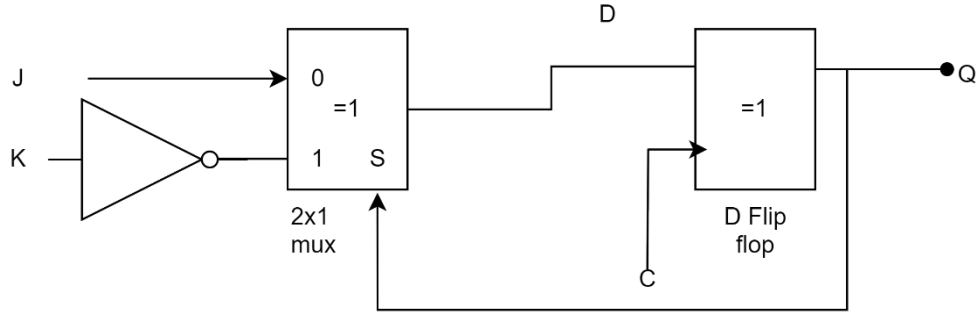
(b) Use NOR gates for all four gates. Inverters may be needed



$$R = (D + C')' = D'C$$
$$S = (D' + C') = DC$$

En	D	Next state
0	X	No change
1	0	0 – reset state
1	1	1 – set state

Question 2 Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter



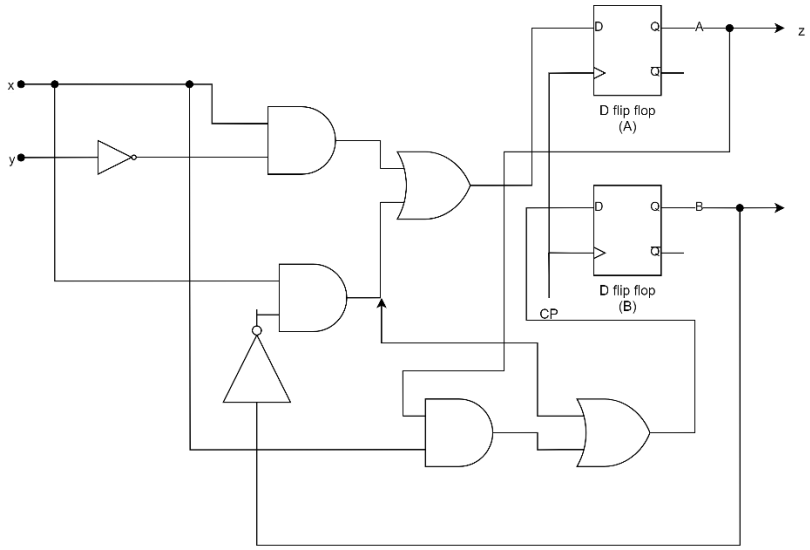
$$D = JQ' + KQ$$
$$Q_{n+1} = JQ' + KQ \Longrightarrow JK\ Flip\ flop$$

Question 3

A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified by the following next-state and output equations

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

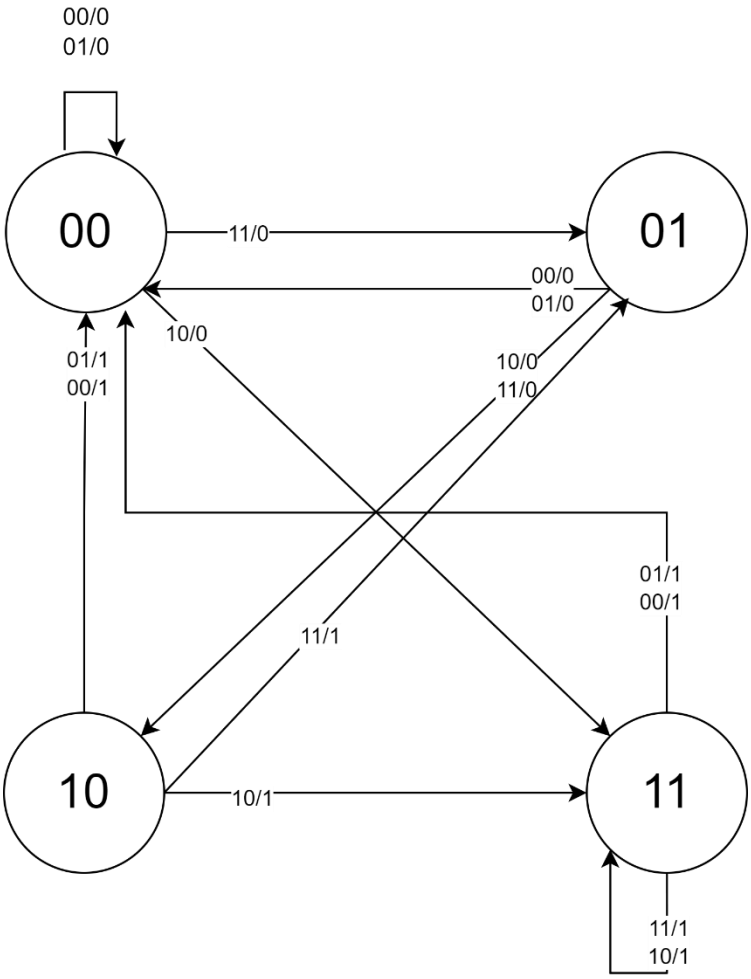
(a) Draw the logic diagram of the circuit.



(b) List the state table for the sequential circuit.

Present state		inputs		Next state		output
A(t)	B(t)	x	y	A(t+1)	B(t+1)	z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	1	1
1	0	1	1	0	1	1
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

(c) Draw the corresponding state diagram.



Question 4

A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations:

$$J_A = x \quad K_A = B$$
$$J_B = x \quad K_B = A'$$

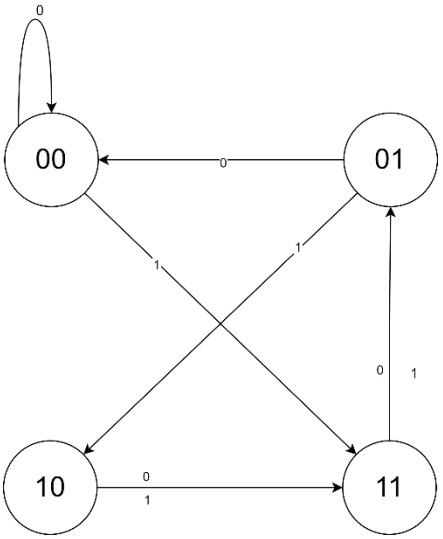
(a) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables.

$$Q(t+1) = JQ' + K'Q$$

$$A(t+1) = J_A Q' + K_A' Q = xA' + B'A$$
$$B(t+1) = J_B Q' + K_B' Q = xB' + AB$$

(b) Draw the state diagram of the circuit.

Present state		Input	Next state	
A	B	x	A(t+1)	B(t+1)
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	1
1	1	0	0	1
1	1	1	0	1



Question 5

The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift

	0	0	1	1	1	0
0110	0011	0001	1000	1100	1110	0111