LABORATORY WORK # 5

MULTIPLEXER, DEMULTIPLEXER AND BINARY COMPARATOR

Aims: investigate multiplexer, demultiplexer and binary comparator operation; make examples of data selection, data transfer and data comparison according to the task. Compare the results with ones, made by theoretical way.

PREPARATION TO LAB WORK

1. Learn the information about multiplexer, demultiplexer and binary comparator.
2. Consider experiment's schemes and analyze their operation. Draw them using Scheme Design System.
3. Fill in the tables theoretically.
4. Draw the scheme which is suitable to define if 4-bit binary number A is equal to the 4-bit binary number B or not (use Scheme Design System).
5. Show the principal scheme of 2*4 decoder with application of Scheme Design System.
6. Answer the questions below in written form.
   6.1. What is magnitude comparator?
   6.2. How many output signals may exist for magnitude comparator simultaneously and why?
   6.3. Why A<B, A>B inputs of the first 7485 must be grounded, and A=B input must be HIGH?
   6.4. What are a decoder and DUX, show differences?
   6.5. What is functionality of enable input of a decoder?
   6.6. What is an encoder?
   6.7. What is a priority encoder?
   6.8. Compare decoder and encoder.
   6.9. What is a MUX?
   6.10. How many functions can a MUX realize?
   6.11. What is a role of a MUX's selection lines?
   6.12. Compare DUX and MUX.

LAB WORK PERFORMANCE

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 5.1 on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4 – 6 for the experiments 5.2 through 5.4.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, and clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

EXPERIMENT 5.1 EXPERIMENT OF 8 X 1 MULTIPLEXER (MUX)

Equipments Used in the Experiment:

1- Y-0016 main unit

2- Y-0016-009D module

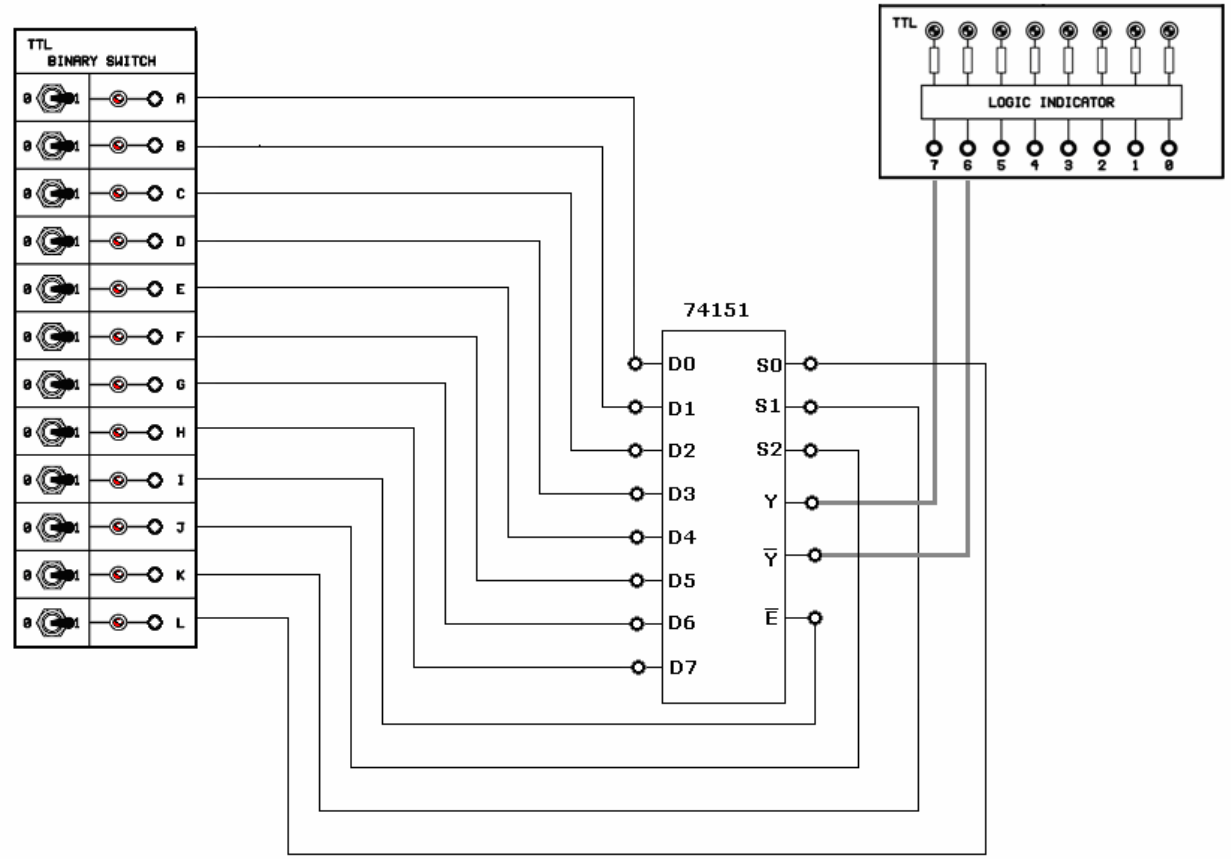


Figure 5.1

Experimental Work:

1. Connect the circuit as shown in figure 5.1 and apply the power.
2. Apply the inputs given in Table 5.1 using the switches. Use one of the following input combinations provided by your instructor for **D0-D7 inputs**: **a) 10110010; b) 01010101; c) 00011100; d) 11101110**. Observe the Y and Y' outputs from LED display and note them on the table 8.1
3. Have the inputs been transferred to the output Y?

DATA SELECT			**E'**	**INPUTS**								**OUTPUTS**	
S2	**S1**	**S0**		**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**Y**	**Y'**
X	X	X	1	X	X	X	X	X	X	X	X		
0	0	0	0										
0	0	1	0										
0	1	0	0										
0	1	1	0										
1	0	0	0										
1	0	1	0										
1	1	0	0										
1	1	1	0										

Table 5.1

EXPERIMENT 5.2 EXPERIMENT OF 1 X 8 DE-MULTIPLEXER (DUX)

Equipments Used in the Experiment:

1- Y-0016 main unit

2- Y-0016-009D module

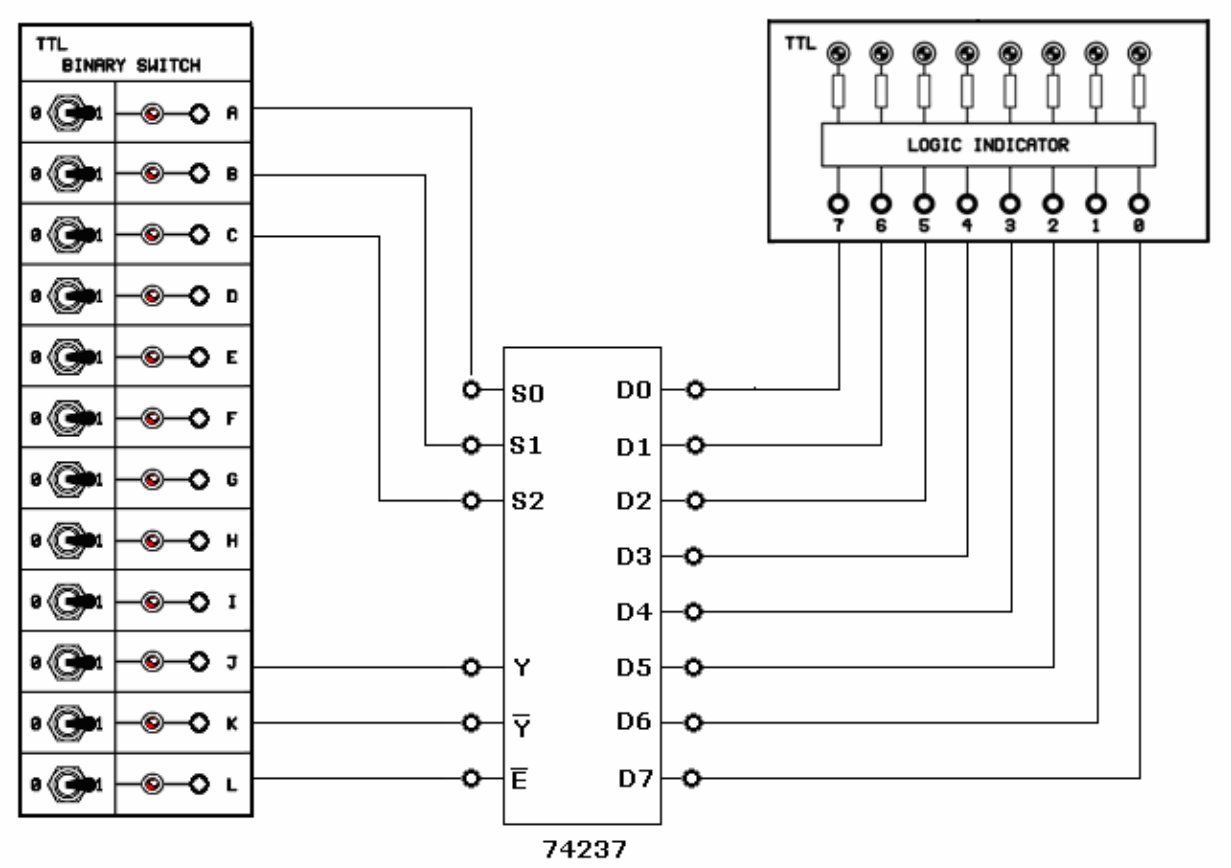


Figure 5.2

Experimental Work:

1. Connect the circuit as shown in figure 5.2 and apply the power.
2. Apply the inputs given in Table 5.2 using the switches. Observe the D outputs from LED display and note them on the table 5.2
3. Have the input Y been transferred to the outputs D0-D7?

INPUTS						**OUTPUTS**							
S2	**S1**	**S0**	**E'**	**Y**	**Y'**	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
0	0	0	0	1	0								
0	0	1	0	1	0								
0	1	0	0	1	0								
0	1	1	0	1	0								
1	0	0	0	1	0								
1	0	1	0	1	0								
1	1	0	0	1	0								
1	1	1	0	1	0								

Table 5.2

EXPERIMENT 5.3 EXPERIMENT OF DATA TRANSFER GATE (MUX-DUX COMBINATION)
Equipments Used in the Experiment:
1- Y-0016 main unit
2- Y-0016-009D module

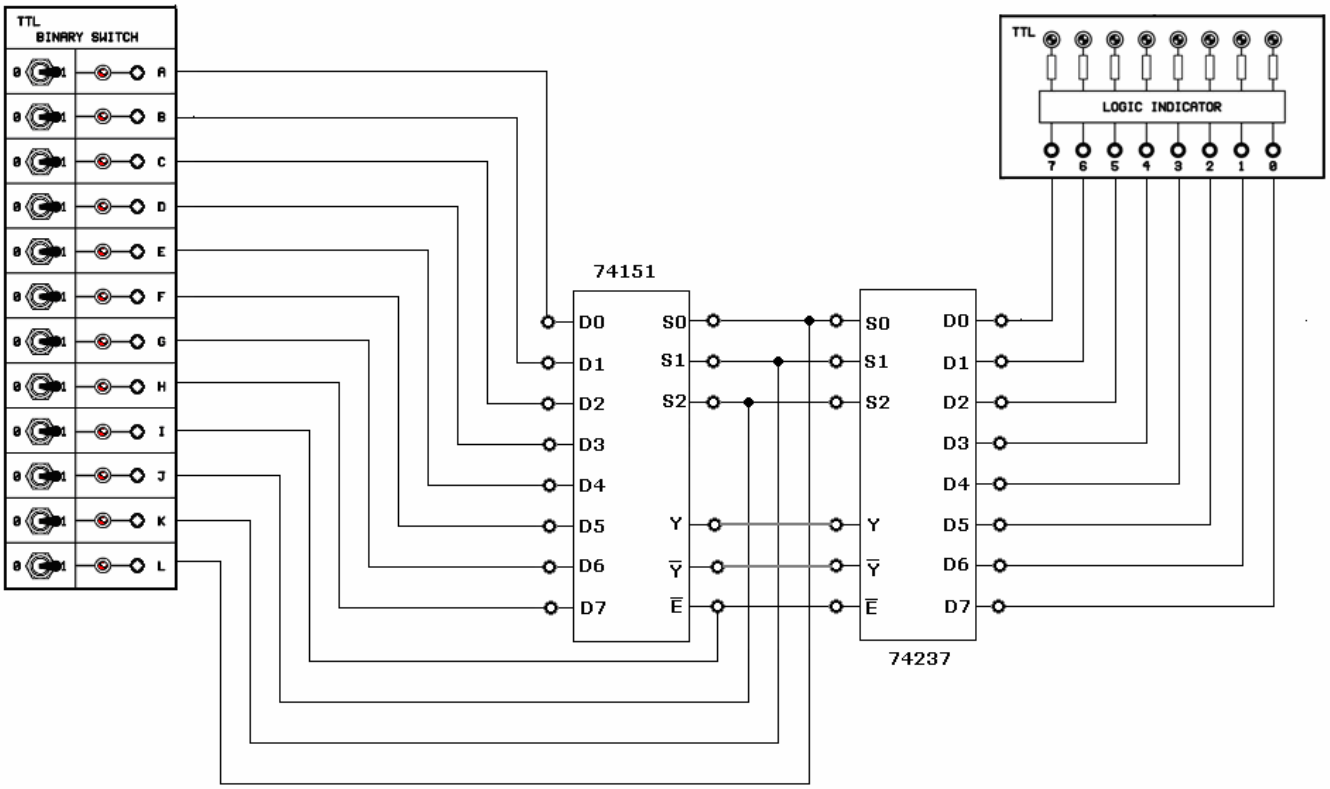


Figure 5.3

Experimental Work:
1. Connect the circuit as given in figure 5.3 and apply the power.
2. Apply the inputs given in table 5.3 using the switches. Use one of the following input combinations provided by your instructor for **D0-D7 inputs**: **a) 10110010; b) 01010101; c) 00011100; d) 11101110**. Fill in the table 8.3 by observing outputs D0-D7 from LED display.

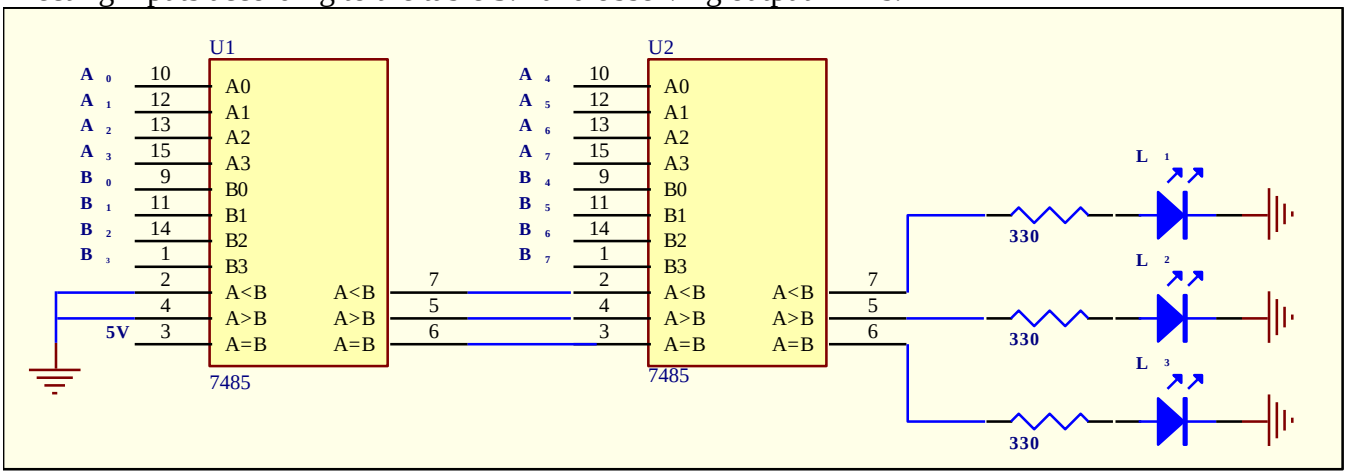
NOTE: Don't forget to combine the pins S0-S1-S2 and E'; so that the ICs will operate synchronously.

3. Have the data at the input been transferred to the output?

MUX & DUX INPUTS				DATA INPUTS								DATA OUTPUTS							
S2	S1	S0	E'	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0																
0	0	1	0																
0	1	0	0																
0	1	1	0																
1	0	0	0																
1	0	1	0																
1	1	0	0																
1	1	1	0																

Table 5.3

Experiment 5.4 Prepare the circuit on the breadboard. Do not forget to connect pin 8 of the 7485 chip to the GROUND and pin 16 to VCC. Apply the signals according to the table below. Fill in the table 5.4 by connecting inputs according to the table 5.4 and observing output LEDs.



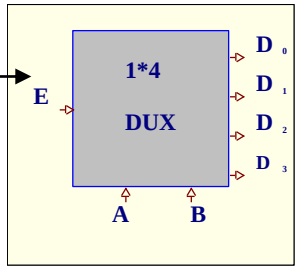
Inputs																outputs		
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	A<B	A>B	A=B
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0			
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1			
0	1	1	0	1	1	0	0	0	1	1	0	0	1	0	0			
0	1	1	0	1	1	0	0	1	1	1	0	0	1	0	0			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1			

Table 5.4

TEST QUESTIONS

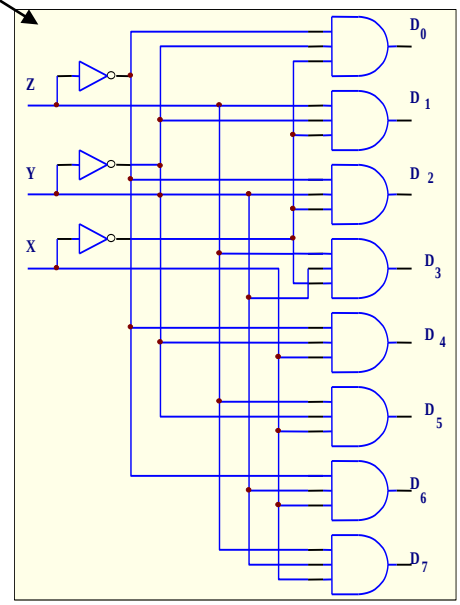
1. A decoder is a combinatioal circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

2. Output of 1*4 demultiplexer is D_1. What are selection lines?
A. 00 B. 01 C. 10 D. 11 E. any of them

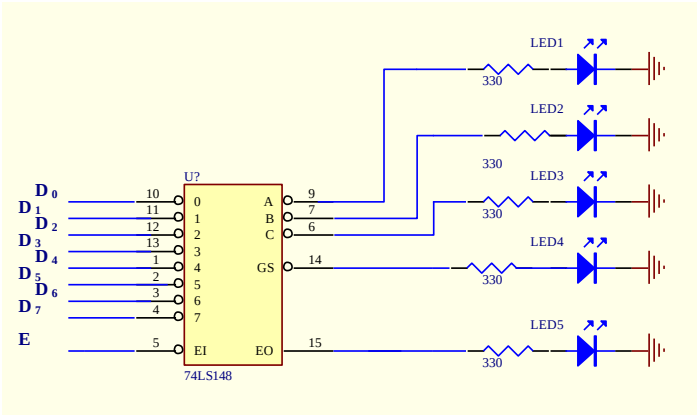


3. What signals for XYZ inputs are applied if active output is D_0?
A.0, 0, 0 B. 0, 1, 1 C. 1, 0, 0 D. 0, 1, 0 E. 0, 0, 1

4. DUX sometimes is called
A. code converter B. data selector C. data distributor
D. decoder E. all answers are correct



5. For the circuit below if EI=5V, D1=0, D5=0 the state of L1 to L5 will be

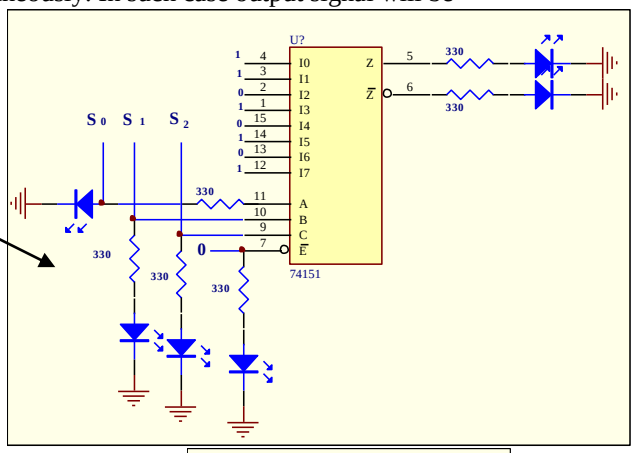


A. ON,ON,ON,ON,ON B. OFF,OFF,OFF,ON,ON
C. ON,ON,ON,OFF,OFF D. OFF,OFF, ON,ON,ON,
E. OFF, ON,ON,ON, OFF

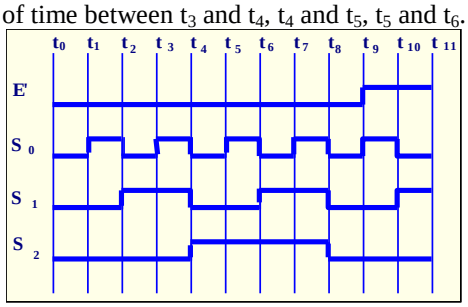
6. For priority encoder we have got input lines D_1, D_3, and D_6 active simultaneously. In such case output signal will be corresponded to … A. D_1 B. D_3 C. D_6 D. D_1or D_3 E. D_3 or D_6

7. Decoder is _____ component.
A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

8. For the circuit below if selection lines $S_2S_1S_0$=011 the output Z will be ____, if $S_2S_1S_0$=100, Z will be ____, if $S_2S_1S_0$=001, Z will be ____.
A. 1,1,0 B. 0,1,1 C. 1,1,1 D. 0,1,0 E.1,0,1



9. For the circuit in question 8 the output Z is equal to _____ for periods of time between t_3 and t_4, t_4 and t_5, t_5 and t_6.



A. 0,1,1 B. 0,1,0 C. 1,1,1 D. 0,0,1 E. 1,0,1

10. What function is implemented with multiplexer?
A. F(A,B,C,D)= Σ(0,1,3,4,5,8,15) B. F(A,B,C,D)= Σ(0,1,3,4,7,14)
C. F(A,B,C,D)= Σ(0,1,3,4,8,15) D. F(A,B,C,D)= Σ(0,1,3,4,8,9,15)
E. F(A,B,C,D)= Σ(0,1,3,5,7,14,15)