COMPUTER ORGANIZATION AND ARCHITECTURE

SYLLABUS and SCHEME

Course Code	Course Title							
116U01C303	Computer Organization and Architecture							
	TH		P		TUT		Total	
Teaching Scheme(Hrs.)	03		02		--		05	
Credits Assigned	03		01		--		04	
Examination Scheme	Marks							
	CA		ESE	TW	O	P	P&O	Total
	ISE	IA						
	30	20	50	25	25	--	--	150

Course prerequisites: Students should be familiar with basic concepts of computers and their applications.

Course Objectives:

Students will try to:

1. Conceptualize the basics of organization and architecture of a digital computer and the detailed working of the ALU
2. Learn the function of each element of a memory hierarchy and detailed working of the control unit
3. Study various input output techniques and their applications.

Course Outcomes:

After completing this course, students will be able to:

CO1- Describe and define the structure of a computer with buses structure and detail working of the arithmetic logic unit and its sub modules

CO2- Understand the Central processing unit with addressing modes and working of control unit in depth

CO3- Learn and evaluate memory organization and cache structure

CO4- Summarize Input output techniques and multiprocessor configurations

Module No.	Unit No.	Details of Topic	Hrs.	CO
1.0		**Structure of a Computer System**	04	CO1
	1.1	Introduction of computer system and its sub modules, Basic organization of computer and block level description of the functional units. Von Neumann model		
	1.2	Introduction to buses, bus types, and connection I/O devices to CPU and memory, PCI and SCSI		
2.0		**Arithmetic and Logic Unit**	11	CO1
	2.1	Introduction to Arithmetic and Logical unit, Computer Arithmetic: Fixed and Floating point numbers, Signed numbers, Integer Arithmetic, 2's Complement arithmetic		
	2.2	Booth's Recoding and Booth's algorithm for signed multiplication, Restoring division and non-restoring division algorithms		
	2.3	IEEE floating point number representation and operations: Addition, Subtraction, Multiplication and Division. IEEE standards for Floating point representations :Single Precision and Double precision Format		
3.0		**Central Processing Unit**	10	CO2
	3.1	CPU architecture, Register organization, Instruction formats and addressing modes (Intel processor), Basic instruction cycle. Control unit Operation ,Micro operations : Fetch, Indirect, Interrupt , Execute cycle Control of the processor, Functioning of micro programmed control unit, Micro instruction Execution and Sequencing, Applications of Micro programming		
	3.2	RISC v/s CISC processors, RISC and CISC Architecture, RISC pipelining, Case study on SPARC		
4.0		**Memory Organization.**	11	CO3
	4.1	Characteristics of memory system and hierarchy, Main memory, Cache memory principles , Elements of Cache Design		
	4.2	ROM, Types of ROM, RAM, SRAM, DRAM, Flash memory, High speed memories		
	4.3	Cache Memory Organization: Address mapping, Replacement Algorithms, Cache Coherence, MESI protocol, Interleaved and associative memories, Virtual memory, Main memory allocation, Segmentation ,Paging, Secondary storage, RAID levels		
5.0		**I/O Organization**	03	CO4
	5.1	External Devices, I/ O Modules		
	5.2	Programmed I/O, Interrupt driven I/O, DMA		
6.0		**Multiprocessor Configurations**	06	CO4
	6.1	Flynn's classification, Parallel processing systems and concepts		
	6.2	Introduction to pipeline processing and pipeline hazards		
	6.3	Design issues of pipeline architecture, Instruction pipelining: Six Stage instruction pipeline		
	6.4	8086 Instruction (Arithmetic Instructions, Logical Instructions, Data transfer instructions)		
		Self-Learning: Pin Diagram of 8086, Minimum Mode and Maximum mode with timing diagram		
		Total	**45**	

Recommended Books:

Sr. No.	Name/s of Author/s	Title of Book	Name of Publisher with country	Edition and Year of Publication
1.	W.Stallings William	*Computer Organization and Architecture:*	Pearson Prentice Hall	7th Edition

Module 1

1	Structure of a Computer System		0 4	CO1
	1.1	Introduction of computer system and its sub modules, Basic organization of computer , Structure and Function, Brief history of computers, Von Neumann model		
	1.2	Introduction to buses, bus types and interconnection structures, PCI and SCSI bus		

Module 2

2	**Arithmetic and Logic Unit**		**10**	**CO1**
	2.1	Introduction to Arithmetic and Logical unit, Computer Arithmetic: Fixed and Floating point numbers, Signed numbers, Integer Arithmetic, 2's Complement arithmetic		
	2.2	Booth's Recoding and Booth's algorithm for signed multiplication, Restoring division and non-restoring division algorithms		
	2.3	IEEE floating point number representation and operations: Addition. Subtraction, Multiplication and Division. IEEE standards for Floating point representations :Single Precision and Double precision Format		

Module 3

3	**Central Processing Unit**		**11**	**CO2**
	3.1	CPU architecture, Register organization, Instruction Sets: Operands and Operations , Instruction formats and addressing modes(Intel processor).,Basic instruction cycle, Instruction interpretation and sequencing		
	3.2	Control unit Operation ,Micro operations : Fetch ,Indirect ,Interrupt ,Execute cycle Control of the processor, Functioning of micro programmed control unit, Micro instruction Execution and Sequencing , Applications of Micro programming		
	3.3	RISC v/s CISC processors, RISC and CISC Architecture, RISC pipelining, Case study on SPARC		

Module 4

4	**Memory Organization.**		**11**	**CO3**
	4.1	Characteristics of memory system and hierarchy, Main memory ,Cache memory principles , Elements of Cache Design		
	4.2	ROM, Types of ROM, RAM, SRAM, DRAM, Flash memory, High speed memories		
	4.3	Cache Memory Organization: Address mapping, Replacement Algorithms, Cache Coherence, MESI protocol, Interleaved and associative memories, Virtual memory, Main memory allocation, Segmentation ,Paging, Secondary storage ,RAID levels		

Module 5 & 6

5	**I/O Organization**		05	CO4
	5.1	External Devices , I/ O Modules		
	5.2	Programmed I/O, Interrupt driven I/O, DMA		
6	**Multiprocessor Configurations**		04	CO4
	6.1	Flynn's classification, Parallel processing systems and concepts		
	6.2	Introduction to pipeline processing and pipeline hazards,		
	6.3	Design issues of pipeline architecture, Instruction pipelining: Six Stage instruction pipeline		

COA-William Stallings

Recommended Books:

Sr. No.	Name/s of Author(s)	Title of Book	Name of Publisher with country	Edition and Year of Publication
1.	W. Stallings	"Computer Organization and Architecture: Designing for performance",	Prentice Hall of India	8th Edition, 2003, ISBN 81 – 203 – 2962 – 7
2.	C. Hamacher, V. Zvonko, S. Zaky	"Computer Organization"	McGraw Hill	5th edition, 2002 ISBN 007-120411-3
3.	Kai Hwang & Bridggs	Computer Organization & Parallel Processing	McGraw Hill	International Editions 1985

William Stallings
Computer Organization and Architecture

Chapter 1
Introduction

Architecture & Organization

- **Architecture** is those attributes **visible** to the programmer
  - Instruction set, number of bits used for data representation, I/O mechanisms, addressing techniques.

- **Organization** is **how** features are implemented
  - Control signals, interfaces, memory technology.
  - e.g. Is there a hardware multiply unit or is it done by repeated addition?

COMPUTER ARCHITECTURE	COMPUTER ORGANIZATION
Way hardware components are connected together to form a computer system.	**Structure and behaviour** of a computer system as **seen by the user**.
It acts as the interface between hardware and software.	It deals with the components of a connection in a system.
Helps us to understand the **functionalities** of a system.	How exactly all the **units in the system are arranged and interconnected.**
A programmer can **view architecture** in terms of **instructions, addressing modes and registers**.	Whereas Organization expresses the **realization of architecture.**
While **designing** a computer system **architecture is considered first**.	An organization is done on the basis of architecture.
Computer Architecture deals with high-level design issues.	Computer Organization deals with low-level design issues.
Architecture involves **Logic** (Instruction sets, Addressing modes, Data types, Cache optimization)	Organization involves **Physical Components** (Circuit design, Adders, Signals, Peripherals)

Architecture & Organization

- All **Intel x86** family share the same basic **architecture**
- The **IBM System/370** family share the same basic **architecture**
- This gives **code compatibility**
  - At least backwards
- **Organization** differs between different versions

S.NO	Processor	Clock Speed	Bus Width	MIPS	Power	Price
1	**Intel Pentium 111**	The clock speed of Intel Pentium 111 processor is 1GHz	The bus width of Intel Pentium 111 processor is 32	A million instructions per second of Intel Pentium 111 processor is ~900	The power of this processor is 97 W	$900
2	**IBM PowerPC 750X**	The clock speed of the IBM PowerPC 750X processor is 550 MHz	The bus width of the IBM PowerPC 750X processor is 32/64	A million instructions per second of IBM PowerPC 750X processor is ~1300	The power of this processor is 5 W	#900
3	MIPS R5000	The clock speed of the MIPS R5000 processor is 250 MHz	The bus width of the MIPS R5000 processor is 32/64	NA	NA	NA
4	StrongARM SA-110	The clock speed of StrongARM SA-110 processor is 233 MHz	The bus width of StrongARM SA-110processor is 32	The million instructions per second of StrongARM SA-110processor is 268	The power of this processor is 1 W	NA

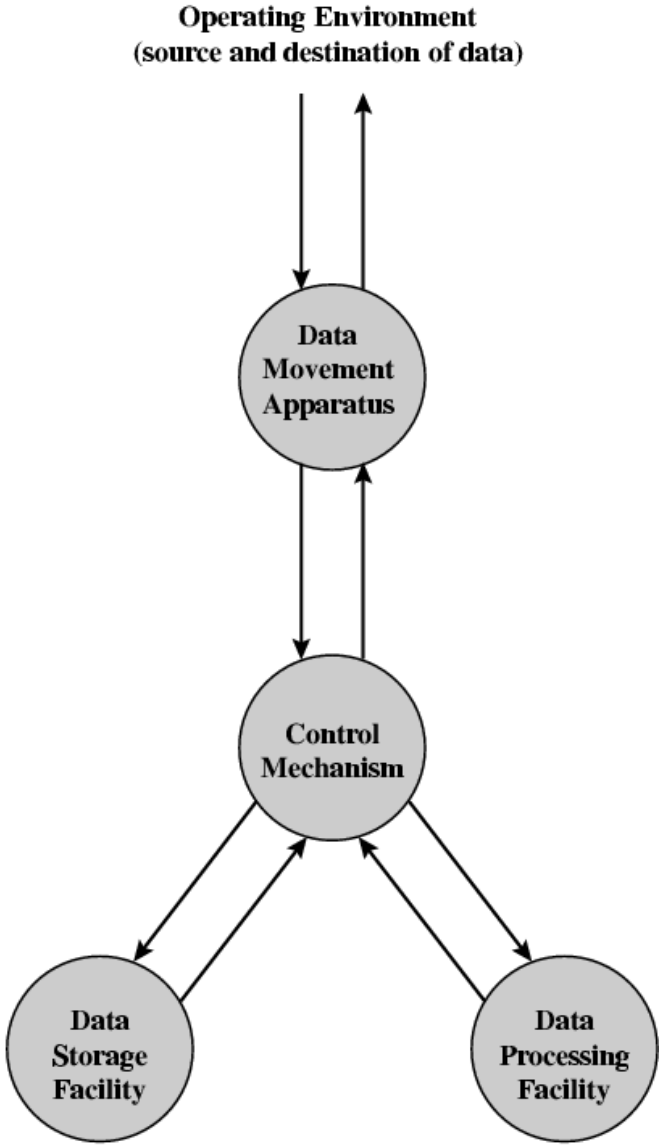
Structure & Function

- **Structure** is the way in which components relate to each other
- **Function** is the operation of individual components as part of the structure

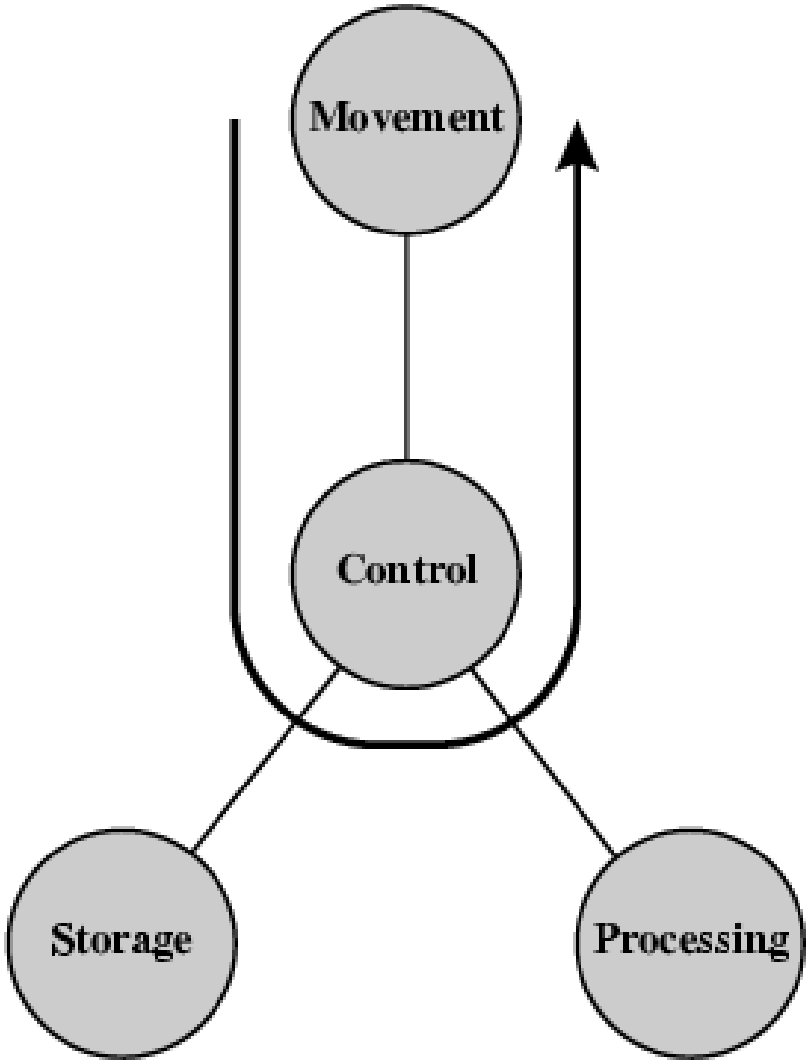
Function

- All computer **functions** are:
  - Data processing
  - Data storage
  - Data movement
  - Control

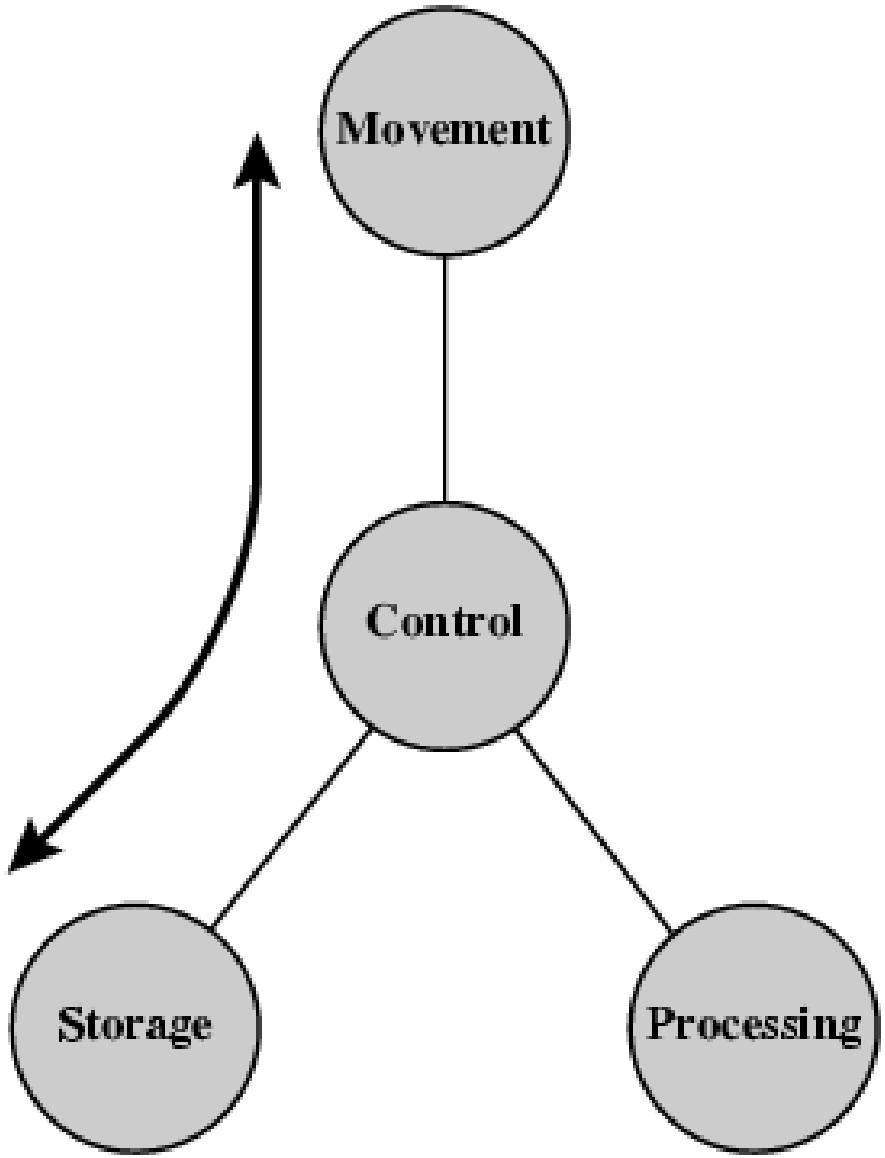
Functional View



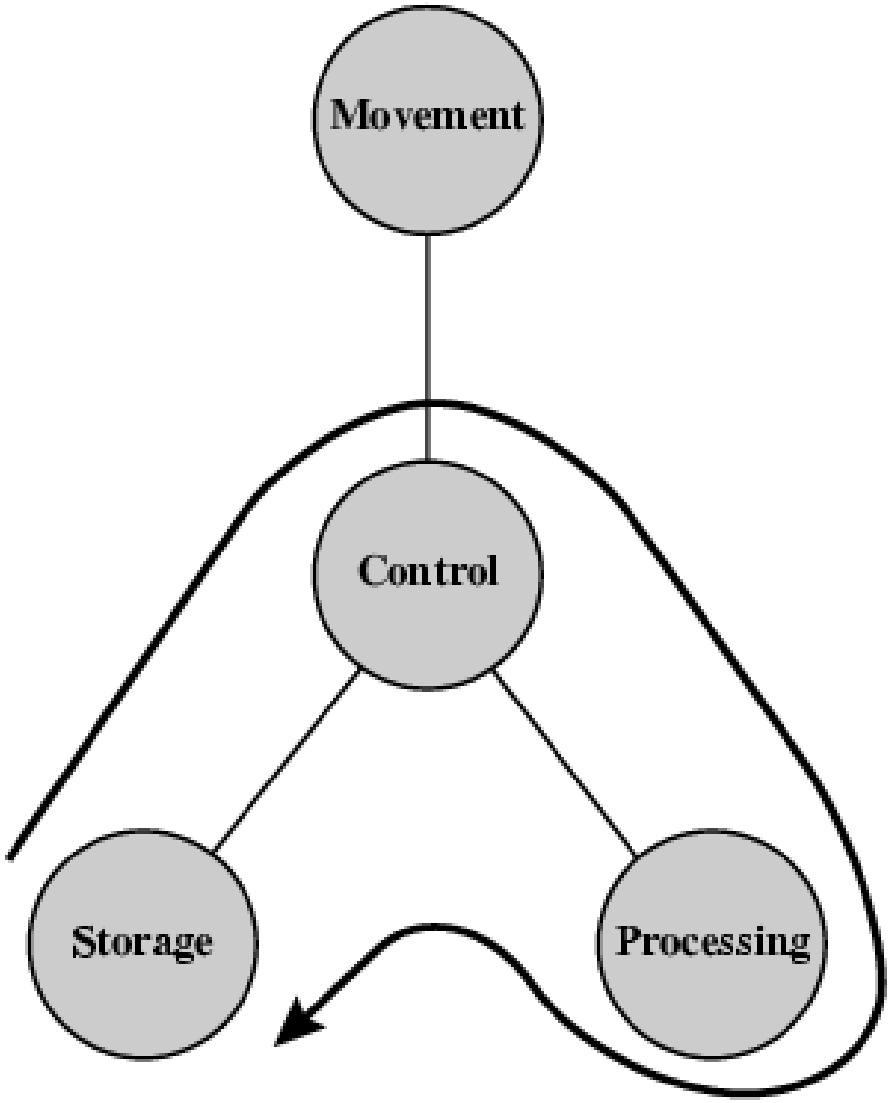
Operations (a) Data movement



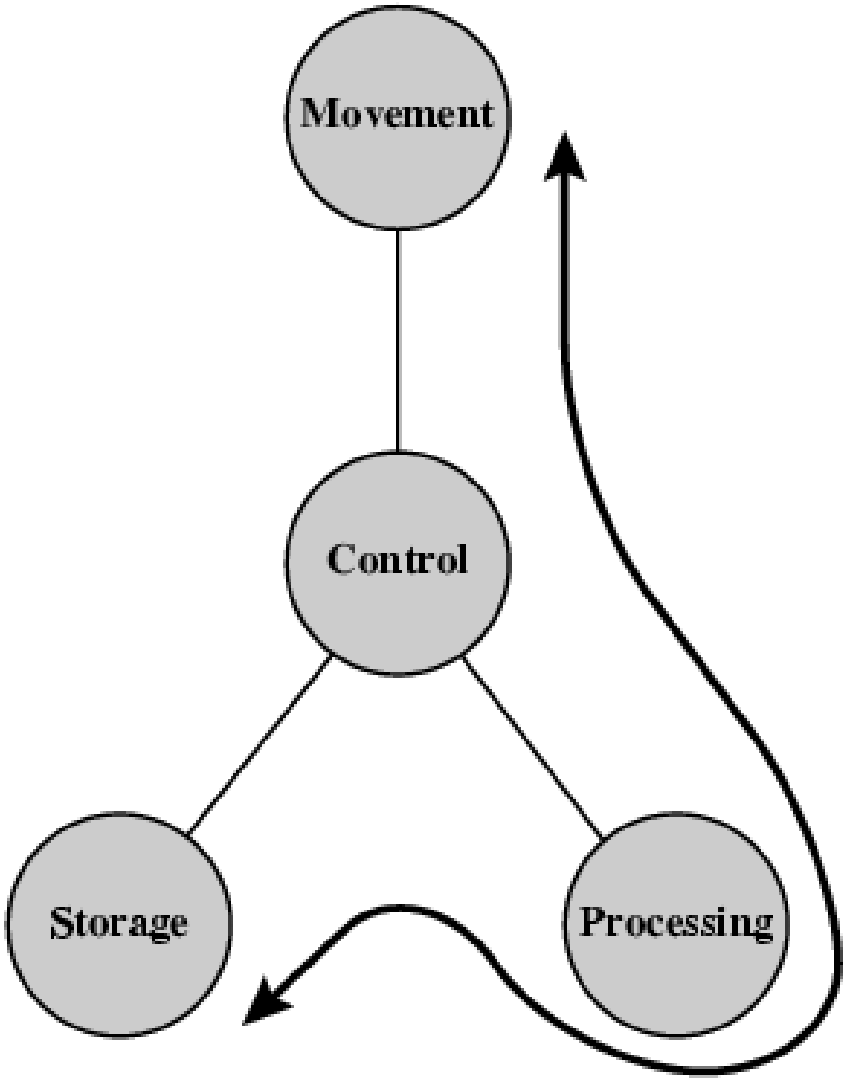
Operations (b) Storage



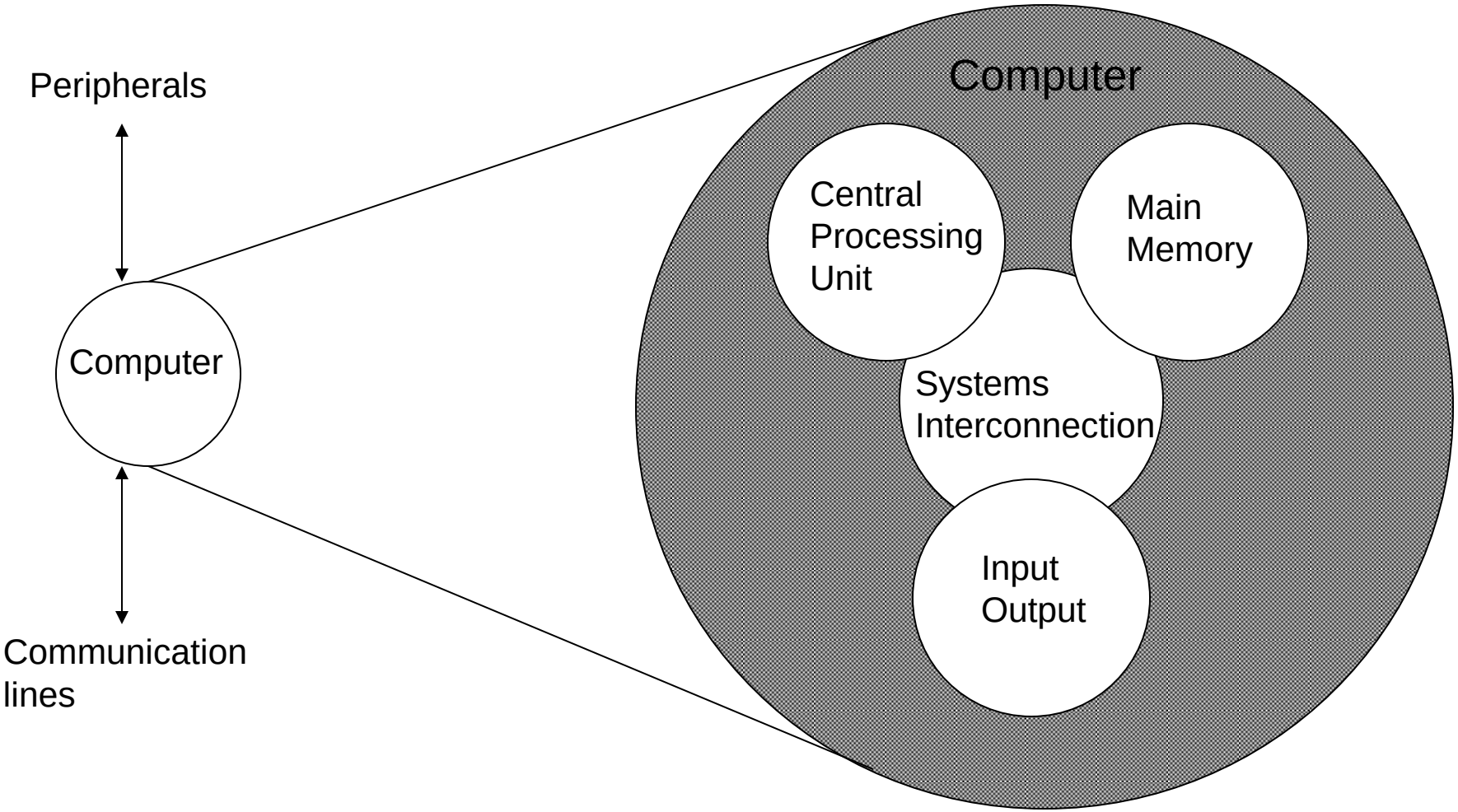
Operation (c) Processing from/to storage



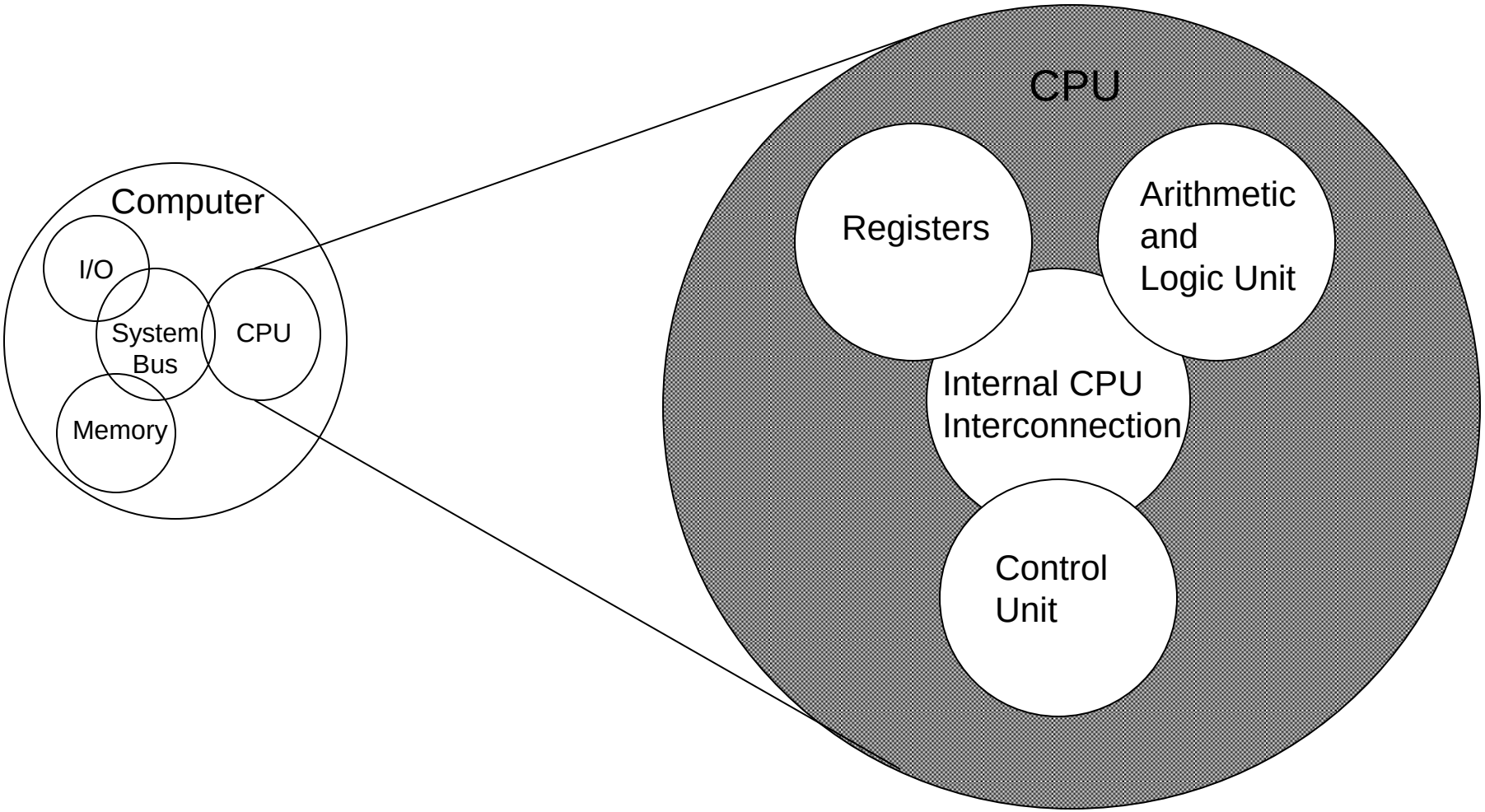
Operation (d)
Processing from storage to I/O



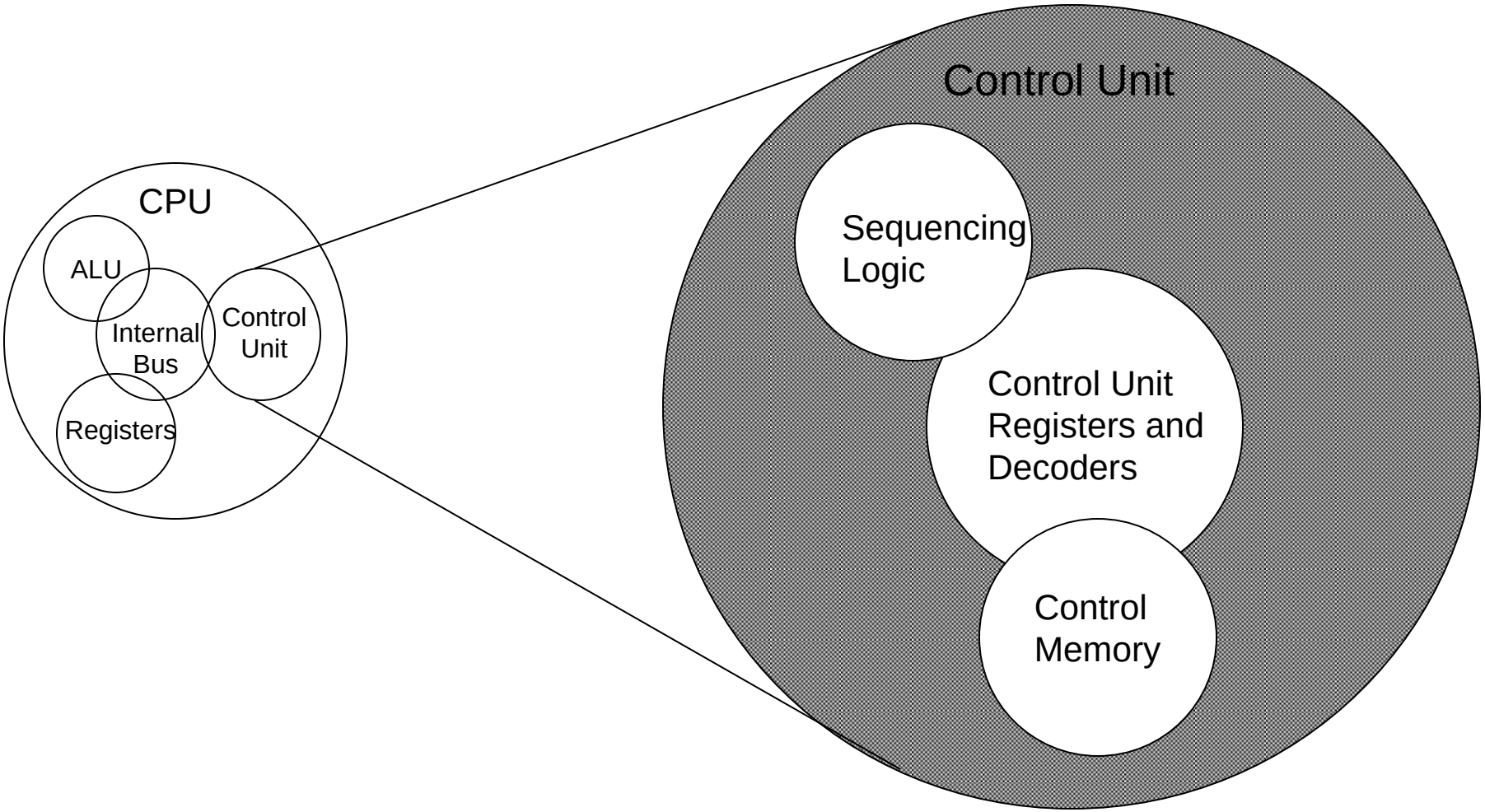
Structure - Top Level



Structure - The CPU



Structure - The Control Unit



William Stallings Computer Organization and Architecture 8th Edition

Chapter 2

Computer Evolution and Performance

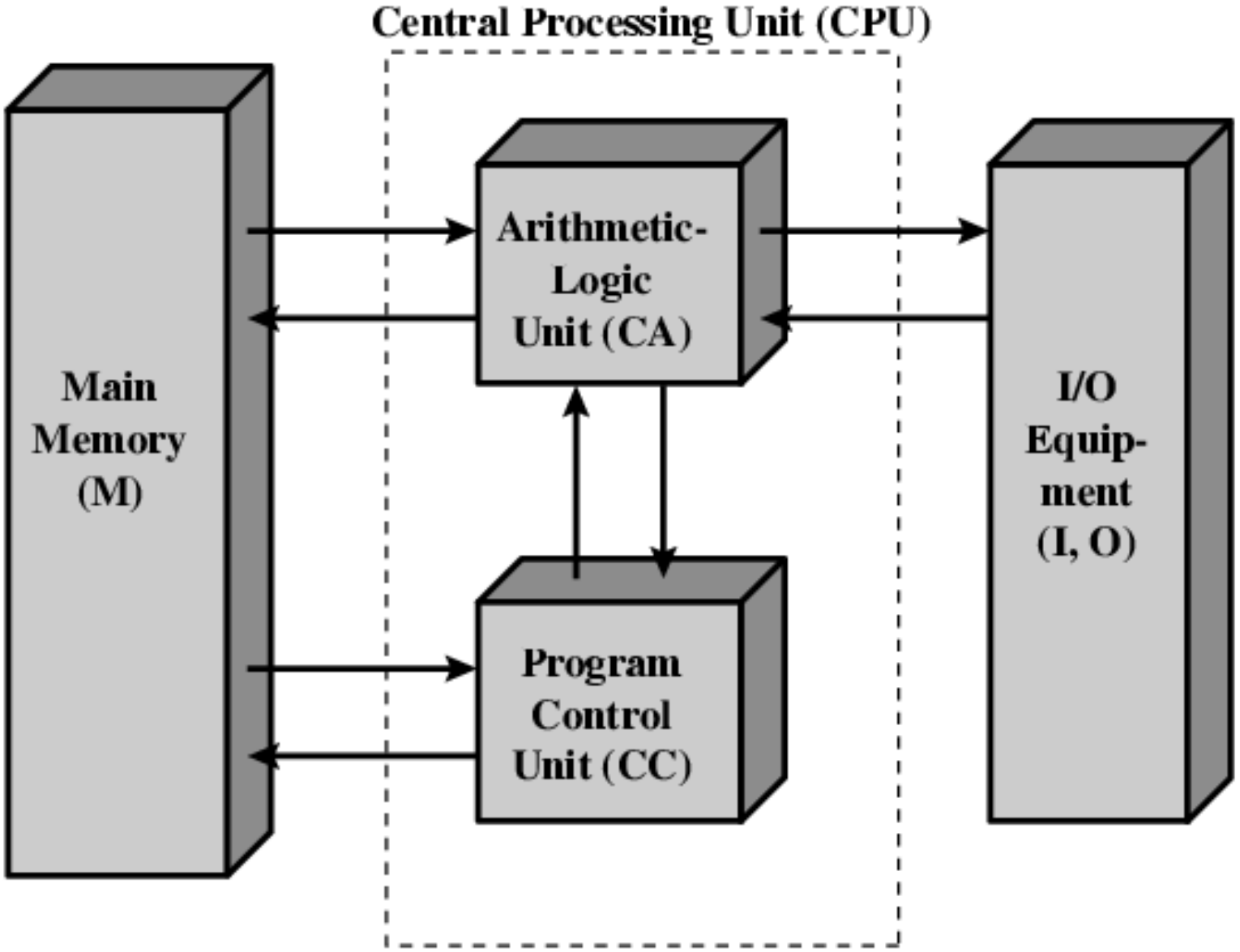
Von Neumann

- **Stored Program concept**

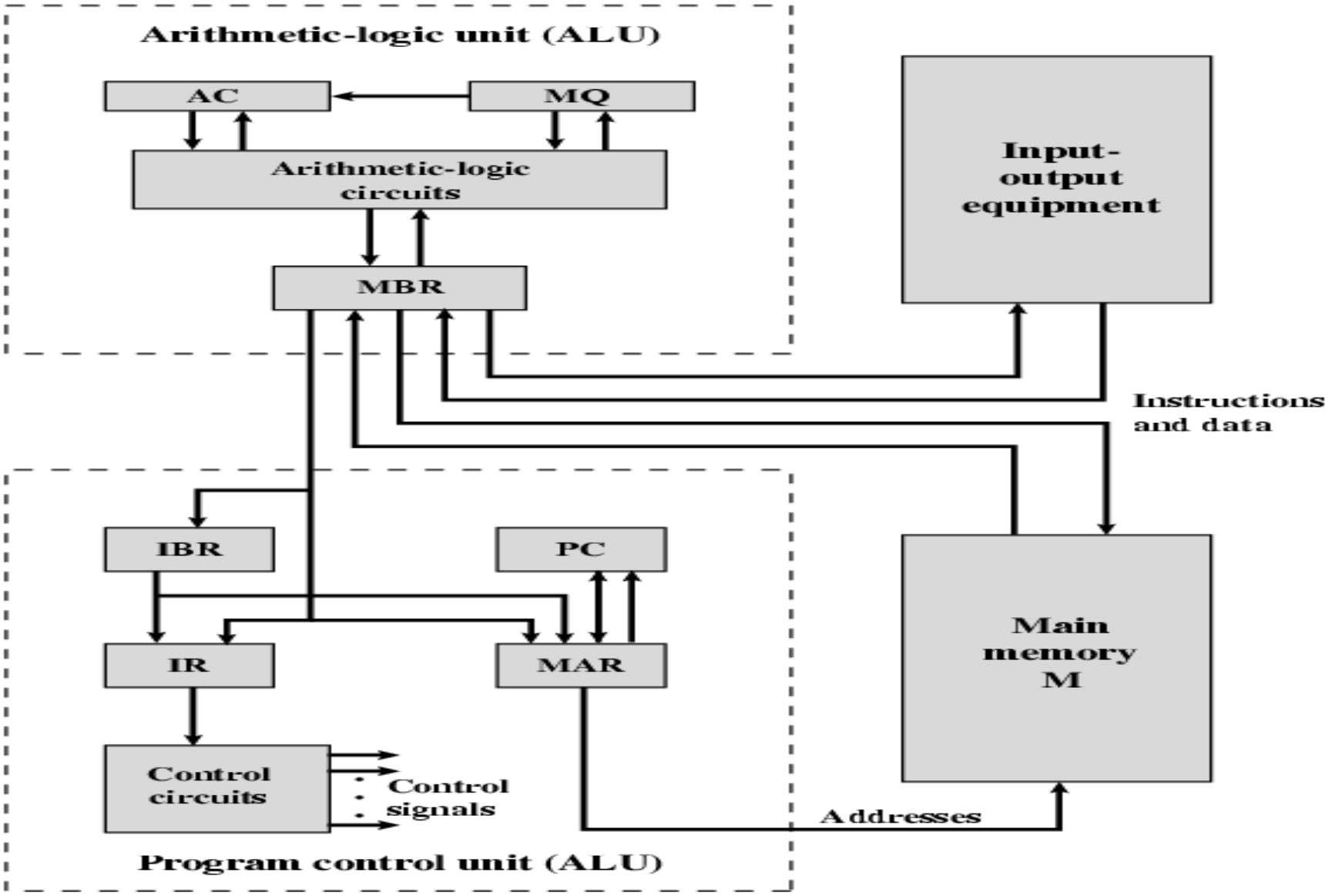
- **Main memory** storing programs and data
- **ALU** operating on binary data
- **Control unit** interpreting instructions from memory and executing
- **Input and output** equipment operated by control unit

- Princeton Institute for Advanced Studies
  - IAS
- Completed 1952

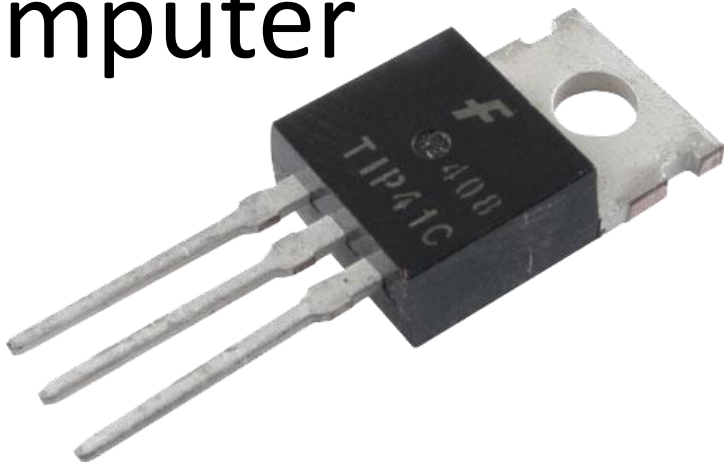
Structure of Von Neumann machine



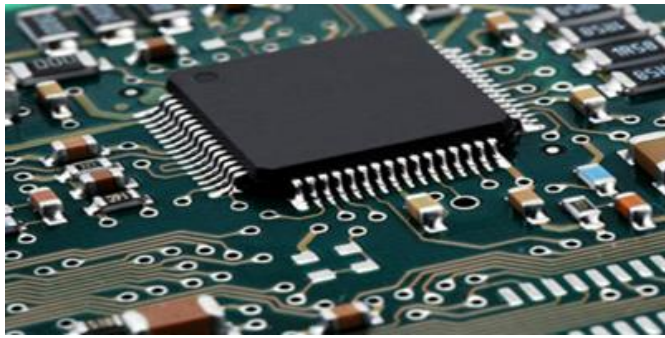
Structure of IAS – detail



Generations of Computer



- Vacuum tube - 1946-1957
- Transistor - 1958-1964
- Small scale integration - 1965
  - Up to 100 devices on a chip
- Medium scale integration - to 1971
  - 100-3,000 devices on a chip
- Large scale integration - 1971-1977
  - 3,000 - 100,000 devices on a chip



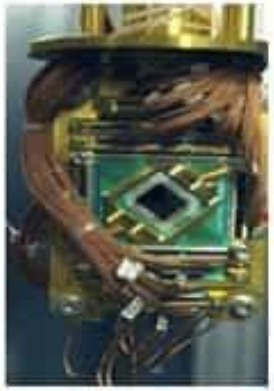
- Very large scale integration - 1978 -1991
  - 100,000 - 100,000,000 devices on a chip
- Ultra large scale integration – 1991 -Over 100,000,000 devices on a chip

Vacuum Tube

Transistors

Integrated Circuit

Microprocessor



Quantum Computer

1st Generation Computer

2nd Generation Computer

3rd Generation Computer

4th Generation Computer

5th Generation Computer

Subject	1st generation	2nd generation	3rd generation	4th generation	5th generation
Period	1940-1956	1956-1963	1964-1971	1971-present	present & beyond
Circuitry	Vacuum tube	Transistor	Integrated chips (IC)	Microprocessor (VLSI)	ULSI (Ultra Large Scale Integration) technology
Memory Capacity	20 KB	128KB	1MB	Magnetic core memory, LSI and VLSI. High Capacity	ULSI
Processing Speed	300 IPS instructions Per sec.	300 IPS	1MIPS (1 million inst. Per sec.)	Faster than 3rd generation	Very fast
Programming Language	Machine, Language	Assembly language & early high-level languages(FORTRAN, COBOL, ALGOL)	C,C++	Higher level languages,C,C++,Java	All the Higher level languages,,Neural networks,
Example of computers	UNIVAC, EDVAC	IBM 1401, IBM 7094, CDC 3600,D UNIVAC 1108	IBM 360 series, 1900 series	Pentium series,Multimedia,	Artificial Intelligence, Robotics

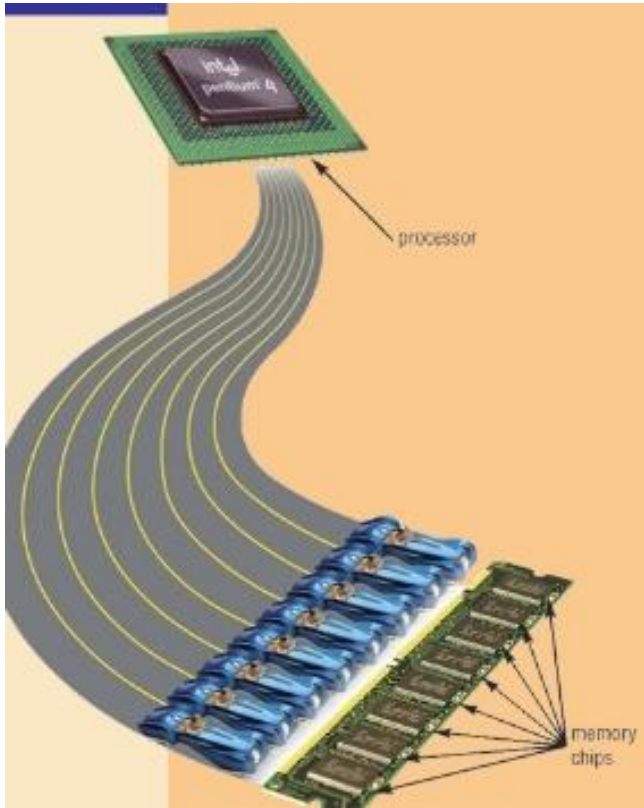
What is a Bus?

- A **communication pathway** connecting two or more devices
- Data connection between 2 or more devices connected to the computer
- Usually **broadcast** ,Often grouped
  - For Ex: A bus enables a computer processor to communicate with the memory or video card to communicate with the memory
  - e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown

Buses

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus (PC)
- e.g. Unibus (DEC-PDP)

(Digital Equipment Corporation-Programmed Data Processor)



Functions of Buses in Computers

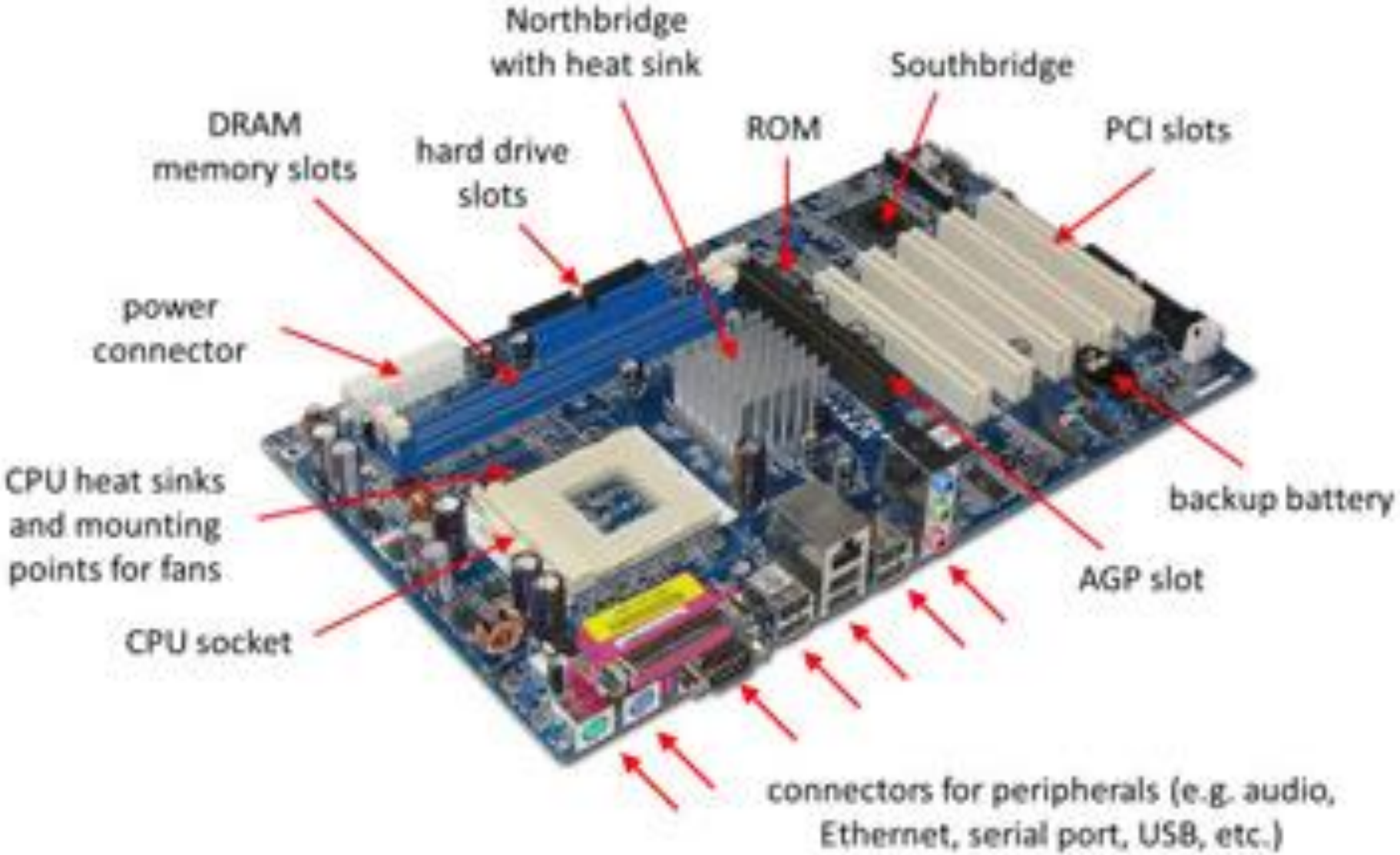
Data sharing - Serial/Parallel, 8-bit, 16-bit, 32-bit or even 64-bit buses.

Addressing - A bus has address lines which allows data to be sent to or from specific memory locations.

Power - A bus supplies power to various peripherals connected to it.

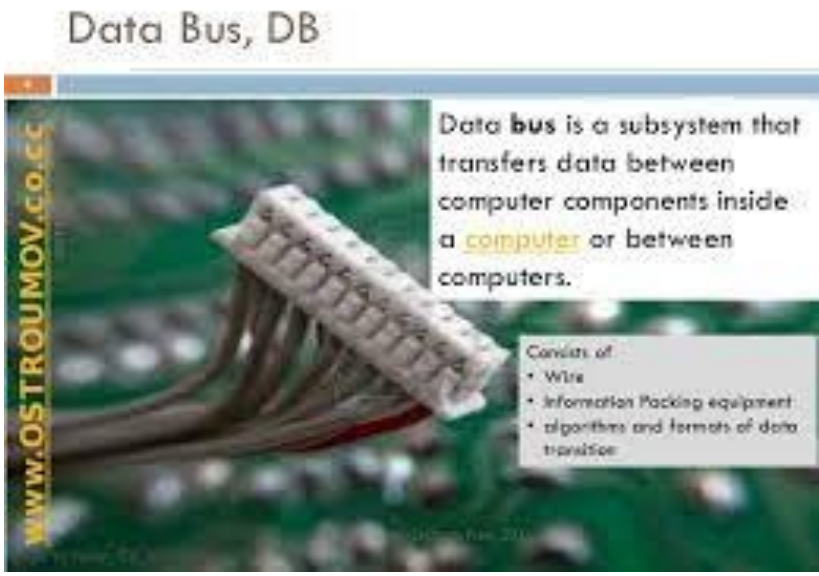
Timing - System clock-**s**ynchronize the peripherals attached to it with the rest of the system.

Eg: The expansion bus facilitates easy connection of more or additional components and devices on a computer such as a TV card or sound card.


Northbridge
with heat sink
Southbridge
DRAM
memory slots
hard drive
slots
ROM
PCI slots
power
connector
CPU heat sinks
and mounting
points for fans
backup battery
AGP slot
CPU socket
connectors for peripherals (e.g. audio,
Ethernet, serial port, USB, etc.)

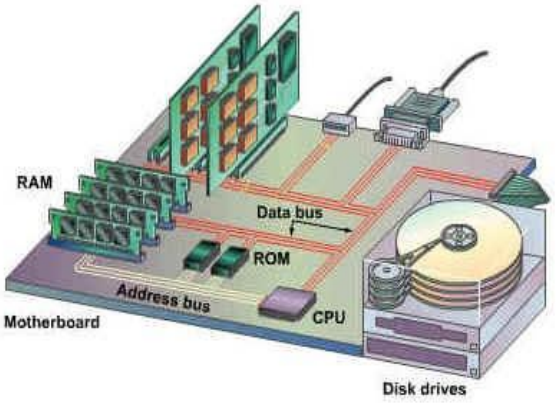
Data Bus

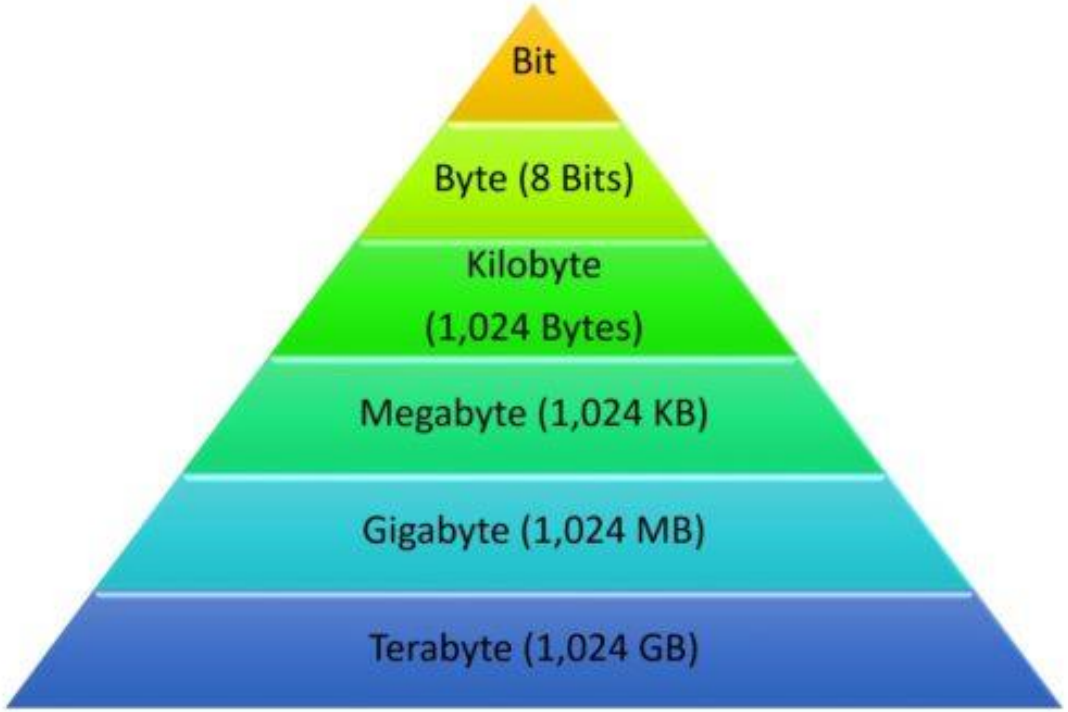
- Carries **data**
  - Remember that there is no difference between “data” and “instruction” at this level
- **Width** is a key determinant of **performance**
  - 8, 16, 32, 64 bit

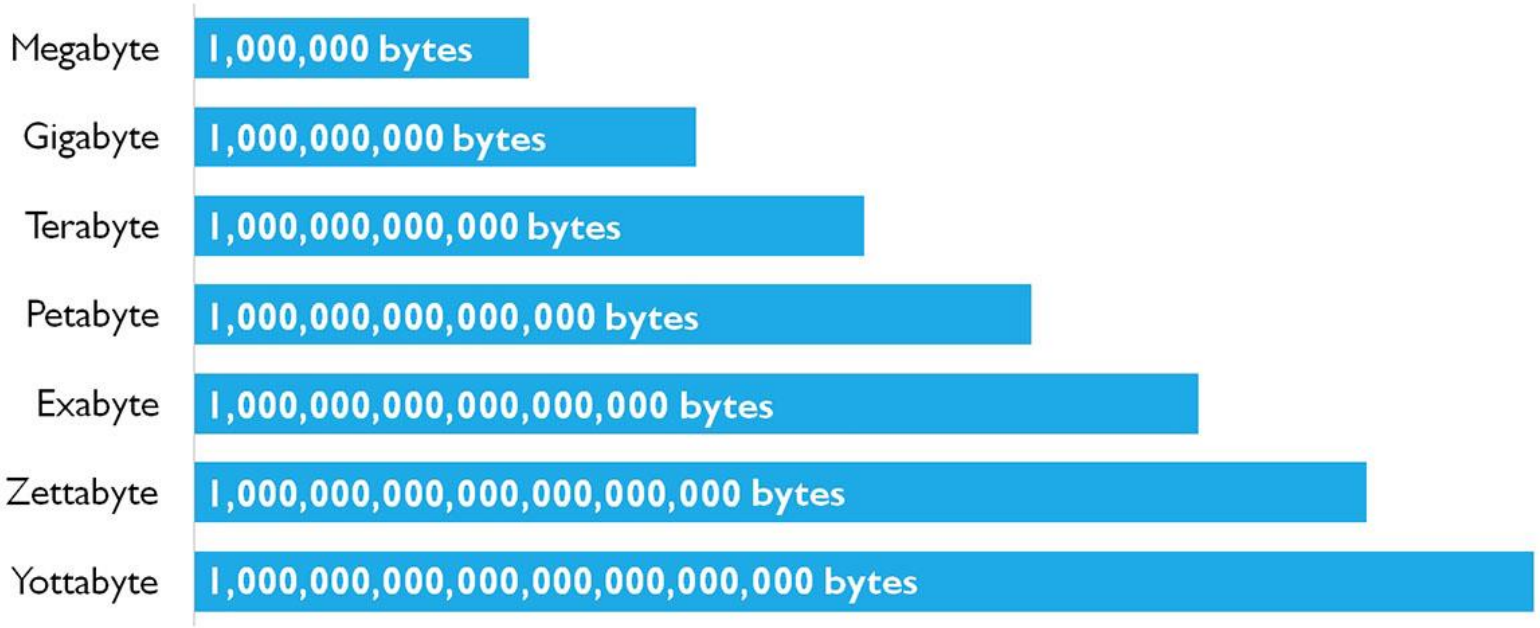


Address bus

- Identify the source or destination of data-Eg 1000H,1200H
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines **maximum memory capacity** of system
- 2 ^nos of address lines=Memory Capacity
  - e.g. 8080 has 16 bit address bus giving 64k address space
  - 32 bit?64bit ? 2 ^
  - (16.777216 million terabyte)




Bit
Byte (8 Bits)
Kilobyte
(1,024 Bytes)
Megabyte (1,024 KB)
Gigabyte (1,024 MB)
Terabyte (1,024 GB)


Megabyte
1,000,000 bytes
Gigabyte
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Terabyte
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Petabyte
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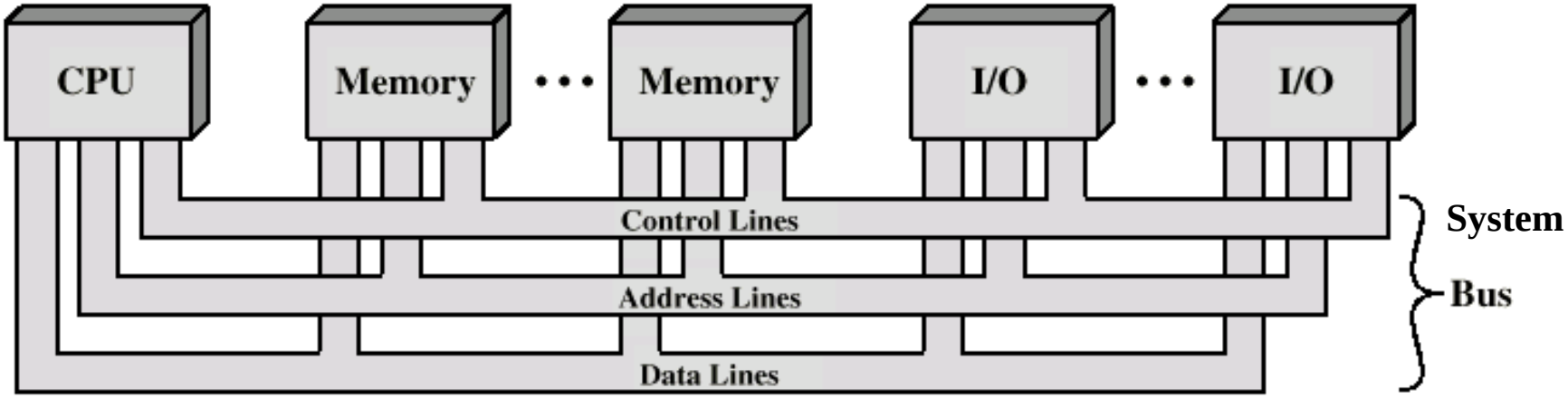
Exabyte
1,000,000,000,000,000,000 bytes
Zettabyte
1,000,000,000,000,000,000,000 bytes
Yottabyte
1,000,000,000,000,000,000,000,000 bytes

Control Bus

- Controls activities of all units of a computer
- Main Function is to carry **control signals** generated by control unit
  - Ex: One line of control bus is used to indicate whether the CPU is reading/writing to the main memory
- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

Bus Interconnection Scheme



Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Bus Types

- **Dedicated**
  - Separate data & address lines
- **Multiplexed**
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance

Bus Arbitration

- More than one module controlling the bus
- e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

Centralised or Distributed Arbitration

- Centralised
  - Single hardware device controlling bus access
    - Bus Controller
    - Arbiter
  - May be part of CPU or separate
- Distributed
  - Each module may claim the bus
  - Control logic on all modules

Introduction to PCI Bus

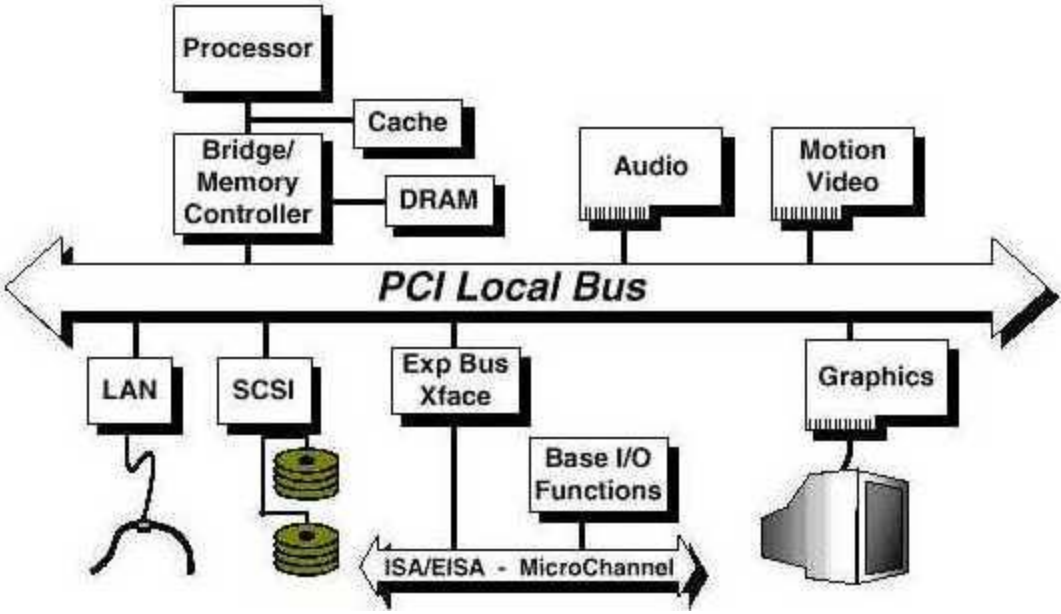
- Bus
  a) highways that take information and power from one place to another.
  b) channel or path between the components in a computer
  c) lets you connect components to the computer's processor
  d) hard disks, memory, sound systems, video systems , graphics card etc…
- PCI Bus
- Nowadays USB-
- Used as the standard in most computers' high-speed buses
- Firewire ?
- ISA Bus- Industry Standard Architecture
- IT PROVIDES DIRECT ACCESS TO SYSTEM MEMORY FOR CONNECTED DEVICES
- Intel created the PnP standard and incorporated it into the design for PCI.

PCI Bus-Peripheral Component Interconnect

- Intel released to public domain-32 bit and 64 bit versions
- PCI bus connects the CPU and expansion boards
  - Examples of PCI devices
    - Modem
    - Network Card
    - Sound Card,Video Card,etc

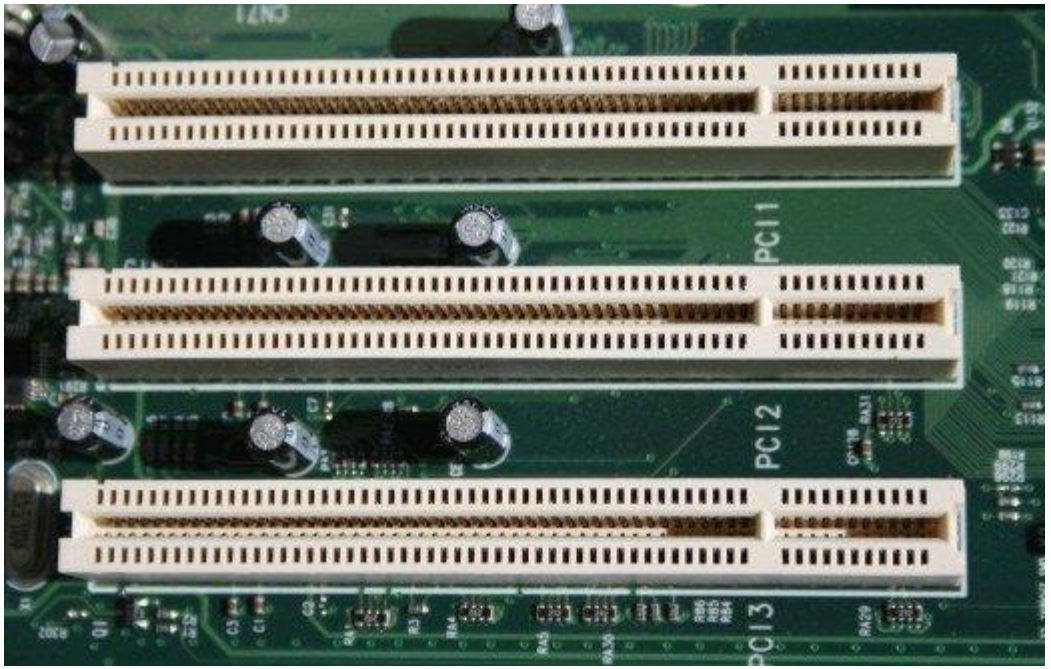
PCI Bus Lines (required)

- Systems lines
  - Including clock and reset
- Address & Data
  - 32 time mux lines for address/data
  - Interrupt & validate lines
- Interface Control
- Arbitration
  - Not shared
  - Direct connection to PC bus arbiter
- Error lines



PCI Bus Lines (Optional)

- Interrupt lines
  - Not shared
- Cache support
- 64-bit Bus Extension
  - Additional 32 lines
  - Time multiplexed
  - 2 lines to enable devices to agree to use 64-bit transfer

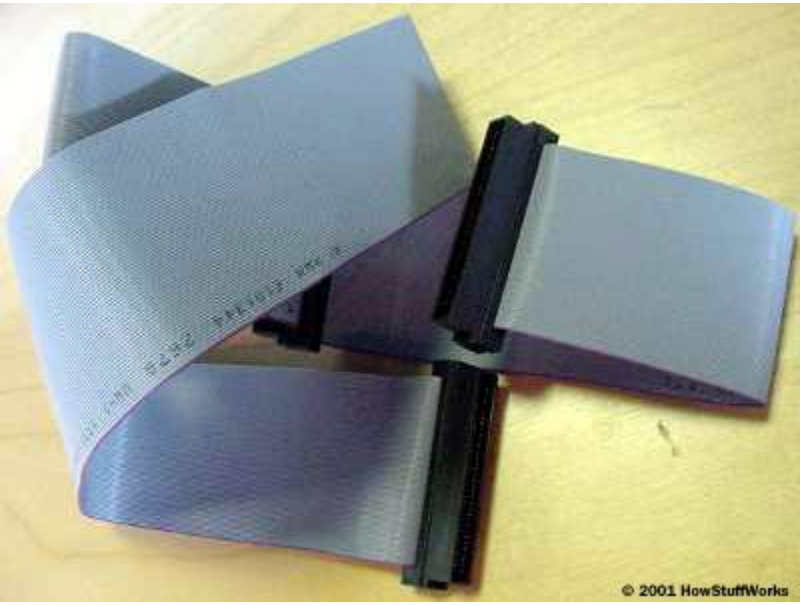


- **Let's say that you have just added a new PCI-based sound card to your Windows XP computer. Here's an example of how it would work**.
- You open up your computer's case and plug the sound card into an empty PCI slot on the motherboard
- You close the computer's case and power up the computer.
- The system BIOS initiates the PnP BIOS.
- The PnP BIOS scans the PCI bus for hardware. It does this by sending out a signal to any device connected to the bus, asking the device who it is.
- The sound card responds by identifying itself. The device ID is sent back across the bus to the BIOS.
- The PnP BIOS checks the ESCD to see if the configuration data for the sound card is already present. Since the sound card was just installed, there is no existing ESCD record for it.
- The PnP BIOS assigns IRQ, DMA, memory address and I/O settings to the sound card and saves the data in the ESCD.
- Windows XP boots up. It checks the ESCD and the PCI bus. The operating system detects that the sound card is a new device and displays a small window telling you that Windows has found new hardware and is determining what it is.
- In many cases, Windows XP will identify the device, find and load the necessary drivers, and you'll be ready to go. If not, the "Found New Hardware Wizard" will open up. This will direct you to install drivers off of the disc that came with the sound card.
- Once the driver is installed, the device should be ready for use. Some devices may require that you restart the computer before you can use them. In our example, the sound card is immediately ready for use.
- You want to capture some audio from an external tape deck that you have plugged into the sound card. You set up the recording software that came with the sound card and begin to record.
- The audio comes into the sound card via an external audio connector. The sound card converts the analog signal to a digital signal.
- The digital audio data from the sound card is carried across the PCI bus to the bus controller. The controller determines which device on the PCI device has priority to send data to the CPU. It also checks to see if data is going directly to the CPU or to system memory.
- Since the sound card is in record mode, the bus controller assigns a high priority to the data coming from it and sends the sound card's data over the bus bridge to the system bus.
- The system bus saves the data in system memory. Once the recording is complete, you can decide whether the data from the sound card is saved to a hard drive or retained in memory for additional processing.

Introduction to SCSI Bus

- Pronounced "scuzzy"
- Fast bus that can connect lots of devices to a **COMPUTER** at the same time, including hard drives, scanners, CD-ROM/RW drives, printers and tape drives unlike USB connected for small devices.
- Helps to put multiple items on one bus.
- Also works with most computer systems.
- Prob---
  - Limited BIOS support as it has to be configured for each computer
  - No common SCSI software interface
  - All different types of SCSI have different speeds,bus widths,connectors

  Which can be confusing !

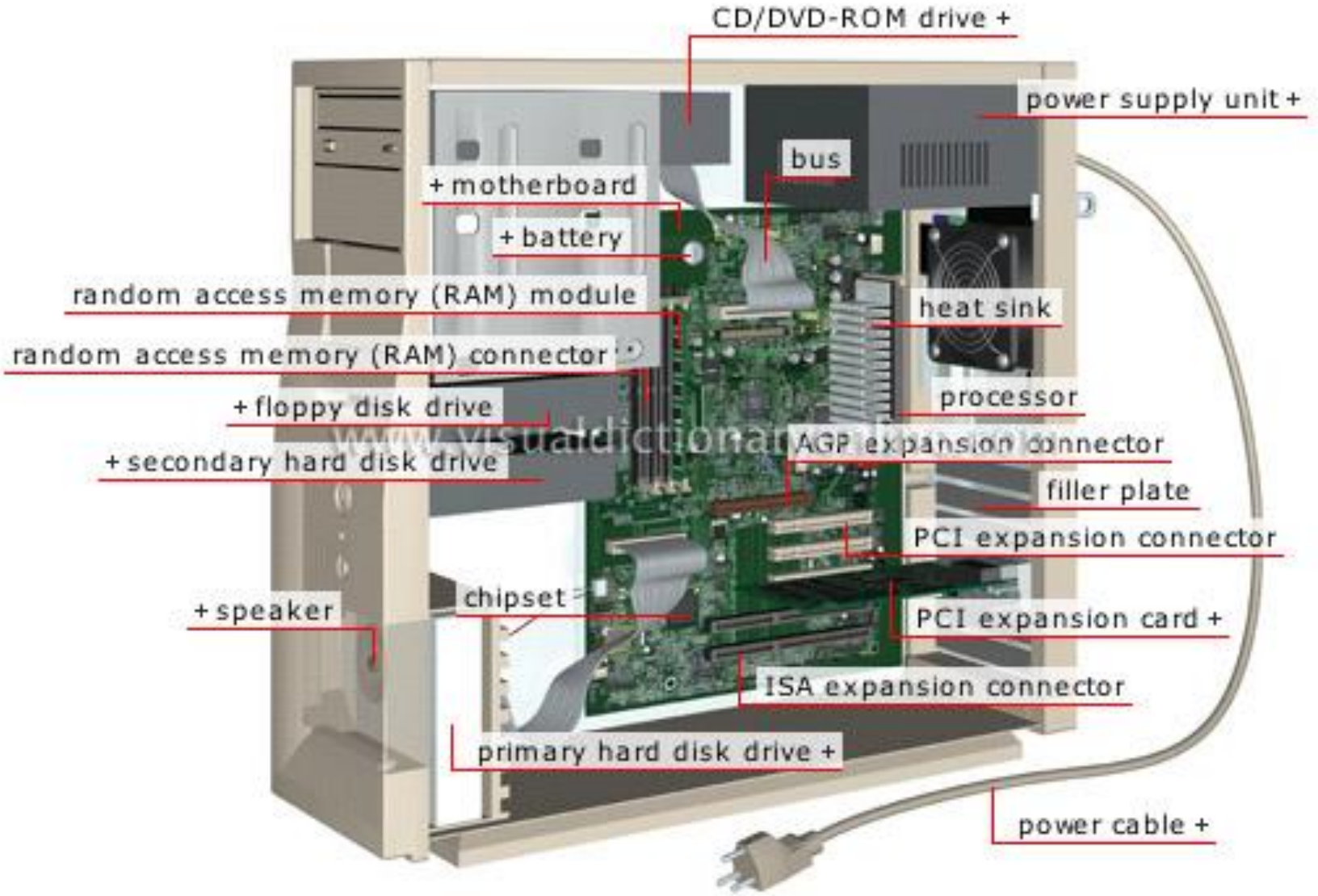


Internal SCSI devices connect to a ribbon cable.

External SCSI devices connect using thick, round cables

SCSI-Small Computer System Interface

- Set of standard electronic interfaces that allow personal computers **PC's to communicate with peripheral hardware** such as disk drives,tapes,CDs,Printers,scanners,etc
- Faster.
- SCSI standards are generally backward compatible
  - A parallel interface standard used by Apple Macintosh computers, PCs and Unix systems for attaching peripheral devices to a computer.


CD/DVD-ROM drive +
power supply unit +
bus
+ motherboard
+ battery
random access memory (RAM) module
heat sink
random access memory (RAM) connector
processor
+ floppy disk drive
AGP expansion connector
+ secondary hard disk drive
filler plate
PCI expansion connector
chipset
+ speaker
PCI expansion card +
ISA expansion connector
primary hard disk drive +
power cable +