Course Name:	Digital Design Laboratory	Semester:	III
Date of Performance:	18 / 9 / 2023	Batch No:	C-2
Faculty Name:		Roll No:	16010122267
Faculty Sign & Date:		Grade/Marks:	___/25

Experiment No: 7
Title: Asynchronous Counter

Aim and Objective of the Experiment:

To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:

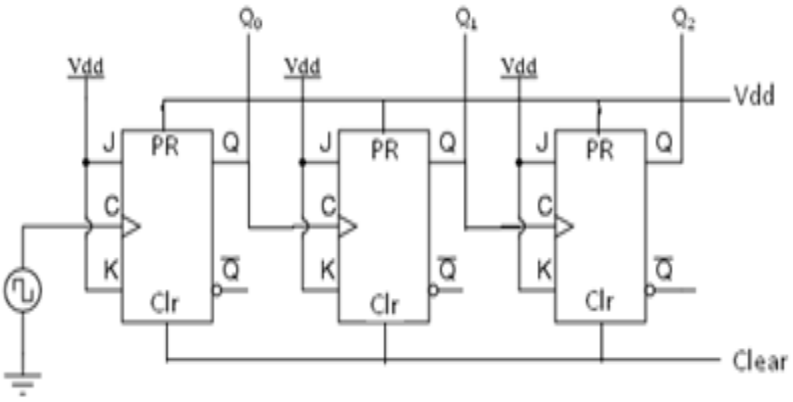
CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

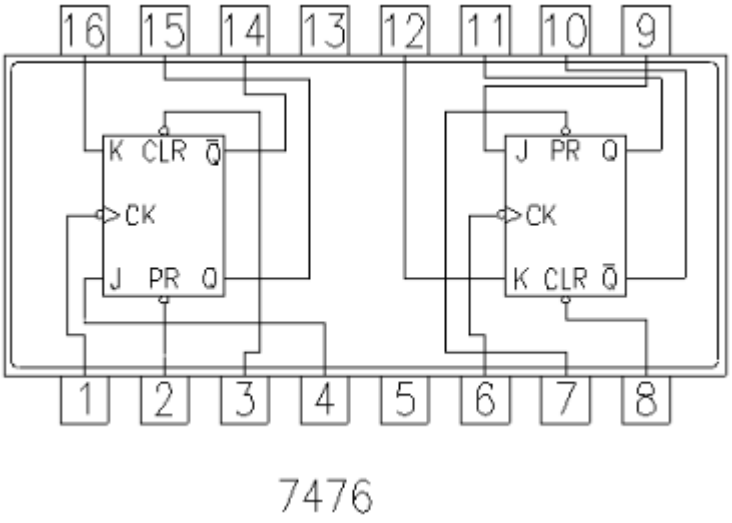
Trainer kits

Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)



Pin diagram of JK FF (IC 7476)



Implementation Details

Procedure

1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

1. How JK FF need to be configured to use for counter operation?

Ans:

To configure a JK flip-flop for counter operation:

a) Connect the clock input to a clock signal.
b) Set J = 1 and K = 1 for the first flip-flop (LSB).
c) Connect the Q output of the previous flip-flop to the J and K inputs of the next flip-flop for multibit counters.
d) Optionally, use clear (CLR) or preset (PRE) inputs for initializing the counter.

2. What changes are required to use the same counter as 3 bit asynchronous down counter?

Ans:

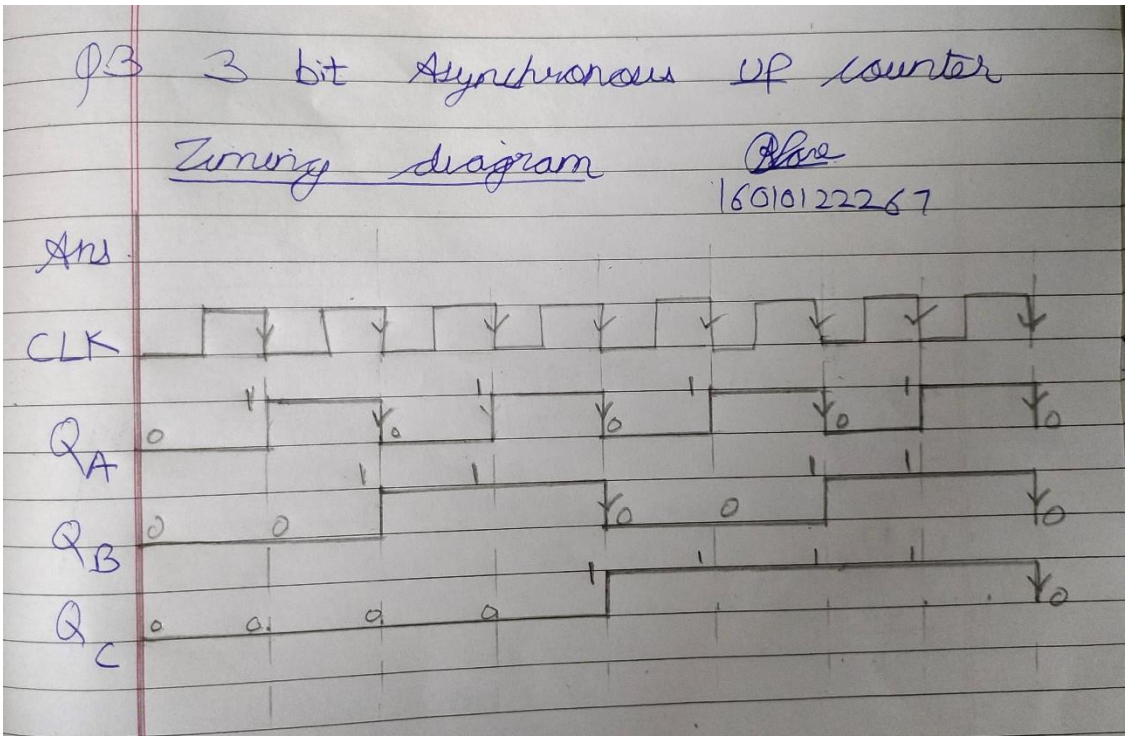
To convert a 3-bit asynchronous up counter to a down counter:

a) Change the J and K input settings for each flip-flop as follows:
    a. FF0: J=K=0
    b. FF1: J=1, K=0 (or vice versa)
    c. FF2: J=K=1

b) Add Load (LD) inputs to preset the counter to your desired initial value (e.g., 7).
c) Optionally, include Clear (CLR) inputs for resetting the counter to its initial state.

3. Draw the timing diagram of 3 bit Asynchronous up counter.

Ans:



4. What is mod n concept used in counters?

Ans:

In counters, the "mod n" concept means that the counter counts from 0 to (n-1) before resetting to 0, creating a cyclical pattern. For example, in a mod 8 counter, it counts 0, 1, 2, 3, 4, 5, 6, 7, and then resets to 0. This concept is crucial in digital electronics for creating repetitive sequences and controlling timing events, such as in clocks, timers, and frequency dividers.

5. For Mod-5 counter how many JK FFs are required?

Ans:

For a Mod-5 counter, you would need a total of 3 JK flip-flops (JK FFs).
The reason for this is that a Mod-5 counter counts from 0 to 4 (or equivalently, 000 to 100 in binary), which requires three bits to represent all the states. Each JK flip-flop represents one bit of the counter.
Here's how the counting sequence works for a 3-bit Mod-5 counter using JK flip-flops:

- 000 (Decimal 0)
- 001 (Decimal 1)
- 010 (Decimal 2)

- 011 (Decimal 3)
- 100 (Decimal 4)

So, to count through these five states, you need three JK flip-flops to represent the three bits of the counter.

Conclusion:

In conclusion, we learnt to implement synchronous and asynchronous sequential circuits using IC7476 and verified the truth table.

Signature of faculty in-charge with Date: