28.05.2024 (E)

SOMAIYA VIDYAVIHAR UNIVERSITY

Semester: MAY-2024		
Maximum Marks: 100	Examination: ESE Examination – KT	Duration:3 Hrs.
Programme code: 01 Programme: BTECH COMPUTER ENGG.	Class: SY	Semester: III(SVU 2020)
Name of the Constituent College: K. J. Somaiya College of Engineering	Name of the department: Computer Engineering	
Course Code: 116U01C303	Name of the Course: Computer Organization & Architecture	
Instructions: 1)Draw neat diagrams 2) All questions are compulsory 3) Assume suitable data wherever necessary		

Que. No.	Question	Max. Marks
Q1	Solve any **Four**	**20**
i)	Define Computer Organization& Computer Architecture? Draw Von Neumann Model for the basic structure of a computer.	5
ii)	What is meant by IEEE-754 floating point representation? Explain with an example.	5
iii)	What is meant by Microprogramming? State with the help of example and state applications of the same.	5
iv)	List the elements of cache design.	5
v)	Brief on DMA	5
vi)	List the six stages of an instruction pipeline	5

Que. No.	Question	Max. Marks
Q2 A	Solve the following	**10**
i)	Draw the flowchart for floating point multiplication.	5
ii)	Draw the flowchart for floating point division.	5
	OR	
Q2 A	Draw the flowchart for restoring division. Hence Solve M=12, Q =23	10
Q 2 B	Solve any **One**	**10**
i)	Solve by Booth's Recoding for M=11 , Q = 12	10
ii)	Solve for M= - 24 and Q = 20 using Booth's Algorithm for signed multiplication.	10

Que. No.	Question	Max. Marks
Q3	Solve any **Two**	**20**
i)	Write the micro operations for Fetch, Indirect cycle and Interrupt Cycle	10
ii)	Differentiate between RISC and CISC	10
iii)	What is meant by Control Unit? Hence draw and explain Microprogrammed Control Unit.	10

Que. No.	Question	Max. Marks
Q4	Solve any **Two**	20
i)	List and Explain characteristics of Memory system with an appropriate example	10
ii)	Draw SRAM and DRAM in detail. Hence differentiate between them	10
iii)	Briefly explain: Virtual Memory. Paging. Segmentation.	10

Que. No.	Question	Max. Marks
Q5	(Write notes / Short question type) on any **four**	20
i)	Draw Programmed I/O flowchart and briefly explain the concept of busy waiting.	5
ii)	What is meant by Pipeline Hazards and hence explain pipeline processing.	5
iii)	Differentiate between PCI and SCSI Bus	5
iv)	Neatly draw the Instruction Cycle state diagram	5
v)	Draw RAID Levels from 0-6	5
vi)	What is FIFO and LRU with an example in real life applications.	5

2-12-2023 (E)

SOMAIYA VIDYAVIHAR UNIVERSITY

Semester: July 2023 –October 2023		
Maximum Marks: 100 **Examination: ESE Examination**		**Duration:3 Hrs.**
Programme code: 01 **Programme: B Tech Computer Engineering**	**Class: SY**	**Semester:III (SVU 2020)**
Name of the Constituent College: **K. J. Somaiya College of Engineering**	**Name of the department: COMP**	
Course Code: 116U01C303	**Name of the Course: Computer Organization & Architecture**	
Instructions: 1)Draw neat diagrams 2) All questions are compulsory **3) Assume suitable data wherever necessary**		

Que. No.	Question	Max. Marks
Q1	Solve any **Four**	**20**
i)	List the functions of I/O Module for interaction with peripherals and CPU.	5
ii)	What will be contents of register PC and SP after execution of **CALL function1** instruction? Assume suitable values for contents of registers and address of label "function1"	5
iii)	Explain following features of PCI Bus • Burst transfers for better data Transfer rate • Hidden Bus Arbitration	5
iv)	Explain Bit pair recoding of Booth Multiplier with suitable example	5
v)	Discuss Memory Hierarchy in Computer Systems	5
vi)	Explain how BCD numbers are added with example as **19 + 25** (by Representing these numbers in BCD)	5

Que. No.	Question	Max. Marks
Q2 A	Solve the following	**10**
i)	Explain tasks performed by CPU for instruction execution with a neat diagram	5
ii)	For the register set of intel X86 family explain specific function of each of following register CX,CS, IP, SI and Flags	5
	OR	
Q2 A	Explain restoring Division Algorithm and solve **37 / 13** using binary representations of these numbers using the same	10
Q 2 B	Solve any **One**	**10**
i)	Explain with neat diagram basic components in IAS architecture with its functionality	10
ii)	Draw the formats for single precision and double precision. Represent 0.00635 in single precision and in double precision format.	10

Que. No.	Question	Max. Marks
Q3	Solve any **Two**	**20**
i)	With reference to Virtual Memory implementation write whether following are true or false and justify your answer with suitable explanation • Virtual memory address generated by processor gives reference to page frame in page table.	10

	• Translation Lookaside buffer helps in reducing memory references • Page fault is a tool used by the Memory Management Unit for getting pages from secondary storage devices. • Main memory pages are copy of Secondary storage • LRU replacement algorithm can be applied to page replacement	
ii)	A two-way set-associative cache has lines of 16 bytes and a total size of 8 kB. The 64-MB main memory is byte addressable. Show the format of main memory addresses. Show cache organization with a neat diagram. Comment on Look up penalty when compared with 4 way set associative cache.	10
iii)	Explain write policy used in cache memory	10

Que. No.	Question	Max. Marks
Q4	Solve any **Two**	20
i)	Explain following parameters considered in designing Instruction Format of a microprocessor. • Addressing Modes • number of Operands • Registers • Address range	10
ii)	With neat diagram explain Microprogrammed Control Unit and its functions	10
iii)	Explain the term RAID Explain all possible RAID levels, with neat diagrams and examples.	10

Que. No.	Question	Max. Marks
Q5	Write notes on any **four**	20
i)	MESI Protocol with possible situations for state changes	5
ii)	Interrupt driven I/O mechanism and its advantages.	5
iii)	Hazards in Pipelining	5
iv)	Data transfer techniques used in DMA	5
v)	Analyze 2 level memory hierarchy with following specifications Calculate Average access time,	5
vi)	Explain following Instructions of X86 1. MOV AX, BX 2. MOV [SI],CX 3. DIV CL 4. PUSH BX 5. CALL N1	5

	Cache Memory (M1)	Main Memory (M2)
Size	4K	64K
Hit ratio	0.9	
Access time	10 ns	110 ns

SOMAIYA VIDYAVIHAR UNIVERSITY

09.06.2023(E)

Semester: August 2022 – December 2022		
Maximum Marks:100	Examination: ESE Examination – KT	Duration: 3hrs
Programme code: 116U01 Programme: BTech Computer Engineering	Class: SY	Semester: III (SVU 2020)
Name of the Constituent College: K. J. Somaiya College of Engineering	Name of the department: COMPUTERS	
Course Code: 116U01C303	Name of the Course: Computer Organization and Architecture	
Instructions: 1)Draw neat diagrams 2)Assume suitable data if necessary		

Question No.		Max. Marks
Q1 (a)	Explain page replacement algorithms, and find out page faults for the following string using LRU 2 3 2 1 5 2 4 5 3 2 5 2 (Assume cache size of 3 pages).	10
Q1 (b)	Explain Flynn's classification of the parallel computer.	10
Q2 (a)	Draw 5 state instructional pipelining. OR a) Differentiate between SRAM and DRAM units. b) Hardwired control unit and Microprogrammed control unit.	10
Q2 (b)	With a neat sketch explain the design of the control unit of a basic computer	10
Q3 (a)	Using Restoring Division algorithm perform 448 / 17. OR Explain the flowchart algorithm for floating-point addition and subtraction.	10
Q3 (b)	Write the format of the microinstruction and micro-operations for the control memory.	10
Q4 (a)	What is the cache coherence problem? Explain various protocols to handle it. OR Explain cache memory organization with Associative mapping. Explain how it improves memory access time.	10

Q4 (b)	Explain DMA-based data transfer techniques for I/O devices.	10
Q5 (a)	What is virtual memory? Explain the role of paging & segmentation in virtual memory.	10
Q5 (b)	Write a short note (5 marks each) Solve any two a) Booth's multiplication flowchart b) Applications of micro programming c) PCI bus features. d) IEEE 754 floating point formats	10

27.01.2023 (E)

SOMAIYA VIDYAVIHAR UNIVERSITY

Semester: August 2022 – December 2022 – (Jan-2023)		
Maximum Marks: 100 Examination: ESE Examination DSY (Reg+RT) Duration:3 Hrs.		
Programme code: 01 Programme: Computer Engineering	Class: SY	Semester:III (SVU 2020)
Name of the Constituent College: K. J. Somaiya College of Engineering	Name of the department: Computer	
Course Code: 116U01C303	Name of the Course: Computer Organization and Architecture	
Instructions: 1)Draw neat diagrams 2) All questions are compulsory 3) Assume suitable data wherever necessary		

Que. No.	Question	Max. Marks
Q1	Solve any **Four**	20
i)	Represent 43.8765 in single and double precision floating point formats	5
ii)	Compare Vertical and Horizontal microinstructions of control unit	5
iii)	Write the microinstructions for the following instruction ADD R1,(R2)	5
iv)	Assume that there are 3 page frames which are initially empty. If the page reference string is 1,2,3,4,2,1,5,3,2,4,6,5, what will be the number of page faults using the optimal page replacement policy?	5
v)	Explain different Cache write policies	5
vi)	Give five important features of a PCI bus	5

Que. No.	Question	Max Marks
Q2 A	Solve the following	10
i)	Explain the stages of a 6 stage pipeline. Briefly explain when does a pipeline stall.	5
ii)	Explain any two pipelining hazards that need to be avoided for correct program execution	5
	OR	
Q2 A	What is interrupt? Explain the interrupt cycle in an instruction cycle execution. Hence explain Interrupt driven I/O	10
Q 2 B	Solve any **One**	10
i)	Multiply 18 with -18 using Booth's Multiplication algorithm	10
ii)	Explain the restoring division and solve using restoring division 121/5	10

Que. No.	Question	Max. Marks
Q3	Solve any **Two**	20
i)	Compare Paging with Segmentation	10
ii)	What is Cache Coherence problem, Explain MESI Protocol to solve cache coherence problem in uniprocessor and multiprocessor systems	10
iii)	A computer system has main memory consisting of 16GB and 4K cache organized in 4 way-set-associative manner, and 32 bytes per block. Calculate the number of bits in each of TAG, SET and WORD fields of the main memory format.	10

Que. No.	Question	Max. Marks
Q4	Solve any **Two**	**20**
i)	Explain instruction format and basic instruction cycle with the help of neat diagram	10
ii)	Explain microprogrammed Control unit in detail	10
iii)	Compare Bit recoding and Booth's multiplication algorithm for multiplication, Which ot the two is faster. Demonstrate giving one example	10

Que. No.	Question	Max. Marks
Q5	Write short notes on any **four**	**20**
i)	Non restoring Division and its advantages over restoring division	5
ii)	Comparison of RISC vs CISC architectures	5
iii)	Page Replacement Algorithms	5
iv)	MIMD and SIMD with one practical example of each	5
v)	DMA data transfer modes	5
vi)	RAID Memory levels	5

23-12-2022(E)

SOMAIYA VIDYAVIHAR UNIVERSITY

Semester: August 2022 – December 2022		
Maximum Marks: 100 **Examination: ESE Examination**		**Duration:3 Hrs.**
Programme code: 01 **Programme: Btech Computer Engineering**	**Class:** **SYBTECH**	**Semester: III(SVU 2020)**
Name of the Constituent College: **K. J. Somaiya College of Engineering**	**Name of the department: Computer**	
CourseCode: 116U01C303	**Name of the Course: Computer Organisation and Architecture**	
Instructions: 1)Draw neat diagrams 2) All questions are compulsory **3) Assume suitable data wherever necessary**		

Que. No.	Question	Max. Marks
Q1	Solve any **Four**	**20**
i)	Explain the function of each functional unit in computer system	5
ii)	List features of PCI bus structure	5
iii)	What is micro programmed control unit ?	5
iv)	What is use of input output module ?	5
v)	Explain the application of microprogramming	5
vi)	List the different replacement algorithms in cache	5

Que. No.	Question	Max. Marks
Q2 A	Solve the following	**10**
i)	Explain SCSI bus standards	5
ii)	Explain restoring division algorithm and divide 8/3	5
	OR	
Q2 A	Explain different addressing modes of 8086	10
Q 2 B	Solve any **One**	**10**
i)	Draw and explain different RAID levels	10
ii)	What is DMA? Also explain the different modes of data transfer of DMA	10

Que. No.	Question	Max. Marks
Q3	Solve any **Two**	**20**
i)	Write note on Programmed Input output technique.	10
ii)	Write note on Flynn's classification	10
iii)	Compare paging and segmentation	10

Que. No.	Question	Max. Marks
Q4	Solve any **Two**	**20**
i)	What is virtual memory? Discuss how virtual address is converted to physical address	10
ii)	Explain six stage instruction pipeline and which unit take care of each stage	10
iii)	Explain floating point representation IEEE standard format	10

Que. No.	Question	Max. Marks
Q5	(Write notes / Short question type) on any **four**	**20**
i)	Explain the function of SCSI bus	5
ii)	What is an interrupt?	5
iii)	Compare RISC and CISC	5
iv)	Explain the set associative cache	5
v)	When is the Booth's algorithm less efficient ?	5
vi)	Discuss the pipeline hazards	5