Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**07 /08 /2023**	**Batch No:**	**C2**
Faculty Name:		**Roll No:**	**16010122267**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 3

Title: 4:1 Multiplexer and 3: 8 Decoder

Aim and Objective of the Experiment:

To design and implement a 4:1 multiplexer and 3: 8 Decoder

COs to be achieved:

CO2: Use different minimization technique and solve combinational circuits.

Tools used:

Trainer kits

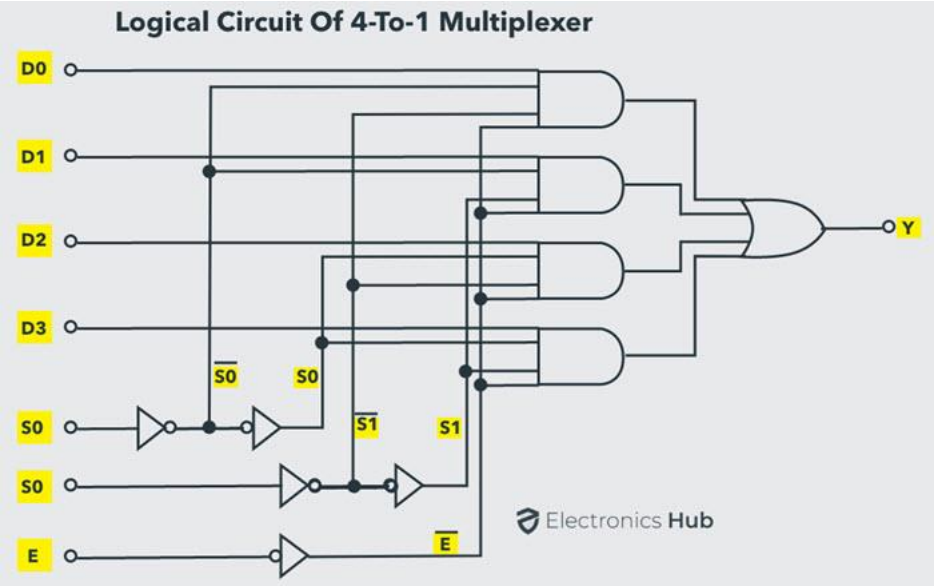
Theory:

Multiplexer: Multiplexer is a special type of combinational circuit. It is a digital circuit that selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the select lines. To select n inputs we require m select lines, such that $2^m=n$. Depending on the digital code applied at the select inputs, one out of the n data sources is selected and transmitted to a single output.

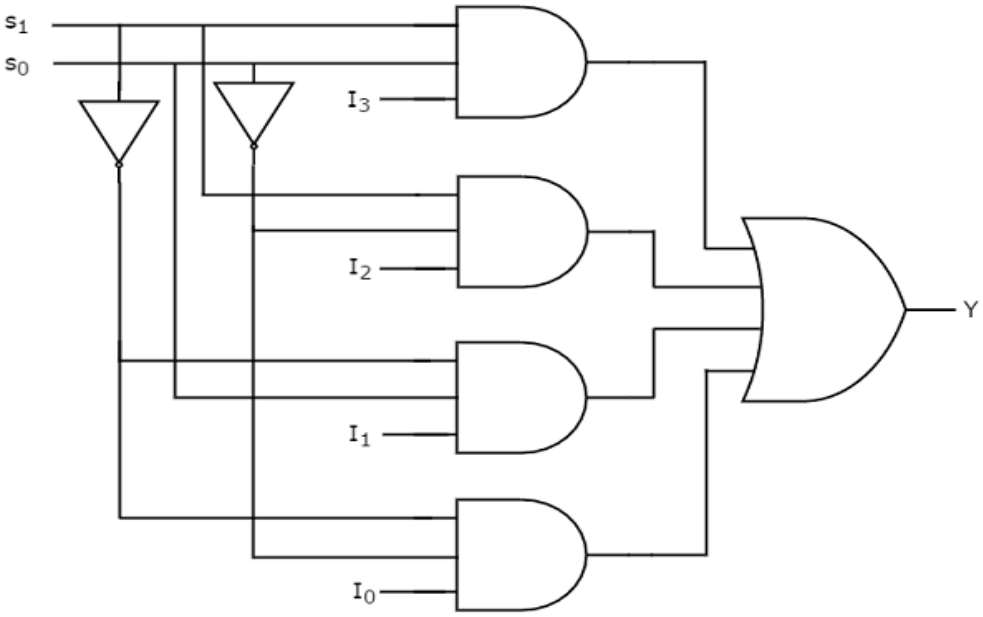
Decoder: A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is a one-to-one mapping from input code words into output code words. The general structure of a decoder circuit is shown in the Figure below. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. The most commonly used input code is an N-bit binary code, where an N-bit word represents one of 2^N different coded values. Normally, they range from 0 through $2^N - 1$. The input code lines select which output is active. The remaining output lines are disabled.

Implementation Details:

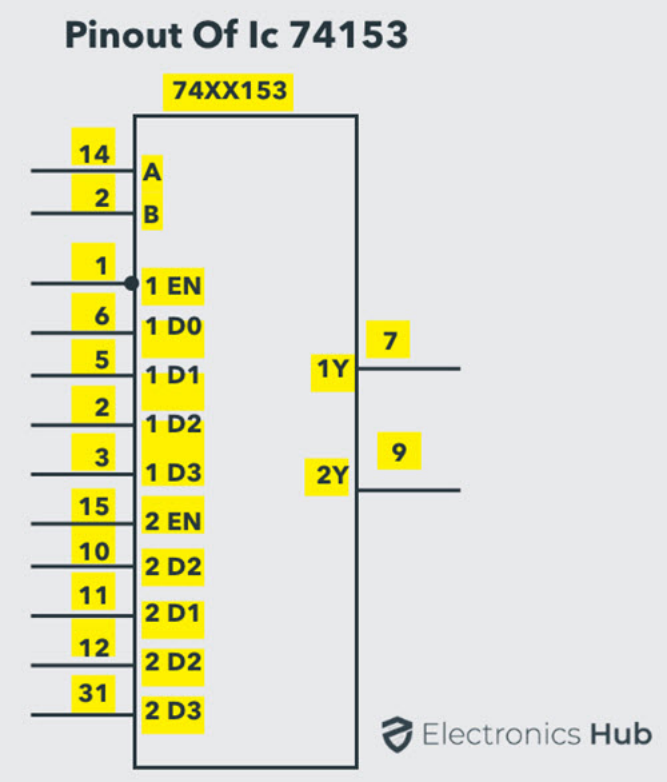
4:1 Multiplexer Block Diagram



4:1 Multiplexer Circuit



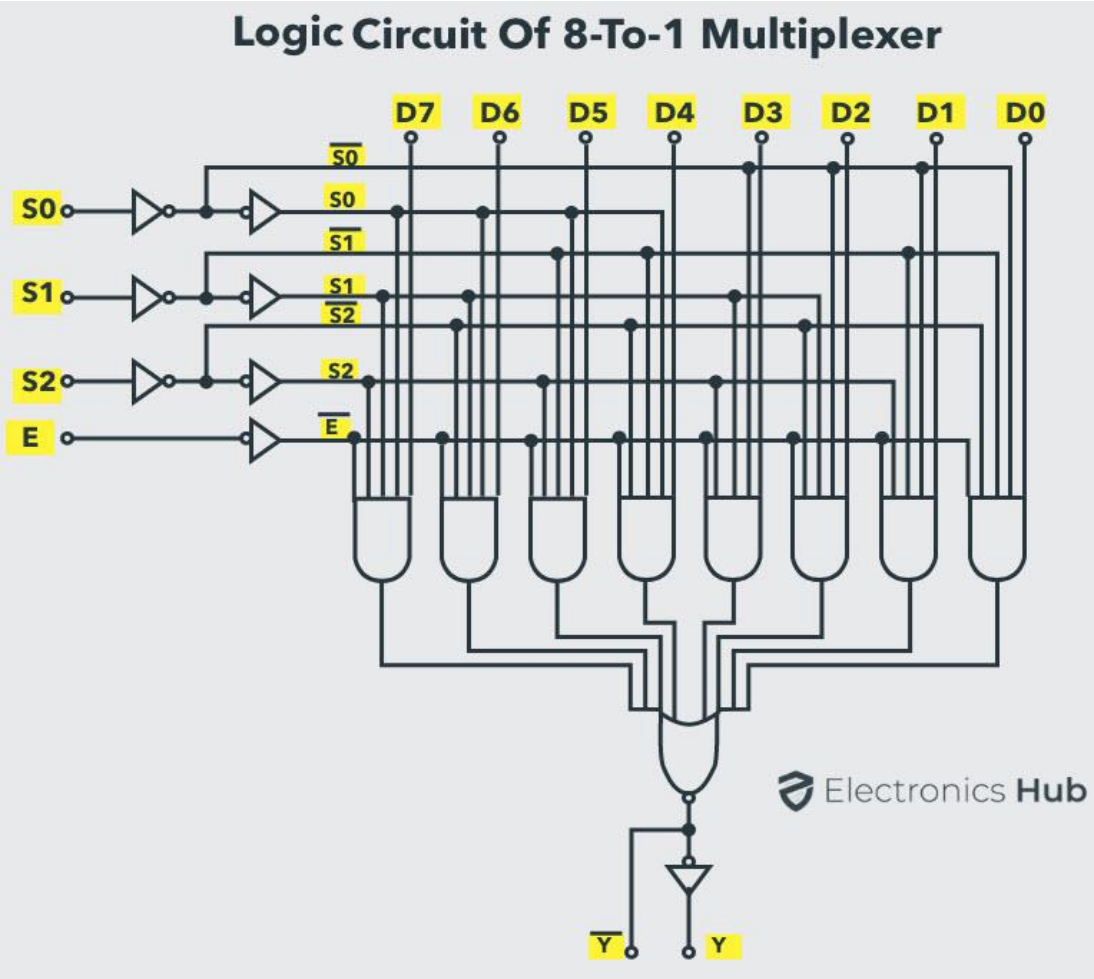
Pin Diagram IC74153



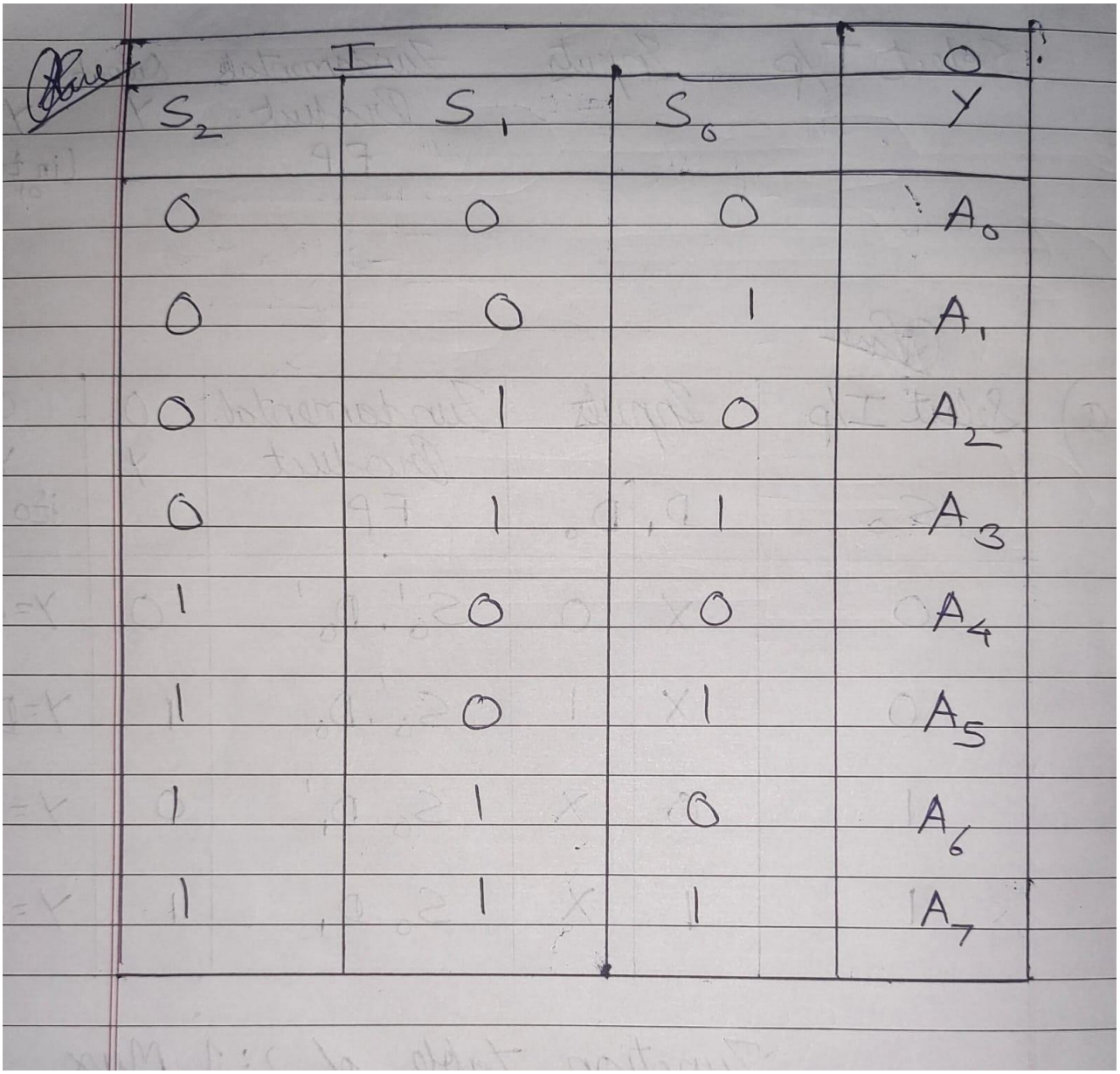
Implementation Details of 8:1 MUX

An 8-to-1 multiplexer consists of eight data inputs D0 through D7, three input select lines S0 through S2 and a single output line Y. Depending on the select lines combinations, multiplexer selects the inputs.

Circuit Diagram of 8:1 MUX

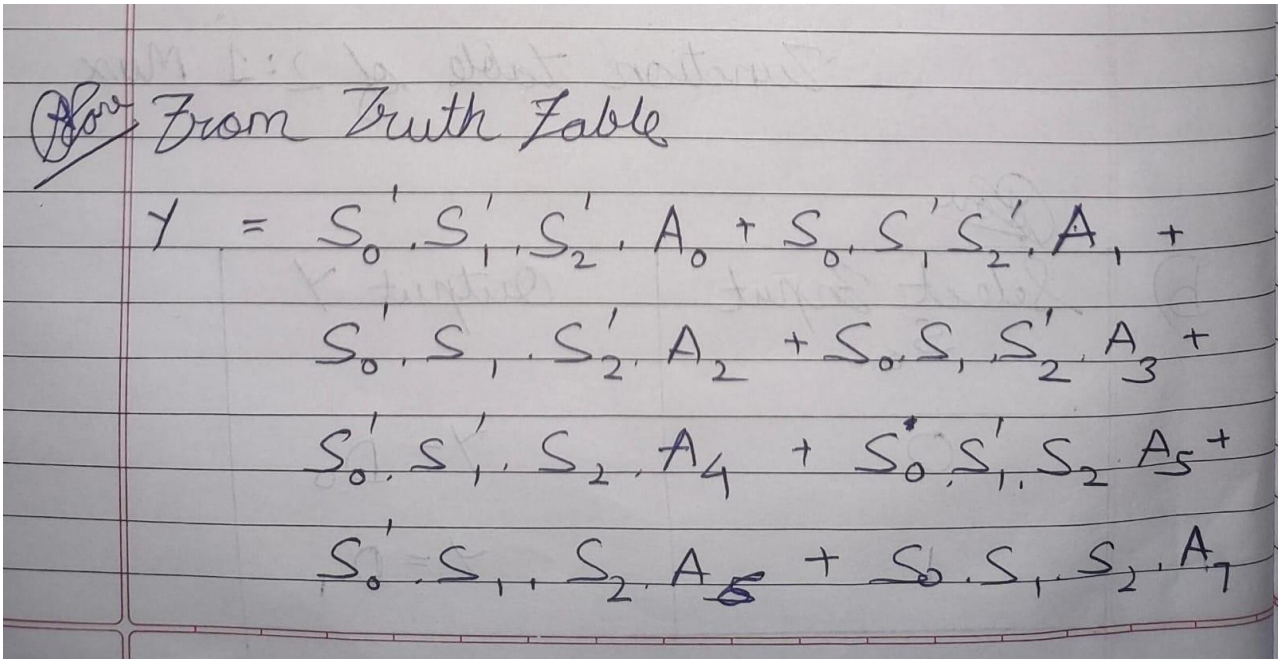


Truth Table for 8:1 Multiplexer

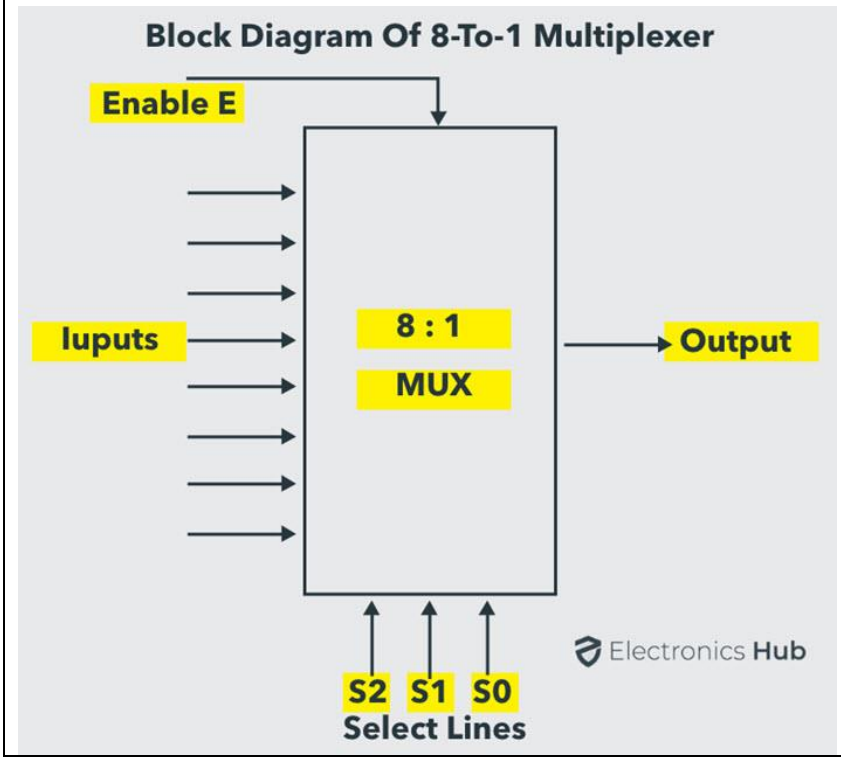


S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

From Truth Table:



Pin diagram: IC 74151



Implementation Details

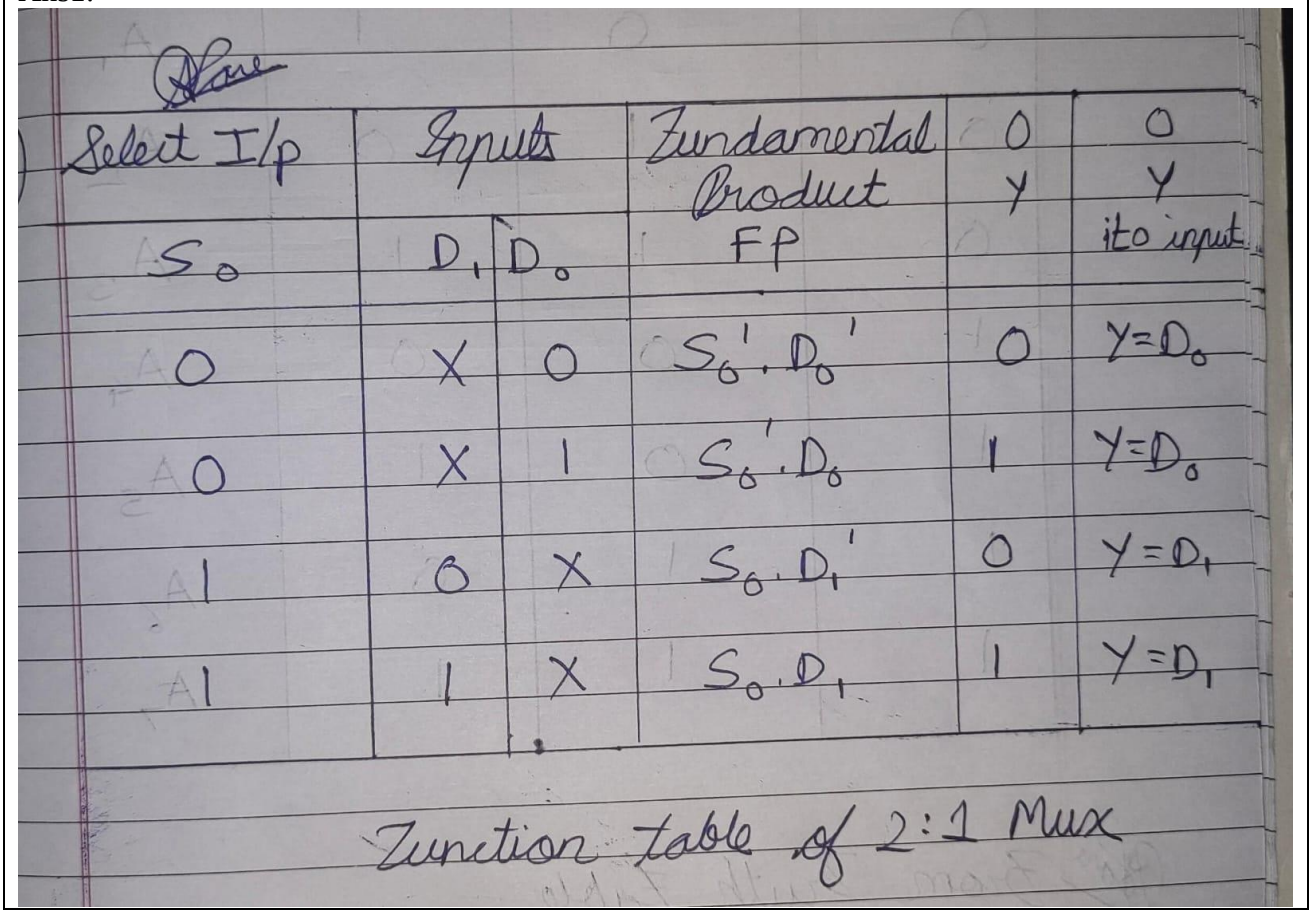
Procedure:

1) Locate the IC 74153 and place the IC on trainer kit.
2) Connect VCC and ground to respective pins of IC trainer kit.
3) Implement the circuit as shown in the circuit diagram.
4) Connect the inputs to the input switches provided in the trainer kit.
5) Connect the outputs to the switches of O/P LEDs
6) Apply various combinations of inputs according to the truth table and observe the condition of LEDs.
7) Note down the corresponding output readings for various combinations of inputs.

Post Lab Subjective/Objective type Questions:

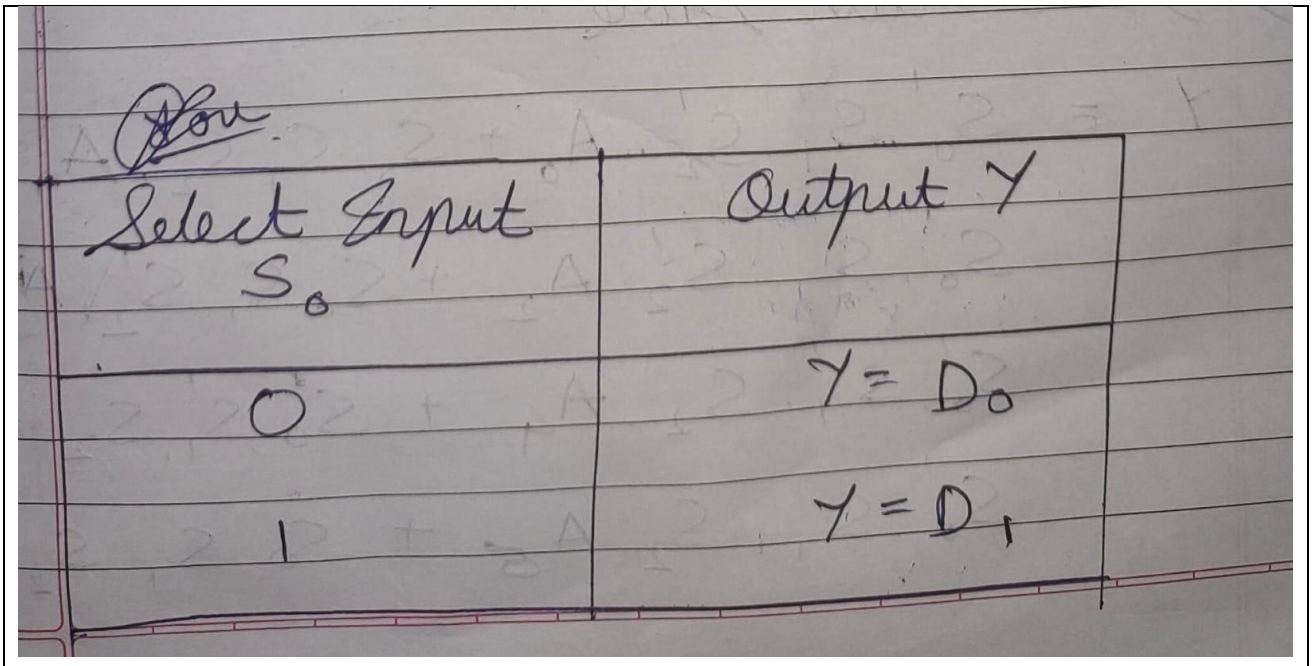
1. Design and verify a 2:1 multiplexer using logic gates.
2. Build an 8:1 multiplexer using only 2:1 multiplexers.

Ans1:

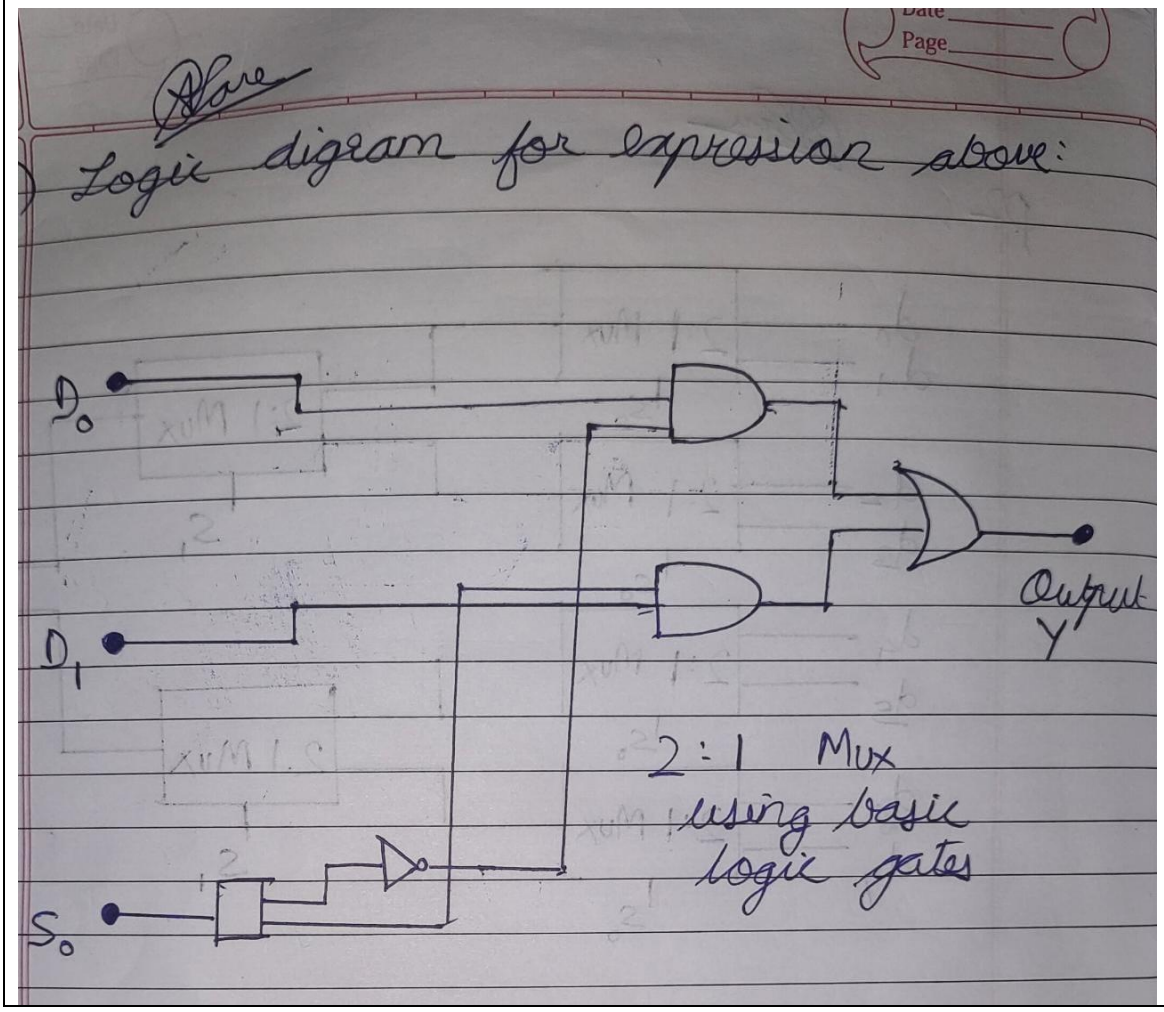


Select I/p	Inputs		Fundamental Product	O	O
S_0	D_1	D_0	FP	Y	Y i/p to input
0	X	0	$S_0' \cdot D_0'$	0	$Y=D_0$
0	X	1	$S_0' \cdot D_0$	1	$Y=D_0$
1	0	X	$S_0 \cdot D_1'$	0	$Y=D_1$
1	1	X	$S_0 \cdot D_1$	1	$Y=D_1$

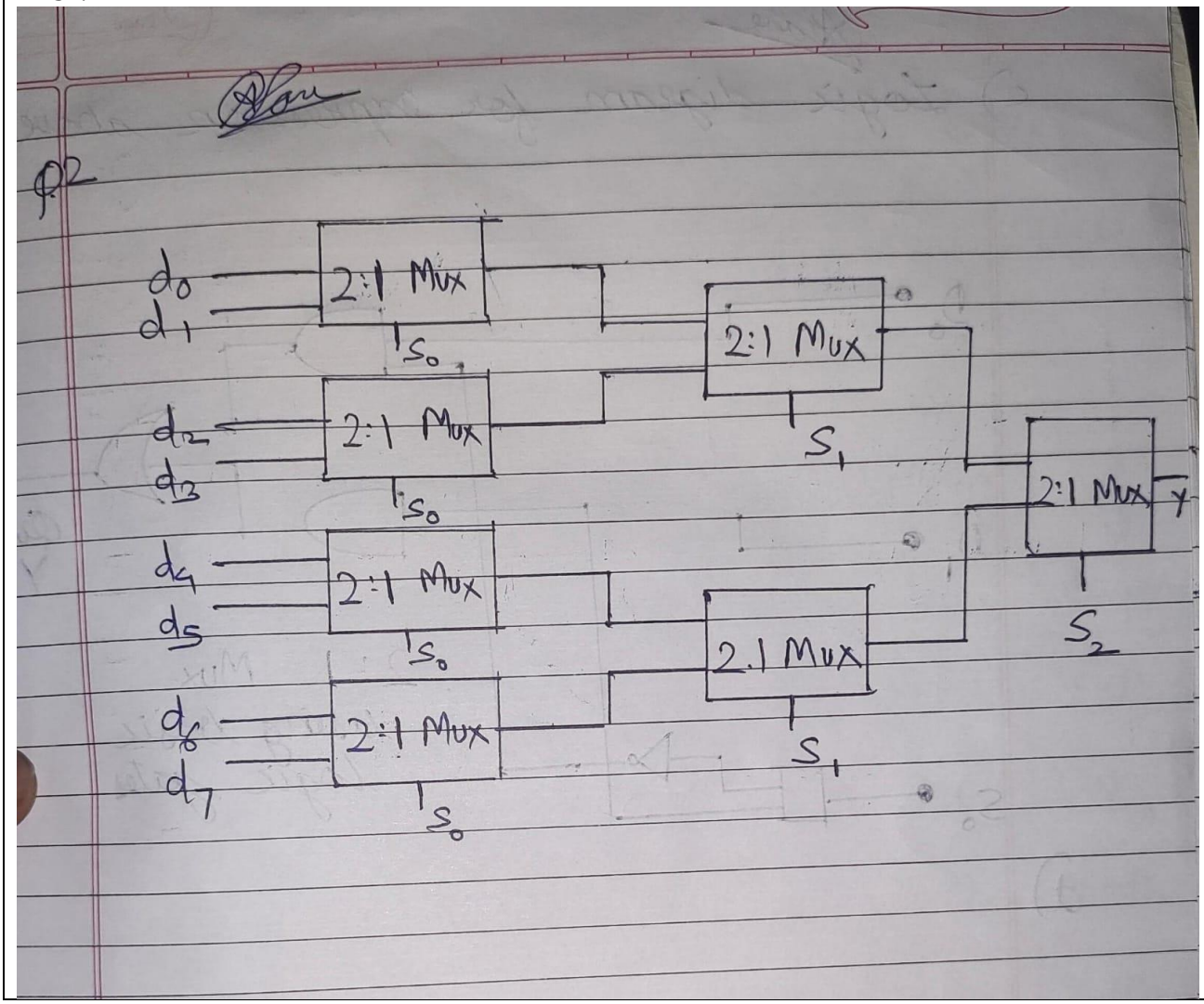
Function table of 2:1 Mux



Select Input S_0	Output Y
0	$Y = D_0$
1	$Y = D_1$



Ans2:



Conclusion:

We successfully implemented 4:1 multiplexer and 3:8 Decoder.

Signature of faculty in-charge with Date: