# Class D Amplifier — Design, BOM, PCB & Simulation README

**Target:** Single-channel Class-D audio amplifier — **5 W RMS into 8 Ω** using a single-supply **12 V** rail. (Scalable.)

**Scope:** - Discrete/analog-only design (no dedicated Class-D driver IC). Uses: op-amps, comparator/timer, MOSFETs, passive components, and discrete gate drive. - Full documentation: component selection rationale, schematic block diagram, PCB recommendations (layer stack, board size, trace widths), placement guidelines and layout notes. - A software simulation (ideal switching) that demonstrates PWM generation and LC output filtering.

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## 1) Overview & topology

We use a classic **two-stage** approach: - **Modulator**: produce a high-frequency triangular carrier (f_c = 100 kHz) and compare the audio signal against it to get PWM pulses. - **Power stage**: complementary half-bridge MOSFETs (P-channel high-side, N-channel low-side) driven by the PWM to switch the supply into the LC output filter. - **Output filter**: second-order LC low-pass tuned so that audio (20 Hz–20 kHz) passes and carrier energy is largely attenuated.

**Why this topology?** It’s simple to implement with op-amps/comparators and gives good audio performance for hobbyist/proof-of-concept designs without specialized driver ICs.

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## 2) Design requirements & targets

- Supply: **12 V DC** (single rail).
- Load: **8 Ω** loudspeaker.
- Output: **≈5 W RMS** into 8 Ω (I_rms ≈ 0.79 A, I_pk ≈ 1.12 A).
- PWM carrier: **f_c = 100 kHz** (>> audio bandwidth). This keeps switching losses moderate while being easy for common op-amps/comparators.
- LC filter cutoff: **f_cuttoff ≈ 30 kHz** (above audio band but well below switching). Second-order Butterworth-like damping.
- PCB: **4-layer** (Top signal, inner GND plane, inner PWR plane, Bottom signal) recommended for best SI and ground return.

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## 3) Block diagram

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Audio in --> Input gain / anti-alias filter --> PWM comparator --> Gate
driver --> Half-bridge MOSFETs --> LC low-pass --> Speaker
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                      Triangle carrier (from integrator / oscillator)
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## 4) Detailed circuit description (modules)

### A. Carrier (triangle) generator

- Implemented as an **op-amp integrator + comparator** relaxation oscillator (classic triangular oscillator). Comparator output switches integrator polarity producing linear ramps.
- Component choices: a **fast comparator** for crisp switching (e.g., LM311 family or any faster logic-level comparator) and an **op-amp with moderate slew rate** for integrator (slew > ~5–10 V/µs recommended at 100 kHz carrier). A dual audio op-amp (e.g., OPA2134 family or similar) can be used if it meets slew and supply-voltage specs.

**Behavior:** the comparator toggles at the integrator threshold → integrator integrates ±Vin to create triangle. Choose component values to set f_c.

### B. PWM comparator

- The audio (after preamp/gain) is compared with the triangle. The comparator produces PWM where duty ∝ audio amplitude.
- Use a comparator (or rail-to-rail op amp used as comparator) with clean output drive to the gate-driver stage.

### C. Output stage (half-bridge MOSFET pair)

- We use a **P-channel MOSFET (high-side)** and an **N-channel MOSFET (low-side)** in a totem-pole arrangement.
- Gate drive: PWM outputs from comparator are level shifted/inverted so that when comparator output is high, either high-side or low-side turns on appropriately. Add small gate resistors (10–100 Ω) to limit di/dt and ringing.

- MOSFET selection criteria: Vds > 1.5× Vsup (choose ≥30 V margin for safety if you plan to scale), Rds(on) low enough to keep conduction losses small for expected currents, low gate charge Qg if you want faster switching and lower gate-drive losses, and thermal rating to handle expected switching/conduction losses. Choose parts that are easy to source.

### D. Output LC filter

- Second order LC low-pass with cutoff f0 about 30 kHz. Design formula:
- $$f_0 = \frac{1}{2\pi\sqrt{LC}}$$
- For speaker RL (8 Ω) an approximate useful inductor value can be calculated with: $$L \approx \frac{R_L}{2\pi f_0}$$ (practical approximation used in many Class-D filter designs).
- Choose an L with low DC resistance and rated current > I_pk. Choose a C that is non-polar, low ESR, good AC rating (polypropylene or film caps preferred for audio path).

### E. Power supply & decoupling

- Use local decoupling: 10 µF (electrolytic/MLCC) + 0.1 µF ceramic close to MOSFET power pins and op-amp supply pins. A strong ground plane and short decoupling loops are essential.

### F. Protection & snubbers

- Add snubber (RC or RCD) across MOSFETs or across the output to tame switching spikes. Add TVS if you expect transients. Add a current sense resistor if you want overcurrent protection.

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## 5) Component selection & reasoning (BOM — suggested examples)

> **Note:** these are example families. Substitute equivalents that meet the specs for your project.

- **Comparator (PWM comparator + Schmitt):** LM311 / LM393 family (single comparator OK) — choose faster variants if you increase carrier frequency.
- **Integrator op-amp:** OPA2134 (audio op-amp with decent slew), or OPA350 / TLV237x (check slew/rail-to-rail if 12 V single-supply). You need slew ≥ ~5–10 V/µs for 100 kHz triangular waves.
- **MOSFETs:** Low-Rds(on), logic-level types with low Qg. Examples (as reference): IRLZ44N (N), IRF9Zxx for P (or modern SMD P-channel like SI2301 or AOZ P-channel) — pick devices rated ≥30 V, Id > 10 A, low Rds(on). For a 5 W design, parts with low gate charge and Rds(on) ~10–50 mΩ are fine.
- **Gate resistors:** 10–100 Ω (1/4 W)
- **Bootstrap / level-shift:** For pure discrete approach we use P-channel for high-side, which simplifies gate drive.
- **Inductor:** 100–470 µH (estimate — final value calculated under "Calculations"). Must handle peak current >1.2 A without saturating and have low DCR.
- **Capacitor (output):** 1 µF – 2.2 µF film (non polar) or high-voltage MLCC bank. Voltage rating at least 50 V for margin on switching.
- **Decoupling caps:** 10 µF electrolytic (low ESR), 0.1 µF ceramic (X7R) near supply pins.

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## 6) Calculations (values used in the example)

**Design choices used in this README (worked example)** - Supply: 12 V - Target: 5 W RMS into 8 Ω - f_pwm = 100 kHz - f_filter (corner) ≈ 30 kHz

Using the approximate formula for L (practical class-D rule of thumb):

$$L \approx \frac{R_L}{2\pi f_c}$$

If R_L = 8 Ω and f_c = 30 kHz,

$$L \approx \frac{8}{2\pi \times 30000} \approx 42.4\ \mu H.$$

Choose **L = 47 µH** (standard value). Then compute C for fc with formula fc = 1/(2π sqrt(L C)). Solving for C:

$$C = \frac{1}{(2\pi f_c)^2 L}$$

With L = 47 µH and fc = 30 kHz, we get C ≈ 1.87 µF. Use **C = 2.2 µF** (polypropylene or MLCC bank).

This gives a gentle roll-off above 30 kHz; choose component quality (low DCR for L, low ESR for C) to preserve fidelity.

**Current/thermal**: For 5 W into 8 Ω, I_rms ≈ 0.79 A. Peak current ≈ 1.12 A. Use traces and MOSFETs rated for at least **3 A continuous** and higher pulsed peaks. Make sure MOSFET Rds(on) keeps conduction losses low.

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## 7) PCB design: layers, board size, stackup, trace widths and via strategy

**Recommended board:** 4-layer PCB for good ground referencing and power distribution

**Stackup (top → bottom)** - L1 Top: signal & components - L2 GND plane (solid) - L3 PWR plane (V+) - L4 Bottom: signal & routing

**Board size:** approximately **80 mm × 50 mm** for single channel (allow extra room for heatsinking and connectors). For stereo two channels use ~130 mm × 80 mm.

**Trace width guidance:** - Output traces carrying speaker current should be sized for worst case currents. For our 5 W target (peak ≈ 1.2 A), using IPC-2152 guidelines a **1 oz copper** outer-layer trace of **50 mil (≈1.27 mm)** will comfortably carry ~3 A with small temperature rise — giving margin. (Use inner plane stitching or add copper pour if you want smaller width.) For the power input (V+) use **40–80 mil** depending on length.

(References: IPC-2152 calculators and manufacturers provide wide tables — verify with your board house.)

**Via strategy:** - Use multiple vias to connect power plane to top/bottom power pours (stitching). For MOSFET thermal relief use multiple thermal vias under the pad if placing MOSFET on top with exposed pad.

**Heatsinking:** - For low-power (5 W) with efficient class D the MOSFETs may not need large heatsink, but provide thermal copper area and consider a small aluminum heatsink if >3–5 W dissipation predicted.

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## 8) Component placement & routing guidelines

- Place MOSFETs close to speaker connector and LC filter to minimize loop area of switching currents.
- Keep the gate-drive traces short. Place gate resistors close to MOSFET gates.
- Place decoupling capacitors as close as possible to MOSFET supply pins with shortest traces.
- Keep comparator/op-amp and oscillator away from large switching currents and ensure analog ground star connection into board ground plane.
- Place LC filter at the very edge close to speaker connector to keep EMI low.

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## 9) Simulation: approach and included code

**Approach used here (included in the repo):** - We simulate the modulation chain in Python (ideal switches): 1. Generate a 1 kHz audio sine. 2. Generate a 100 kHz triangle carrier. 3. Compare to produce PWM (ideal comparator). 4. Low-pass filter the PWM using the designed LC (simulated by a digital 2nd order IIR approximation or RLC continuous time solved numerically) to recover audio. - This simplified simulation uses ideal switches (no MOSFET switching transitions) but proves concept: PWM encodes the audio and LC recovers it.

The simulation script and plots are included in the repository portion of this README.

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## 10) Assembly, test plan, and measurement checklist

1. Visual inspection of the board, solder joints, orientation of polarized parts.
2. Power up without load; verify supply rails and that gate drive signals are present (use oscilloscope): check triangle and PWM on scope with probe ground short and be careful.
3. Connect small dummy load (10–20 Ω resistor) before connecting speaker.
4. Sweep audio frequency and measure THD, output amplitude, and overheating.
5. EMI testing: check for excessive HF emission; add snubbers or increase LC corner if necessary.

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## 11) Further improvements & scaling notes

- For higher powers and higher efficiency use N-channel high-side with a driver IC or bootstrap driver.
- For stereo, duplicate channels or add shared power filtering and separate analog input stages.
- If you increase PWM frequency above ~200 kHz, choose faster comparators/op-amps and MOSFETs with lower gate charge.

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## Files included:

- README (this file)
- `sim_pwm_lc.py` — Python simulation script (generates PWM, performs LC filtering, plots the waveforms)
- `schematic.png` — simple hand-drawn schematic (not included inline)

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**End of README**