# EEE Digital Assignment (Software)

## Logic Gates

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Registration Number: 16BCE0789

Slot: L11+L12

Batch: 10(B-Tech Computer Science (Core))

# LOGIC GATES

## AIM:

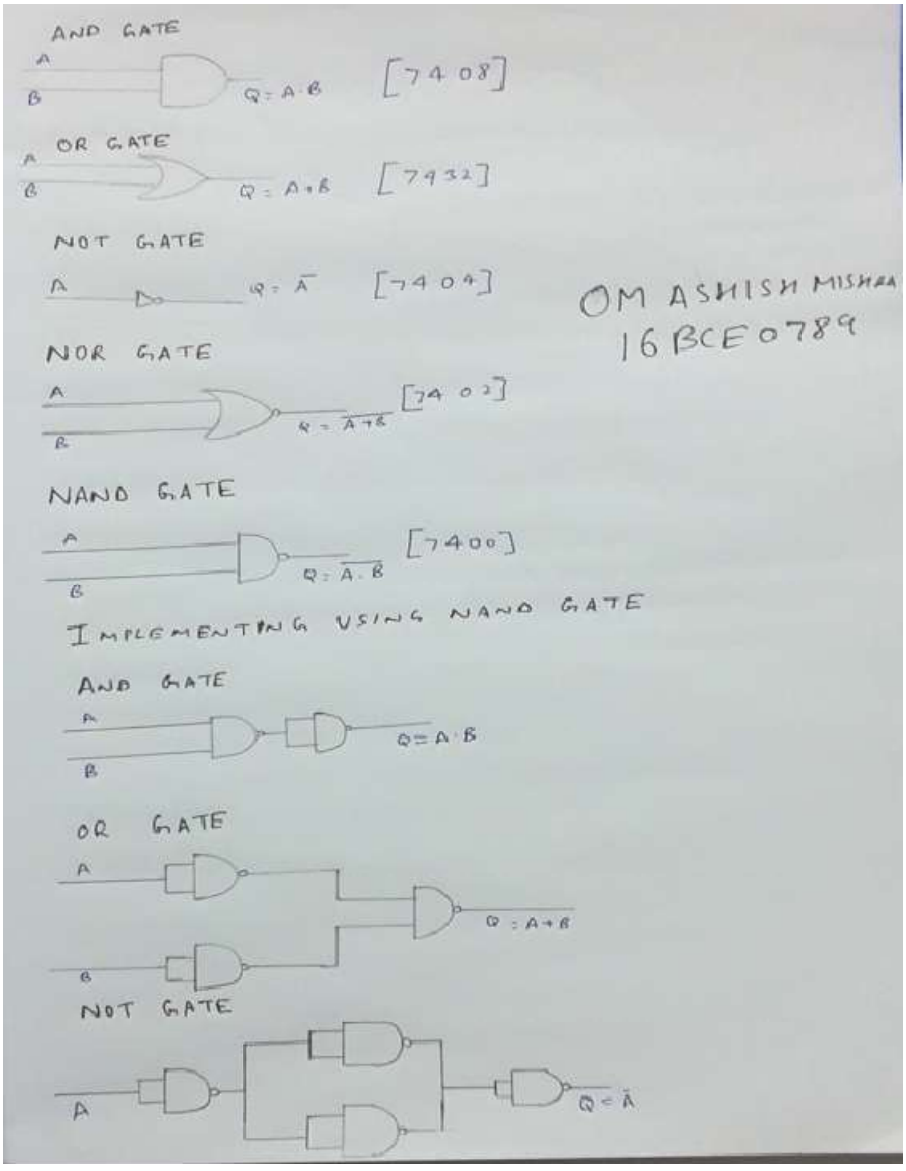
To from primary logic gates using Universal logic gate(NAND).

## APPARATUS/TOOL REQUIRED:

ORCAD / PSpice simulator - > **7400 Library – 7408, 7432, 7486, 7404,7402&7400**

Simulation Settings: **Analysis Type - Time Domain**
**Run to time - 8ms**

## CIRCUIT DIAGRAM:



## SIMULATION CIRCUIT DIAGRAM:

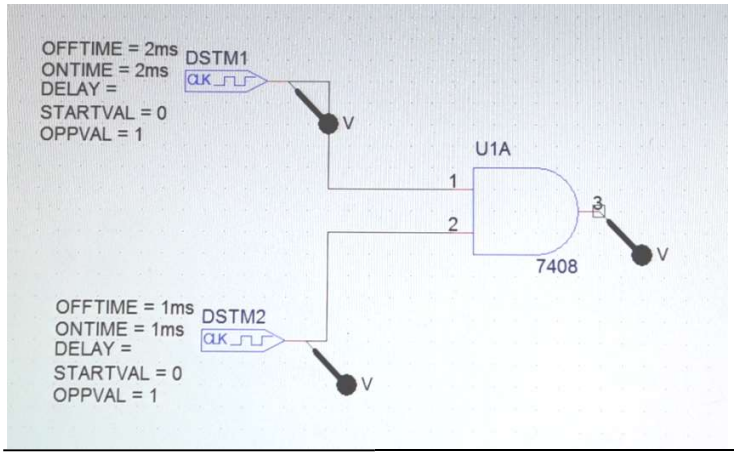



**Fig: AND GATE**

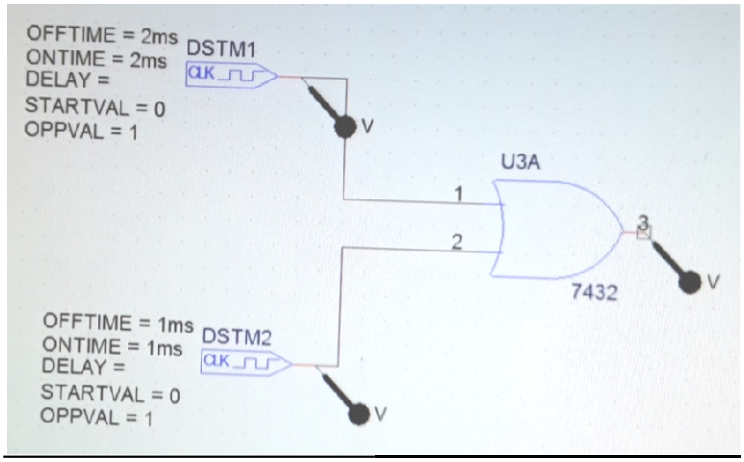



**Fig: OR GATE**

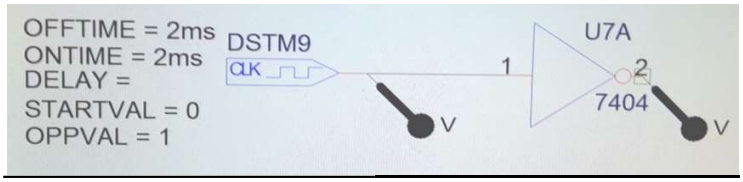



**Fig: NOT GATE**

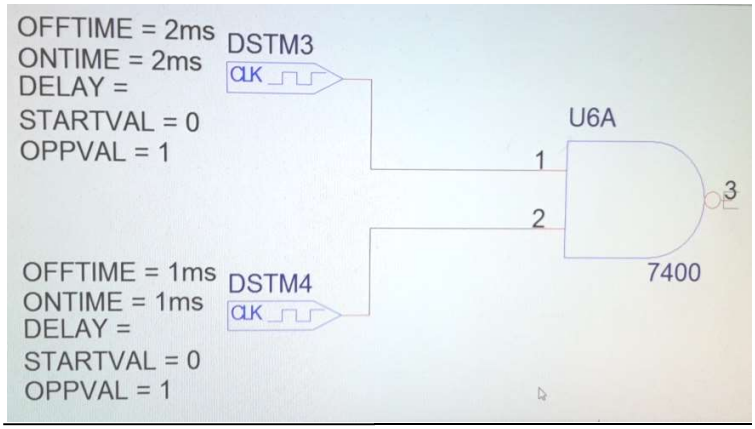



**Fig: NAND GATE**

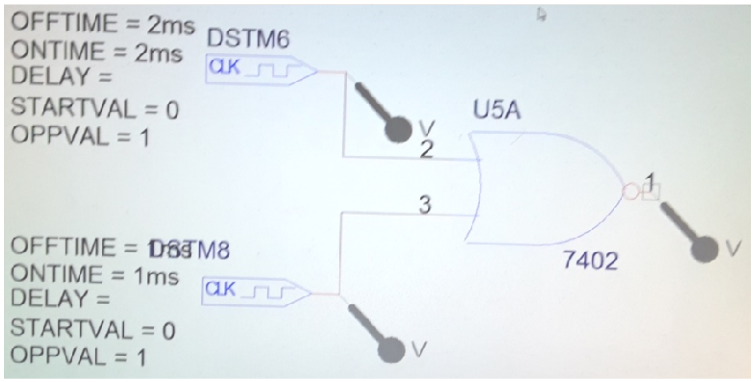



**Fig: NOR GATE**

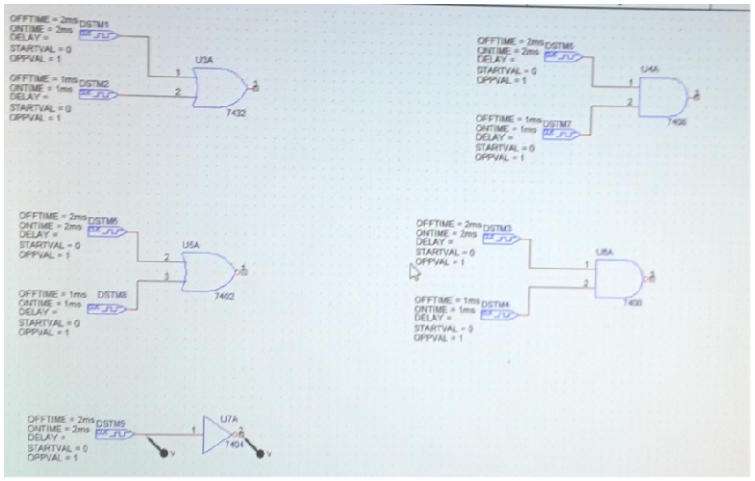


**Fig: ALL**

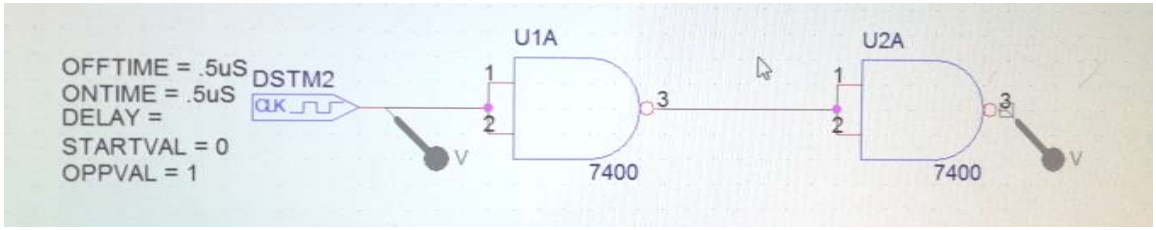



**Fig: AND Using NAND**

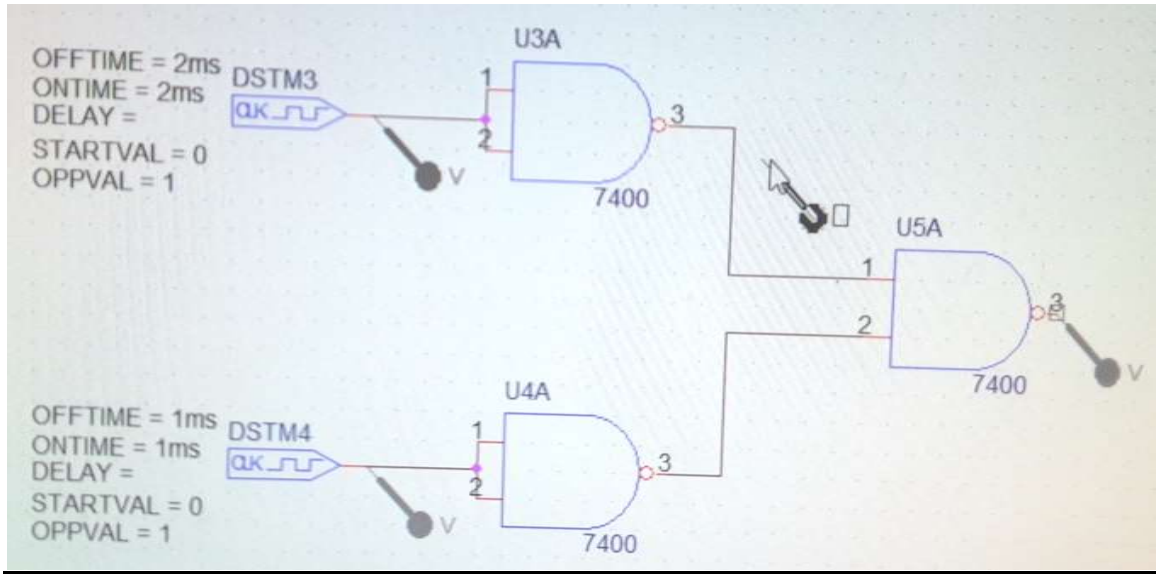



**Fig: OR Using NAND**

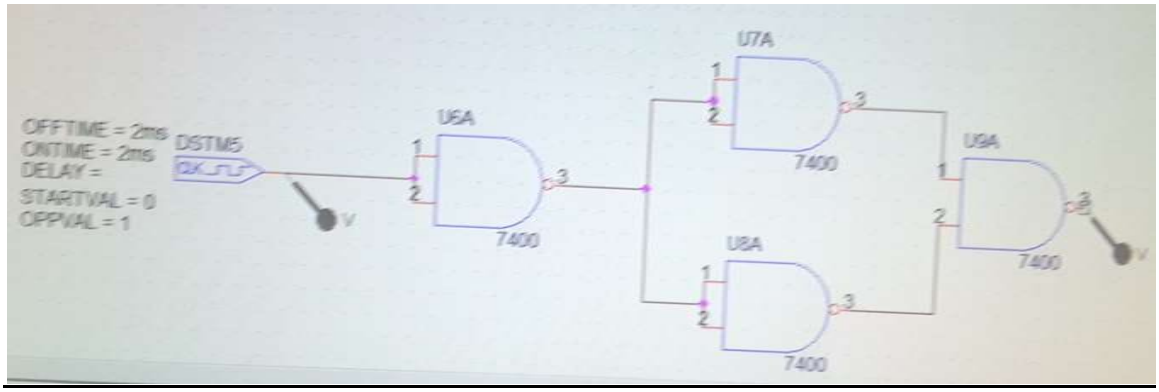



**Fig: NOT Using NAND**

## THEORY:

<table>
<tr><th>Type</th><th>Distinctive shape (IEEE Std 91/91a-1991)</th><th>Rectangular shape (IEEE Std 91/91a-1991 IEC 60617-12 : 1997)</th><th>Boolean algebra between A & B</th><th>Truth table</th></tr>
<tr><td>AND</td><td>  </td><td> 
</td><td>A.B</td><td>
<table>
<tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr>
<tr><td>A</td><td>B</td><td>A AND B</td></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
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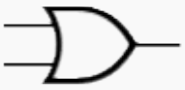
</td></tr>
<tr><td>OR</td><td>  </td><td> 
</td><td>A+B</td><td>
<table>
<tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr>
<tr><td>A</td><td>B</td><td>A OR B</td></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
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<table>
<tr>
<td>NOT</td>
<td>  </td>
<td> 
</td>
<td>Á</td>
<td>
<table>
<tr><th>NPUT</th><th>OUTPUT</th></tr>
<tr><td>A</td><td>NOT A</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td></tr>
</table>
</td>
</tr>
<tr>
<td>NAND</td>
<td>  </td>
<td> 
</td>
<td>(A.B)’</td>
<td>
<table>
<tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr>
<tr><td>A</td><td>B</td><td>A NAND B</td></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
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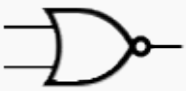
</tr>
<tr>
<td>NOR</td>
<td>  </td>
<td> 
</td>
<td>(A+B)’</td>
<td>
<table>
<tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr>
<tr><td>A</td><td>B</td><td>A NOR B</td></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
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</td>
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| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | 1 | 0 | 0 |
| | | | | 1 | 1 | 0 |

**PROCEDURE:**

Step 1: Open Capture CIS

Step 2: Click on the File button

Step 3: Click on New Project

Step 4: Select Blank Project

Step 5: Go to Library and click on Sources

Step 6: Select 7400 Library – 7408, 7432, 7486, 7404, 7402&7400

Step 7: Click on New Simulation

Step 8: Analysis Type - Time Domain

Step 9: Run to time – 8 ms (for 2 cycles)

Step 10: Apply it

Step 11: Then we run the simulated program

Step 12: Then we get the graph as the output.

## MODEL GRAPH:

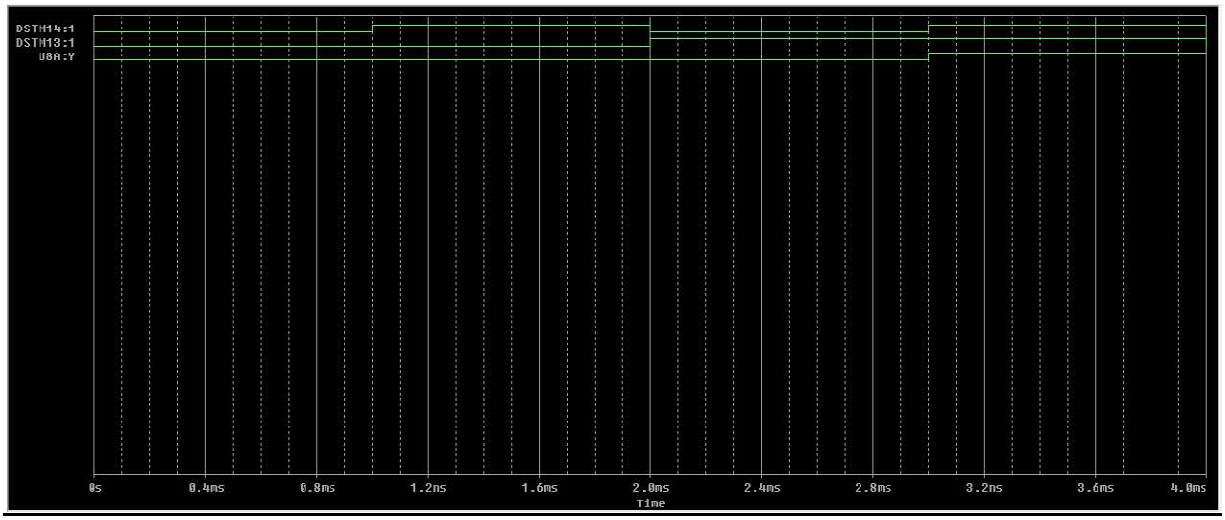


Fig: AND GATE

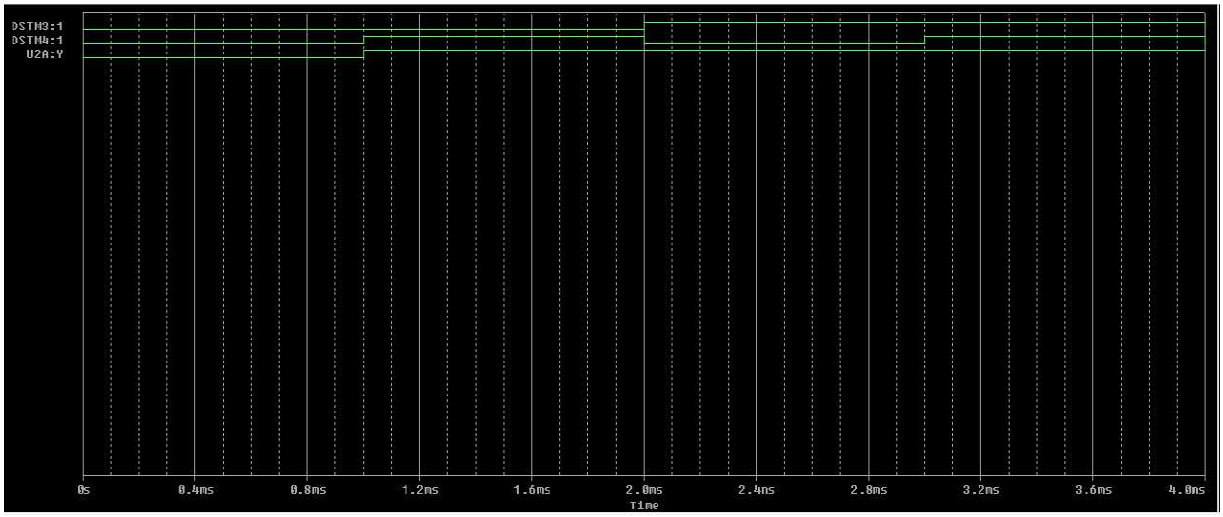


Fig: OR GATE

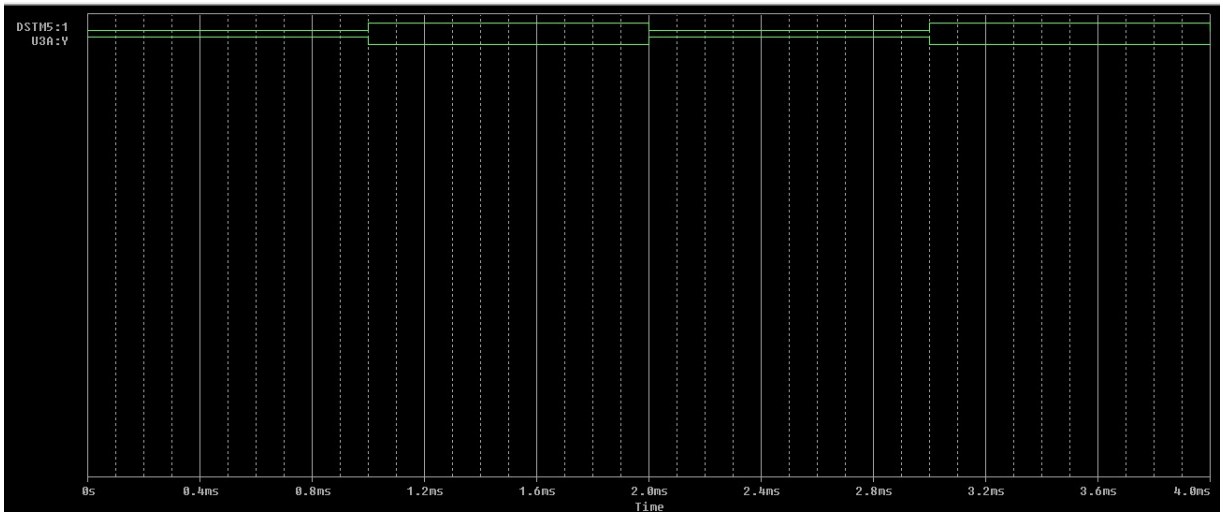


Fig: NOT GATE

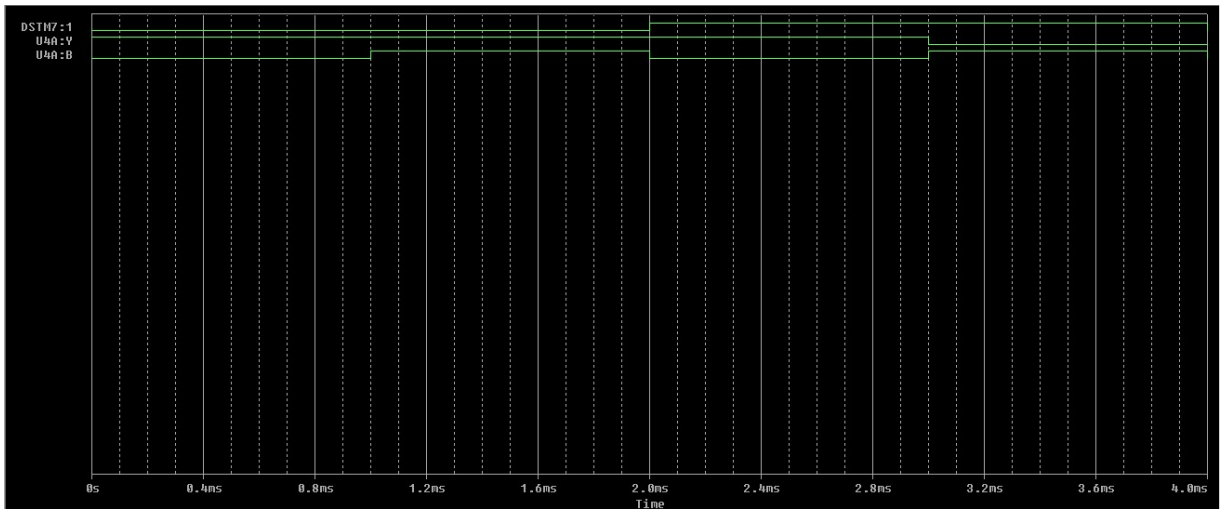


Fig: NAND GATE

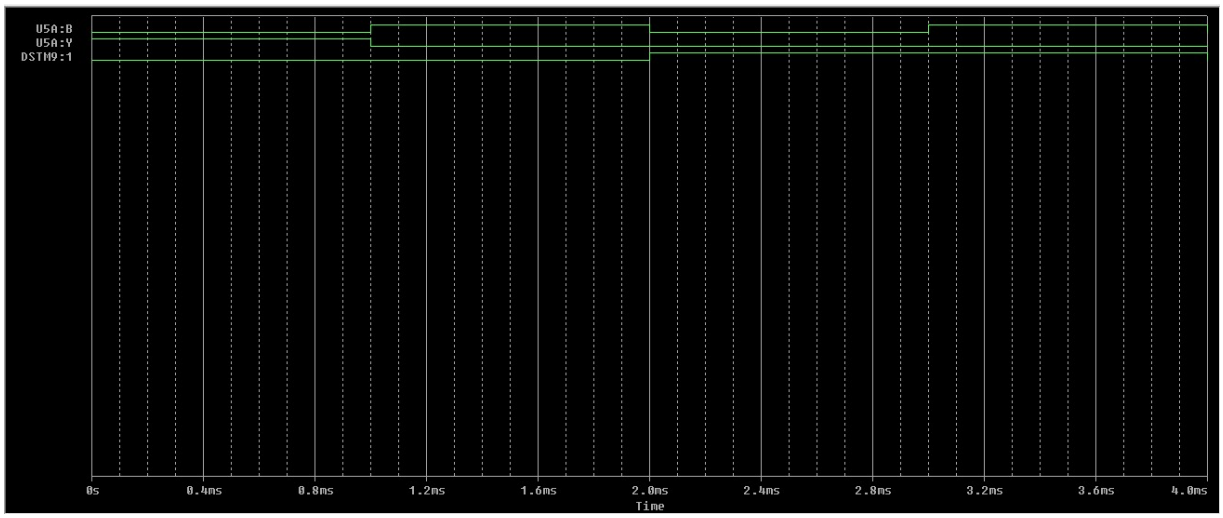


Fig: NOR GATE

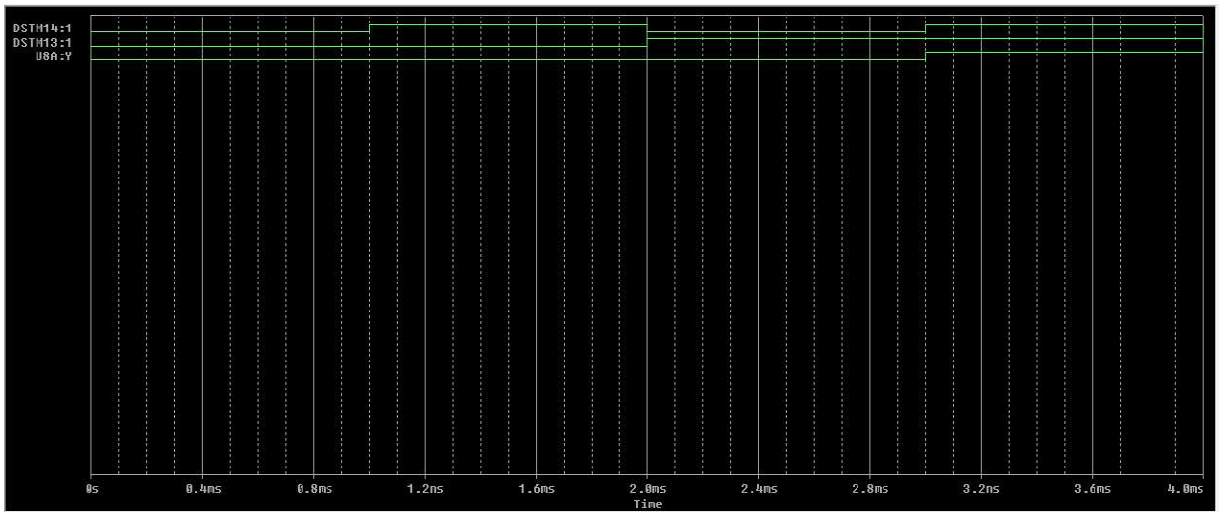


Fig: AND GATE USING NAND GATE

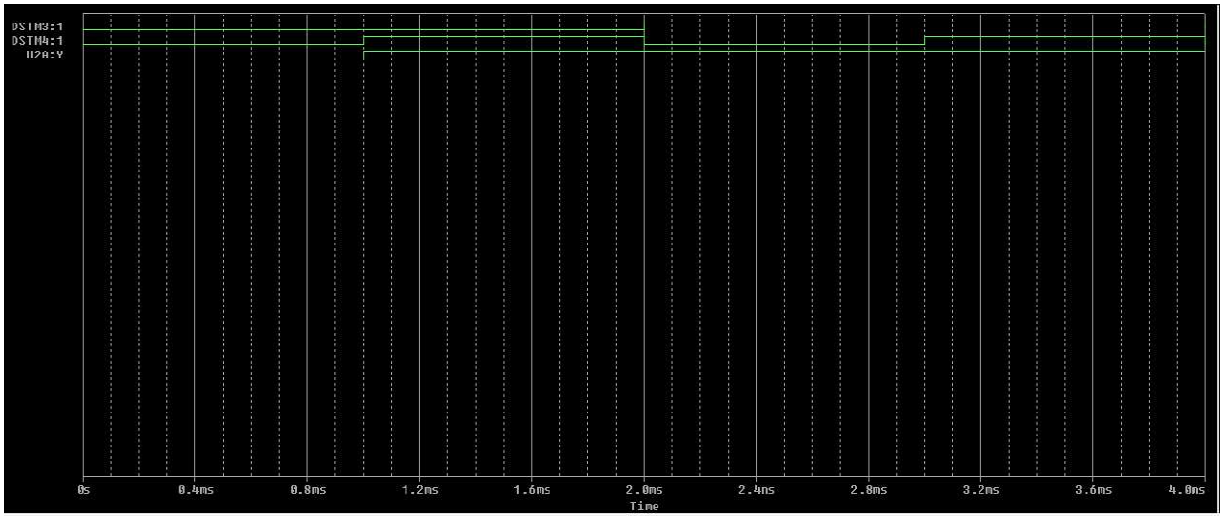


Fig: OR GATE USING NAND GATE

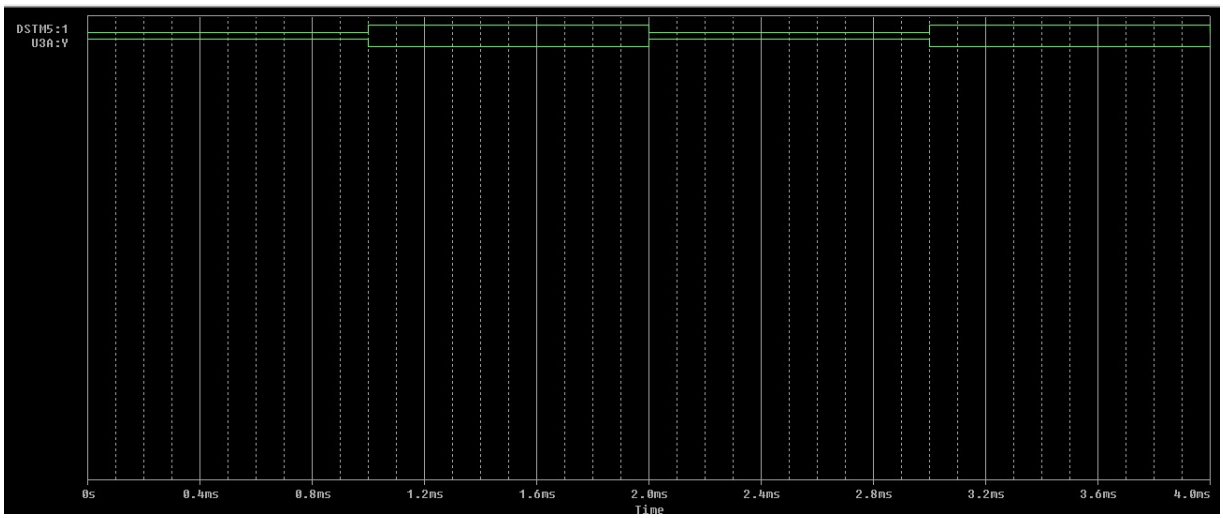


Fig: NOT GATE USING NAND GATE

## RESULT:

We also learned to use NAND GATE which is one of the Universal Gates and its implementation in formation of AND, OR, NOT Gates.

## INFERENCE:

From this experiment we have got a clear picture about the use of different gates(AND,OR,NOT,NAND,NOR).