CSE 2001

COMPUTER ARCHITECTURE AND ORGANIZATION

DIGITAL ASSIGNMENT I

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SLOT : B2

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(1) A computer employs RAM chips of 1024 x 8 and ROM chips of 512 bytes. Design the memory system which needs 2K x 32 of RAM, 1K x 8 of ROM and an interface unit with 128 registers.

Ans : RAM

$N \times M = 1024 \times 8$

$N' \times M' = 2000 \times 8$

ROM

$N \times M = 512 \times 8$

$N' \times M' = 1000 \times 8$

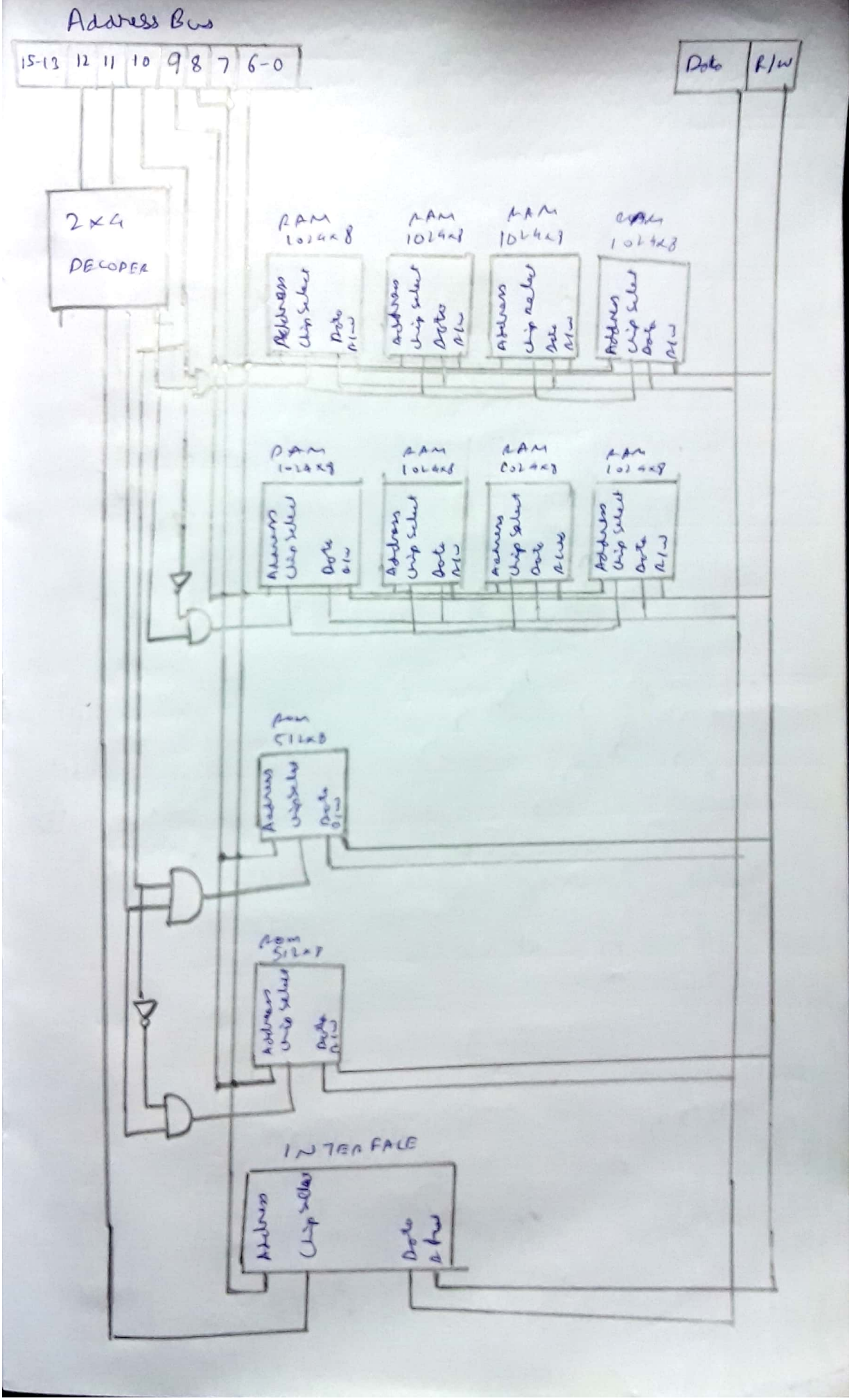
Interface : $N \times M = 128$

Requirements

Sr NO	Memory	N x W	N' x W'	P	Q	P*Q	X	y	z	Total
01	RAM	1024 x 8	2000 x 22	2	4	8	10	1	2	13
02	ROM	512 x 6	1000 x 8	2	1	2	9	1	2	12
03	Interface	128		1	1	1	7	0	2	9

Memory Address Map:

Component	Hexadimal Address		Address Bus															
	From	To	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1.1	0000	03FF				0	0	0	x	x	x	x	x	x	x	x	x	x
RAM 1.2	0000	03FF				0	0	0	x	x	x	x	x	x	x	x	x	x
RAM 1.3	0000	03FF				0	0	0	x	x	x	x	x	x	x	x	x	x
RAM 1.4	0000	03FF				0	0	0	x	x	x	x	x	x	x	x	x	x
RAM 2.1	0400	07FF				0	0	1	x	x	x	x	x	x	x	x	x	x
RAM 2.2	0400	07FF				0	0	1	x	x	x	x	x	x	x	x	x	x
RAM 2.3	0400	07FF				0	0	1	x	x	x	x	x	x	x	x	x	x
RAM 2.4	0400	07FF				0	0	1	x	x	x	x	x	x	x	x	x	x
ROM 1	0800	09FF				0	1	0	x	x	x	x	x	x	x	x	x	x
ROM 2	0C00	0DFF				0	1	1	x	x	x	x	x	x	x	x	x	x
INTERFACE	1000	107F				1	0					x	x	x	x	x	x	x



(2) A (a) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

(c) How many lines must be decoded for chip select? Specify the size of the decoder?

B A computer uses RAM chips of 1024×1 capacity.

(a) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?

(b) How many chips are needed to provide a memory capacity of 16K bytes. Explain in words how the chips are to be connected to the address bus.

Ans: A a) $N \times M = 128 \times 8$

$N' \times M' = 2048 \times 8$

$P = \frac{2048}{128} = 16 \quad Q = \frac{8}{8} = 1$

No of chips required $= P * Q = 16 * 1 = 16$

b)

Memory	N×M	N'×M'	P	Q	P×Q	x	y	z	Total
RAM	128×8	2048×8	16	1	16	7	4	0	11

Total 11 lines of the address bus

7 lines of address bus common to all chips

c) 4 lines must be selected for chip select

size of decoder is 4×16 Decoder.

B $N \times M = 1024 \times 1$

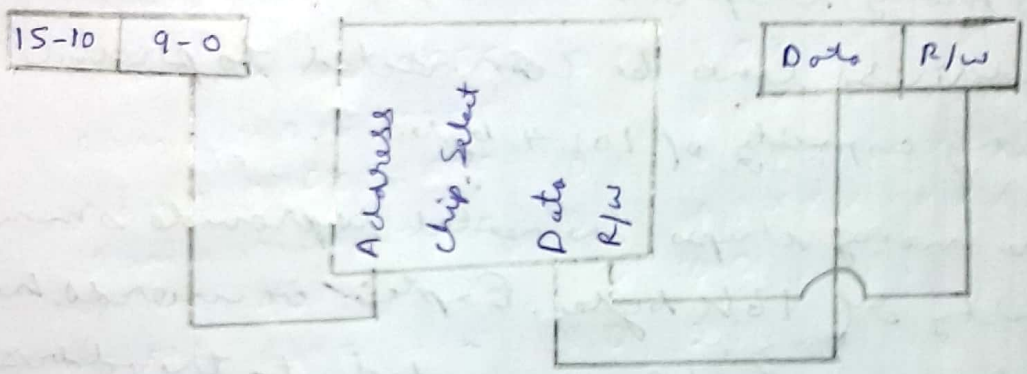
$N' \times M' = 1024 \times 1$

$P = 1 \quad Q = 1$

∴ No of chip required $= P \times Q = 1$

Memory	N x M	N'xM'	P	Q	P x Q	x	y	z	Total
RAM	1024x1	1024x1	1	1	1	10	0	0	10

Memory Address Map



$N \times M = 1024 \times 1$

$N' \times M' = 16K \times 1$

$P = \left\lceil \frac{16000}{1024} \right\rceil = 16 \quad Q = \frac{1}{1} = 1$

∴ No of chip required $= P \times Q = 16 \times 1 = 16$

Memory	N x M	N'xM'	P	Q	P x Q	x	y	z	Total
RAM	1024x1	16K x 1	16	1	16	10	4	0	14

We need 16 chips of 1024 x 1 RAM. We need 4x16 Decoder for selection of chips. We need 14 line of Address Bus. All chips will be connected in parallel.

(3). A computer employs RAM chips of 256×8 and ROM chips of 1024×8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. Assign 00 for RAM, 01 for ROM, and 10 for interface registers.

(a) How many RAM and ROM chips are needed?

(b) Draw memory-address map for the system.

(c) Give the address range in hexadecimal for RAM, ROM and interface.

(d) Show the chip layout for the above design.

Ans: RAM

$N \times M = 256 \times 8$

$N' \times M' = 2K \times 8$

ROM

$N \times M = 1024 \times 8$

$N' \times M' = 2K \times 8$

INTERFACE

4 REGISTERS

SNO	MEMORY	N×M	N'×M'	P	Q	P×Q	x	y	z	Total
01	RAM	256×8	2K×8	8	1	8	8	3	2	13
02	ROM	1024×8	4K×8	4	1	4	10	2	2	14
03	Interface	4		4	1	4	2	2	2	6

a) 8 RAM chips and 4 ROM chips needed.

COMPONENT	HEXADECIMAL ADDRESS		ADDRESS BUS															
	FROM	TO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1.1	0000	00FF		0	0	0	0	0			X	X	X	X	X	X	X	X
RAM 1.2	0400	04FF		0	0	0	0	1			X	X	X	X	X	X	X	X
RAM 1.3	0800	08FF		0	0	0	1	0			X	X	X	X	X	X	X	X
RAM 1.4	0C00	0CFF		0	0	0	1	1			X	X	X	X	X	X	X	X
RAM 2.1	1000	10FF		0	0	1	0	0			X	X	X	X	X	X	X	X
RAM 2.2	1400	14FF		0	0	1	0	1			X	X	X	X	X	X	X	X
RAM 2.3	1800	18FF		0	0	1	1	0			X	X	X	X	X	X	X	X
RAM 2.4	1C00	1CFF		0	0	1	1	1			X	X	X	X	X	X	X	X
ROM 1	2000	23FF		0	1		0	0	X	X	X	X	X	X	X	X	X	X
ROM 2	2400	27FF		0	1		0	1	X	X	X	X	X	X	X	X	X	X
ROM 3	2800	2BFF		0	1		1	0	X	X	X	X	X	X	X	X	X	X
ROM 4	2C00	2FFF		0	1		1	1	X	X	X	X	X	X	X	X	X	X
INTERFACE 1	4000	4003		1	0		0	0									X	X
INTERFACE 2	4400	4403		1	0		0	1									X	X
INTERFACE 3	4800	4803		1	0		1	0									X	X
INTERFACE 4	4C00	4C03		1	0		1	1									X	X