8253/8254 Timer and Counters

- The 8253/54 solves one of most common problem in any microcomputer system, the generation of accurate time delays under software control.
- Instead of setting up timing loops in system software, the programmer configures the 8253/54 to match this requirements, initializes one of the counters of the 8253/54 with the desired quantity, then upon command the 8253/54 will count out the delay and interrupt the CPU when it has completed its tasks.

- Some of the counter/timer functions common to microcomputers which can be implemented with the 8254 are:
  - Real time clock
  - Event-counter
  - Digital one-shot
  - Programmable rate generator
  - Square wave generator

- Difference between 8253 and 8254
- The following table differentiates the features of 8253 and 8254 –

8253	8254
Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
Read-Back command is not available	Read-Back command is available
Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.

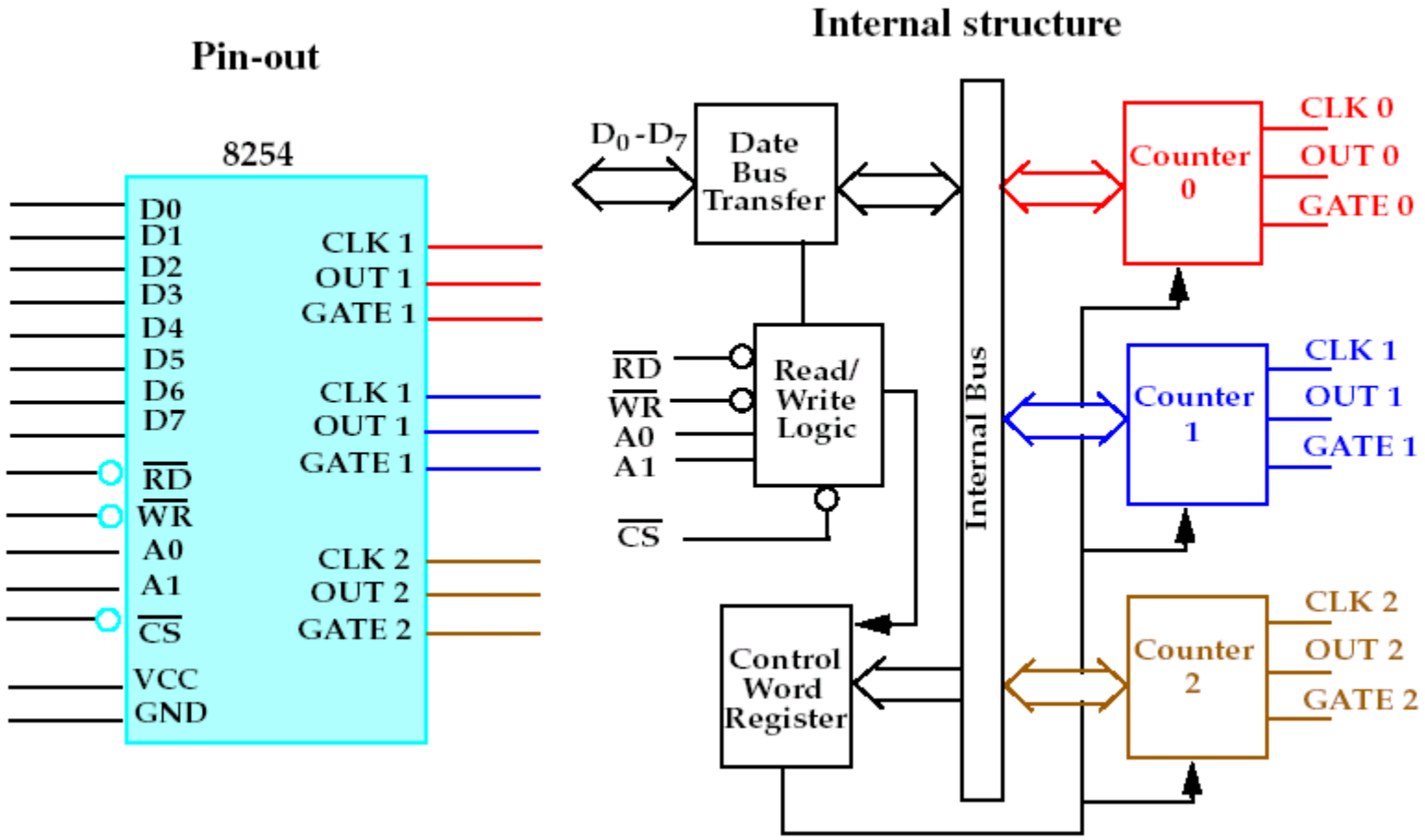
Features of 8253 / 54

- The most prominent features of 8253/54 are as follows −
  - It has three independent 16-bit down counters.
  - It can handle inputs from DC to 10 MHz.
  - These three counters can be programmed for either binary or BCD count.
  - It is compatible with almost all microprocessors.
  - 8254 has a powerful command called READ BACK command, which allows the user to check the count value, the programmed mode, the current mode, and the current status of the counter.

8253 / 8254 Timer

- PIT (programmable Interval Timer), used to bring down the frequency to the desired level
- Three counters inside 8253/8254. Each works independently and is programmed separately to divide the input frequency by a number from 1 to 65536

Block Diagram of 8254



- Inside the 8253/54 timer, there are 3 counters.
- Each timer works independently and programmed separately.
- Each counter is assigned an individual port address.
- The control register common to all 3 counters and has its own port.

A_1	A_0	Result
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

8253 / 8254 Timer

- Each of the three counter has 3 pins associated
  - CLK: input clock frequency
    - A square wave of 33% duty cycle
    - 8253: 0 ~ 2 MHz, 8254: 0 ~ 10 MHz
  - OUT: can be square wave, or one shot
  - GATE: Enable (high) or disable (low) the counter
- Data Pins: (D0 ~ D7)
  - Allow the CPU to access various registers inside the 8253/54 for both read and write operations. RD and WR are connected to IOR and IOW of control bus.

Control word

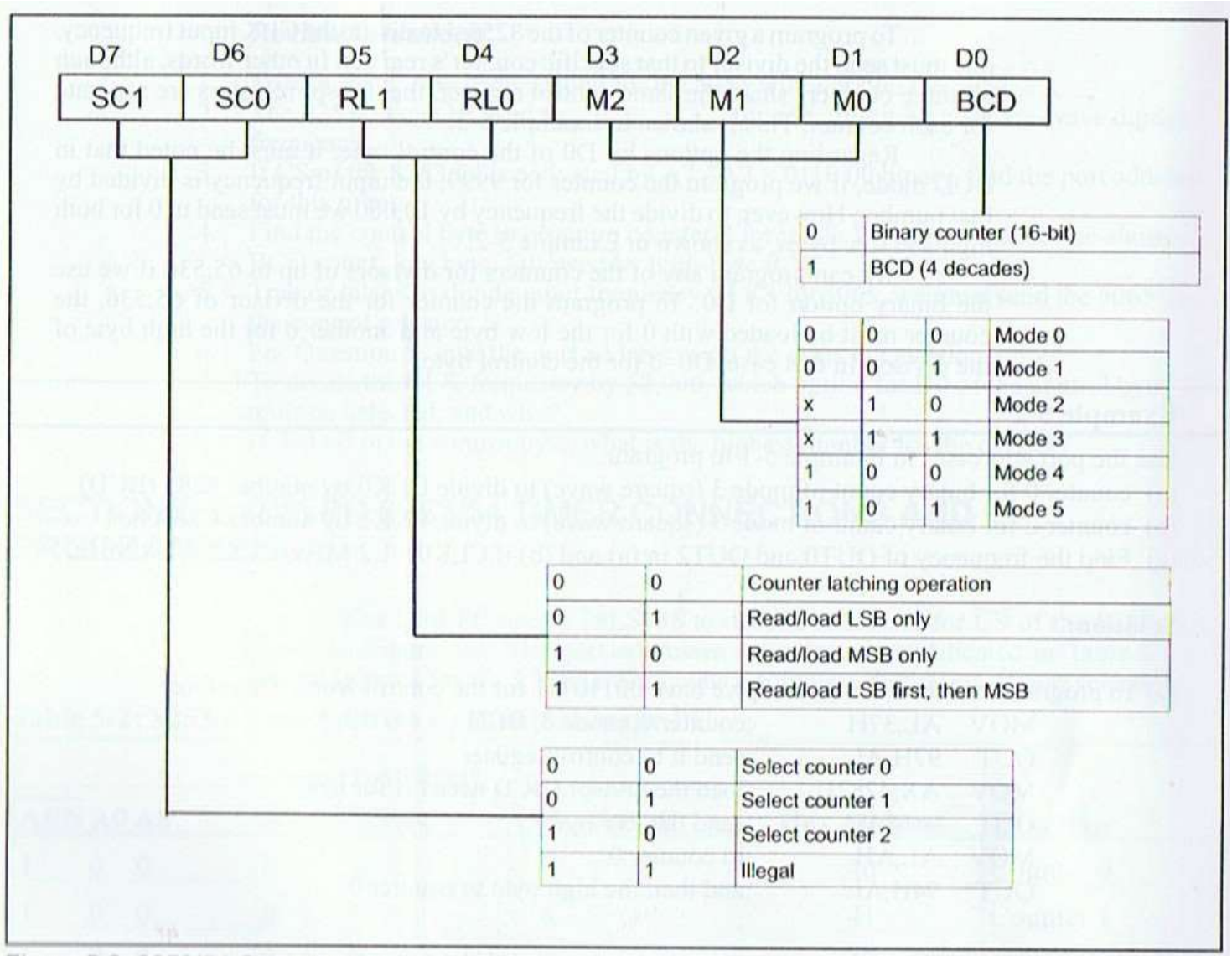


Figure 5-2. 8253/54 Control Word Format

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8253 / 8254 Timer

- Control byte must be first written into the control register. The 8253/54 must be initialized before use
- The programmer can not only write the value of the divisor into the 8253/54, but read the content of the counter at any given time as well
- All counters are down counters.

8253 / 8254 Timer

- To program a given counter to divide the CLK input frequency, one must send the divisor to that specific counter's register.
- Although all three counters share the same control register, the divisor registers are separate for each counter

8253 / 8254 Timer

- Example: given the port addresses for 8253/54:
- Counter 0: 94H Counter 1: 95H
  Counter 2: 96H Control Reg: 97H
- Task1: program counter 0 for binary counter for mode 3 to divide CLK0 by number 4282 (BCD)

```
MOV AL, 0011 0111B
OUT 97H, AL
MOV AX, 4282H
OUT 94H, AL (Low Byte)
MOV AL, AH
OUT 94H, AL (High Byte)
```

- OUT0 = CLK0 / 4282

Shape of the 8253/54 Output

- Given CLK = 1.193 MHz, the clock period of input frequency is 838 ns
- If the number N loaded into the counter is even, both high and low pulse are the same length, which is N/2 * 838 ns
- If the number N loaded into the counter is odd, the high pulse is (N+1)/2 * 838 ns and the low pulse is (N–1)/2 * 838 ns
- ➔ If N is odd, the high portion of the output square wave is slightly wider than the low portion

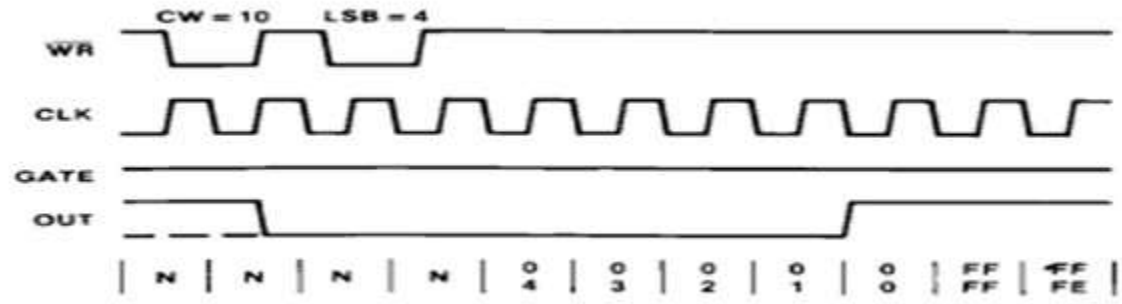
8253/54 Operation Modes

- Mode 0: Interrupt on terminal count
  - The output is initially low, and remain low for the duration of the count if GATE=1. When the terminal count is reached, the output will go high and remain high until a new control word or new count number is loaded
    - Width of low pulse = N * T, where T is clock period
  - Example: GATE=1 and CLK = 1 MHz

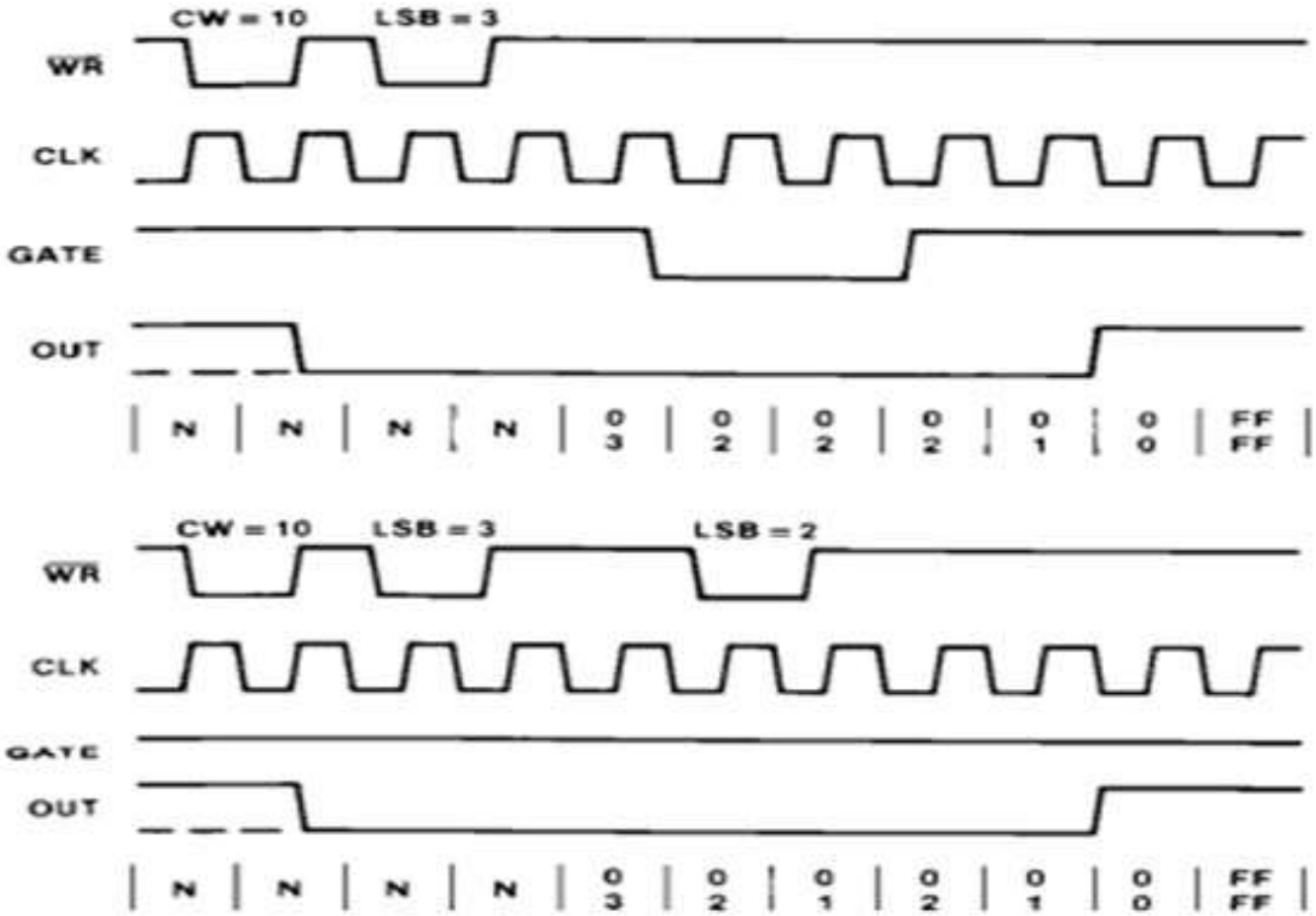
    Clock count N = 4

8253/54 Operation Modes

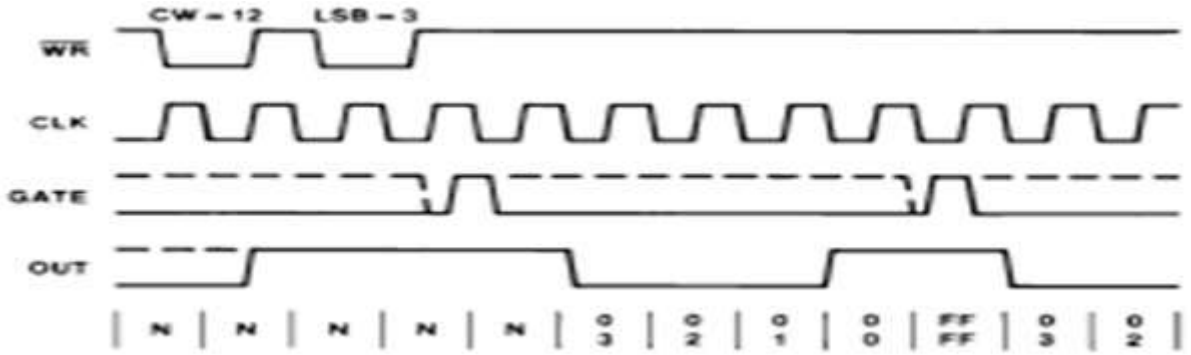
- Mode 0: Interrupt on terminal count
  - If GATE becomes low at the middle of the count, the count will stop and the output will be low. The count resumes when the GATE becomes high again ➔ This in effect adds to the total time the output is low.



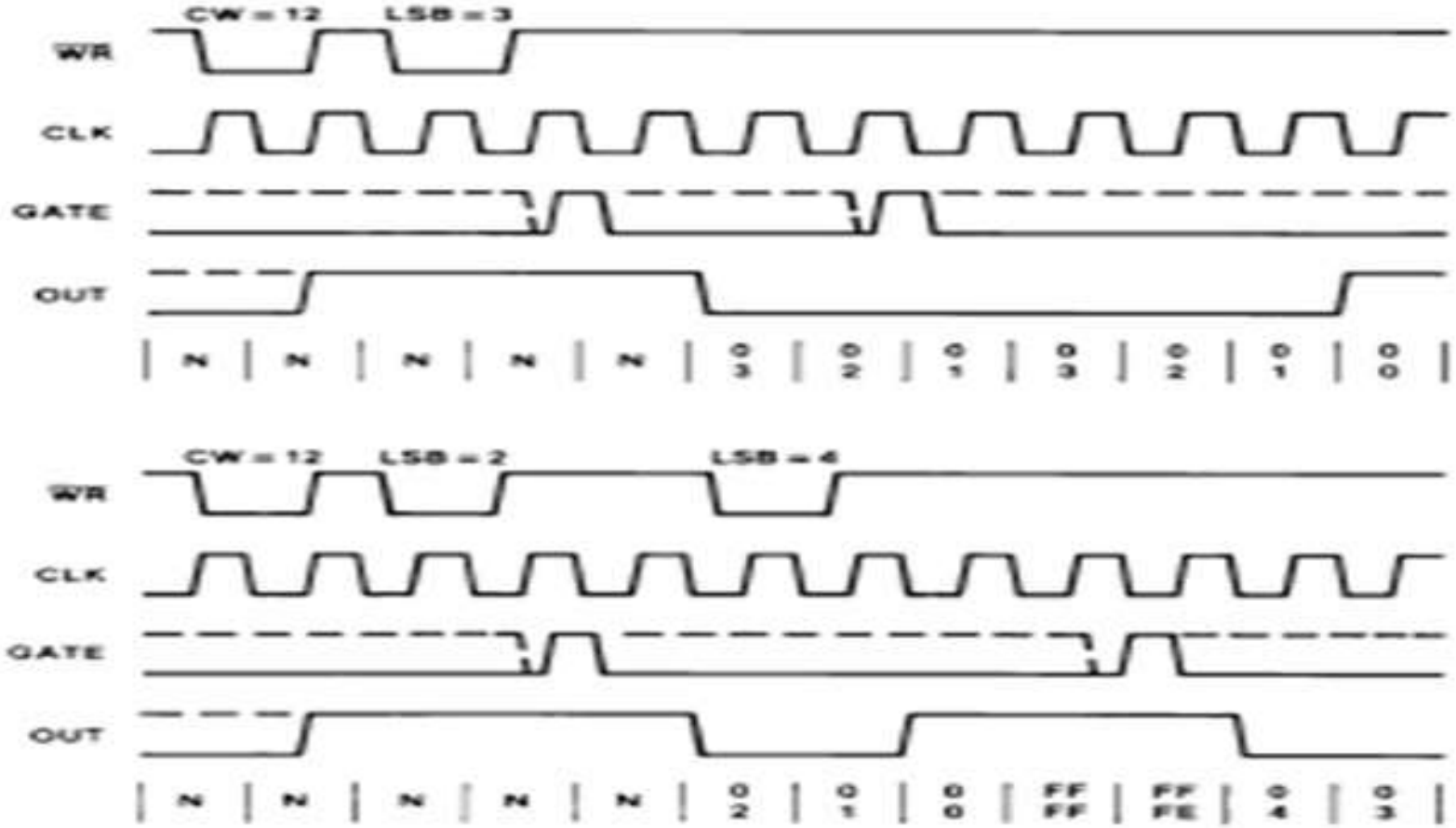
Mode 0: Interrupt on terminal count (contd)



- **Mode 1: HW triggered / programmable one shot**
  - The triggering must be done through the GATE input by sending a 0-to-1 pulse to it.
  - Steps: 1) Load the count register
    2) A 0-to-1 pulse must be sent to the GATE input to trigger the count
  - In Mode 1, after sending the 0-to-1 pulse to GATE, OUT becomes low and stays low for a duration of N*T, then becomes high and stays high until the GATE is triggered again
  - If during the activation, a retriggered happened, then restart the down counting

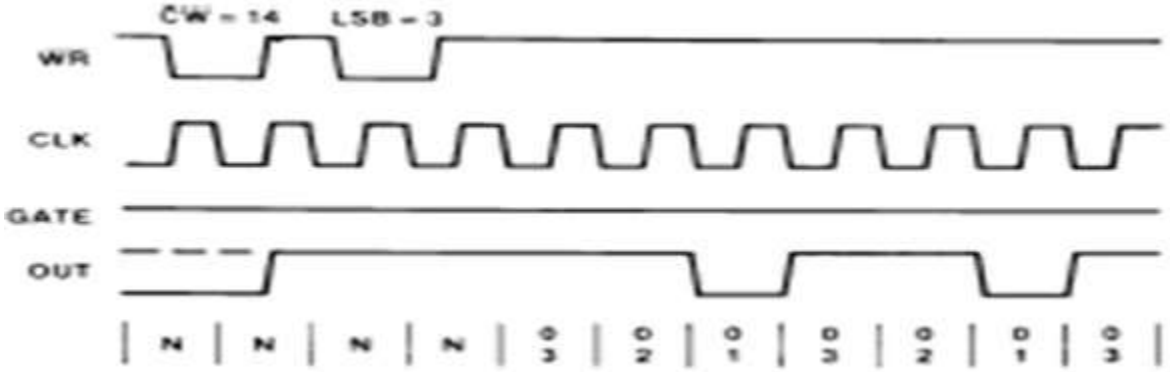


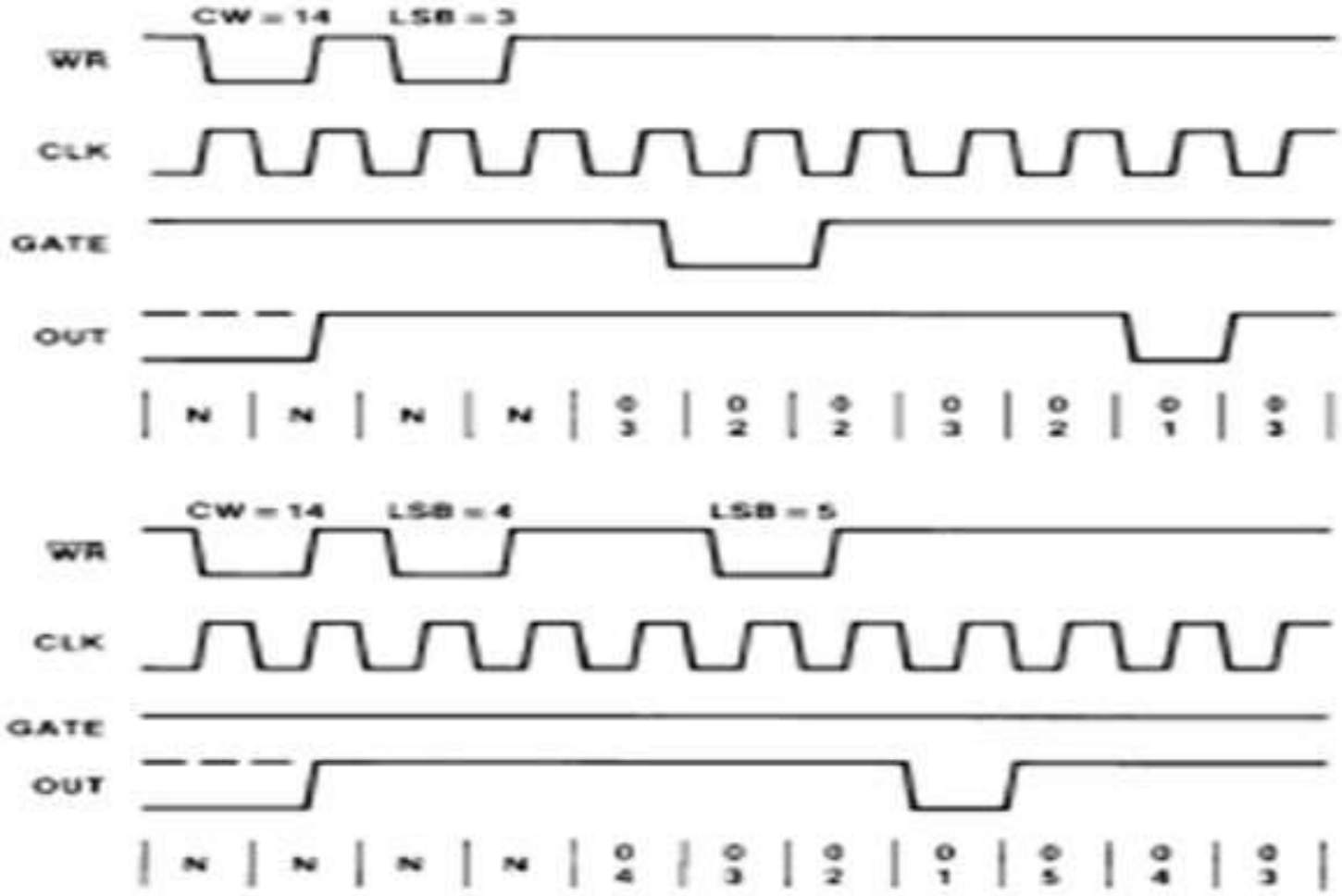
Mode 1


CW = 12
LSB = 3
WR
CLK
GATE
OUT
N
N
N
N
N
03
02
01
03
02
01
00
CW = 12
LSB = 2
LSB = 4
WR
CLK
GATE
OUT
N
N
N
N
N
02
01
00
FF FF
FF FE
04
03

8253/54 Operation Modes

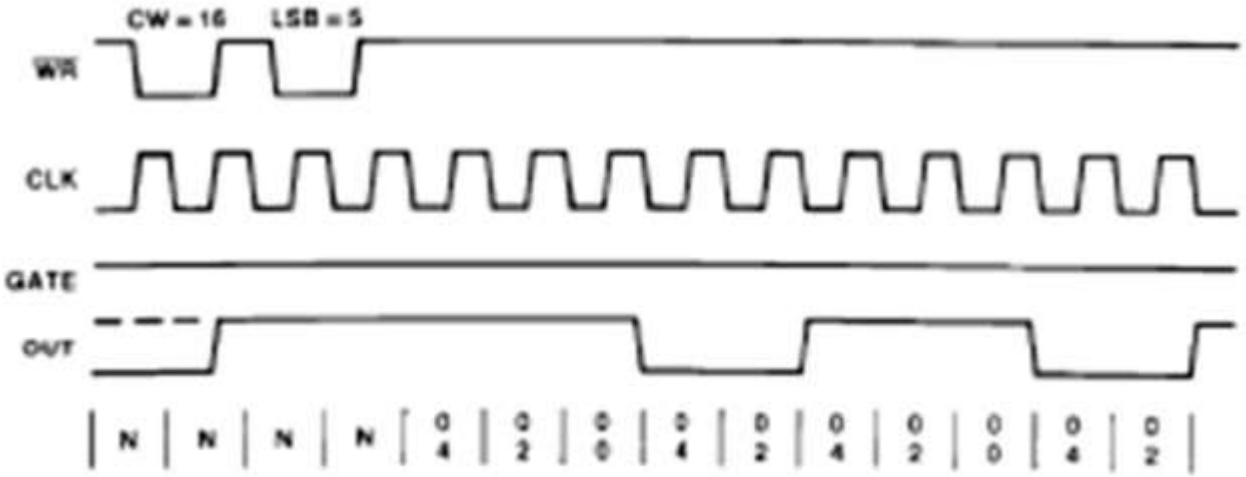
- Mode 2: Rate Generator (Divide-by-N counter)
  - In Mode2, if GATE=1, OUT will be high for (N-1)*T, goes low only for one clock pulse, then counter is reloaded automatically, and the process continues indefinitely. ➔ Whole period: N * T



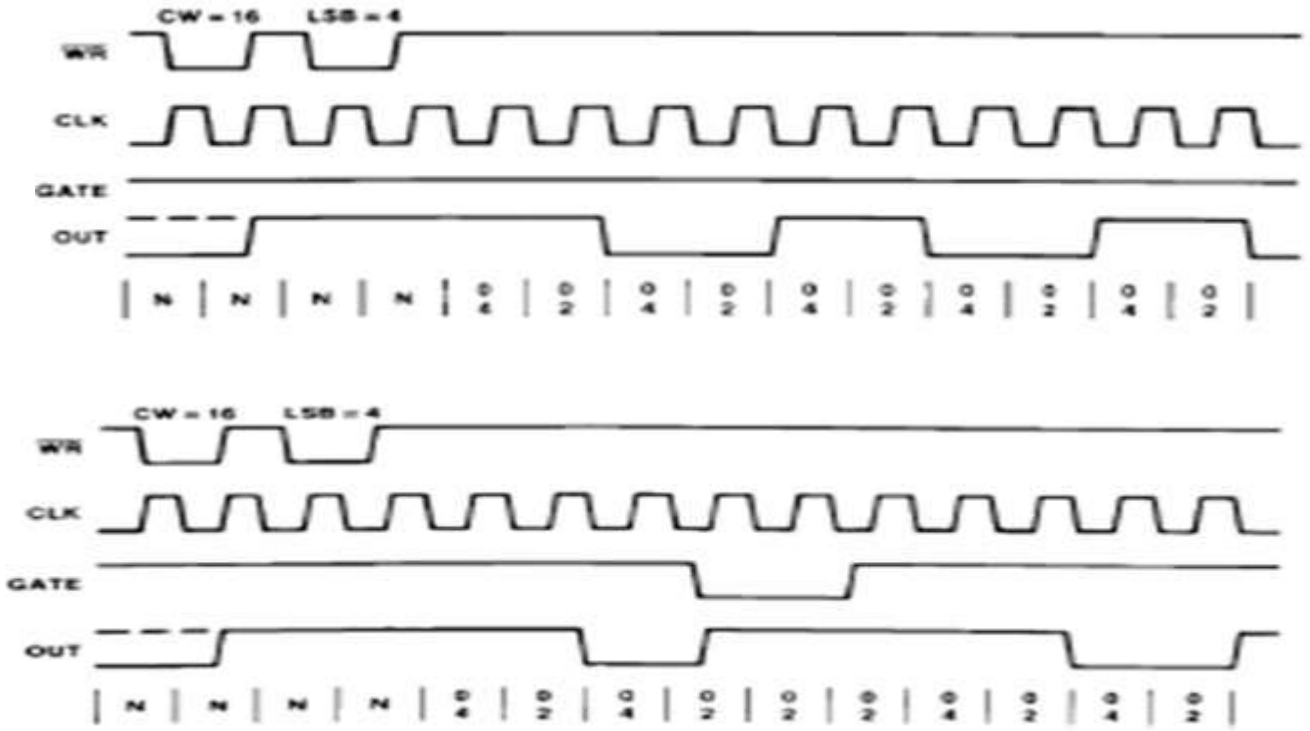

CW = 14
LSB = 3
WR
CLK
GATE
OUT
N N N N 03 02 02 03 02 01 03
CW = 14
LSB = 4
LSB = 5
WR
CLK
GATE
OUT
N N N N 04 03 02 01 05 04 03

8253/54 Operation Modes

- **Mode 3: Square wave rate generator**
  - Most commonly used

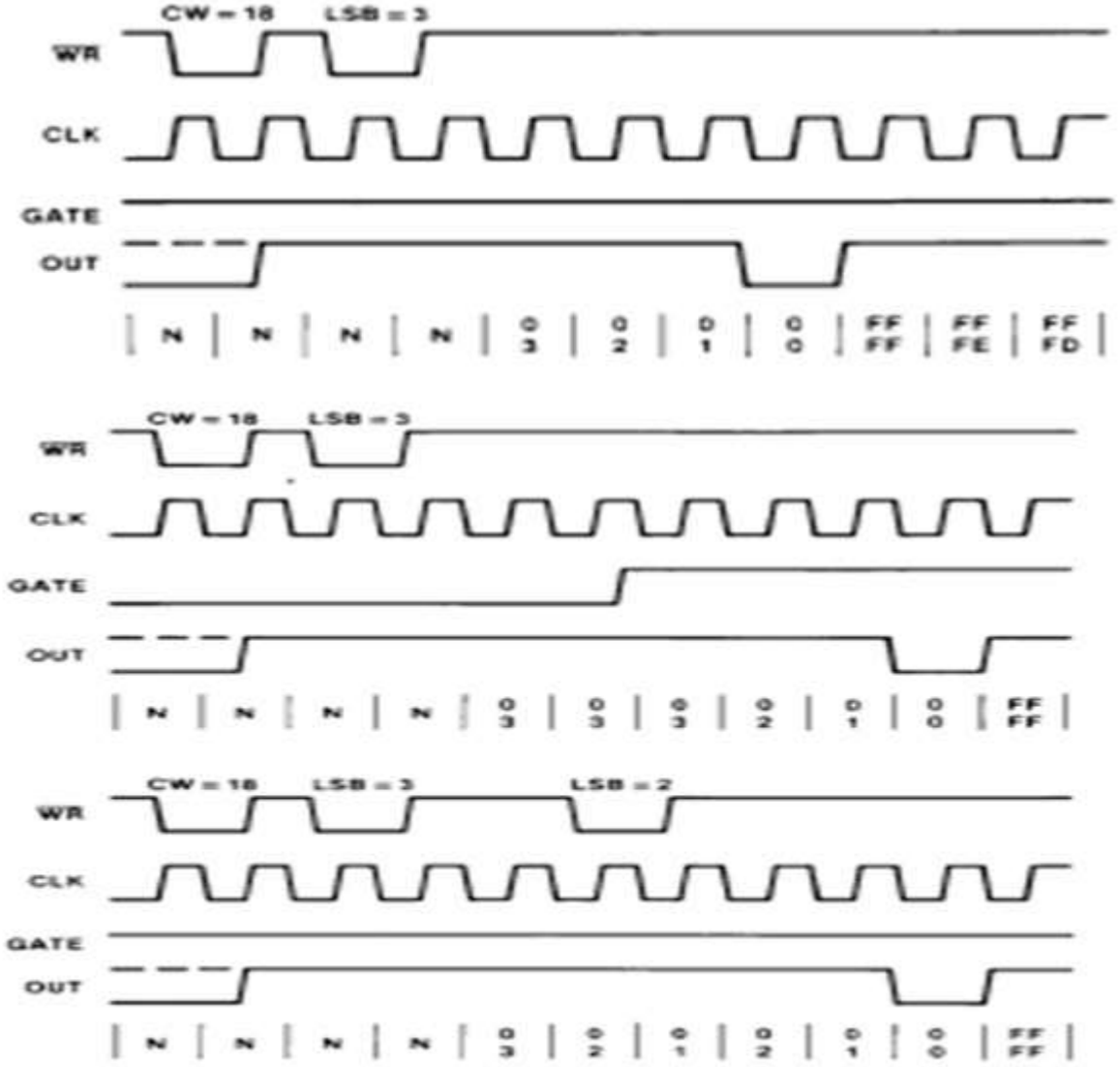


Mode 3


CW = 16
LSB = 4
WR
CLK
GATE
OUT
N
N
N
N
0 4
0 2
0 4
0 2
0 4
0 2
0 4
0 2
0 4
0 2
CW = 16
LSB = 4
WR
CLK
GATE
OUT
N
N
N
N
0 4
0 2
0 4
0 2
0 2
0 2
0 4
0 2
0 4
0 2

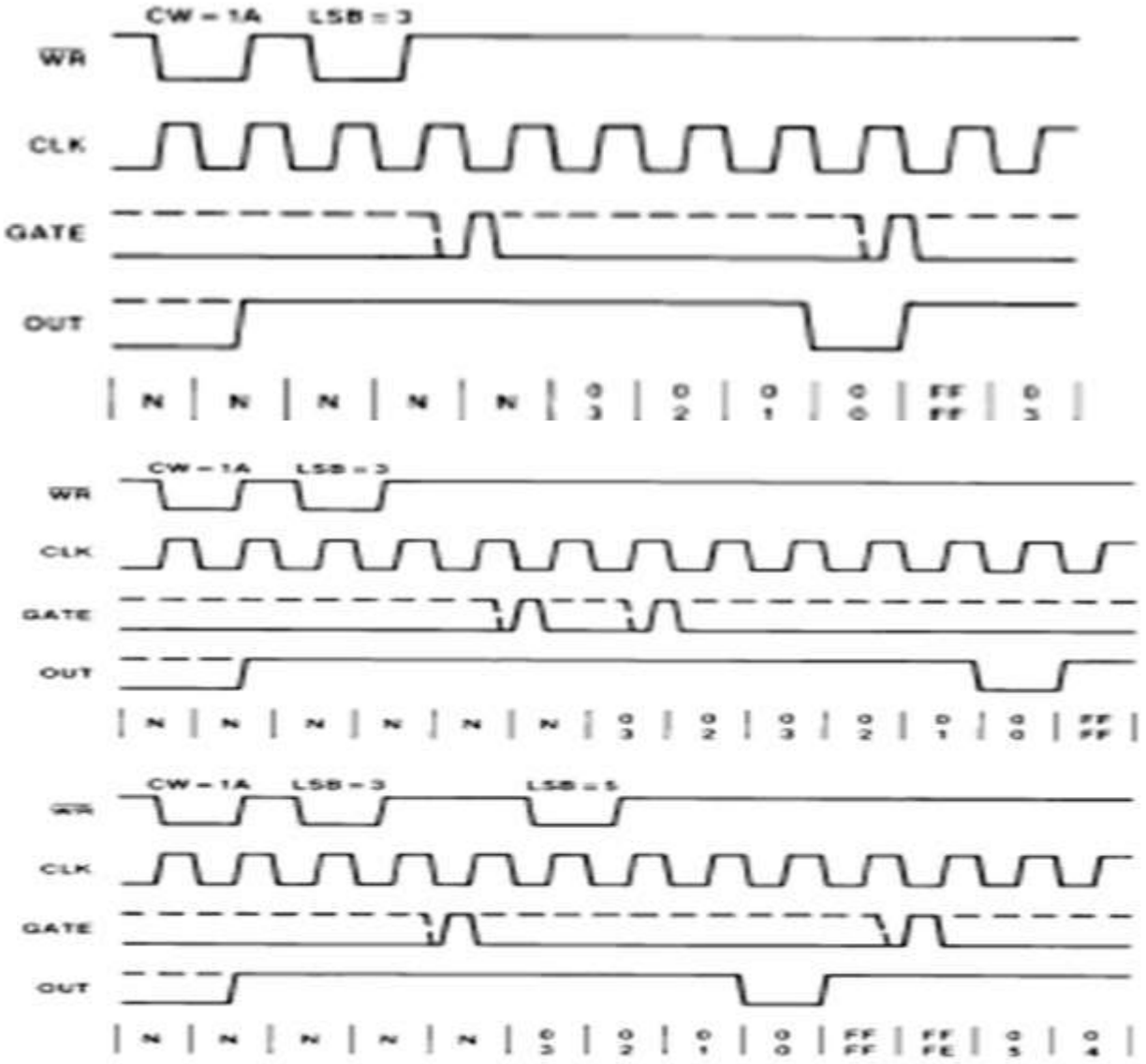
Mode 4: Software triggered strobe

- Similar to Mode2, except that the counter is not reloaded automatically
- In Mode4, if GATE=1, the output will go high when loading the count, it will stay high for duration N*T. After the count reaches zero, it becomes low for one clock pulse, then goes high again and stays high until a new command word or new count is loaded
- To repeat the strobe, the count must be reloaded


CW = 16
LSB = 3
WR
CLK
GATE
OUT
N
N
N
N
03
02
01
00
FF
FF
FF
FE
FF
FD
CW = 16
LSB = 3
WR
CLK
GATE
OUT
N
N
N
N
03
03
03
02
01
00
FF
FF
CW = 16
LSB = 3
LSB = 2
WR
CLK
GATE
OUT
N
N
N
N
03
02
01
02
01
00
FF
FF

8253/54 Operation Modes

- Mode 5: Hardware triggered strobe
  - Similar to Mode4, except that the triggering must be done with the GATE input
  - The count starts only when a 0-to-1 pulse is sent to the GATE input
  - If GATE retriggered during the counting, it will restart the down counting


CW = 1A
LSB = 3
WR
CLK
GATE
OUT
N
N
N
N
N
03
02
01
00
FF FF
03
CW = 1A
LSB = 3
WR
CLK
GATE
OUT
N
N
N
N
N
N
03
02
03
02
01
00
FF FF
CW = 1A
LSB = 3
LSB = 5
WR
CLK
GATE
OUT
N
N
N
N
N
05
02
01
00
FF FF
FF FE
03
04

Modes of Operation

- six modes (0–5) of available to each of the 8254 counters
- each mode functions with the CLK input, the gate (G) control signal, and OUT signal

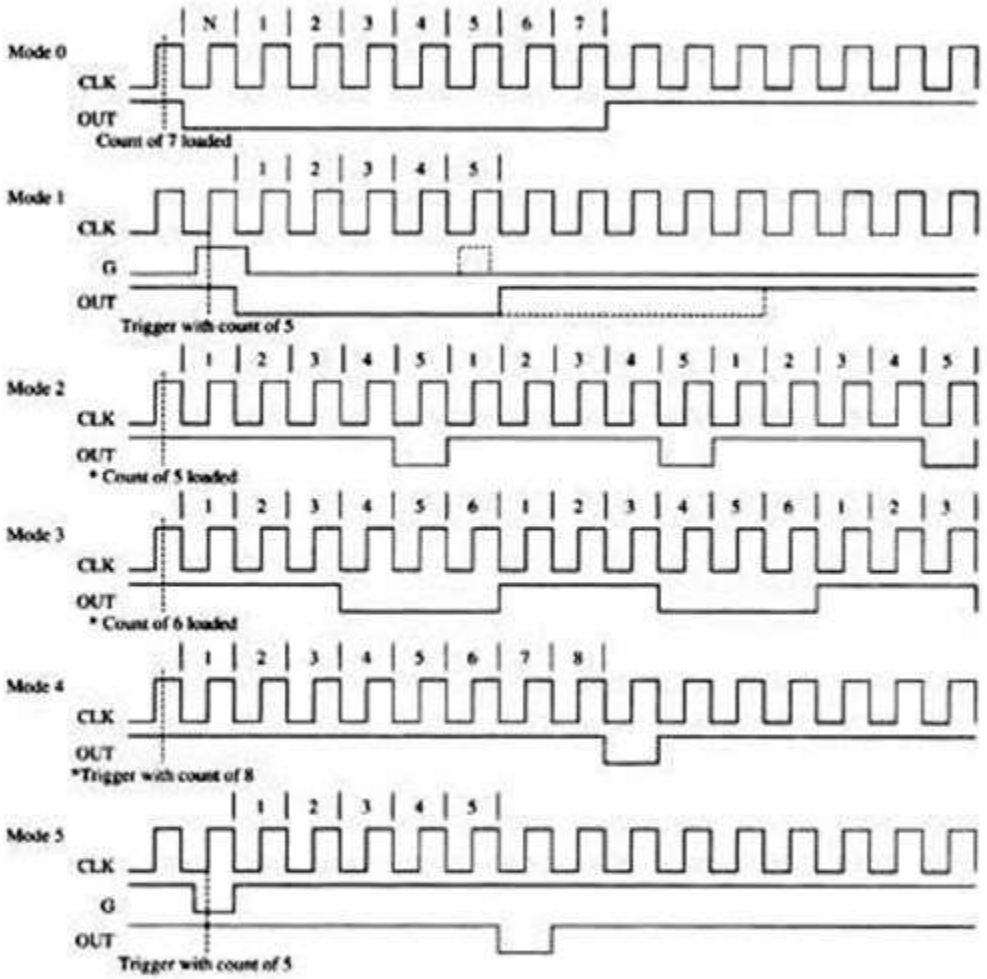


Figure 11–35 The six modes of operation for the 8254-2 programmable interval timer. The G input stops the count when 0 in modes 2, 3, and 4.

Gate pin operation summary

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	— —	Enables Counting
1	— —	1) Initiates Counting 2) Resets Output after Next Clock	— —
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	— —	Enables Counting
5	— —	Initiates Counting	— —

Min and Max Count of counters in different modes

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

8254 Read Operations

- There are three possible methods for reading the counters:
  - A simple read operation
  - The Counter Latch Command, and
  - The Read-Back Command.

Simple Read Operation

- This operation read the counter after stopping.
- To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.
- Two I/O read operation are performed by the MPU
    1. The first I/O operation reads the low order byte.
    2. The second I/O operation reads high order byte.

Counter Latch Command

- This allows reading the contents of the Counters “on the fly'' without affecting counting in progress.
- The selected Counter's output latch (OL) latches the count at the time the *Counter Latch Command* is received.
- This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to “following'' the counting element (CE).

Counter Latch Command (Continued)

Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

Example:

```
; Latching counter0
MOV DX, C_REG
MOV  AL, 00000000B ; count latched for counter 0.
OUT DX, AL
;Reading counter0
MOV DX, CNTR0
IN AL, DX
```

A_1,A_0 = 11; CS = 0; RD = 1; WR = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1,SC0—specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4—00 designates Counter Latch Command

X—don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

- Another feature of the 8254 is that reads and writes of the same Counter may be interleaved;
- for example: if the Counter is programmed for two byte counts, the following sequence is valid.
  1) Read least significant byte.
  2) Write new least significant byte.
  3) Read most significant byte.
  4) Write new most significant byte.
- If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

- This command is used to read several counters at a time. It eliminates the need of writing separate counter-latch commands for different counters.
- It allows the user to check the count value, programmed Mode, and current states of the OUT pin and Null Count flag of the selected counter/ counters.
- The read back command is written to the Control Word Register.
- The command is written into the Control Word Register and has the format shown in Figure.
- The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 =0 and selecting the desired counter(s).
- A single **read back command** is functionally equivalent to several **counter latch commands.**
- Each counter's latched count is held in the OL until it is read (or the counter is reprogrammed). The counter is automatically unlatched when read, but other counters remain latched until they are read.

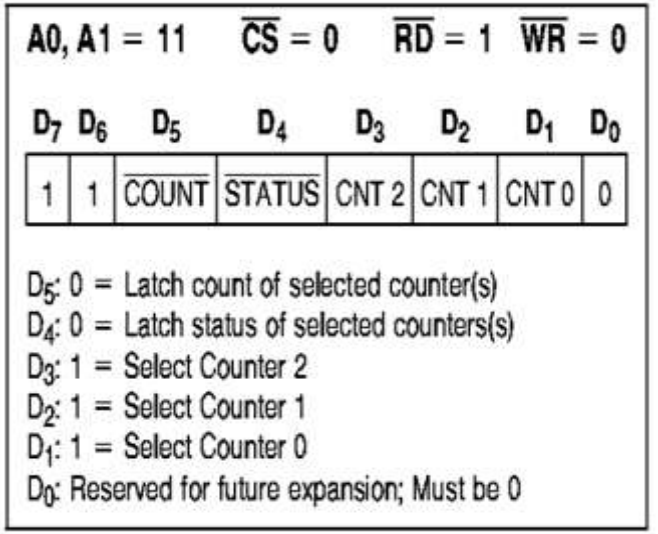
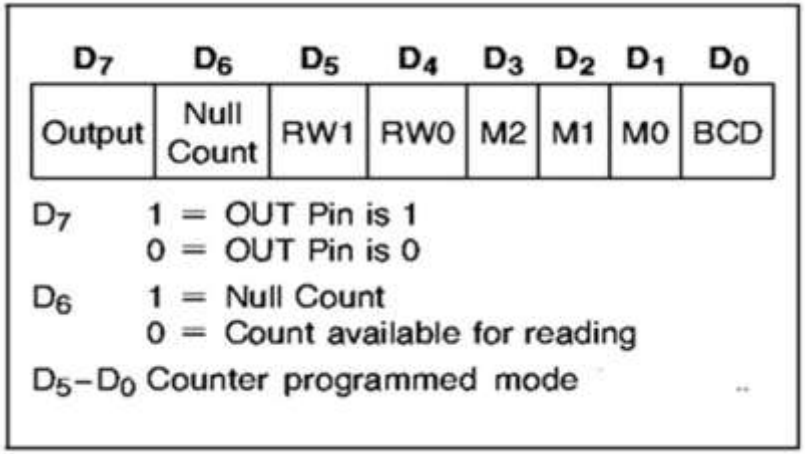


Figure Read-Back Command Format

Read-Back Command (Continued)

- The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.
- Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word.

- OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.
- The counter status format is shown in Figure below.



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null Count	RW1	RW0	M2	M1	M0	BCD

D_7 1 = OUT Pin is 1
0 = OUT Pin is 0

D_6 1 = Null Count
0 = Count available for reading

D_5–D_0 Counter programmed mode

- If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first.
- The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

- NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE).
- The exact time this happens depends on the Mode of the counter. Until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written.

Action	Causes
Write to the control word register;	Null Count=1
Write to the count register (CR);	Null Count=1
New Count is loaded into CE (CR-> CE)	Null Count =0

Command								Description	Result
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

Read-Back Command (Continued)

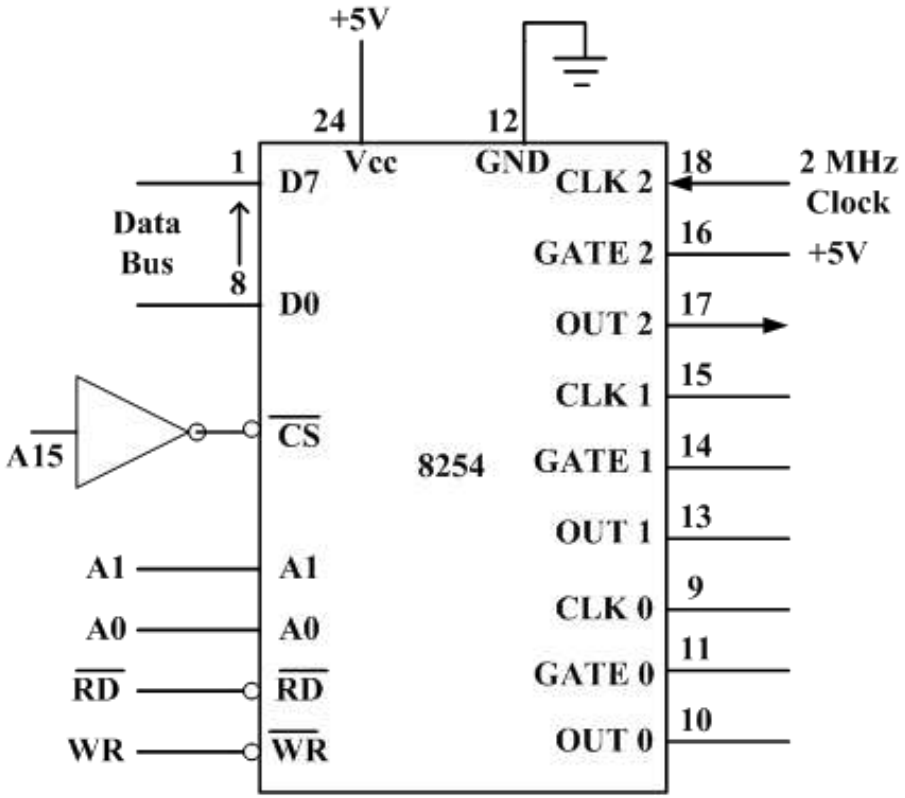
```
; Count and Status latched for count 0

MOV DX, C_REG
MOV AL, 11000010B ; count latched for count 0
OUT DX, AL

; Reading the latched status for count 0

MOV DX, CTRM0
IN AL, DX  ; Reading Status
MOV AH, AL

; Reading the latched count for counter 0

IN AL, DX      ; Reading LSB of counter 0
MOV BL, AL
IN AL, DX      ; Reading MSB of counter 0
MOV BH, AL
```

Problem 1

(a) Identify the port address of the control register and counter 2 in figure.

(b) Write a subroutine to initialize counter 2 in mode 0 with a count of 50,000. The subroutine should also include reading counts on the fly; when count reaches zero, it should return to the main program.

(c) Write a main program to display seconds by calling the subroutine as many times as necessary.


+5V
24
Vcc
12
GND
1
D7
Data
Bus
8
D0
A15
CS
8254
A1
A1
A0
A0
RD
RD
WR
WR
CLK 2
18
2 MHz
Clock
GATE 2
16
+5V
OUT 2
17
CLK 1
15
GATE 1
14
OUT 1
13
CLK 0
9
GATE 0
11
OUT 0
10

Solution (a):

A15	A14	A13	A12	A11……A5	A4	A3	A2	A1	A0	Address	
1	0	0	0	……	0	0	0	0	0	8000H	Counter 0
1	0	0	0	…….	0	0	0	0	1	8001H	Counter 1
1	0	0	0	…….	0	0	0	1	0	8002H	Counter 2
1	0	0	0	…….	0	0	0	1	1	8003H	Control Register

Address of counter 2 = 8002H

Address of control register = 8003H

Solution (b):

We have to initialize counter 2 in Mode0.

Count=$(50,000)_{10}$ = C350H

Control Word to initialize counter 2 in mode0 and to load 16-bit count:

1	0	1	1	0	0	0	0
Counter 2		Load 16 bit count		Mode 0			Count in binary

- To read count 2 on the fly counter latch command is:

1	0	0	0	0	0	0	0
Counter 2		Counter latch command		Don’t care			

Problem 1 (Continued)

```
COUNTER  PROC  NEAR
        CNT2   EQU   8002H
        CNTR  EQU   8003H
        MOV  AL, B0H
        MOV DX,CNTR
        OUT   DX, AL
        MOV DX,CNT2
        MOV   AL, 50H
        OUT  DX, AL
         MOV AL, C3H
        OUT  DX, AL
READ: MOV AL, 80H
         MOV DX,CNTR
        OUT  DX, AL
                        MOV DX,CNT2
                        IN AL, DX
                        MOV  DL, AL
                        IN AL, DX
                        OR  AL, DL
                        JNZ READ
                RET
                 COUNTER  ENDP
```

Problem 1 (Continued) Solution (c)

Clock frequency, fc = 2 MHz

Time period of each clock cycle, $Tc = \frac{1}{2 \times 10^6} = = 5 \times 10^{-7}$ sec

Every time subroutine is called then, $50000 \times 5 \times 10^{-7} = 25\ m\text{sec}$ is counted.

To count 1 sec subroutine needed to be called, $\frac{1s}{25ms} = 40 = 28\ time$

Main Program:

Assuming segment registers are already initialized.

```
        MOV  BL, 00H
SECOND:  MOV CL, 28H
WAIT:    CALL  COUNTER
         DEC  CL
         JNZ  WAIT
         MOV  AL, BL
         ADD   AL, 01
         DAA
         OUT  25H, AL ; assuming 8 bit port 25H
         MOV  BL, AL
         JMP SECOND
         HLT
```

Problem 2

- Write instructions to generate a pulse in every 50 us later from counter 0.Consider the figure of problem1.
- **Solution-**To generate a pulse in every 50 us later, we should initialize counter0 in mode 2. Gate0 should be high.
- **Count:** Clock frequency, fc = 2 MHz

  Needed count, $N = \frac{\text{pulse time}}{\text{Clock period}} = 100 = 64h$

- **Control Word**

0	0	0	1	0	1	0	0
Counter 0		Load least significant byte only		Mode 2			Count in binary

```
CNT0 EQU 8000H
CNTR EQU  8003H
MOV   AL, 14H
MOV DX,CNTR

OUT  DX, AL

 MOV  AL, 64H
MOV DX,CNT0
OUT  DX, AL
```

Problem 3

- Write instructions to generate a 1 KHz square wave from Counter1. Assume the gate of counter1 is tied to +5V through a 10K resistor. Explain the significance of connecting the gate to +5V. (use figure of problem 1)(Clock=2MHz)

Soln: To generate a square wave from counter1, it should be initialize in Mode 3.

Needed count = 2000 (i.e 2MHz / 1KHz)= 07D0H

Control Word=76H

```
CNT1 EQU 8001H
CNTR EQU 8003H
MOV   AL, 76H
OUT  CNTR, AL
MOV  AL, D0H
OUT  CNT1, AL
MOV  AL, 07H
OUT   CNT1, AL
```

Problem 4

- Write a subroutine to generate an interrupt every 1sec. Consider the figure of problem1.
- **Solution:** To obtain a pulse every 1 sec, the count should be 2×10^6, which is too large for one 16-bit counter. We can divide this counter as follows:

Counter 1 [Clk=2 MHz]- Mode 2 – Count 50,000(C350H)

Counter 2 [Clk=out1 (output of counter 1)]- Mode 2-Count 40 (28H)

So, finally we get $50{,}000 \times 40 = 2 \times 10^6$ count and from OUT2 we get the desired output.

Control word:

Counter 1= 01 11 010 0 = 74H

Counter 2= 10 01 010 0=94H

```
CNT1 EQU 8001 H
CNT2 EQU 8002H
CNTR EQU 8003H
MOV AL, 74H
OUT CNTR, AL
 MOV AL, 94H
OUT CNTR, AL
MOV AL, 50H
 OUT CNT1, AL
MOV AL, C3H
 OUT CNT1, AL
 MOV AL, 28H
 OUT CNT2, AL
```

Problem 5

- Write the instruction to generate a 100 KHz square-wave at OUT0 and a 200 KHz continuous pulse at OUT1 of 8254. Consider a clock of 8 MHz at clk0 and clk1. Again address pins A0 and A1 of 8254 are directly connected to A0 and A1 of 8086 and A15 of 8086 is connected to CS' of 8254 through an inverter.
- **Solution:**

  To generate 100 KHz square wave at OUT0,

  No. of count: x×100 KHz=8MHz; ≫x=80=50H

  Control Word=16H

  To generate 200 KHz continuous pulse at OUT1,

  No. of count, $x \times 200\ \mathrm{KH}z = 8\mathrm{MH}z$; $\gg x = 40 = 28\mathrm{H}$

  Control Word=54H

Address of Counter 0 = 8000H
Address of Counter 1= 8001H
Address of counter 2=8002H
Address of Control Register = 8003H

```
CNT0   EQU   8000 H
CNT1   EQU   8001H
CNTR  EQU   8003H
MOV AL, 16H
OUT CNTR, AL
MOV AL, 50H
OUT CNT0, AL
MOV  AL, 54H
OUT CNTR, AL
MOV AL, 28H
OUT CNT1, AL
```