CS311: Computer Architecture Lab
Assignment5

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1 Observations

Table 1: Observations(Assignment 5)

Program Name	**#DynamicInstructions**	**#Cycles**	**IPC**
Descending	365	15221	0.02398002759
Even odd	6	254	0.02362204724
Fibonacci	94	3861	0.02434602434
Palindrome	56	2335	0.02398286937
Prime	34	1405	0.02419928825

Table 2: Observations(Assignment 4)

Program Name	**#DynamicInstructions**	**#Cycles**	**IPC(Assign4)**
Descending	405	600	0.675
Even odd	10	16	0.625
Fibonacci	113	148	0.76351351351
Palindrome	73	117	0.62393162393
Prime	38	55	0.6909090909

2 Inferences

The delay in processing each event has a substantial impact on overall data throughput. Furthermore, when we examine the throughput of all benchmark programs, we notice that they are consistently close to 0.02. This value corresponds to the reciprocal of memory latency, which is notably higher than the latency of other events.

Our analysis reveals that the number of instructions a processor can execute per cycle (Instructions Per Cycle or IPC) for all benchmark programs falls within the range of 0.021-0.025. This observation aligns with our expectations, as each instruction fetch inherently introduces a 40-cycle delay. In simpler terms, this suggests that the processor is capable of executing instructions within this specified range during each clock cycle.

However, it's important to emphasize that IPC can exhibit significant improvements when programs involve a higher proportion of memory-related store and load operations. When a program predominantly consists of these memory-related instructions, the IPC tends to decrease, as these instructions often require more cycles for execution. In such cases, the IPC may fall below the 0.021-0.025 range, indicating less efficient instruction execution.instructions.