
STM32
CubeMX

1. Description

1.1. Project

Project Name	cv6
Board Name	NUCLEO-F030R8
Generated with:	STM32CubeMX 6.15.0
Date	10/29/2025

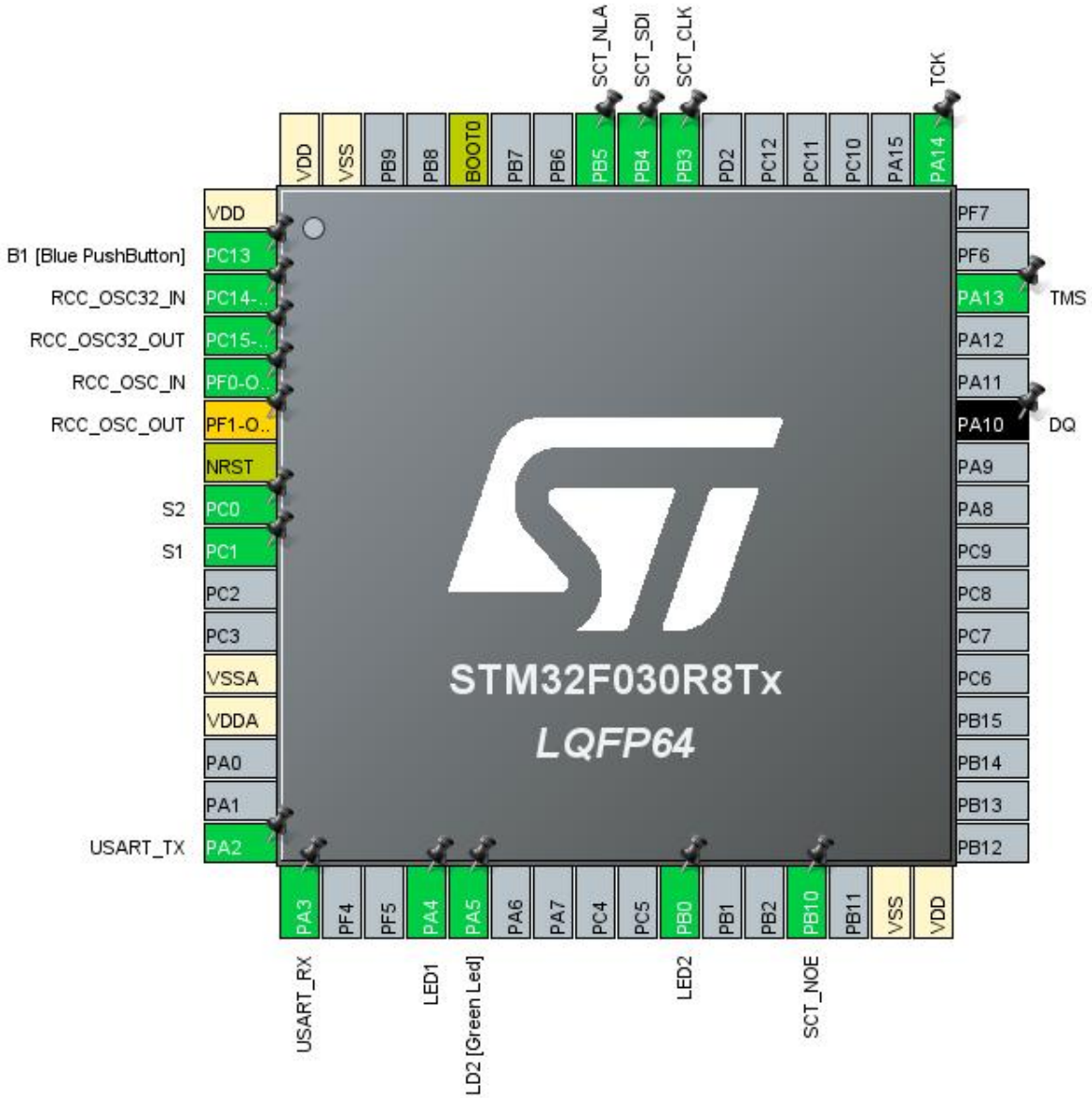
1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x0 Value Line
MCU name	STM32F030R8Tx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M0

2. Pinout Configuration



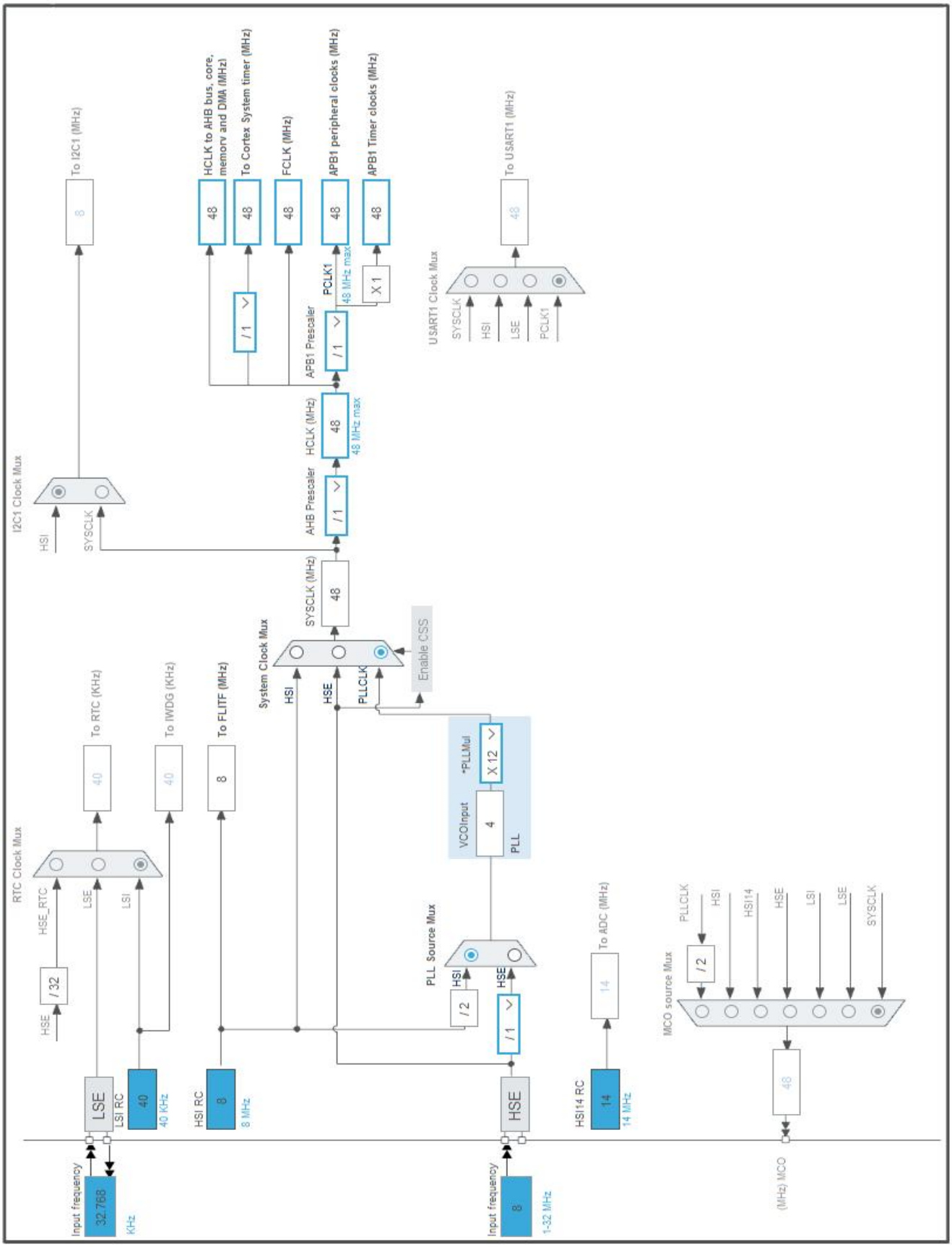
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 **	I/O	GPIO_Input	S2
9	PC1 **	I/O	GPIO_Input	S1
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
20	PA4 **	I/O	GPIO_Output	LED1
21	PA5 **	I/O	GPIO_Output	LD2 [Green Led]
26	PB0 **	I/O	GPIO_Output	LED2
29	PB10 **	I/O	GPIO_Output	SCT_NOE
31	VSS	Power		
32	VDD	Power		
43	PA10 **	I/O	GPIO_Output	DQ
46	PA13	I/O	SYS_SWDIO	TMS
49	PA14	I/O	SYS_SWCLK	TCK
55	PB3 **	I/O	GPIO_Output	SCT_CLK
56	PB4 **	I/O	GPIO_Output	SCT_SDI
57	PB5 **	I/O	GPIO_Output	SCT_NLA
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x0 Value Line
MCU	STM32F030R8Tx
Datasheet	DS9773_Rev2

1.2. Parameter Selection

Temperature	25
Vdd	3.6

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

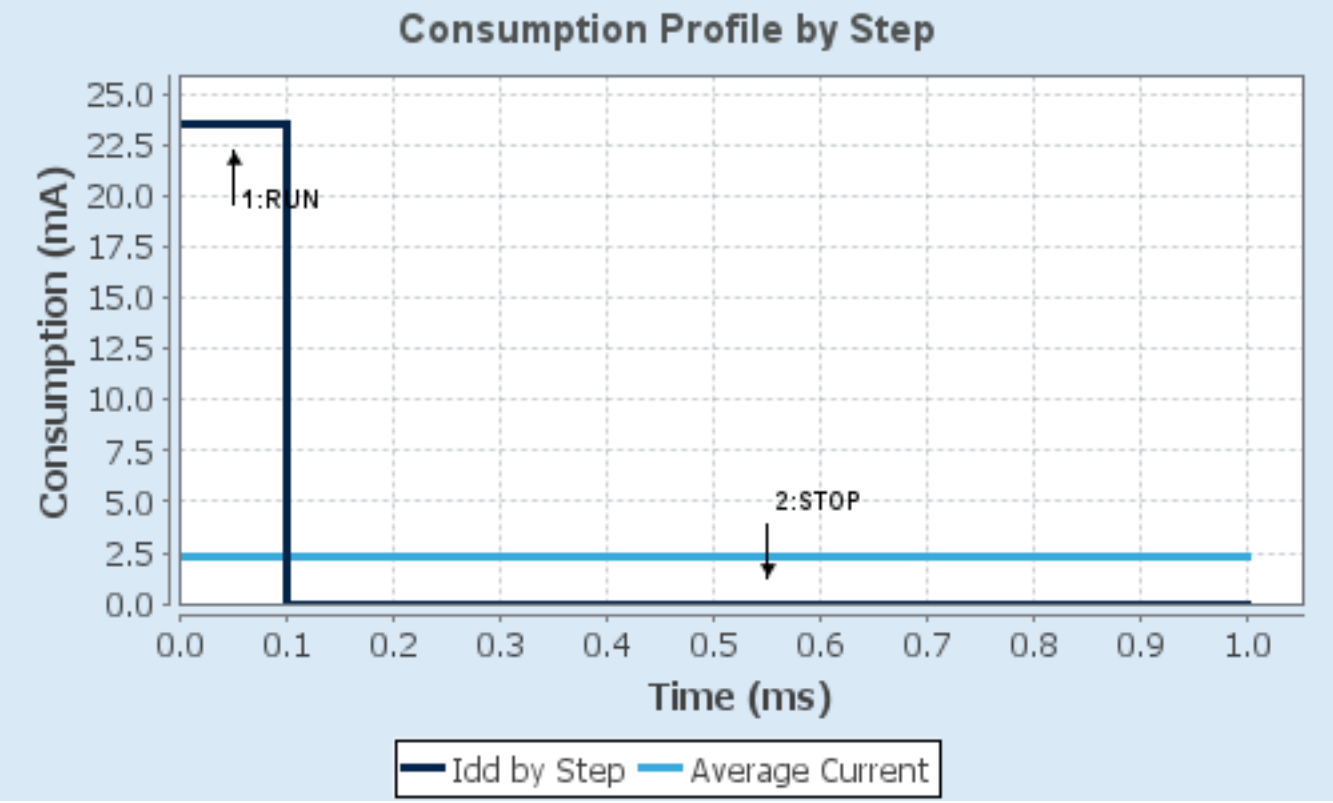
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	48 MHz	0 Hz
Clock Configuration	HSE PLL All IPs ON	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	23.46 mA	7.9 µA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Ta Max	101.28	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.35 mA
Battery Life	1 month, 29 days, 16 hours	Average DMIPS	0.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
25.0
22.5
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	cv6
Project Folder	C:\Temp\MPC-MKS\cv6\cv6
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F0 V1.11.5
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART2_UART_Init	USART2

3. Peripherals and Middlewares Configuration

3.1. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

3.2. SYS

mode: Debug Serial Wire

3.3. USART2

Mode: Asynchronous

3.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable

DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART_RX
Single Mapped Signals	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_Input	Input mode	**Pull-up ***	n/a	S2
	PC1	GPIO_Input	Input mode	**Pull-up ***	n/a	S1
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SCT_NOE
	PA10	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DQ
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SCT_CLK
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SCT_SDI
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SCT_NLA

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line 4 to 15 interrupts	unused		
USART2 global interrupt	unused		

4.3.2. NVIC Code generation

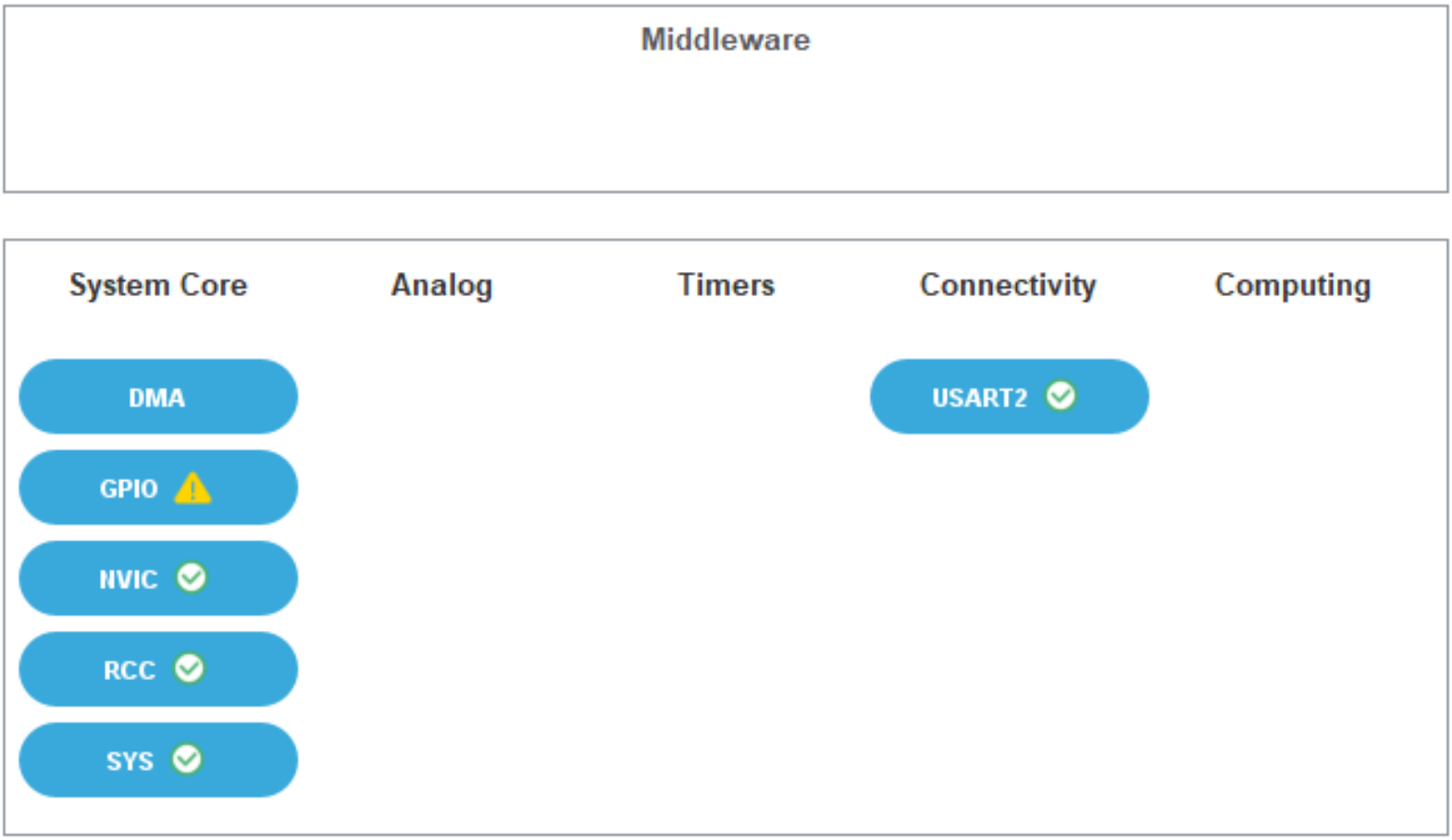
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type	Link