CS1050 – Lab4

Index: 210670N

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PART 1

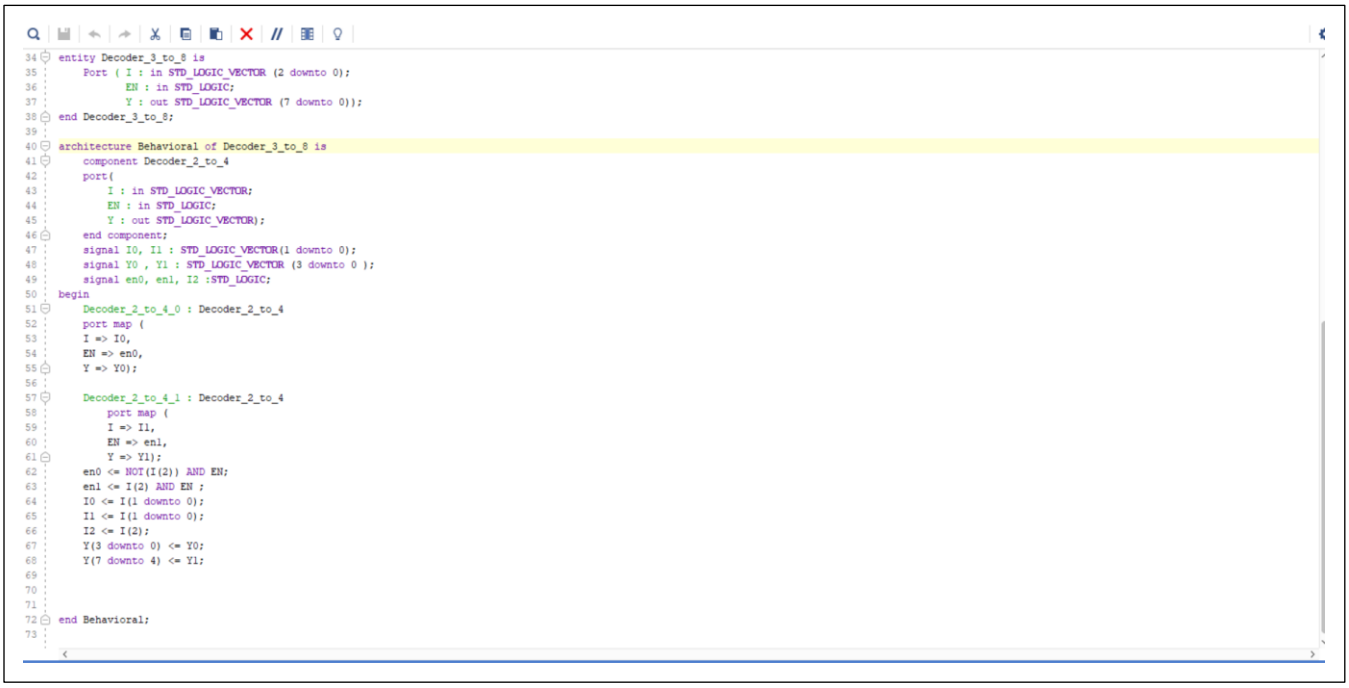
The assigned task of lab4 was to design the circuit for a 2_to_4 decoder simulates it using Xsim. The next task was to build the circuit for a 3 _ to_8 decoder using two 2_to_4 decoders .and simulate the circuit with several possible inputs. The final task was to implement the circuit for an 8-to-1 multiplexer, simulate it, create the constrains file and to test the circuit on a Basys 3 board.

PART 2- VHDL Files

2_to_4 Decoder

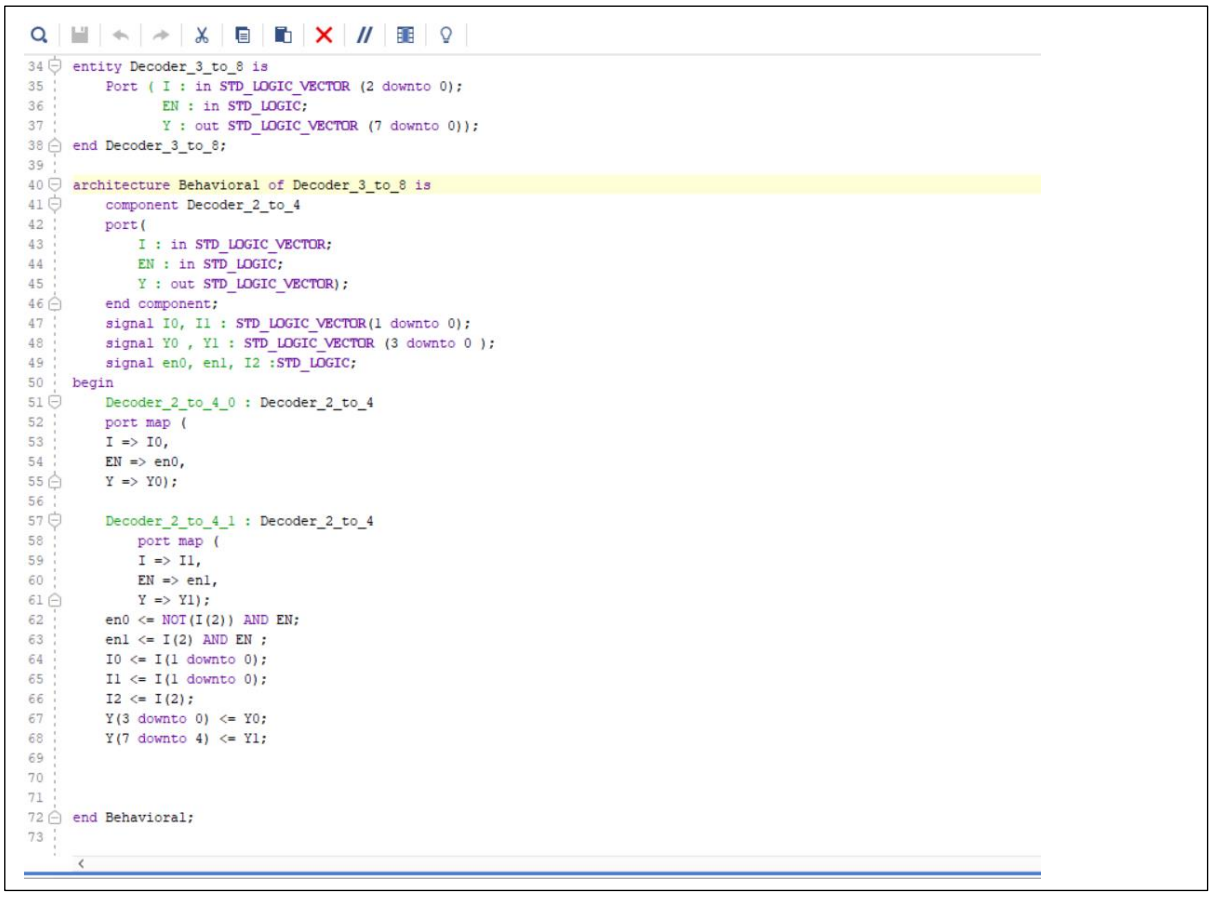
```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Decoder_2_to_4 is
35      Port ( I : in STD_LOGIC_VECTOR (1 downto 0);
36             EN : in STD_LOGIC;
37             Y : out STD_LOGIC_VECTOR (3 downto 0));
38  end Decoder_2_to_4;
39
40  architecture Behavioral of Decoder_2_to_4 is
41
42  begin
43  Y(0) <= NOT(I(0)) AND NOT(I(1)) AND EN;
44  Y(1) <= I(0) AND NOT(I(1)) AND EN ;
45  Y(2) <= NOT(I(0)) AND I(1) AND EN;
46  Y(3) <= I(0) AND I(1) AND EN;
47
48
49
50
51  end Behavioral;
52
```

3_to_8 Decoder



```
entity Decoder_3_to_8 is
    Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
           EN : in STD_LOGIC;
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end Decoder_3_to_8;

architecture Behavioral of Decoder_3_to_8 is
    component Decoder_2_to_4
    port(
        I : in STD_LOGIC_VECTOR;
        EN : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR);
    end component;
    signal I0, I1 : STD_LOGIC_VECTOR(1 downto 0);
    signal Y0 , Y1 : STD_LOGIC_VECTOR (3 downto 0 );
    signal en0, en1, I2 :STD_LOGIC;
begin
    Decoder_2_to_4_0 : Decoder_2_to_4
    port map (
    I => I0,
    EN => en0,
    Y => Y0);

    Decoder_2_to_4_1 : Decoder_2_to_4
        port map (
        I => I1,
        EN => en1,
        Y => Y1);
    en0 <= NOT(I(2)) AND EN;
    en1 <= I(2) AND EN ;
    I0 <= I(1 downto 0);
    I1 <= I(1 downto 0);
    I2 <= I(2);
    Y(3 downto 0) <= Y0;
    Y(7 downto 4) <= Y1;



end Behavioral;
```

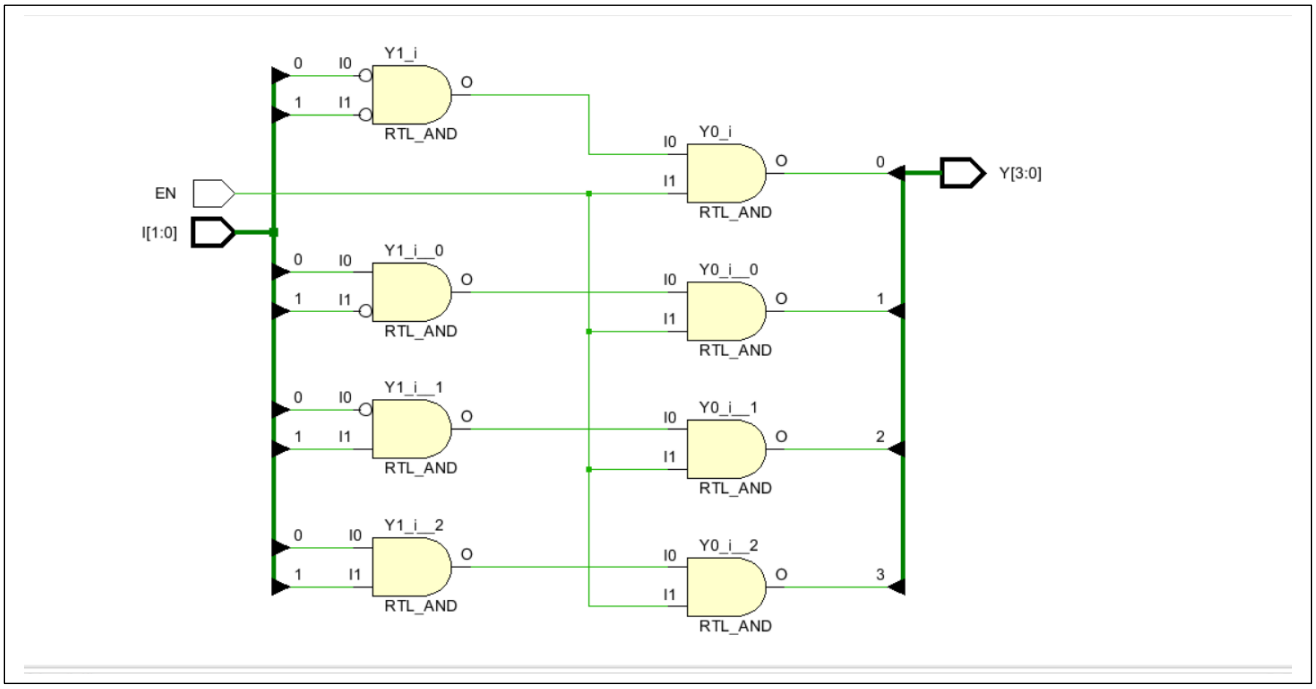
8_to_1 Multiplexer



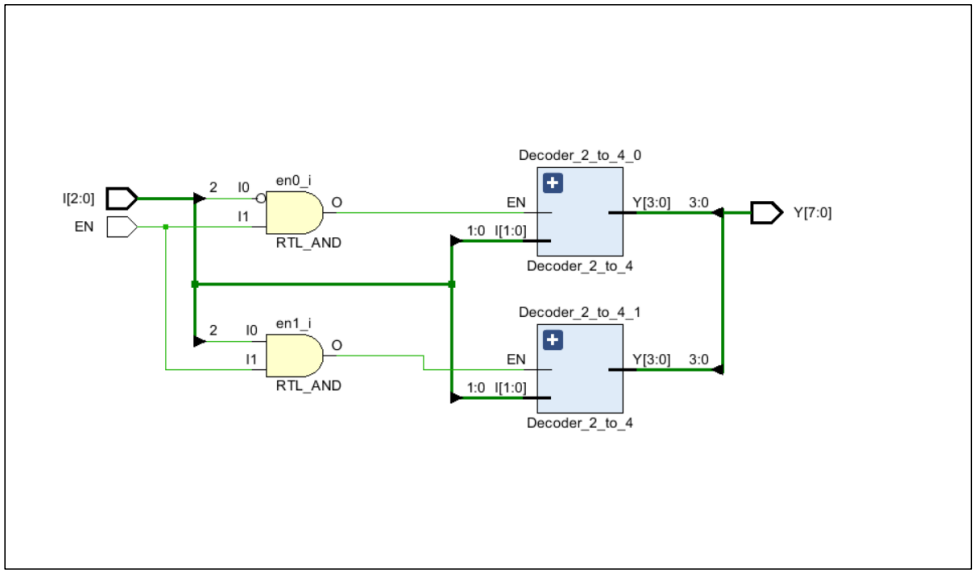
```
entity Decoder_3_to_8 is
    Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
           EN : in STD_LOGIC;
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end Decoder_3_to_8;

architecture Behavioral of Decoder_3_to_8 is
    component Decoder_2_to_4
    port(
        I : in STD_LOGIC_VECTOR;
        EN : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR);
    end component;
    signal I0, I1 : STD_LOGIC_VECTOR(1 downto 0);
    signal Y0 , Y1 : STD_LOGIC_VECTOR (3 downto 0 );
    signal en0, en1, I2 :STD_LOGIC;
begin
    Decoder_2_to_4_0 : Decoder_2_to_4
    port map (
    I => I0,
    EN => en0,
    Y => Y0);

    Decoder_2_to_4_1 : Decoder_2_to_4
        port map (
        I => I1,
        EN => en1,
        Y => Y1);
    en0 <= NOT(I(2)) AND EN;
    en1 <= I(2) AND EN ;
    I0 <= I(1 downto 0);
    I1 <= I(1 downto 0);
    I2 <= I(2);
    Y(3 downto 0) <= Y0;
    Y(7 downto 4) <= Y1;



end Behavioral;
```

PART 3- Schematic Diagram

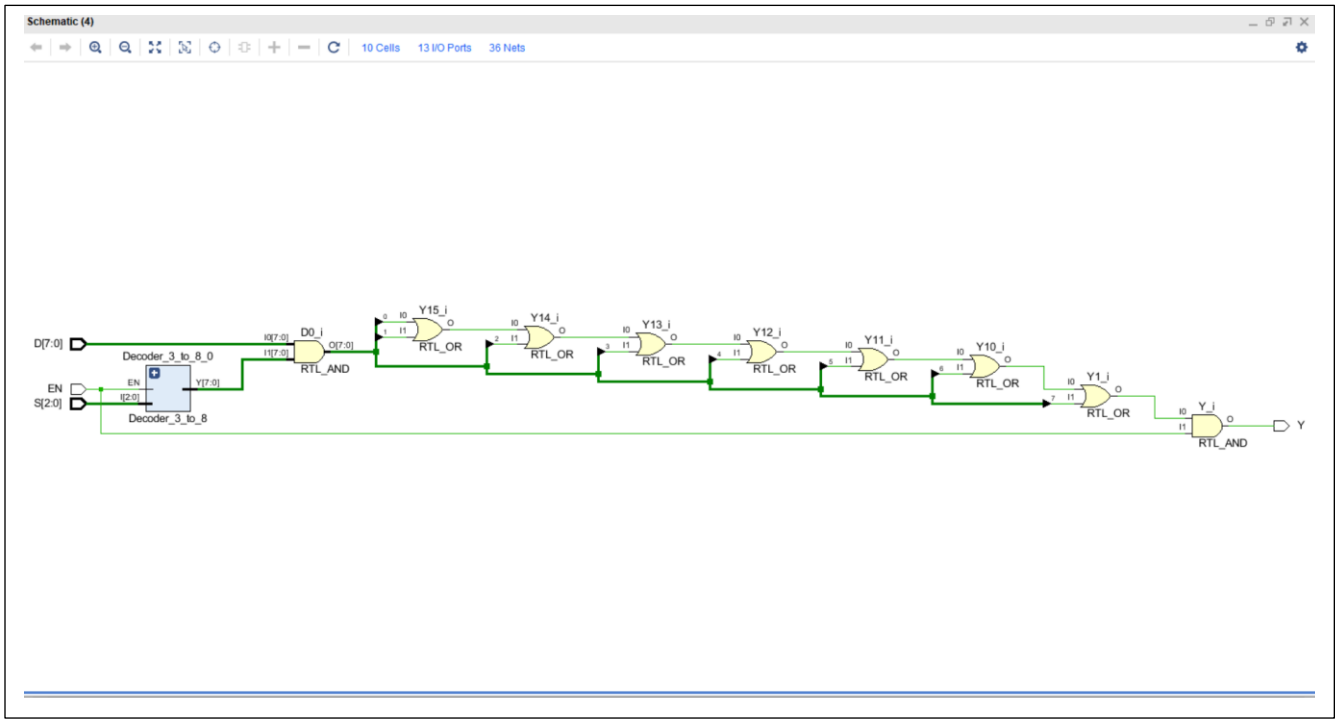
2_to_4 decoder



3_to_8 decoder

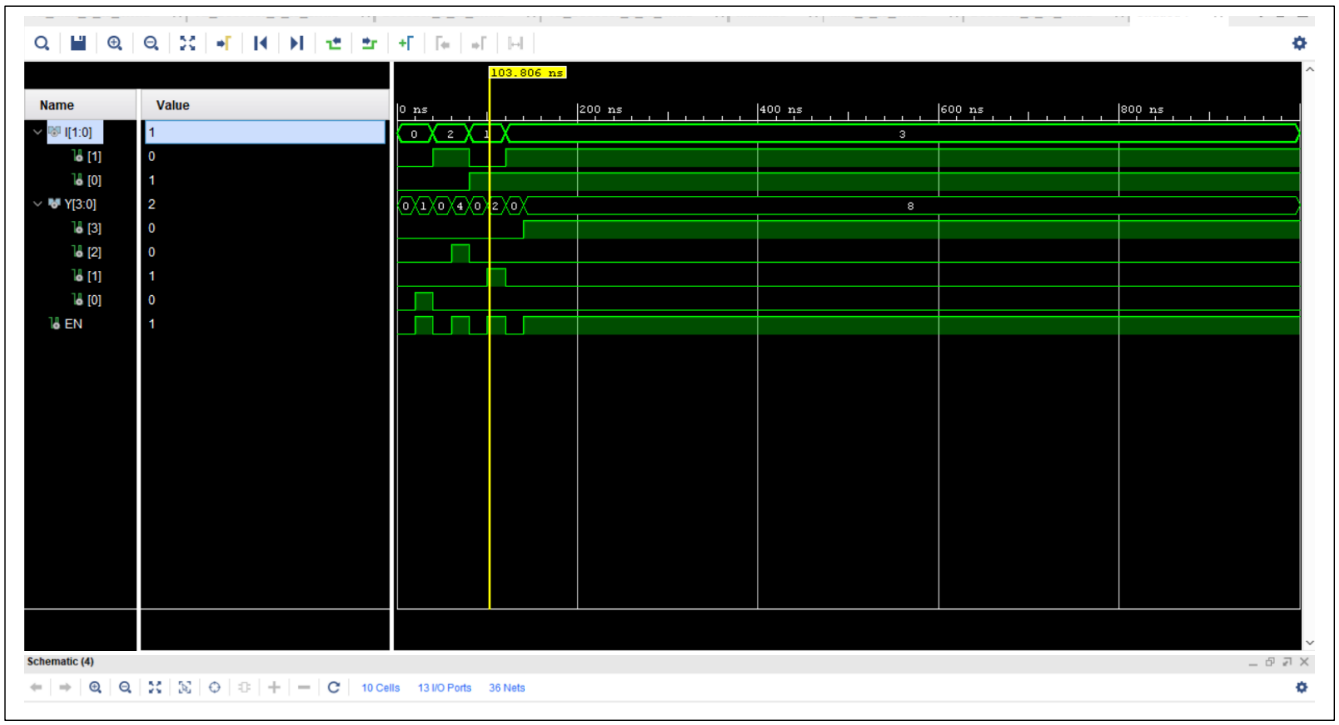


8_to_1 Multiplexer

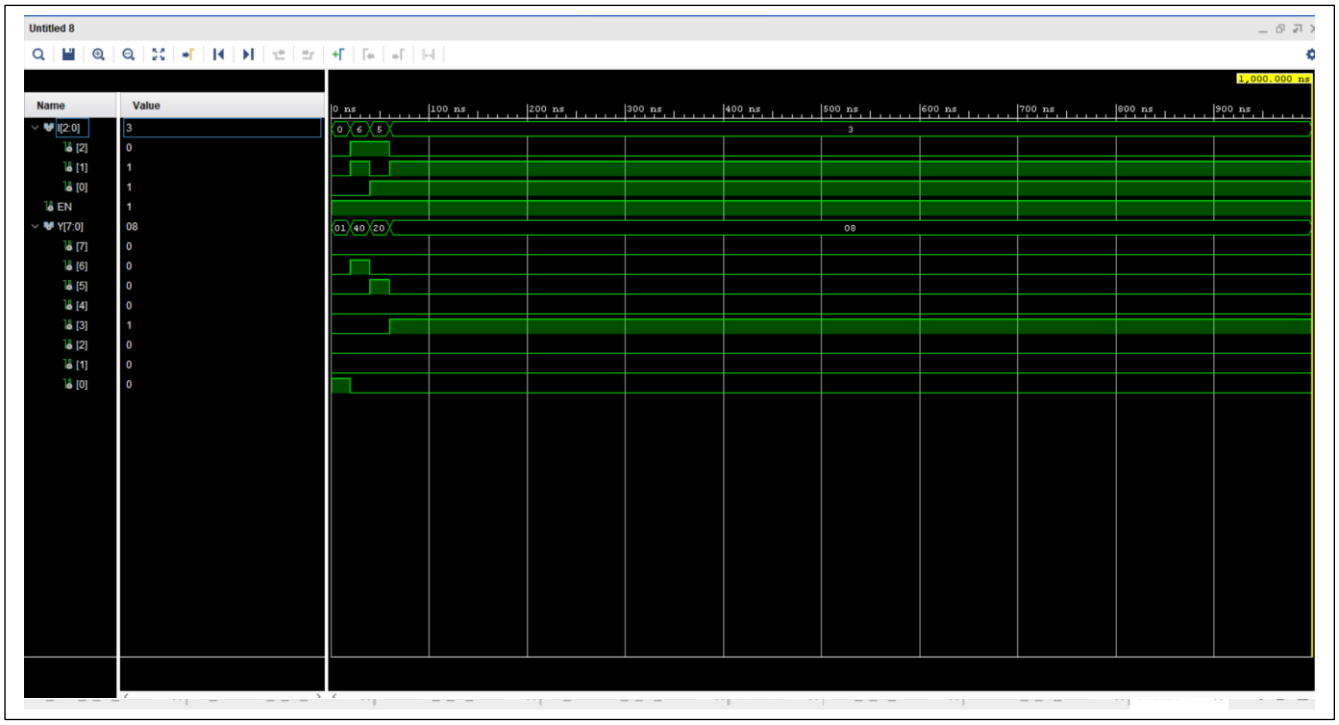


PART 3- Timing graphs

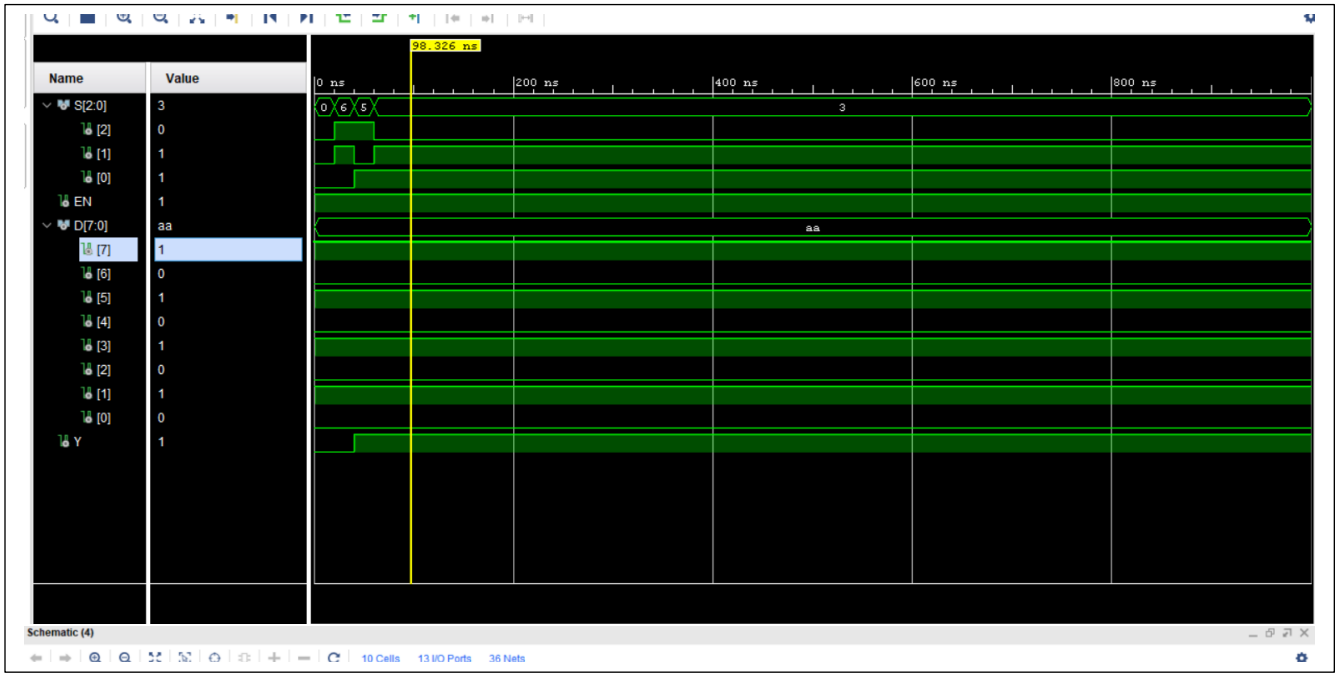
2_to_4 decoder



3_to_8 decoder



8_to_1 Multiplexer



PART 4- Conclusion

- Through this lab we could gain the experience on designing and simulating a decoder, and a multiplexer which are key components of a multiplexer.
- Two of the built 2- to 4 decoders were used to build the circuit for a 3 to 8 decoder and then one 3 to 8 decoder was again utilized to build the circuit for the multiplexer 8_to 1.
- Decoders converts binary data from n number of coded inputs to maximum of 2^n outputs
- Multiplexers can be used as a data selector where a particular input can be selected out of many.