November 16, 2021

Low Voltage Supply Static CMOS 2:1 MUX

FIVE DIFFERENT TECHNIQUES TO REDUCE STATIC POWER CONSUMPTION

Omama Mahmoud Hassan Elsayed Elrefaei, 2001704 | ECE612 | Fall 2021

Software tools:
Cadence Virtuoso, 65nm

Static CMOS Logic:

A static CMOS circuit has an nMOS pull-down network to connect the output to 0 (GND) and pMOS pull-up network to connect the output to 1 (V_{DD}). The networks are arranged such that one is ON and the other OFF for any input pattern.

Advantages:

1. Robustness (i.e., low sensitivity to noise), good performance, and easy to design,
2. Fast and low power consumption with no static power dissipation,
3. Insensitive to device variations, and minimum switching time,
4. Widely supported by CAD tools, and readily available in standard cell libraries,

Disadvantages:

1. Large area.

TECHNIQUES TO REDUCE STATIC POWER CONSUMPTION:

1] Transistor Stacking:

Stacked transistors will have larger V_{th} which will reduce the leakage current, and causes lower V_{DS} which will reduce the ON current.

Disadvantages:

1. Large transistor count and larger delay.

2] Negative Body Biasing (NBB):

Causes larger V_{th} which will reduce the leakage current.

Disadvantages:

1. Need body bias generation circuit, and triple well needed.

3] Schmitt Transistor Logic:

Output NMOS and PMOS increase V_{th} of middle NMOS and PMOS. Does not reduce the value of leakage, but allows operation at lower voltages.

Advantages:

1. Hysteresis improves noise performance,
2. Power mostly consumed by leakage quenching path.

4] Dynamic Leakage Suppression Logic (DLS):

Feedback path limits leakage path dynamically.

Disadvantages:

1. Very low frequency of operation.

TECHNIQUES TO REDUCE STATIC POWER CONSUMPTION:

5] Forward Body Biased DLS (FBB-DLS) [3]:

The DLS header and footer transistors was shown to greatly reduce logic gate delay with just a small increase in leakage power.

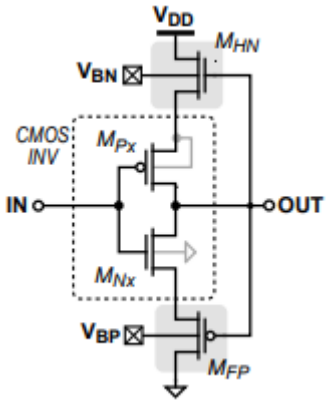


Fig. 1. The Forward Body Biased (FBB) DLS inverter logic gate.

For the pull-up logic, FBB lowers the V_T of M_{HN}, which leads to a significant increase in I_{ON}, and thus shorter gate delay. When the pull-up logic is leaking ($V_{IN} = V_{DD}$), the lower V_T of the M_{HN} increases the voltage V_X settles at from $V_{DD}/2$. This leads to:

I. $V_{GS,HN}$ being further reduced below $-V_{DD}/2$, which increases leakage due to Gate-Induced Drain Leakage (GIDL),
II. $V_{DS,HN}$ being decreased, which reduces leakage due to Drain-Induced Barrier Lowering (DIBL).

Where $V_{BN} = V_{DD}$ and V_{BP} = GND.

These two effects counteract, and result in a small net increase in I_{OFF}. A similar analysis can be done for the pull-down logic.

Advantages:

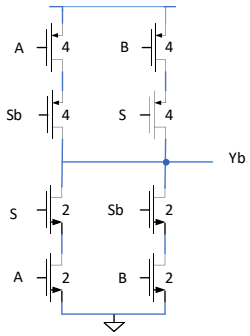
1. The L_{V_T} FBB variant enables circuits to operate at up to a few kHz.

Disadvantages:

1. The leakage power is less than an order of magnitude below the leakage floor of static CMOS implemented with H_{V_T} devices.

MUX 2-1:

In this project I used this mux schematic, which consists of two tristate buffer, and it is assumed to be perfectly symmetric $L_{min} = 60\ nm, W_{ref} = 120\ nm$.



S	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

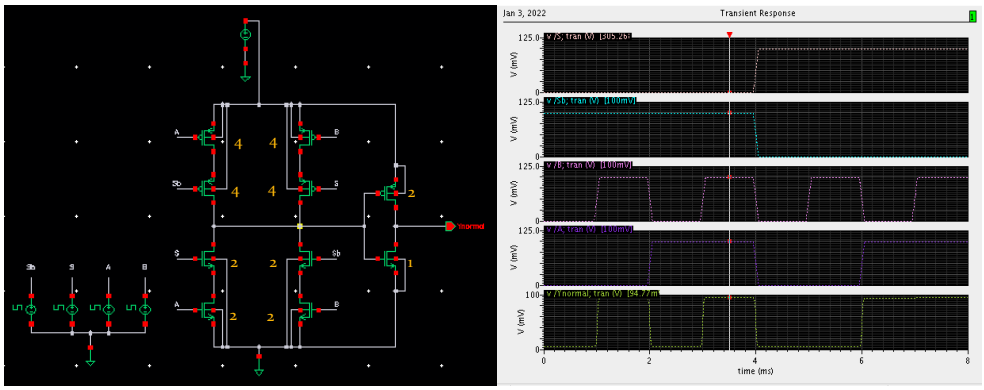
The total static current, I_{DD} is also called the leakage current or the quiescent supply current flowing between V_{DD} and GND. The static power consumption is proportional to this static current [2]:

$$P_{static} = I_{DD} * V_{DD}$$

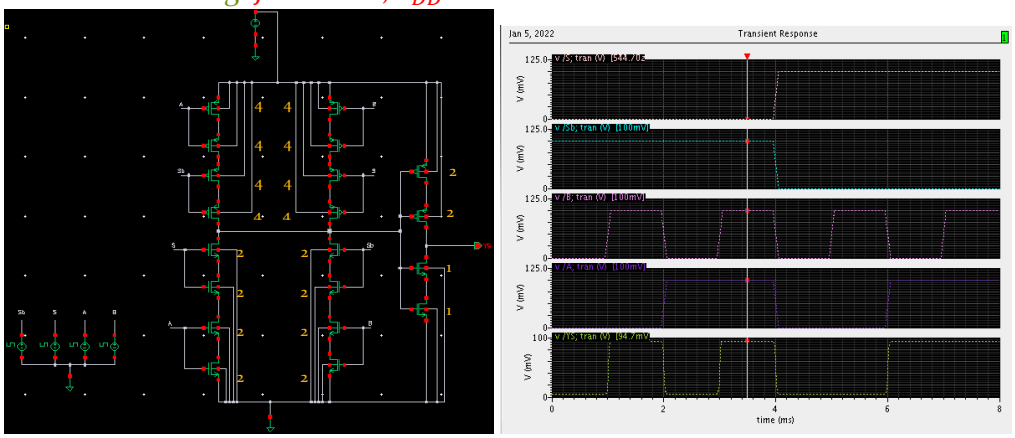
Testbench:

The logic 1 equal V_{DD}. NMOS, and PMOS are “nch”, and “pch”.

1] Normal: $f = 1KHz, V_{DD} = 0.1V$

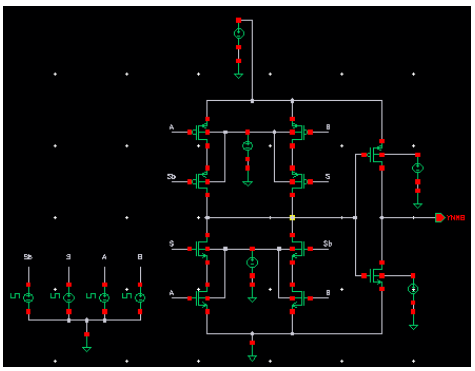


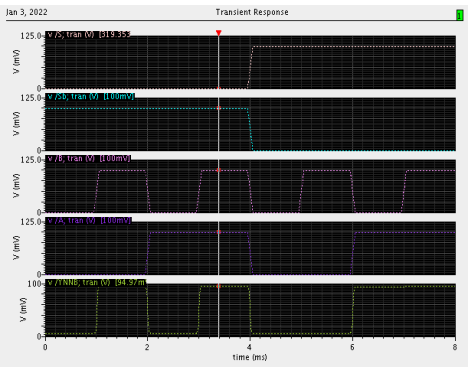
2] Transistor Stacking: $f = 1KHz, V_{DD} = 0.1V$



3] Negative Body Biasing: $f = 1KHz, V_{DD} = 0.1V$

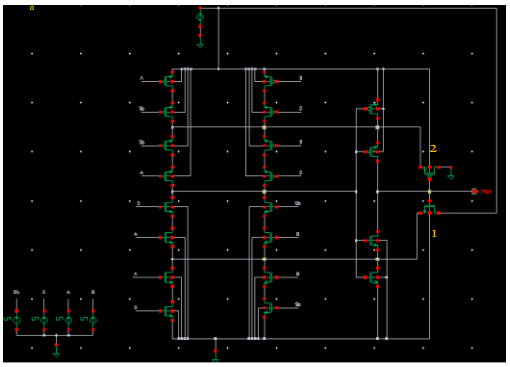
The size is the same as Normal.

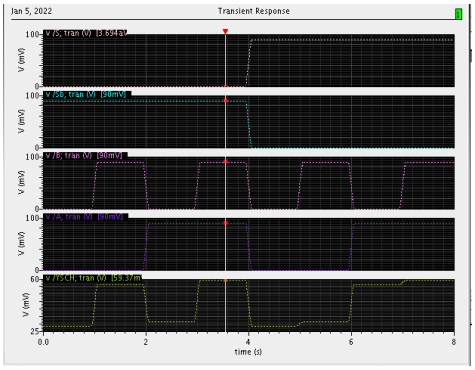




4] Schmitt Transistor Logic: $f = 1Hz, V_{DD} = 90mV$

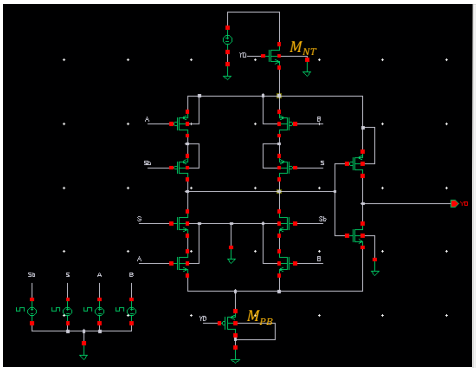
The other transistors are as Stacking.

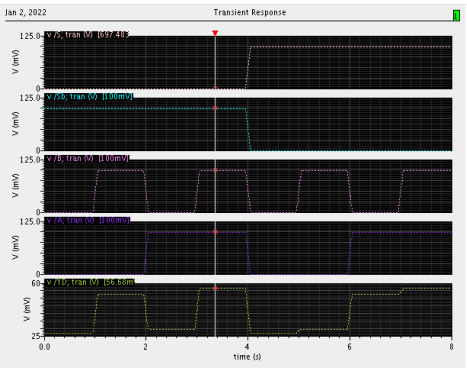




5] Dynamic Leakage-Suppression Logic: $f = 1Hz, V_{DD} = 0.1V$

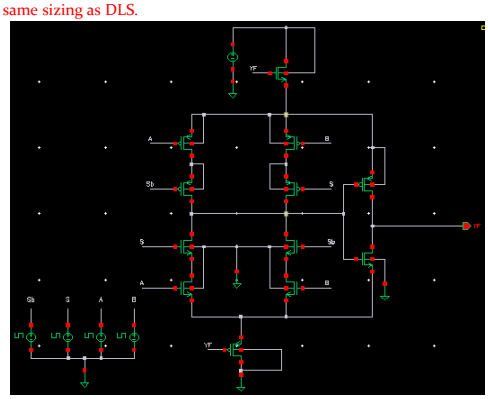
Since increasing W_{PB} and decreasing W_{NT} improves the OUT falling transition while degrading its rising transition, $W_{PB} = 12W_{ref,}$ and $W_{NT} = 6W_{ref}$ [3]. The other transistor sizes are the same as Normal.

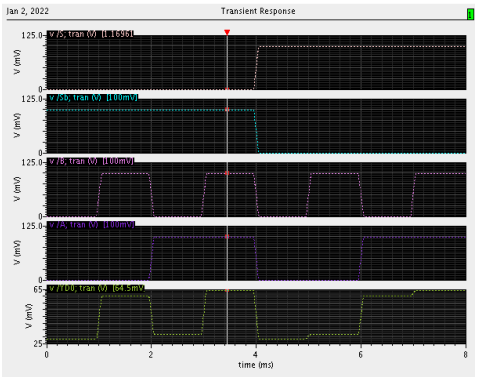




6] Forward Body Biased DLS: $f = 1Hz, V_{DD} = 0.1V$

The same sizing as DLS.

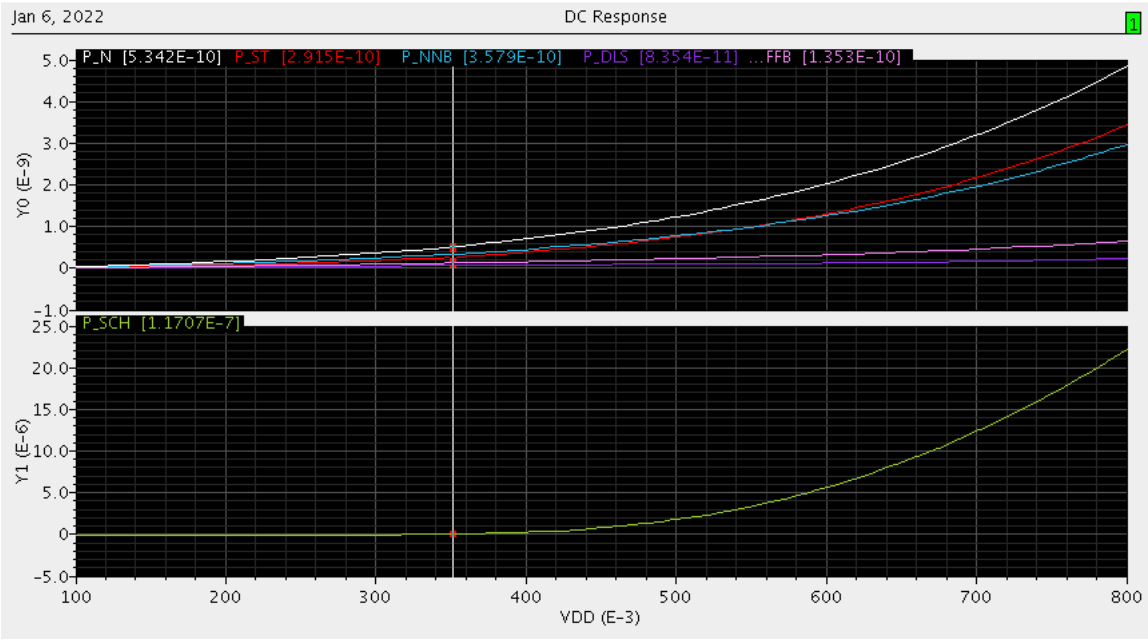




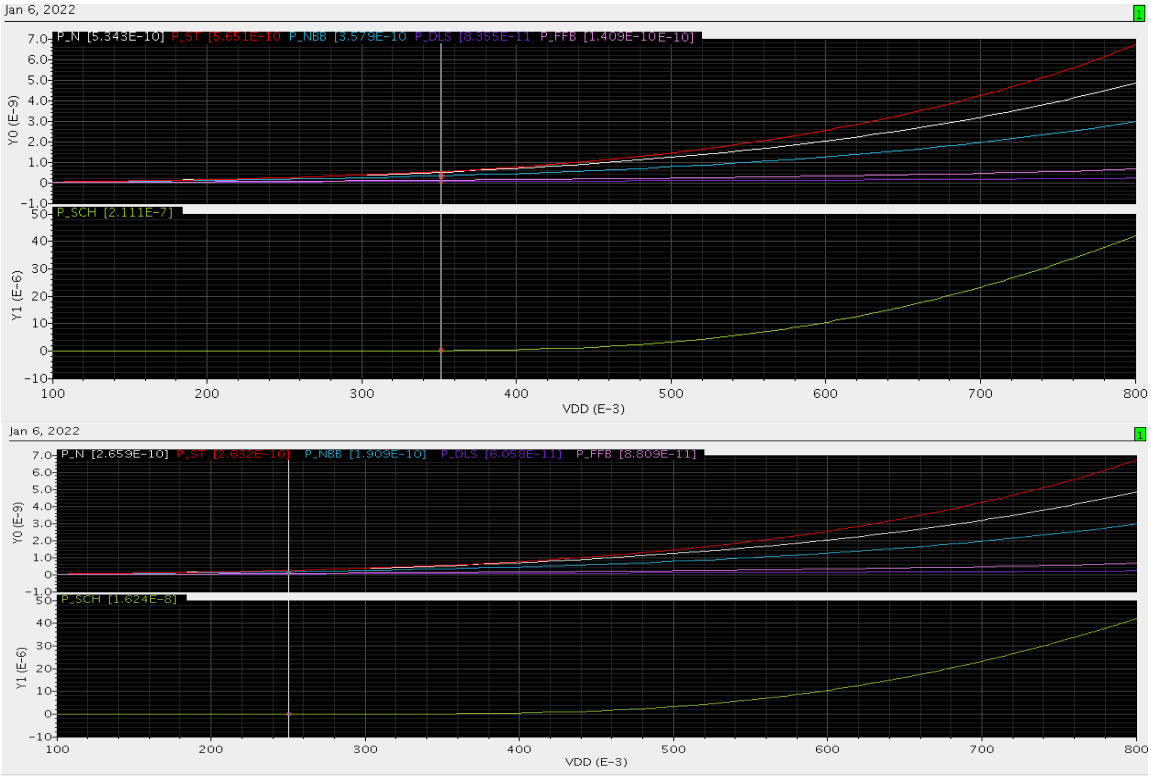
MUX 2-1:

Testbench:

To measure the static power I put all input stimulus by DC voltage sources to make all the circuit nodes stabilize on the operating point, and power consumption is constant. I run DC simulation sweeping V_{DD} from $0.1V$ to $0.8V$ to plot the power which equal the average of I_{DD} at the eight inputs conditions multiply by V_{DD}.



This when Transistor Stacking, and Schmitt Transistor Logic sized by 8, 4 for the tristate PUN and PDN, 4, 2 for the output inverter and Schmitt transistors PUN and PDN.



References:

[1] Rabaey: Sections 6.1 & 6.2

[2] Weste: Sections 9.1 & 9.2

[3] Lim, Wootaek, et al. "Batteryless Sub-nW Cortex-M0+ processor with dynamic leakage-suppression logic." Solid-State Circuits Conference-(ISSCC), 2015 IEEE International. IEEE, 2015.

[4] Truesdell, D. S., & Calhoun, B. H. (2019). Improving Dynamic Leakage Suppression Logic with Forward Body Bias in 65nm CMOS. 2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S). doi:10.1109/s3s46989.2019.9320713.