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# PAM4 Voltage-Mode Transmitter Design

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Software tools:
Cadence Virtuoso, 65nm

# Contents

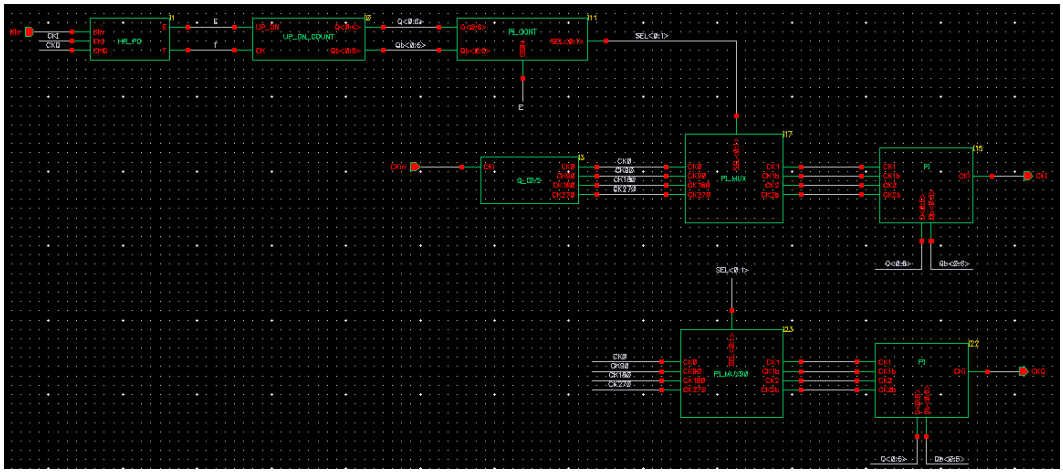
## Introduction

In the transmitter, the quarter-rate 4:1 multiplexer (MUX) is popular for the last serialization stage due to its relaxation on the timing constraint and low-power consumption in the clock path than the half-rate structure. However, the inputs of the 4:1 MUX should be skewed with 1 UI among each other by the retiming latches, increasing the power consumption in both data and clock paths.

In this design the retiming latches of the quarter-rate 4:1 MUX are eliminated by adopting an automatic phase alignment technique, achieving a power-efficient and robust design.

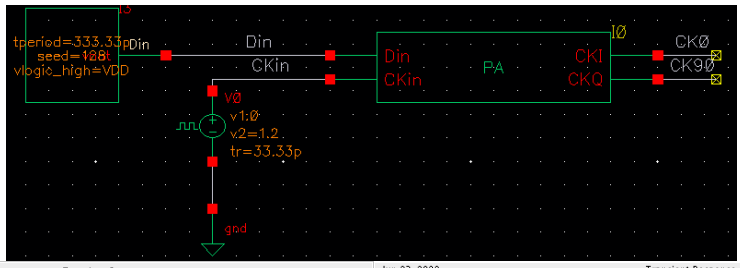
## Chapter 1 **Phase Aligner**

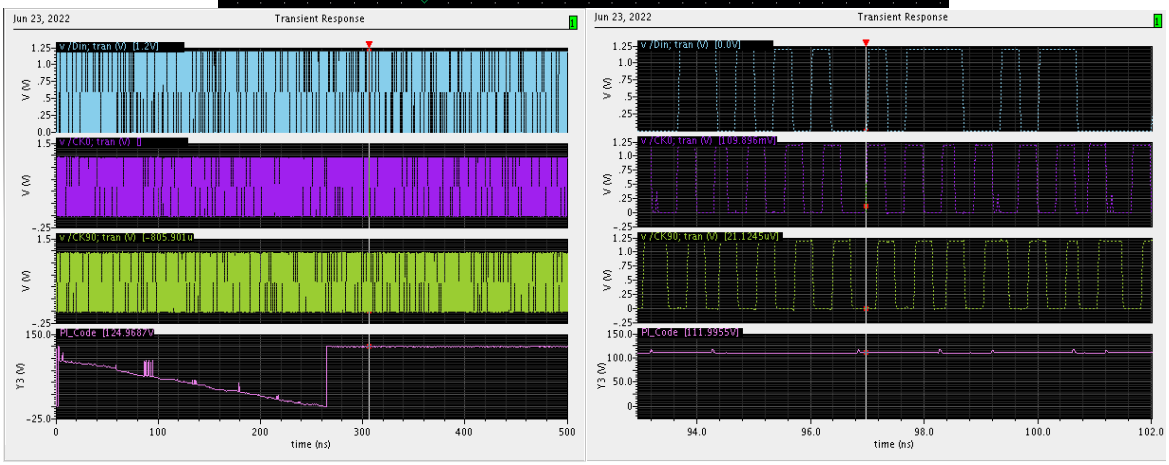
The phase aligner consists of a two Phase Interpolators (PIs), Half-Rate Phase Detector, and an Accumulator that implements control logic for the PIs.



Simulation:

- *$CK_{in}$ is 3GHz*
- *Data rate ($D_{in}$) is 3Gbps*
- *$R = 750\,\Omega$*
- *$I_{DC} = 100\ uA$*
- *$I_{COMP} = 35\ uA$*
- *$V_{DD} = 1.2\ V$*

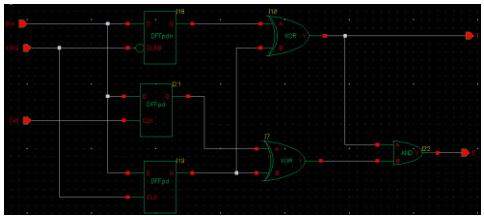


### 1.1 Half-Rate Phase Detector (HR-PD)

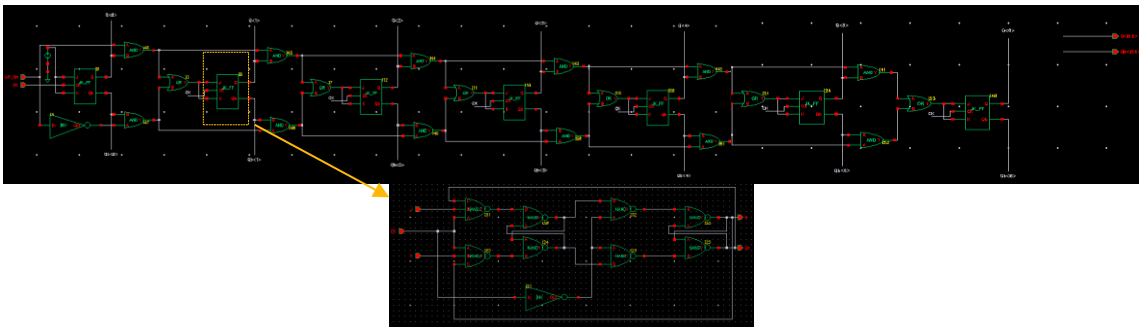
The Half-rate Alexander PD compares the links received data to the negative edge of the clock signal from the VCO and the present data bit with the previous data bit. The output of the PD is three signals (T, E). The Transition "T" signal indicates there has been a transition in the data stream while the Early "E" signal indicates the position of the rising edge VCO clock relative to the data stream rising edge.

The PD output drives the accumulator. The transition signal triggers the accumulator to count-up or down while the Early signal is used as the accumulator sign bit with a 1 signaling count-down (increase phase) and a 0 signaling count-up (decrease phase).



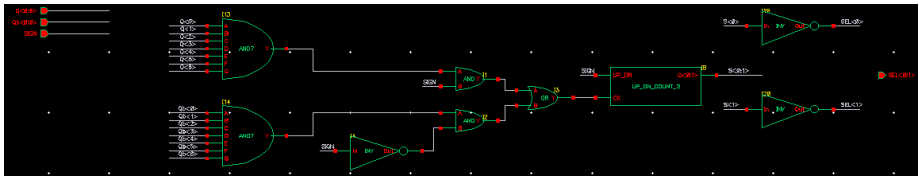
### 1.2 Accumulator

The accumulator is comprised of a 7-bit up/down counter. It is designed from transistor level JK-FF's and logic gates (AND, OR). Accumulator clock is triggered from the transition signal from the PD and the sign bit comes from the PD "E" signal.



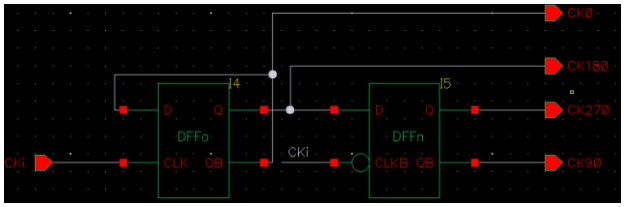
### 1.3 Phase Interpolator Controller

The controller is comprised of two 7-bit AND, one OR, three inverters, and a 2-bit up/down counter.



### 1.4 Quadrature Divider

The quadrature divider divide the input clock by two and produce four different phases.

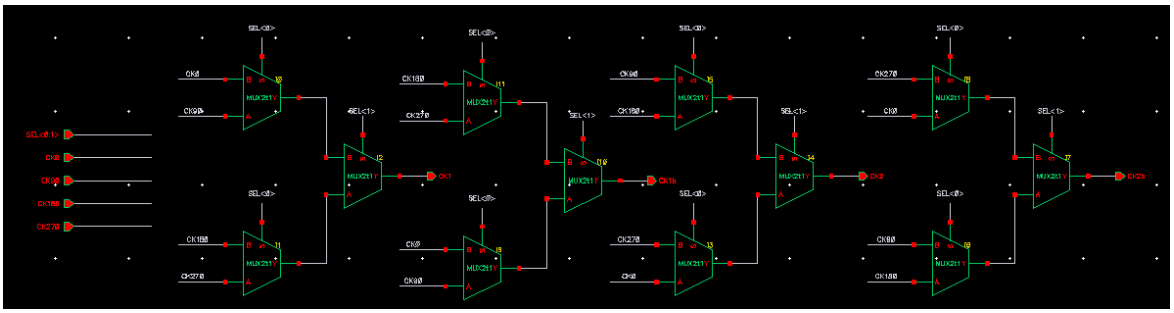


## 1.5 Voltage Control Oscillator Selector

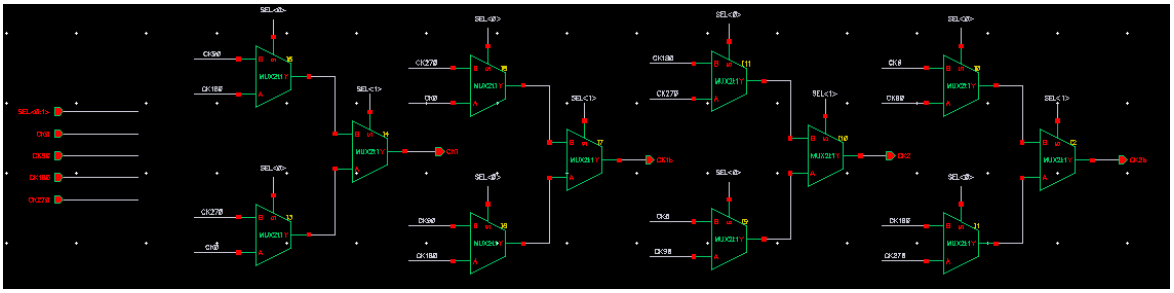
The first PI is supposed to choose 1 region out of 4, which are 0°-90°, 90°-180°, 180°-270°, 270°-0°, where the second PI is supposed to choose 1 region out of 4, which are 90°-180°, 180°-270°, 270°-0°, 0°-90°.

So each PI needs to have its own mux select logic to rotate from region to region if the desired phase delay is not in the current region. 7-bit data is 128 in decimal so the phase delay resolution is $\frac{90°}{128} = 0.703°$.

First selector:

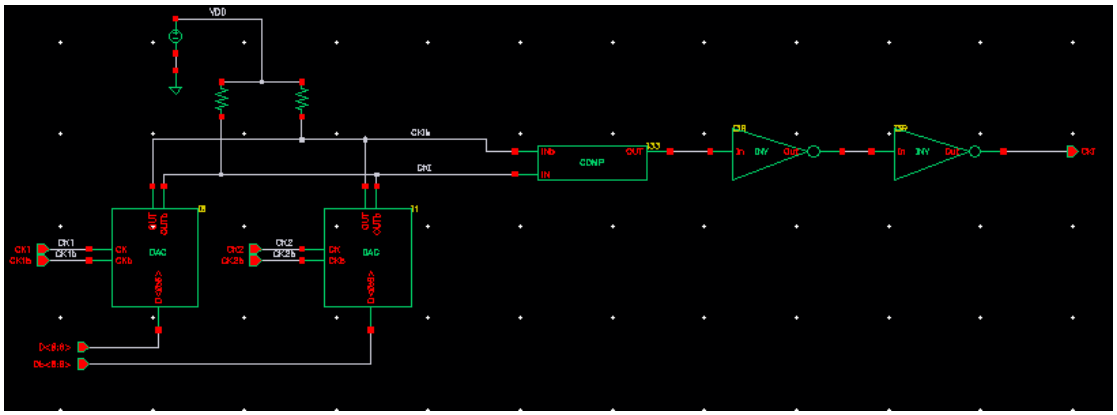


Second selector:



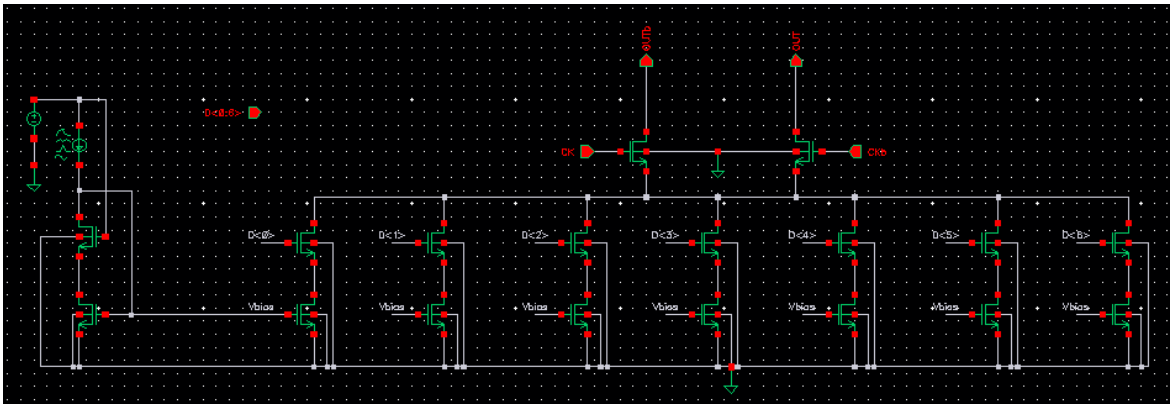
## 1.6 Phase Interpolator (PI)

The Phase Interpolator is constructed with two 7-bit current DAC's differentially tied to termination resistors. The differential summing node signal is converted to single ended with a differential pair.



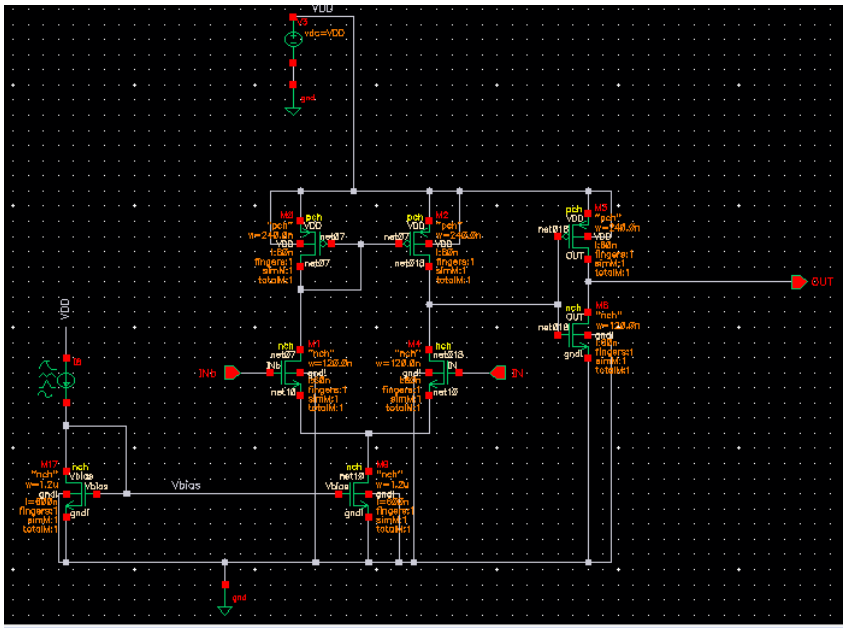
### 1.6.1 Digital to Analog Converter (DAC)

The DAC and associated current steering pair are designed to provide full rail differential swing.



### 1.6.2 Comparator

A comparator on the current summing node provides single ended output to an output buffer for driving the PD.



### 1.6.3 Output Buffer

The output buffer is two stages of inverters.

## References


1] https://www2.eecs.berkeley.edu/Pubs/TechRpts/2018/EECS-2018-63.pdf

2] Pen-Jui Peng;Yan-Ting Chen;Sheng-Tsung Lai;Hsiang-En Huang; (2021). A 112-Gb/s PAM-4 Voltage-Mode Transmitter with Four-Tap Two-Step FFE and Automatic Phase Alignment Techniques in 40-nm CMOS. IEEE Journal of Solid-State Circuits, (), –. doi:10.1109/jssc.2020.3038818.