

Q₂

(a) Similarities

- * Both are PIC microcontrollers made by Microchip
- * Both use Harvard architecture, which means they have separate memory for program and data
- * Both can be programmed with assembly language or C
- * Both support digital I/O, timers, and interrupts

Difference

- * 16F84A is simpler. It has less memory 13 I/O pins, and no ADC
- * 16F877 is advanced. It has more memory 33 I/O pins, built-in ADC, PWM and USART

(b)

Faster development

- * Changes and test can be tested immediately
No need to remove the chip
- * Reduces risk of damaging pins or boards
Can debug in real environment
- * You can see how the microcontroller behaves with real sensors or motors

- (c)
- * Reprogrammable - You can erase and write it many times
 - * Non-volatile - It keeps data when power is off
 - * Faster and cheaper

- (d)
- * The CPU processes 8 bits at a time
 - * The registers and data bus are 8 bit wide

(e) "8 k" means $8 \times 1024 = 8192$ words

In pic microcontrollers, each word is 14 bits

$$\begin{aligned}\text{total bits} &= 8192 \times 14 \\ &= 114,688 \text{ bits}\end{aligned}$$

(f) The RC circuit connected to RESET is called a Power On Reset circuit

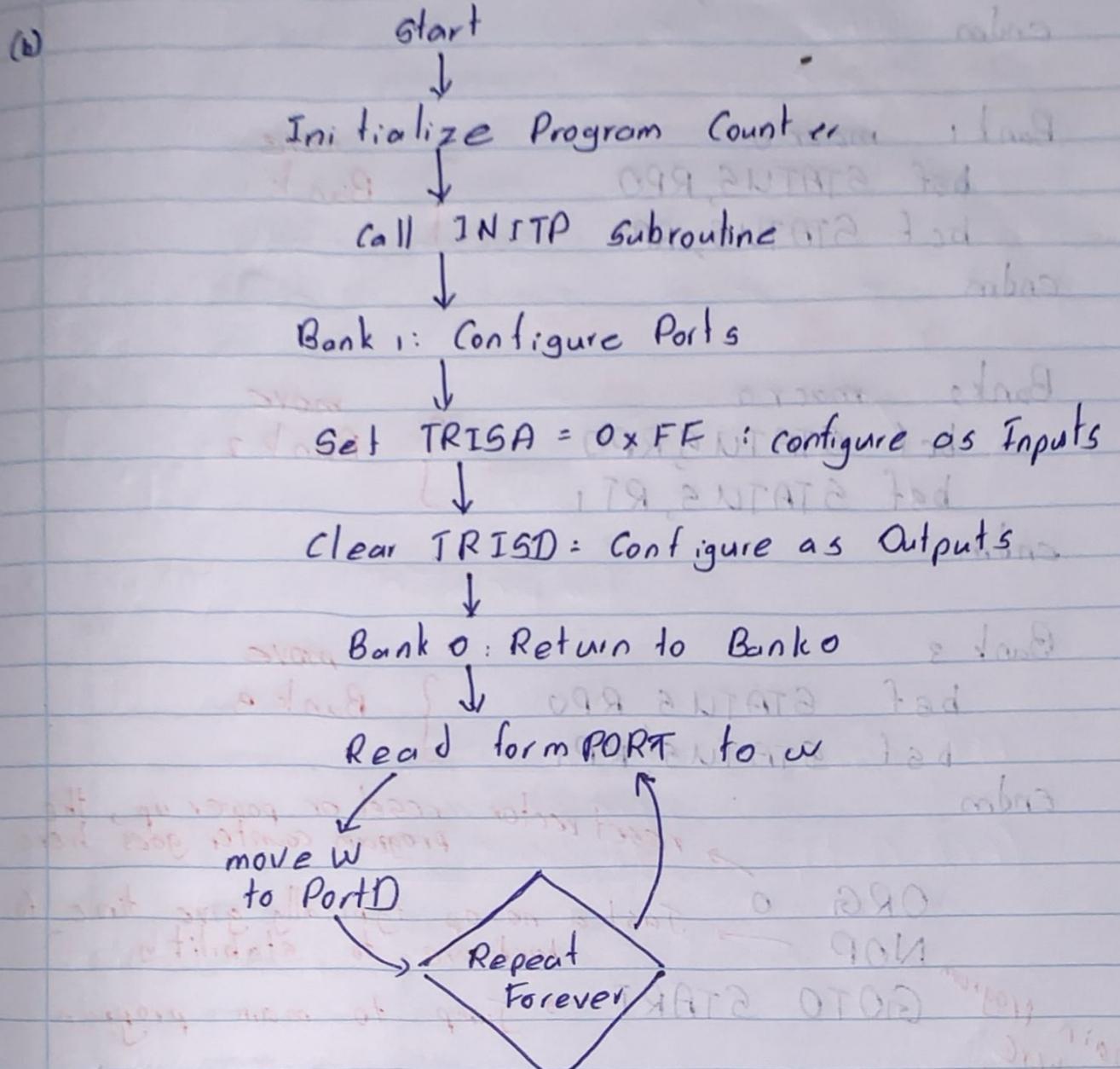
* when a power is turn on, the capacitor charges slowly. keeping the RESET pin LOW for a short time

* This gives time for the power supply to stabilize

* The RESET goes HIGH, and the microcontroller starts running normally

(i) `movlw b'1110000'`
Load binary to working register
`movwf trish`
Move the contents of WREG into the TRIGB register

Q. (a) Push Button LED Array Controller



CALL INTL

AT90S8513

AT90S8513

AT90S8513

Logic control logic

in bin a hex code

and now set of all

values

Atlas

goal

not solve yet

no integer problem

0 to 1000 digits

(c) Bank 0 macro

```

bcf STATUS, RP0
bcf STATUS, RP1
endm

```

move
Bank 0

Bank 1 macro

```

bsf STATUS, RP0
bcf STATUS, RP1
endm

```

move
Bank 1

Bank 2 macro

```

bcf STATUS, RP0
bsf STATUS, RTI
endm

```

move
Bank 2

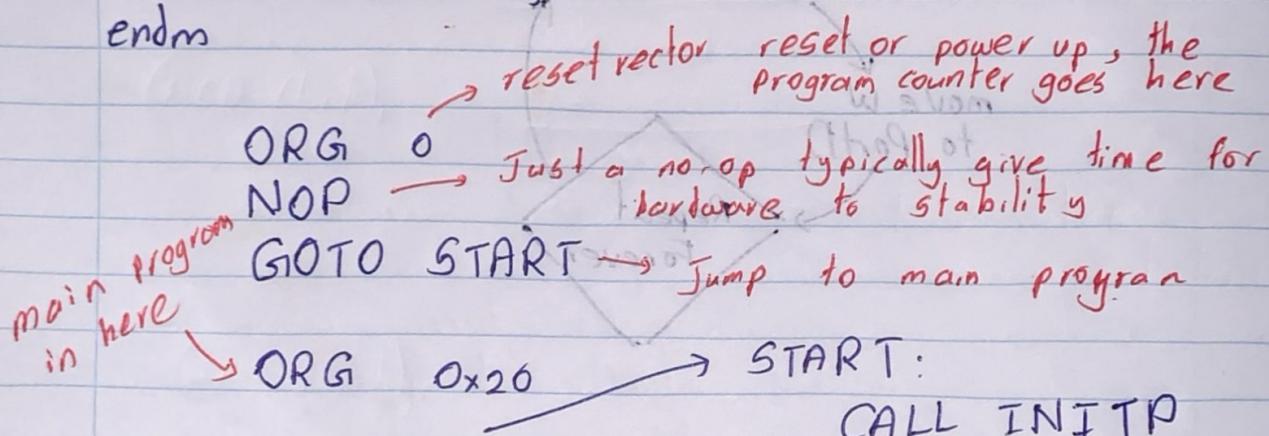
Bank 3

```

bsf STATUS, RP0
bsf STATUS, RP1
endm

```

move
Bank 3



REPEAT :

```

MOVF PORTA,W
MOVF PORTD
GOTO REPEAT

```

call INITP to configure PORT A and PORT D

give value from working register and put into portD

Loop

Read button input from port A and put in to the working Register

INIT

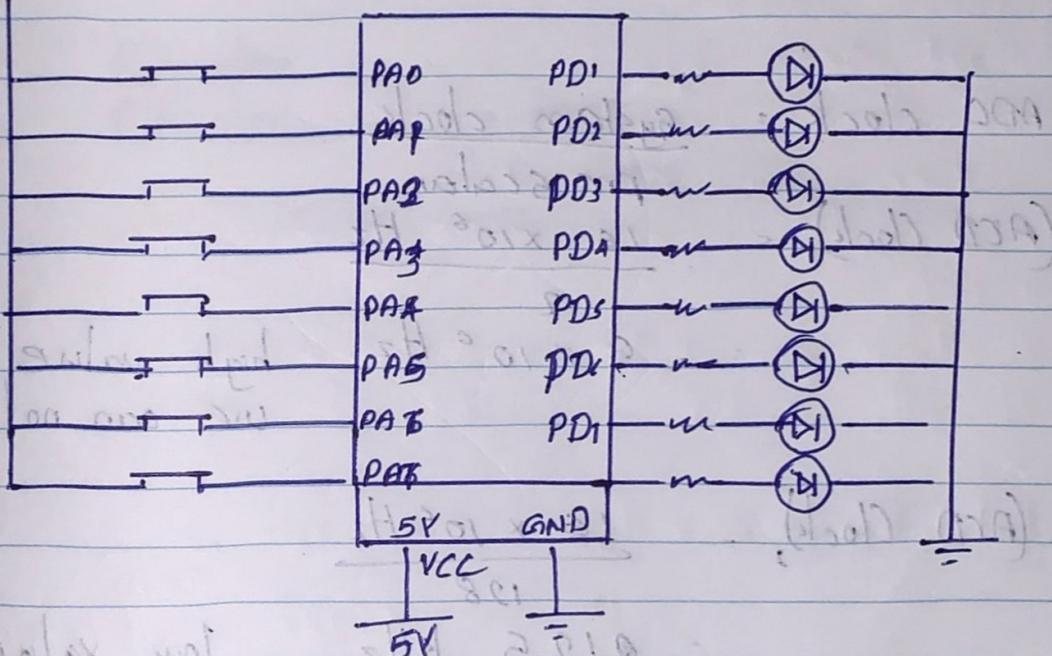
INI TP:

Bank 1 → switch to Bank 1 to access TRIS
 MOVWF TRISB → do this for PORTB
 MOVLW 0x06 → ADCON1 = 0000 0110 (Bank 1)
 MOVLW 0xFF → ADCON0 = 0000 0001 (Bank 0)
 MOVWF TRISA → Configure analog pins as digital (off A/D on PORTA)
 MOVWF TRISD → Set all Port D pins as inputs
 CLRF TRISD → set all Port D pins as outputs
 BANK 0 → RETURN to Bank 0 for normal operation

END

(d)

5V

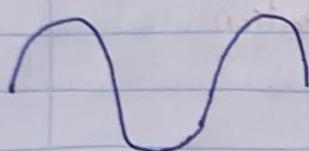


Q₃

(a)

(i) void initHardware(void){
 DDRA = 0b1111110; //WVOM
 DDRC = 0b1111111; //WVOM
 //TxD WIVOM}

(ii) We can use the system clock to convert the analog signal to digital.



low pre scaler

high pre scaler

ADC clock = system clock

$$(\text{ADC clock})_1 = \frac{16 \times 10^6}{1} \text{ Hz}$$

$$= 16 \times 10^6 \text{ Hz}$$

high value

we can not identify.

$$(\text{ADC clock})_2 = \frac{16 \times 10^6 \text{ Hz}}{128}$$

$$= 125 \text{ kHz}$$

low value

we can identify

(ii) void initADC(void)

{
ADCSRA |= (1 << ADEN);

ADCSRA |= (1 << ADPS2) | (1 << ADPS1) | (1 << ADPS0);

(iv) ADCSRA |= (1 << ADSC);

(v) while (ADCSRA & (1 << ADSC));

(vi) PORTA |= ones | (tens << 4);

PORTC |= hundreds | (thousands << 4);

(vii) Register
Register = 1×10^3

and 002P to

latching point

002P

1 added on a step by step

1 x 10³ x A = sum conversion. Total

002P

threshold 881. A

b) ~~10~~

(b) 20 bits bps (iv)

(i) stop bit

* no of parity bit and 1st bit should be same even or odd

* baud rate of the devices

* Number of data carry bit (Data frame format)

* Voltage levels

(v)

(ii) Total bits per frame = start bit

8 data bit

1 parity bit

1 stop bit

10 bit

At 9600 bps

$$\text{time per bit} = \frac{1}{9600}$$

$$\text{Time per byte} = 10 \text{ bits} \times \frac{1}{9600}$$

$$\begin{aligned} \text{total transmission time} &= 4 \times 10 \times \frac{1}{9600} \\ &= 4.168 \text{ milliseconds} \end{aligned}$$

(c) Watchdog timer

Crucial points

- a System recovery mechanism that automatically reset the microcontroller if software becomes unresponsive
- b Acts as a failsafe against software bugs, unexpected conditions, or hardware issues that cause program execution to freeze
- c Requires periodic resets by properly functioning software to prevent timeout
- d Can be configured with different timeout periods depending on application requirement.

Ques: What is a watchdog timer?

Ans: A watchdog timer is a timer that monitors the system's operation. If the timer times out before it receives a reset signal from the application, it triggers a system reset.

Q.

(a) UART

Asynchronous serial communication (no clock signal)

2 (Tx, Rx)

Full duplex

Longer range

SPI

Synchronous serial communication (with clock signal)

4: MOSI, MISO, SCLK, SS

Full duplex

Short range

I₂C

Synchronous Serial communication (with clock signal)

2 (SDA, SCL)

Half duplex

Short to medium range

(b) (i) Communication mechanism between ATmega328P and LCD

Parallel communication

typically 4-bit or 8-bit interface

```

② #include <avr/io.h>
#include <util/delay.h>
#include "LCD-Commands.h"

int main(void) {
    LCD_Init();
    LCD_SetCursor(0, 0);
    LCD_WriteString("Embedded Systems");
    for (int i = 0; i < 16; i++) {
        delay_ms(300);
        LCD_ShiftLeft();
    }
    for (int i = 0; i < 16; i++) {
        delay_ms(300);
        LCD_ShiftRight();
    }
    LCD_Clear();
    LCD_SetCursor(1, 0);
    LCD_WriteString("DEIE");
    while (1) {
}
}

```

- (c) (i) Three SPI settings to match between transmitter and receiver.
01. Clock polarity (CPOL)
 02. Clock phase (CPHA)
 03. Data order (MSB / LSB first).

:(0,1,1,0,1)

(ii) Slave Select Pin

- * The SS pin is used by the master to select a specific slave device for communication.
- * When SS is LOW (0), the slave is selected and responds to SPI signals.
- * If the master selects more than one slave at a time, multiple devices may try to send data simultaneously, causing bus contention and data corruption.

:(0,0,1) am - polish.

:(0,1,1,0,1,0,1)

- (d) Burn in testing involves running hardware components under stressfull conditions for a prolonged period to identify early failures.

:(0,1,0,0,1,0,1)

:(0,1,1,0,1)

:(0,1,1,0,1)

:(0,1,1,0,1)

:(0,1,1,0,1)

No: _____ Date: _____
3e (a) November 2024

Operating System Programming

SOCK_STREAM

Provides sequenced, reliable, two way, connection based byte streams. It uses TCP.

SOCK_DGRAM