Semiconductor Design and Verification Training

JoSDC'23

Training Description:

This training offers a comprehensive exploration of digital logic design principles with a strong emphasis on practical applications using Simulation and Field-Programmable Gate Arrays (FPGAs). Through a combination of theoretical instruction and hands-on exercises, students will develop a solid understanding of digital circuits, logic design, and FPGA programming. In addition, the training will teach the fundamentals of timing analysis, simulation and debugging using FPGA tools, Assertions, and static verification. In addition, participants will learn the fundamentals of Universal Verification Methods (UVM) which is a standard method for verifying digital designs and System-on-Chip (SoC) in the semiconductor industry.

The DE10-Lite Development and Education Boards will be used throughout the training. Those boards have been developed to provide an ideal tool for learning about digital technology in a laboratory setting. The software tool required to use the DE10-Lite boards is the Intel Quartus Prime Lite Edition and the ModelSim simulator. It is recommended to have the DE-series board connected to your computer that has Quartus Prime software installed. If you don't have access to any DE-series boards, following the training modules should still be effective and teach you the FPGA programming and configuration tasks performed.

Prerequisites:

- Previous knowledge of Verilog/VHDL,
- Digital Logic Design fundamentals.

Training Duration: This is a four-week training (Sunday – Wednesday) program consisting of a total of six hours of theory and eight hours of practical training per week.

Training Outline:

Week No.	Day	Covered Topic	Description
1	Sunday	Introduction to Digital Logic Hardware Design	Introduction to FPGA and the basic input/output devices (switches, LEDs, Multiplexers, and seven-segment displays) using Quartus Prime Software (Lite Edition).
	Monday	Numbers and Display	Designing combinational circuits that can perform binary-to-decimal number conversion and binary-coded-decimal (BCD) addition.
	Tuesday	Latches, flip-flops, and registers.	Investigate latches, flip-flops, and registers.
	Wednesday	Counters	Understand and implement counters using Verilog.

2	Sunday	Timers and Real-Time Clock	Study the use of clocks in timed circuits.
	Monday	Adders, Subtractors, and Multipliers	Examine arithmetic circuits that add, subtract, and multiply numbers.
	Tuesday	FSM	Implement a finite state machine (FSM) in Verilog
	Wednesday	Memory Blocks	Learn how to use different prebuilt memory modules that are provided in libraries and load memory modules with data when the circuit is programmed into the FPGA chip.
3	Sunday	Design a simple processor	Build a digital system that contains a number of 16-bit registers, a multiplexer, an adder/subtracter, and a control unit (finite state machine).
	Monday	Timing Analysis	Learn fundamentals of timing analysis for digital electronics
	Tuesday	Simulation and Debugging	fundamentals of logic simulation and FPGA debugging tools available in Quartus using the DE10-Lite development kit
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4	Sunday	Static Verification	Static Verification, Introduction to UVM & Assertions
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	Tuesday	Special Topics	TBD
	Wednesday	Special Topics	TBD

Assessment Methods:

- Attending and successful completion of all labs is a prerequisite for receiving a certificate of completion for this training course.
- Throughout the training, you will be assigned a number of in-class assignments that need to be submitted, as well as some assignments that you will be asked to complete at home.