**JoSDC Test benchmarks**

**Instructions:**

* For benchmark #1 make sure to fill out the “Expected Results” column.
* For benchmark #2:
  + If you implemented an out-of-order processor you are allowed to use Loop Unrolling for performance improvement.
  + It is recommended to start with size 20 and then transition to size 2000 for more comprehensive testing.
  + When submitting your work, please consider submitting the size 2000 version.
  + If your team encounters difficulties running the size 2000 version, you may submit the size 20 version along with proper justification.
* Any additional functionality or modifications made to the design after submitting Phase III report must be clearly documented.

**Benchmark #1:**

Instructions should be hand-assembled, converted to hexadecimal, and loaded into the instruction memory.

Initializing Registers (Testing I-Type ALU):

|  |  |  |
| --- | --- | --- |
| Instruction | Hexadecimal | Expected Result |
|  |  | Initialize r1 = 0xf1e0 |
| ori r2 ,r0, 4 |  | r2 = |
| addi r3, r0, -2 |  | r3 = |
|  |  | Initialize r4 = 0x001e |

Testing R-Type ALU Instructions (NO RAW hazards – NO Forwarding)

|  |  |  |
| --- | --- | --- |
| Instruction | Hexadecimal | Expected Result |
| add r5, r1, r1 |  | r5 = |
| sub r6, r1, r2 |  | r6 = |
| and r6, r3, r4 |  | r6 = |
| or r7, r1, r2 |  | r7 = |
| xor r5, r1, r3 |  | r5 = |
| nor r6, r1, r2 |  | r6 = |
| sll r7, r4, r2 |  | r7 = |
| srl r5, r1, r2 |  | r5 = |

Testing RAW hazards and Forwarding

|  |  |  |
| --- | --- | --- |
| Instruction | Hexadecimal | Expected Result |
| add r5, r1, r1 |  | r5 = |
| sub r6, r5, r4 |  | r6 = |
| and r7, r5, r6 |  | r7 = |
| ori r5, r5, 0x000f |  | r5 = |

Testing SW and LW

|  |  |  |
| --- | --- | --- |
| Instruction | Hexadecimal | Expected Result |
| sw r1, 0(r0) |  | MEM[0] = |
| sw r4, 1(r0) |  | MEM[1] = |
| lw r5, 0(r0) |  | r5 = MEM[0] = |

Testing Load delay, stalling pipelining, and forwarding after LW

|  |  |  |
| --- | --- | --- |
| Instruction | Hexadecimal | Expected Result |
| lw r6, 1(r0) |  | r6 = MEM[1] = |
| andi r7, r6,0x000b |  | r7 = |
| sw r7, 2(r0) |  | MEM[2] = |
| lw r5, 0(r0) |  | r5 = MEM[0] = |
| sw r5, 3(r0) |  | MEM[3] = |

Testing Branch and Jump Instructions

|  |  |  |
| --- | --- | --- |
| Instruction | Hexadecimal | Expected Result |
| beq r1, r1, P1 |  |  |
| add r5, r2, r2 |  |  |
| P1: bne r0, r1, P2 |  |  |
| add r6, r2, r2 |  |  |
| add r7, r4, r4 |  |  |
| P2: j P3 |  |  |
| add r5, r2, r2 |  |  |
| add r6, r4, r4 |  |  |
| P3: add r0, r0, r0 |  |  |

**Benchmark #2:**

1. Bubble Sort(20 elements):

Description/C Code:

* Declare an array of size 20 with values as given in the Assembly code below
* Initialize your design RAM and registers as needed
* Perform the given bubble sort algorithm such that the array elements are in ascending order

Assembly:

|  |
| --- |
| .data  array: .word 32000, 14849, 5683, 3987, 1024, 982, 401, 373, 183, 94, 68, 25, 6, -1, -39, -284, -620, -9102, -20375, -31000  .text  main:  jal sort  j end  sort:  la R16, array #This is a sudo instruction called "load address" that saves the initial address of array in register R16.  addi R8, R0, 0  addi R17, R0, 19    sortLoop1:  bgt R8, R17, sortEndloop1  addi R9, R0, 0  sub R10, R17, R9    sortLoop2:  bgt R9, R10, sortEndloop2  sll R11, R9, 2  add R12, R16, R11  lw R13, 0(R12)  lw R14, 4(R12)  bgt R13, R14, swap  j endSwap    swap:  add R15, R13, R0  add R13, R14, R0  add R14, R15, R0  sw R13, 0(R12)  sw R14, 4(R12)    endSwap:  addi R9, R9, 1  j sortLoop2    sortEndloop2:  addi R8, R8, 1  j sortLoop1    sortEndloop1:  jr R31    end:  add R0, R0, R0 |

1. Bubble Sort(2000 elements):

Description/C Code:

* Declare an array of size 2000 with values as given in the Assembly code below
* Initialize your design RAM and registers as needed
* Perform the given bubble sort algorithm such that the array elements are in ascending order

Assembly:

|  |
| --- |
| .data  array: .word 31995, 31991, 31988, 31986, 31950, 31900, 31878, 31847, 31754, 31734, 31683, 31636, 31609, 31583, 31567, 31559, 31559, 31556, 31533, 31398, 31366, 31360, 31302, 31261, 31246, 31069, 31046, 31004, 30985, 30927, 30926, 30898, 30864, 30858, 30844, 30838, 30797, 30746, 30714, 30696, 30666, 30590, 30563, 30550, 30527, 30460, 30367, 30228, 30208, 30169, 30078, 30073, 30040, 30031, 29946, 29905, 29891, 29890, 29773, 29763, 29729, 29717, 29717, 29621, 29594, 29535, 29528, 29513, 29490, 29490, 29458, 29443, 29372, 29368, 29346, 29292, 29285, 29225, 29223, 29222, 29142, 28993, 28952, 28952, 28870, 28865, 28808, 28801, 28724, 28679, 28669, 28617, 28603, 28589, 28579, 28577, 28522, 28518, 28501, 28471, 28451, 28433, 28411, 28366, 28341, 28288, 28288, 28246, 28236, 28229, 28193, 28182, 28170, 28148, 28063, 28044, 28027, 28004, 27946, 27892, 27855, 27844, 27824, 27817, 27739, 27728, 27724, 27723, 27700, 27676, 27634, 27606, 27505, 27483, 27449, 27416, 27415, 27376, 27356, 27334, 27333, 27296, 27235, 27232, 27218, 27211, 27177, 27165, 27116, 27046, 27032, 27016, 26949, 26907, 26895, 26786, 26767, 26753, 26750, 26723, 26711, 26702, 26671, 26544, 26526, 26472, 26458, 26444, 26438, 26405, 26392, 26361, 26338, 26329, 26281, 26279, 26271, 26130, 26118, 26097, 26072, 26054, 26044, 26044, 26039, 26039, 26018, 26003, 25938, 25818, 25818, 25804, 25761, 25673, 25629, 25494, 25485, 25388, 25319, 25302, 25237, 25217, 25203, 25197, 25187, 25082, 25050, 24967, 24954, 24919, 24913, 24893, 24870, 24835, 24824, 24778, 24755, 24711, 24707, 24658, 24629, 24618, 24601, 24534, 24463, 24422, 24415, 24390, 24381, 24377, 24355, 24248, 24219, 24189, 24182, 24179, 24149, 24107, 24097, 24086, 24083, 24020, 24003, 23970, 23919, 23885, 23827, 23821, 23732, 23712, 23657, 23636, 23573, 23566, 23562, 23541, 23517, 23500, 23499, 23464, 23463, 23438, 23414, 23413, 23365, 23363, 23360, 23350, 23318, 23318, 23285, 23284, 23237, 23216, 23205, 23187, 22978, 22976, 22937, 22921, 22876, 22851, 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