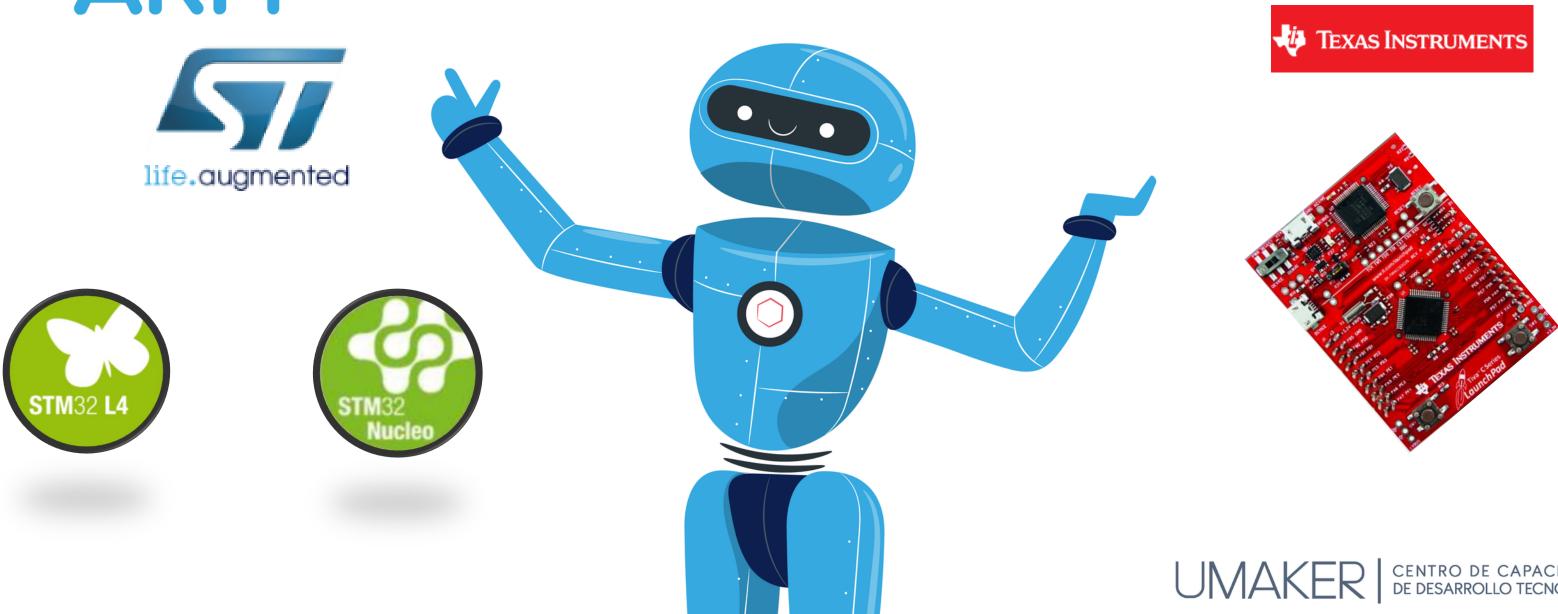
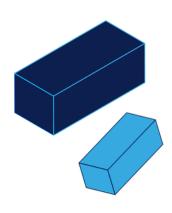
CLASE 4: SYSTICK

MICROCONTROLADORES ARM





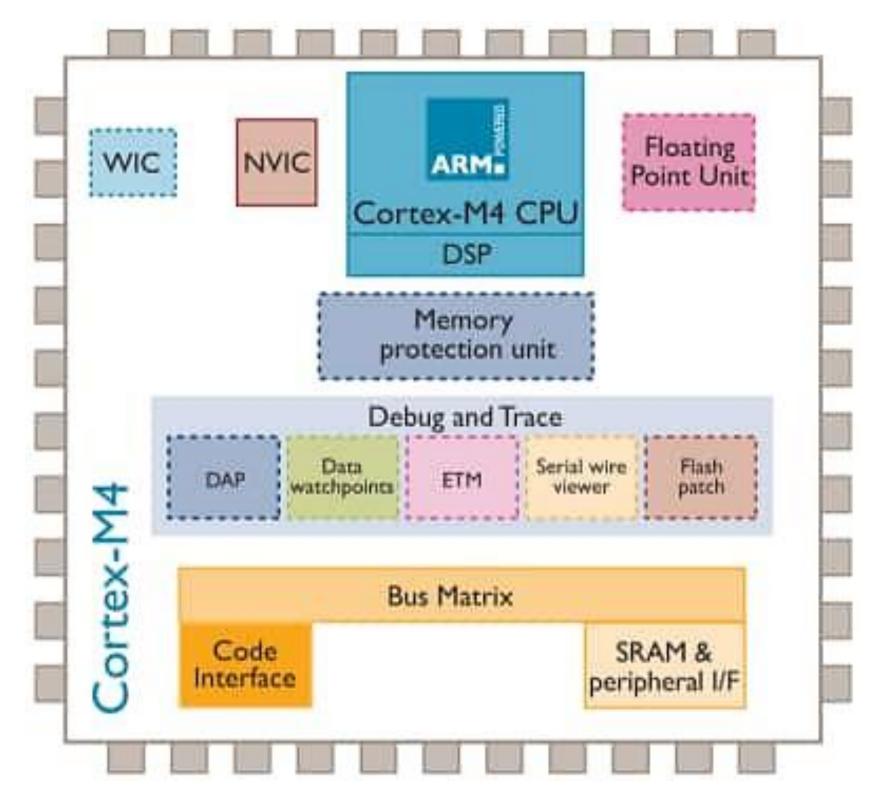
PERIFERICOS CORTEX-M4





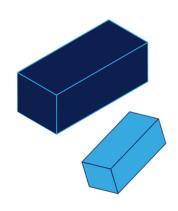


- SysTick
- NVIC
- SCB
- MPU
- FPU









SYSTICK TIMER

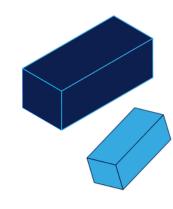


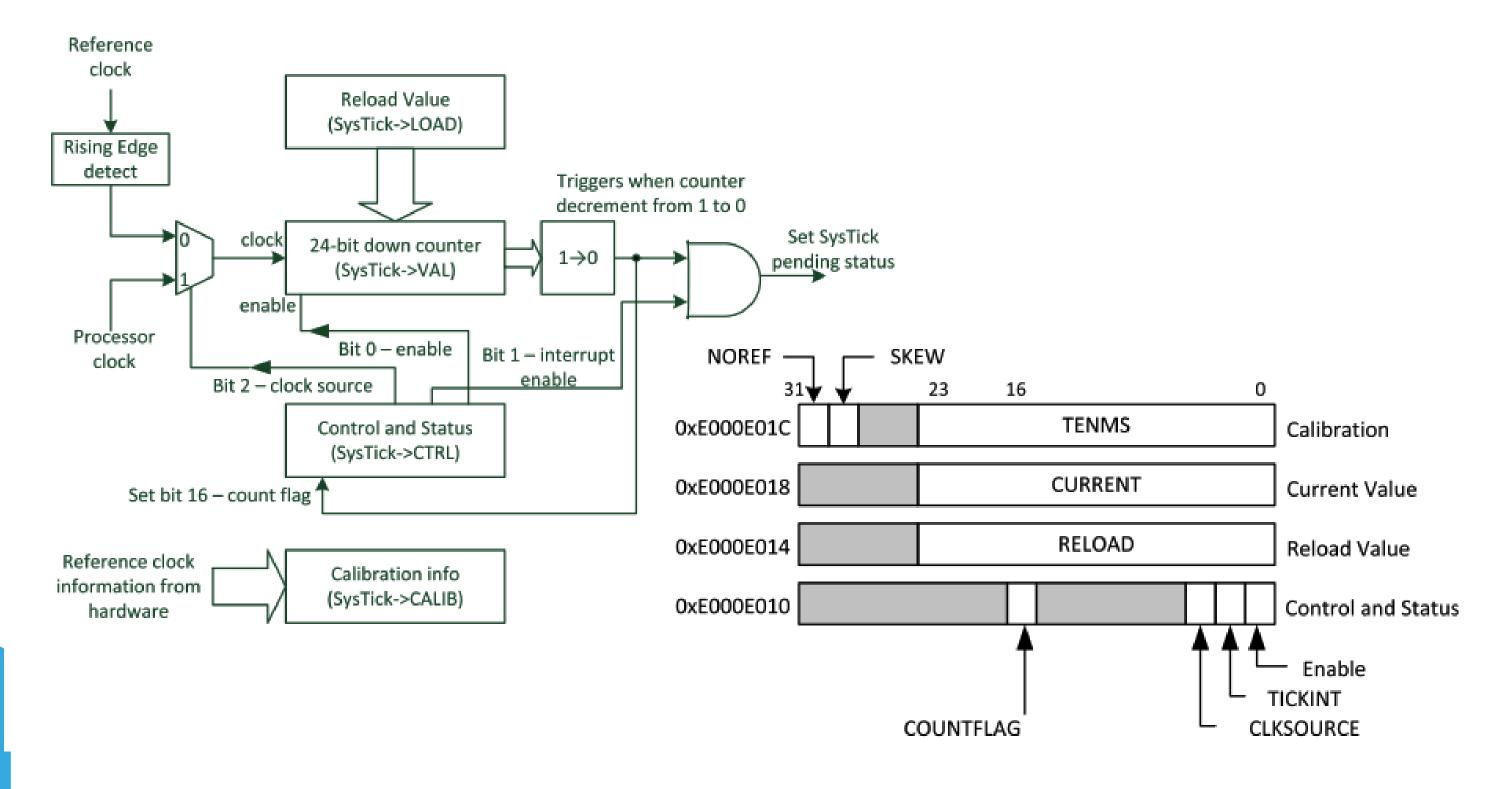
- El procesador CORTEX M4 incluye un temporizador del sistema integrado conocido como SysTick de 24 bits de longitud de palabra. El contador es de 24 bits y de decremento .
- El contador del **SysTick** se ejecuta en sincronización del reloj del sistema (system clock) o del oscilador interno (SYSCLK) divido por 8.
- Está integrado como parte del NVIC y puede generar la excepción SysTick (tipo de excepción n. ° 15).
- Si no necesita un sistema operativo integrado en su aplicación (RTOS), el temporizador SysTick se puede utilizar como un simple periférico temporizador para la generación periódica de interrupciones, la generación de retardos o la medición de tiempos.





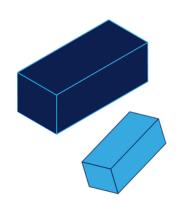
FUNCIONAMIENTO







UMAKER CENTRO DE CAPACITACIÓN DE DESARROLLO TECNOLÓGICO



CONFIGURACION DEL SYSTICK TIMER





SYSTICK REGISTROS

Address	CMSIS-Core Symbol	Register
0xE000E010	SysTick->CTRL	SysTick Control and Status Register
0xE000E014	SysTick->LOAD	SysTick Reload Value Register
0xE000E018	SysTick->VAL	SysTick Current Value Register
0xE000E01C	SysTick->CALIB	SysTick Calibration Register





REGISTROS

SysTick control and status register (STK_CTRL)

Address offset: 0x00

Reset value: 0x0000 0000

Required privilege: Privileged

The SysTick CTRL register enables the SysTick features.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							Reserve	ed							COUNT FLAG
															rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										CLKSO URCE	TICK INT	EN ABLE			
													rw	rw	rw

Bits 31:17 Reserved, must be kept cleared.

Bit 16 COUNTFLAG:

Returns 1 if timer counted to 0 since last time this was read.

Bits 15:3 Reserved, must be kept cleared.

Bit 2 CLKSOURCE: Clock source selection

Selects the clock source.

0: AHB/8

1: Processor clock (AHB)

Bit 1 TICKINT: SysTick exception request enable

0: Counting down to zero does not assert the SysTick exception request

1: Counting down to zero to asserts the SysTick exception request.

Note: Software can use COUNTFLAG to determine if SysTick has ever counted to zero.

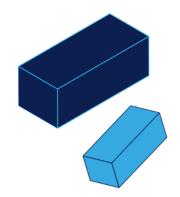
Bit 0 ENABLE: Counter enable

Enables the counter. When ENABLE is set to 1, the counter loads the RELOAD value from the LOAD register and then counts down. On reaching 0, it sets the COUNTFLAG to 1 and optionally asserts the SysTick depending on the value of TICKINT. It then loads the RELOAD value again, and begins counting.

0: Counter disabled

1: Counter enabled







REGISTROS

SysTick reload value register (STK LOAD)

Address offset: 0x04

Reset value: 0x0000 0000

Required privilege: Privileged

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			Pas	erved							RELOA	D[23:16]			
			Res	erveu				ΓW	rw	rw	ΓW	rw	ΓW	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RELOAD[15:0]															
rw	rw	rw	ΓW	rw	ΓW	rw	rw	ΓW	rw	rw	rw	rw	rw	rw	rw

Bits 31:24 Reserved, must be kept cleared.

Bits 23:0 RELOAD: RELOAD value

The LOAD register specifies the start value to load into the STK_VAL register when the counter is enabled and when it reaches 0.

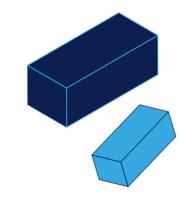
Calculating the RELOAD value

The RELOAD value can be any value in the range 0x00000001-0x00FFFFF. A start value of 0 is possible, but has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.

The RELOAD value is calculated according to its use:

- To generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. For example, if the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.
- To deliver a single SysTick interrupt after a delay of N processor clock cycles, use a RELOAD of value N. For example, if a SysTick interrupt is required after 100 clock pulses, set RELOAD to 99.







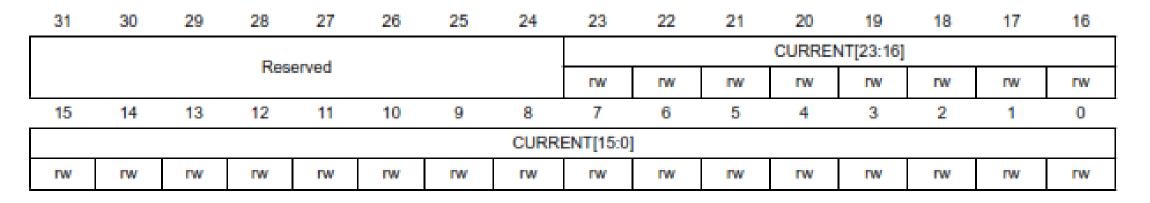
REGISTROS

SysTick current value register (STK VAL)

Address offset: 0x08

Reset value: 0x0000 0000

Required privilege: Privileged



Bits 31:24 Reserved, must be kept cleared.

Bits 23:0 CURRENT: Current counter value

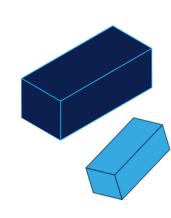
The VAL register contains the current value of the SysTick counter.

Reads return the current value of the SysTick counter.

A write of any value clears the field to 0, and also clears the COUNTFLAG bit in the STK_CTRL register to 0.







SYSTICK REGISTROS

SysTick calibration

value register (STK CALIB)

Address offset: 0x0C Reset value: 0x000000

Required privilege: Privileged

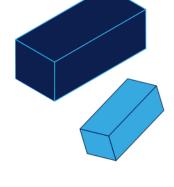
The CALIB register indicates the SysTick calibration properties.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NO REF	SKEW			Res	erved			TENMS[23:16]							
г	r							r	г	г	г	Г	Г	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TENMS[15:0]															
Γ	Γ	Γ	Γ	Γ	Г	Γ	Γ	Γ	Γ	Γ	Γ	Г	Γ	Γ	Г

- Bit 31 NOREF: NOREF flag. Reads as zero. Indicates that a separate reference clock is provided. The frequency of this clock is HCLK/8.
- Bit 30 **SKEW:** SKEW flag: Indicates whether the TENMS value is exact. Reads as one. Calibration value for the 1 ms inexact timing is not known because TENMS is not known. This can affect the suitability of SysTick as a software real time clock.
- Bits 29:24 Reserved, must be kept cleared.
- Bits 23:0 **TENMS[23:0]:** Calibration value. Indicates the calibration value when the SysTick counter runs on HCLK max/8 as external clock. The value is product dependent, please refer to the Product Reference Manual, SysTick Calibration Value section. When HCLK is programmed at the maximum frequency, the SysTick period is 1ms.

If calibration information is not known, calculate the calibration value required from the frequency of the processor clock or external clock.







CONFIGURACION DEL SYSTICK TIMER

Para la configuración se deben seguir los siguientes pasos:

- 1. Desactivar el contador. ENABLE=0.
- 2. Cargar el valor de RELOAD.
- 3. Escribir cualquier valor en la cuenta para que se ponga a 0.
- 4. Configurar los registros de control y estado, incluyendo la activación.

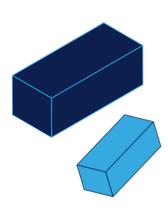
```
ValorDe Recarga = SysTickCounterClock \times TemporizacionDeseada(s) \\ ValorDe Recarga = 16000000 \times 0.001 \\ ValorDe Recarga = 16000
```

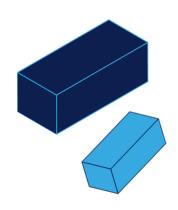
Estos pasos pueden ser realizados por la función SysTick_Config

```
STATIC INLINE uint32 t SysTick Config (uint32 t ticks)
□ {
   if ((ticks - lUL) > SysTick LOAD RELOAD Msk)
                                                                     /* Reload value impossible */
     return (1UL);
   SysTick->LOAD = (uint32 t) (ticks - 1UL);
                                                                     /* set reload register */
   NVIC SetPriority (SysTick IRQn, (1UL << NVIC PRIO BITS) - 1UL); /* set Priority for Systick Interrupt */
   SysTick->VAL = OUL;
                                                                     /* Load the SysTick Counter Value */
   SysTick->CTRL = SysTick CTRL CLKSOURCE Msk |
                    SysTick CTRL TICKINT Msk
                    SysTick CTRL ENABLE Msk;
                                                                     /* Enable SysTick IRQ and SysTick Timer */
                                                                     /* Function successful */
   return (OUL);
```







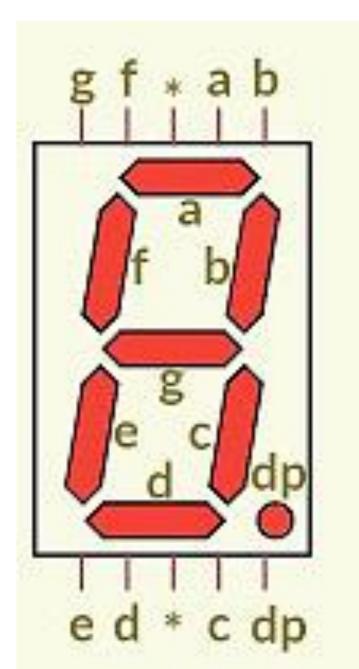


MULTIPLEXACION DE DISPLAY DE 7 SEGMENTOS





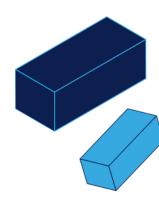
DISPLAY 7 SEGMENTOS CATADO COMUN



HEX					n	mu	Có	Cátodo	
	a	b	С	d	е	f	g	Número	Común*
0 x 3 F	1	1	1	1	1	1	0	0	GND
0x06	0	1	1	0	0	0	0	1	GND
0 x 5B	1	1	0	1	1	0	1	2	GND
0x4F	1	1	1	1	0	0	1	3	GND
0x66	0	1	1	0	0	1	1	4	GND
0x6D	1	0	1	1	0	1	1	5	GND
0x7D	1	0	1	1	1	1	1	6	GND
0x07	1	1	1	0	0	0	0	7	GND
0x7F	1	1	1	1	1	1	1	8	GND
0x67	1	1	1	1	0	1	1	9	GND

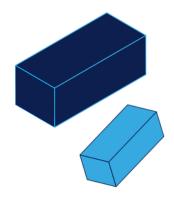


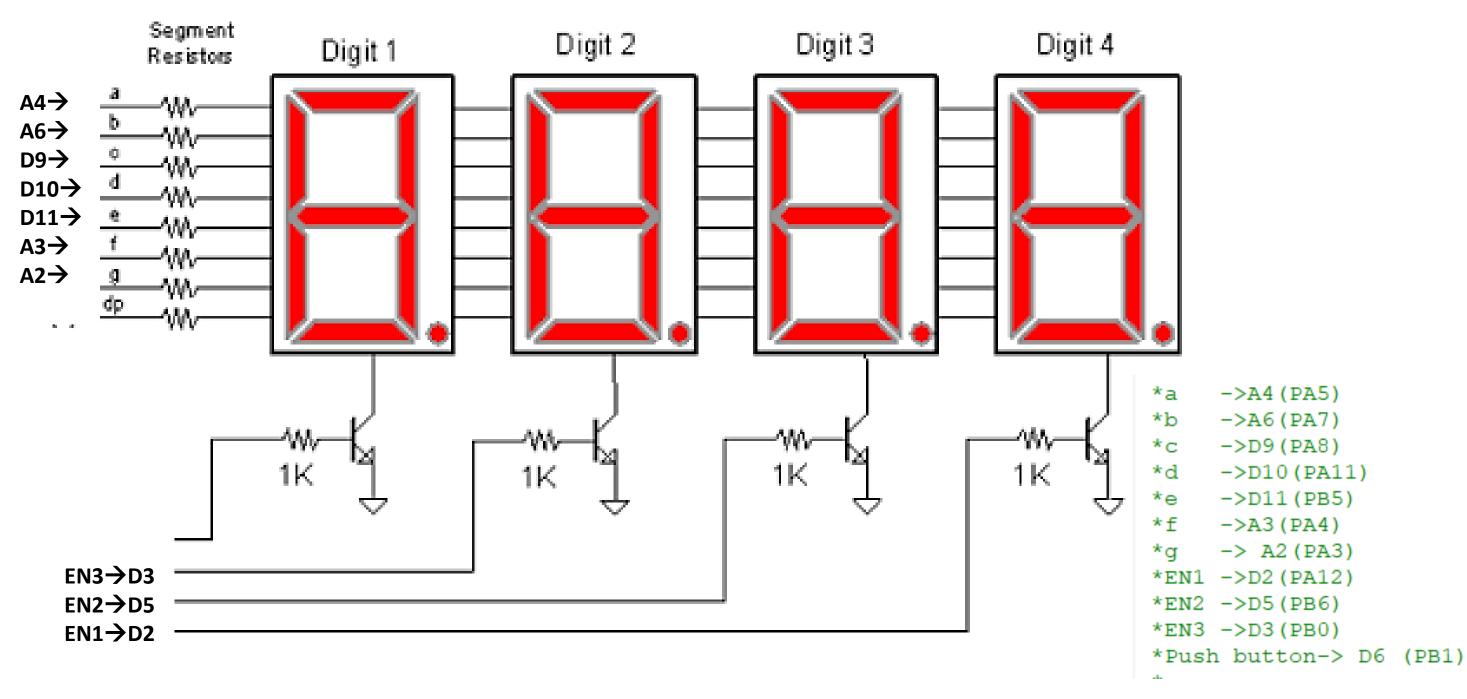




DISPLAY 7 SEGMENTOS CATADO COMUN

MULTIPLEXACION







UVAKER CENTRO DE CAPACITACIÓN DE DESARROLLO TECNOLÓGICO