Computer Organization and Architecture

Q & A

- Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache line will have memory block 7?

- Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache line will have memory block 7?

Reference order:

0
1
2
3
4
5
6
7

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3
4
5
6
7

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If LRU replacement policy is used, which cache line will have memory block 7?

Reference order:

2
1
0
3
4
5
6
7

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If LRU replacement policy is used, which cache line will have memory block 7?

0	1	2	3	4	5	6	7
4	3	25	8				

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3
2
1
0
4
5
6
7

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0	1	2	3	4	5	6	7
4	3	25	8	19			

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4
3
2
1
0
5
6
7

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4	3	25	8	19	6		

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5
4
3
2
1
0
6
7

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6
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5
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6
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0	1	2	3	4	5	6	7
4	3	25	8	19	6	16	

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6
3
2
5
4
1
0
7

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0	1	2	3	4	5	6	7
4	**3**	**25**	**8**	**19**	**6**	**16**	**35**

Reference order:

7
6
3
2
5
4
1
0

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45	3	25	8	19	6	16	35

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3
2
5
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45	22	25	8	19	6	16	35

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6
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3
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Reference order:

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4
3
1
0
7
2
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- Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests:

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0	1	2	3	4	5	6	7
45	22	25	8	3	6	16	35

Reference order:

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6
4
3
1
0
7
5

- Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache line will have memory block 7?

0	1	2	3	4	5	6	7
45	22	25	8	3	7	16	35

Reference order:

5
2
6
4
3
1
0
7

The answer is line 5!

- Consider a fully associative cache memory with 4 lines that implements FIFO cache replacement policy. For the following block requests

  2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

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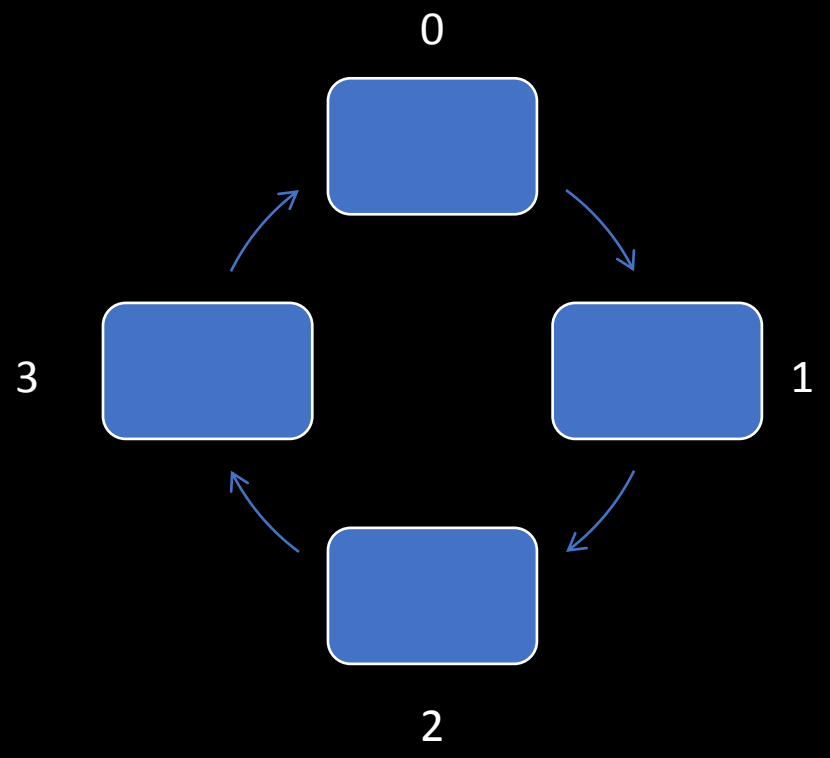
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses:

hits:



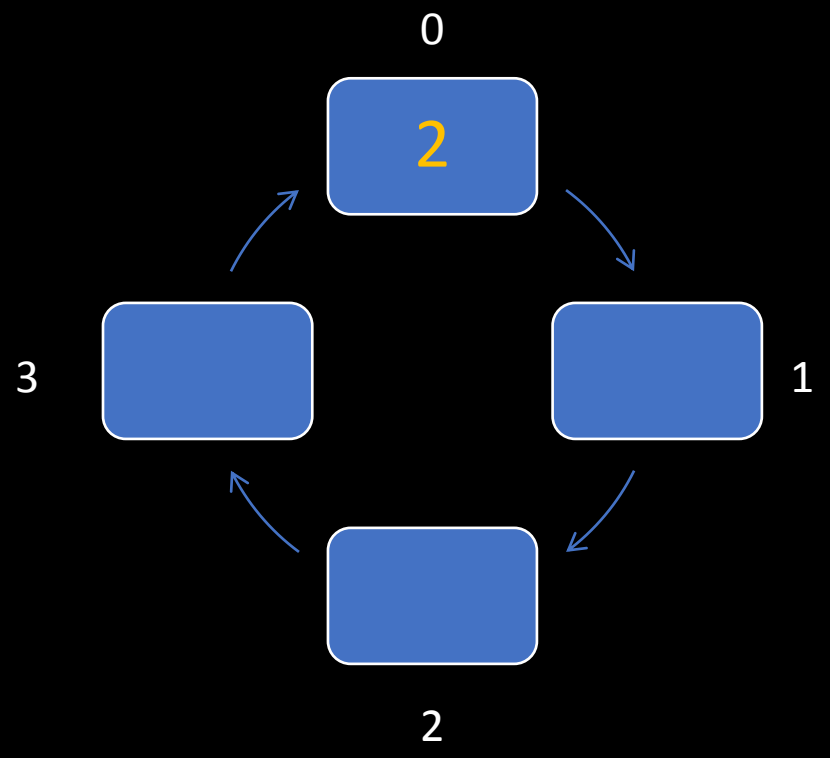
- Consider a fully associative cache memory with 4 lines that implements FIFO cache replacement policy. For the following block requests

2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 1

hits:



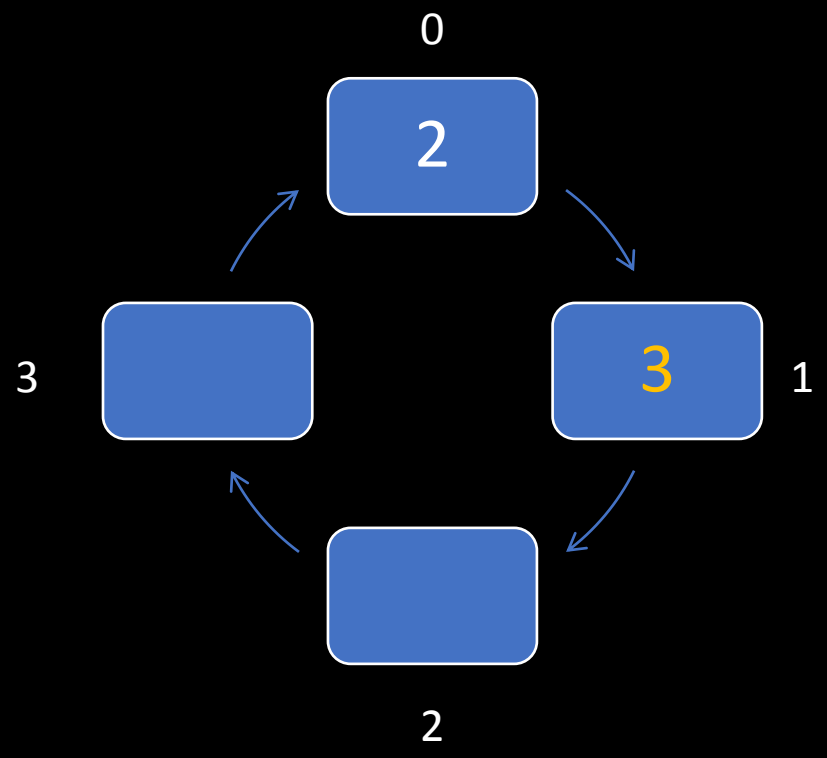
- Consider a fully associative cache memory with 4 lines that implements FIFO cache replacement policy. For the following block requests

2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 2

hits:



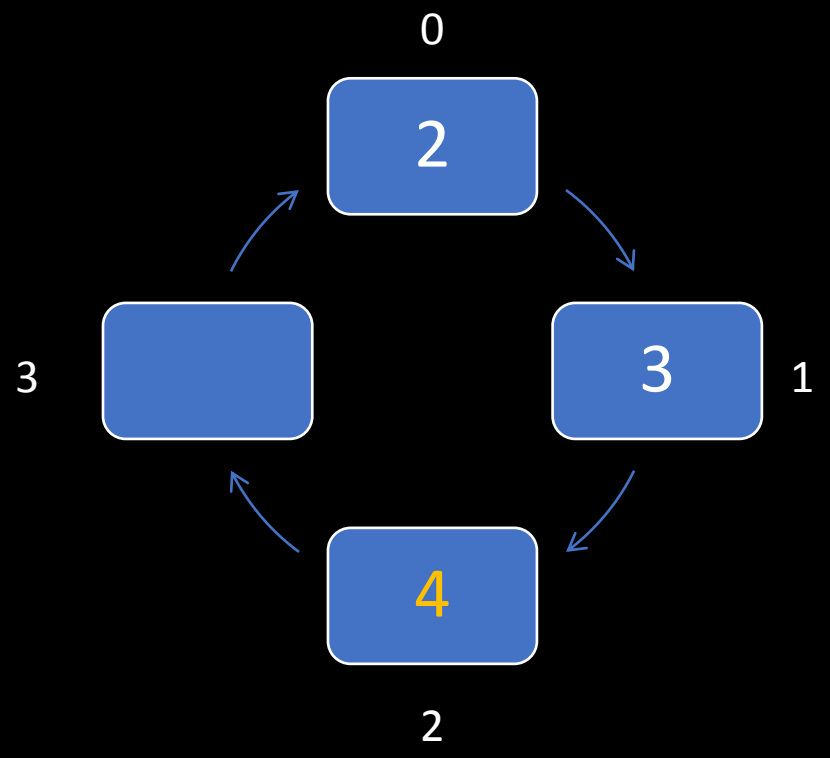
- Consider a fully associative cache memory with 4 lines that implements FIFO cache replacement policy. For the following block requests

2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 3

hits:



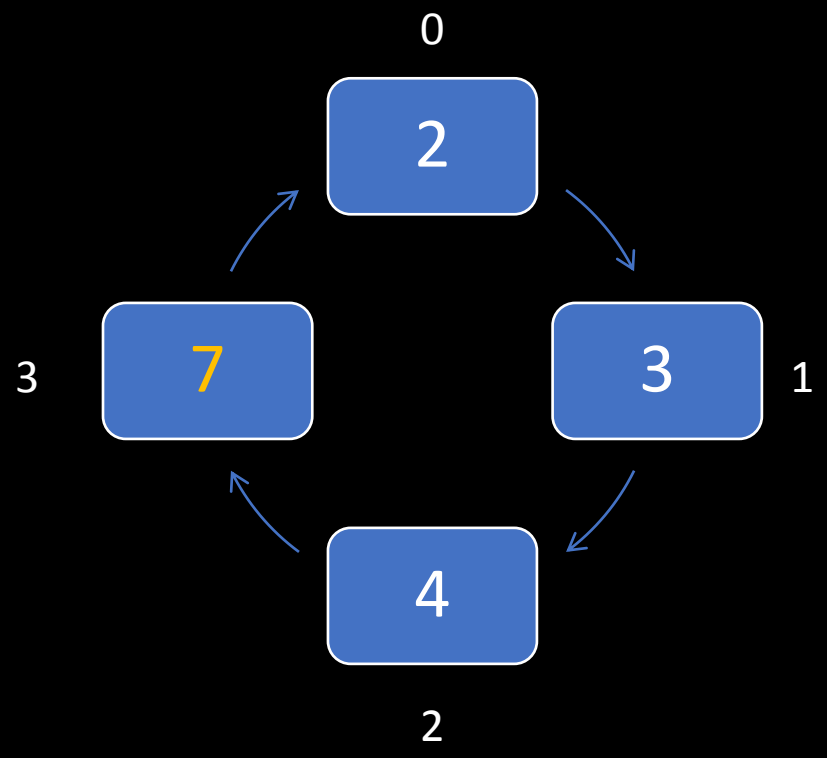
- Consider a fully associative cache memory with 4 lines that implements FIFO cache replacement policy. For the following block requests

2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 4

hits:



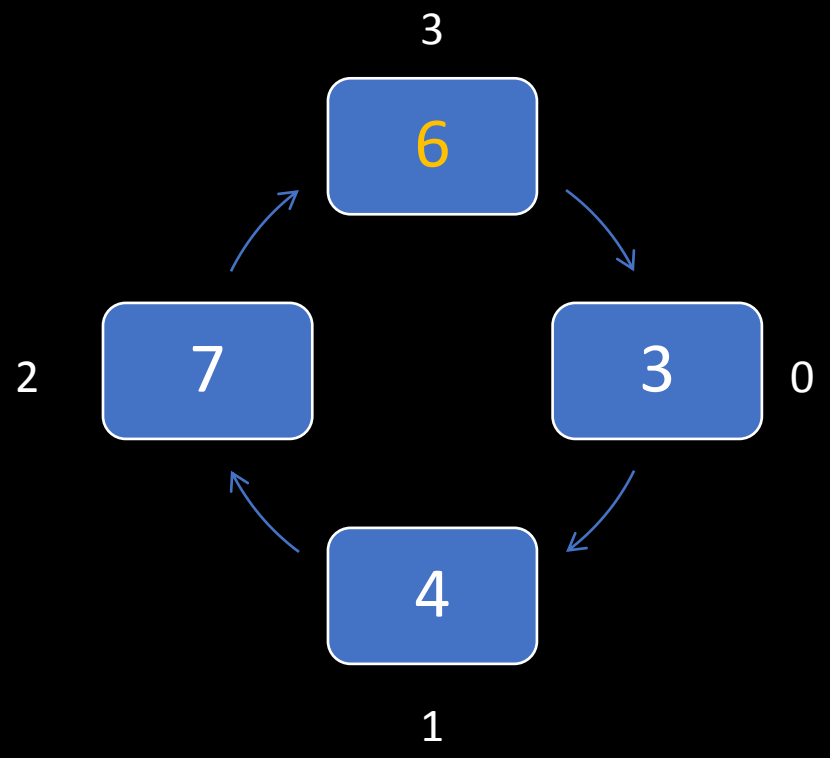
- Consider a fully associative cache memory with 4 lines that implements FIFO cache replacement policy. For the following block requests

2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 5

hits:



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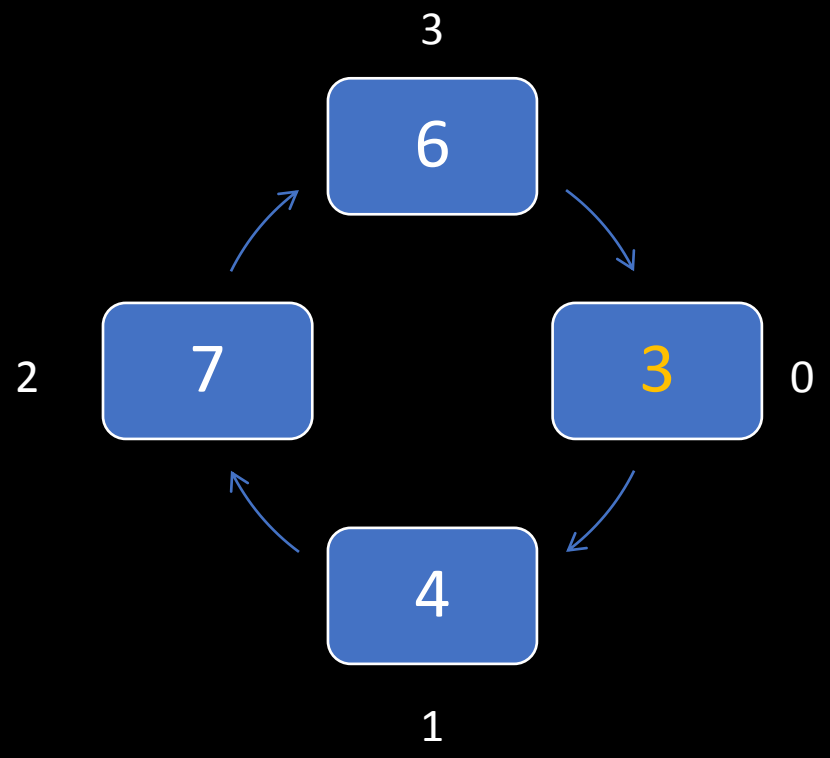
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 5

hits: 1



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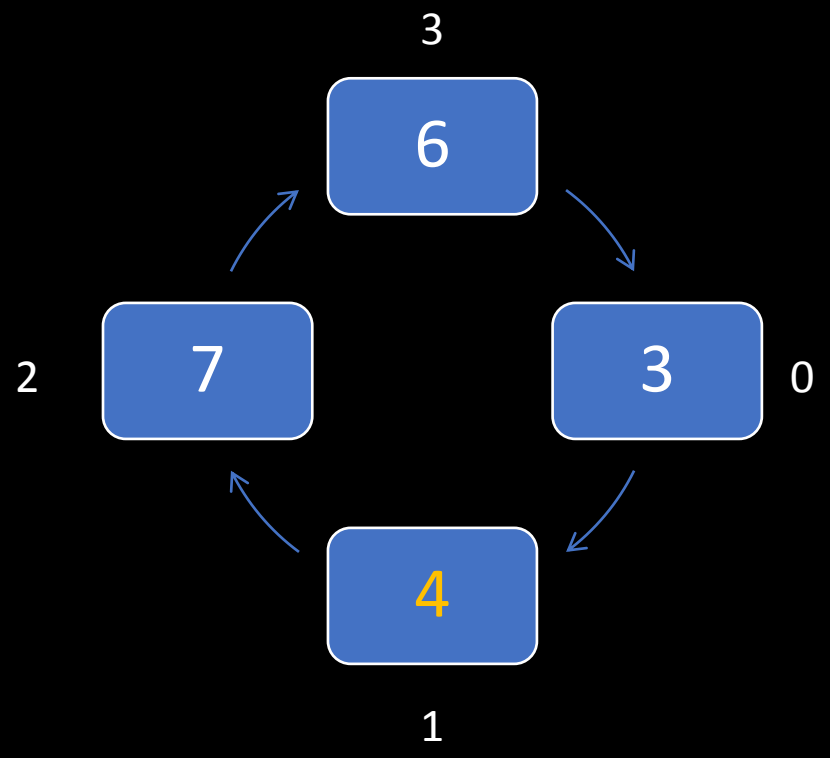
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 5

hits: 2



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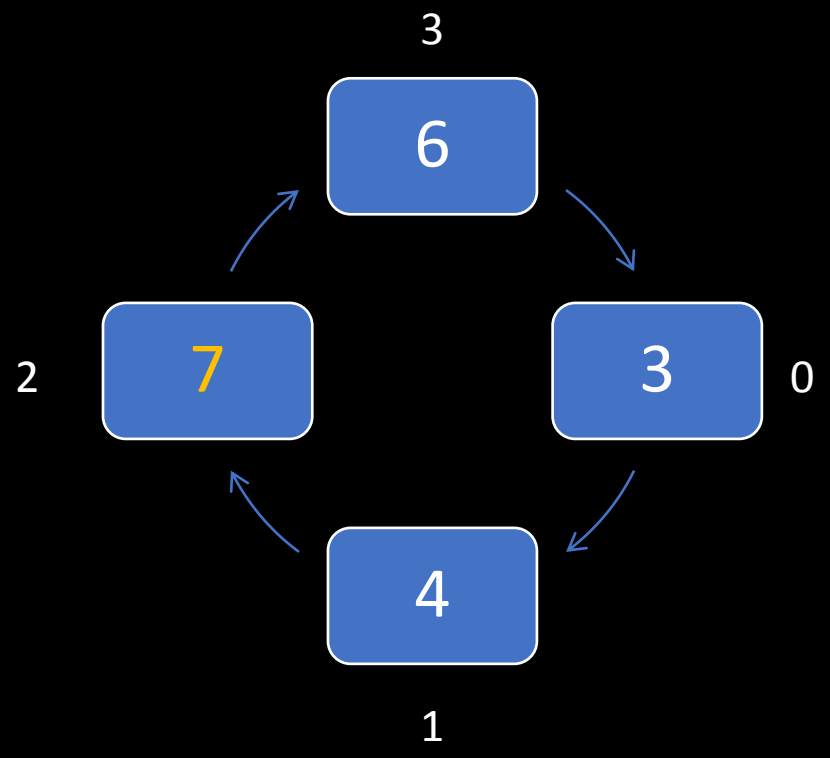
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 5

hits: 3



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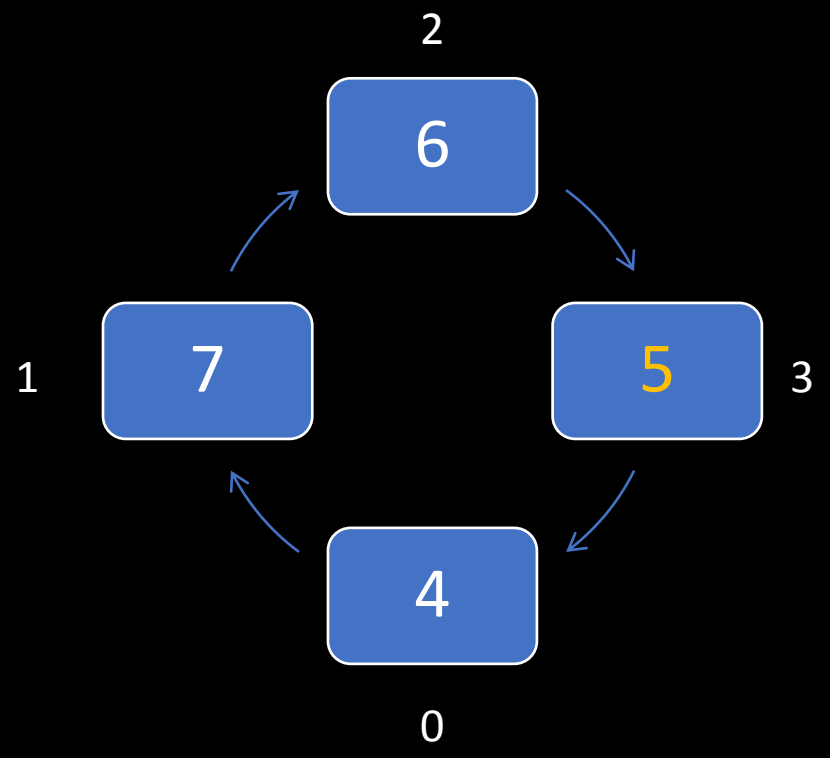
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 6

hits: 3



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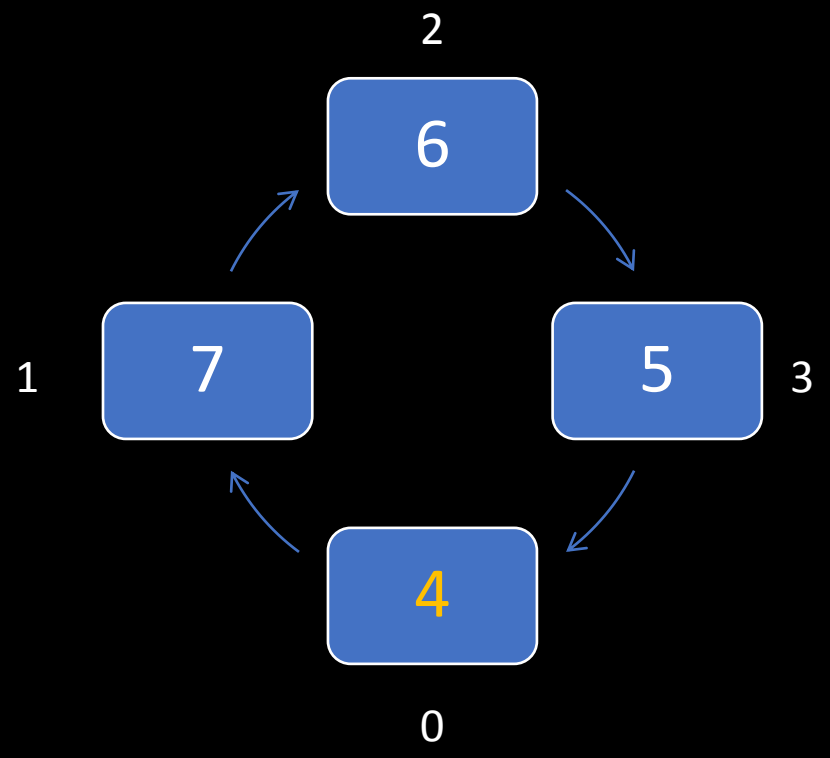
What is Miss and Hit ratio, respectively.

misses: 6

hits: 4



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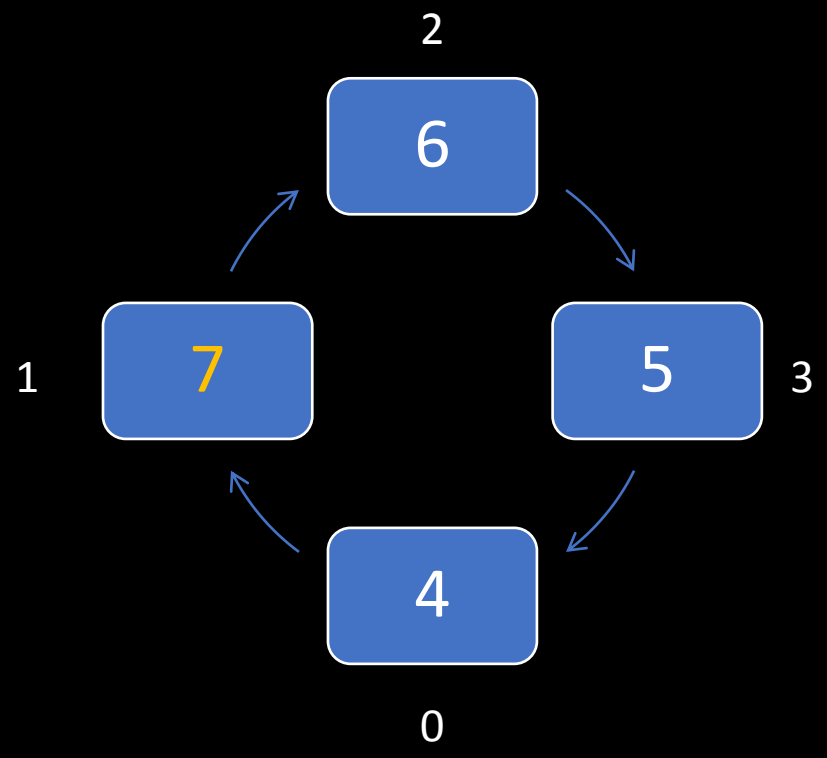
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 6

hits: 5



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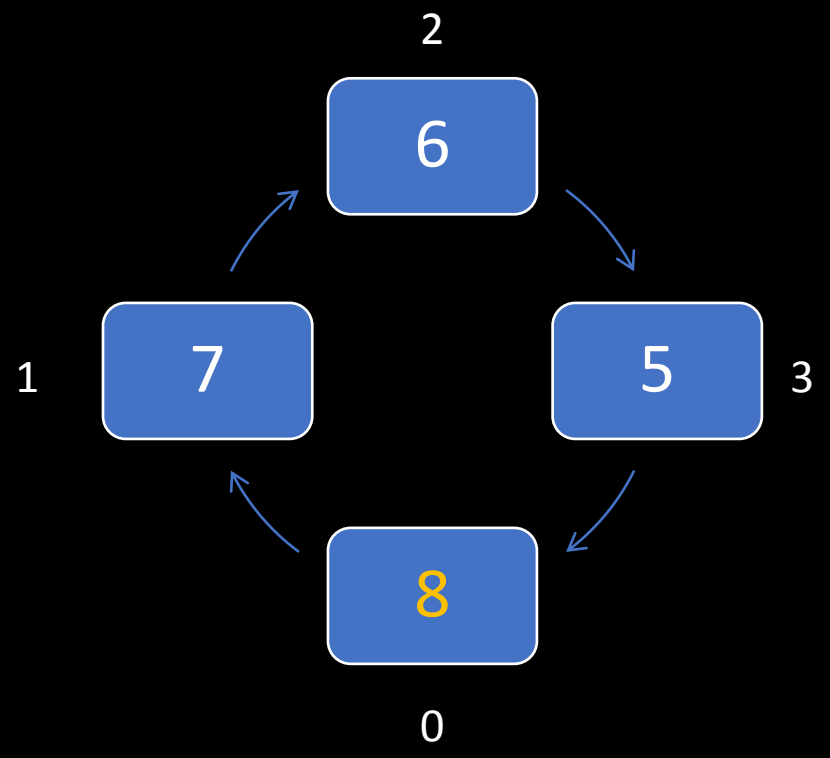
2,3,4,7,6,3,4,7,5, 4, 7, 8.

What is Miss and Hit ratio, respectively.

misses: 7

hits: 5



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$$Hit\ ratio\ = \frac{number\ of\ hits}{total\ access\ requests}$$

$$= \frac{5}{12} = 0.41666;\ 41.67\%$$

$$miss\ ratio\ = \frac{number\ of\ misses}{total\ access\ requests} = 1 - hit\ ratio$$

$$= \frac{7}{12} = 0.5833;\ 58.33\%$$